Ambipolar independent double gate FET (Am -IDGFET) logic design : methods and techniques

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Ambipolar Independent Double Gate FET (Am-IDGFET) logic design -Methods and Techniques-

Ecole Doctorale Electronique, Electrotechnique, Automatique

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Abstract

The continuous growth of global demand for semiconductor products (in a broad range of sectors, such as security, healthcare, entertainment, connectivity, energy, etc.) has been both enabled and fuelled by Moore's law and regular doubling of circuit density and performance increases. However, as CMOS technology scaling begins to reach its theoretical limits, the ITRS predicts a new era known as "Beyond CMOS". Novel materials and devices show an ability to complement or even replace the CMOS transistor or its channel in systems on chip with silicon-based technology. This has led to the identification of promising phenomena such as ambipolar conduction in quasi one- and zero-dimensional structures, for example in carbon nanotubes, graphene and silicon nanowires. Ambipolarity, in a dual-gate context (DG-FETs), means that n- and p-type behavior can be observed in the same device depending on the back gate voltage polarity. In addition to their attractive performances and the low power consumption, ambipolar double gate devices enable the development of completely new circuit structures and design paradigms. Conventional logic synthesis techniques cannot represent the capability of DG-FETs to operate as either n-type or p-type switches and new techniques must be found to build optimal logic.

The work in this thesis explores design techniques to enable the use of such devices by defining generic approaches and design techniques based on ambipolar DG-FETs. Two different contexts are tackled: (i) improving standard cell logic design with more compact structures and better performance, as well as low-power design techniques exploiting the fourth terminal of the device, and (ii) adapting conventional logic synthesis and verification techniques such as Binary Decision Diagrams or Function Classification to ambipolar DG-FETs in order to build reconfigurable logic cells. The proposed methods and techniques are validated and evaluated in a case study focused on DG-CNTFET through accurate simulations, using the most mature and recent DG-CNTFET model available in the literature.

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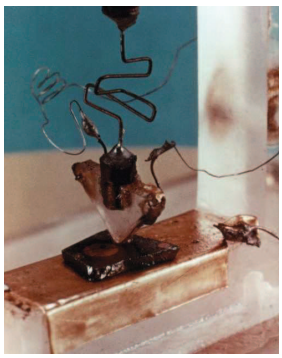
Chapter 1

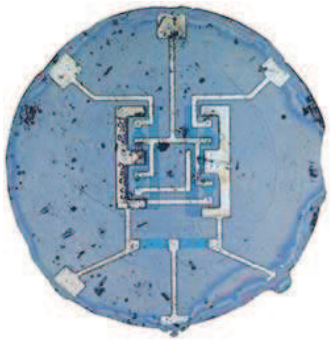
Introduction

The advent of the semiconductor switching transistor has, since the mid-20th century, resulted in the birth of mainstream information processing, consequently transforming almost all aspects of life, with no end to this development in sight. New fields such as quantum computing and bioinformatics will in the long-term future undoubtedly lead to revolutionary advances in information processing for the data deluge.

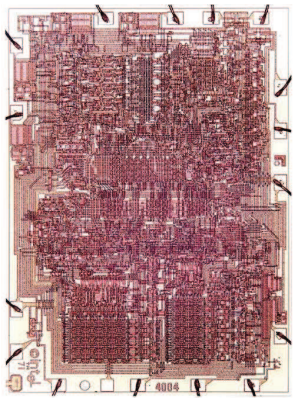
(a) Vaccum tube (1904) [1-1]



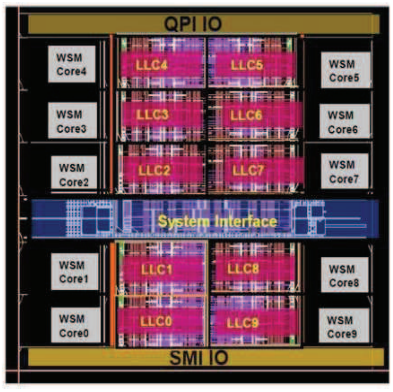
(b) First transistor (1947) [1-2]



(c) First Integrated Circuit,4 transistors (1961) [1-3]



(d) Intel 4004, 10µm process, 2300 transistors, First CPU (1971) [1-4]



(e) Intel Xeon 10-core, 32 nm process, 2.5 Billion transistors, highest transistor count in a CPU (2012) [1-5]

Figure 1-1. Electronics evolution from the early 20th century till today

For a glimpse of the short- to mid-term future, the *International Technology Roadmap for Semiconductors (ITRS)* [1-6] is one proof of the enthusiasm driving the research in the semiconductor field. The ITRS is a consortium of leaders in the fields of semiconductor research and industry, whose goal is to survey the trends of the semiconductor technology and predict its future evolution. Today, the ITRS recognizes the existence of physical limits to this

growth: electronics-based technologies cannot be scaled down beyond certain dimensions that are defined by some physical limits [1-7].

The semiconductor technology that dominates the electronics market today is the *complementary metal-oxide-semiconductor (CMOS)* technology, which is based on the utilization of complementary transistors, designated by N- and P-types and in which carriers are, respectively, electrons and holes. The challenging task of the ITRS today is to find a way to continue the scaling of CMOS technology or its fundamental replacement by other technologies promising more scaling opportunities. The efforts undertaken in this sense are reflected by the variety of processing techniques, device architectures and system designs that have been investigated in the last decade.

The candidates that are viable for a possible replacement of CMOS technology, are commonly called *emerging technologies*. These tentative solutions are based on novel materials, device physics, circuit designs etc. They share some common aspects: for instance, the dimension scaling is pushed so far, that typical device dimensions are in the range of an average-size molecule. At this scale, uncertainty becomes high and variability increases at the single device level, so that a reliable operation of the system can no longer be guaranteed. On the other hand, the accurate placement of devices with the size of single molecules challenges manufacturing and increases overall variability.

In this context, the emergence of new devices offers the opportunity to provide novel building blocks, to elaborate non-conventional techniques for reconfigurable design and consequently to reconsider the paradigms of architectural design. The ITRS Emerging Research Device (ERD) and Emerging Research Materials (ERM) chapters propose emerging technology fields for prospective research [1-8]. Two different directions are envisaged:

i) The extension of the MOSFET device to other geometries and materials, and

ii) The use of other technologies and state variables for computing.

This thesis deals with the first direction envisaged by the ITRS; to assess the relevance of new nanodevices for the semiconductor industry, it is necessary not only to invest in the maturation of the technology of nanodevices, but also in a predictive assessment of the performance of architectures and of new computing paradigms, thus requiring design tools and techniques adapted to new devices.

The novelty and contributions of this thesis consist of developing new design approaches and tools adapted to a completely new type of switching device known as “ambipolar devices”. This device possesses the property of ambipolar conduction behaviour, distinct from conventional devices and characterized by a superposition of electron and hole currents, experimentally reported in many post-silicon devices (Carbon nanotubes, Graphene, Silicon Nanowires…). Such behaviour is not exploited with conventional design techniques for digital and analogue circuits based on unipolar transistors, thus in a conventional approach

device behaviour would be modified either at manufacturing level (suppression of Schottky barriers) or at design level (connection of double gates) to convert those devices from ambipolar to unipolar behaviour. However, it has been demonstrated that the polarity of ambipolar devices, i.e., whether they are N- or P-type devices, can be controlled during the operation of the device. This represents an opportunity for new design methodologies for ambipolar circuits, and which can be addressed from several angles: standard gates or reconfigurable architectures, speed or power consumption optimization and static or dynamic logic styles. This thesis proposes several novel design techniques and methodologies based on this new type of ambipolar device in the context of a double gate structure. The proposed design approaches are initially described. Then, innovative logic blocks are derived, validated and evaluated. A physically accurate Double Gate Carbon-Nanotube FET (DG-CNTFET) device model is used, thanks to a close synergy between research teams.

This chapter is an introduction, and is organized in the following way. First, we give an overview of past decades of conventional linear scaling. Second, the state of the art of current CMOS computing devices, architectures and tools, their recent trends and their limits are outlined. Then, promising emerging technologies that may either sustain CMOS technology or replace it, as well as corresponding novel architectures and tools are described. The chapter concludes with the contributions and structure of this thesis.

1.1 Linear Scaling

Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) has been the major device for integrated circuits over the past two decades (Fig.1-2). With technology advances exploiting a natural dimension-based scalability of the device structure, silicon MOSFET based VLSI circuits have continually delivered performance gain and/or cost reduction to semiconductor chips for data processing and memory functions following an empirical observation known as Moore's Law [1-9]. Rather than a law of physics, it is merely an empirical and accurate observation of what electrical engineers, when organized properly, can do with silicon. The basic rule - which states that the number of transistors on a chip doubles every 24 months - has been the guiding principle of the high-tech industry since it was coined by Intel co-founder Gordon Moore in 1965. It predicts technological progress and explains why the computer industry has been able consistently to deliver products that are smaller, more powerful and less expensive than their predecessors - a dynamic that other industries cannot match.

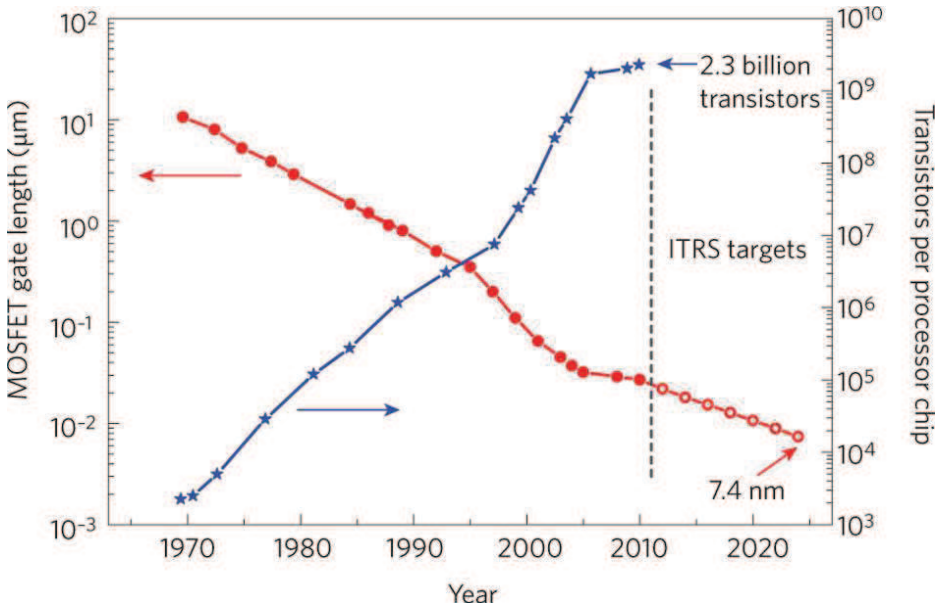


Figure 1-2. Past and projected evolution of MOSFET gate length and number of transistors per processor chip since 1970 [1-10]

Scaling is the process of miniaturizing devices while attempting to maintain electrical characteristics constant. There have been many different attempts at scaling. The main problem with miniaturization is the direct, and more importantly, indirect dependence of electrical characteristics on controllable physical parameters. This causes many non-ideal effects that hinder the performance or power consumption characteristics of devices. It is important to observe that scaling leads to a reduction of device power by a factor of α^2 and a speed up in the intrinsic delay by a factor of α (Table 1-1).

TABLE 1-1. LINEAR SCALING RULES [1-11]

Parameters	Scaling factor
Transistor length and width *(L, W)*	1/α
Junction depth *(x_j)*	1/α
Oxide thickness *(t_{ox})*	1/α
Doping concentration *(N_d, N_a)*	α
Supply voltage *(V_D)*	1/α
Drive current *(I_D)*	1/ α
Electric field *(E)*	1
Capacitance *($\varepsilon.A/t_{ox}$)*	1/α
Delay time *($\tau=C.V_D/I_D$)*	1/α
Power dissipation *($\sim V_D.I_D$)*	$1/\alpha^2$
Device density *(~1/A)*	α^2

The exponential growth of transistor density per chip means that silicon cost - computed per single IC transistor - has been constantly decreasing, making multimillion transistor systems on a single die both feasible and cost effective. While silicon costs were dominant in the early ages of the semiconductor industry, they are today in fact marginal, while *electronic*

design automation (EDA) tools, mask fabrication and circuit design costs are dominant compared to material costs. Figure 1-3 is a chart showing some of the costs involved.

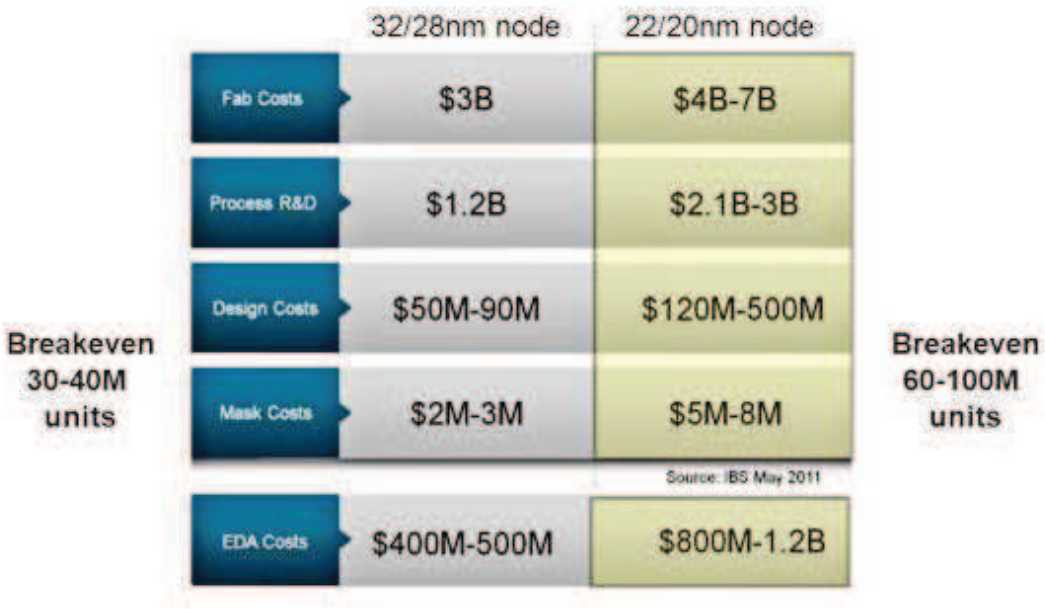


Figure 1-3. Semiconductor/EDA chart of costs [1-12]

Increased competition has led to a decrease in previously lucrative profit margins. Lowering the costs of processing and storage enabled the development of powerful software, taking advantage of the ever-increasing capabilities of the hardware. New software gives rise to new applications that in turn increase the demand for hardware. Thus, Moore's Law is driving the acceleration of computing performance (a basic measure of which is operations per second) over the entire Information Technology industry and beyond. In fact, the entire semiconductor industry is striving to track Moore's Law: the Semiconductor Industry Association puts together periodic "Technology Roadmaps" that are defined then closely followed by the chip industry and academia. These roadmaps, designed by technology working groups made up of leading industry experts, define in detail the course for future developments over a 15-year period, driven by the desire to continue the past trends of Moore's Law including device research, process integration, semiconductor materials, circuit design, interconnect issues, packaging, EDA tools, etc. In this way, Moore's Law has become a self-fulfilling prophecy.

1.2 CMOS computing

As device scaling continues into the 21st century, it turns out that past trends in growth, doubling circuit density and increasing performance by around 40% for each new technology generation [1-13] cannot be maintained by conventional scaling. This section surveys the most important issues that need to be addressed with the latest milestones at different research levels.

1.2.1 Device

In this section, we briefly review the issues encountered by scaling down the MOSFET channel length below 100 nm and the short-term solutions that have already taken place; Silicon on Insulator technology (SOI) and Multigate structures.

1.2.1.1 Sub-100-nm CMOS

To understand the behavior of sub-100-nm devices, numerous studies have been conducted in nanoscale MOSFETs. The main challenges encountered by bulk MOSFETS in the submicron and deep submicron region for low-power, low-voltage applications are the short-channel effects, gate induced drain leakage, threshold voltage roll-off, drain-induced barrier lowering (DIBL), hot carrier effects, poly depletion effects, band-to-band tunnelling (BTBT), and so forth. By investigating different issues of nanoscale MOSFETs, one can analyze where the problems occur (gate, channel, drain/source, and substrate).

Channel: (i) *Sub-threshold leakage current* is the weak inversion conduction current, which is dominated by the diffusion current flowing between the drain and source when $|V_{GS}| < |V_{th}|$. It is the main contribution to standby leakage power dissipation. (ii) *Threshold voltage variation* due to the reduced channel length represents V_{th} roll-off. Further V_{th} reduction, caused by increasing drain voltage, is described by drain-induced barrier lowering (*DIBL)*. Also, charge-sharing effect between the channel depletion region and source/drain depletion regions makes a transistor require a lower gate voltage to deplete the substrate beneath the gate dielectric, decreasing V_{th} [1-13, 1-14, 1-15]. (iii) *Carrier mobility degradation* is a result of the high channel doping level, [1-16] and the situation worsens with the applied electrical field, due to phonon scattering [1-17], and by the scattering at the Si/SiO_2 interface between the channel and the gate oxide [1-18]. (iv) *Hot carrier effects (HCEs),* especially highly accelerated carriers near the drain region, can generate new electron-hole pairs by collision with the silicon atoms, called “impact ionization” which causes charges to become trapped in the gate oxide. This causes threshold voltage shifts and therefore the device becomes unstable and can even fail [1-19, 1-20].

Gate: (i) *Direct tunneling gate leakage current* increases exponentially due to quantum mechanical tunneling. This leakage not only increases standby power dissipation but also limits proper device operation [1-21]. These problems can be solved by replacing the conventional SiO_2 gate oxide material with higher permittivity (high-k) gate dielectric materials such as hafnium-based oxides [1-22], which allow a physically thicker dielectric layer with the required (relative to SiO2) Equivalent Oxide Thickness EOT [1-23] to be used. (ii) *Gate depletion:* Poly-Si (doped N^+ or P^+) forms a SiOx layer at the interface with gate dielectric. There remains a high probability for Fermi-level pinning to occur [1-24]. Metal (rather than polysilicon) gates have been re-introduced to mainstream CMOS technology, in order to avoid variation in V_{th}.

Drain/Source: (i) *Parasitic resistance*: The ideal scaling theory [1-25] predicts that the channel resistance, R_{chan}, should remain constant as the channel length dimensions are reduced. However, the ideal scaling theory has not been followed in the last forty years and will not likely be followed in the future [1-26]. Higher performance is achieved by higher current drive capability and, therefore, R_{chan} has been dramatically decreased as the technology has scaled. Furthermore, the decreasing of the junction depth [1-27] and the use of smaller contacts [1-28] has led to a large increase in parasitic resistances. As a result the ON current characteristic of the transistor, I_{ON}, can be significantly degraded [1-29].

(ii) *Parasitic capacitance*: As MOSFETs enter into the nanoscale regime, the gate capacitance does not decrease in proportion to the gate length reduction due to relatively increased parasitic capacitance. Therefore, in order to sustain performance improvement from scaling, parasitic capacitance reduction techniques are required [1-30].

Substrate (bulk): (i) *GIDL current*, also called surface BTBT current, has become one of the major OFF-state leakage current components in state-of-the-art MOSFETs. When the drain of an n-MOSFET is biased at the supply voltage (V_{DD}) and the gate is biased at either zero or negative voltage, a depletion region is formed under the gate and drain overlap region. In the same way as the BTBT current, if the high electric field is formed in the narrower depletion region as a result of the reverse-bias between channel and drain, a significant amount of surface BTBT current flows through drain to substrate junctions due to twisting of bandgaps [1-31, 1-32]. (ii) *Reverse-biased junction leakage current (I_{REV})* is the current flowing between the source/drain (S/D) and the substrate through the parasitic reverse-biased *PN*-junction diode in the OFF-state MOSFET. It mainly consists of the diffusion and drift of minority carriers near the depletion region edge and the generation of electron-hole pairs in the depletion region of the reverse-biased *PN*-junction. The amount of I_{REV} depends on the junction area and doping concentration. In nanometer devices, higher channel and S/D doping with shallow junction depths are required to minimize SCEs, otherwise there is significant increase in BTBT current [1-32].

1.2.1.2 Evolution of MOSFET

With so many CMOS issues, there is little room left for scaling, in particular for oxide thickness. This means that the gate control of the channel cannot be made much stronger, and consequently the channel length cannot be made much shorter lest the drain exerts a proportionately large control leading to excessive short-channel effects and high OFF-state transistor leakage. New approaches are needed to allow the continued reduction of channel length in future technologies. Silicon On Insulator technologies [1-33] and multi-gate structures appear at present to be the most promising approaches [1-34].

a. *Silicon on Insulator*

SOI wafers are now viewed as the most important emerging wafer engineering technology for use in leading edge CMOS IC production during the next 3-5 years [1-35]. The advantages of SOI technology come from its buried oxide (BOX) layer (Fig. 1-4). SOI transistors are classified into two types; "partially depleted PD-SOI," if the silicon film (typically 100 nm or more) on the BOX layer is thicker than the depletion region depth beneath the gate oxide, and "fully depleted FD-SOI," if the body (silicon film) thickness is thin enough (typically 50 nm or less) or the doping concentration of the body is low enough to be fully depleted (figure 1-4). FD-SOI transistors have superior advantages over PD-SOI transistors in terms of extremely low sub-threshold slope (<65 mV/decade), no floating-body effects, and low threshold voltage variation with temperature (2-3 times less than bulk transistors). However, FD-SOI transistors are also more sensitive to process variations such as the silicon film layer variation, which results in threshold voltage fluctuation, such that PD-SOI devices were commercially introduced first. With careful device design and advanced process techniques, Fully Depleted Ultra Thin-Body SOI (FD UTB SOI) devices are considered as one of the best scaling options.

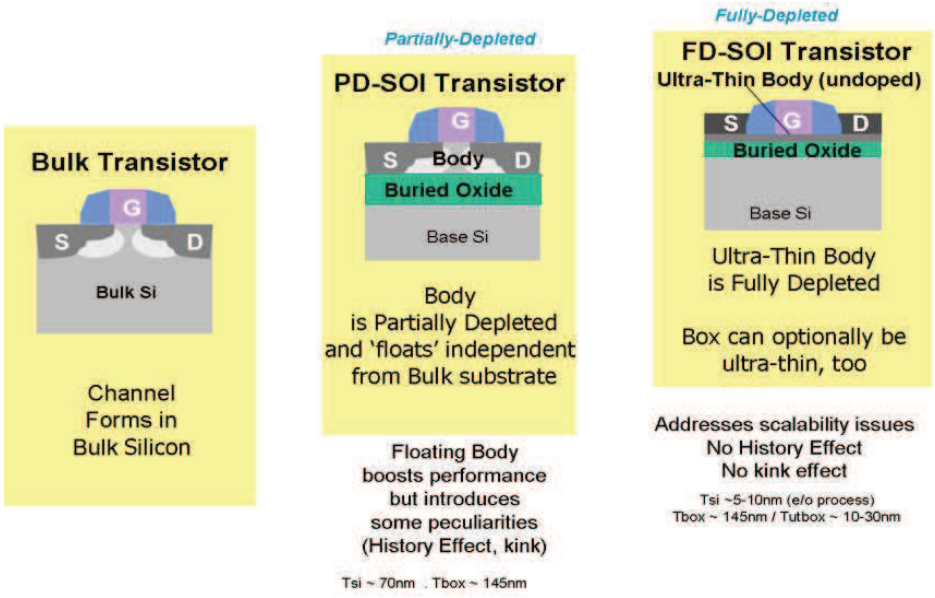


Figure 1-4. FD-SOI Transistors vs. Bulk and PD-SOI Transistors [1-36]

With the reduction of the parasitic capacitances, mostly as a result of the reduced drain/source junction capacitances, SOI devices yield improved switching speed and reduced power consumption. The operating speed is also improved since the isolated channel from substrate bias prevents the increase in a threshold voltage of stacked SOI transistors. In addition, the perfect lateral and vertical isolation from substrate provides latchup and inter-device leakage free CMOS technology, reduction in various interferences, and better soft error immunity. Moreover, SOI technology offers tighter transistor packing density and simplified processing [1-33]. Another important merit of SOI technology is that it provides

the cornerstone for new device structures such as Multi Gate Field-Effect Transistors (MuGFETs), which include more than one gate into a single device. Some examples are presented in the next part of the section below.

b. ***Multi Gate devices***

There are different structures of Multi Gate MOSFETs. Several examples are shown in Figure 1-5 as presented in [1-37]. Perhaps the best known example is the FinFET [1-38]. The FinFET consists of a thin silicon body (the fin) and a gate wrapping around its top and two sides. The ITRS [1-39] considers it to be the candidate to replace planar MOSFETs for its capability to resolve many aforementioned issues caused by short channel effects and because a FinFET is *relatively* easy to fabricate. FinFETs can be made on either bulk or SOI substrates, creating the bulk FinFET (Fig. 1-5(a)) or the SOI FinFETs (Fig. 1-5(b)) respectively. In some FinFET processes the oxide hard mask on top of the fin is not removed, creating the double-gate FinFET (Fig. 1-5(c)). In Double-gate FinFETs the top surface of the fin does not conduct current, whereas in Triple-gate FinFETs (Figs. 1-5(a) (b)) the side surfaces and the top surface all conduct current. Another example of MuGFET is the Gate-All-Around (GAA) device (Fig. 1-5(d)). It consists of a pillar-like body surrounded by the gate dielectric and the gate. The Nanowire MOSFET [1-40] is one example of GAA devices. Depending on the fabrication process, the channel may be oriented either vertically [1-41] or horizontally [1-40]. Optionally, a FinFET can have two separated gates that are independently biased. This can be achieved by removing the top portion of the gate of a regular FinFET using chemical mechanical polishing, forming the independent Double-gate FinFET (Fig. 1-5(e)) [1-42]. Independent Double-gate MOSFETs may also be made as planar devices [1-43]. The Planar Double-gate SOI (Fig. 1-5(f)) is essentially a Planar SOI MOSFET with a thin buried oxide (labeled as BOX). A heavily-doped region in silicon under the buried oxide acts as the back gate. Unlike the front gate, the back gate is primarily used for tuning the device threshold (V_{th}). The buried oxide is usually thick such that the back gate cannot induce an inversion layer at the back surface. V_{th} tuning can be used to compensate for variability in IC manufacturing from chip to chip or even circuit to circuit within the same chip. Doing so improves the IC speed and power consumption. It can also be used to dynamically raise or lower V_{th} circuit by circuit within a chip in response to the need for less leakage or more speed. This is a very effective means of managing power consumption.

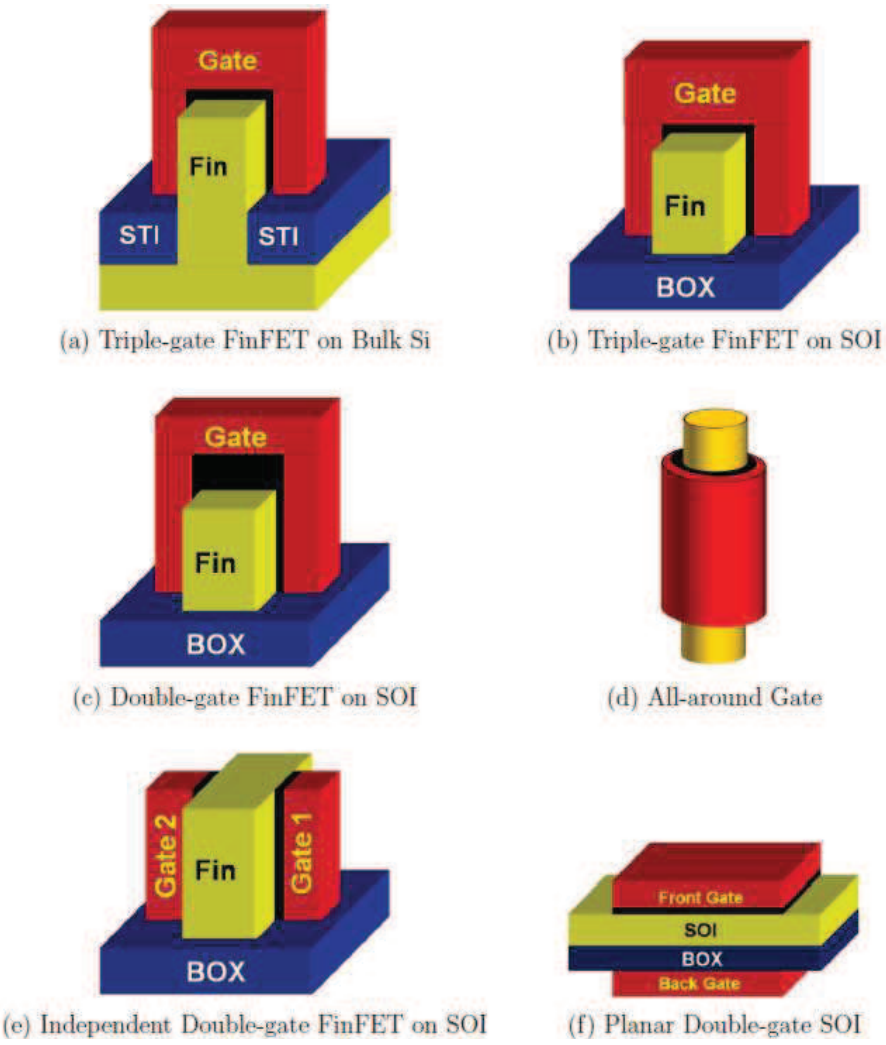


Figure 1-5. Various examples of Multi Gate MOSFETs [1-37]

The main advantage of multi-gate devices is the improved short channel effects. Since the channel (body) is controlled electrostatically by the gate from several sides, the channel is better controlled than in the conventional transistor structure and undesirable leakage components are reduced. Improved gate control also provides lower output conductance, in the current saturation region, which leads to greater voltage gain, beneficial to analog circuit performance as well as to digital circuit noise tolerance.

The second advantage of multi-gate devices is the improved on-state drive current (I_{ON}) and therefore faster circuit speed thanks to the reduction of channel . In addition, a promising multi-gate structure, the FinFET, provides a larger channel width with a small footprint in area, which also raises I_{ON}. Finally, the third advantage is the reduced manufacturing variation. In the absence of channel dopants, the effect of random dopant fluctuation (RDF) is minimized [1-37].

1.2.1.3 Conclusions

In this section we reviewed current CMOS technology devices and their evolution. Due to dramatic CMOS scaling, many issues have emerged mostly because of the Short Channel Effect (SCE). To improve SCE and allow future reduction of channel length, new approaches have already been implemented and proved their efficiency. Silicon On insulator Technology and Multi Gate structures are the most promising approaches. Indeed, SOI wafers are now considered among the most important emerging wafer engineering technology for use in leading edge CMOS IC production during the next 3-5 years thanks to improved switching speed and reduced power consumption over conventional Bulk-CMOS. When it comes to MuGFETs, several examples were illustrated in this section, the main advantage being a better electrostatically controlled channel (body) from multiple sides of the gate. This offers better I_{ON} and decreases undesirable leakage.

1.2.2 Architectures

In order to keep following Moore's law and to achieve the computing capacities necessary for future software applications, it is today widely recognized that Systems-on-Chip (SoC) will move initially towards Multi Processor Systems-on-Chip (MPSoC), then towards reconfigurable platforms. These systems will be used in the majority of solutions and in particular for high-performance computing (analysis and modeling of complex phenomena, advanced human-machine interaction) and for low-power mobile systems (sensor networks...).

1.2.2.1 Many-core architectures

The emergence of many-core architectures is an established industry trend. High-end microprocessor architectures are moving to a many-core format. Dual-core, quad-core and eight-core products are currently available commercially chips. Indeed, Intel announced that its 8-core Nehalem-EX will be pushed aside as the chip maker's fastest server chip, conceding the performance crown to Westmere-EX, a 10-core Xeon processor in 2011-2012. Several other companies are now producing many-core like devices that some are calling “next generation FPGAs.” Specifically, they are implementing FPOA (“Field Programmable Object Arrays”) technology, consisting of arrays of “objects” which are simple processors and other support objects such as memory [1-44]. Likewise, many ASIC / embedded SoC systems are taking on a many-core like configuration. These many-core architectures utilize the complexity obtained from scaled CMOS while obtaining more equitable use of on-chip devices, and at the same time mitigating heat management and reliability problems. It is estimated that there is headroom for perhaps an order-of-magnitude improvement, relative to single-core processors, in these performance metrics as more elementary processors are added [1-45]. Recently, according to Tilera, its new chips, which are being offered in 36-core, 64-core, and 100-core flavours (Fig.1-6), deliver a 10-fold performance-per-watt advantage over

Intel's Sandy Bridge CPUs, ultimately reducing the total cost of ownership by around 50 percent [1-46].

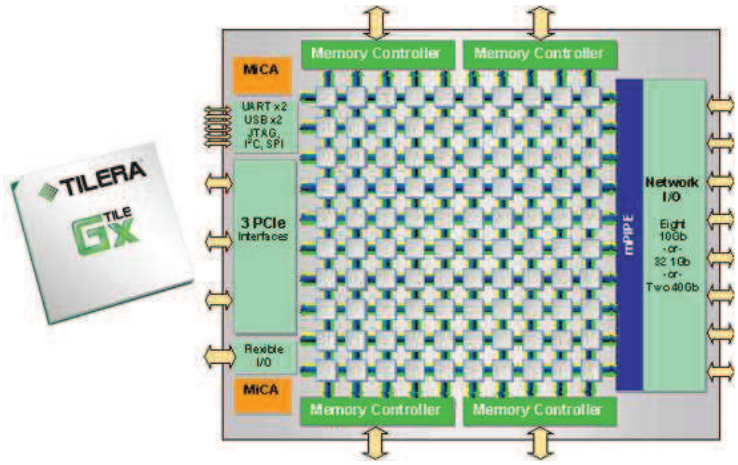


Figure 1-6. Raw architecture as an example for CMOS many-core regular architecture: Tile-Gx100 processors [1-47].

Such large many-core architectures raise several issues that represent the topics of many research fields. On the one hand, the communication between the different cores can be the bottleneck to be addressed in order to avoid performance degradation due to signal delay or congestion. The network-on-chip (NoC) paradigm solves this issue in a very efficient way [1-48] by providing both the hardware to interface the cores and the communication protocol for the network. On the other hand, there is an issue at the software and algorithmic level: given such a large number of cores, it is necessary to optimize the task management by compiling the software properly in order to maximize the performance, improve the yield and reduce the power supply.

1.2.2.2 Reconfigurable Architectures

The first approach for logic reconfigurability was the introduction of gate arrays, which were basically NAND gates that the designer could interconnect with specific mask layers as needed to generate any desired logic function [1-49]. The introduction of Programmable Logic Arrays (PLAs) in the 1980s went further by using AND-OR logic planes and by replacing the application-specific interconnect layer approach with user-programmable (i.e. after manufacturing) connections to have a really programmable solution. Programmable Array Logic (PAL) devices were a subsequent improvement in performance and cost over the PLA structure. Today, these devices are collectively called Programmable Logic Devices (PLDs), while Complex PLDs (CPLDs) are a collection of multiple PLDs with programmable interconnections [1-50]. Recently, Field Programmable Gate Arrays (FPGAs) have emerged as a platform of choice for optimized hardware realization of computation intensive algorithms. Many different architectures and programming technologies have evolved to provide better designs that make FPGAs economically viable and an attractive alternative to application specific integrated circuits (ASICs).

a. *Modern FPGA structure*

A typical modern FPGA (Fig. 1-7) provides the designer with Configurable Logic Blocks (CLB) that contain the pool of combinatorial blocks and flip-flops to be used in the design. In addition, vendors acknowledge the fact that logic is often used in conjunction with memory, and typically include variable amounts of static Random Access Memory (RAM) inside their chips. Clock conditioning has also become commonplace, and support in the form of Delay Locked Loops (DLLs) and Phase Locked Loops (PLLs) is also provided inside the same silicon chip. Finally, an FPGA chip needs to be easily interfaced to other chips or external signals, so FPGA vendors have invested a great deal of effort in enhancing the flexibility of the input/output blocks behind the chip pads. Each pad can serve as an input, an output, or both. The list of supported electrical standards is extensive, and novel techniques for maximizing bandwidth, such as clocking data using both edges of the clock, are widely supported.

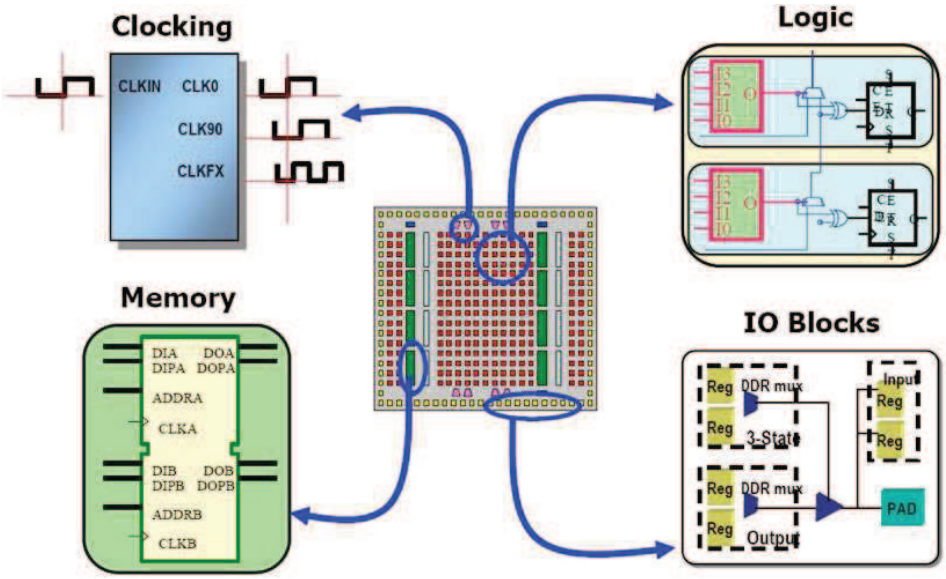


Figure 1-7. Internal structure of a generic FPGA (courtesy Xilinx, Inc.) [1-49]

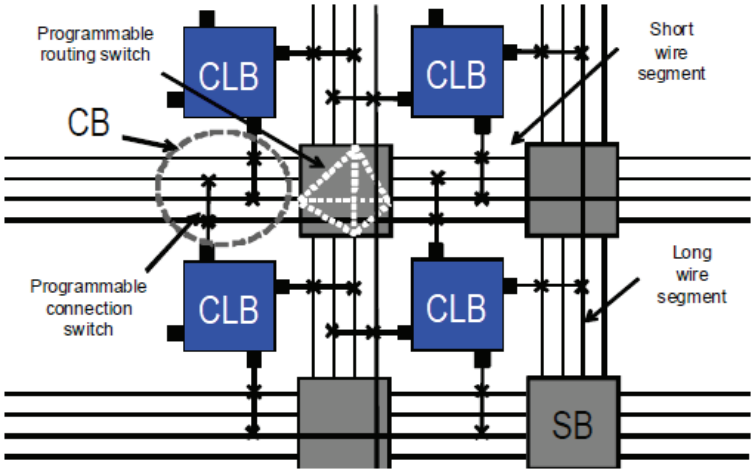


Figure 1-8. Routing organizations in an island-style FPGA [1-51]

All the components shown in figure 1-7, however, typically account for less than 22% of the silicon inside an FPGA chip [1-52]. Large amounts of resources are given over to programmable interconnect and auxiliary circuits, shown in figure 1-8, which 'program' the generic blocks to become a well-defined piece of logic. This part of FPGAs consumes most of the die area (nearly 80%) as shown in figure 1-9. As a result, this limits drastically their use in large volume manufacturing. More details about FPGAs constraints are illustrated below.

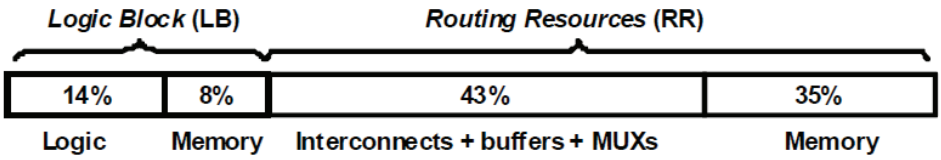


Figure 1-9. Field Programmable Gate Arrays area repartition per block [1-53]

b. ***FPGA limitations***

In addition to consuming most of the die area, programmable routing also increases the total path delay in FPGAs. In [1-54, 1-55], interconnect delays are estimated to account for roughly 80% of the total path delay. Furthermore, power consumption measurements in some commercial FPGAs have shown that programmable routing causes more than 60% of the total dynamic power consumption [1-56, 1-57, 1-58]. Finally, it is commonly admitted that FPGAs are over 10 times less efficient in logic density, 3 times larger in delay, and 3 times higher in total power consumption than cell-based implementations [1-59]. Hence FPGAs have traditionally been more successful in high-end, low-volume applications, with ASICs taking a leading role for high-volume applications. With Moore's law, however, the line between high-end and low-end applications is continuously shifting, and FPGAs are increasingly used in domains which used to be dominated by ASICs.

1.2.2.3 Standard Cells

Standard cell libraries are considered as the underlying fabric on which all architectures are based (ASICs in particular, but also – with extra levels of structuration - manycores and FPGAs). Standard Cell-based design has been a mainstay of the semiconductor industry since many decades. It enables the design of complex multi-million gate computing systems from single-function ICs (of several thousand gates). Standard cell methodology is an example of design abstraction, whereby a transistor-level gate layout is encapsulated into an abstract logic representation (such as a NAND gate).

A *standard cell library* is a collection of low-level logic functions such as AND, OR, INVERTER, flip-flops, latches, and buffers. These cells are realized as fixed-height, variable-width full-custom cells. The cells are typically optimized full-custom layouts, which minimize delay and area. A complete group of standard-cell descriptions is commonly called a technology library. Commercially available Electronic Design Automation (EDA) tools use the technology libraries to automate Synthesis, Placement, and Routing (SPR) of a digital ASIC. "Standard cell" falls into a more general class of design automation flows called cell-

based design. Structured ASICs, FPGAs, and CPLDs are variations on cell-based design. From the designer's standpoint, all share the same input front end: an RTL description of the design. The three techniques, however, differ substantially in the details of the SPR flow and physical implementation.

The designer's challenge is to minimize the manufacturing cost of the standard cell's layout (generally by minimizing the circuit's die area), while still meeting the cell's speed and power performance requirements. Thus, design flows based on standard cell libraries strongly depend on the richness of the library [1-60, 1-61], on the complexity of gates [1-62, 1-63], on their logic style used [1-64, 1-65] and the structures of gates themselves [1-166, 1-67]. Among the goals of this thesis work is to define a design methodology to build logic circuits with more compact logic structures and afford low-power design techniques using novel technology devices.

1.2.2.4 Conclusions

To respond to the growing demand of software technology and the continuous integration capacity of billions of transistors on a single die, we showed in this section that current CMOS architectures seem to converge toward two main approaches: many-core architectures and reconfigurable architectures. In [1-168], S. Borkar from Intel's Lab predicts that many-core architectures with hundreds to thousands of small cores will deliver unprecedented computing performance in an affordable power budget, as well as providing resiliency to combat variability and reliability. However, there are still many challenges to face, especially at the software level given such a large number of cores. Concerning reconfigurable architectures, the FPGA is a structure based on a hierarchical and homogeneous arrangement of logic blocks. While highly flexible, it does suffer from area, power and delay penalties (with respect to ASIC solutions) due mainly to the programmable routing part. Today, in order to overcome its limitations, FPGAs tend towards heterogeneity at the design level by adding of various logic blocks (DSPs, memories blocks, etc.) as well as at the technology level, by the co-integration of non-volatile memories (flash, MRAM, PCRAM, ReRAM ...) [1-69, 1-70, 1-71]. While the main issue with flash memories is the high programming voltage, resistive non-volatile memories appear to be an attractive alternative to SRAM, especially since the technology fabrication is progressing toward maturity.

1.2.3 EDA tools

The main purpose of Electronic Design Automation (EDA) tools is to explore means for designing and fabricating electronic circuits. It comprises several levels; i) TCAD for process and device modelling, ii) Floor planning and place and route for physical level design iii) behavioural modelling, electrical simulations and system level simulations for architectural design and so forth. It also covers many phases of the design process, including many forms of verification (geometrical and electrical design rule checking, several types of simulation)

and various aspects of design synthesis (generation of masks from layout, automatic placement and routing, logic synthesis and optimization) [1-72, 1-73, 1-74].

Among various methods and techniques utilized by EDA tools, we briefly resume two logic synthesis techniques which represent the cornerstone for many digital circuits, and which were used as a starting point in this thesis logic design based on emerging devices. The two methodologies are: Functions classification approach and Binary Decision Diagrams (BDDs).

1.2.3.1 Function Classification

The linear classification of Boolean functions is meaningful for two reasons: (i) equivalent functions have similar properties (e.g. Hamming weight distribution in error-correction coding, nonlinearity in cryptography), and (ii) the number of representatives is much lower than the number of Boolean functions [1-75, 1-76, 1-77].

Even with a moderate number of input variables, circuits generate very large truth tables. A more compact representation of the circuit is possible by using a mathematical expression called a Boolean switching function. Moreover, the output vector of the truth table may be encoded as an integer for an even more compact representation [1-78].

There are several ways of encoding this vector as an integer such as an octal number, hexadecimal and decimal. Hurst, et al. indicated in [1-79] that although encoding provides a compact representation of the functions, it does not "give any direct indication of Boolean functions of similar structure or complexity." A classification system can be used to group functions together based on specific properties, and also provide an even more compact representation of these Boolean functions.

Using classification, all 2^{2^n} Boolean functions can be considered through a small number of representative Boolean functions where n is the number of inputs. In other words, there are approaches to group Boolean functions according to some specific property [1-79, 1-80, 1-81, 1-82, 1-83]. Then, if one considers a representative Boolean function of a given class as a generic black box circuit, it could be used as a building block for all Boolean functions within that class [1-78]. For the logic synthesis process, Boolean function classification is very useful for the matching phase performed during technology mapping [1-84], where a function (or part of it) to be implemented is matched against cells from a library. Sometimes this matching is limited to cells with a maximum number of inputs. So, we classify n-input functions in order to have a precise idea about the search space of the whole set of n-input functions [1-85]. More details about different methods of functions classification are tackled in chapter 3 of this dissertation where we exploit the potential of such a technique to design reconfigurable logic circuits from structures of classes when using novel devices properties.

1.2.3.2 Binary Decision Diagrams (BDDs)

Although the concept of BDDs is relatively old [1-86, 1-87], the effort made by Bryant in [1-88] has renovated the curiosity of many researchers and attracted their attention to

intensively exploit the capabilities of such an approach. With the continuous increase of computing system complexity, there is a growing need for new means to analyse and manipulate large propositional formulae. Many tasks in the design and verification of digital systems have proved the attractive utility and the flexibility of BDDs as the representation of choice for many CAD applications. Nowadays, reduced and ordered binary decision diagrams are usually implied when referring to BDDs as a canonical representation of Boolean functions. In fact, canonicity reduces the semantic notion of equivalence to the syntactic notion of isomorphism. It is the source of both efficiency and ease of use for BDDs, since it both enhances the effectiveness of memorization techniques, and also makes the test for equivalence inexpensive. Canonicity has however one important drawback: such BDDs are less concise (compact) than circuits in general [1-89].

The more popular and significant applications of BDDs are;

- The verification of the correctness of hardware for both the representation of circuits and the manipulation of sets of states.
- Model checking algorithms for systems with very large numbers of states [1-90, 1-91, 1-92].
- The optimization of logic circuits.
- The representation of "don't care" conditions [1-93].
- Translation of Boolean functions into circuits based on a specific implementation technology known as Pass-Transistor-Logic (PTL) [1-94, 1-95, 1-96].
- Testing and optimization of sequential circuits [1-97].

Since the pioneering work of Bryant, many variants of BDDs have been proposed in the literature. OBDDs are still the state-of-the-art data structure for Boolean functions (at least in many areas). Zero-suppressed binary decision diagrams (ZBDDs), ordered functional decision diagrams (OFDDs) and Ordered Kronecker Functional decision diagrams (OKFDDs) are three among many other variants of BDDs [1-98].

In chapter 3 of this thesis, we will use BDD basics to create a new variant of BDD adapted to novel devices capabilities.

1.2.3.3 Conclusions

EDA is one of the richest knowledge fields in computer science and engineering (CS&E) Figure 1-10 shows the tremendous inter-disciplinary effort required to develop EDA tools. Thus, scientists and engineers in EDA need electrical engineering to derive circuit and system models, and mathematics and theoretical computer science to solve complexity and optimize algorithmic analysis. Concerning the function classification approach, this enables the identification of Boolean functions which share some specific properties, then group them into classes considered as black boxes. This helps to deal with functions in a more generic

way and to simplify the research space of functions. When it comes to BDDs, they remain a flexible canonical representation of Boolean functions utilized by many CAD tools. Both concepts are used further in this thesis to enable logic synthesis with emerging nanodevices.

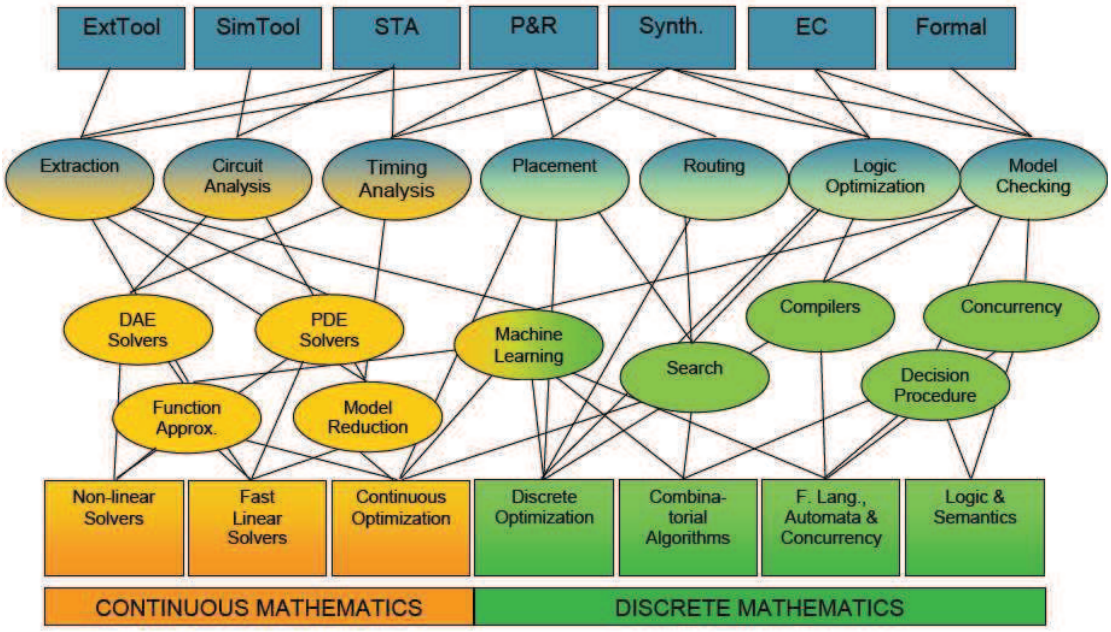


Figure 1-10. Fundamental Areas and Domain Knowledge in EDA [1-99]

1.2.4 CMOS fundamental limits

Currently, there are three basic limitations to the conventional CMOS scaling trend: material related performance limits, lithography limits and economic limits.

Performance limits

The materials of electronic devices define the limits of reliability, conductivity and breakdown voltages. At sub-100nm CMOS technology nodes, leakage currents increase by several orders of magnitude. At the same time, traditional switching leads to greater power consumption and less power efficiency. With higher packing densities, junction temperatures rise to a level that no longer allows higher clock frequencies and thus better speed. This has contributed to the slowdown in the trend of maximum clock frequencies of microprocessors [1-100], which have been power-limited to 4GHz clock frequency for about a decade.

Lithography limits

For quite some time, the minimum resolution line width below the wavelength used for their exposure has been an important issue. This requires significant effort in optical proximity correction, off-axis illumination, short wavelength, high output power laser light sources and appropriate resists. The latest step in lithography process complexity is the implementation of immersion-based lithography tools [1-100]. With the market moving to more immersion lithography tools , and as extreme ultraviolet (EUV) lithography units enter the market, lithography tool average selling prices will trend from $20.1M in 2011 to $22.1M

in 2012 [1-101]. Volume production of mass-market semiconductors requires several of these expensive tools. Some resolution enhancement technologies, such as double exposure, are expected to have a negative impact on throughput and will thus further increase manufacturing costs.

Economic limits

Lithography limits and the tremendous efforts in tool and unit process development directly drive up typical wafer facility costs. With respect to the increasing costs, for most applications, in-house manufacturing for advanced technology nodes will be difficult to afford for a single semiconductor supplier.

Manufacturing will need to be outsourced to a foundry or executed in clusters of a sufficient number of semiconductor suppliers. Even considering consortia, it will be difficult to achieve the desired return on investment (ROI). Memory and microprocessors – both high volume markets – may at some point in time be the only products to justify the move to the most advanced technology nodes. In other areas, most of the product innovation will be driven by factors other than scaling. Continuously and significantly decreasing cost per function accompanied by a performance increase has been the key driver in the past. Cost considerations will stall this trend and set tight limitations for node usage at 32nm and below.

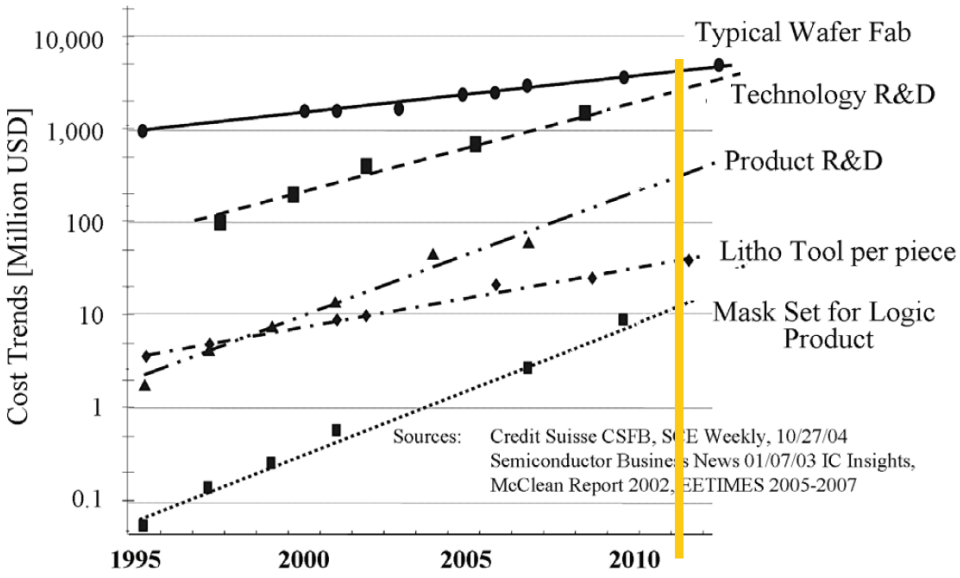


Figure 1-11. Cost trends in the semiconductor industry [102]

1.2.5 Conclusions of CMOS Computing

The aim of this section was to give an overview of current CMOS technology from various angles: from device limits and trends, to architectural capabilities and drawbacks, to EDA tools. At the device level it was shown that the aggressive scaling of CMOS technology leads to critical degradations of Bulk-MOSFET performance metrics, mainly due to SCE. The semiconductor industry is tending towards two engineering technologies, SOI and Multi

Gates. Both approaches demonstrate a significant improvement in speed and power, although with expected cost penalties due to additional fabrication process steps and consequent increase in design parameters. For CMOS based architectures, regularity is of a prime concern to combat variability and increase reliability. Many-core architectures represent a promising approach towards this end with an affordable power budget. In parallel, advances in reconfigurable architectures continue. FPGAs dominate this approach, with rising capacity to handle a variety of applications. Some limitations persist however, such as resource inefficiency in FPGAs, and the complexity of software algorithms in many-cores. Both structures are converging toward the integration of other units such as DSP, flash/CMOS memories and non-volatile memories. Also, we presented conventional EDA tools and we singled out Boolean function classification and BDD techniques. We explained their principles and use, since these will form the basis of our proposed design techniques for emerging nanodevice-based logic design. Finally, we reminded the principle limitations of CMOS computing. In the next part of this chapter, we investigate beyond conventional approaches, in the form of emerging technologies: devices, architectures and tools.

1.3 Computing with Emerging Technologies

According to the ITRS, the general tendency today is to consider that after 2015, emerging technologies may complement or replace scaled CMOS. They will be most probably embedded with CMOS technology in hybrid solutions, but can also enable novel information processing paradigms with improved performance metrics over CMOS. Various kinds of alternative logic devices, so called “Beyond CMOS Devices,” such as nanowire (NW) transistors, carbon nanotube field-effect transistors (CNTFETs), graphene nanoribbon (GNR) transistors, single electron transistors (SETs), and quantum-dot cellular automata (QCA) [1-103], have been proposed. These nanodevices benefit from quantum mechanical phenomena and ballistic transport characteristics under lower supply voltages with lower power consumption. Further, they are expected to be used for ultra high density integrated electronic systems due to their extremely small size.

As a result, research in emerging device technologies must be associated with advances in circuit and system architectures. As shown in figure 1-12, even if the standard way to carry out computation is based on silicon MOSFETs in von-Neumann many-core system architectures, several other ways could be explored.

In this part of the chapter, we explore different emerging devices and we briefly overview system architectures using such devices in order to avoid facing the same limitations that are challenging CMOS technology. Furthermore, they enable new computing paradigms to go beyond the conventional CMOS concept. Special attention is given to the presentation of carbon and nanowires devices. Both technologies demonstrate a specific property known as “ambipolarity”, which is at the heart of this thesis, in a double gate device context.

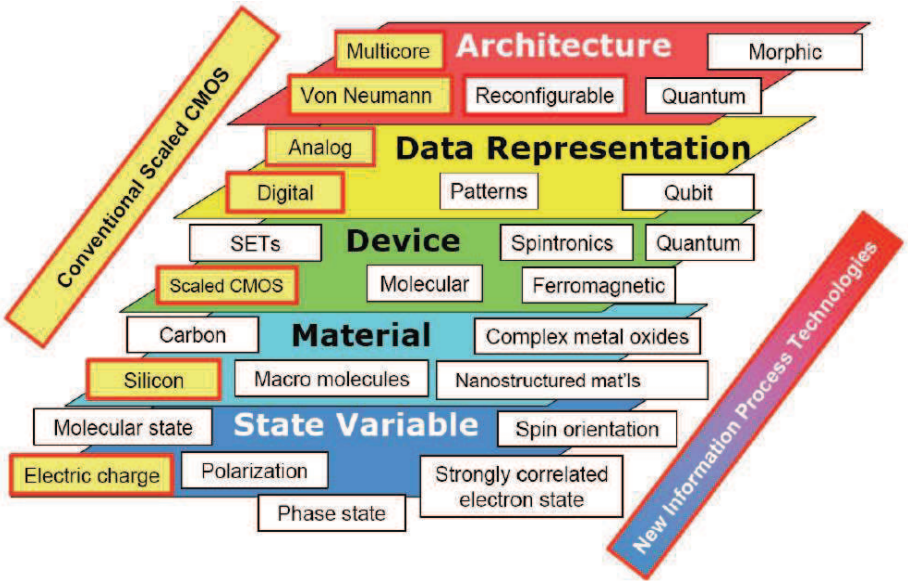


Figure 1-12. Taxonomy for emergent technologies [1-8]

1.3.1 Device

While some emerging devices use a different state variable to represent logical information, by using different physics from that of conventional field-effect CMOS transistors (such as spin or molecular state), the most straightforward way to overcome some limitations of CMOS technology is in the use of novel materials to replace the channel. Two approaches are possible. The first approach consists of the monolithic use of materials with high mobility, such as Ge or III-V compound layers. The second approach supposes a specific replacement of the Si channel (on a silicon substrate) by using new materials such as SiNWs, CNTs and GNRs, all of which are considered as low-dimensional devices. Whichever the approach, the state variable is still represented by voltage (or charge on a capacitance) and is based on the field-effect control of electrons in different regimes (inversion, depletion or enhancement) of the switching device.

In this section, we initially review the first category of emerging technologies which use non-conventional state variables (SET, spin devices, molecular electronics ...). We subsequently discuss the second category, based on the electric charge state variable and considered as an extension of CMOS technologies. In this context, we investigate a new class of FETs, which is in reality a sub-category of devices using new channel materials (SiNW, CNT, graphene). This class of FETs controls the ambipolarity behaviour reported in many post-silicon devices by using an additional gate.

1.3.1.1 Unconventional state variable technologies

The ITRS Emerging Research Devices (ERD) and Emerging Research Materials (ERM) chapters suggest the possibility of using new state variables for computation as well as for information storage. Here, we illustrate the most promising devices.

a. *Single-electron transistors (SETs)*

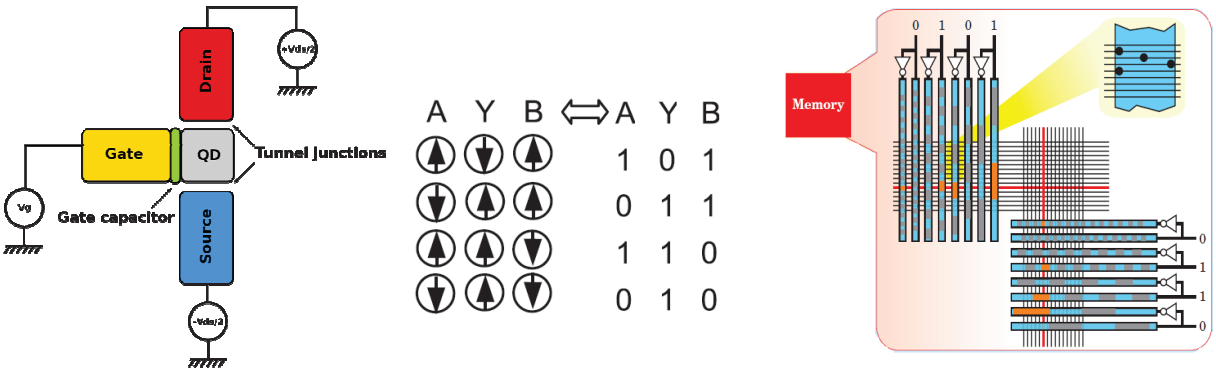
SET devices are very attractive for future large-scale integration thanks to their small size and low-power dissipation. A schematic of a SET is shown in Figure 1-13(a). The majority of SET circuits demonstrated to date employ so called "voltage state logic," where a bit is represented by the voltage of a capacitor charged by many electrons. These devices were initially considered to have a theoretically estimated maximum operation temperature T of around 20K, integration density n of $\sim 10^{11}$ cm^{-2}, and speed of the order of 1GHz [1-104]. Some variants of SETs operating at room temperature have been recently fabricated and have led to the development of applications and architectures such as SET/CMOS hybrid multi-value logic circuits [1-105], multi-band filtering circuits [1-106], analog pattern matching circuits [1-107], associative recognition tasks [1-108], and others [1-109].

b. *Spin devices*

Spintronics (spin transport electronics), also known as magneto-electronics, exploits both the intrinsic spin of the electron and its associated magnetic moment, in addition to its fundamental electronic charge, in solid-state devices [1-110]. In fact, electrons trapped in quantum dots have overlapping wave functions, and can influence the state of each other mutually. The coupling of the spin states of electrons was used to transmit data [1-111] and to implement logic gates [1-111, 1-112]. Figure 1-13(b) shows the way spin devices are organized in arrays of quantum dots in QCAs. In spite of the extremely low energy consumption, a severe problem of QCA arises from their sensitivity to the background charge and noise sensitivity. Today, no viable solutions to the background charge immune single-electron systems are known.

c. *Molecular electronics*

Molecular electronics spans physics, chemistry, and materials science. Their physics is generally based on either charge trapping (in a similar way to Coulomb blockades), or on resistance depending on the molecular state (phase). One interesting use of molecular devices is their application as latching switches [1-109]. The size scale of molecules is between 1-100nm, a scale that permits functional nanostructures with accompanying advantages in cost, efficiency, and power dissipation. One can exploit specific intermolecular interactions to form structures by nanoscale self-assembly, and thus modify electronic behavior, providing both switching and sensing capabilities on the single-molecule scale. The CMOS-molecular (CMOL) hybrid circuit concept is based on linking CMOS circuit parts with crossbars fabricated with silicon nanowires and molecular latching diodes at the cross points of the nanowires [1-113, 1-114] as shown in figure 1-13(c). Molecules have disadvantages, though, such as instability at high temperatures.



(a) Single electron transistor (b) Spin QCA (c) Molecular-crossbar-electronics

Figure 1-13. Novel information processing devices: (a) SET device (b) Spin QCA realizing Y = NAND with spin up = 1 and down = 0 [1-111] (c) 256-bit memory circuit [1-115]

1.3.1.2 CMOS extension

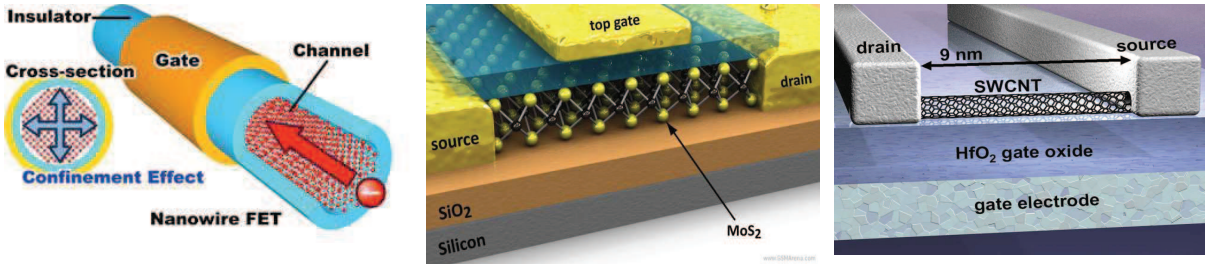
In this section, we review another alternative to overcome CMOS limits. Based on the conventional state variable (electric charge), novel materials can replace the FET channel. We start by presenting ways to increase the mobility of device channels by using high mobility materials. Then, we explain the advantages of replacing the silicon channel by using 1-dimensional materials such as SiNWs, CNTs and graphene.

a. *Stress engineering*

Mobility loss resulting from higher channel doping and scaled gate dielectrics should be compensated to meet performance targets. A straightforward and cost-effective way to improve device performance and scalability is mobility-enhancement technology. This can be achieved either by using high-mobility channel materials (such as Ge or GaAs), or by straining the channel mechanically. Various CMOS fabrication processes can be used to induce appropriate strain to the channel region of the MOSFETs, such as by depositing a thin layer of silicon on a relaxed SiGe virtual substrate, resulting in mobility enhancements of 110% for electrons and 45% for holes [1-103].

b. *Low Dimensional Structures*

The generic expression “low-dimensional structures” is an approximate description of CNTs, SiNWs and graphene nanoribbons [1-103]. In fact, a 2D sheet of single-atom carbon is called graphene, and becomes a nanoribbon when etched to within a few nanometers width. A CNT structures is a sheet of graphene rolled upon itself. As for SiNWs, they are sometimes in reality three dimensional structures with extremely small cross-section dimensions. The main common point between all these cases is a notable confinement effect which offers much higher mobility.



(a) SiNWFET (b) GNRFET (c) CNTFET

Figure 1-14. Low dimensional structure FETs: (a) Silicon Nanowire device (b) Top-Gated Graphene transistor (Samsung, April 2012) [1-116] (c) Back-Gated carbon nanotube transistor (Technische Universität München, April 2012) [1-117]

Nanowire electronics

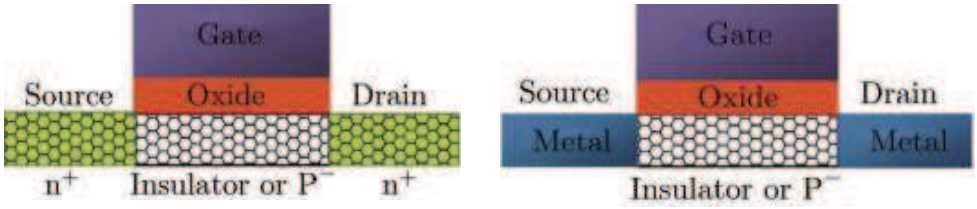
Nanowire field-effect transistors *NWFETs* (Fig. 1-14(a)), Gate All Around (GAA) FETs with a thin nanowire channel, have drawn much attention and have been considered as promising candidates for continuous CMOS scaling, since their non-planar geometry provides superior electrostatic control of the channel than conventional planar structures. The increasing attention in nanowire research stems from several key factors such as their highly reproducible electronic properties [1-118, 1-119, 1-120] and cost-effective "bottom-up" fabrication which circumvents some fabrication challenges [1-121, 1-122, 1-123, 1-124, 1-125, 1-126]. DeHon [1-127] proposed that programmable logic arrays (PLAs) can be built using nanowire FET NOR planes. General logic computing can be achieved in an array-based architecture such that the output from one array forms the input of the other through crossbar interconnects [1-127, 1-128]. The use and limitations of nanowires in computing architectures are discussed further in this chapter.

Carbon electronics

Carbon nanotubes have been studied for the past two decades, whereas graphene has only been developed recently in 2004. Both show excellent electronic performances [1-129, 1-130]. Semiconducting single-walled carbon nanotubes (SWCNTs) and graphene nanoribbons (GNRs) have demonstrated high electrons mobility of up to nearly 200 000 $cm^2\ V^{-1}\ s^{-1}$ [1-131] compared to only 1400 $cm^2\ V^{-1}\ s^{-1}$ with Silicon technology. The bandgap of SWCNTs is inversely proportional to the nanotube diameter, with a typical bandgap of 0.7eV at 1.4nm [1-132]. GNRs show similar behavior to SWCNTs, although the typical bandgap is 10meV for a ribbon width of 10nm [1-128], at the device level this means that graphene transistors cannot be "switched OFF," resulting in a small ON/OFF ratio. Monolayer graphene shows high transmittance of nearly 97% [1-133]. This implies that the potential of nanoscale carbon structures for future flexible electronics is very high, although some technical barriers still exist prior to practical utilizations. Figures 1-14 (b) and (c) depict examples of GNRFET and CNTFET devices, respectively, fabricated very recently in 2012.

Different types of CNTFETs have been demonstrated in the literature; the most important distinction is between MOSFET-like (Fig. 1-15(a)) and Schottky-Barrier CNTFETs (SB-

CNTFETs) (Fig. 1-15(b)). While the first family is characterized by doped CNTs, the second family is made up of intrinsic CNTs that form a Schottky Barrier at the drain and source contacts.



(a) (b)

Figure 1-15. CNTFET types: (a) MOSFET-Like CNTFET (b) SB-CNTFET

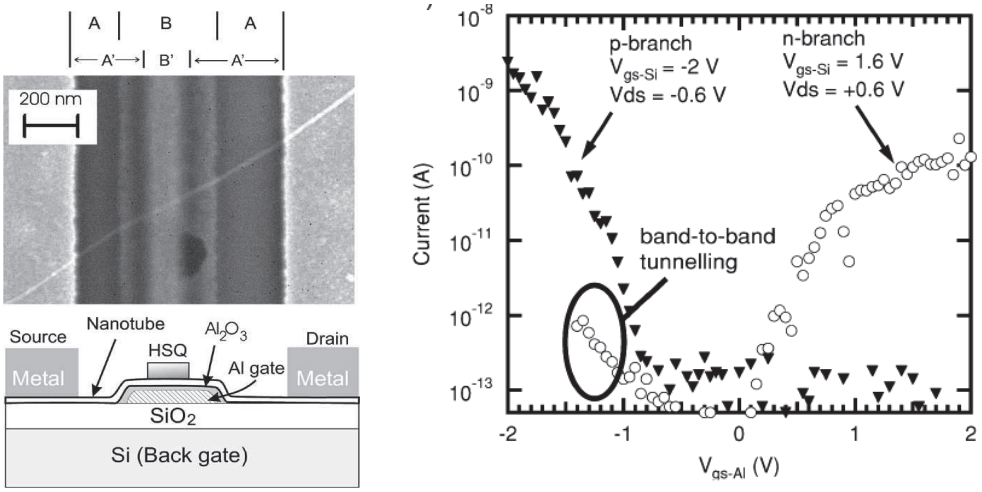
SB-CNTFETs are ambipolar, i.e. they conduct both electrons and holes, showing a superposition of N- and P-type behaviors. The Schottky barrier thickness can be modulated by the fringing gate field at the CNT-to-metal contact; allowing the polarity of the device to be set electrically [1-134, 1-135]. Similar ambipolar behavior has been reported for graphene nanoribbon field-effect transistors, and suggests the possible electrical polarity control of these novel devices as well [1-136]. Very recently, Sachetto from EPFL also realized the same concept with a double gated Si-nanowire [1-137]. In the next section, we investigate in more detail ambipolar behavior and its controllability in the context of double gate devices.

c. *Ambipolar Independent Double-Gate FETs (Am-IDGFET)*

With intensive research in new devices and materials, novel phenomena such as ambipolar conduction have been identified, characterized by a superposition of electron and hole currents and experimentally reported in many post-silicon devices including carbon nanotubes [1-138] graphene [1-139], silicon nanowires [1-140, 1-141, 1-42], organic single crystals [1-143], and organic semiconductor heterostructures [1-144]. Initially, such ambipolar behaviour was considered undesirable since it is not compatible with conventional digital and analog circuits designed with unipolar transistors leading to a high leakage current. Thus several techniques were proposed to convert such devices from ambipolar to unipolar behaviour [1-145]. However, the ability to select the polarity (P- or N-type) in-field by using a second polarity gate [1-135, 1-137] has inspired some design teams to exploit Am-IDGFET devices to build novel logic circuits showing significant gains in area, power, and performance [1-146, 1-147, 1-148, 1-149, 1-150]. In several works, ambipolar conduction has proved to offer more design options . In [1-153], Yang and Mohanram have generalized the design principles of ambipolar electronic and presented new designs and applications.

Review of Am-IDGFET fabrication

In the case of CNTFETs with double gates to control the ambipolarity behaviour, a single DG-CNTFET has been fabricated and characterized by using one top- and one back-gate [1-135]. Figure 1-16 shows the view and the controllable I-V characteristics of this ambipolar double-gate device.



(a) (b)

Figure 1-16. Ambipolar CNTFET view and characterization [1-135]: (a) View based on a SEM of ambipolar double-gate CNTFET. Region A is back gate and B is top gate. (b) I_{DS}-V_{GS} curve with top gate for a fixed back-gate voltage. For a positive (negative) back gate voltage: device behaves as N- (P-) type.

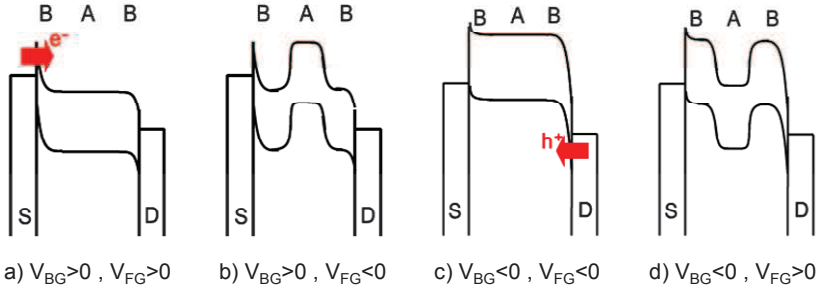


Figure 1-17. Band diagram of an ambipolar CNTFET: (a) With $V_{BG} > 0$ the CNTFET behaves as a N-type device. For $V_{FG} > 0$, an electron current flows. (b) The N-type device blocks the electron current flow for $V_{FG}<0$. (c) With $V_{BG} < 0$ the CNTFET behaves as a P-type device. For $V_{FG} < 0$, a hole current flows. (d) The P-type device blocks the hole current flow for $V_{FG} > 0$ [1-135, 1-103]

The top gate (or Front Gate, FG) in region A controls the current conduction through the device, while the polarity gate (or Back Gate, BG) in region B controls the type of polarity: a high or low voltage yields, respectively, an N- or P-type behavior. The operating principle of these devices can be understood by means of the band diagram in figure 1-17. This device possesses a Schottky barrier at the drain and source contacts, which can be thinned by applying the right contact in region B. If the voltage applied at the electrode controlling the region B is positive and large enough (V+), then the Schottky barrier is transparent to tunneling electrons and the transistor has an N-type behavior, as shown in figures 1-17(a) and (b). When the same voltage is negative and large enough (V-), then the Schottky barrier is transparent to tunneling holes and the transistor has P-type behaviour figures 1-17(c) and (d). Between these two values, the barrier is too thick for both electrons and holes and conduction through the transistor is poor, and minimal for a BG bias $V_0 = V_{DS}/2$ if V_{DS} is applied between drain and source. While the choice of the voltage applied in region B determines the polarity of the devices, the voltage applied in region A may set up a high potential barrier in the middle of the channel and stop any potential current flow. Independently from the technological integration

process, the principal advantage of the device is its unique in-field reconfigurability, meaning that each back-gate needs an individual control.

It has also been shown that the type conversion of CNTFETs could be possible by trap-layer-induced electrostatic doping using a charge-trap layer between the top gate and semiconducting CNT channel [1-154]. Figure 1-18 shows the transfer characteristics of P-type and N-type CNTFETs converted using a floating gate (FL-G). At high negative gate bias, which is applied initially before the device operation, positive charges are caught in the trap layer. Therefore, electron tunneling is favored, creating N-type doping behavior. The Control Gate (CG) voltage sweep between –6V and +6V then provides I–V characteristics of an N-type FET. Inversely, negative charges are trapped at high positive gate bias, where hole tunneling is favored, creating a P-type FET.

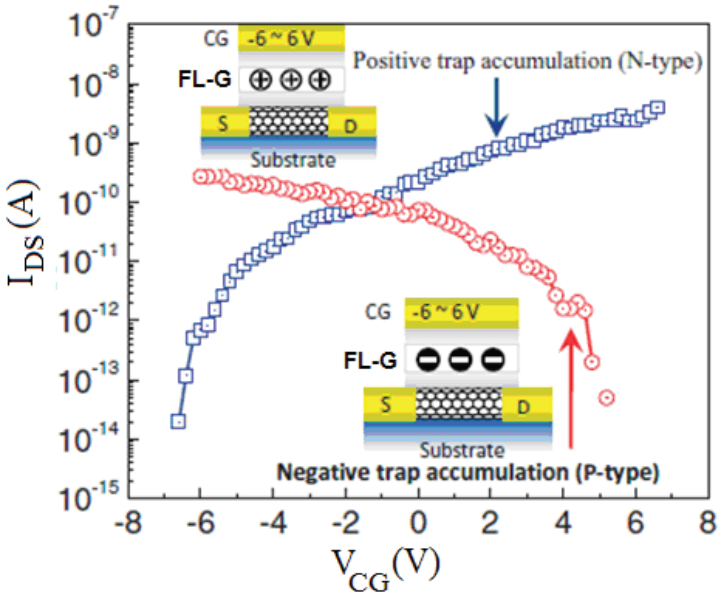


Figure 1-18. Transfer characteristics of a CNTFET device that consists of a floating gate in between top gate and semiconducting channel. The device shows P-type and N-type behavior due to trap layer-induced electrostatic doping from floating gates [1-154]

Although Am-IDGFETs were initially demonstrated with carbon nanotubes, recent work realized devices with the same property with Silicon Nanowire technology. In [1-137], a new device structure exploiting an Independent Double Gate configuration with SiNW and top-down fabrication flow has been demonstrated. Figures 1-19 and 1-20 show the structure of the device as well as its transfer characteristics, respectively. All the I_{DS}–V_{GS} characteristics, defining N-type, P-type, and ambipolar behavior, have been obtained with I_{ON}/I_{OFF} ratios of up to four orders of magnitude and with inverse subthreshold slopes close to those of state-of-the-art Schottky-barrier FETs.

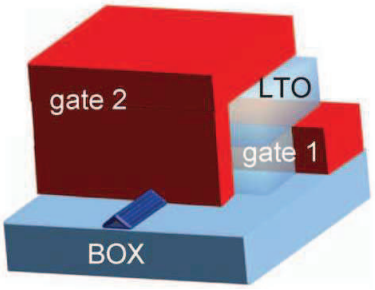


Figure 1-19. Double Gate ambipolar Nanowire FET structre. [1-137]

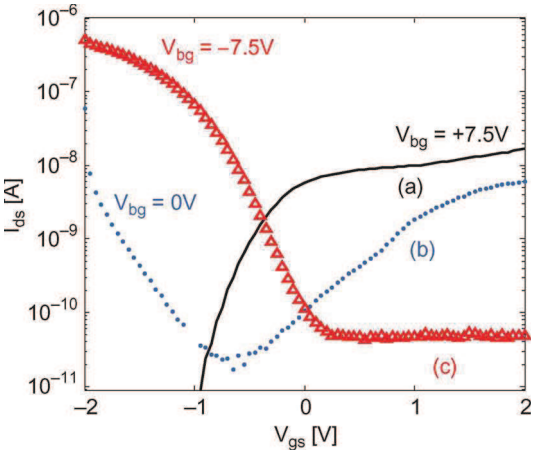


Figure 1-20. Controlled ambipolar I_{DS}–V_{GS} characteristics at different V_{BG} backgate voltages. (a) Positive V_{BG} = +7.5 V is used to obtain an n-type characteristic. (b) V_{BG} = 0 V gives ambipolar I_{DS}–V_{GS}. (c) Negative V_{BG} = −7.5 V is used to obtain a P-type characteristic. [1-137]

In a recently published paper [1-155], the concept of reconfigurable silicon nanowire transistor is demonstrated by employing an axial nanowire heterostructure (metal/intrinsic-silicon/metal) with a diameter of 20nm embedded in a silicon oxide shell (of thickness 10nm) and two independently working top gates as seen in figure 1-21. The reconfigurability enhances electrical characteristics, providing record I_{ON}/I_{OFF} values (up to 1×10^9) for silicon nanowire devices and significantly reducing the source - drain leakage currents, compared to conventional field effect transistors.

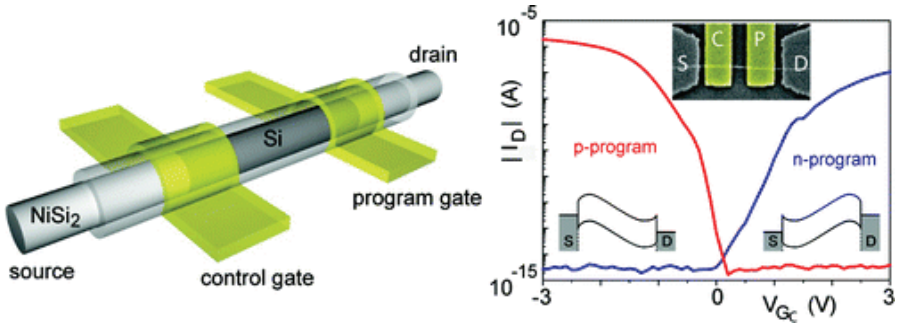


Figure 1-21. Schematic and I-V characteristics of a reconfigurable silicon nanowire field effect transistor (RFET). The program gate is used to select the P- or N-polarity whereas the control gate tunes the conductance through the nanowire [1-155]

Am-IDGFET Generic Structure

Independently of the technology on which the Am-IDGFET is based, we aim to explore ambipolar behavior through all three states of the device (N-type, P-type or OFF). Figure 1-22 describes the generic behavior of a single Am-IDGFET. This symbol, as well as the three configurations achievable via its Back-Gate (BG), is used throughout this thesis.

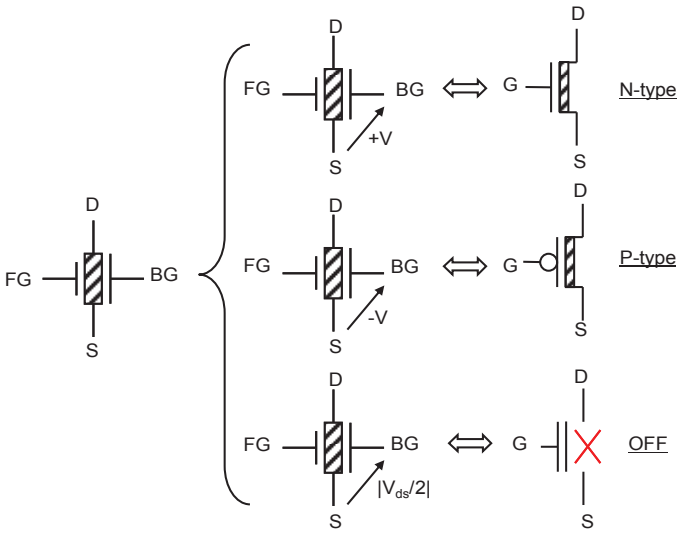


Figure 1-22. Symbol and configurations of Am-IDGFET device

The front gate FG turns the device ON or OFF, in the same way as the regular gate of a MOSFET; while the back-gate BG controls the device polarity setting to N- or P-type with a positive (V_{BG}-V_S= +V) or negative (V_{BG}-V_S= -V) voltage, by permitting electrons or holes to enter into the channel respectively. The device is in the OFF-state (whatever the voltage on gate FG) if the back gate is set to $V_0 = |V_{DS}/2|$ (V_{DS} referring to the voltage applied between drain and source).

1.3.1.3 Conclusions

Emerging nanodevices benefit from unique intrinsic physical properties such as quantum mechanical phenomena or ballistic transport characteristics, which enable them to perform potentially better than conventional CMOS devices. In this section, we explored unconventional state variable technologies (SET, spin devices and molecular electronics) and we highlighted their opportunities and their limitations. We subsequently looked at a second category of emerging devices considered as CMOS extensions, based on the same state variable as MOSFETs, (electric charge), and where the channel is replaced by 1-D materials such as SiNW, CNTs or graphene, providing high mobility. Such materials also demonstrate ambipolar behavior, which can be controlled by using an additional gate. This gives rise to a new class of devices “ambipolar IDGFETs” abbreviated as Am-IDGFET throughout this dissertation. The fabrication of such devices with CNT and SiNW technologies has been described, as well as their characterization. In the next section, we outline emerging technologies architectures in general and we evoke many structures using Am-IDGFETs.

1.3.2 Architectures

Table 1-2 shows a projection of possible application areas for emerging research devices in the context of special functions, which might offer a performance advantage relative to CMOS technology. It is useful to speculate on the relative performance attributes of the three architectural classes considered herein: homogeneous many-core, hybrid architectures, and neuromorphic architectures [1-156]. The homogeneous many-core approach has already been discussed in section 1.2.2.1. Concerning neuromorphic architectures, many flavors are possible: we quote for instance Cellular Nonlinear Networks (CNNs) [1-157, 1-158], Associative Memory Processors (AMP) [1-159] and bio-inspired systems [1-160, 1-161] used to emulate the behaviour and the structure of complex biological neural systems. In this work, we are focusing on standard computation paradigms. Thus, we focus only on hybrid architectures, i.e. relative to computing systems where various emerging devices (SiNW, CNT, Molecular, etc) are integrated with CMOS technology.

TABLE 1-2. EMERGING NANODEVICE-BASED ARCHITECTURES [156]

Architecture	Implementation	Computational elements	Network	Application	Research activity[1]
Homogeneous Many-core	Symmetric cores	CMOS	Irregular/fixed	Synthesis/GPP	158
Hybrid	Asymmetric cores	CMOS	Irregular/fixed	Synthesis/GPP	
	CMOL	CMOS+ molecular switches	Irregular/fixed	Synthesis/GPP	12
	Molecular cross-bar	Molecular switches	Regular/fixed	Synthesis/GPP	23
	Check-point	CMOS+ Ferromagnetic logic	Irregular/fixed	Synthesis/GPP	3
Neuromorphic	CNN	CMOS+ sensors, FG-FET	Regular/fixed	Recognition/vision	84
	AMP	FG-FET, SET	Irregular/fixed	Recognition/vision	11
	Bio-inspired	MTFD, Spin transistor	Mixed	Recognition	35[2]
				Mining	
				Synthesis	

[1] number of referred articles in technical journals that appeared in the Science Citation Index database for 7/1/2005-7/1/2007
[2] Not including CNN and AMP

Definition of terms
recognition—machine learning techniques that examine data and construct models for the data; mining—finding a model in a large volume of data; synthesis—exploring new scenarios by constructing new instances of a model; CMOL—molecule on CMOS architecture; CNN—cellular nonlinear network; AMP—associative memory processor; FG-FET—floating-gate field-effect transistor; SET—Single electron transistor; MFTD—multiferroic tunnel diode; GPP—general-purpose processor

Heterogeneous architectures can be classified into two categories according to the means of improvement which can be pointed out:

- The improvement is realized by increasing the integration density (i.e. more devices with the same functionality in the same area) thanks to high regularity usually obtained from a crossbar arrangement of nanodevices such as SiNWFETs and CNTFETs. This case of "*Regular Architectures*" is detailed first in this section.
- The improvement is realized by increasing the device functionality (i.e. the use of the same number of devices with more functionality in the same area). Here, novel nanodevices

make up a hardware platform that can be reconfigured during operation to perform different logic computations, improving circuit design flexibility. This case of "*Enhanced Reconfigurable Architectures*" is discussed in the second part of this section.

1.3.2.1 Regular Architectures

The ultra-scaled dimensions of nanodevices are limited by the abilities of photolithography equipment, leading to a critical variability issue. One solution is to use specific layout patterns to enable optical proximity correction at the circuit scale. Redundancy and regularity of integrated circuits are also considered to be key. With emerging technologies, regularity becomes necessary to solve the issue at the architectural level, especially since it is compatible with bottom-up fabrication techniques. Crossbar-based circuits and regular arrays of nanoblocks are intensively used by emerging technologies based regular architectures. Examples of nanodevices arrangement are presented in this section.

a. *NanoPLA*

Crossbar architectures have emerged as a possible paradigm for reliable massive and parallel computing with highly defective basic components [1-162]. At the nanowire crossings (called cross points), molecular devices can perform logic operations or store information. The nanoPLA architecture is an example of the crossbar concept implementation, where programming is enabled by switches. Signal routing or wired-OR logic functions can be performed. The input of the crossbar represents a decoder, which is used in order to address each nanowire independently of the others. The output of the crossbar is routed to a second crossbar, in which the signals can be inverted by gating the nanowires carrying the signals. A cascade of these two planes is equivalent to a NOR plane. Two back-to-back NOR planes are universal gates, and they can implement the traditional AND-OR PLA. A nanoPLA block from [1-163] is shown in Figure 1-23.

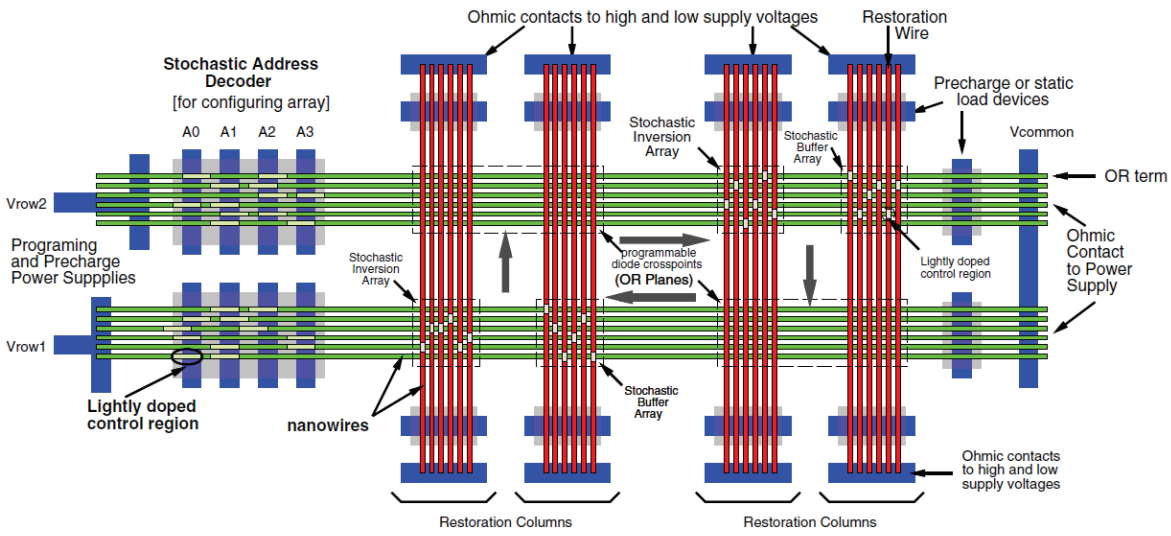
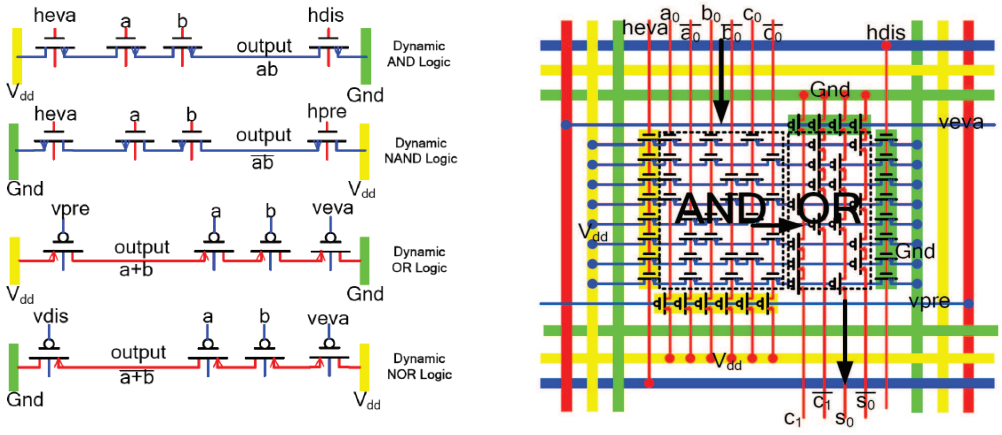


Figure 1-23. NanoPLA architecture [1-163]

b. *Nanoscale Application Specific Integrated Circuit (NASIC)*

Using the same concept of crossbar arrangements, a second architecture known as Nanoscale Application Specific Integrated Circuit (NASIC) was proposed in [1-164]. The main difference between NASIC and NanoPLA is the use of FETs instead of using diode logic [1-165] at the cross-points. This technology, based on FETs, can address specific application-driven designs. Several basic logic circuits such as adders, multiplexers and flip-flops were implemented using NASIC tiles based on a dynamic logic style. Two clock transistors are placed between the power lines and a stack of transistors, which realize the logic function. It is possible to implement standard AND/OR functions and their inverted counterparts as shown in figure 1-24 (a). A complete NASIC tile is depicted in Figure 1-24 (b). A first set of AND logic functions are realized in the horizontal direction. Nano-scale wires are connected to micro-scale power lines and to the other blocks that are surrounding the crossbar core. The second horizontal AND functions drive transistors in the vertical orientation. The vertical line set implements OR functions. A 1-bit full adder example is illustrated in figure 1-24 (b).



(a) (b)

Figure 1-24. NASIC architecture: Dynamic logic implementation of AND, NAND, OR and NOR functions (a) (1-bit full adder circuit) (b) [164]

c. *CMOS/Molecular Hybrid Systems (CMOL)*

The CMOL approach combines CMOS with molecular and one-dimensional devices. This way, the approach can benefit from both technologies. In CMOL circuits, the crossbar part represents a programmable interconnect grid, and it can perform the wired-OR function without any inversion, while the logic functions, including the signal inversion, are performed by the CMOS part [1-109]. This part is also dedicated to input/output interfacing, and decoding of the nanowire crossbar. Many circuits have been simulated with the CMOL approach, including a FPGA-like programmable digital logic architecture [1-167] and biologically-inspired circuits for image recognition [1-166]. They promise a improved performance and fault-tolerance over CMOS.

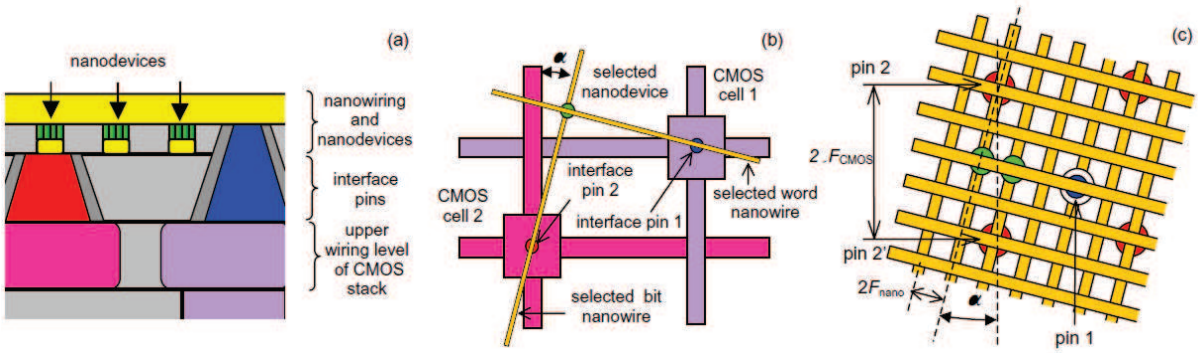


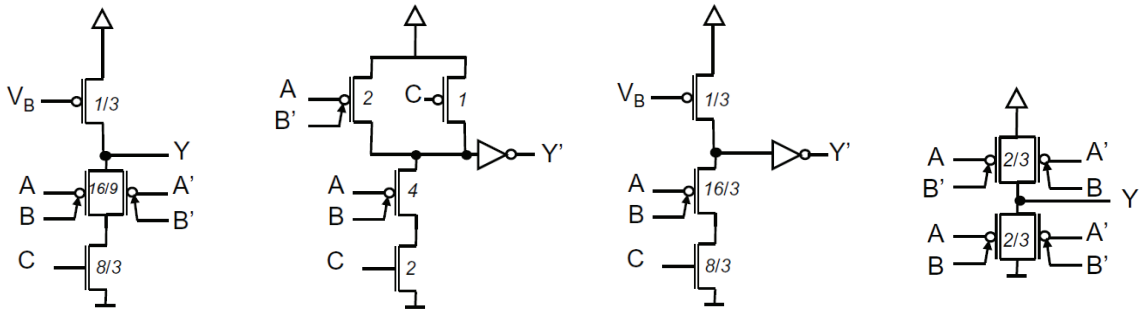
Figure 1-25. CMOL architecture: (a) Schematic cross-section of CMOS and crossbarparts. (b) Addressing of sublithographic nanowires. (c) Addressing of two crosspoints [1-168] [1-109].

1.3.2.2 Enhanced Architectures

In the previous part, emerging devices have been used to realize crossbar circuits. In fact, 1-D structures have been mainly envisaged to create dense interconnection networks or dense substrates to build active devices at the nanoscale. In section 1.3.1.2.c of this chapter, we surveyed some 1-D materials (CNTs, SiNW …) used as FET channels with "ambipolar" behavior, which does not exist in CMOS technology. This could be used efficiently to obtain new functionalities at the device level. The benefit of rich-logic-states transistor on logic circuit design is assessed at two levels: standard cells and reconfigurable logic structures.

a. *Am-IDGFET-based standard logic cells*

For standard cells, more compact logic circuits can be achieved thanks to the ability of performing logic operations on signals feeding both gates of a single ambipolar device. In [1-109], the author designed a set of static logic families including combinations of transmission gates / pass-transistors on one hand and complementary / pseudo-logic on the other. Figure 26 shows some examples of the designed gates. The XOR2 gate showed a natural, simple and efficient implementation with low cost, as shown in figure 1-26(d). In the same perspective, authors in [1-169] showed that a single ambipolar double gate SiNW device can be used to perform any of the XOR, XNOR, NAND, AND, and NOR binary logic operations depending on the encoding of the input signals. The proposed integration scheme was envisaged for logic circuits exploiting the improved expressive power of ambipolar-controlled SiNW devices, which is enabled by the reliability of Si fabrication technology. These compact gates form an efficient standard library which can be used by synthesis and mapping tools to implement more complex logic circuits.



(a) (b) (c) (d)

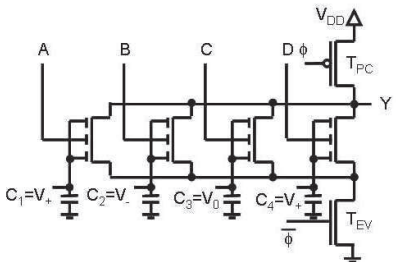
Figure 1-26. Compact implementation of (A ⊕ B).C function: transmission gate pseudo logic (a), pass transistor static logic (b), pass transistor pseudo logic (c) Compact implementation of (A ⊕ B) function (d)

b. *Am-IDGFET-based reconfigurable logic*

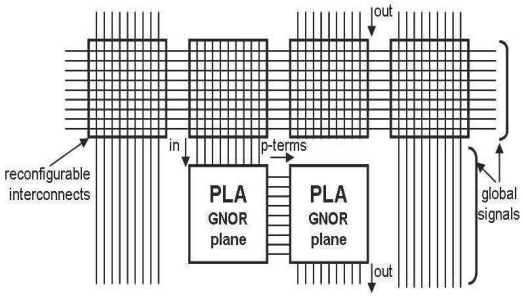
The potential of ambipolar devices is not limited to the construction of standard cells; it can also be used to build reconfigurable logic. Many design teams highlighted the efficiency of such devices to build reconfigurable logic cells and architectures. In [1-170], a Generalized NOR (GNOR) reconfigurable cell has been designed with a dynamic logic style as shown in figure 1-27(a). The cell is reconfigured according to the back gate voltage C_i of transistors. This GNOR is used as the building block of an ambipolar CNTFET-based PLA, depicted in figure 1-27(b), and proved to be more powerful than classical PLA with smaller area, lower number of wires and increased frequency. Furthermore, the compact XOR designed in [1-169] has been exploited to build single- and dual-rail universal logic modules (ULMs) as candidates for DG-CNTFET based regular logic fabrics. The gates were able to leverage LUT-based mapping tools to better exploit ambipolar behavior and provided improvements in area, delay and total power of 37%, 12%, and 33%, respectively, compared to previous works [1-171]. The structure of ULM is shown in figure 1-27(c).

In [1-147] a carbon nanotube based architecture was proposed. It used a reconfigurable DG-CNTFET (RDG-CNFET) device, and enabled manufacture of nanoelectronic systems in CMOS circuit design styles. However, in this case, the ambipolarity of CNT was not exploited. The reconfigurability of CNT-based architecture was allowed by the integration of molecular devices. Bistable molecules have been electrically sandwiched in a double gate CNFET.

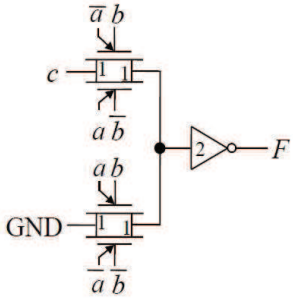
Finally, in [1-172], a dynamic reconfigurable logic cell is designed and used in the context of matrix-based architectures. As presented in figure 1-27 (d), the cell is composed of seven DG-CNTFETs organized in two logic stages: logic function and follower/inverter [1-172]. The polarities (N-type/P-type) of double gate devices T_{C1}, T_{C2} and T_{C3} are controlled by the corresponding back-gate bias voltages V_{bgA}, V_{bgB} and V_{bgC}. The cell may thus be configured to one of fourteen basic binary operation modes, as shown in figure 1-27(e). This type of cell will be considered in more detail in chapter 3.



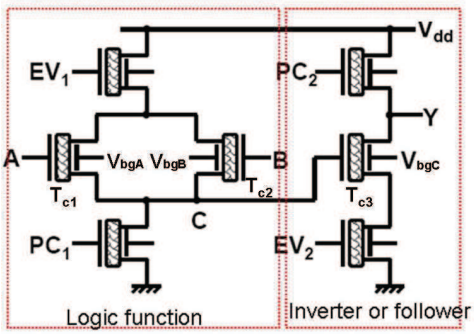
(a) GNOR gate configured as Y = NOR(A,¬B,D)



(b) PLA architecture with GNOR planes



(c) 3,2 ULM structure



(d) 7-transistor CNT reconfigurable cell [1-172]

V_{bgA}	V_{bgB}	V_{bgC}	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	-V	A+B
+V	-V	+V	$\overline{A}$.B
+V	-V	-V	A+$\overline{B}$
-V	+V	+V	A.$\overline{B}$
-V	+V	-V	$\overline{A+B}$
-V	-V	+V	A.B
-V	-V	-V	$\overline{A.B}$
+V	0	+V	$\overline{A}$
+V	0	-V	A
0	+V	+V	$\overline{B}$
0	+V	-V	B
0	0	0	1
0	0	-V	0

(e) Configuration table of the CNT reconfigurable cell [1-172]

Figure 1-27. Reconfigurable cells based on ambipolar double gate CNT devices

1.3.2.3 Conclusions

In this section we described how emerging technologies could lead to new architectural paradigms for reconfigurable computation. We suggested that emerging reconfigurable architectures can be analyzed from two different angles: i) architectures with density-increased devices (i.e. ultra-scale devices) and ii) architectures with functionality-enhanced devices (i.e. devices with richerfunctionality within the same area). In the second case, ambipolar logic has been deeply exploited, both for standard-cell logic and for elementary reconfigurable logic cells and arrays, leading to performance improvement as compared to CMOS structures. However, no design methodology or CAD tool has been built to allow structured design of Am-IDGFET-based logic cells. The understanding of ambipolar reconfigurable logic design is among the goals of this work, where we break from conventional logic design paradigms and propose design techniques and tools in order to build Am-IDGFET-based reconfigurable logic (this will be the topic of chapter 4).

1.3.3 EDA tools

The key to effectively use nanoscale devices in electronic circuits and systems is the availability of an accurate and efficient interface between the physical device technology and the circuit design process. With nanoelectronics enjoying a higher level of device integration than their CMOS counterparts, we expect that it will be necessary to revise or reinvent many existing synthesis, physical design, and verification methodologies and techniques to handle the sheer complexity of nanoscale designs. With the huge number of nanodevices available in a nano-integrated circuit, it is essential to raise the level of design entry and abstraction from register-transfer level to the architecture and system level to manage design complexity and increase design productivity. New design flows and tools to optimize nanoelectronic circuits for performance and yield are required. There are many initiatives in the literature which attempt to help designers to go further with emerging nanodevices by reshaping conventional design tools and flows to meet with novel devices requirements and opportunities. Some of these attempts are described in this section.

1.3.3.1 Modified design flow tools

A conventional logic synthesis flow contains three main distinct phases: technology-independent optimization, technology mapping, and technology-dependent optimization. In [1-173], an integration of the different phases of logic synthesis with each other is proposed (Fig. 1-28). This results in improved optimization of the synthesized logic, since it becomes possible for the optimization algorithms to recover from fundamental mistakes made during other phases. This was the result of a robust optimization framework driven by a powerful simulated annealing based engine [1-174]. Several other optimization techniques were explored; including a greedy optimization algorithm based on local transformations generated using NPN classes [1-175] of Boolean functions. One exciting contribution of this work is the possibility to apply the developed logic synthesis framework to two emerging technologies: chemically assembled nanotechnology and molecule cascades.

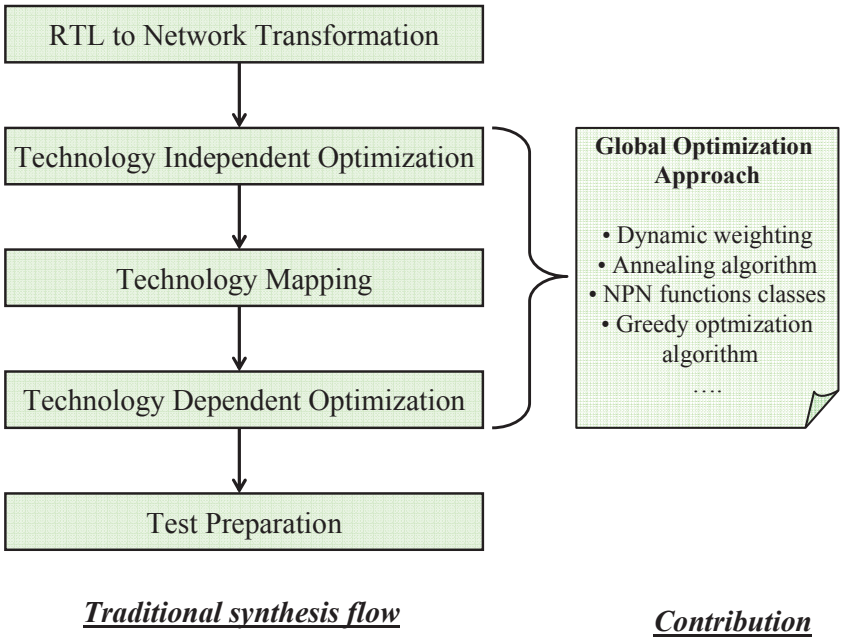


Figure 1-28. Optimization synthesis flow framework (integration of 3 steps in 1) [1-173]

A cell-library based design approach with emerging nanoelectronics could be possible for synthesizing terascale integration circuits [1-176]. In [1-169], EPFL built a variety of cell-libraries based on ambipolar DG-CNTFET devices. Then, libraries were characterized in the extended space of delay, power, and area. They were then connected to synthesis tools for logic circuit benchmarking. The tool flow used by the ambipolar DG-CNTFET libraries was based on the Verilog-To-Routing (VTR) [1-177] project from Toronto University designed to handle LUT-based logic in modern FPGAs. The modified tool flow is depicted in figure 1-29(a). In the same perspective of reshaping conventional design flow tools, [1-178] proposes to keep the use of the same Verilog-To- Routing (VTR) tool flow of FPGAs, but aims to replace Look-Up Tables (LUTs) by DG-CNTFET reconfigurable logic cells organized into *regular matrices*. The tool flow must therefore be adapted in order to handle the complexity of the new structures. To do so, a specific packing tool, called MPack, has been developed and inserted as a step of the design flow as shown in figure 1-29(b).

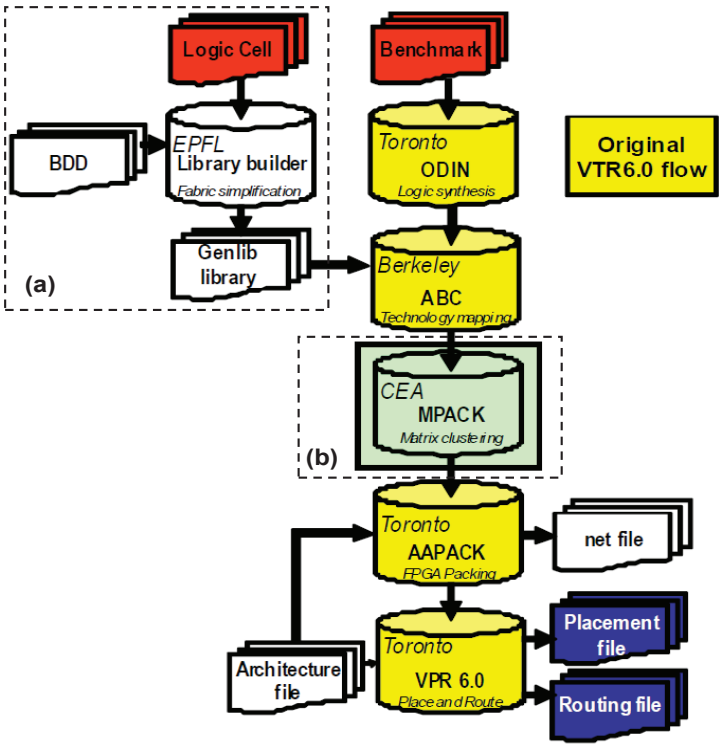


Figure 1-29. Disruptive technology compatible benchmarking flow diagram [1-178]

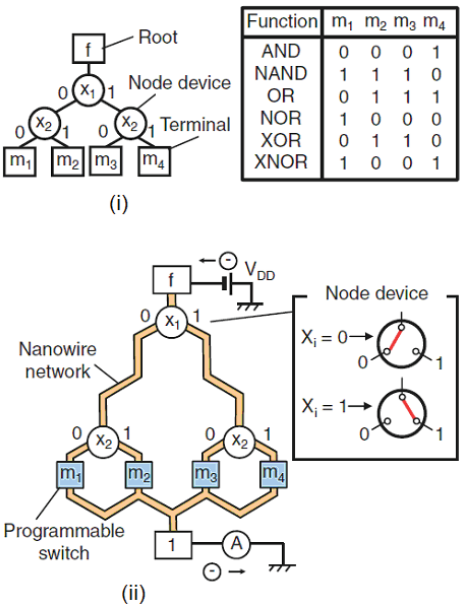
Such solutions can help designers towards a fast evaluation of emerging nanodevices. It avoids inventing the tool flow from scratch, and rather complements it to meet with designer requirements. In addition, it allows good compatibility with conventional electronic architectures and guarantees their efficiency.

1.3.3.2 Reconfigurable BDDs

Some research works focus on the implementation of conventional BDD (one cornerstone of EDA tools) with emerging technologies such as nanowire networks. In [1-179], a Compact Reconfigurable BDD Logic Circuit based on a GaAs Nanowires was described. To demonstrate the method and characterize it, a reconfigurable circuit of two-variable Boolean logics was fabricated on a GaAs etched nanowire network having hexagonal topology with Schottky wrap gates (WPGs) and SiN-based metal–insulator–semiconductor (MIS) gate programmable switches. By suitable programming of BDD terminals m_j, every two-variable logic function can be realized without changing this circuit configuration (Fig. 1-30(a)).

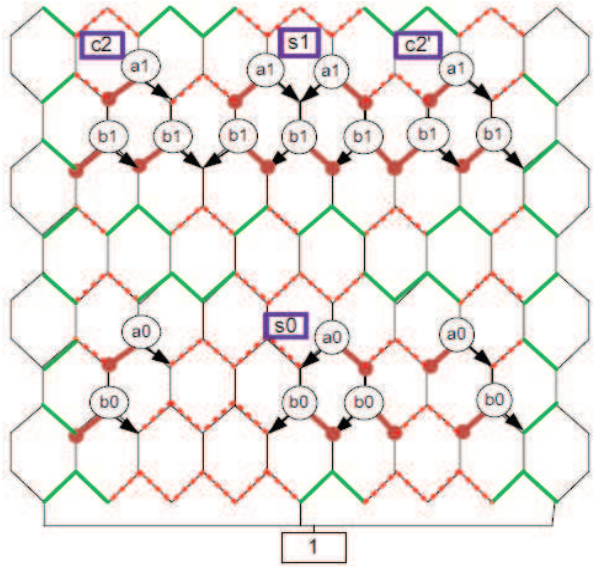
Other groups have tried to adapt synthesis techniques to innovative devices, such as the Quantum Multiple-valued Decision Diagram (QMDD) proposed for the efficient specification and simulation of reversible and quantum circuits [1-180, 1-181]. Unlike conventional BDD, QMDD has r^2 transition edges from each vertex (where r is the radix). The motivation for the QMDD structure comes from the regular structure of the matrices encountered for reversible and quantum gates and circuits. However, the notion of reconfigurability is not within the scope of this type of BDD. BDD reconfigurability was investigated in [1-182], where the authors incorporated a unique programmability feature in nanodot devices which can operate

in 3 distinct operation modes: a) active b) open and c) short mode, based on the split gate bias voltages and enabling functional reconfiguration. The reconfigurable BDD was based on Split-Gate quantum nanodots using III-V compound semiconductor-based quantum wells (Fig. 1-30(b)). However, the flexibility of the approach is lost in the reconfigurable fabric as the connections to the left and right edges are fixed at fabrication time (for every row). To solve this issue, additional architectural combinations and modified BDD mapping techniques are required [1-182].



Function	m_1	m_2	m_3	m_4
AND	0	0	0	1
NAND	1	1	1	0
OR	0	1	1	1
NOR	1	0	0	0
XOR	0	1	1	0
XNOR	1	0	0	1

a) Concept of a reconfigurable BDD circuit (i) Binary decision tree representing a complete set of two-input Boolean logic functions, and the table of m_j for major logic functions. (ii) Schematic of circuit architecture. [1-179]



b) 2-bit adder on a reconfigurable fabric. Programmable etching (dotted lines) or shorting (solid lines) when individual bias is applied to each split edge of a BDD node [1-182].

Figure 1-30. Reconfigurable BDDs based on emerging technology devices

Finally, we note that another key to reduce the gap between nanodevices and EDA, is to develop algorithmic approaches that can start with first principles based descriptions of novel nanotechnology and rapidly and reliably synthesize manufacturable designs. Several design tools are evolving this direction, with new customizable physical simulators, automatic parameterized low-order model extraction, and ever improving algorithms for robust optimization - new techniques that generate manufacturable designs by optimizing both system performance and robustness to manufacturing variations. In [1-183], many examples of algorithmic-based tools have been reviewed.

1.3.3.3 Conclusions

The EDA tool field is much wider than that presented in this chapter section. We limited our review to only some design approaches which are related to this thesis, such as reconfigurable BDDs and ambipolar cell-based libraries used by modified design tools. With

emerging nanodevices, the EDA field needs more inter-disciplinary collaboration to derive for example various levels of circuit and manufacturing models, to conduct various kinds of complexity analysis and to improve highly scalable simulation and synthesis methods, etc.

1.3.4 Conclusions of Computing with Emerging Technologies

This part of the chapter dealt with promising emerging technologies that may either sustain or replace CMOS technology as well as their corresponding novel architectures and tools. Special interest was given to the description of 1-D structures such as CNTs or SiNW, and to a particular variant of device that we call “Am-IDGFET”. This class of device was reviewed and many details about their fabrication and electrical behaviour have been given. Furthermore we highlighted its use in many works to build cells and architectures and finally we outlined how EDA tools can be used for emerging nanodevices such as SiNW, Quantum dots or CNTs. Design flow tools, standard-cell libraries and BDD synthesis technique have been adapted to fit with the capabilities of a new technology generation. The contributions of this thesis are mainly centered on the latter section “EDA tools”, where we aim to develop design approaches and logic synthesis techniques based on Am-IDGFETs and evaluate the benefits of such innovative logic through accurate simulations based on a compact device model.

1.4 Challenges and Thesis Contributions

In this section, we briefly describe the challenges facing EDA tools and their origins. Then, we explain how this work proposes design methodologies and CAD tools to exploit the capacities of Am-IDGFETs to build innovative logic design paradigms.

1.4.1 Challenges

At the time of writing, the first consumer-level CPU deliveries for the 22nm node started in April 2012. Consequently, new-generation EDA design tools for nanoscale CMOS chips started adopting computational quantum physics (density function theory, non-equilibrium Green's function, Wigner's function) to tackle nanoscale issues such as leakage currents through high-k gate dielectrics and so forth. For the beyond-Moore's-Law technologies such as carbon nanotubes, graphene and tunneling FETs, quantum dots, single electron transistors, and molecular devices, challenges are more complex. Because they’re still in their infancy; the manufacturing precision is low, resulting in significant statistical variability of each device’s key physical, chemical, and electrical properties. Thus, applications, architectures, and models must advance in parallel with efforts in devices and materials [1-176]. In spite of the considerable effort achieved by engineers and scientists that we tried to survey throughout this chapter, more research in architectures, methods, and tools are required to maximally leverage nanoscale devices to terascale capacity. Researchers need to synergistically incorporate several factors into traditional methods for reliable design synthesis to construct circuits that map efficiently to underlying nanofabrics and ensure reliable operation despite high levels of fault

rates [1-176].The new paradigm for nanoelectronics should be in a multi dimensional space covering devices, interconnects, architecture, circuit design, CAD, and fabrication issues.

The focus of this thesis concerns the exploitation of the potential of a new class of emerging devices to bring innovative computing paradigm with enhanced functionality. We present design approaches and CAD tools to automate the logic synthesis and the optimization of standard cells structures built with some emerging nanodevices. Another goal of the thesis is to validate and evaluate the design techniques proposed by electrical simulations based on accurate physical device models. The thesis work contributions are detailed below.

1.4.2 Research Contributions

Am-IDGFET is a new family of particular devices in view of the fact that it associates three benefits: (i) it is usually a 1-D electronic device (CNT or SiNW), meaning high mobility, achievable current density, theoretical transition frequency and high I_{ON}/I_{OFF} ratio; (ii) *Independently* controlled gates which offers the device extra logic options; (iii) ambipolar behaviour opens the way for N- and P-type polarity in the same device. Hence, the Am-IDGFET is considered as "*3 boons in 1 device*". We stress that *mustering* different technologies (CNT, GNR, SiNW) under the same flag of -promising candidates to fabricate Am-IDGFET- is very useful from a logic design point of view. The more points *in common* devices have, the more universal design approaches and techniques. The creativity of the thesis work consists of looking at this new class of emerging technology as an opportunity for new design paradigms. Then, many options become available in ambipolar technology with no equivalent counterparts in CMOS technology. There is no doubt that this new design paradigm is promising. Nevertheless, this approach requires design approaches and tools to build a feasible and complete picture of ambipolar logic. Thus, it will be required to revise or reinvent many existing logic synthesis, design methods, and evaluation techniques to automate the design and handle the device opportunities for an optimized logic. As shown in figure 1-31, this work proposes a novel paradigm of design methodologies and techniques to help designers dealing with emerging technologies. The opportunities provided by ambipolar DGFETs are exploited according to two design axis; standard-cells and reconfigurable logic with evaluation of the proposed design approaches, based on a solid physically compact model of a DG-CNTFET device.

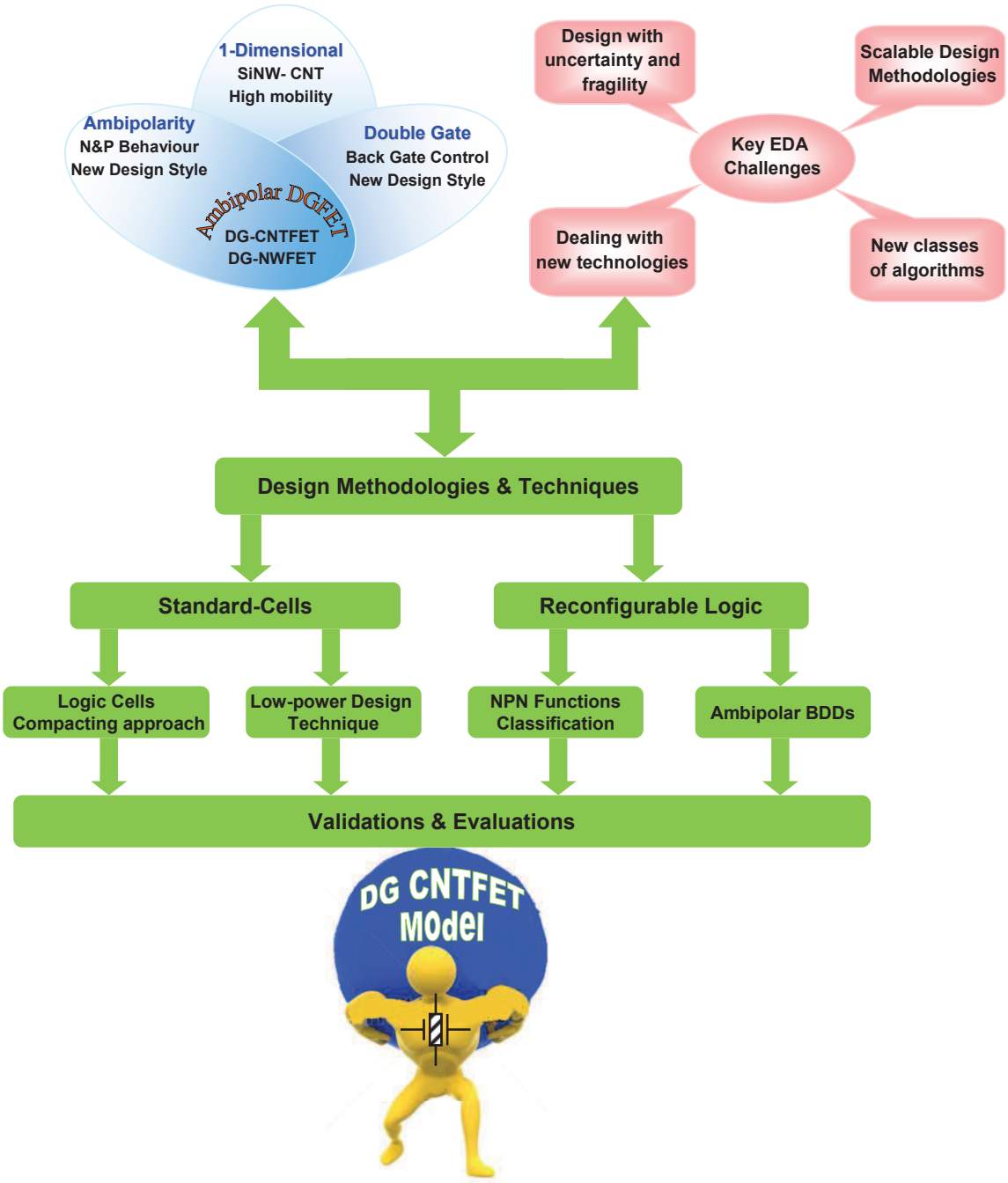


Figure 1-31. Diagram of the thesis organization

Standard cells: It is conceivable to have a cell-based design methodology for synthesizing terascale integration circuits. Here, key logic cells are designed based on appropriate nanodevice composition and stored in a cell library for use by the synthesis tools. Properties of standard cells forming the library in the extended space of delay, power and area have a direct impact on final generated circuits. Also, the regularity of logic structures is highly required at the nanoscale to enhance reliability and solve issues related to the fabrication process. Based on Am-IDGFETs, we describe a design approach to improve the compactness of standard logic cells. While the main goal of the design technique is to achieve less area with more compact logic structures, a significant improvement of circuit performance is also highlighted.

Furthermore, the design technique is applicable in both static and dynamic logic styles. In the same context of standard gates, power consumption represents a hurdle at nanoscale integration. With Am-IDGFETs, this becomes even worse due to some issues connected to their physics and structures. But given the high potential of the devices, we may be able to work around this inherent drawback by applying specific techniques at the design level to dynamically lower the power consumption.

Reconfigurable logic: The concept of reconfigurability offers much for computing systems. With Am-IDGFETs, an innovative prospect of reconfigurability is possible thanks to its second gate. Synthesizing and mapping VLSI circuits and systems onto fabrics and dynamically reconfiguring the fabric to match the application needs requires sophisticated design methodologies and tools. Two methodologies are proposed in this thesis. The first method matches the capacity of Am-IDGFETs to switch between 3-states to the capacity of the NPN classification tool to manipulate Boolean functions. Based on a certain correlation between logic structures of Boolean functions classes, reconfigurable logic cells are designed. The second method is inspired from conventional EDA tools, the BDDs. To fit to the new functionality of Am-IDGFETs, BDDs are reshaped. New steps and rules for Ambipolar-Binary-Decision-Diagrams (AmBDDs) are defined to generate multi-function reconfigurable logic circuits from scratch.

Validation and evaluation: We must be able to compare the new Am-IDGFETs-based circuits against existing silicon-based fabrics, and more generally, any other competing fabric. This requires developing a comprehensive, modular, and flexible evaluation platform to compare and contrast the competing nanocircuit and architectures in terms of the key performance metrics: such as density, latency, power dissipation, and so forth. For use in circuit simulations, we need to freshly model newly conceived nanodevices with a different way from conventional CMOS models. While device modeling builds on a deep-rooted modelling framework, compact physics-based models are required for accurate simulation results with Am-IDGFETs, as emerging technology nanodevices. A part of the ANR research project “Nanograin” to which this thesis work mainly contributes, is devoted to compact modelling of an Am-IDGFET in the case of CNT technology. Thus, our simulations are based on the IMS research team model, which represents the first physically accurate model of a DG-CNTFET with efficient convergence and simulation speed compatible with circuit design. We do not limit the appraisal of the design approaches to CNT technology, but we set an exhaustive comparison with the most advanced CMOS technology node available in literature by using a predictive model 16nm CMOS technology.

1.4.3 Organization of Thesis

The thesis is organized in three main chapters not including the introduction and the conclusions chapter.

In **Chapter 2**, we exploit Am-IDGFETs to cope with two nanodevices challenges, the need for regularity and high power consumption. At first, we propose a design approach to build regular compact logic structures in dynamic and static logic styles with high performance and comparable power consumption. Then, we define a low-power design technique to dynamically lower static and short-circuit power in Am-IDGFETs -based logic circuits.

In **Chapter 3**, we intend to cross borders of current CAD tools for synthesizing optimal logic for emerging technology. We reshape some CAD tools and reinvent design techniques to meet with the unique ability of Am-IDGFETs to synthesize fine-grain reconfigurable logic. NPN Boolean function classification was initially exploited to build reconfigurable ambipolar logic. Thereafter, BDDs were adapted to fit to the three-switching-states of ambipolar devices in order to achieve optimal logic and build reconfigurable logic cells from scratch.

In **chapter 4**, we confront the issue of validation and evaluation of emerging technology based circuits by utilizing a compact DG-CNTFET device model developed on solid physical basis. With accurate electrical simulations we were able to compare the logic circuits designed throughout the thesis, in chapter 2 and 3, with their CMOS counterparts in both standard-cells and reconfigurable logic contexts. Thus, we could highlight advantages and drawbacks of the proposed design methodologies and envisage the best scenarios.

In **Chapter 5**, the thesis is concluded and possible future works are outlined.

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Chapter 2

Ambipolar Independent Double Gate FETs for a New Paradigm of Standard logic cells

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Abstract

This chapter deals with standard logic cells at two levels. Firstly, we propose a circuit design approach to achieve compact logic circuits with ambipolar Independent-double-gate devices (Am-IDGFET), merging every two-transistors in series (TTS) structure using the in-field controllability via the back-gate of ambipolar devices. The approach is demonstrated for two logic styles: with a complementary static logic design style, it demonstrates an efficiency that can improve the compactness of logic structure by a factor of 2X; while with a dynamic logic design style, a gain of 30% of gain in terms of transistors count is achieved for a variety of application scenarios. Secondly, we propose a design approach to improve power consumption in digital circuits. It *dynamically* lowers the dynamic power (specifically the short-circuit power) during the active mode and significantly decreases the static power during the inactive mode. Preliminary observations showed an average improvement of 3X in total power consumption compared to conventional structures, with a decrease by a factor of 4X in short circuit power, and of 100X in static power (during the standby mode). This technique represents an attractive solution to the issues usually present in ambipolar FETs with channels composed of carbon nanotubes, graphene or undoped silicon nanowires; (i) V_{DS}-dependent I_{OFF}, which is a source of high leakage, as well as (ii) low V_{th}, which is a mixed blessing factor, since it achieves high speed but it increases short-circuit power.

2.1 Introduction

Along with advances in semiconductor manufacturing, the standard cell methodology has helped designers over several decades to scale ASICs from comparatively simple single-function ICs (of several thousand gates), to complex multi-million gate system-on-a-chip (SoC) devices. The methodology is based on a combination of automated design tools and libraries of standard cells, which are today a fundamental part of the design process. Such libraries clearly define several variants and logic styles per functionality which, while allowing optimization according to environment, area, delay, and power constraints, avoids low-level optimization and high design overhead. Nevertheless, with the aggressive scaling of CMOS technologies, new restrictions have emerged at the nanoscale device. Indeed, due to the nature of molecular-scale circuitry, designers must add a new constraint (reliability) to the optimization equation. It is necessary to analyze how the reliability of standard cells changes as devices shrink further and to identify the origins of faults.

At the manufacturing level, photolithography can be identified as the main hurdle against the reliability of nanoscale logic circuits. Today, photolithography teams are not able to completely validate a technology process for any design pattern due to the mutual effects on neighboring patterns and the large number of possible patterns within a standard library that create catastrophic proximity effects. This has an impact at several design levels. For instance, variability affecting the line width (leading to discrepancy between the drawn and physical dimensions) affects basic transistor parameters such as channel length. This causes a large variability in the device current, which in turn influences the system design by causing variation in the delay and power dissipation [2-1].

To overcome photolithography limits and in particular proximity effects, *macroregularity* becomes highly desirable at the circuit level [2-2] and enables accurate and optimized validation of cells in a known layout. FPGAs and memory cells are examples of circuits best reflecting the benefits of macroregularity. Due to their programmability and the fact that the spatial localization of an individual cell has no relationship to the overall functionality, they also demonstrate a certain degree of intrinsic redundancy. For this reason, they are often the first product to come to market in a new technology process, and illustrate a growing trend: redundancy and regularity are increasingly attractive and necessary for the design of high-performance robust systems [2-3, 2-4] in CMOS technology.

In emerging (nanoscale) technologies, the need for regularity is even more primordial because of the enormous challenges in device fabrication, as well as circuit- and system-level design and CAD tools. Self-assembly of quasi-one dimensional devices is an attractive and natural approach for fabrication from the point of view of cost- and time-efficiency [2-5]. This technique yields dense and regular arrays of the considered structures (organized in parallel or perpendicular layers), and can be naturally associated to build larger regular *fabrics*. A regular

fabric is a set of resources (usually logic gates, memory, or interconnect) laid out in a regular manner, and that can be mask- or in-field configured to implement specific logic functions. Various forms of regular gate and logic arrays have been recently proposed to reduce the design risk caused by the increasing variability at the current and future technology nodes [2-6, 2-7, 2-8, 2-9, 2-10].

In this chapter, we firstly aim to define a design methodology in order to improve the compactness and the speed of standard logic cells at comparable power consumption. The configurable polarity of ambipolar DGFETs is exploited to produce logic gates with reduced area and improved speed. Compared to CMOS technology, the design approach opens up the opportunity to implement in a very efficient and compact way complex logic functions such as XOR, MUX and many other gates. This offers the ability to build efficient standard cell libraries for resourceful technology mapping. The proposed approach is generic, and we demonstrate its flexibility for various logic styles. In the second part of the chapter, we focus on a design technique for standard cells utilizing Am-IDGFETs to decrease dynamically both components of power consumption. Using the back-gate of ambipolar devices, the short-circuit power can be avoided during the active mode, and also the static power can be decreased during the inactive mode.

2.2 Generic design approach for improved logic structures based on Am-IDGFETs

In CMOS standard logic cells, transistors in series structures exist both in N- and P-networks to implement logic function minterms and maxterms respectively. As the gate fan-in increases, so too does the complexity of the minterms/maxterms and the number of transistors in series. This leads in CMOS structures to high branch resistance and slow gate response. This issue, which is key to digital circuit performance, can be efficiently improved by utilizing independent Double Gate Field Effect Transistors (IDGFET). In this section of the chapter, we describe a generic circuit design approach achieving compact logic structures by merging same-type (P or N) two-transistors in series structures into a single IDGFET. The approach is demonstrated with ambipolar double gate transistors. The use of such devices, in a dual gate context, offers in-field controllability. Through the evaluation of gates in a dynamic logic style, we investigate the possible forms of application and consequent impact on the transistor count. For static logic structures, we apply the approach in a generic way and illustrate the benefits through the design and evaluation of several examples of gates. Before describing the concept of the design approach, we illustrate the impact of transistors in series on time delay. Then, we review some techniques to reduce transistors count in logic circuits.

2.2.1 Impact of transistors in series on time delay

The principle goal of reviewing examples of delay models in this section is to highlight the importance of the presence of series connected transistors and explore their fundamental impact on logic circuit performance.

Series connected FETs, as shown in figure 2-1 (a), are used in various logic families including dynamic logic families, static CMOS gates and pass-transistor logic circuits. They have a decisive impact on delay, power and area. This is why many compact delay models for series connected FETs have been derived especially to predict worst-case delay accurately in logic circuits. Formulas (1), (2), (3) and (4) are taken from various delay models for series connected FETs [2-11, 2-12, 2-13], respectively.

The simplest and oldest way to estimate the delay is to use Elmore delay rules [2-11]. In this case, drain and source capacitances are taken in consideration. In the Elmore delay model, transistors are modeled as resistors and the delay T can be calculated using the Elmore delay rules:

- C_L is equal to the total capacitance at V_{out}
- R_1, $R_2 \ldots R_N$ are the equivalent resistances of the MOSFETs M_1, $M_2 \ldots M_N$ and C_1, $C_2 \ldots C_{N-1}$ are their drain/source capacitances, as shown in figure 2-1 (b).

$$T = 0.69 \times \left(R_1 C_1 + (R_1 + R_2) \times C_2 + (R_1 + R_2 + R_3) \times C_3 + \ldots + (R_1 + R_2 + \ldots + R_{N-1}) \times C_{N-1} + (R_1 + R_2 + \ldots + R_N) \times C_L \right) \quad (1)$$

Assuming all transistors to be of equal size leads to $R_1 = R_2 \ldots = R_N = R$ and $C_1 = C_2 \ldots = C_{N-1} = C$, so that the delay expression can be simplified to:

$$T = 0.69 \left(\frac{N^2 - N}{2} R.C + N.R.C_L \right) \quad (2)$$

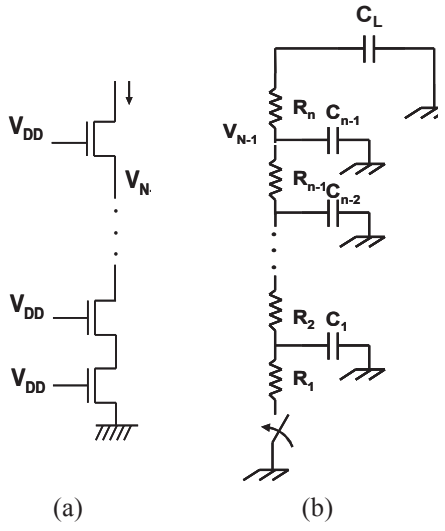


Figure 2-1. Series connected FETs (a) transistors schematic (b) Elmore delay rules schematic

In [2-12], Sakurai describes a model for series connected transistors when the drain/source capacitance is small compared to the load capacitance, such that they are assumed to be negligible. In this case, the ratio of the delay of Series Connected FETS (SCFS) to the delay of a single transistor, as a function of the number of transistors N is:

$$F_D = \frac{delay(SCFS)}{delay(inverter)} = \frac{I_{DSAT}}{I_{DN}} = 1 + \frac{1-1/\sqrt{2}}{1-1/\sqrt[q]{2}} \frac{V_{DSAT}}{V_{DD}-V_{TH}}(1+\gamma_1)(N-1)$$
$$\approx 1 + \frac{1}{2}\alpha \frac{V_{DSAT}}{V_{DD}-V_{TH}}(1+\gamma_1)(N-1) \quad (3)$$

F_D is the ratio of the delay of N transistors in series to the delay of a single transistor discharging the same load capacitance. I_{DN} is the equivalent current of the SCFS and N is the number of transistors in series. I_{DSAT} is the drain current when $V_{GS}=V_{DS}=V_{DD}$, while V_{DSAT} is the drain saturation voltage when $V_{GS}=V_{DD}$ and V_{TH} is the threshold voltage with body bias, α is an empirical parameter and γ_1 is the body bias factor.

This model is in good agreement with the delay of normal static logic gates where the load capacitance, C_L is large compared to the drain/source capacitances. However, it provides inaccurate results with *dynamic* logic gates where drain/source capacitance is not negligible with respect to the load capacitance. This issue was resolved in [2-13] by Shakeri who derived a compact delay model that can be used to calculate the delay of series connected MOSFETs used in any logic family. In this work, the delay was decomposed into two components: T_1 is the delay induced by drain/source capacitors, calculated using a transfer function with a Laplace Transform; and T_2 is the delay induced by the load capacitance, calculated using Sakurai's model. Based on the Elmore delay rules, T_1 and T_2 are combined to define the overall delay, as shown in formula (4).

$$Delay = T_1 + T_2 = \frac{RC \cdot N \cdot (N-1)}{R_N + (N-1)R}\left[\frac{R_N}{2} + R \cdot \left(\frac{N}{6} - \frac{1}{3}\right)\right] + \frac{C_L V_{DD}}{2 \cdot I_{D0}}\left(1 + \frac{1}{2}\alpha \frac{V_{DSAT}}{V_{DD}-V_{TH}}(1+\gamma_1)(N-1)\right) \quad (4)$$

This model proved accurate prediction of delays for various logic families. It also provides insight into how device parameters impact on delay, and key results show that the relative delay of series connected MOSFETs is almost invariant for different generations of technology. Although every model is better fitted to a specific logic family with disparities between the complexity and the accuracy of the corresponding formulas, we clearly see that the number of transistors N is the basis of the delay determination.

2.2.2 Conspectus of techniques and technologies to reduce transistor count

Reducing transistor count in logic switching networks is a critical vector to improving circuit performance because *propagation delay* depends on the number of transistors in series in a logic function path (as it was shown in section 2.2.1), while circuit *area* obviously depends also on the number of transistors and their channel sizes. *Dynamic power* dissipation

is to a large extent governed by output node capacitance, which in turn is a function of the same parameters that also control circuit size. For the Static power, it mainly depends on the OFF current of devices (I_{OFF}). In view of this fact, several works in the literature focus on methods and tools to reduce transistor count in circuits at various levels.

2.2.2.1 Circuit design level

Some works suggest efficient design at the transistor level, by demonstrating that the use of complex gates gives a better solution in terms of power and delay over the traditional basic standard cells [2-14]. This has been demonstrated with a full adder [2-15] and with an XOR gate [2-16]. Other approaches use a logic style requiring fewer transistors such as pass-transistor logic [2-17, 2-18] or dynamic logic [2-19]. Furthermore, in [2-20] an approach using an algorithm was developed to reduce the total transistor count in sign-select Booth encoding circuits, and a design methodology was patented in [2-21] to reduce logic circuit design by one or more stages. Possani et al. proposed an edge sharing method, on a graph structure, to generate optimized transistor networks [2-22]. All these works were based on conventional MOSFET devices, where the main focus was on how to implement a Boolean function or truth table at the transistor level by using the minimum number of devices. However, as novel device structures and geometries emerge, further design opportunities exist to go optimize transistor count.

2.2.2.2 Device Technology level

From the technology point of view, performance scaling has led to the investigation of novel transistors which could also reduce transistor count in logic circuits, such as Floating Gate transistors [2-23] and the neu-MOS transistor structure using complementary GaAs HIGFET transistors [2-24]. In this context, four-terminal devices such as multiple gatestructures have also shown potential to develop new logic gates with a significant decrease in transistor count, with for example FinFETs [2-25]. Also, recent research utilizes the properties of independent-gate FinFETs (IG-FinFET) to design a 3-transistor FinFET NAND gate [2-26]. In [2-27] the author extended this property beyond a simple logic gate such as a NAND gate and proposed a general methodology for effectively synthesizing logic circuits by using both gates of FinFETs as inputs to obtain an equivalence of two transistors in parallel. Although the synthesized FinFET logic circuits achieve significant area and power reduction, they suffer greatly in circuit speed. It was mainly due to a high threshold voltage and a weak I_{DS}/V_{GS} slope.

Among four-terminal devices, ambipolar DGFETs such as DG-CNTFET (DG-Carbon Nanotube FET) [2-28], DG-GFET (DG-Graphene FET) [2-29], DG-OFET (DG-Organic FET) [2-30, 2-31] and DG-NWFET (DG-Nanowire FET) [2-32], reviewed in the first chapter, allow innovative techniques for the design of digital circuits and have shown attractive performance metrics in many works [2-28, 2-29, 2-33, 2-34, 2-35, 2-36, 2-37, 2-38].

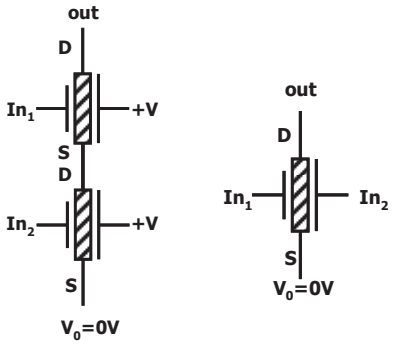
For instance, in [2-33] the author suggested to build a new library of ambipolar gates where an XOR gate was utilized as a pass-gate.
The approach presented in this chapter shows the potential of Am-IDGFETs to build logic gates with a lower number of transistors, and unlike the logic circuits generated with IG-FinFET in [2-27], the design approach allows faster logic while maintaining comparable power consumption figures with conventional logic gates and improved compactness. Also, unlike [2-33], the approach is not based on an XOR gate to build other gates, but is more generic and can be applied to any logic circuit independently of the logic style used. This approach can be based on any type of Am-IDGFETs.

In this section, we begin by presenting the general principle of the circuit theory which is the cornerstone of the whole generic approach to generate compact logic circuits. We then apply this concept to two different logic styles (static logic and dynamic logic) and illustrate the approach with logic gate examples. We stress that the devices on which this work is based are ambipolar independent double gate FETs with the abbreviation Am-IDGFETs . Here, the Back-Gate (BG) signal is considered to be a free independent variable.

2.2.3 General concept

In addition to the load capacitance and drain/source capacitance, we have seen from delay models detailed in section 2.2.1 that the number of transistors in series is the heart of the delay estimation. The more in-series transistors we have, the larger the delay. Indeed, the equivalent logic path resistance is proportional to the number of minimum-length transistors in series, and inversely proportional to the average transistor width. Hence, two N-type transistors in series (NTTS structure) or two P-type transistors in series (PTTS structure) must either demonstrate a path resistance of $2R_{ch}$ with no transistor resizing or an input gate capacitance of $2C_g$ with transistor width doubling to reduce overall path resistance (where R_{ch} and C_g represent the channel resistance and gate capacitance of a single minimum width transistor, respectively). Hence two transistors in series (TTS) structures are critical for path resistance and gate capacitance optimization, with consequent impact on delay, power and area. The switching between the N- and P-states in Am-IDGFETs allows TTS structures to be substituted by a single Am-IDGFET with no loss of functionality as shown in figures 2-2 and 2-3 for the NTTS and PTTS structures respectively. Since the idea of this work is to develop a generic approach to merge every two transistors in series into a single device, it will be abbreviated along the paper as TTSM approach (Two-Transistors-in-Series-Merger approach).

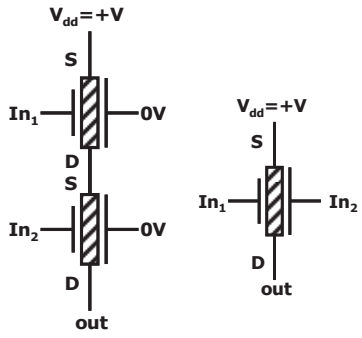
In the TTS structure, we assume that the properties of both transistors are identical (i.e. they have the same width, length, threshold voltage and saturation current, and operate at the same temperature), so that, if the same terminal voltages were applied to both devices, their channel currents would be identical.



(a) (b)

Figure 2-2. Direct transposition of CMOS-NTTS structure with Am-IDGFETs (a), Single Am-IDGFET equivalent to a TTS structure (b)

In the initial NTTS structure in figure 2-2(a), both transistors are N-type since the back gate BG is set to +V and V_0 is set to 0V (i.e. V_{BG}-V_S=+V). In this case, a path is established between "V_0" and "out" only for In_1In_2="11". In the single Am-IDGFET structure, shown in figure 2-2(b), the same condition is true since for In_2="1", the back gate BG is set to +V such that the transistor is N-type and will be ON only if In_1="1" also. For other combinations In_1In_2= {"01","10","00"} the transistor will be OFF. Thus, the NTTS structure can be replaced by a single Am-IDGFET.



(a) (b)

Figure 2-3. Direct transposition of CMOS-PTTS structure with ambipolar DGFETs (a), Single ambipolar DGFET equivalent to a TTS structure (b)

By analogy, the PTTS structure in figure 2-3(a) obtains the same benefit since both transistors are P-type when the back gate BG is set to 0V and V_{dd} is set to +V (i.e. V_{BG}-V_S=-V). In this case, a path is established between "V_{dd}" and "out" only for In_1In_2="00". In the single Am-IDGFETstructure, shown in figure 2-3(b), the same condition is true since for In_2="0", the back gate BG is set to 0V such that the transistor is P-type and will be ON if In_1="0". For other combinations In_1In_2= {"01","10","11"} the transistor will be OFF.

2.2.3.1 Double Gate static logic (DGSL) cells

The TTSM approach can be applied to the design of many logic gates. In this section, we introduce the opportunities for use of the approach in generic complementary static logic

structures based on conventional CMOS technology, and analyze the benefits of the structure resulting from application of the TTSM approach based on Am-IDGFETs.

a. ***Generic function***

Using the TTSM approach, we can replace any NTTS or PTTS structure in static logic pull-down and pull-up networks respectively with equivalent ambipolar Am-IDGFET. A generic example illustrating the transformation between a Conventional CMOS Static-Logic (CSL) structure and the Double-Gate Static Logic (DGSL) structure (which deploys the TTSM approach) is shown in figure 2-4. In the figure, transistors constituting networks are presented arbitrary. The purpose of the figure is just to show that the TTSM approach can be utilized in both networks. Accurate examples are shown later.

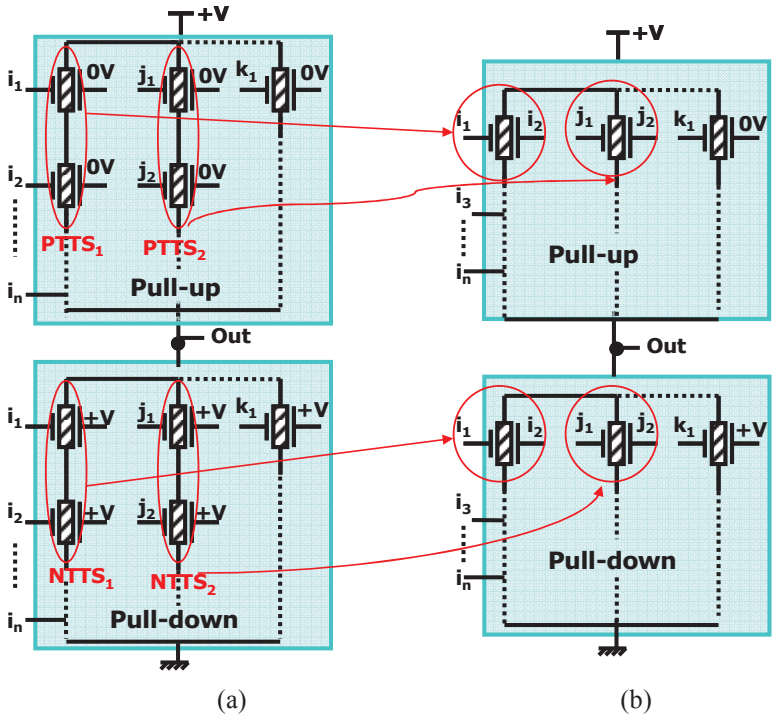


Figure 2-4. CSL structure (a), DGSL structure (b)

If we consider *n* to be the number of inputs of the function implemented in a conventional complementary static logic way (CSL structure), *m* the number of NTTS structures and *p* the number of PTTS structures in the function path, then it is clear that the obtained DGDL structure requires *2n-(m+p)* transistors instead of *2n*. Consequently, a more compact structure (with fewer transistors) can be achieved using the TTSM approach.

b. ***Examples of gates***

The approach can be applied to any complementary static logic gate containing TTS structures. In for example simple monotonic gates, such as the NAND (resp. NOR) gate, where the pull-down (resp. pull-up) network contains one NTTS (resp. PTTS) and the pull-up (resp. pull-down) network is formed from 2 transistors in parallel, only the pull-down network is substituted with a single Am-IDGFET and we obtain a gain of a single transistor. However, in

the case of more complex gates where more transistors in series are used, such as XOR/XNOR gates and multiplexers, the gain can be more significant and the approach can be applied to all branches of the gate.

The conventional CMOS-type 2 input XOR structure (CSL) is shown in figure 2-5(a). We note that in figure 2-5(a), we choose to connect the back gates of the pull-up transistors to the ground and the back gates of the pull-down transistors to V_{dd}. This choice is not strictly necessary - we could connect the back gates to any voltage as long as the condition holds that the polarity of the device is set to N- or P-type with a positive (V_{BG}-V_S= +V) or negative (V_{BG}-V_S= -V) voltage, respectively.

By applying the approach to this gate, figure 2-5(b) shows a compact XOR gate where all TTS structures were substituted with a single Am-IDGFET, leading to a reduced transistor count with a simpler structure of 4 transistors instead of 8. Figure 2-5(c) shows simulation results with the transistor model and under the conditions detailed in chapter 3.

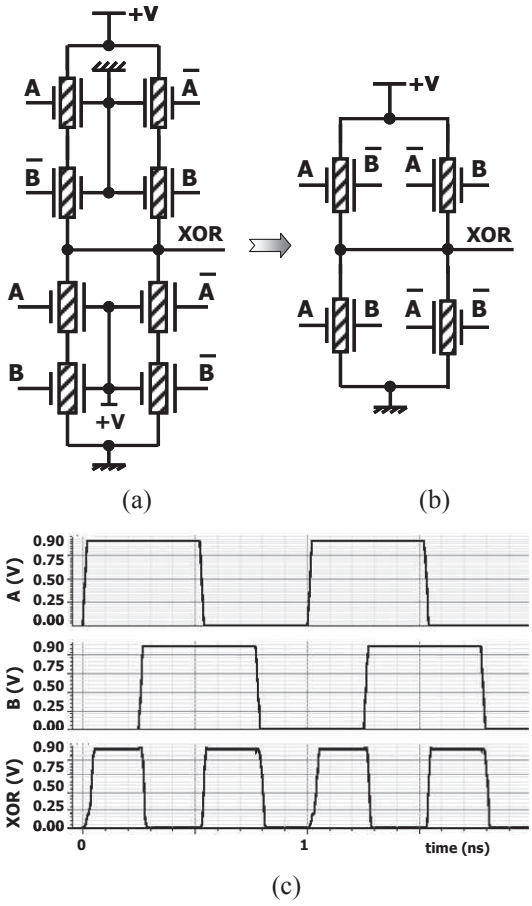
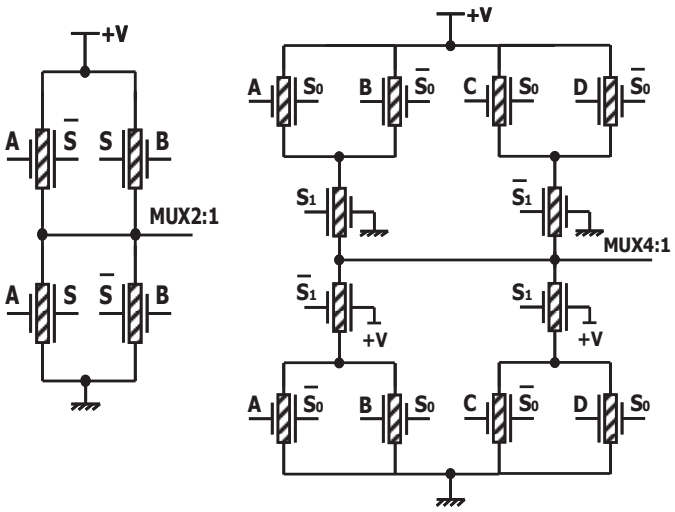


Figure 2-5. 2-input XOR gate: CSL structure(a) DGSL structure (b) DGSL simulated waveform (c)

To further illustrate the principle of the DGSL cells, some examples of elementary circuits are shown in figure 2-6. The structure of the static logic 2:1 MUX is very similar to the XOR gate, and a similar gain in terms of transistor count is observed. In the case of the static logic

4:1 MUX, 8 transistors fewer are used than in the conventional structure, i.e. a reduction of 40% is observed rather than 50% as in the 2:1 MUX or the XOR gate.



(a) (b)

Figure 2-6. DGSL 2:1MUX gate (a), DGSL 4:1MUX (b)

c. ***Achievements***

By applying the TTSM approach to a complementary static logic structure, we showed its ability to decrease the transistor count in static logic gates leading to more compact logic structures. The gain in terms of transistor count can attain up to 2X with some gates. Obviously, the more transistors in series a logic structure uses, the more efficient the approach. With static logic structures, it was possible to apply the TTS approach in both pull-up and pull down networks. In the next section, we aim to explore the capability of the approach with a dynamic logic style.

2.2.3.2 Double-Gate Dynamic Logic (DGDL) cells

The logic cells described in this section are derived only from dynamic-logic, known for its ability to reduce the transistor count within a logic cell. We aim to prove that by the application of the TTSM approach it is possible to reduce the transistor count even further according to three different scenarios that are detailed in this section. A simple example of a 3-input NAND gate will be our starting point to describe these scenarios, and we then generalize each scenario for *n*-input dynamic logic cells, illustrated by further examples of logic gates. However, since the dynamic logic style in general can use a pull-up or a pull-down network, as well as one or several clock signals, we define as a first step the general structure of the dynamic logic on which all the work in section is based.

a. ***Dynamic logic structures***

In the conventional approach, a dynamic logic style leads to a transistor count of *n+2* (where *n* represents the fan-in), rather than *2n* in a functionally equivalent static-logic implementation. This reduction is due to the elimination of the complementary network

(usually pull-up or PMOS) and the addition of two clock-driven transistors (precharge and evaluation), as shown in figure 2-7.

To build a dynamic logic structure there are two possibilities. The first is to use a p-type transistor for the precharge phase (connected to power supply V_{DD}) in order to avoid logic degradation for the "1" state, and utilize n-type transistors for all the other devices (evaluation transistor and function path transistors). The second possibility is to use an n-type transistor for the precharge phase (connected to ground G_{nd} in this case) and use p-type transistors for all the other devices (evaluation transistor and function path transistors). Since N-type and P-type transistors in Am-IDGFETs represent symmetric behavior, we choose to illustrate the proposed approach with the first topology (figure 2-7) and consider that the application of the approach and its corresponding results still hold with the second topology.

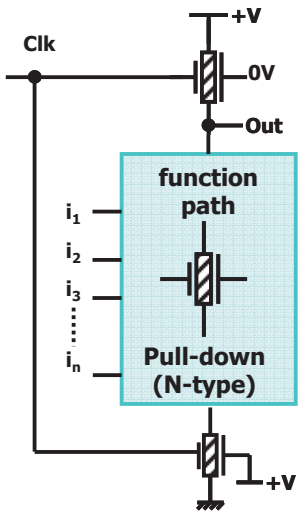


Figure 2-7. Conventional Dynamic Logic structure

In [2-39], a family of standard dynamic logic cells was built with Am-IDGFETs, with a variety of cases in which single or multiple clock signals can be utilized. In the case of multiple clocks, some issues are apparent, such as logic level degradation. In addition, the use of many clocks in a logic circuit will certainly exacerbate the timing issues usually encountered with clock signals, such as skew (spatial variations in clock edges), jitter (temporal variations in clock edges) and variation of clock pulse width, all caused by non-idealities of clock generation and distribution structures. This leads to defective logic and impacts critically circuit performance. Furthermore, the higher the number of clock signals, the more complex the consideration of their distribution (types of interconnections and metal layers used for routing clocks, overall shape of the network, fanout of clock drivers and buffers, load balancing, rise/fall time of clocks, skew specifications, etc). To avoid/limit those difficulties, we chose to apply the TTSM approach to dynamic logic gates using a *single* clock signal (figure 2-7). But, careful consideration should be given to the transition time of the single clock approach which can dramatically increase power consumption.

The next part of this section describes three different scenarios using the TTSM approach with a dynamic logic style.

b. ***TTSM approach applied to a dynamic logic structure: Three possible scenarios***

There are several possible structural variants that can be implemented to apply the TTSM approach in a dynamic logic structure. To analyze the pros and cons of the various scenarios, we illustrate their application through the example of a 3 input NAND gate. In this case, three different possibilities to apply the TTSM approach, as shown in figure 2-8. In the first scenario (S1), we keep both *evaluation and precharge* transistors and apply the TTSM approach *inside the function path block*. In the second scenario (S2), we present a dynamic structure where *only a precharge* transistor and merge the *evaluation* transistor inside the function path block. Finally, the third scenario (S3) describes specific cases where it is possible to combine approaches from both scenarios 1 and 2.

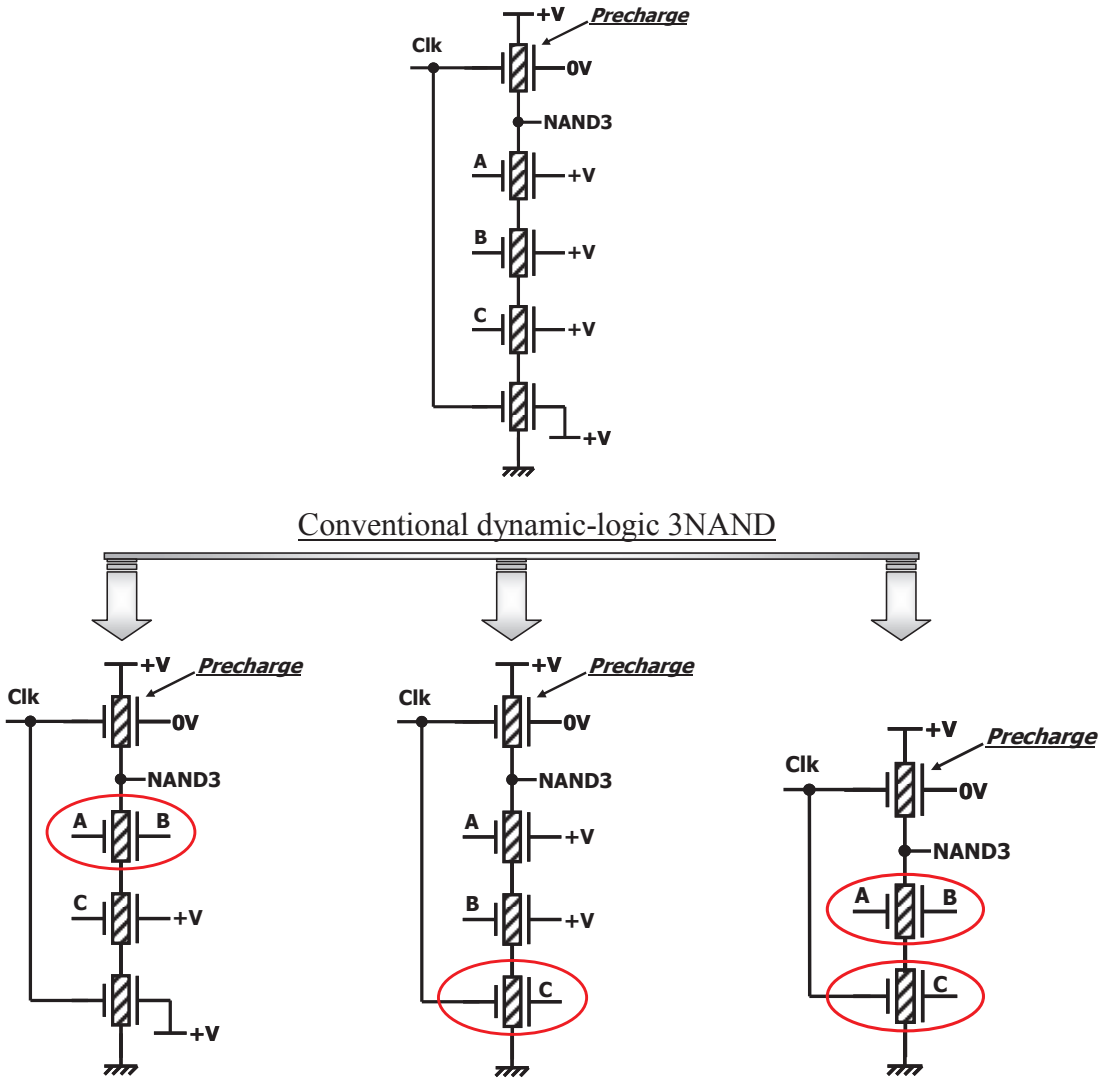


Figure 2-8. 3NAND descriptive example of the three possible TTSM scenarios

As explained previously, the logic structure is based on N-type function path blocks, such that domino-type logic is not precluded and will not require output inversion when considering cascaded logic blocks. Generic examples illustrating the differences between a Conventional CMOS-like Dynamic-Logic (CDL) structure and the DGDL structure after deploying the TTSM approach are shown in figures 2-9, 2-10 and 2-11, respectively for scenario 1, scenario 2 and scenario 3. Am-IDGFETs can be placed in series branches (for AND functions), parallel branches (for OR functions) or any combination of series and parallel branches, as with conventional CMOS. All circuits implement the output function:

$$Out = \neg(Clk \wedge [(i_1 \wedge i_2 \wedge i_3 \wedge ... i_n) \vee (j_1 \wedge j_2) \vee (k_1)]).$$

- ***Scenario 1 (S1): TTSM approach within the function path block***

In the first scenario (S1), to build a generic approach for the design of DGDL cells, we set up the TTSM approach within the function path block while retaining the conventional dynamic logic precharge and evaluation transistors (Fig. 2-9).

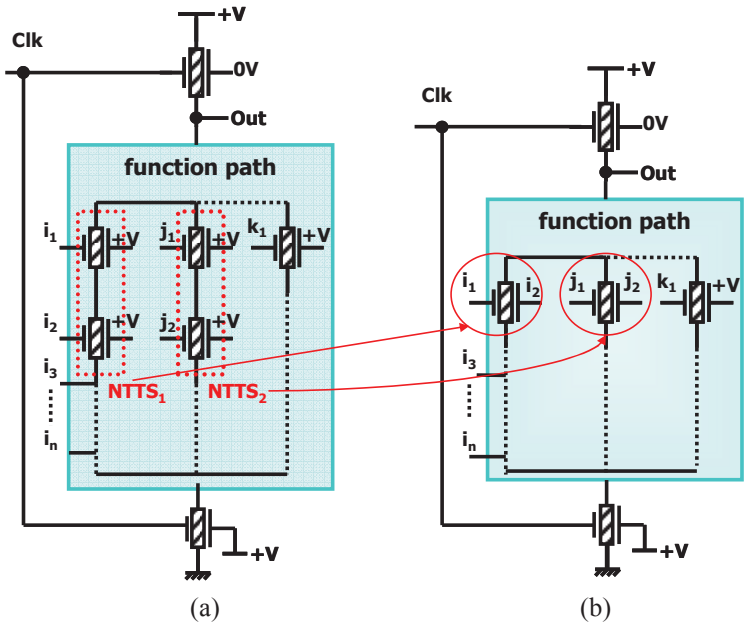


Figure 2-9. CDL structure (a), S1-DGDL structure (b)

If we consider that *n* is the fan-in and m is the number of TTS structures that can replace two AND-related inputs in the function path, the required number of transistors will be *n+2-m* rather than *n+2* as normally required by conventional dynamic logic design.

- ***Scenario 2 (S2): TTSM approach to merge the evaluation transistor into the function path***

In the second scenario (S2), we structure of the function path is identical, but the evaluation transistor is replaced by connecting the evaluation signal directly to the back gates of at least one Am-IDGFET in each branch of the function path from the output node to ground (Fig. 2-10). In fact, all function path transistor back gates could be connected to the evaluation signal,

which would lower leakage current but would also increase the load on the evaluation clock signal.

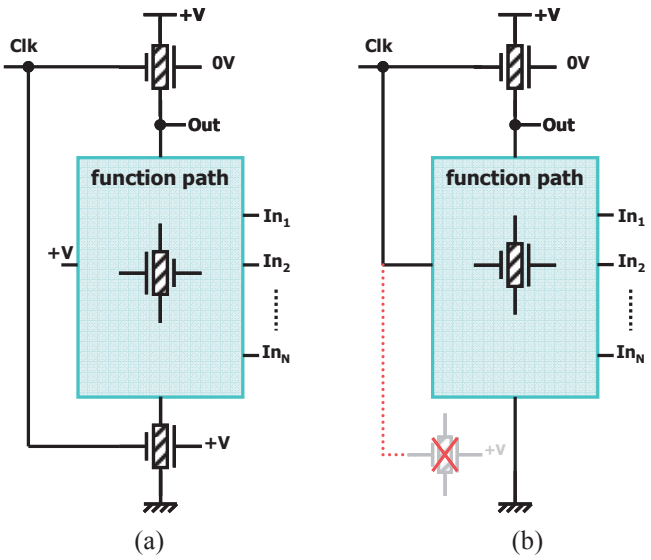


Figure 2-10. CDL structure (a), S2-DGDL structure (b)

Again, if we consider *n* to be the fan-in, the required number of transistors in this scenario will be *n+1* rather than *n+2* required in the conventional dynamic logic style structures (i.e. a gain of one transistor).

- ***Scenario 3 (S3): TTSM approach within the function path and merged with the evaluation transistor***

In the third scenario (S3), we aim to present some cases where both scenarios 1 and 2 can be merged together to further decrease the transistor count in dynamic logic cells (Fig. 2-11).

This scenario handles the particular following case; when the number of transistors N_T in each series branch of the function path connecting the ground to the output node is an odd number greater or equal to three ($N_T \geq 3$). For example, in the case of figure 2-11(a), the function path is composed of one branch of 3 transistors in series, combined in parallel with a branch using 5 transistors in series. By applying the TTSM approach inside the function path as in scenario 1, three NTTS structures were identified in figure 2-11(a) and transformed to a single Am-IDGFET each, as shown in figure 2-11(b). Furthermore, we exploited the back gates of the remaining transistors (T_1 and T_2) to merge the evaluation transistor and consequently further reduce the number of devices utilized by the whole structure as in scenario 2.

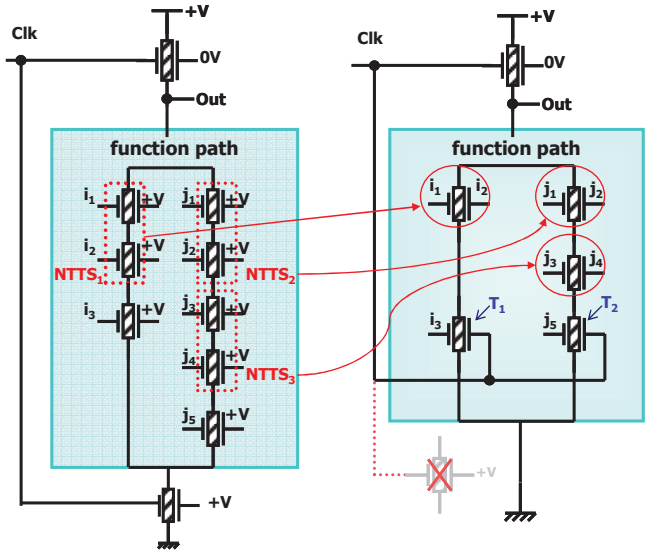


Figure 2-11. CDL structure (a), Scenario3-DGDL structure (b)

If we consider that *n* is the number of inputs of the function and *m* is the number of TTS structures that can replace two AND-related inputs in the function path, the required number of transistors will be *n+1-m* rather than *n+2* normally required by conventional dynamic logic design.

c. *Example of gates for each scenario*

- ***Examples of logic cells with scenario1-DGDL structure***

The cell structure of a 2-input S1-DGDL NAND gate is given in figure 2-12(a). The cell operation is based on 3 Am-IDGFETs. The function path is a single transistor with the front gate connected to the first input A and the polarity gate connected to the second input B.

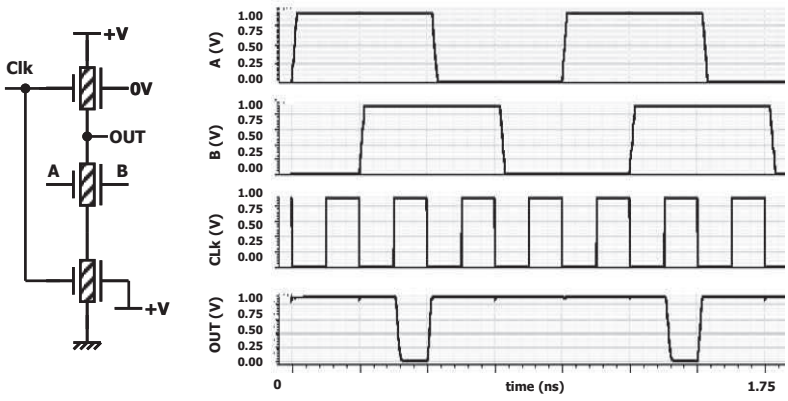


Figure 2-12. S1-NAND gate: Schematic (a) associated waveform (b)

To further illustrate the principle of the DGDL gates according to S1, some example structures of elementary logic functions are shown in figure 2-13.

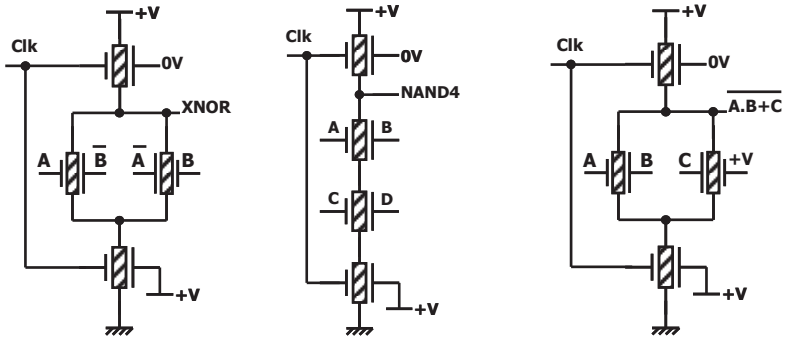


Figure 2-13. S1-XNOR gate (a), S1-NAND4 gate (b) S1-AOI gate (c)

- ***Examples of logic cells with S2-DGDL structure***

The simplest gate designed according to scenario 2-DGDL is that of an inverter where the function path is composed of a single transistor. The cell structure is given in figure 2-14(a). Two phases are clearly identifiable and demonstrate the dynamic-logic style behaviour of the cell:

- Precharge: Clk=0. The P-type transistor is ON and the output node is charged to +V. The bottom transistor is OFF.
- Evaluation: Clk=+V. The P-type transistor is OFF, and the bottom transistor is in the N-state, allowing evaluation. It is only in this configuration that the input signal has an influence on the output. If In=0, then the transistor is OFF and the output node is unchanged (i.e. it remains charged at +V established during the precharge phase). If In=1, then the transistor is ON and the output node is discharged to 0. The value of In must be stable slightly *before* the rising edge of the Clk signal, and also during the whole time that Clk is at 1. Failing this, the resulting value of the output voltage may be erroneous.

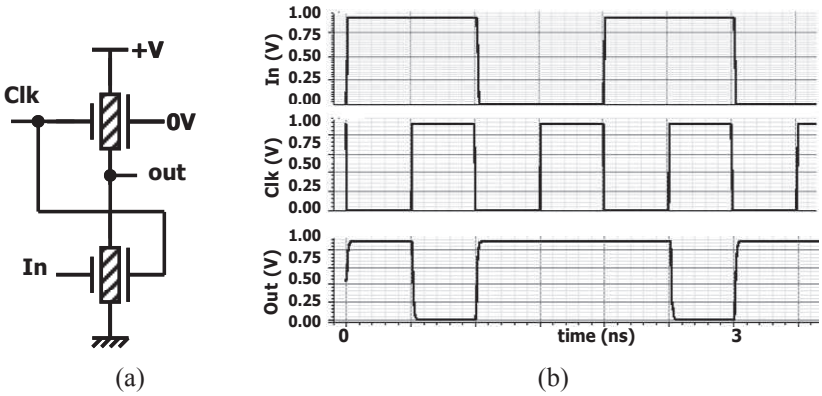


Figure 2-14. Inverter schematic (a) associated waveform (b)

To further illustrate the principle of the DGDL gates according to scenario 2, some example structures of elementary logic functions are shown in figure 2-15.

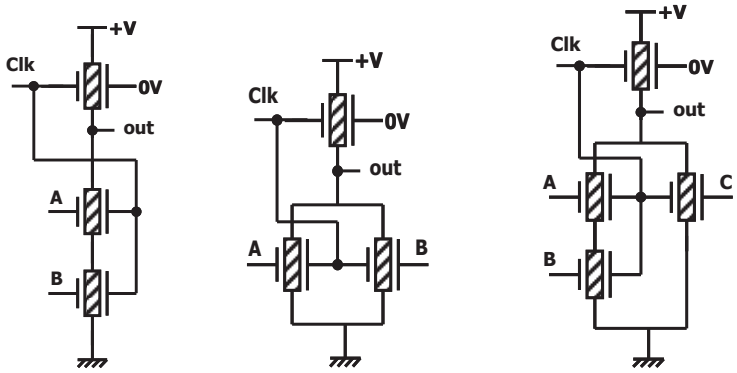


Figure 2-15. S2-NAND2 gate (a), S2-NOR2 gate (b) S2-AOI gate (c)

- ***Examples of standard logic cells with S3-DGDL structure***

In the case of dynamic *n*-input NAND gates, where *n* is an odd number and ≥ 3, the concept of Scenario3 is efficiently used. For example in the case of NAND3 as shown in figure 2-16: Out= ¬(Clk ∧ A ∧ B ∧ C).

During evaluation, if any of the inputs (A, B, C) are equal to 0, then at least one transistor of the function path is off and the output node is unchanged (i.e. it remains charged at +V, as established during the precharge phase). The only condition where both transistors of the function path are on is (A=1, B=1, C=1), and the output node is discharged to 0.

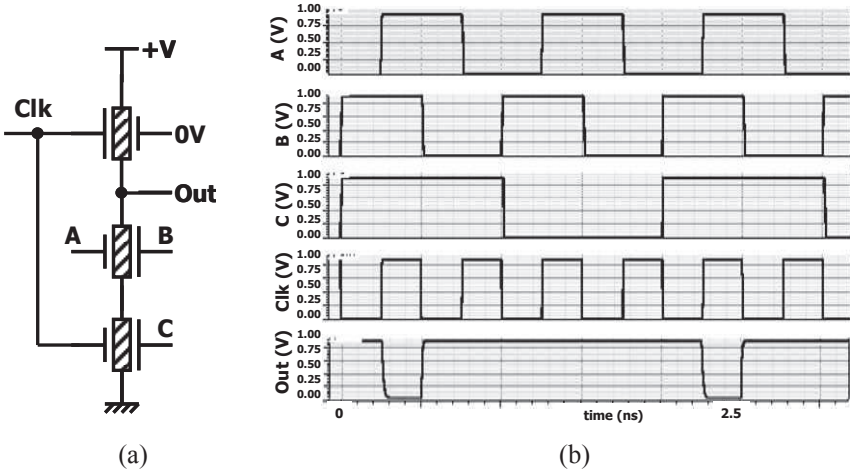
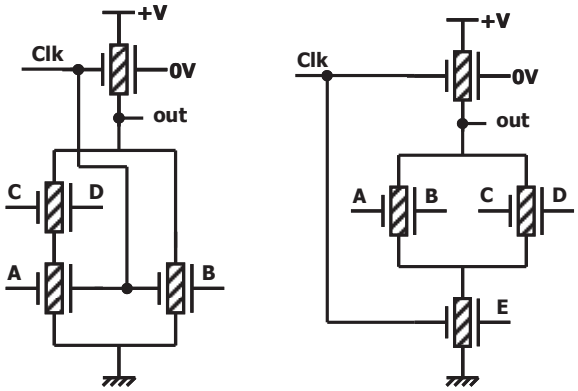


Figure 2-16. S3-NAND3 gate (a), associated waveform (b)

To further illustrate the principle of the DGDL gates according to scenario 3, some example structures of complex logic functions are shown in figure 2-17.



(a) (b)

Figure 2-17. ¬((A∧C∧D)∨B) gate (a), ¬(((A∧B)∨(C∧D))∧E) gate (b)

d. ***Comparison of scenarios***

Unlike in complementary static logic, the application of the TTSM approach to the dynamic logic structure reveals 3 different scenarios, leading to different gains in terms of transistor count, as summarized in Table 2-1.

- N: function path fan-in

- m: number of NTTS structures in the function path

TABLE 2-1. TRANSISTOR COUNT GAIN OF THE 3 SCENARIOS AS COMPARED WITH CDL STRUCTURE

Logic structure	Transistor count	Gain
Conventional dynamic logic (CDL)	N+2	0
Scenario 1 (S1)	N+2-m	m
Scenario 2 (S2)	N+1	1
Scenario 3 (S3)	N+1-m	m+1

The lowest gain is achieved by S2 with a single transistor. In this scenario, the clock signal drives the back-gate of several transistors in the dynamic structure, which dramatically increases the clock load capacitance and results in a slower circuit. This also leads to other issues arising from the complex routing of clocks.

Furthermore, electrical simulations and accurate explanations (detailed in chapter 4) show higher power consumption and time delay in S2 as compared to other scenarios. Nevertheless, S2 is still useful with a single gate function path (NOR, INV) – these are specific cases for which the other scenarios cannot be applied due to the absence of TTS structures in the function path.

Scenario S1 offers a gain of *m* transistors depending on the number of TTS structures in the function path. Scenario S3 results in the best gain (*m+1* transistors). However, it can only be deployed in specific cases (function path branches with an odd number of transistors $N_T \geq 3$). For example, S3 presents the best transistor count gain in the case of the NAND3 gate over other scenarios (only 3 transistors are used instead of 5).

The following pseudo-code describes how to choose between the three scenarios when building logic gates from the TTSM approach to achieve the best benefit.

N_T = number of transistors in one branch of the function path ($N_T > 0$)

B = number of branches within the function path

```
For branch = 1 to branch = B
 If (NT<2) then use S2 ) /* S2 is used with single gate function path */
  Else
   If (NT = odd number) then use S3
    Else (use S1)
   End if
  End if
End for
```

In this section of the work, we described different methodologies to exploit the fourth gate of Am-IDGFETs to reduce transistor count and achieve more compact standard logic structures. The evaluation of its impact on performance metrics (power, delay, area) are investigated in details in chapter 4.

Finally, we point out that the use of the back-gate in a dynamic logic style can go further than providing compact structures. The next section of this chapter deals with *dynamic* techniques to decrease the power consumption in digital circuits. Once again, the back-gate of Am-IDGFETs is utilized to offer new design opportunities. It is used to define a low- power design technique to solve some general issues of high power consumption in logic circuits.

2.3 Dynamic low-power design technique with Ambipolar Independent double gate devices

The main goal of adding a second gate to ambipolar devices is to allow their behaviour to be set to N-type, P-type or OFF-state by applying an external voltage. The applied back-gate voltage can be tied to a specific voltage value in order to obtain the same functionality as classical CMOS logic. However, as we demonstrated in the first part of the chapter,

considering the back-gate signal as a *free variable* offers an efficient approach to reduce transistor count. In more general terms, the back-gate signal is a powerful vector to control in a transistor state in a more detailed way. This can also be used to suppress transitional states in logic gates, in particular to reduce power consumption.

In this section of the chapter, we propose a circuit design technique to reduce power consumption issues in logic circuits. By using the in-field controllability via the fourth terminal of Am-IDGFETs, we show a method to control dynamically the state of switches within a circuit structure to optimize different components and phenomena responsible for power consumption. We first start by reviewing the most used low-power design techniques to highlight the innovation of the work.

2.3.1 Overview of low-power design techniques

The dramatic scaling of CMOS technology has led to a large increase in energy consumption for both active and inactive states of digital circuits. At the same time, the growing demand of ultra-low power consumption and long-standing battery lifetime, related to portable electronics, has motivated designers to come up with power optimization techniques.

This optimization includes the choice of technology and computer aided design (CAD) techniques for device sizing and interconnect [2-40, 2-41], circuit style and topology [2-42, 2-43], architecture and algorithms for implementing the circuits. Although supply and threshold voltages scaling have proved to be an efficient means to lower dynamic power [2-44, 2-45], it has also led to a significant growth in leakage power (static power) due to higher sub-threshold leakage currents. To manage the increasing leakage in ultra-deep-submicrometer CMOS circuits, solutions for leakage reduction have to be sought both at the process technology and circuit levels. At the process technology level, well-engineering techniques by retrograde and halo doping are used to reduce leakage and improve short-channel characteristics. At the circuit level, transistor stacking, multiple, variable, and dynamic techniques can effectively reduce the leakage current in high-performance logic and memory designs.

In [2-46, 2-47], several design techniques to solve this issue were described and improved by combining two techniques together. In general, four main approaches can be identified to reduce the sub-threshold current in standby mode: Self-Reverse Bias (SRB) [2-48], Multi Threshold (MT) [2-49] – a modified version of the SRB technique, Super Cut-off CMOS (SCCMOS) [2-50] – proposed to solve the problem of the extra cost of the MT approach, and Variable Threshold (VT) [2-51].

In the context of ultra-low power systems with Double-Gate FETs (DGFETs), the investigation of various configurations (connected or independent gates) of DGFETs has demonstrated a promising future compared to bulk CMOS in [2-52]. However, instead of exploiting the fourth terminal of the DGFET to improve the performance metrics of logic gates

dynamically, this approach makes direct replacements of bulk CMOS devices with DGFETs at the circuit level. In [2-53] [2-54], the authors modulate the back-gate bias in DGFETs to vary dynamically the threshold voltage V_{TH} and consequently decrease the leakage power. Reduction factors of 10^3 as well as a factor of 10^4 were demonstrated, respectively, in [2-53] and [2-55] with thin-body (TB), fully depleted (FD) double-gate (DG) silicon-on-insulator (SOI) devices.

To the best of our knowledge, no design technique was suggested to *dynamically* optimize the short-circuit power during the switching time. In this chapter, we explore the new capabilities of Am-IDGFETs to describe a new design technique which lowers the dynamic power during input switching time thanks to the OFF state enhanced by such a device. Furthermore, the new design technique is extended to reduce the static power during the standby mode of circuits.

2.3.2 Low-Power design technique with ambipolar DGFETs

Total power consumption Power P_{tot} is the sum of three components: static power P_{stat}, dynamic active power P_{dyn} and dynamic short-circuit power P_{sc}. To lower the dynamic power, the usual techniques are based on scaling the supply voltage, decreasing the capacitance by reducing output drain capacitance, interconnect wire-length and input gate capacitance, as well as reducing the frequency and the switching activity factor. In this work, we propose an additional technique enabled by the 4-terminal structure of Am-IDGFETs, by using the Back-Gate to reduce *dynamically* the short-circuit power during *input transition time*. Furthermore, the technique includes the static power lowering, again through the use of the back-gate. While the idea of using the back-gate of DGFETs to dynamically decrease leakage power through threshold voltage modulation has inspired some designers [2-53, 2-54, 2-55], it should be noted that in the case of Am-IDGFETs, the additional electrode (BG) offers an additional degree of freedom since it controls the electrostatic doping of the source and drain access regions. Moreover, this property enhances OFF-state performance and provides an abrupt switching behaviour that is close to theoretical limits.

2.3.2.1 Dynamic power lowering

For static logic CMOS gates, it has been shown in [2-56] that the short-circuit current can consume up to almost 15% of the total chip power. This component of the total power consumption is generally decreased by using techniques to balance the transition time (rise and fall) at the input with that at the output in a logic circuit. For instance, in [2-57] the author discussed the use of on-chip inductance to improve the signal slew rate, thereby reducing the short-circuit power consumption. In our proposed technique, we aim to deactivate all transistors in the circuit during this time to abolish/limit the short-circuit current, such that the signal slew rate is irrelevant. This also diminishes the capacitive power since the output node is charged or discharged during the input transition time.

a. *Technique description*

During switching between steady-state zones of operation, a direct current path between the supply V_{dd} and ground exists for a short period of time, directly related to rise and fall times of the input signal. Both the NMOS and PMOS devices will be simultaneously ON when $V_{THn} < Vin < V_{dd} - |V_{THp}|$, as shown in figure 2-18(a), where we suppose that $V_{THn}=|V_{THp}|=V_{TH}$, $V_{dd}=+V$ and I_{MAX} is the saturation current of the P and N transistors which depends on their sizes, process technology, temperature, etc.

The main idea at this level of work is to force both NMOS and PMOS devices into the OFF state during changes on the input signal to eliminate/optimize the short-circuit current as shown in figure 2-18(c). Once input signals have reached steady-state values, the devices are turned on again and enable switching at the output node.

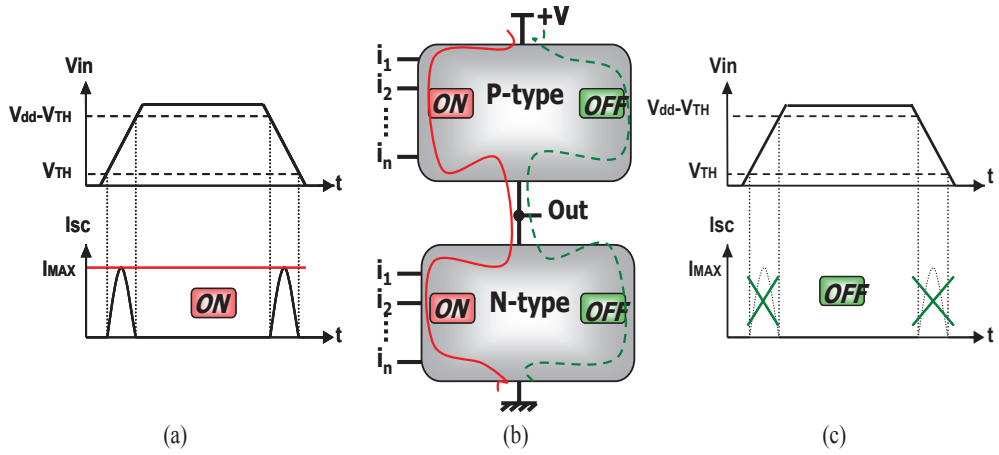


Figure 2-18. Short-circuit current when both P/N devices are ON (a), Complementary static logic structure (b) Elimination of short-circuit when both P/N devices are OFF (c)

A generic example in figure 19 illustrates the use of transistor back gates to control the state of devices such that while input signals are at steady-state values ("High" and "Low" states) the pull-up and pull-down network transistors are configured to P- and N-type respectively and the circuit operates in the conventional way; and during input signal switching (transition from 1→0 and from 0→1), the transistors are switched off via the back gate to eliminate the short-circuit current.

In the circuit, the front gates FG of transistors are connected to data inputs, while the back gates are used to control the state of transistors. In practice, this means that two clock signals are used:

- Clk_P is connected to the BG of the pull-up network transistors (BGP). When VBGP= +V/2, all pull-up network transistors are OFF (during input transitions), and when VBGP= 0V, all pull-up network transistors are set to P type (during input steady states).

- Clk_N is connected to the BG of the pull-down transistors (BGN). When VBGN= +V/2, all pull-down network transistors are OFF (during input transitions), and when VBGN= +V, all pull-down transistors are set to N type (during input steady states).

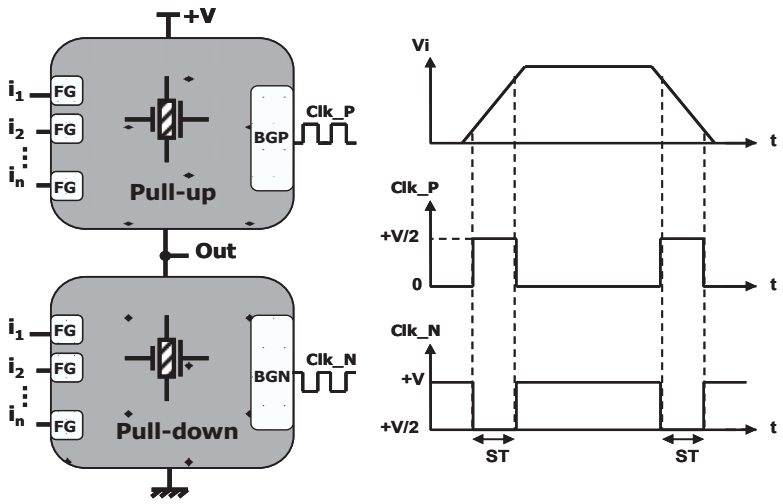


Figure 2-19. Structure of low short- circuit power gates

The pulse width of clocks depends on the rise/fall time of input signals. In figure 2-19, we choose a value "ST" (switching time) which is exactly equal to the time during which both transistors (N type and P type are ON) to demonstrate the concept. In fact the pulse width is constrained to lie between ST and T-dt (T period of data, dt output switching time).

b. ***Inverter example***

We applied the approach in the case of an inverter gate with simulations conditions detailed in the validation section. In order to show only the short-circuit current; no capacitive load is cascaded at the output (no capacitive dynamic power). The conventional logic structure of an inverter (Cnv-inverter) is shown in figure 2-20(a) and the new clocked structure design (Clk-inverter) is shown in figure 2-20(b). Figure 2-20(c) shows that peaks of current I_C corresponding to conventional design are diminished when using the new technique (I_{CLK} current) but small peaks of current (I_{CLK}) still remain due to the rise/fall time of the clocks (Clk_P and Clk_N). The short-circuit power was estimated to decrease up to 6X with the Clk-inverter. More gates are simulated in chapter 4 of this dissertation to highlight more clearly the effect of the back-gate clocking approach in several logic gates. It should be noted that since the small peaks of currents appearing in figure 2-20(c) with the Clk-inverter depends on the transition time of the clock, so the faster the clock transition time (rise and fall) is, the better the optimization of short-circuit power.

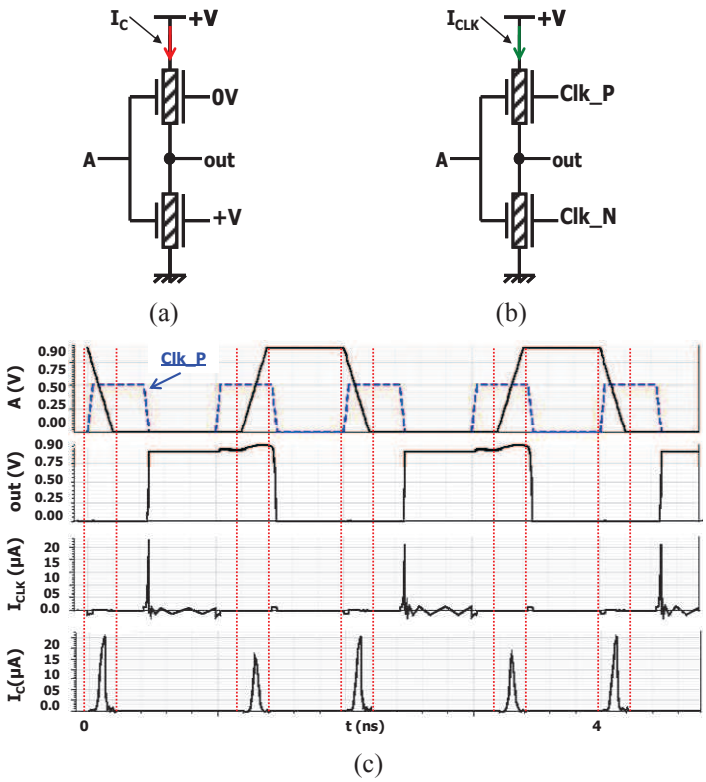


Figure 2-20. Inverter gate: Conventional schematic (a) Backgate-Clocked design schematic (b) Simulated waveforms (c)

2.3.2.2 Static power lowering

We mentioned in the introduction (chapter 1), that the back-gate controls the device polarity setting to N- or P-type with a positive (V_{BG}-V_S= +V) or negative (V_{BG}-V_S= -V) voltage respectively. In figure 2-20 (a), we applied those rules for the design of a conventional inverter structure. During the standby mode of the gate, we aim to have a value of the I_{OFF} as low as possible for both transistors networks (pull-up and pull-down). That's why, in a similar way to variable threshold low-power circuit techniques, we aim to use a high back-gate voltage value BGN for N-type transistors and a low back-gate voltage value BGP for P-type transistors during the active mode to ensure a *high* I_{ON}, and *vice-versa* during the *standby* mode to ensure a *low* I_{OFF} and consequent static power. Table 2-2 shows the values of back-gate voltages during the two phases of circuit operation (active mode / standby mode). Here the values are chosen to be the same values as V_{dd} and ground (both because of availability of these voltages and because of the optimality of their impact).

TABLE 2-2. TRANSISTOR BACK-GATE VOLTAGES DURING BOTH CIRCUIT MODES

	Active	Standby
V_{BGN}	+V= 0.9 V	0 V
V_{BGP}	0 V	+V=0.9 V

In figure 2-20, DC analysis of an inverter gate shows the evolution of the current as a function of the input gate V_{IN} in both configurations shown in table 2-2. The standby mode

corresponds to the current conducting the gate when V_{IN}= 0V or V_{IN}= 0.9V (steady-states). At those two points, figure 2-21 shows clearly a factor of 100X decrease in I_{OFF} with the standby mode configuration. When it comes to transient analysis of the same inverter, this is confirmed by transient simulations results where an improvement by more than 100X of the static power has been observed by inverting back-gates voltages. The same simulations conditions detailed in chapter 4 of this dissertation have been used and more logic gates are simulated.

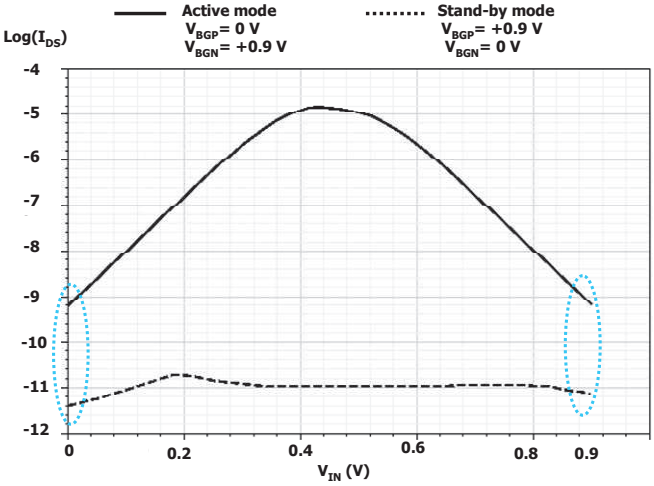


Figure 2-21. I_C/V_{IN} of an inverter gate in both configurattions (active and standby)

2.3.2.3 Proposed module for total power decreasing

In order to incorporate both Am-IDGFET low-power techniques, it is necessary to control the action on the back-gate voltages to decrease the short-circuit power dynamically in the active mode, and to decrease the static power during the standby mode. Figure 2-22 presents a complete circuit structure which enables the implementation of both low power design techniques using a control module to configure dynamically the circuit block via transistor back-gates by means of a simple unit which switches between the two modes (active /standby).

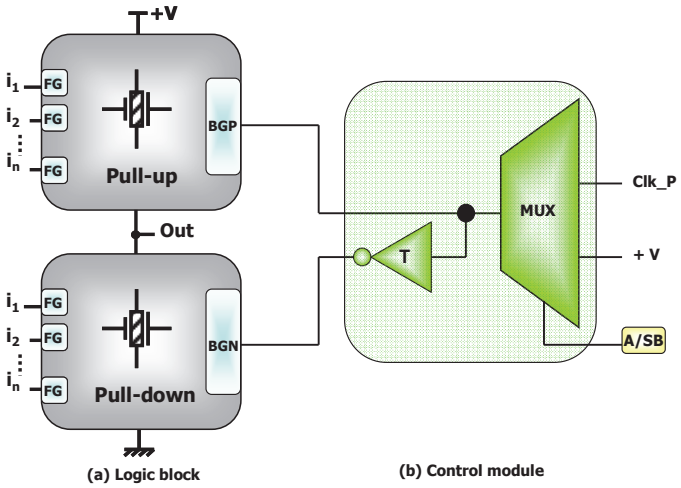


Figure 2-22. Low-power circuit dynamic structure

The output of the MUX is connected to Pull-up transistors (BGP) and to a ternary inverter (T-inverter). The T-inverter supplies the Pull-down transistors (BGN) and operates according to {+V→0V, +V/2→+V/2, 0V→+V}.

The structure of the T-inverter used within the module is presented in figure 2-23; it is composed of two transistors and two equal values resistors. In chapter 4 of this dissertation, we will discuss and evaluate the power consumption of this circuit depending basically on resistors values of the T-inverter as well as its impact on the operation of the logic block circuits.

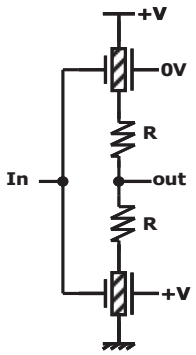


Figure 2-23. T-inverter structure

The control signal (A/SB) of the multiplexer is used to switch between the active mode and the standby mode. During the active mode, Clk_P is selected and provides the clock signal for the transistor back-gates to inhibit the short-circuit current, as explained in 2.3.2.1. During the standby mode, the input +V of the MUX is selected to lower the static power, as explained in 2.3.2.2.

The proposed design technique does not suffer from any racing, since it is a static logic (power CLKs are gating the back gate, defaults and delays of power CLK signals will simply generate a delay in the signal rising and falling, unless this delay is greater than the actual logic CLK period).

In practice there are three additional challenges to apply this approach:

(i) The synchronization of clock signals with data transitions, for instance by using a pulse detector usually employed to design edge-triggered latches (flip-flops). Pulse detector circuits may be made from time-delay relays for ladder logic applications or from logic gates (exploiting the phenomenon of propagation delay [2-58]).

(ii) Cascading gates means that the input of one gate is the output of another, which will lead to a need for phase-shifted clocks [2-59].

(iii) The clock waveforms must be particularly sharp –careful design of the clock distribution network helps ensure that critical timing requirements are satisfied.

2.3.2.4 Achievements

The back-gate of Am-IDGFETs is used to control dynamically the behaviour of devices in logic circuits. In this approach, transistors are switched OFF during input transitions to limit the short-circuit current and significantly decrease the dynamic power. The back-gate voltage of transistors is also changed during the standby mode to decrease the I_{OFF} current and consequently limit the leakage power. To switch between both circuit modes (active / standby) a control module was proposed.

2.4 Conclusions

Based on Am-IDGFETs, we described two circuit design techniques. Both techniques exploit the fourth- terminal of the device to achieve a new concept for the design of standard logic gates. The first approach (TTSM approach) efficiently reduces the transistor count for logic cells in different logic styles, leading to a greater integration density by replacing all two transistors in series structures with a single Am-IDGFET for equivalent functionality. We have depicted the generic structure of static logic gates when using the TTSM approach and proved that the number of transistors required by conventional structures can be divided by 2 in the case of some static gates. Concerning the dynamic logic style, we showed how the TTSM approach can be applied according to three different scenarios, depending on the number of transistors and their distribution in the gate branches with an expected gain in transistor count of nearly 30%. The second design approach, presented in this chapter, deals with the issues of power consumption in two forms (short-circuit power and static power). We suggest controlling the state of transistors by switching them off during input transitions via their back-gates; in such a way as to decrease the dynamic power (short-circuit). Moreover, we showed that by inverting transistor back-gate voltages during the standby mode, the leakage current I_{OFF} is reduced by a factor of 100X. The validation of both design approaches and the evaluation of their capabilities to improve various standard cell performance metrics are investigated further in the fourth chapter of this dissertation.

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Chapter 3

Synthesis Techniques for reconfigurable logic with Ambipolar Double Gate FETs

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Abstract

Logic synthesis is one aspect of electronic design automation by which an abstract form of desired circuit behavior is turned into a design implementation in terms of logic gates. Despite of all the late and recent developments in logic synthesis, current tools are not able to cope with newly emerging designs. In the case of Am-IDGFET, conventional logic synthesis techniques cannot directly represent the property of in-field device reconfigurability with the back gate as free variable, such that new techniques must be found to build optimal logic with such devices. In this chapter, we exploit functional classification, a powerful tool for the construction and analysis of Boolean functions, to build reconfigurable logic blocks by defining a hierarchical correlation between structures of functions with ambipolar devices. We demonstrate how this correlation enables us to build ambipolar DGFET-based n-input reconfigurable cells. Several dynamically reconfigurable 2-inputs logic cells with partial and full functionality are designed in this chapter in both dynamic- and static-logic styles.

Furthermore, the key logic synthesis and verification technique of Binary Decision Diagrams has been used to describe a novel reconfigurable logic synthesis method with ambipolar devices. We propose an Ambipolar Binary Decision Diagram (Am-BDD), by adapting the conventional BDD technique to ambipolar devices. We describe how this approach offers the possibility to build DGFET-based n-input reconfigurable cells based on pass-transistor-logic obtained from Am-BDDs. We also show how specific correlations between configuration signals can lead to a minimization of their total number. Using the Am-BDD technique, we designed a reconfigurable 2-input cell library based on pass-transistor logic with full and partial functionality.

3.1 Introduction

Reconfigurable architectures such as FPGAs are of great interest to system designers because they allow fast and flexible hardware design as well as opportunity for reuse in digital circuits. Short design cycles make FPGAs ideal for prototyping designs prior to full-fledged production. However, with this ease of uses comes a significant penalty in terms of area, speed and power, as circuits implemented in FPGAs are at least ten times larger, three times slower and three times higher in total power consumption than custom implementations. This is mainly due to the large amounts of programmable interconnections and the auxiliary circuits which 'program' the generic blocks to become a well-defined piece of logic. To minimize these factors, designing the FPGA itself to be high-speed and low-area is essential. For this reason, alternative manufacturing techniques and emerging devices may enable the optimization of reconfigurable architecture performance and density. With emerging technology devices, and in particular four-terminal devices, the overheads imposed by reconfigurability can be reduced or hidden to an extent where it becomes possible to support complex datapath architectures with homogeneous fine-grained organization [3-1, 3-2]. In order to fully exploit these new devices and integrate their innovative capabilities in the design flow, novel design tools are required to automate logic synthesis.

Conventional logic synthesis flow contains three main separate phases: technology independent optimization, technology mapping, and technology dependent optimization. To deal with design flow steps and automating the design, logic synthesis tools are utilized. They consist of a number of various programs and algorithms for synthesis and optimization of logic circuits, typically based on algebraic decomposition techniques, graphs (Boolean networks, BDDs…) and so forth.

For conventional technologies with unipolar transistors, *Binary Decision Diagrams (BDDs)* [3-3, 3-4], direct acyclic graph representations of Boolean functions, are a key technique in EDA and the cornerstone of automatic pass transistor logic (PTL) synthesis flows [3-5, 3-6, 3-7]. In addition to BDDs, there is also an interesting tool for the design of digital circuits known as *function classification* which involves a deep understanding of the concept of Boolean functions. For the digital circuit synthesis process, function classification is very useful for the matching phase performed during technology mapping [3-8].

However, existing versions of these methods are limited to conventional (unipolar) transistors and cannot exploit new design opportunities provided by Am-IDGFET devices. Although many reconfigurable cells and architectures have been proposed for such devices, no systematic methodology or synthesis techniques for Am-IDGFET-based reconfigurable cells exist. This is mainly due to the low level of maturity of this type of FET. Nevertheless, their capability to operate as either N-type or P-type switches according to the back gate bias

voltage opens the way to a new paradigm of reconfigurable logic and requires reconfigurable logic synthesis approaches to fully explore the potential of this approach.

In this chapter, both function classification methods and BDDs are adapted to define systematic synthesis techniques to built reconfigurable cells with Am-IDGFETs.

- The first technique is a direct adaptation of the *function classification* tool, since it matches every class of functions to its corresponding circuit. Given the in-field reconfigurability of each DGFET, any logic circuit based on this device is inherently reconfigurable. Furthermore, specific correlations can be observed between different circuit's structures represinting classes of functions. This offers the possibility to build cells with more functionality. A case study of 2-input functions is presented in this chapter, defining correlations between classes and leading to the design of partial/complete-functionality reconfigurable cells.
- The second technique proposes an Ambipolar Binary Decision Diagram (*Am-BDD*), to adapt the conventional BDD logic synthesis and verification technique to ambipolar devices. Starting from basic rules of generating BDDs, we defined some new rules and steps related to the fourth terminal of Am-IDGFETs to shape a novel AmBDD that enables us to build n-input reconfigurable cells based on pass-transistor-logic.

3.2 Function classification approach for Ambipolar DGFET-based reconfigurable logic

In this part of the dissertation, we explore the concept of function classification in the context of reconfigurability using ambipolar DGFETs. Once a classification technique is defined, two main issues must be tackled: (i) defining the transistor-level implementations of all function classes, (ii) finding correlations between class structures and states of the switch taking into account the additional terminal.

Based on these objectives, a novel approach to build reconfigurable cells is proposed, to apply function classes to logic built with such devices. We demonstrate how this method enables us to build Am-IDGFET-based n-input reconfigurable cells based on the dynamic-logic style, and then extend them to build static-logic cells. With the function class approach, dynamically reconfigurable cells with partial or complete functionality (tuned according to the requirements of the designer), can be designed methodically. To authenticate the approach, a library of reconfigurable cells with partial/complete functionality was built.

Before describing the function class-based design methodology, we begin by presenting the concept of function classification.

3.2.1 Function classification

3.2.1.1 Concept

Functions classification finds significant applications as a powerful tool for the field of cryptography [3-9, 3-10, 3-11]. Recently, in [3-12] authors exploited the Boolean function classification concept to build an approach for the classification of remote sensing images. With straightforward construction and analysis of functions, the notion of Boolean function classification shows great potential for application in many advanced fields.

When considering Boolean switching functions with n input variables, there are 2^{2^n} possible functions, each of which can be realized by enumerating all possible combinations of input values and arrangements of output values. As is expected with double exponential complexity, the number of functions becomes unmanageable very quickly even for relatively small values of n. Using classification, all 2^{2^n} functions can be considered through a small number of representative functions. In other words, there are approaches to group functions according to some specific property [3-13, 3-14, 3-15, 3-16, 3-17]. Then, if one considers a representative function of a given class as a generic black box circuit, it could be used as a building block for all functions within that class [3-18]. For the digital circuit synthesis process, function classification is very useful for the matching phase performed during technology mapping [3-8], where a function (or only part of it) to be implemented is matched against cells from a library. Sometimes this matching is limited to cells with a maximum number of inputs. Hence, we classify n-input functions in order to have a precise idea about the search space of the whole set of n-input functions [3-18].

Hurst et al [3-17] list two advantages of classification:

1. Increased understanding of functions that have essentially identical circuit realisations, leading to the classification of all functions of ≤n variables in some compact manner.

2. Possibility of establishing a small set of "standard functions" or "prototype functions," from which any particular function may be realised by implementation of appropriate operations corresponding to the classification procedure.

Once a classification technique is determined, if one considers a representative function of a given class as a generic black box circuit, it could be used as a building block for all functions within that class.

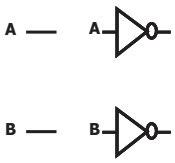
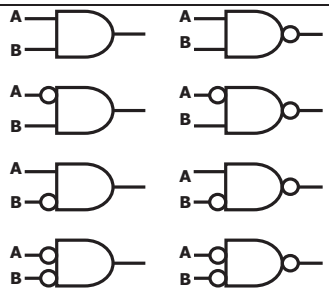
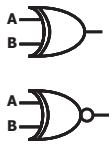
There have been numerous approaches to grouping functions according to some specific property: threshold classification [3-13], unit classification [3-14], spectral classification [3-15, 3-16] and algebraic classification [3-17]. For more details concerning the classification of Boolean functions, in [3-18] the author surveyed all classification techniques with theoretical analysis and examples; he also developed a new approach for computing spectral classes.

In our study, we will use the algebraic classification scheme, since it is the most common and straightforward approach utilized in the literature. It is based on NPN: Negation of input variables (N), Permutation of input variables (P) and Negation of output (N). However, it is worth mentioning that any other classification approach could also be considered to define Boolean function classes since the result is expected to be the same (the same number of classes and functions constituting the class).

3.2.1.2 NPN classification for 2-input functions

For a given number *n* of input variables, there are 2^{2^n} possible functions. Here we use 2-inputs, so there are16 achievable different functions. NPN equivalence between 2 functions is obtained when it is possible to achieve identical values for both truth table outputs by permutation and/or negation of the function inputs and/or negation of the function output. Table 3-1 shows all 4 different NPN classes of 2-input functions, one NPN class per column. It is important to note that despite the existence of 16 different 2-input functions, there are only 4 different 2-input NPN classes shown in table 3-1. NPN equivalent functions can be implemented with the same circuit plus some inverters (used in the negation operations for the inputs and the output, if necessary). This way, it is possible to use a smaller library composed of one representative gate for each NPN class plus some inverters. This approach is especially useful when the cost of the inverter is very low [3-19].

TABLE 3-1. 2-INPUT FUNCTION NPN CLASSES

Class1	Class2	Class3	Class4
			

3.2.2 Class-based design approach to build reconfigurable logic

From table 3-1, it is clear that NPN equivalent functions can be implemented with the same circuit plus some inverters. We aim to propose, for each class of function, the corresponding logic structure of the function path block. However, every Boolean function can be written in canonical form as a sum of products *(SOP)*, i.e. minterms or as a product of sums *(POS)*, i.e. maxterms; consequently, the structure of the function path will depend on the choice of canonical form. In our case, both forms will be used to build reconfigurable logic cells.

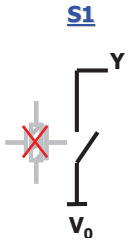
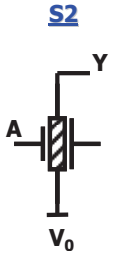
3.2.2.1 Corresponding function path structures for every class

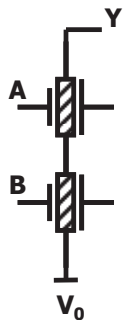
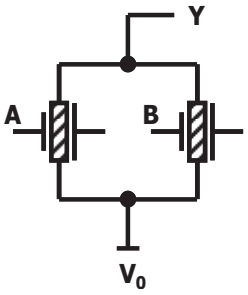
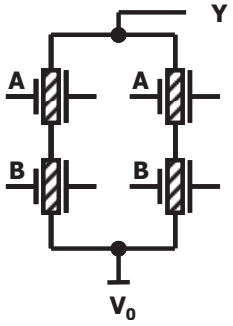
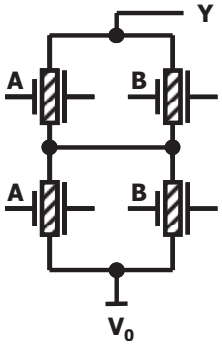
Each of the three operations (negation of inputs / permutation of inputs / negation of output) has its equivalent realization at the transistor level thanks to the three switch states (p-type, n-type, and off-state) offered by Am-IDGFETs:

- negation of inputs: the function path transistor front gate inputs are not in fact complemented (which would require an extra inverter). Rather, Am-IDGFETs are configured to P-type using the corresponding voltage on their back-gate (i.e. -V). This results in the same effect as negated inputs.
- permutation of inputs: the off-state of Am-IDGFETs can be used to fulfill this operation by switching off the transistor connected to one input.
- negation of the output: this can be realized at circuit level by simply placing an inverter/follower structure at the output Y of the function path. Depending on the configuration of the inverter/follower stage, the output of the function path is propagated or negated.

The table below (table 3-2), describes the function path of every class of functions. The structures are generic, which is why the back-gate voltage is not presented (this is used during the negation of inputs step). Similarly, the inverter/follower at the output of the function path is not presented (since this is added during the negation of outputs step). The next step of the work is to determine the correlation between different class structures.

TABLE 3-2. 2-INPUT FUNCTION NPN CLASSES AND CORRESPONDING GENERIC STRUCTURE

<table>
<tr><th>Class</th><th>NPN classification</th><th colspan="2">Circuit structure</th></tr>
<tr><td>1</td><td>T
$\perp$</td><td colspan="2"> 
</td></tr>
<tr><td>2</td><td>A
B
$\overline{A}$
$\overline{B}$</td><td colspan="2"> 
</td></tr>
<tr><td rowspan="2"></td><td rowspan="2">$\overline{A.B}$</td><td>Minterm-based</td><td>Maxterm-based</td></tr>
<tr><td></td><td></td></tr>
</table>

3	$A.B$ $A.\overline{B}$ $B.\overline{A}$ $\overline{A+B}$ $A+B$ $\overline{A}+B$ $A+\overline{B}$	S3′ 	S3 
4	$A \oplus B$ $\overline{A \oplus B}$	S4′ 	S4 

3.2.2.2 Bottom-up hierarchical correlations between classes' structures

From results of the NPN classes and their corresponding structures in table II, we clearly observe that each class has its own function path structure. However, hierarchical correlations may be identified from the bottom up.

a. ***Hierarchical correlations between Minterm-based structures (S3', S4')***

S4' coverage: Starting from the bottom of table 3-2 and using minterm-based structures, we can consider that the structure S4' contains duplicates of the structure S3'. This means that all functions of class 3 can be implemented with the structure S4' of class 4. Also, S4' is a sum of two minterms, which means that functions of class 2 can be implemented with the structure S4' of class 4, since for example A = (¬B∧A) V (A∧B). Finally, when all transistors of the structure S4' are configured to the Off-state, the functions of class 1 are implemented.

Thus, we can write: S3' ⊂ S4', S2 ⊂ S4' and S1 ⊂ S4', which means that the circuit in the table with the structure S4' can map the whole set of the 16 functions.

S3' coverage: By starting from the structure S3' of class 3, we cannot achieve the functions of class 2 since the structure S3' is composed of a single minterm. However, when all transistors of the S3' structure are in the off-state, the functions of class 1 are mapped.

Thus, we can write: S2 $\not\subset$ S3' and S1 $\subset$ S3', meaning that the structure S3' can map 10 functions (functions of class 3 and class 1).

S2 coverage: Finally, the structure S2 can map only 2 functions of the class 2 since it is composed of only one transistor (which means only one input A or B). S1$\subset$S2, since all transistors of the S2 structure can be switched OFF to achieve the class 1 functions, which means that structure S2 can map 4 functions (functions of class 1 and 2 functions of class 2)

b. *Hierarchical correlations between Maxterm-based structures (S3, S4)*

S4 coverage: Starting from the bottom of the table 3-2 and using maxterm-based structures, we can consider that structure S4 contains duplicates of structure S3. This means that all functions of class 3 can be implemented with structure S4. Also, S4 can map all functions of class 2, since we can switch OFF transistors connected to the unused input and operate those connected to the used input (e.g. switch OFF transistors with input B on their front gate and operate the others to achieve the A function). Finally, when all transistors of structure S4 are configured to the OFF-state, the functions of class 1 are implemented.

Thus, we can write: S3 $\subset$ S4, S2 $\subset$ S4 and S1 $\subset$ S4, meaning that structure S4 can map the whole set of 16 functions.

S3 coverage: Unlike minterm-based structures, the structure S3 can achieve the functions of class 2 simply by switching OFF one transistor. Also, when all transistors of the S' structure are in the off-state, functions of class 1 are mapped. Thus, we can write: S2 $\subset$ S3 and S1 $\subset$ S3, which means that the structure S3 can map 14 functions (the whole set of functions except those of class 4, XOR/XNOR).

S2 coverage: As previously established, structure S2 can map 4 functions (functions of class 1 and 2 functions of class 2).

c. *Hierarchical correlations between Maxterm- and Minterm-based structures*

Maxterm-based structures demonstrate a greater flexibility to encapsulate the functions of a higher class by a structure of a lower class (higher and lower is defined according to the position how they are presented in the table 3-1). Indeed, maxterm-based structure S3 can map upper classes (class 2 and class 1) with a total of 14 achievable functions, while minterm-based structure S3' cannot map the functions of class 2 and achieves only 10 functions.

Using the maxterm-based structure, we can go further to build more compact reconfigurable cells utilizing a single stage (that of the function path) *without* the need to cascade an inverter/follower stage. A set of 15 functions can be mapped (except for the "true" - unconditional "1" - function).

In fact, S4 can achieve both functions of class 3 since it is a product of two maxterms and every transistor is reconfigurable. Hence, *maxterm-functions* of class 3 (A∨(¬B), (¬A)∨B, (¬A)∨(¬B), A∨B) are directly mapped by duplicating the same transistor configuration as used for S3. Concerning the *minterm-functions* of the same class 3 (A∧(¬B), (¬A)∧B, (¬A)∧(¬B), A∧B), we can simply switch OFF two transistors of the S4 function path, one of which must have the front gate connected to the first input (A in this case) and the other of which must have the front gate connected to the second input (B in this case). In this way, we obtain the same structure S3' as shown in figure 3-1 (dashed green line). To achieve functions of classes 2 and 1, we can switch OFF both transistors connected to an identical input, and configure the two others to n-type or p-type depending on the output function we aim to achieve. For instance, the (¬A) function can be obtained by switching off transistors which have input B on their front gate, and configuring the others to n-type. Finally, when all transistors of the structure S4 are configured to the OFF-state, the function "false" or "0" of class 1 is implemented. The only missing function is "true" (unconditional "1").

Assuming that every transistor can have one of the three states (P-type, N-type and OFF), figure 3-1 shows the presence of different class structures within the structure S4. S1 is not presented in the figure since this structure is realized simply by switching all transistors OFF.

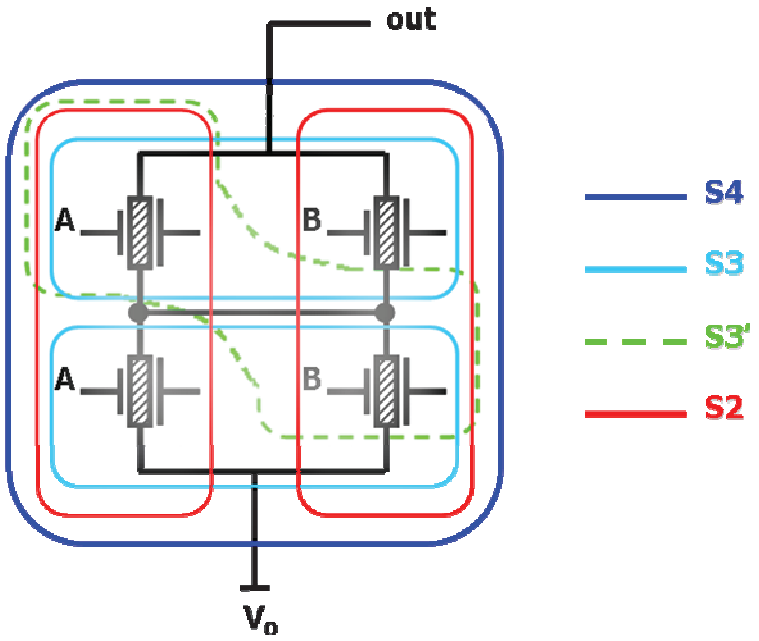


Figure 3-1. The ability of the S4 class structure to express other class structures

3.2.2.3 Summary of the function classification approach to build reconfigurable cells

In this section, we showed that by using classification, all 2^{2^n} functions (with *n* the number of inputs) can be considered through a small number of representative functions called classes. For n=2, we demonstrated 16 functions distributed over 4 classes. By matching each

class to its generic structure, we observed that bottom up hierarchical correlations exist between different classes. We presented these hierarchical correlations according to two approaches: one based on minterm structures, and the other based on maxterm structures. For each approach, three different coverage scenarios were identified, each one corresponding to a reconfigurable cell. Independently of the approach considered (minterm- or maxterm-based), we showed that the last class of functions encapsulates other classes and is able to build the whole set of 16 functions. Furthermore, in 3.2.2.2.c, we showed that a more compact reconfigurable cell *without* an inverter/follower stage at the output could be built and also fulfils the whole set of 16 functions except the “true" (unconditional "1") function.

3.2.3 Library of dynamically reconfigurable logic cells

In the previous section, we explained that from every function class a reconfigurable logic cell can be derived, and that by defining correlations between class circuits, cells with a higher number of achievable functions can be designed. In this section, we will apply this approach by describing a library of dynamically reconfigurable cells based on such structures with details about their configuration technique and clock systems. The final transistor-level implementation of dynamic logic cells is presented with a complementary static logic version. In order to base this approach on verifiable physical structures, we start this section by describing an Am-IDGFETs transmission gate that will be used for the design of all reconfigurable cells in this work.

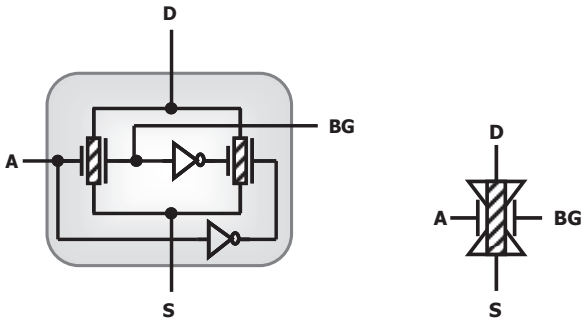
3.2.3.1 Am-IDGFETs Transmission Gate

The required elementary Am-IDGFET switching structure, and basis for the implementation of the previously described approach, is one of two types. The first, “T”, can be configured according to 2 states (P and N); we will see that this structure can be used for the follower/inverter stage of reconfigurable cells since it does not require the OFF state. The second, “TI”, can also be configured to the OFF state; this structure can be used in the function path stage, which requires the three configurations (N, P and OFF) to implement a maximum number of functions. Both structures (T and TI) are to be used as elementary switching structures in circuits designed in this chapter. Since they are requiring more area than single transistors, we choose to use them only when the use of a single transistor is not possible. Hence, all cells designed in this chapter contain single ambipolar transistors as well as T and TI transmission gates within the same circuit.

The reconfigurable cell, based on dynamic logic, essentially requires a network of transmission gates to propagate logic levels with no degradation and for a wide range of data and control voltage combinations.

Due to non-zero threshold voltages, N-type channels drain potential cannot exceed V_{DD}-V_{THn}, and P-type channel drain potentials cannot go under V_{SS}+|V_{THp}|. This causes signal

degradation when using an N-type device in the pull-up network, or when using a P-type device in the pull-down network. To avoid this effect and to ensure full voltage swing in all configurations, we replace each Am-IDGFET with a transmission gate composed of two DGFets which are controlled (at both the front- and back-gate) by complementary signals. In a transmission gate, both N- and P-type devices are in parallel to ensure that one of the two transistors passes the signal level with no degradation in all cases (Fig. 3-2).



(a) (b)

Figure 3-2. DGFET binary transmission gate: structure (a), symbol (b)

A transmission gate with signals A and BG applied respectively on the front gate and the back-gate gate of one transistor and their complements applied on the other transistor implements the XOR function by passing current ***if and only if A⊕ BG =0 (condition 1)***.

Unlike a single DGFET, the new structure of the proposed transmission gate *(abbreviated as T)* prevents any logic degradation. If we suppose that A is the input of the structure and BG is configuration signal, we can write:

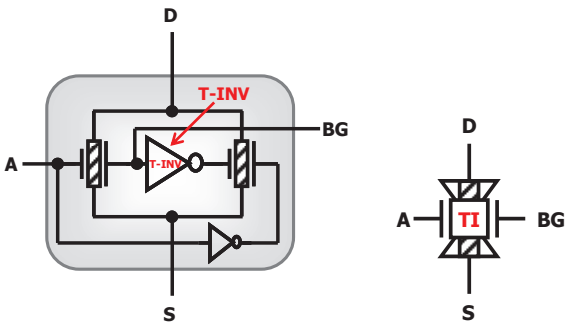
- If BG=1 → A⊕BG = 0 and the structure T conducts if and only if A=1 ➔ N-type transmission gate.

- If BG=0 → A⊕BG = 0 and the structure T conducts if and only if A=0 ➔ P-type transmission gate.

Thus, the T structure behaves in the same way as would a single Am-IDGFET whose configuration (N- or P-type) depends only on its *absolute* back-gate value.

However, some reconfigurable cells use the third state of the DGFET (the OFF state) which is not available with the structure T. Since the OFF state corresponds to $|V_{DS}/2| = +V/2$ in our case, the use of a ternary inverter instead of the conventional inverter linking the back-gates of the two transistors in parallel in figure 3-2(a) can resolve this issue and make the OFF state of the T structure possible.

The structure of the transmission gate allowing switching between the three states (N, P and OFF) using a ternary inverter (T-INV) is shown in figure 3-3(a) and it is abbreviated as "TI". Figure 3-3(b) shows the symbol of the structure.



(a) (b)

Figure 3-3. DGFET ternary transmission gate: structure (a), symbol (b)

The T-inverter supplies the back-gate of the parallel DGFET and operates according to {+V→0V, +V/2→+V/2, 0V→+V}. The structure of the T-inverter used within the structure "TI" is presented in figure 3-4; it is composed of two transistors and two resistors of equal value (100kΩ). In the validation and evaluation chapter, we will discuss and evaluate the behavior of this T-inverter. Also, the choice of the resistance value will be justified.

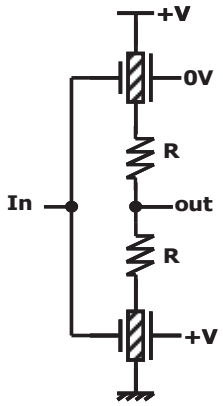


Figure 3-4. T-inverter structure

3.2.3.2 2-input dynamic logic cells with ambipolar DGFETs

The generic structures of reconfigurable cells corresponding to each class has been presented in table 3-2 by supposing that every transistor within the function path can be configures to one of the three states (N, P, or OFF). In this section, we describe 4 different reconfigurable dynamic logic cells applying this approach and using the previously described transmission gate structures (T and TI) in the function path.

As we use dynamic logic design, it is necessary to pay particular attention to the design method in order to avoid the "*Evaluation*" problem encountered when cascading dynamic logic gates. Indeed, with simple cascading of dynamic logic stages, the pre-charged high

voltage on the output node of the second stage may be inadvertently (partially) discharged by its logic inputs which have not yet reached final correct (low) values from the first stage evaluation operation. Hence, we cannot simply cascade dynamic logic gates without reliably preventing unwanted loss of charge from pre-charged nodes.

There are many techniques to correct the operation of cascaded dynamic logic gates, of which the following three are the most frequent:

i) Four phase non-overlapping clocks as in [3-20, 3-21]. However, this can still be subject to local delay variation and further requires complex clock generation circuitry.

ii) Use of inverters to create Domino Logic by placing an inverter in series with the output of each gate [3-22]. This approach avoids the race problem of cascaded dynamic CMOS since the precharged (high) output of the first stage will by default be inverted to prevent N-type transistors in the function path of the second stage from turning on and discharging the second stage output node. However, all circuits only provide non-inverted outputs, and more logic area is used by the additional inverters.

iii) NP Domino Logic (NORA logic) [3-23]. This is an elegant solution to provide an alternate race-free approach to cascading dynamic logic by using two flavors (Pull-up "P-tree" and Pull-down "N-tree") of dynamic logic. A disadvantage of the NORA logic style is that the P-tree blocks are slower than the N-tree blocks, due to the lower mobility of the PMOS transistors in the logic network. Equalizing the propagation delays requires extra area.

Except the first technique of using four phase non-overlapping clocks, none of above techniques can be used in our case, since the function paths are reconfigurable and can change from N-type to P-type such that no guaranteed precharge conditions can be established to prevent transistors turning on ahead of evaluation, as required by the rules of design in ii) and iii).

a. *Double–Stage 2-input reconfigurable cells*

In table 3-2 we presented four 2-input function classes and detailed all possible cases. Here, we present two dynamic-logic reconfigurable cells derived from the table. The first achieves the complete set of 16 functions and represents class 4 in the table. The second, with fewer transistors, offers 14 functions and represents class 3 in the table. Both cells are composed of 2 stages: the logic function stage and the follower/inverter stage.

- *Full functionality 2-input reconfigurable cell*

Figure 3-5 shows the dynamically reconfigurable cell based on SOP and abbreviated SOP-DRLC. Transistors TI1 and TI2 of the function path are placed in series to form a first minterm (wired AND), while TI3 and TI4 form a second minterm. Both structures are connected in parallel (wired OR) to enable the potential use of the sum of both minterms. It may be configured to one of 16 basic binary operation modes (Table 3-3). The logic function

block could be implemented using POS forms (structure S3' of table II), but it is expected that it will have almost the same structure and the POS form is used further to design a single stage reconfigurable cell.

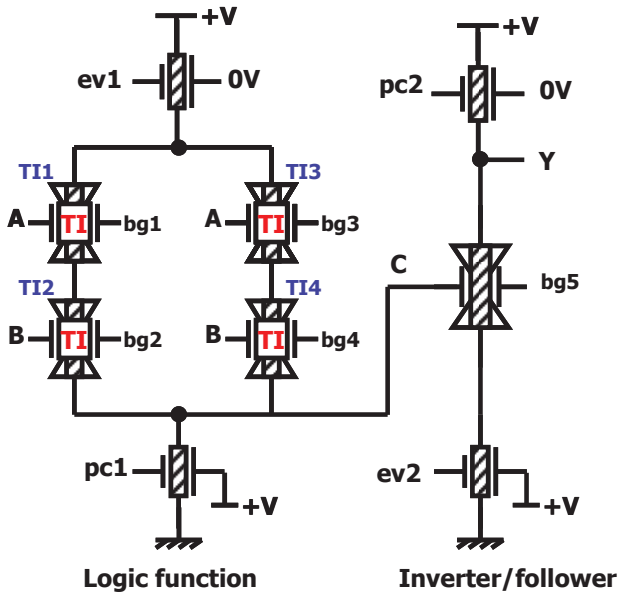


Figure 3-5. SOP based dynamically reconfigurable dynamic logic cell SOP-DRLC

The implementation of this cell requires single polarity inputs (i.e. 0V for logic "0" and +V for logic "1"), to avoid additional inverters and dual rail interconnects. In the case of complemented inputs, Am-IDGFETs can be configured to P-type using the corresponding PG voltage (-V). In this cell, there are ten inputs and one output:

- two boolean data inputs A and B (where the logic levels are represented by the supply voltage values 0V and +V)
- five control inputs $bg_{\{1\text{-}5\}}$ to configure the circuit
- a four-phase clock signal set consisting of 2 precharge inputs pc1, pc2 and 2 evaluation inputs ev1, ev2. The signals are non-overlapping as in classical CMOS dynamic logic gates
- circuit output "Y"

These circuit signals are illustrated in figure 3-6, showing a cyclic simulation of the SOP-DRLC circuit in the NAND configuration.

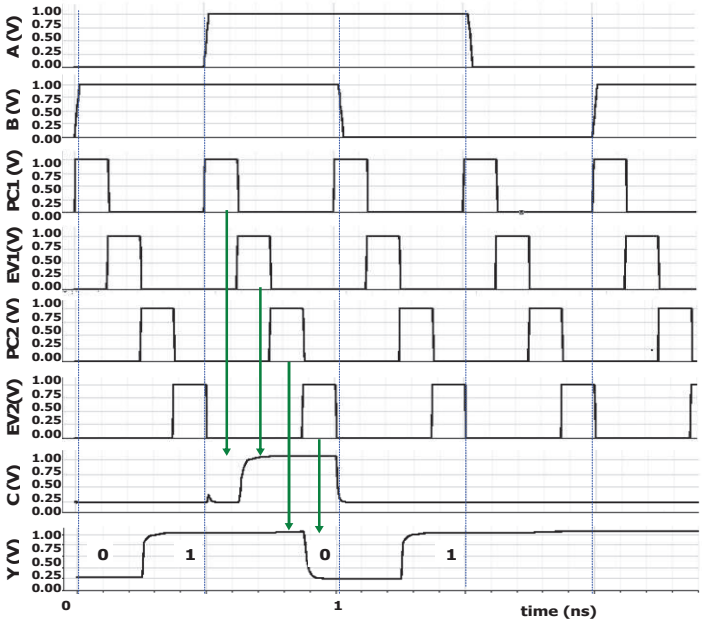


Figure 3-6. Simulation results for SOP-DRLC in NAND configuration

The available basic binary operations and the associated configuration BG voltage combinations are shown in table 3-3.

TABLE 3-3. SOP-DRLC CONFIGURATION SIGNALS AND CORRESPONDING BOOLEAN OPERATIONS

bg1=bg	bg3	bg4	bg5	Y
V/2	0V	0V	0V	$\overline{A+B}$
V/2	0V	0V	+V	$A+B$
V/2	+V	0V	+V	$\overline{A}+B$
V/2	0V	+V	+V	$\overline{B}+A$
V/2	0V	+V	0V	$\overline{A}\bullet B$
V/2	+V	0V	0V	$\overline{B}\bullet A$
V/2	+V	+V	0V	$A\bullet B$
V/2	+V	+V	+V	$\overline{A\bullet B}$
+V	0V	+V	+V	$\overline{B}$
+V	0V	+V	0V	B
+V	+V	0V	0V	A
+V	+V	0V	+V	$\overline{A}$
0V	+V	+V	0V	$\overline{A\oplus B}$
0V	+V	+V	+V	$A\oplus B$
V/2	V/2	V/2	0V	$\perp$
V/2	V/2	V/2	+V	T

- *Partial functionality 2-input reconfigurable cell*

The previous cell SOP-DRLC was an implementation of the logic structure of the class 4 from table 3-2. The cell can achieve the whole set of 16 functions. In this section, we prove that it is also possible to build reconfigurable cells with partial functionality and requiring

fewer transistors by using other classes. Here, we use the generic structure S3 from table 3-2 to design a 14 functions reconfigurable logic cell. This cell (Fig. 3-7) is arranged in two dynamic logic stages (logic function and follower/inverter) and can be configured to any one of 14 basic binary operation modes according to table 3-4. The first stage uses requires fewer transistors than the full-functionality cell. Only three configuration signals are required - reconfiguration of the cell depends on the back gate voltages V_{bA}, V_{bB}, V_{bC} (each of which can take one of three voltage levels: 0V, V/2 or +V, which result respectively in a P-type, OFF or N-type behaviour). The input signals are the two Boolean inputs A and B, while clock signals are global precharge and evaluation inputs pc1, ev1, pc2 and ev2.

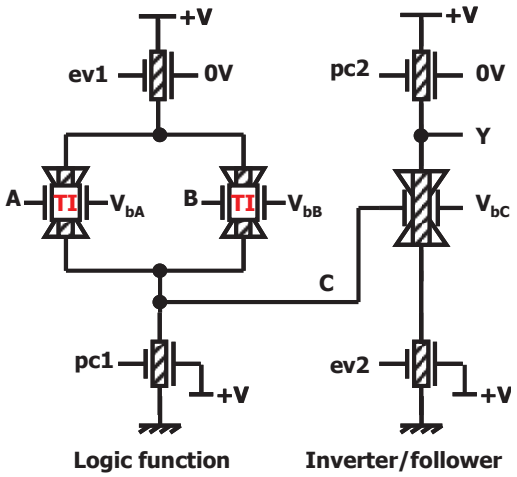


Figure 3-7. Dynamically reconfigurable dynamic logic cell (DRLC-7T) [25]

TABLE 3-4. 3-INPUT CONFIGURATIONS FOR DRLC-7T WITH 3 LOGIC LEVELS (0V, V/2, +V) AND CORRESPONDING 14 BASIC BINARY LOGIC FUNCTIONS

V_{bA}	V_{bB}	V_{bC}	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	0V	$A+B$
+V	V/2	+V	$\overline{A}$
+V	V/2	0V	A
0V	0V	+V	$A \bullet B$
0V	0V	0V	$\overline{A \bullet B}$
+V	0V	+V	$B \bullet \overline{A}$
+V	0V	0V	$A+\overline{B}$
V/2	+V	+V	$\overline{B}$
V/2	+V	0V	B
V/2	V/2	V/2	T
V/2	V/2	0V	$\perp$
0V	+V	+V	$A \bullet \overline{B}$
0V	+V	0V	$\overline{A}+B$
INACCESSIBLE			$\overline{A \oplus B}$
INACCESSIBLE			$A \oplus B$

b. ***Single–Stage 2-input reconfigurable cell***

Unlike the two previously designed cells, this cell uses only one stage (without the need of the inverter/follower stage) and realizes the whole set of functions (except for the "true", or unconditional "1", function) by exploiting the possibility to express a function as a POS or as SOP (*promoting the form which requires a lower transistor count*) using the same circuit. Since there is no cascading of stages, the cell uses only one clock signal.

Figure 3-8 illustrates the transistor level implementation of the single-stage dynamically reconfigurable cell abbreviated as SS-DRLC. TI1 and TI2 of the function path are placed in parallel (wired OR) to form a first maxterm, while TI3 and TI4 form the second maxterm. Both structures are connected in series (wired AND) to enable the potential use of the product of both maxterms. Further, by switching OFF one of the two TI structures in each maxterm (i.e. TI2 / TI3 or TI1 / TI4) the other transistor pair will form a structure of two transistors in series. In this way, functions in minterm form can also be implemented. The cell may thus achieve 15 basic binary operations (Table 3-5). The "true" function is missing, because the function path is a pull-up network and cannot be made unconditionally conducting.

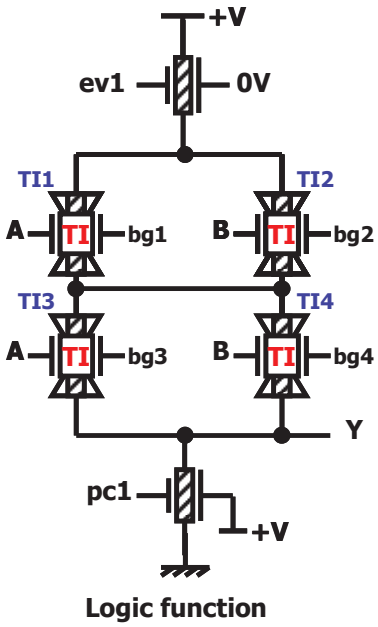


Figure 3-8. Single-stage dynamically reconfigurable dynamic logic cell SS-DRLC

TABLE 3-5. SS-DRLC CONFIGURATION SIGNALS AND CORRESPONDING BOOLEAN OPERATIONS

bg1	bg2	bg3	bg4	Y
0V	V/2	V/2	0V	$\overline{A+B}$
+V	+V	+V	+V	$A+B$
0V	+V	0V	+V	$\overline{A}+B$
+V	0V	+V	0V	$\overline{B}+A$
0V	V/2	V/2	+V	$\overline{A}\bullet B$
+V	V/2	V/2	0V	$\overline{B}\bullet A$
+V	V/2	V/2	+V	$A\bullet B$
0V	0V	0V	0V	$\overline{A\bullet B}$
V/2	0V	V/2	0V	$\overline{B}$
V/2	+V	V/2	+V	B
+V	V/2	+V	V/2	A
0V	V/2	0V	V/2	$\overline{A}$
+V	0V	0V	+V	$\overline{A\oplus B}$
+V	+V	0V	0V	$A\oplus B$
V/2	V/2	V/2	V/2	$\perp$
INACCESSIBLE				T

3.2.3.3 2-input static logic reconfigurable cell with Am-IDGFETs

The previously described dynamic structure demonstrates an attractive flexibility to switch between wired OR and wired AND, and achieves almost the whole set of functions. In this section, we derive a static logic cell from the previous dynamic cell, by duplicating the pull-up network to achieve the complementary static logic composed of pull-up network and pull-down network. In the same way as dynamic logic cells, TI structures are used for both networks, so no logic degradation is observed, independently of the type of the structure (N, P, OFF) and its position within the cell (pull-up or pull-down).

Figure 3-9 illustrates the transistor-level implementation of the complementary static logic dynamically reconfigurable cell abbreviated as CSL-DRLC. The cell may thus achieve 14 basic binary operations (Table 3-6). The functions "true" and “false” are missing.

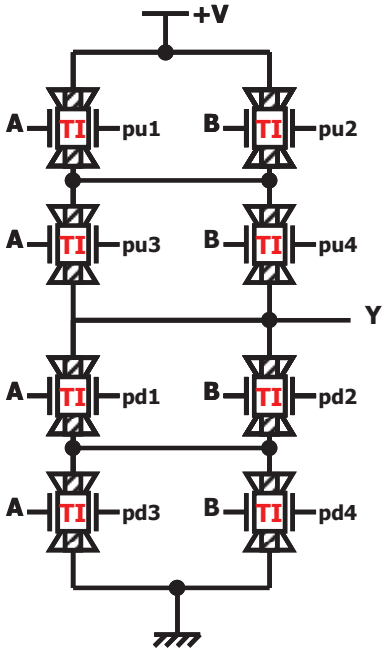


Figure 3-9. Complementary static logic dynamically reconfigurable dynamic cell CSL-DRLC

TABLE 3-6. SS-DRLC CONFIGURATION SIGNALS AND CORRESPONDING BOOLEAN OPERATIONS

pu1	pu2	pu3	pu4	pd1	pd2	pd3	pd4	Y
0V	V/2	V/2	0V	+V	+V	+V	+V	$\overline{A+B}$
+V	+V	+V	+V	0V	V/2	V/2	0	$A+B$
0V	+V	0V	+V	+V	V/2	V/2	0V	$\overline{A}+B$
+V	0V	+V	0V	0V	V/2	V/2	+V	$\overline{B}+A$
0V	V/2	V/2	+V	+V	0V	+V	0V	$\overline{A}\bullet B$
+V	V/2	V/2	0V	0V	+V	0V	+V	$\overline{B}\bullet A$
+V	V/2	V/2	+V	0V	0V	0V	0V	$A\bullet B$
0V	0V	0V	0V	+V	V/2	V/2	+V	$\overline{A\bullet B}$
V/2	0V	V/2	0V	V/2	+V	V/2	+V	$\overline{B}$
V/2	+V	V/2	+V	V/2	0V	V/2	0V	B
+V	V/2	+V	V/2	0V	V/2	0V	V/2	A
0V	V/2	0V	V/2	+V	V/2	+V	V/2	$\overline{A}$
0V	0V	+V	+V	+V	0V	0V	+V	$\overline{A\oplus B}$
+V	0V	0V	+V	0V	0V	+V	+V	$A\oplus B$
INACCESSIBLE								$\perp$
INACCESSIBLE								T

3.2.4 Summary of the function classification approach

By exploiting the in-field reconfigurability specific to ambipolar DG-FET devices, we described a novel design methodology inspired from the concept of "function classification" which groups functions according to some specific property. By matching each class to its generic structure, we investigated the bottom-up hierarchical correlations between various classes to build ambipolar DG-FET-based reconfigurable cells with partial or complete functionality based on dynamic-logic style and extend them to build static-logic cell. The

evaluation and comparison of all logic cells designed in this chapter are detailed in chapter 4 of the dissertation.

3.3 Binary-decision-diagrams with Ambipolar double-gate FET (Am-BDD) for reconfigurable fine-grain logic

In this section, we explore the use of BDDs in the context of reconfigurability using Am-IDGFETs. Conventional BDDs, developed for unipolar three-terminal devices, cannot be applied directly in the case of Am-IDGFET devices and must therefore be adapted. In this section, we tackle two main issues: (i) how to adapt BDDs to represent the additional terminal and states of the switch (this is a valid issue for any multiple-gate devices, where the gates are independent); and (ii) how to adapt BDDs to represent the extra dimension of reconfigurability in the switching networks.

In light of these issues, we propose a novel Ambipolar Binary Decision Diagram (Am-BDD), to adapt this technique to logic built with such devices. We demonstrate how this method enables us to build Am-IDGFET-based n-input reconfigurable cells based on pass-transistor-logic obtained from Am-BDDs. We can choose the reconfigurable functions that should be attainable by the synthesized gate, map their corresponding Am-BDD and thus tune the functionality of Am-IDGFETs at the circuit level to perform different functions at the output. To validate the approach, a library of reconfigurable cells with partial and complete functionality was built using the Am-BDD technique.

3.3.1 Am-IDGFET-based BDD for reconfigurable logic cells

For Am-IDGFETs, no systematic design methodology exists to generate reconfigurable cells from function definition. In this section, we describe a method through its constituent steps and rules that should be applied, from the specification of the output function through to the circuit implementation at the transistor level.

In order to adapt the BDD technique to the DG-FET device, we first consider the specific impacts of representing the device with respect to conventional BDDs. Firstly, one node can have more than two edges depending on the functions attainable at the output; secondly, a single edge can take different values; and thirdly, multiple functions can be mapped onto the same BDD sharing the same output. All these considerations are integrated into a design methodology for n-input reconfigurable cells. The steps of the proposed method are the following:

Step 1
Define the set of functions to be realized at the output of the reconfigurable cell
Step 2
Map BDDs of all functions to the same BDD (to identify shared nodes and edges) /* This common BDD will be abbreviated Am-BDD (for Ambipolar-BDD). One important point here is the necessity to use the same variable ordering when mapping the BDD of each function. */
Step 3
Label every edge connecting two different nodes in Am-BDD
Step 4
Define rules to be respected before implementing the Am-BDD into a pass-transistor network. The edges mapped in the graph will be represented as transistors at the circuit level according to the following rules:

1. *If an edge is used by all functions in the Am-BDD then*
   a. *If the edge value is the same for all functions, the transistor representing this edge does not need to be reconfigurable at the circuit level.*
   b. *If there is a difference between the edge values, the transistor representing this edge is reconfigurable at the circuit level and will be in either n- or p-state.*
2. *If an edge is not used by all functions in the Am-BDD, then the transistor representing this edge is reconfigurable at the circuit level and must include the off-state.*

Step 5
Trace the configuration table and identify correlations. /*It contains every functions and the corresponding edges values. A correlation can exist between edges.
Step 6
Implement the AmBDD into pass-transistor circuit. /* A '0' edge means that the corresponding transistor is configured as P-type (PG=0V), while a '1' edge means that the corresponding transistor is configured as N-type (PG=+V). If an edge is not used by a function, its corresponding transistor will be switched off (PG=V/2). */

3.3.2 Example of Am-BDD implementation

To illustrate the method of building a reconfigurable cell using BDDs and ambipolar DG-FET properties we choose a simple case where we wish to reconfigure between two arbitrary functions: $F_1 = \neg(A+B+C)$ and $F_2 = \neg(A.B.C)$. We will also use this example to observe how configuration signals can be correlated. As we illustrated with dynamic cells in the first part of this chapter, TI structures replace single ambipolar transistors in some points of the circuit to avoid logic degradation.

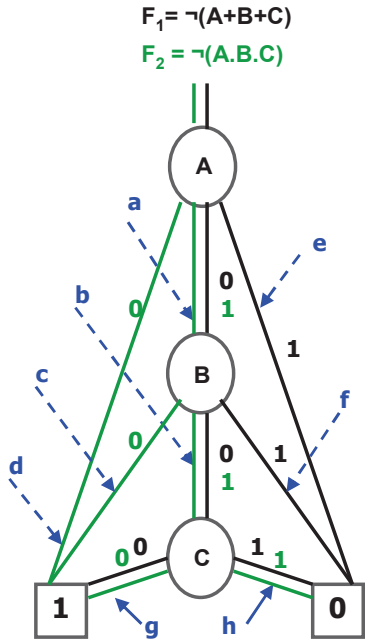


Figure 3-10. Am-BDD of 2 arbitrary functions

The steps described in section 3.3.1) are applied to both functions:

Step 1

The functions to be realized at the output of the reconfigurable cell are F_1= ¬(A+B+C) and F_2= ¬(A.B.C).

Step 2

Figure 3-10 represents the (Am-BDD) *using the same variable ordering* of inputs (A, B, C).

Step 3

Edges connecting two *different* nodes in the Am-BDD are labelled as follows: *A-B=a, B-C=b, B-0=c, A-0=d, A-1=e, B-1=f, C-0=g, C-1=h*

Step 4

1. a. For edges (g, h), F_1 and F_2 share the same value, indicating that the transistors representing those edges do not need to be reconfigurable at the circuit level.

   b. For edges (a, b), F_1 and F_2 do not share the same edge value, indicating that the transistors representing these edges should be reconfigurable at the circuit level between the N- and P-states.

2. Edges (c, d) are used only by F_2 and edges (e, f) are used only by F_1. The transistors representing these edges are reconfigurable at the circuit level between the P- and off-states for edges (c, d) and between the N- and OFF-states for edges (e, f).

Step 5

Table 3-7 shows the configuration signals required for each function.

TABLE 3-7. F_1/F_2 FUNCTION CONFIGURATION TABLE

F	a	b	c	d	e	f
F_1=¬ (A+B+C)	0V	0V	V/2	V/2	+V	+V
F_2=¬ (A.B.C)	+V	+V	0V	0V	V/2	V/2

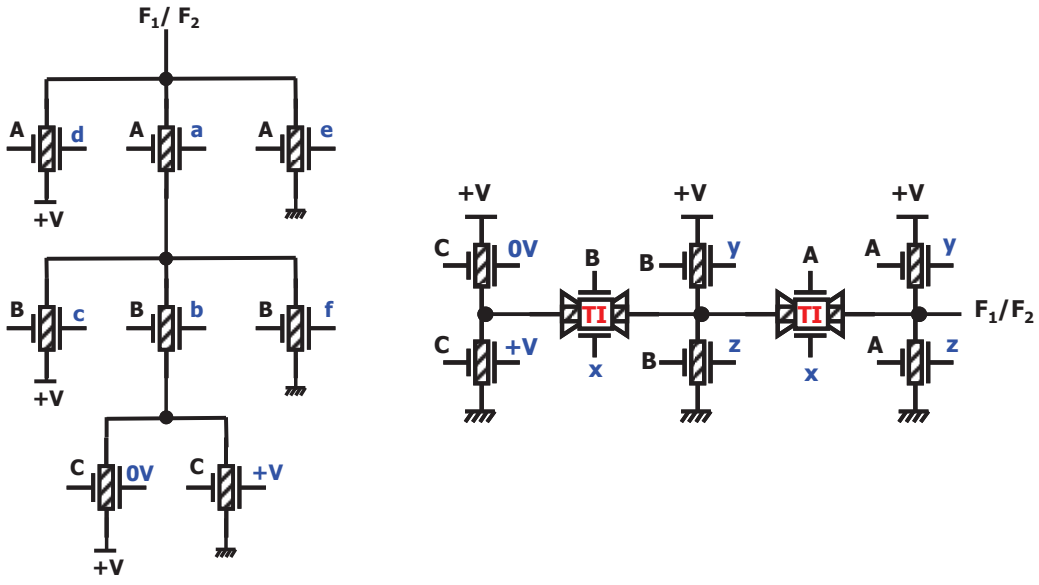
Correlations exist between certain edges (which share the same values) and will be detailed below. The set of optimized configuration signals resulting from correlation analysis is given in Table 3-8.

TABLE 3-8. OPTIMIZED 2-FUNCTION CONFIGURATION TABLE

F	x	y	z
F_1=¬ (A+B+C)	0V	V/2	+V
F_2=¬ (A.B.C)	+V	0V	V/2

Step 6

The implementation of the pass-transistor circuit is shown in Figure 3-11.



(a) (b)

Figure 3-11. Reconfigurable cell based on PTL: direct transposition from Am-BDD (a) conventional representation with TI structures and optimized number of control signals (b)

The implemented circuit (Fig. 3-11) is thus a reconfigurable cell with six control signals (a, b, c, d, e, and f) able to realize F_1 or F_2 by choosing the corresponding values of control signals as shown in the configuration table (Table 3-7). Edges g and h are not in the configuration table since the transistors implementing those edges do not need to be reconfigurable.

- Identification of correlations to minimize the number of configuration signals

The number of control signals in a reconfigurable cell is an aspect of fundamental interest, since it impacts directly on the number of required memory cells and consequently on overall circuit complexity. For this reason, it is useful to extract specific correlations from the configuration table to reduce the total number of control signals.

Through analysis of the configuration table, we can see that some edges retain a common value when changing the configuration to realize a different output function. For example in F_1, a = b = 0V, while in F_2, a = b = +V. Thus for all output functions (F_1 or F_2) a = b, such that the same control signal can and should be used for both transistors representing 'a' and 'b'. From table 3-7, we can easily identify such direct correlations: (a = b) = x, (c = d) = y and (e = f) = z, such that only three control signals are required (instead of six).

Indirect logical correlations can also exist between inputs (such as inversion or more complex Boolean dependencies), which can further reduce the number of control signals and alleviate configuration memory requirements. However, this must of course be offset by the logic required to handle the indirect correlations.

If we aim to have non-inverted functions, an inverter can simply be cascaded at the output. Figure 3-12 shows the simulated waveforms of the cell configured sequentially to both functions $\neg F_1$ and $\neg F_2$. We notice that the model used for simulations is described later in chapter 4, and that the simulation result shown here is for functional validation purposes only. Cyclic simulations at a frequency of 2GHz show that both functions are obtained by varying the configuration signals. No logic level degradation was observed.

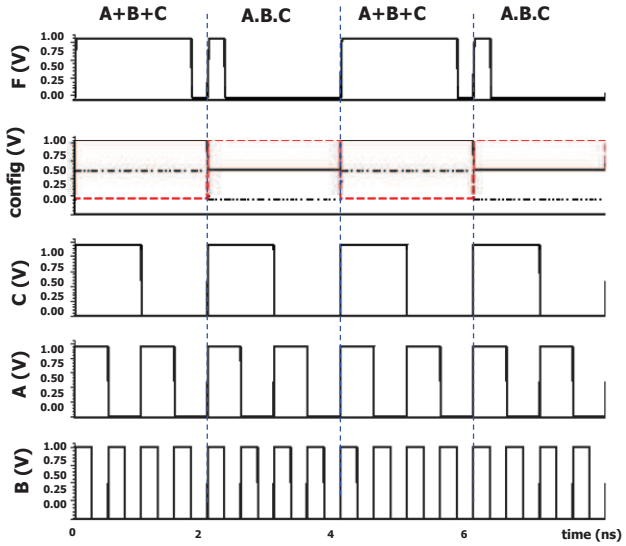


Figure 3-12. Circuit validation of 2-input reconfigurable cell

In this simple example of only two functions, we showed in detail the utility of AmBDDs to synthesize reconfigurable logic cells methodically. More complex cases are presented in the following sections, where we aim to design reconfigurable logic cell that can realize 16 functions at the output.

3.3.3 2-input reconfigurable logic cells generated from Am-BDD

In this section, we apply the Am-BDD technique to several examples of 2-input reconfigurable cells. We will firstly introduce a cell targeting the implementation of a complete set of 16 functions. Two other 2-input cells were subsequently derived with partial functionality in order to show the dependency between the number of functions at the output and the complexity of the corresponding generated circuits (transistor count, number of configurations signals, etc). The main purpose is to show the ability of Am-BDD technique to generate reconfigurable cells with a large number of achievable functions.

3.3.3.1 Full-function set 2-input reconfigurable cell (16F-AmBDD)

The general structure of the Am-BDD aiming to map the 16 different functions is shown in Figure 3-13. In the figure, we have only represented the various nodes and edges for the sake of clarity; the corresponding values of the configuration signals for each edge are shown in table 3-9. Figure 3-14 represents the final circuit implementation of the 2-input reconfigurable cell.

In the Am-BDD we chose a variable ordering (A, B). In view of the fact that the technique requires the same variable ordering for all functions when mapping the Am-BDD, functions which do not include the variable A in their expression (i.e. 1, ¬B, B, 0) require a direct path to the output without using node A (edges a, c, f, h).

This example shows that the method can be adapted to some issues such as variable ordering (incurring however a penalty of more edges). Furthermore, it shows that the technique is sufficiently flexible to be applied to any number of output functions. The new designed Reconfigurable Static Logic cell is shown in figure 3-14 and is abbreviated (16F-AmBDD).

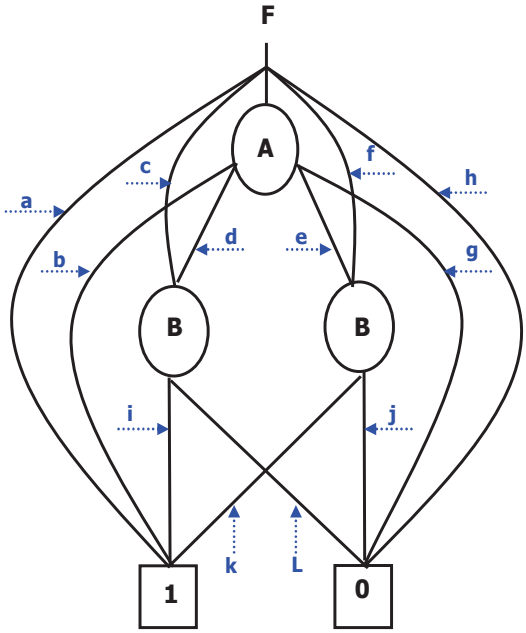


Figure 3-13. Am-BDD of 2-input reconfigurable cell

TABLE 3-9. 16-FUNCTIONS CONFIGURATION TABLE

a	b	c	d	e	f	g	h	i	j	k	l	F
V/2	V/2	V/2	0V	V/2	V/2	+V	V/2	0V	V/2	V/2	+V	$\overline{A+B}$
V/2	+V	V/2	V/2	0V	V/2	V/2	V/2	V/2	0V	+V	V/2	$A+B$
V/2	0V	V/2	V/2	+V	V/2	V/2	V/2	V/2	0V	+V	V/2	$\overline{A}+B$
V/2	V/2	V/2	+V	V/2	V/2	0V	V/2	0V	V/2	V/2	+V	$A\bullet\overline{B}$
V/2	+V	V/2	0V	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	$A+\overline{B}$
V/2	V/2	V/2	V/2	0V	V/2	+V	V/2	V/2	0V	+V	V/2	$B\bullet\overline{A}$
0V	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	T
V/2	V/2	V/2	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	V/2	$\perp$
V/2	V/2	V/2	V/2	+V	V/2	0V	V/2	V/2	0V	+V	V/2	$A\bullet B$
V/2	0V	V/2	+V	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	$\overline{A\bullet B}$
V/2	+V	V/2	V/2	V/2	V/2	0V	V/2	V/2	V/2	V/2	V/2	A
V/2	0V	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	V/2	V/2	$\overline{A}$
V/2	V/2	+V	V/2	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	$\overline{B}$
V/2	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	0V	+V	V/2	B
V/2	V/2	V/2	0V	+V	V/2	V/2	V/2	0V	0V	+V	+V	$\overline{A\oplus B}$
V/2	V/2	V/2	+V	0V	V/2	V/2	V/2	0V	0V	+V	+V	$A\oplus B$

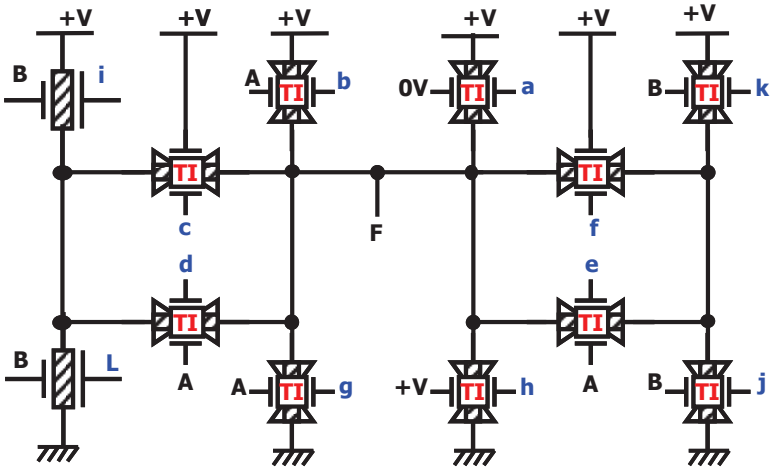


Figure 3-14. 16F-AmBDD schematic

3.3.3.2 Partial-functionality 2 inputs reconfigurable cells

The main issue of the 16F-AmBDD cell is the high number of configuration signals, which can lead, at the architectural level, to a heavy use of interconnections and memory resources inducing layout congestion and a consequent increase in power consumption, delays and area. In this section, by pruning the complete Am-BDD diagram of figure 3-13 and its corresponding table 3-10, we build reconfigurable logic cells with partial functionality and which consequently require fewer transistors and configuration signals.

According to the diagram in figure 3-13 and by scanning the corresponding configuration table 3-9, we can clearly observe that some edges such as (a, c, f, h) are used only once to

realize a single function (T, ¬B, B, ⊥ respectively). Hence these edges are candidates for pruning, in order to focus only on functions which share intensively the same edges.

We introduce two different reconfigurable cells achieving different function sets. In figure 3-15, Cell 1 (abbreviated as 12F-AmBDD) uses a more compact structure by requiring fewer transistors and is capable of achieving 12 functions (excluding T, ¬B, B, ⊥ from the complete set) according to the configuration table 3-10. Cell 2 (abbreviated as 6F-AmBDD) is an even more compact cell (figure 3-16) but can only handle 6 elementary logic functions according to the configuration table 3-11.

TABLE 3-10. 12-FUNCTIONS CONFIGURATION TABLE

b	d	e	g	i	j	k	l	F
V/2	0V	V/2	+V	0V	V/2	V/2	+V	$\overline{A+B}$
+V	V/2	0V	V/2	V/2	0V	+V	V/2	$A+B$
0V	V/2	+V	V/2	V/2	0V	+V	V/2	$\bar{A}+B$
V/2	+V	V/2	0V	0V	V/2	V/2	+V	$A\bullet\bar{B}$
+V	0V	V/2	V/2	0V	V/2	V/2	+V	$A+\bar{B}$
V/2	V/2	0V	+V	V/2	0V	+V	V/2	$B\bullet\bar{A}$
V/2	V/2	+V	0V	V/2	0V	+V	V/2	$A\bullet B$
0V	+V	V/2	V/2	0V	V/2	V/2	+V	$\overline{A\bullet B}$
+V	V/2	V/2	0V	V/2	V/2	V/2	V/2	A
0V	V/2	V/2	+V	V/2	V/2	V/2	V/2	$\bar{A}$
V/2	0V	+V	V/2	0V	0V	+V	+V	$\overline{A\oplus B}$
V/2	+V	0V	V/2	0V	0V	+V	+V	$A\oplus B$

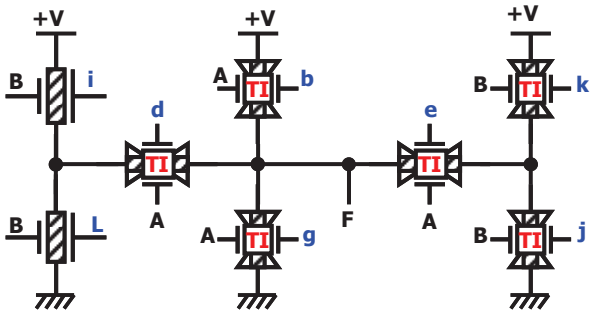


Figure 3-15. 12F-AmBDD schematic

TABLE 3-11. 6-FUNCTIONS CONFIGURATION TABLE

b	d	g	i	l	F
V/2	0V	+V	0V	+V	$\overline{A+B}$
V/2	+V	0V	0V	+V	$A\bullet\bar{B}$
+V	0V	V/2	0V	+V	$A+\bar{B}$
0V	+V	V/2	0V	+V	$\overline{A\bullet B}$
+V	V/2	0V	V/2	V/2	A
0V	V/2	+V	V/2	V/2	$\bar{A}$

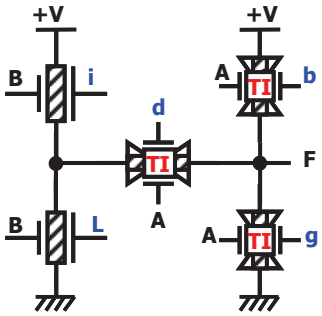


Figure 3-16. 6F-AmBDD schematic

3.3.4 Summary of the AmBDD approach

We have described and evaluated an approach presenting a systematic design methodology specifically exploiting Am-IDGFETs to build reconfigurable PTL cells using BDD. The methodology was illustrated with a simple example to observe in detail various steps of the

approach and highlight the correlation that can exist between configuration signals. We resort to transmission gates instead of single Am-IDGFET to resolve the issue of logic degradation, and we showed how the correlation between configuration signals can decrease their total number. Using this Am-BDD design approach, we designed a reconfigurable 2-input cell capable of achieving 16 functions (16F-AmBDD). The main disadvantage of this circuit synthesis technique remains the high number of configuration signals. To further inspect the cells obtained from the Am-BDD approach and try to limit/solve the number of configuration signals, we propose two other more compact cells with partial functionality derived from the original 16F-AmBDD cell. The validation and evaluation of the whole pack of cells is detailed in the next chapter (chapter 4).

3.4 General conclusion

Based on Am-IDGFETs, a new class of device capable of operating as either N-type or P-type switches according to the back gate bias voltage, we have defined two reconfigurable logic synthesis techniques. We firstly investigated the function classification concept which represents a powerful tool in both the construction and analysis of Boolean functions. We exploited this conventional tool to build reconfigurable logic blocks by defining a hierarchical correlation between structures of classes. A library of reconfigurable dynamic logic cells was built using this method, as well as a static logic cell. Furthermore, in the same context of logic synthesis techniques, we propose an Ambipolar Binary Decision Diagram (Am-BDD), to adapt the conventional BDD logic synthesis and verification technique to Am-IDGFET devices. We demonstrate how this method enables us to build Am-IDGFET-based n-input reconfigurable cells based on pass-transistor-logic obtained from Am-BDDs. We also show how specific correlations between configuration signals can lead to a minimization of their total number. Using the Am-BDD technique, we designed a reconfigurable 2-input cell capable of achieving 16 functions and we derived more compact cells with partial functionality. At a transistor level implementation, we explained how the use of ambipolar transmission gates to replace some single critical Am-IDGFETs can be an efficient solution to avoid logic degradation and ensure the proper operation of the synthesized circuits. The validation of both design approaches and the evaluation of their capabilities to offer a new paradigm of reconfigurable logic with improved performance metrics are investigated in the next chapter.

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Chapter 4

Validation and evaluation of design methodologies and techniques

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4.1 Introduction

This part of the thesis presents a validation and estimation of the whole set of novel approaches to design logic circuits with Am-IDGFETs, described in chapters 2 and 3. When it comes to the evaluation of electrical performance metrics of logic circuits, the device model has prime concern. This work can be implemented with any type of Am-IDGFETs, but we choose to validate our generated circuits with Double Gate CNTFET devices using the most accurate model available in the literature, as described and detailed in the first part of this chapter.

Many works studied ambipolar CNTFET-based circuits [4-1, 4-2, 4-3, 4-4, 4-5]. The central question related to the assessment of the benefits of the designed logic circuits concerns the accuracy of the given results. The device model is of course the cornerstone of result accuracy. For example in [4-1], in order to simulate several libraries of logic gates, Ben Jamaa uses the Stanford CNTFET model which is in reality developed for unipolar devices [4-2]. To append the reconfigurability of DG-CNTFET via the second gate, the unipolar device is "emulated" as two N-and P-type unipolar devices in parallel. This can give an idea about the behavior of the circuit, for instance the output swing, but very accurate estimation of the delay and power consumptions cannot be derived. In the framework of the NANOGRAIN project, the research teams (INL-Lyon IMS Bordeaux, and CEA-LETI) cooperated together to contribute to the electrical and physical modelling of compact carbon nanotube transistors [4-3], in order to evaluate the metrics of a set of reconfigurable DG-CNTFETcells [4-4]. In [4-5], based on the CNTFET compact model developed by InESS-Strasbourg, several standard logic gates were designed and a package of fault tolerance techniques was investigated. All these works represent encouraging initiatives and push the progress of research on design with ambipolar devices. However, simulations are in these cases carried out with a simple model based on a limited number of parameters (essentially the Chirality of the nanotube, contact resistances and temperature). Limited to thermionic transport, such a model does not take into account other physical phenomena within the device such as coupling between the two gates, SB (sub-band) modelling or BTBT (band-to-band tunnelling). This leads to erroneous calculation of the current which, in turn, will give incorrect estimation of power and delays of the designed circuits.

The special feature of this chapter is that we refine the approaches used by previous works in terms of technology, device optimization and design thanks to the synergy between different research teams (INL, CEA-LETI and IMS). Concerning technology and layout, a credible technology process and device layout are proposed in close collaboration with CEA-LETI in the framework of the NANOGRAIN project. Also, device optimization and modeling is performed through simulation in order to ensure correct hypotheses for the analysis thanks to rigorous work with IMS research group. The contribution of INL is illustrated through this thesis work.

In addition to the evaluation of the design approaches in CNT technology, we carry out an exhaustive comparison with the most advanced CMOS technology node available in the community by using a predictive model for 16nm CMOS technology. Dimensions of both devices (DG-CNTFET and CMOS-16nm) are calibrated to match their I-V characteristics in order to make the comparison objective and fair.

Based on well described device models, we validate with accurate electrical simulations the set of logic circuits generated from all design theories described in this thesis:

- TTSM approach and low-power design technique for standard cells as described in chapter 2
- AmBDD technique and function classification approach for reconfigurable cells as described in chapter 3

A detailed description of the DG-CNTFET device is presented at the beginning of the chapter with a brief depiction of the CMOS-16nm model used for comparisons purposes. Then, the dimensions of the CMOS 16-nm devices are calibrated to furnish figures leading to meaningful comparisons with the DG-CNTFET. Finally, each approach is evaluated and discussed based on the results obtained from simulations of the various circuits and gates already designed and described in chapters 2 and 3.

4.2 Technological Assumptions and Device Modeling

In order to consider the benefits of the generic design approaches at the circuit level, we need to simulate the electrical behaviour of the designed logic gates. This requires a precise physical model, which, in turn, depends on the underlying technology. The technological assumptions and physical compact model for the DG-CNTFET device are detailed in this section. For the CMOS gates, we introduce a CMOS-16nm model and we calibrate the transistor width for comparison purposes.

4.2.1.1 DG-CNTFET technological hypotheses

Most experiments on CNT-FETs have been on back-gated devices because of the simplicity of their fabrication. Recently in [4-6] CEA-LETI proposed, in the context of the

NANOGRAIN project, a DG-CNTFET structure with one top-gate and one back-gate following a process flow based on Silicon-On-Insulator (SOI) wafers. In this process, it is possible to build silicon mesas (i.e. islands of silicon surrounded by oxide) to realize the DG-CNFET back-gate, thus guaranteeing individual addressing of each device back-gate (i.e. the back-gates are not shared). The final device is shown in figure 4-1.

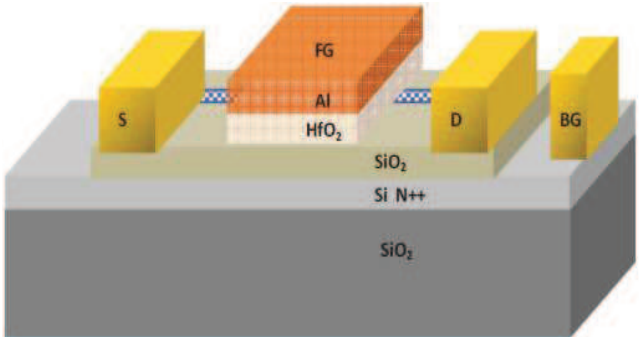


Figure 4-1. One front-gate and one back-gate DG-CNTFET: device cross-section [4-6]

The expected technology process is based on a practical and CMOS-compatible process flow. Starting with a SOI wafer, where the silicon-on-insulator layer will be used as back-gate, N^{++} doping (or NiSi salicidation) can be realized to ensure a good conductivity of the back electrodes. SiO_2 is subsequently deposited as back-gate oxide, and intrinsic carbon nanotubes are transferred on top of this. Then, the gate oxide (HfO_2) and the metal (Al) of the top gate are deposited and patterned,.Then, the active area and the back gate are defined by SiO_2 and Si etching respectively. Subsequently, the metal is sputtered onto the contacts to drain, source and both gates. The bulk terminal is not depicted because it is not used during normal operation. The bulk does not exist in the sense of MOSFETs since the CNT body is isolated from the Si substrate by means of a SiO_2 layer.

4.2.1.2 Process tuning

Once the device topology has been fixed, the final step to complete the process flow is to optimize the process materials such that symmetric operation is guaranteed. The meaning of symmetric operation is threefold. First, the I_{ON} current of the P- and N-type devices should be within the same range (10-20% difference). Second, the back gate voltage range, which has been reported in the literature to be from -2 to +2V, should be scaled down to $-V_{dd}$ to $+V_{dd}$ (with V_{dd} typically between 0.7 to 1V) in order to be compatible with the front gate voltage range. Third, the I_{OFF} current must be sufficiently low to control the leakage of the device. This optimization has been carried out by IMS by tuning the work function of the top and back gates. The gate materials (doped Si for the back gate and Al for the front gate); the gate oxides (SiO_2 for the back gate and HfO_2 for the front gate) and their thicknesses have thus been chosen in order to meet the conditions on the work function [4-6].

4.2.1.3 DG-CNTFET modeling

Practically, useful compact models have to describe the characteristics of a device as a function of bias, temperature, frequency, structure, and process variability in a computationally efficient, numerically stable, and accurate way. A useful compact model must allow the determination of parameters from measurements (or device simulations) at the device terminals. These stringent requirements can only be met by physics-based modeling strategies. Hence, an extensive literature survey ensures that it is possible to carry out accurate modeling for electrical simulation [4-7,4-8, 4-9, 4-10]. Many compact models [4-11, 4-12] have been developed to describe CNTFET technologies such as Schottky barrier (SB) CNTFETs or MOS-like CNTFETs with a top gate or surrounding gates. However, none of these are able to model a DG-CNTFET properly. A prior model presented in [4-4] is limited to thermionic transport without taking into account the coupling between the FG and BG and does not include SB (sub-band) modeling or BTBT (band-to-band tunneling).

Recently, a more accurate model has been presented in [4-13]. To the best of our knowledge; it represents the first physically accurate model of a DG-CNTFET with efficient convergence and simulation speed compatible with circuit design. This model has been developed by IMS in the context of the NANOGRAIN project. It considers a device described in three different regions: source access, inner part (underneath the front gate) and drain access. In this structure, four energy barriers appear in the device: at the metal to source (or drain) access junction, two SB-like barriers appear; while at the source (or drain) access to the inner part junction, the barrier is more conventional and is of a PN-junction shape. Depending on the work function difference between the metal contact and the CNT, carriers at the metal-CNT interface encounter different barrier heights, which determine the way in which carriers can reach the channel. Carriers with energies *above* the Schottky barrier height reach the channel by thermionic emission, while carriers with energies *below* the Schottky barrier height may reach the channel with probability determined by a transmission function describing the tunnel effect which can be calculated from the WKB (Wentzel–Kramers–Brillouin) approximation.

To overcome the complexity of the WKB expression for compact modeling, an approximation based on works from [4-14] is applied. This effective barrier height model is described in [4-13]. The electron (hole) current is calculated through the Landauer equation, by integrating over energy from the dominating barrier to infinity. The dominating barrier position depends on the applied bias. In fact, the electron current can be limited by three barriers: (i) the Schottky barrier from the source, (ii) the Schottky barrier from the drain and (iii) the conduction (valence) band of the inner part. The analytical expression of the drain current is given in [4-13]. In this model several other features are included. On the one hand, the band-to-band tunneling has been developed for MOSFET-like CNTFETs in [4-15] and has been validated through Non-Equilibrium Greens Function NEGF simulation. On the other hand,

charges have been modeled according to the ballistic assumption and the analytical expression of charge in each region is given in [4-16]. The potential calculation inside the device is given in [4-17]. Finally, it is worth noticing that the parasitic components have been taken into account in the model. The parasitic capacitances until metal 1 are extracted from 3-D TCAD simulation and subsequently implemented in the transistor model.

Furthermore, the comparison of the model with measurements from two technologies published in the literature (a DG-CNTFET from IBM [4-16] and a DG-CNTFET from Stanford University used as a MOS-like CNTFET [4-18]) showed the accuracy of the compact model in different technology configurations since the values of the extracted parameters are close to those measured.

4.2.1.4 PTM 16nm CMOS Model

To efficiently predict the characteristics of future bulk CMOS, a predictive modeling methodology was presented in [4-19]. It has an efficient better physicality and scalability over a wide range of process and design conditions. In the referenced work, both nominal values and process sensitivity values were captured for robust design research, and excellent accuracy was achieved according to published transistor data. The model also takes into account physical correlations among parameters as well as the impact of process variations. We chose the most advanced available model (16nm node) from [4-20], and we selected the PTM LP (Low Power) model file for low-power design applications in order to be as fair as possible for the comparison with circuits based on DG-CNTFET, since both models work with same power supply range (V_0=0V and V_{dd}=0.9V), unlike the PTM HP (High Performance) which works with 0.7V as V_{dd}. In fact, V_{dd} can be lower for HP since V_{th} is lower (leading to high ON-current). The LP model (with high V_{th}) that we use for comparison is therefore weak on speed and good on static power. So the results that we will find in the following evaluations should be tempered to some extent to the choice of the models. The CMOS model selected to be used is abbreviated CMOS-16nm along this chapter.

4.2.1.5 Devices model characterization and calibration

For a clear quantitative comparison between the DG-CNTFET based cells and the CMOS-based cells, it is necessary to calibrate the CMOS transistor width to match the ON-current performance of the DG-CNTFET (26µA-33µA) at V_{FGS}=V_{DS}=V_{dd}. Both types of transistor (P-type and N-type) are studied. Concerning the CMOS-16nm, we worked with a width of 56nm (i.e. W/L ratio of 3.5) for the N-type transistor and a width of 90 nm (i.e. W/L ratio of 5) for the P-type transistor. Table 4-1 shows the parameters used for the DG CNTFET compact model and the tuned W/L of the predictive model. As we explained in 4.2.1.2, the parameters of the DG-CNTFET model (the range of voltages, gates materials, oxide materials, layers

thickness, dimensions, number and diameter of nanotubes…) have been tuned by the IMS research team to match with the nanometric scale.

TABLE 4-1. PARAMETERS OF TRANSISTORS USED

Parameters	**DG CNTFET**	**PTM 16nm LP**
Inner channel	20nm	16nm
Width	50nm	56nm(N-type)/90nm(P-type)
Supply voltage	0.9 V	0.9 V
Drain access channel length	50nm	0nm
Source access channel length	50nm	0nm
Chirality (n,m)	(11, 0)	-
Nb of nanotubes	12	-
Diameter of 1 nanotube	0.861176 nm	-
Nanotube relative permittivity (ε)	5	-
Back gate capacitance	t_{ox}=8 nm ε= 15	-
Front gate capacitance	t_{ox}=2 nm ε= 3.9	t_{ox}=1.2 nm ε= 3.9

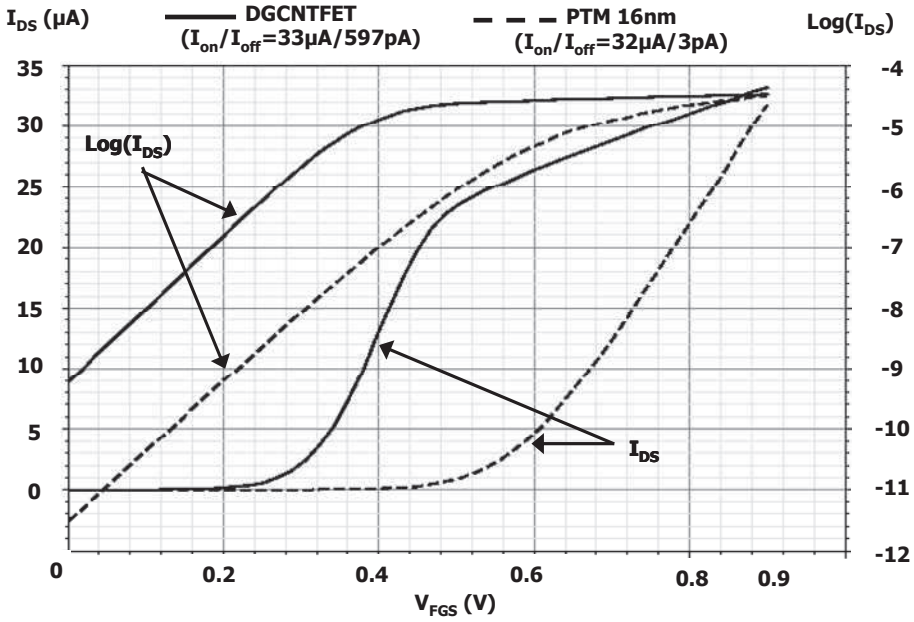


Figure 4-2. I_{DS}/V_{FGS} characteristics of the N-branch (V_{BG} -V_S = +V= +0. 9V)

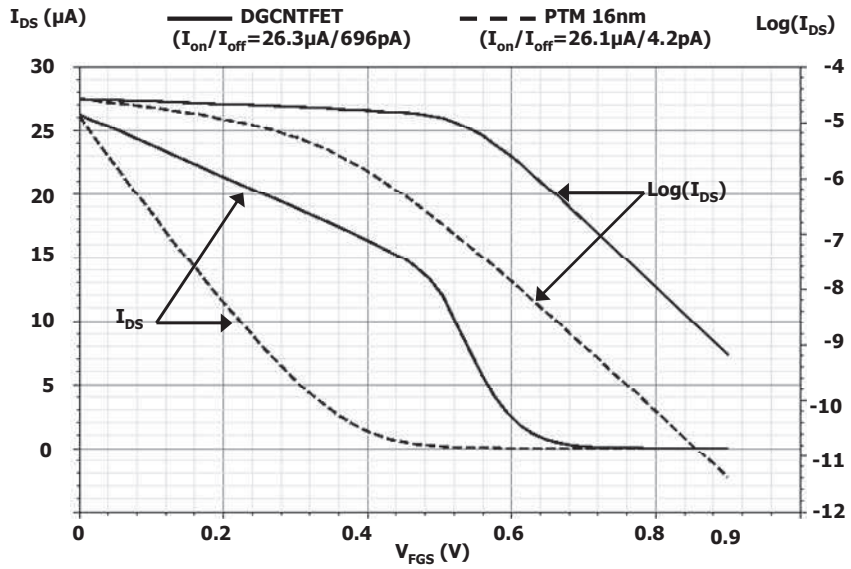


Figure 4-3. I_{DS}/V_{FGS} characteristics of the P-branch (V_{BG} -V_S = -V= - 0. 9V)

Figures 2 and 3 show the I_{DS}/V_{FGS} characteristics of the DG-CNTFET model and CMOS-16nm model, respectively for N-type and P-type configurations, where V_{FGS} varies between 0V and 0.9V, V_D=0.9V and V_S=0V. Compared to CMOS-16nm, the DG-CNTFET shows a high I_{OFF} current (~ 600pA vs. ~3pA) and a low threshold voltage V_{th} (~ 0.2V vs. ~0.4V). In fact, these two characteristics are related to ambipolar technology in general. The current through an ambipolar CNTFET is dominated by a tunnel current, unlike the drift-diffusion current in MOSFETs. Consequently, it has been observed that ambipolar devices with undoped channel have a V_{DS}-dependent I_{OFF} .This remark also holds for other ambipolar FETs with graphene nanoribbon or intrinsic SiNW channels. The drawback of this property is that I_{OFF} increases exponentially when V_{DS} increases, which may be a source of a high leakage. Using a smaller diameter (d) decreases the band gap, the V_{th} increases (V_{th}~0.45/d) and therefore the OFF current decreases. But at the same time, the ON current is decreased as well. This problem should be handled with care, because of course the ideal switch in most applications should demonstrate a high ON current, but also a very low OFF current. Furthermore, the selection of the suitable geometric parameters will probably remain a difficult problem to solve in the short term from a technology point of view.

In fact, figures 4-2 and 4-3, illustrating the I_{DS}/V_{FGS} characteristics of both model devices used for our simulations with an equal I_{ON}, explain clearly the better speed and the worse power consumption expected with the use of a DG-CNTFET device. This is mainly due to the lower threshold voltage (V_{th}) and the higher OFF current of the DG-CNTFET compared to CMOS-16nm. Power consumption (*P*) depends on the static leakage current $I_{leakage}$ which, in turn, depends on V_{th} $\{I_{leakage} \propto e^{-C \times Vth}\}$. *P* also depends on the short-circuit current expressed as $\{I_{SC} \propto (\beta.\tau_{in}/12.V_{DD}).(V_{DD}-2.V_{th})^3.f\}$. Performance is linked to I_{ds} which, in turn, is proportional to V_{th} $\{I_{ds} \propto (V_{DD}-V_{th})^{1\sim2}\}$. This high dependency between the transistor current and threshold voltage causes any improvement in speed to require an increase in dynamic

power, requiring low threshold voltage and high $I_{leakage}$, consequently augmenting the static power.

4.3 TTSM design approach : validation, evaluation and discussion

The principal goal of using the TTSM approach is to reduce transistor count in logic cells, with consequent expected impact on power consumption, area and delay. In this section, we compare the designed logic gates with their equivalent gates working with conventional CMOS-like logic, using the same DG-CNTFET device, and we extend the comparison to conventional CMOS logic built with CMOS-16nm technology. We discuss the results obtained from simulations and highlight the advantages of the design approach. Then we suggest layouts for several gates in both static and dynamic logic to show the flexibility of the method at the physical (layout) level.

4.3.1 Program of investigation and simulations results

We consider the same rise and fall times (20ps) for front and back gate inputs. We run SPECTRE simulations at a frequency of 1GHz with a fan-out-of-four (FO4) load. The supply voltage is 0.9V according to table 4-1 of device parameters, and clock and data inputs are single rail (i.e. +V=0.9V, V_0=0V). As previously mentioned, we used the parameters shown in table 4-1 for all transistors in the logic gates (i.e. W/L ratio of 2.5 for the DG-CNTFET, 3.5 for N-type CMOS transistors and 5 for P-type CMOS transistors). No resizing is carried out to balance branch resistances since this technique can be applied to all gates by using parallel transistors and has no impact from a comparative point of view. Various performance metrics are evaluated: power consumption “P”, time delay “TD”, the active area “Area” (i.e. sum of all channel areas W*L) and Power-Delay-Product “PDP”. Cyclic simulations are performed to establish mean power consumption and worst-case time delay figures over all data combinations.

4.3.1.1 Static logic gates

Our comparative study is carried out between:

- Conventional static logic structures (CMOS) built with CMOS-16nm devices.
- Conventional static logic structures (CSL) built with DG-CNTFET technology (Figure 2-4(a), chapter 2).
- Double gate static logic structures (DGSL) designed in this work by applying the TTSM approach (Figure 2-4(b), chapter 2).

To emphasize the benefit of the TTSM design approach, we simulated four different monotonic gates (XOR, XNOR, 2:1MUX, 4:1MUX) where the impact of the approach is

clearly observed since their structures contains many transistors in series. Results are shown in table 4-2. Figure 4-4 shows average values.

TABLE 4-2. COMPARISON OF STATIC LOGIC GATES: CMOS VS CSL VS DGSL

	P (µW)			TD (ps)			PDP (aJ)			Area (10^3. nm^2)		
	CMOS	CSL	DGSL	CMOS	CSL	DGSL	CMOS	CSL	DGSL	CMOS	CSL	DGSL
XOR2	1.3	2.3	2.5	40.0	21.0	16.0	52.0	48.3	40.0	8.7	8	4
XNOR2	1.4	2.3	2.5	36.7	21.0	16.0	51.4	48.3	40.0	9.3	8	4
MUX2:1	0.6	0.6	0.6	36.0	26.0	20.0	21.6	15.9	12.5	9.3	8	4
MUX4:1	1.2	1.7	1.9	91.0	40.0	30.0	109.2	68.0	57.0	21.8	20	12
Average	1.1	1.7	1.9	50.9	27.0	20.5	57.3	46.6	38.6	12.3	11	6

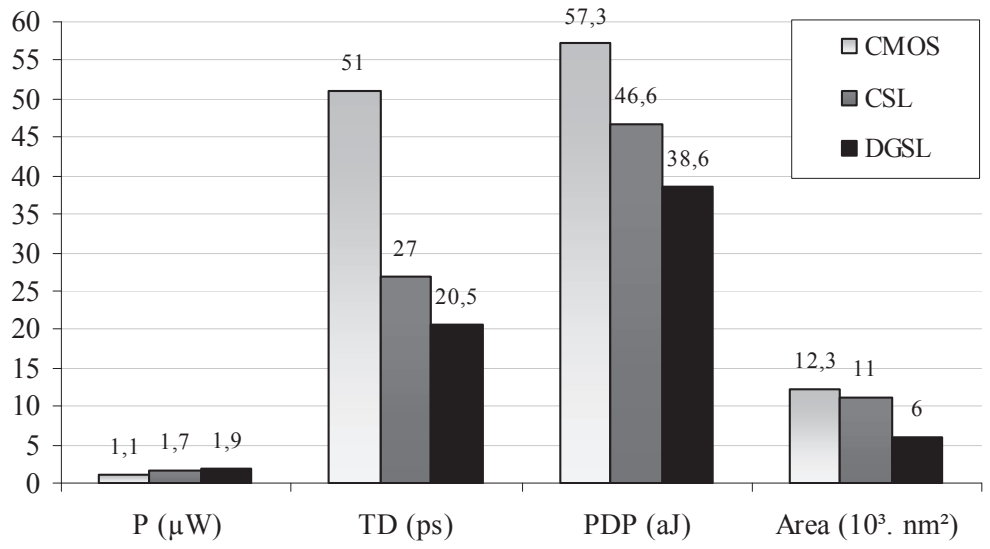


Figure 4-4. Static Logic Gates average values comparison: CMOS vs CSL vs DGSL

It is obvious that the TTSM approach efficiently decreases the number of transistors within a logic structure. Some gates such as the XOR2 or the MUX2:1 require only half the number of transistors usually needed for conventional static logic. Figure 4-4 shows the impact of the compact structures (DGSL) on the area which is decreased by nearly 45% compared to conventional structures (CSL). The gain in area attains 51% of improvement with static logic gates when compared to CMOS-16nm.

An increase of slightly more than 10% is observed with DGSL gates compared to CSL gates (1.9µW vs 1.7µW) with an improvement in delay of nearly 1.5X (20ps vs 27ps). Thanks to this decrease in time delay, the designed gates (DGSL) still achieve a better PDP (~20% of improvement) compared to CSL gates. Compared to CMOS gates, simulations show that the CNT technology offers an improvement of 32% concerning the PDP. These results are discussed further after the evaluation of dynamic logic gates in the section below.

4.3.1.2 Dynamic logic gates

Our comparative study is carried out between:

- Conventional dynamic logic structures (CMOS) built with CMOS-16nm technology
- Conventional dynamic logic structures (CDL) built with DG-CNTFET technology (Figure 2-7 (a), chapter 2).
- Double gate dynamic logic structures (DGDL) designed in this work by applying the TTSM approach, detailed in chapter 2.

Since the dynamic structures use only one clock signal, great attention must be given to the transition time (clock rise and fall times) which is a major factor in power consumption (short circuit current during the transition time). Furthermore it presents a risk of erroneous discharge of the output node through the function path. For this reason, we must ensure that input signals are stable before rising clock edges and also minimize as much as possible the clock rise and fall times. Figure 4-5 clearly shows the evolution of power consumption as a function of clock signal transition time in the case of a conventional dynamic logic inverter.

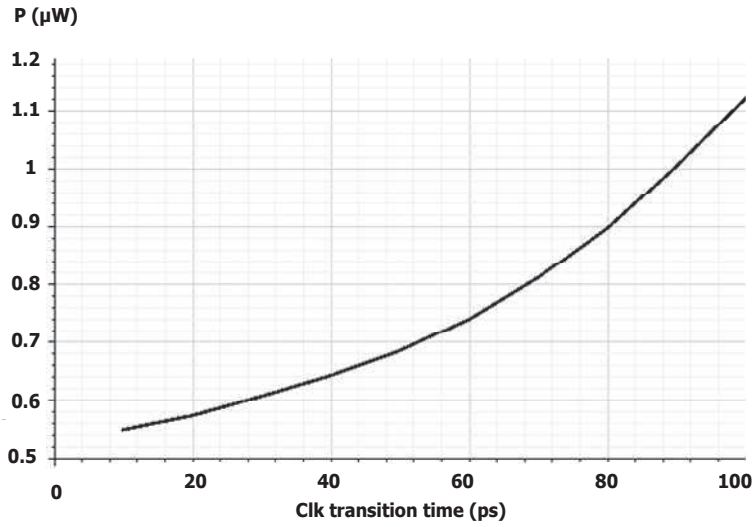


Figure 4-5. Evolution of the power consumption (P) as a function of clock transition time in the case of an inverter gate

Several gates (INV, NAND2, NAND3, NAND4, NOR2, XOR2, AOI …) have been simulated for the dynamic logic gates and the measured performance metrics are shown in table 4-3. Figure 4-6 shows the average values. We mention that to calculate the average value for DGDL gates, we chose the best value from all three scenarios (e.g. to evaluate the average value of DGDL gate time delay (TD), we choose the value for the NAND3 gate with scenario S3 since it is the scenario best fitted to this gate).

TABLE 4-3. COMPARISON OF DYNAMIC LOGIC GATES CMOS VS CDL VS DGDL

	P (µW)					TD (ps)					PDP (aJ)					Area (10^3. nm^2)				
	CMOS	CDL	DGDL			CMOS	CDL	DGDL			CMOS	CDL	DGDL			CMOS	CDL	DGDL		
			S1	S2	S3			S1	S2	S3			S1	S2	S3			S1	S2	S3
INV	0.3	0.5	-	0.7	-	23.0	13.0	-	10.0	-	6.9	6.5	-	7.1	-	3.1	3.0	-	2.0	-
NAND2	0.4	0.6	0.9	2.1	-	26.0	15.0	10.0	15	-	10.4	9.5	9.0	31.5	-	4.0	4.0	3.0	3.0	-
NOR2	1.1	2.0	-	2.7	-	23.0	13.0	-	10.0	-	25.3	25.4	-	27.0	-	4.0	4.0	-	3.0	-
AND2	1.4	2.8	-	3.2	-	24.0	13.0	-	10.0	-	33.6	36.4	-	32.0	-	4.0	4.0	-	3.0	-
OR2	0.7	1.3	1.5	3.9	-	26.0	15.0	10.0	14.0	-	18.2	19.8	15	62.4	-	4.0	4.0	3.0	3.0	-
AOI	1.0	2.0	2.1	4.1	-	27.0	18.3	11.0	13.0	-	27.0	36.6	23.1	65.6	-	4.9	5.0	4.0	4.0	-
XOR2	1.1	2.3	2.8	4.9	-	27.0	18.2	13.0	13.0	-	29.7	41.9	36.4	78.4	-	5.8	6.0	4.0	5.0	-
XNOR2	1.2	2.4	2.8	4.9	-	28.0	18.2	13.0	13.0	-	33.6	43.7	36.4	78.4	-	5.8	6.0	4.0	5.0	-
NAND3	0.4	0.5	0.8	1.9	0.8	36.0	20.0	14.0	17.0	11.0	15.1	10.0	11.2	32.3	6.9	4.9	5.0	4.0	4.0	3
NAND4	0.9	1.4	1.5	1.3	-	48.0	25.0	15.0	20.0	-	44.2	9.0	22.5	26	-	5.8	6.0	4.0	5.0	-
Average	0.9	1.5	1.7	3.0	0.8	28.8	16.9	12.4	12.8	11.0	24.4	23.9	21.1	44.1	6.9	4.6	4.7	3.7	3.7	3

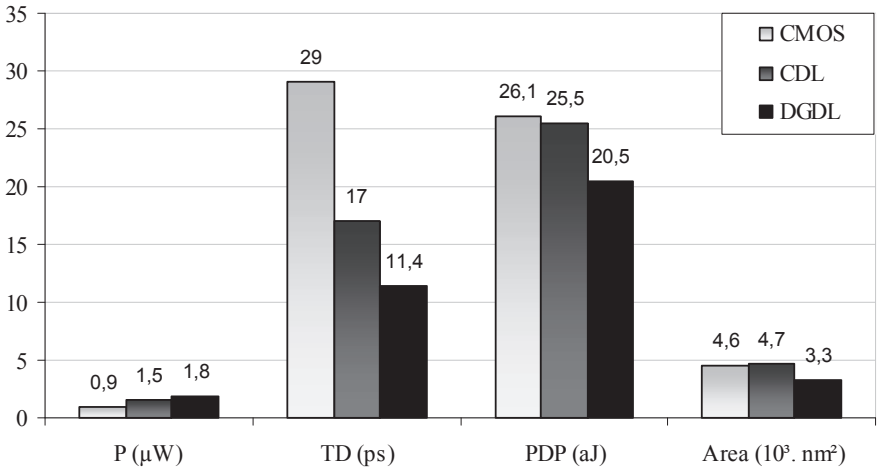


Figure 4-6. Dynamic Logic Gates average values comparison: CMOS vs CDL vs DGDL

With the designed dynamic logic gates (DGDL), the average gain in terms of area is 30% compared to conventional gates (CDL), (3300nm² vs 4700nm²). In the case of NAND3 it can attain 40% since a more compact structure is realized by applying the scenario S3 of the TTSM approach. However, the average power consumption with this approach increases slightly 20% (1.8µW vs 1.5µW). A delay improvement of nearly 1.5X is achieved compared to conventional logic (11ps vs 17ps, for DGDL and CDL respectively) which leads to a better PDP (~20% improvement). Compared with the CMOS technology, a decrease of 23% of the PDP is observed with the DGDL gates. These results are discussed in the next section.

4.3.2 Discussion

The principal benefit provided by the approach is the significant gain in terms of the number of transistors. For instance, while conventional static logic (CSL) generally requires *2n* transistors (where *n* represents fan-in), the designed static cells (DGSL) only require *2n-(m+p)* transistors (where *m* represents the number of NTTS structures and *p* represents the number of PTTS structures in conventional gates). As a result, and even though double-gate devices

require a greater footprint than single-gate devices, more compact logic gates are designed and less area is required. For dynamic and static logic styles, results showed a gain that can attain 45% in the case of static logic gates. In fact, the gain is higher with static logic gates than dynamic logic, since the TTSM approach is applied to both pull-up and pull-down networks, leading to fewer transistors compared to the original structure. Compared to CMOS gates, the improvement is not only due to the compactness of the structure but also because no resizing is needed for P-type transistors (P-type transistors are set via back gate).

Although fewer transistors are used, compared to conventional approaches, the average power consumption is increased by slightly more than 10% and 20% in the case of static logic gates and dynamic logic gates, respectively. This increase in power consumption is due to the shorter path from V_{dd} to ground that the new structures create. Since there are fewer transistors in series, the resistance per branch from (V_{dd}/G_{nd}) to output decreases to the channel resistance of a single transistor (R_{ch}) and results in a consequently higher short-circuit current during signal transition time ,whereas in the conventional structure, two transistors in series offer a path resistance of $2R_{ch}$. However this increase in current per transistor is not expected to be a reliability issue, since I_{ON} in CNTFETs can attain a value 20–30X higher than that of state-of-the-art Si MOSFETs [4-21]. Nevertheless, with fewer transistors in series comes a reduced equivalent channel resistance and associated time constant with load capacitance accordingly. This explains the improvement of delays (1.5X) and the PDP (~20%) reported by results.

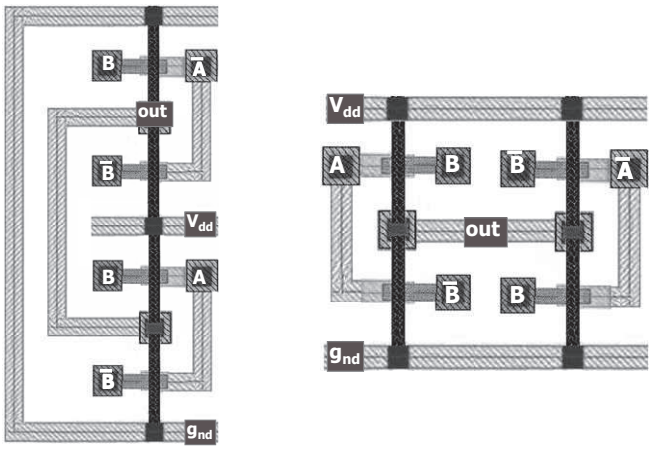
In this study, we also compare the power consumption and time delay of the DG-CNTFET logic gates to that of conventional CMOS-16nm. Simulations show that CNT technology offers an improvement of 2.5X concerning the time delay with an increase of power consumption of almost 2X over CMOS-16nm technology. However, the PDP of gates built with the CNT technology remain better than their CMOS counterparts. By applying the approach presented in this work, we achieve an improvement of 32% and 23% for the static logic and the dynamic logic gates, respectively, when compared to CMOS technology.

In this section, we evaluated and analyzed the performance metrics of the designed cells using the TTSM design approach presented in chapter 2. The main advantages highlighted were the decreased area thanks to the compactness of logic structures and the improved PDP with a decreased time delay. In the next section, we propose some layouts to bring to light the regularity of logic structures built with DG-CNTFET technology.

4.3.3 Layouts

We now consider how to exploit the regularity and symmetry of the circuit structures obtained from the generic design approach. This is in line with future nanotechnology manufacturing contingencies such as the regularity criteria highly required by nano-device fabrics and imposed by the chemical self-assembly process used for aligning CNTs or NWs in parallel rows.

We use arbitrary design rules and exploit the approach of building a complementary logic circuit along the length of a single nanotube. In a system architecture, a single CNT could span several logic cells and thus considerably simplify fabrication issues by requiring a reduced number of individual CNTs. In addition, when the CNT pitch is significantly less than metal track dimensions, a discretized design approach may also be applied to build a CNT planar array for each device [4-22]. This can be used both as an approach to increase I_{ON} without increasing footprint, and as a method to improve reliability. Figure 4-7(a) shows one layout of the XOR gate. This layout exploits the approach of building a complementary logic circuit along the length of a single nanotube. In figure 4-7(b), we propose a second layout of the XOR gate using two nanotubes to show the possibility of direct transposition of the schematic view at the layout level.

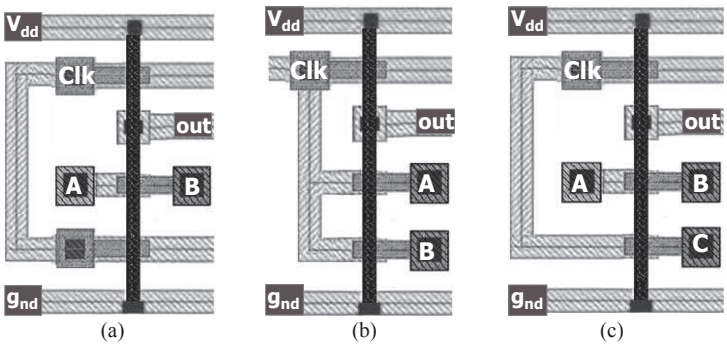


(a) (b)

Figure 4-7. Layout of DGSL XOR gate: single nanotube (a) double nanotubes (b)

As with any standard cell approach, the layout must be normalized to a set *y*-dimension, in order to place cells in rows. The inverted function (i.e. the XNOR function in this case) can be achieved by simply flipping the layout.

Figures 4-8(a) and 4-8(b) propose the layouts of the NAND2 gate built with 2 different scenarios (S1 and S2) respectively. Although the same number of transistors is required, the S2 layout seems to be simpler. In figure 4-8(c), we present the NAND3 layout according to S3, which has almost the same layout of S1-NAND2 despite the extra input.



(a) (b) (c)

Figure 4-8. Layouts of DGDL gates (a) S1-NAND2 (b) S2-NAND2 (c) S3-NAND3

4.3.4 Achievements

We have evaluated the TTSM approach described in chapter 2, which specifically exploits the ambipolar property of Am-IDGFETs to reduce efficiently the transistor count for logic cells in different logic styles, leading to a greater integration density by replacing all two identical-type transistors in series structures with a single Am-IDGFET for equivalent functionality. The TTSM approach proved that an area gain of 51% could be achieved by some static gates. In the case of the dynamic logic style, we showed how the TTSM approach can be applied according to three different scenarios depending on the number of transistors and their repartition in the gate branches with an area gain of nearly 30%. For both logic families, we validated via simulation a set of gates by using the most advanced models available in the community for the DG-CNTFET technology and the CMOS-16nm technology to evaluate the benefits of the obtained compact circuits concerning power consumption and delay. Despite the increase in power consumption observed with the designed gates, we still obtain a 30% improvement in PDP thanks to the time delay decrease (2.5X). Finally, we illustrated the flexibility brought by the DG-CNTFET structures at the layout level thanks to their regularity and symmetry, which responds to some nanotechnology manufacturing contingencies usually required by nano-devices based on nanowires or carbon nanotubes.

4.4 Low-power design technique : validation, evaluation and discussion

In the same context of standard logic cells, we described in the second part of chapter 2 a design technique which exploits the back-gate of Am-IDGFETs to dynamically decrease the short-circuit power and the static power in logic gates. In addition, we proposed a control module, which enables the switching between the active mode and the standby mode to feed the back-gates of transistors with the appropriate signals. In this chapter, we compare the clocked logic gates based on this technique (abbreviated as "Clk") with their equivalent gates based on conventional CMOS-type logic (abbreviated as "Cnv") using the same Am-IDGFET device (DG-CNTFET in this case). Also, we extend the comparison to CMOS logic built with silicon technology (abbreviated as CMOS). Furthermore, we estimated the power consumption of the module for various values of the resistance R of the T-inverter within the module and assess its impact on logic gates.

4.4.1 Simulations and results

The same DG-CNTFET and CMOS-16 nm device models, presented at the beginning of this chapter, are used. First, we start by characterizing the control module and justify the choice of the value of the resistance R of the T-inverter. Then, we proceed to the characterization and comparison of logic gates.

4.4.1.1 Control module evaluation

The control module was described in chapter 2 as a 2:1 multiplexer with a T-inverter at the output. The choice of the resistance value R, which is a part of the T-inverter, is expected to have a direct impact on the power consumption of the whole module. Furthermore, it is necessary to determine the suitable value of R which enables the T-inverter to switch properly between the three values (+V, +V/2, 0V). To determine the range of R, we run a DC analysis on the T-inverter, as shown in figure 4-9. From this figure, a suitable value for R can be in the range of [50KΩ, 500KΩ]. Once the range of the R value is found, we simulated the transient behaviour of the output of the T-inverter when conducting Clk_P as shown in figure 4-10. The input (V_{In}) of the T-inverter corresponds to the signal Clk_P and its output corresponds to Clk_N, as previously explained in figures 2-22 in chapter 2. We ran Spectre simulations with a frequency of 500MHz and equal rise and fall times (40ps) for the clock signal (Clk_P) and with voltages (0V, 0.45V) and output load of FO4. We estimated the power consumption (P) of the module for different values of R within this range. This is illustrated in figure 4-11, representing the evolution of the power consumption and the delay of the module as a function of the resistance R.

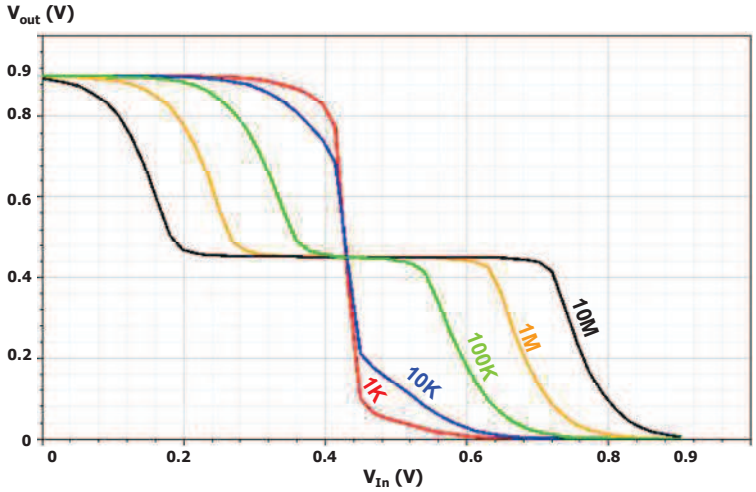


Figure 4-9. V_{out}/V_{In} of the T-inverter as a function of R

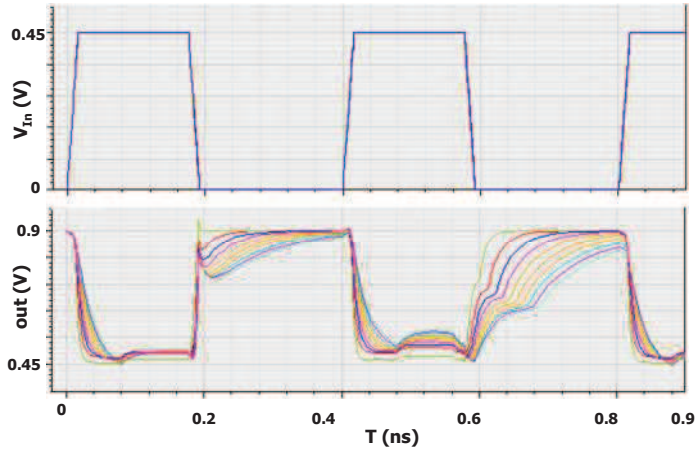


Figure 4-10. T-inverter output as a function of R [50KΩ - 500KΩ]

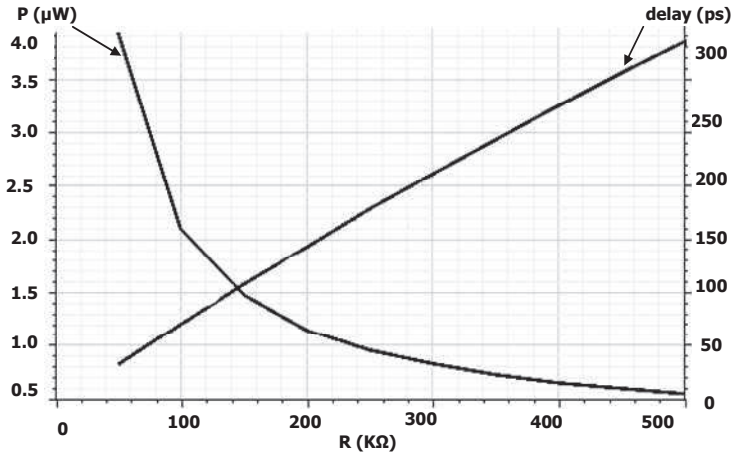


Figure 4-11. Power consumption and delay of the module as a function of the T-inverter resistance (R)

Figure 4-11 shows the total power consumption and delay of the module as a function of R. We propose to choose R in the range of [200KΩ, 300KΩ], where the power consumption of the module is decreased to have almost the same value of a conventional inverter with DG-CNTFET (~0.9µW), as demonstrated further in the next section. In fact, in spite of the notable increase of the delay as a function of R (figure 4-11), this has negligible impact on the power

consumption of logic gates. Indeed, the T-inverter output , i.e. Clk_N, is connected only to the N-type network transistors, while Clk_P is connected to the P-type network transistors directly, without going through the inverter. So the P-type network will be switched OFF, and no short-circuit current will be observed between V_{dd} and ground, even when the N-type network is not completely off because of the T-inverter delay. To sum up with the control module characterization, we chose the value of 250kΩ for the T-inverter which shows an equivalent power consumption of a conventional DG-CNTFET inverter. The next step is to estimate the power consumption of logic gates.

4.4.1.2 Low-power logic gate evaluation

The main goal of the low-power technique is to lower the short-circuit power and the static power. Hence, to evaluate the short-circuit power, we initially run our simulations without any output load. Then, we rerun simulations with an output load of FO4 to evaluate the total power consumption in the presence of output load.

Simulations are carried out with a frequency of 500 MHz and equal rise and fall times (200ps) for the input data A and B and equal rise and fall times (40ps) for clock signals Clk_P and Clk_N with voltages (0V, 0.45V) and (0.9V, 0.45V) respectively. These are the same clock parameters used in the previous section to characterize the control module. The pulse width of clocks was 2X the switching time "ST" of the input A as explained in figure 2-19, chapter 2. The supply voltage was single rail (i.e. +V=0.9V, V_0=0V). Cyclic simulations are performed to establish mean power consumption over all data combinations. Table 4-4 shows the short-circuit power (P_{SC}), the total power (P_{TOT}) with FO4 load and static power (P_{STAT}). Average values are illustrated in figure 4-12.

TABLE 4-4. POWER CONSUMPTION COMPARISON

	P_{SC} (nW)			**P_{TOT} (nW)**			**P_{STAT} (pW)**		
	CMOS	Cnv	Clk	CMOS	Cnv	Clk	CMOS	Cnv	Clk
INV	60	700	116	340	900	400	81	630	6
NAND2	40	380	124	200	530	290	92	632	6.5
NOR2	80	620	112	270	860	290	45	480	5.6
XOR2	300	1800	600	600	2100	760	500	1467	15.6
Average	120	880	240	350	1100	440	180	802	8.4

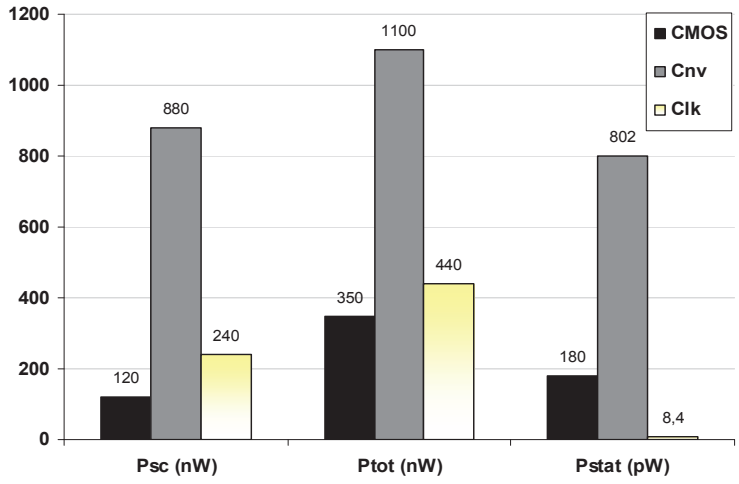


Figure 4-12. Average values of power consumption

Compared with Cnv-gates, the Clk-gates show an average improvement of 3.7X for the short-circuit power consumption. In the case of some gates, such as the inverter, the gain exceeds 6X. Despite this remarkable improvement, the short-circuit power consumption is still 2X higher than CMOS gates. This is mainly due to the lower threshold voltage (V_{th}) of DG-CNTFETs compared to CMOS-16nm. In fact, P_{SC} depends on the short-circuit current which, in turn, relies on V_{th} according to the cubic relation $\{ I_{SC} \propto (\beta.\tau_{in}/12.V_{DD}).(V_{DD}- 2.V_{th})^3.f \}$. The V_{th} of the DG-CNTFET is 2X smaller than that of CMOS-16nm technology. As a result, DG-CNTFET gates show increased power consumption compared to their CMOS counterparts for both P_{SC} and P_{TOT}.

Concerning the static power consumption, Cnv-gates consume over 4X more compared to CMOS technology and this figure exceeds 10X in the case of NOR2. The high leakage is the result of high I_{OFF} current characteristic of DG-CNTFETs and undoped ambipolar devices in general (as explained in section 4.2.1.5). However, by inverting back gate voltages during the standby mode, the I_{OFF} is improved by 100X and consequently leads to a *decrease* in static power by a factor of 100X. Compared to CMOS technology, a gain of 22X is thus achieved. This represents an attractive solution to address the leakage issue of undoped ambipolar devices at the design level.

4.4.2 Achievements

We have evaluated the low-power design technique described in chapter 2. The approach consists of switching off all transistors via their back gates during the switching time to lower the short-circuit power. Simulations results show an improvement of 4X in terms of short-circuit power as compared to conventional gates. Also, the total power consumption has been improved by a factor of 3X. By inverting the back gate voltages of transistors, the I_{OFF} current is decreased by a factor of 100X leading to the decrease of static power with the same magnitude. By analyzing the control module, which enables switching between the active

mode and the standby mode, we showed that a proper choice of the value of R can minimize the power consumption penalty. Thus, the low-power design technique described in chapter 2 has proved to be an efficient way to tackle the problem of power consumption related to Am-IDGFETs.

4.5 Reconfigurable logic cells from classes of functions and AmBDDs : validation, evaluation and discussion

The previous sections dealt with the evaluation of design approaches in the context of standard logic gates as presented in chapter 2. In this section, we validate and evaluate the design methodologies presented in chapter 3 to design reconfigurable logic with Am-IDGFETs.

The first synthesis technique to generate reconfigurable logic was founded on the concept of ***Boolean Function Classification***. Several cells were designed according to a dynamic logic style with full functionality or partial functionality and various structures were proposed with two cascaded logic stages or with a single logic stage. Then, a complementary static logic cell was derived. The second reconfigurable logic synthesis technique relies on the concept of ***Am-BDDs*** with adaptation of some design rules to fit with the switching paradigm of Am-IDGFETs. Three cells were designed according to a static logic style based on pass-transistor logic networks with full functionality or partial functionality.

We aim to validate the behaviour of each cell through simulations and estimate its power consumption and delays based on the DG-CNTFET model described earlier in the beginning of the chapter. Cells are compared between each other, as well as with conventional CMOS-16nm technology. We discuss the results obtained from simulations and highlight the advantages of the reconfigurable cells obtained from both proposed design approaches.

4.5.1 Performance metric evaluation and discussions

Our study concerns reconfigurable circuits built with the dynamic and static logic styles. To make the evaluation and comparisons as fair as possible, we characterize and compare dynamic cells and static cells separately. We start by presenting various *dynamic* cells, the corresponding CMOS benchmark and the simulation results of the main performance metrics. We subsequently tackle *static* logic cells in the same way. Finally, we discuss the results obtained with the whole set of reconfigurable cells designed in this work.

We run SPECTRE simulations with a frequency f=250MHz and equal rise and fall times (40ps) for input signals (A, B) with an output load of FO4. The supply voltage is 0.9V and data inputs are single rail (i.e. +V=0.9V, V_0=0V). For the dynamic logic cells, the same conditions are kept and we use non-overlapping clock signals with equal rise and fall times (10ps). Cyclic simulations are carried out to establish mean power consumption and worst-case time delay over all data combinations.

4.5.1.1 Dynamic Logic Reconfigurable Cells

In this section, we aim to evaluate the three dynamic logic cells designed in chapter 3:

- DRLC-7T is a partial-functionality cell composed of two stages and achieves 14 functions (Figure 3-7, chapter 3);
- SOP-DRLC is a full-functionality cell composed of 2 stages and realizes 16 functions (Figure 3-5, chapter 3);
- SS-DRLC is a single stage cell which achieves 15 functions (Figure 3-8, chapter 3).

The CMOS benchmark is a multiplexer with four data inputs and one data output. It is built according to a dynamic-logic style with the same structure used with the CNT technology cells (i.e. 2 non-overlapping clocks, pull-up function path block). The reconfigurability of this cell is achieved by swapping between different combinations of the 4 data inputs (D_1, D_2, D_3, and D_4) in the same way as the operating principle of a Look Up Table (LUT). The transistor level implementation of the MUX is shown in figure 4-13. It is abbreviated as DL-MUX 4:1. Figure 4-14 illustrates the difference between cells in terms of active area (AREA = sum of all channel areas W*L), number of achieved functions, number of configuration signals and number of stages used by each cell.

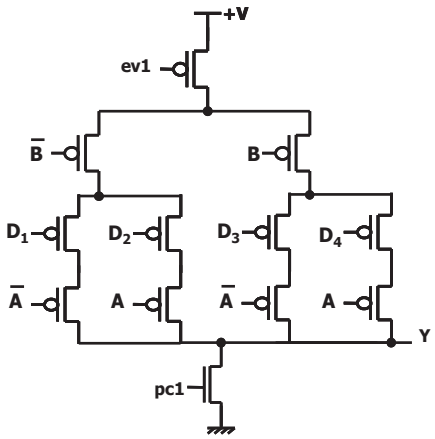


Figure 4-13. Dynamic logic multiplexer (DL-MUX 4:1)

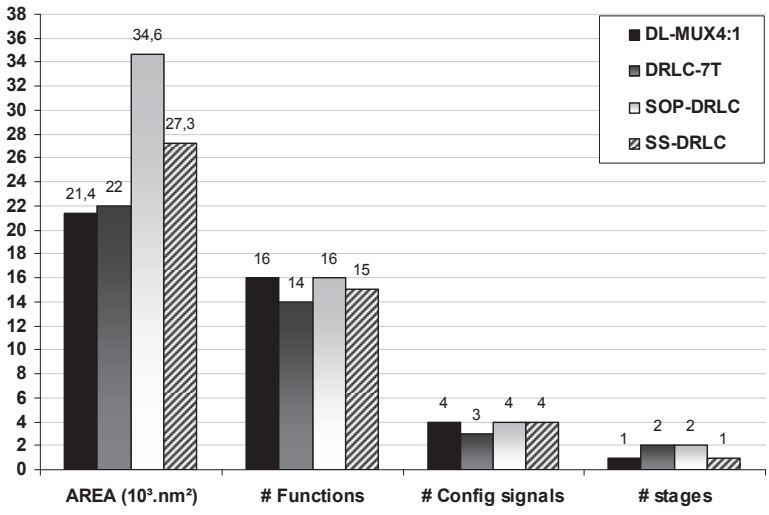


Figure 4-14. Comparison of area, numbers of functions, configuration signals and logic stages used by dynamic logic cells

To emphasize the characteristics of the proposed dynamic logic cells, for every function we estimated: i) power consumption *"P"*, ii) time delay *"TD1"* for the first stage, iii) time delay *"TD2"* for the second stage (since DRLC-7T and SOP-DRLC are composed of two logic stages) and iv) minimum latency "*Lat"* (since cells are implemented in the dynamic logic style). To make clear the evaluation of delays and latency times, we define below these two metrics:

- The time delay is defined, for each logic stage, as the interval of time between the instant corresponding to the beginning of the evaluation period (time at which the signal ev=$V_{dd}/2$) and the instant corresponding to the evaluation of the output (time at which the signal Y = $V_{dd}/2$).

- The minimum latency measures the time of signal propagation in the entire circuit from the first pre-charge operation (time at which the signal pc1=$V_{dd}/2$) until the output is established (time at which the signal Y=$V_{dd}/2$). This obviously depends on the depth of the logic circuit (the number of logic stages).

The four reconfigurable dynamic cells simulated are (DRLC-7T, SOP-DRLC, SS-DRLC, and DL-MUX 4:1). The results for each function are shown in table 4-5 and the average values are illustrated in figure 4-15.

TABLE 4-5. COMPARISON OF RECONFIGURABLE DYNAMIC LOGIC CELLS

	P (nW)				**TD1 (ps)**				**TD2 (ps)**			
F	DL-MUX4:1	DRLC-7T	SOP-DRLC	SS-DRLC	DL-MUX4:1	DRLC-7T	SOP-DRLC	SS-DRLC	DL-MUX4:1	DRLC-7T	SOP-DRLC	SS-DRLC
$\overline{A+B}$	320	2420	1700	1000	222	67	55	150	-	23	23	-
$A+B$	600	2070	1130	2000	241	68	55	76	-	23	23	-
$\overline{A}+B$	600	1870	1250	1960	240	68	109	113	-	24	24	-
$\overline{B}+A$	600	1870	1130	2000	245	68	82	113	-	23	23	-
$\overline{A} \bullet B$	330	2120	1100	700	222	48	82	100	-	23	23	-
$\overline{B} \bullet A$	320	2120	1260	900	235	48	109	135	-	23	24	-
$A \bullet B$	310	2100	1700	1100	229	35	125	151	-	23	24	-
$\overline{A \bullet B}$	600	1800	1120	1800	245	35	125	75	-	23	23	-
$\overline{B}$	430	1600	1960	1350	242	67	135	76	-	23	23	-
B	430	1700	2120	1360	237	67	135	150	-	23	24	-
A	460	1560	2000	1350	238	68	124	76	-	23	24	-
$\overline{A}$	470	1550	1920	1350	224	68	124	151	-	23	24	-
$\perp$	170	1300	1200	200	-	-	-	-	-	-	-	-
T	700	200	200	-	-	-	-	-	-	-	-	-
$\overline{A \oplus B}$	460	-	2140	1400	233	-	124	113	-	-	23	-
$A \oplus B$	490	-	1010	1360	238	-	124	135	-	-	22	-
Average	456	1734	1434	1322	235	59	108	115	0	23	23	0

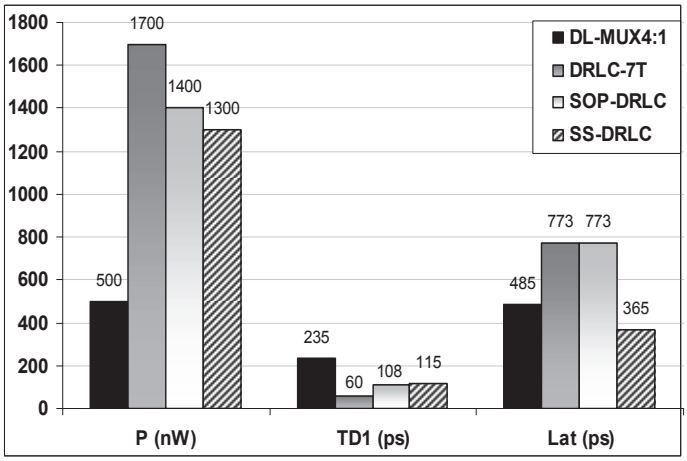


Figure 4-15. Comparison of average performance metric values of reconfigurable dynamic logic cells

Based on figure 4-15, the SS-DRLC cell offers the minimum power consumption compared to the other DG-CNTFET reconfigurable cells. Also, it is a single-stage structure which has a direct impact on time delay and latency compared to other two-stage cells (DRLC-7T and SOP-DRLC). In addition, it requires fewer clock signals (only 2 instead of 4), and fewer transistors (compared to SOP-DRLC) leading to better compactness with the same number of control signals and an increased number of functions over the DRLC-7T. The shortcoming of this cell is the inability to fulfill the function "1". The main benefit of the SOP-DRLC cell compared to other dynamic cells is the full functionality (16 functions achieved). For comparable power consumption and equal latency, this uses only 2 additional transmission gates (TI) and 1 more control signal over the DRLC-7T, part of the cost of achieving the complete set of 16 functions instead of only 14 realized by DRLC-7T. Thus, it seems that the SS-DRLC cell gives the best design trade-off compared to the reconfigurable dynamic cells presented in this work.

Compared with CMOS-16nm, DG-CNTFET reconfigurable cells are power-hungry (2X-3X increase). However, CNT technology demonstrates a decreased time delay compared to CMOS (2X-4X) with worse latency in the case of double-stage cells. Concerning the area, as shown in figure 4-14, the DRLC-7T cell shows almost the same area required by DL-MUX 4:1 based on CMOS-16nm transistors. It also uses only three configuration signals instead of four. However, it is still a partial functionality cell without access to XOR/XNOR functions. For other cells at least an increase of 30% is observed. The origins of the advantages and disadvantages of DG-CNTFET reconfigurable cells are discussed after the evaluation of static logic cells below.

4.5.1.2 Static Logic Reconfigurable Cells

Four reconfigurable static logic cells were designed in chapter 3 of this work; the first designed cell (CSL-DRLC) was obtained from the function classification approach, while three other cells (16F-AmBDD, 12F-AmBDD, and 6F-AmBDD) were obtained from the AmBDD approach. In this section, the whole set of static logic cells are compared with two CMOS-

based multiplexers used as reconfigurable logic cells. The first MUX 4:1 is a complementary static logic circuit with four data inputs and one data output, and is abbreviated as “CSL-MUX 4:1” (Fig. 4-16). The second MUX is also designed with a static logic style, but uses transmission gates (pass transistor logic), and is abbreviated as "TG-MUX 4:1" (Fig. 4-17).

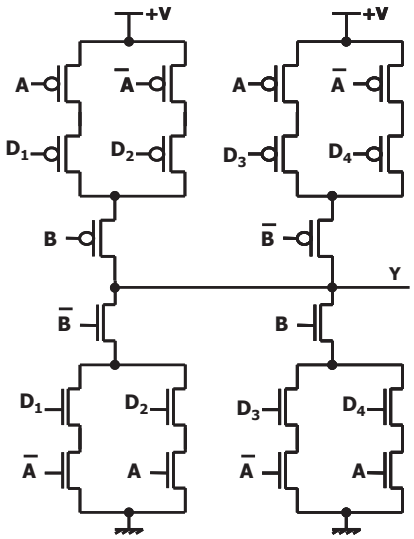


Figure 4-16. Complementary Static Logic multiplexer (CSL-MUX 4:1)

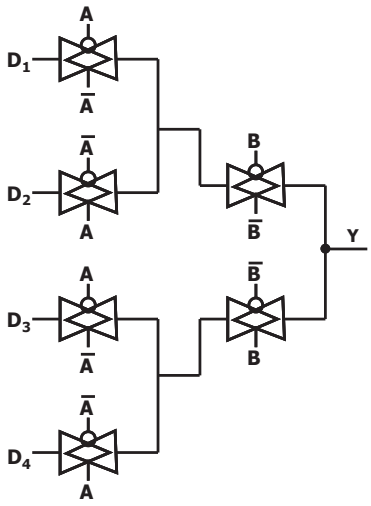


Figure 4-17. Transmission Gate Static Logic multiplexer(TG-MUX 4:1)

Area, number of configuration signals and achieved functions are shown in figure 4-18. The results for every function, in terms of Power (P), Delay (TD) and Power-Delay-Product (PDP), are presented in table 4-6 while average values are illustrated in figure 4-19.

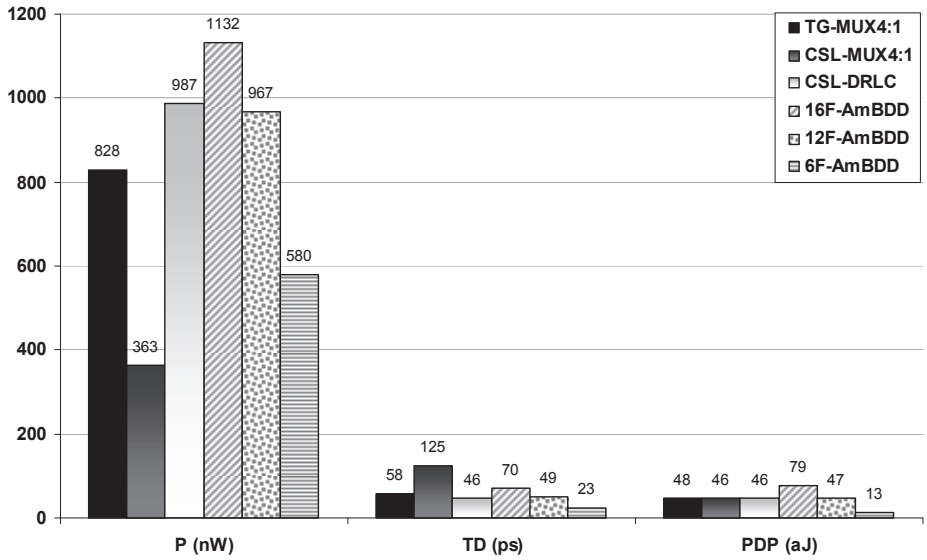


Figure 4-18. Average values comparison of reconfigurable static logic cells

TABLE 4-6. COMPARISON OF RECONFIGURABLE STATIC LOGIC CELLS

Function	P (nW)						TD (ps)						PDP (aJ)					
	TG-MUX4:1	CSL-MUX4:1	CSL-DRLC	16F-AmBDD	12F-AmBDD	6F-AmBDD	TG-MUX4:1	CSL-MUX4:1	CSL-DRLC	16F-AmBDD	12F-AmBDD	6F-AmBDD	TG-MUX4:1	CSL-MUX4:1	CSL-DRLC	16F-AmBDD	12F-AmBDD	6F-AmBDD
$\overline{A+B}$	800	360	860	1000	800	600	63	100	25	55	35	30	50	36	22	55	28	18
$A+B$	800	400	1100	1270	1000	*	57	156	60	86	67	*	46	62	66	109	67	*
$\overline{A}+B$	820	360	1070	1220	960	*	46	89	34	100	79	*	38	32	36	122	76	*
$\overline{B}+A$	890	370	850	1000	820	570	63	89	39	55	35	31	56	33	33	55	29	18
$\overline{A} \bullet B$	810	370	940	1200	970	*	47	132	28	86	67	*	38	49	26	103	65	*
$\overline{B} \bullet A$	800	360	1000	1130	900	630	75	157	28	42	30	24	60	57	28	47	27	15
$A \bullet B$	770	380	1060	1230	1000	*	46	128	30	100	79	*	35	49	32	123	79	*
$\overline{A \bullet B}$	830	300	840	1130	900	620	75	132	32	23	16	26	62	40	27	26	14	16
$\overline{B}$	710	320	700	1000	*	*	63	89	27	96	*	*	45	28	19	96	*	*
B	700	350	900	1230	*	*	47	111	72	100	*	*	33	39	65	123	*	*
A	860	400	900	1100	830	560	57	158	72	25	19	16	49	63	65	28	16	9
$\overline{A}$	910	400	700	960	740	500	75	132	26	22	15	11	68	53	18	21	11	6
$\overline{A \oplus B}$	1100	600	1500	1740	1300	*	57	128	95	100	78	*	63	77	143	174	101	*
$A \oplus B$	1100	600	1400	1800	1380	*	46	155	81	85	67	*	51	93	113	153	92	*
$\perp$	800	140	*	500	*	*	*	*	*	*	*	*	*	*	*	*	*	*
T	540	100	*	600	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Average	828	363	987	1132	967	580	58	125	46	70	49	23	48	46	46	79	47	13

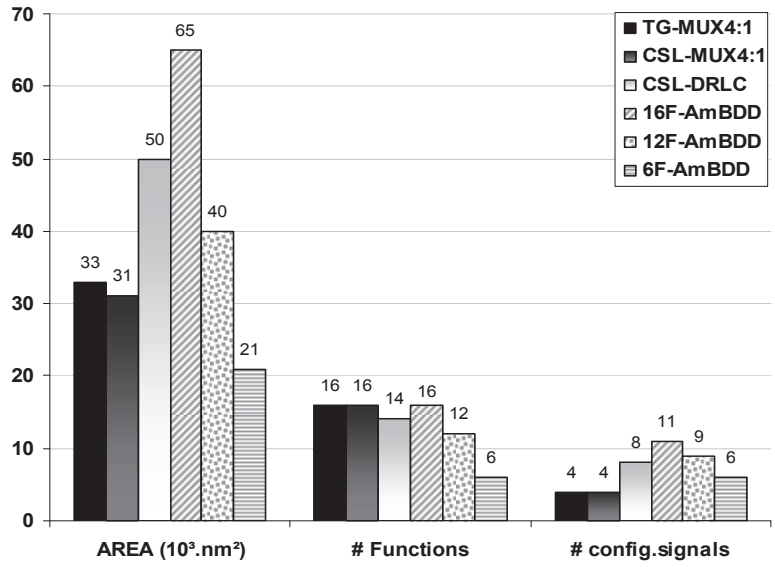


Figure 4-19. Comparison of number of functions and configurations signals of static logic cells

The CSL-DRLC cell, obtained from the function classification approach, demonstrates a PDP similar to that of conventional CMOS-16nm reconfigurable static logic. The main weakness of this cell is the doubled number of configuration points and the two missing functions ("0" and "1"). Also, an increase of 34% in area was observed with this cell. Concerning static cells generated from AmBDDs, the logic circuit required to realize the whole set of 16 functions (16F-AmBDD) shows the highest power consumption. Although the time delay is still smaller than CSL-MUX4:1, its PDP is almost 2X higher than other logic cells. Also, a high number of configuration signals is required, as well as a doubled area. In the case of partial functionality cells (12F-AmBDD and 6F-AmBDD), more interesting results are obtained. With the 6F-AmBDD cell, the PDP is at least 3X better than other cells and a 38% decrease in area can be observed, as compared to CMOS-16nm technology. Thus, the cell is very compact and offers fast logic. Although it does not achieve the whole set of 16 logic functions, the basic functions (INV, NAND, NOR) are still accessible with this cell.

4.5.2 Discussion

The DG-CNTFET cells (dynamic and static) show power consumption figures 1.5X-3X higher than their CMOS counterparts. This is due to two main reasons:

- The first reason is related to the DG-CNTFET device itself, and is the direct consequence of its low threshold voltage (V_{th}) with high I_{OFF} compared to CMOS-16nm. Both short-circuit power and static power consumption are therefore increased. While it is generally expected that better I_{OFF} can be obtained with double gate structures, this was not the case with the DG-CNTFET device used for the evaluation of circuits in this dissertation. A high I_{ON} and sharp I-V subthreshold slope have been observed, but the current in the off state is critical to maintain a low passive power and a reasonable I_{ON}/I_{OFF} ratio ($\geq 10^4$ is typically desirable in logic applications). However, the physics that leads to efficient gate switching (e.g. thinner

gate insulators) and high on-currents in small bandgap CNTs also tends to increase the off-current. Hence, careful engineering (materials, thickness, CNT diameter …) must be considered for the fabrication of CNTFETs and a lot of work is still required to make CNT technology more mature.

- The second reason for the increased power consumption is the high number of transistors and inverters required by using transmission gates instead of single transistors (the Am-IDGFET-transmission gate requires two transistors in parallel and two inverters). Also, the use of transmission gates dramatically increases the area (≥30%), especially if we aim to achieve full-functionality cells. In spite of its negative impact on power and area, the use of transmission gates does allow logic signals to be kept clean (full logic swing). Coupled with the low V_{th} of DG-CNTFETs, the designed reconfigurable cells show an improved time delay by a factor of 3X-4X compared with CMOS technology. A trade-off between these benefits and disadvantages of the designed cells seems to be the choice of partial-functionality cells such as the case of 6F-AmBDD cell which shows 3X better PDP and 38% less area. The reduced number of functions can be compensated at an architectural level, as proved in some publications [4-23, 4-24, 4-25], where – for instance – a partial-functionality cell can be used as a Block Logic Element (BLE), in the context of FPGA architectures.

4.5.3 Achievements

Since both logic styles (dynamic and static) are employed to design reconfigurable logic cells, we chose to compare the generated cells with their CMOS-16nm counterparts operating with the same logic style and having the same implementation structure. 4:1 multiplexers were used as benchmarks since they present the conventional CMOS reconfigurable structures for many digital systems. The use of transmission gates instead of a single transistor in the case of CNT technology was necessary to ensure correct logic behaviour (no logic degradation, compatible voltage values and correct operation of the overall circuit). However, this proved to be a mixed blessing, since an increase of 2X-3X in power consumption was observed as compared to CMOS-16nm, due to the low V_{th} that characterize ambipolar DGFETs. However, the PDP was almost of the same magnitude for some cells thanks to the decreased time delay offered by the low V_{th} and the full swing (without logic degradation) obtained from transmission gates. One more part of the cost of transmission gates is the larger area required by logic circuits. The major disadvantage of the static logic cells generated from the proposed reconfigurable design methodologies was the high number of configuration signals. This issue is alleviated by the design of partial functionality logic cells, which in addition decreases the area and enhances circuit performance. In fact, for both approaches (function classifications or AmBDDs), the first step is to define the functions that we aim to achieve at the circuit output. Thus, a designer can analyze the functions expected to be used intensively in a computing application, and then generate partial-functionality cells

responding to the application needs, subsequently requiring lower area, fewer configuration signals and improved performance.

4.6 Chapter Contributions and Summary

Founded on realistic device models, in this chapter, various logic design flavours with ambipolar CNTFETs were considered simultaneously. In the context of standard cells, a set of dynamic and static logic gates has been characterized. The results were compared to conventional CMOS logic gates. It was demonstrated that the TTSM approach described in chapter 2 allows the implementation of both static and dynamic logic gates in a very efficient and compact way, increasing the compactness of logic gates by a factor of 2X with complementary static logic. Moreover, the proposed efficient design, combined with the benefits of the CNT technology, offers a clear improvement in terms of delay compared to CMOS. Despite the increase of power consumption observed with the designed gates, an improved PDP was reserved. We illustrated the flexibility brought by the proposed compact structures at the layout level thanks to their regularity and symmetry which answers some nanotechnology manufacturing contingencies usually required by nano-devices based on nanowires or carbon nanotubes. In the same context of standard cells, we evaluated the low-power design technique proposed in chapter 2. Results showed an improvement in power consumption for both variants (dynamic and static). These resolve two major problems usually related to ambipolar devices with undoped channels (V_{DS}-dependent I_{OFF}, in addition to low V_{th}).

In the context of reconfigurable circuits obtained from the design approaches of chapter 3, ambipolar DG-CNTFETs showed less efficiency to implement full functionality reconfigurable logic. This was mainly due to the necessity of using transmission gates to resolve some electrical issues connected to Am-IDGFET behaviour in general. It was shown that transmission gates had a mixed impact on the overall circuit structures. On one hand, it offers a very clean and flexible reconfigurable logic (no logic level degradation). On the other hand, it increases the area of logic cells and the power consumption. Concerning delays, CNT technology reconfigurable gates kept the same improvement as shown with the standard cells.

Area, power consumption and the number of configuration signals limit the efficiency of reconfigurable cell design approaches evaluated in this chapter. Cells with partial functionality could be an alternative to full-functionality cells if they are wisely exploited at an architectural level making the approach very interesting for ambipolar-CNTFET-based FPGAs.

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Chapter 5

Conclusions and future works

5.1 Conclusions

One-dimensional materials such as CNTs, GNRs and SiNW benefit from high mobility making them highly promising candidates to replace the silicon channel in CMOS transistors. In addition, when Schottky barriers are present at the drain and source channel access points, they demonstrate an interesting behaviour known as “ambipolarity”. To control such behavior, chemical doping is not easy and a better alternative is to electrostatically control the polarity of devices via a fourth terminal (second gate). Hence by using ambipolar devices in a double gate context, a new category of devices has seen the light, which we call “Am-IDGFETs” (Ambipolar Independent Double Gate Field Effect Transistors). These devices are capable of operating as either N-type or P-type switches according to their back-gate bias voltage. As a result, a richer set of switching options are available in this device, which has no counterpart in CMOS technology. However, richer ambipolar logic requires innovative design paradigms, since conventional methodologies and techniques based on unipolar three-terminal devices are no longer suitable to build optimal ambipolar logic. The contribution of this dissertation is to define systematic design methodologies, logic synthesis and evaluation techniques to obtain more universal design approaches that can exploit the opportunities offered by ambipolar logic. This was focused on two main axes; standard-cell logic and reconfigurable logic. For each axis, design methodologies and/or synthesis techniques were established. To assess the pros and cons of the proposed design approaches, accurate electrical simulations based on a compact DG-CNTFET model as well as detailed comparisons with CMOS-16nm technology were performed. Figure 5-1 summarizes the thesis contributions and describes the obtained results.

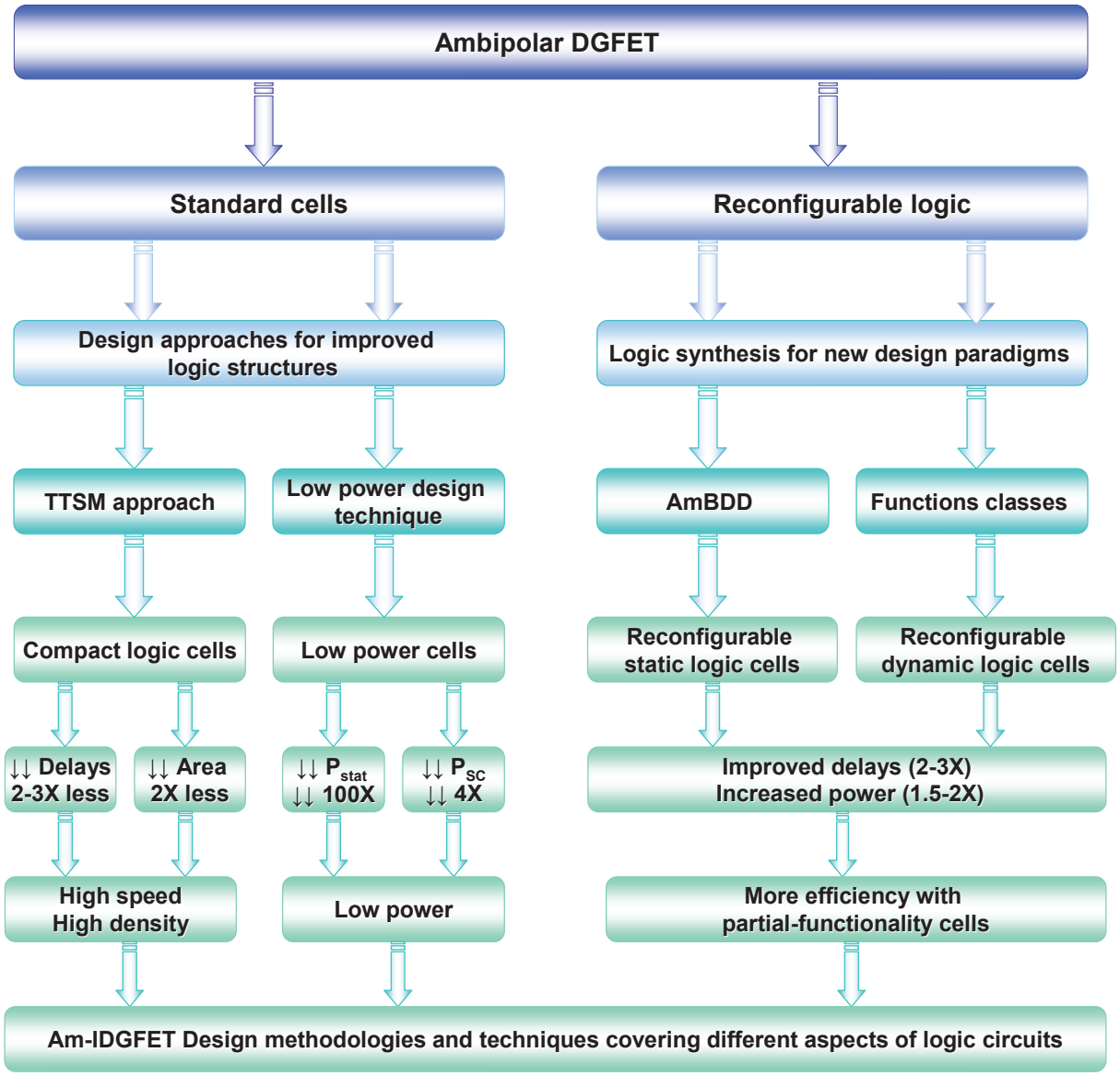


Figure 5-1. Thesis contributions and results

Standard-cells: The standard-cell based design methodology is still likely to hold with emerging (nanoscale) technologies. In this context, we designed key logic cells with Am-IDGFETs to constitute a cell library for use by synthesis tools. The fourth- terminal of the Am-IDGFET device was specifically exploited to realize two novel approaches to the design of standard logic gates.

The first approach (TTSM) efficiently reduces the transistor count for logic cells in static and dynamic logic styles, leading to more compact logic structures with comparable power consumption, and improved speed and area compared to conventional gates. The TTSM approach proves that the number of transistors required by conventional structures can be divided by 2 in the case of some complementary static logic gates. The same gain of 2X has been shown concerning delays. This opens up the opportunity to implement in a very efficient and compact way several logic functions (such as XOR or MUX). Such an approach can be applied to build a whole library of standard logic cells with high density and high speed.

The second design approach is a low-power design technique to solve some issues related to undoped ambipolar devices in general. The first issue is the high I_{OFF} current, which increases the leakage. The second issue is the low threshold voltage V_{TH} which (apart from increasing I_{OFF}) increases short-circuit power as a side-effect of enabling fast logic. To resolve such problems, we propose controlling the state of transistors by switching them off during input transitions via their back-gates; in such a way as to decrease the short-circuit contribution to dynamic power. A decrease of 4X and 3X in terms of short-circuit power and total power has been achieved, respectively, in the case of DG-CNTFET based circuits. Moreover, we showed that by inverting the transistor back-gate voltages during the standby mode, the leakage current I_{OFF} (and consequently static power) is reduced by a factor of 100X.

Reconfigurable logic cells: It was shown that with Am-IDGFETs, a new vector for reconfigurability is possible. In order to synthesize optimal logic, we defined two systematic reconfigurable design methodologies. At first, we investigated the function classification concept by matching each class to its generic structure, and showed that every generic class structure can be implemented in a reconfigurable cell. Furthermore, we identified a correlation between different classes, thus offering the possibility to build reconfigurable logic cells with partial or full functionality. Based on a dynamic logic style, we designed a set of 2-input reconfigurable logic cells, as well as a static logic cell.

We also proposed an Ambipolar Binary Decision Diagram (Am-BDD), to adapt the conventional BDD logic synthesis and verification technique to ambipolar devices in reconfigurable logic. We demonstrated how this method enables us to build Am-IDGFET-based n-input reconfigurable cells from scratch. We also showed how specific correlations between configuration signals can lead to a minimization of their total number. Using the Am-BDD technique, we designed a reconfigurable 2-input cell capable of achieving 16 functions and also derived more compact cells with partial functionality.

At transistor level implementation, for both design approaches, we used transmission gates instead of single Am-IDGFETs to resolve the issue of logic degradation and to ensure the proper operation of the synthesized circuits. This offered a very clean and flexible reconfigurable logic. We subsequently evaluated a set of reconfigurable cells generated from the proposed design approaches in both static and dynamic logic based on DG-CNTFET technology. The simulations showed that full functionality reconfigurable logic resulted in lower efficiency, mainly due to the necessity of using (multiple device) transmission gates instead of single transistors. The penalty on performance metrics concerns the power consumption of logic cells (increased by 2X-3X) as well as the area. Concerning delays, CNT technology reconfigurable gates demonstrated an improvement of 2X-3X as compared to standard logic cells. The increase in power consumption and decrease in delay yielded a comparable PDP.

To sum up, the area, power consumption and number of configuration signals do in fact limit the efficiency of reconfigurable cells design approaches. An efficient alternative could be the use of partial-functionality cells instead of full-functionality cells. This was shown to be a feasible solution if cells are wisely exploited at an architectural level [5-1, 5-2, 5-3], especially if only a single polarity of each input is needed (unlike other technologies), leading to a reduction of the number of signals to route and making the approach very interesting for ambipolar CNTFET-based FPGAs.

To conclude, Am-IDGFETs offer new opportunities for the designer thanks to the fourth terminal. Compact logic cells and reconfigurable logic blocks have been built in this thesis by applying innovative design methodologies and techniques. The common attractive result for all designed circuits was the improvement of delays leading to high speed logic. Although an increase of power consumption was mentioned with Am-IDFET based circuits, we showed the possibility to decrease the power consumption via back gate biasing technique and obtained a decrease of 100X in static power, which will represent more than 50% of the total power in nanoscale logic circuits. The contribution of this thesis, at many levels of logic design (compact standard cells, reconfigurable logic, high performance circuits and low power circuits) could enable designers to envisage the possibility of building a heterogeneous platform where many blocks can be implemented together to achieve maximum benefit from the Am-IDGFET technology.

5.2 Future works

This thesis presented contributions to design techniques for and assessment of ambipolar logic. We stress that all techniques and approaches are generic for any Am-IDGFET, and independent of the target technology (CNT, SiNW, GNRs). This opens the way to further work to optimize the approaches and resolve issues related to Am-IDGFETs as an emergent technology at several levels:

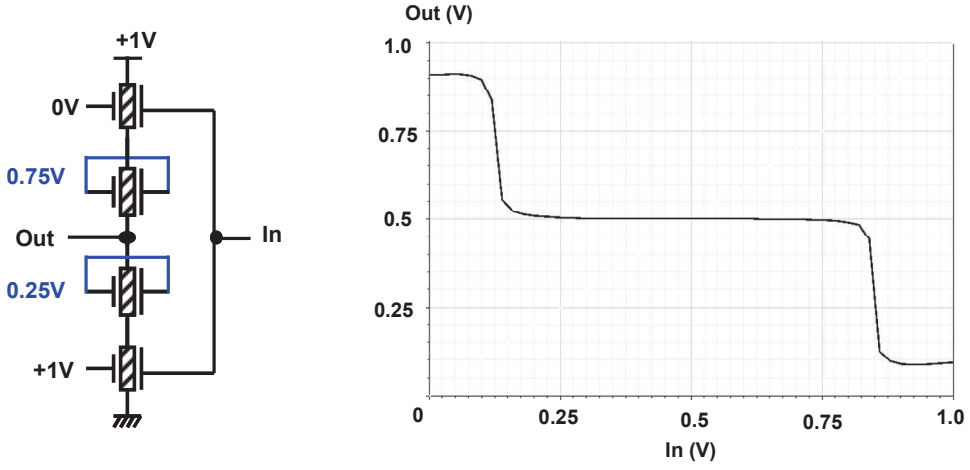
Device:

- Am-IDGFET technology is still at an embryonic stage. Many challenges face 1-dimensional materials. In addition to the two challenges of low cost and large scale manufacture, Graphene has a low energy bandgap, so it continues to conduct a lot of electrons even at the OFF state. If there are a billion of graphene transistors on a chip, a large amount of energy would be wasted. This can be improved if graphene ribbons can be made thinner, and by using techniques like doping and making graphene inverters. Concerning CNT technology, many issues should be resolved; starting with the growth of nanotubes (diameter, chirality, alignment, homogeneity, etc), up to their integration with CMOS process. Finally, some fabrication techniques of silicon nanowires, especially the bottom-up approaches undergo a high variability with respect to the nanowire dimensions (cross-section, length), lattice structure, surface states, etc. The process needs to be controlled in a more accurate way in order to guarantee the uniformity of the electrical properties of the nanowires. With the double gate structure, challenges are accentuated because of the integration of a second gate, requiring a more complex fabrication process. In addition, the contact between the 1D structure and the electrical source/drain contact needs a full understanding of the underlying physics for performance optimization as well as for realistic and reliable modelling of devices.
- In this work, all results are based on a physical compact model of a DG-CNTFET technology, which shows encouraging accuracy compared to measurements published in the literature. It would at this point be interesting to extend the evaluation of design approaches in this work to other ambipolar technologies, such as SiNW. As the basis for technology and device modelling matures, various ambipolar technologies can be compared and increased system-level design opportunities are likely to appear.
- Concerning the electrical properties of ambipolar CNTFET devices, it was assumed in this work that the range of voltage for both gates (front gate and back gate) is the same. However, it is not the case with demonstrated devices whether with CNT technology [5-4] or SiNW technology [5-5]. In [5-6], Ben Jemaa has proposed that the problem can be solved at two different levels. If there is a margin for some extra technological choices, then the work function of both gates, as well as their respective oxide thickness, can be

engineered in order to match the voltage range of both types of gates. If this solution is not available, then the designer has to distinguish between signals feeding FGs and those feeding BGs (implying a natural boundary between data and configuration, which may hinder some system-level design approaches). While the distinction can be handled by design tools, it does mean that additional design complexity and cost can be expected.

Logic:

- Multiple-valued logic (MVL) circuits have attracted substantial interest due to the capability of increasing information content per unit area. Extensive design techniques for MVL circuits (especially ternary logic inverters) have been proposed for implementation in CMOS technology. With the CNTFET device, the threshold voltage of the transistor can be controlled via the diameter, and some papers exploit this feature to design ternary logic inverters by using different CNTFET diameters in the same circuit. Such fine manufacturing control appears however to be outside the domain of feasibility for the foreseeable future. With DG-CNTFET devices, preliminary observations showed that it might be possible to build ternary inverters without recourse to diameter control (but with extra voltage references). For example, the structure presented in figure 5-3(a) gives a DC V_{out}/ V_{in} transfer characteristic very close to that of the T-inverter behavior as shown in figure 5-3(b). More investigations of the appropriate range of voltage and circuit arrangement could be interesting to define a methodology which allows ternary logic design.



(a) (b)

Figure 5-2. T-Inverter using Am-IDGFETs as resistances: schematic (a) V_{out}/V_{in} DC behaviour (b)

Tools:

- Based on the TTSM approach to design compact logic structures, it is possible to build a whole library of standard cells. Once the library is designed and characterized, the results can be used to perform multi-level logic synthesis and to compare the various logic styles. Also, since some gates (such as XOR and MUX) are presented in a very compact way

within the library, it is very useful to orient the logic mapping tools toward the selective utilization of these gates – especially with the high flexibility of MUXs to perform combinatorial logic. Furthermore, the micro-electronics industry is still attached to specific standard cell-based circuit design. Thus, providing a methodology and a tool set that would enable the evaluation of ambipolar DGFET technology within an ASIC flow would be relevant.

- Concerning reconfigurable logic cells, their impact can be investigated at the system level to find out the trade-offs between their characteristics in order to configure architectures in an efficient way. Indeed, the cell performance or number of realizable functions may have some impact on design area, power and critical path delay. Several research works have proven that the use of logic cells with partial functionality can outperform standard look-up-tables (LUT) in FPGA architectures in terms of both delay and area after circuit placement and routing [5-1, 5-2, 5-3]. For example, some logic functions such as XNOR, AOI can be used more often through a circuit mapping which makes them more critical for cell design. In other words, it is possible that partial-functionality cells with fewer transistors and control signals, can show better performance metrics than full-functionality cells when exploited at an architectural level - especially when the basic logic functions (INV, NAND, NOR) to build any Boolean logic function are provided with those cells.
- At a system level, different Nano-Architectures (NAs) based on Nanoscale Application Specific Integrated Circuits (NASICs) [5-7, 5-8, 5-9], hybrid CMOS/nanoelectronic ("CMOL") technology [5-10], Field-Programmable Nanowire Interconnects (FPNIs) or Matrix-based NAs [5-11] have been proposed in the last decade. To efficiently map and configure Nano-Architectures (NAs), appropriate design flows and CAD tools are required to complement mature design techniques, since existing FPGA placement tools can only handle medium-scale circuits, limiting their further reuse. In the framework of the NANOGRAIN project, the INL design team also focused on approaches to map large applications onto NAs. In [5-12], we introduce a new interconnect topology for cell matrices that provides flexible logical depth and the ability to reconfigure cells and read their output values during data pipelining, with the following improvements: (+8%) mapping success rate, (~ +50%) width of output data compared to the top results achieved by other topologies. Also, in [5-13, 5-14] we proposed a new methodology for mapping applications onto matrix-based nanocomputer architectures. The methodology is multi-objective and allows the generation of diverse mapping configurations with specific power consumption, area or delay constraints. Since it takes into account the connectivity restrictions of cell matrices, it can be used for architecture tuning in order to reduce routing overheads and improve the characteristics of a design. A side-by-side comparison with existing algorithms reveals improvements in both routing area and wire width, respectively by 35.63% and 32.88%. Current work tackles how to address the problem of

mapping large applications onto hierarchical nanocomputer architectures by defining a methodology which benefits from (i) the use of libraries of pre-mapped IP cores and (ii) the multi-objective mapping process. These features allow us to reduce the mapping time and to develop circuits with certain area, power and critical path delay characteristics.

Non-volatile memory integration:

- The distribution of the area occupation between logic, memory and routing resources within an FPGA shows that almost 80% of the silicon area is used just for routing resources and configuration memories of the total area. SRAM-based FPGAs have been the standard focus of reconfigurable computing in the last two decades. Some FPGAs use flash memory cells as configuration devices so that the FPGA can retain its configured state when the power is off, but flash memory has its drawbacks in terms of cost, speed, and write power in addition to its limited scalability [5-15]. Recent developments in non-volatile memory technologies may make it possible to increase the flexibility of reconfigurable devices without the limitations of flash memory cells. A multitude of memory technologies are currently pursued in active research, such as ferroelectric RAM and carbon nanotube memory. Among the most promising research results are those based on magnetic switching, resistance-change, and phase-change materials. Table 5-1 is a comparison between some non-volatile technologies.

TABLE 5-1. COMPARISON OF DIFFERENT NON-VOLATILE TECHNOLOGIES [5-15]

	Flash	MRAM	RRAM	PCRAM
Endurance	10^6	$> 10^{16}$	10^6	10^{12}
Switch Speed	> 100ns	~ 10ns	< 50ns	~ 50ns
Read Speed	> 10ns	< 0.5ns	< 50ns	~ 60ns

Hybrid FPGA architectures can be cost-effective, since the routing interconnect and configuration switches can be fabricated above the logic blocks. The lower endurance requirements and higher defect tolerance can allow reconfigurable computing architectures to support emerging memory technologies that may not yet be well-developed enough for commercial memory applications. In parallel with the development of these technologies, it is necessary to create the infrastructure for performing CMOS/resistive-switching FPGAs and SOCs. The issues of using non-volatile memories into circuit and system design must be tackled and the exploration of means and benefits of their integration in a complete architecture at system level must be investigated.

As Am-IDGFET structure can be based on a top gate and a back gate (such as the example of DG-CNTFET), the integration of NVM at the back end of the wafer to set the polarity of the device via its back gate and keep the process of logic with the front gate can achieve a 3-D-like architecture with benefits in terms of area and required routing interconnections.

Regularity and Robustness:

- Regularity is a prime choice to alleviate many issues at the same time. Regular layout fabrics have an advantage of higher yield as they maximize the layout manufacturability. Recently SiNW DGFET arrays of gates have been presented in [5-16]. Figure 5-3 showed the possibility of using a Sea-of-Tiles approach for designing an efficient regular layout fabric. The same tile can be used to implement different functions. Thus such a tile can represent the basic building block for future ambipolar logic blocks. A configurable sea-of-tiles (SoTs) architecture can be built with an array of logic tiles uniformly spread across the chip. As we proposed an approach to build a standard cell library with more compact structures and high performance, the proposed regular layout fabric can be the cornerstone of the whole gates which gives a more complete and authentic library. At the layout level, design rules and maybe automatic generation methodologies can be recreated to efficiently exploit the regularity offered by "Tiles" approach.

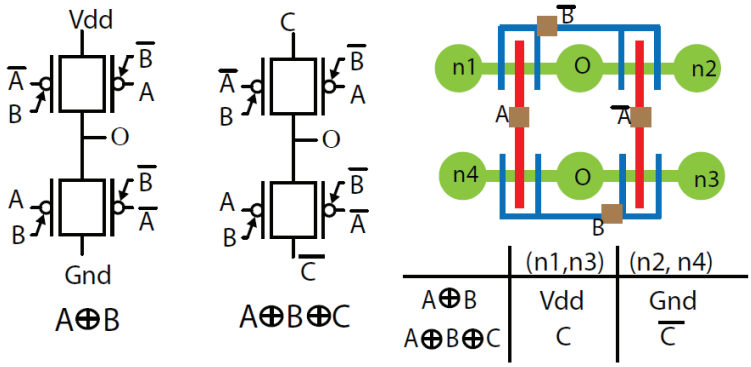


Figure 5-3. Schematic of a 2-input and 3-input XOR along with the mapping on to the same Tile [5-16]

- Finally, as we are dealing with nanoscale emerging technologies, it is necessary to inspect the reliability as the backbone of emergent nanodevices. Reliability in future computing systems can be tackled from different design views; from the layout level to the architecture level. Some designers try to reuse conventional techniques such as defect avoidance [5-17], correction coding [5-18], or redundancy in order to improve robustness. Other design teams choose to handle this issue directly at the physical and layout level by proposing methods and techniques for better alignment [5-19] and an improved immunity to metallic nanotubes [5-20] with the CNT technology. Nevertheless, all the proposed techniques lead to a penalty in terms of performance metrics of logic circuits. This could be incorporated at a design level by the integration of robustness techniques such as defect tolerance as metrics into the evaluation tools. Thus, the tool should be capable of evaluating performance metrics of nanocircuits, taking into account the impact of robustness techniques.

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- I. O'Connor, **K. Jabeur,** S. Le Beux, D. Navarro, "Ambipolar Independent Double Gate FET Logic ", IEEE/ACM International Symposium (NanoArch), July 4-6-2012, Amsterdam, the Netherlands

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Invited Talk

- "Ambipolar double-gate transistor logic circuit design-methods and techniques", Integrated Systems Centre SI with Prof. G. De Micheli, 29 May 2012, EPFL, Lausanne, Suisse.

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Résumé Etendu

Méthodes et techniques de synthèse des circuits logiques à base des transistors ambipolaires à double grille

Résumé

La croissance continue de la demande mondiale des produits semi-conducteurs (dans un large éventail de secteurs, tels que la sécurité, la santé, le divertissement, la connectivité, l'énergie, etc) a été conduite par la loi de Moore en doublant régulièrement la densité et les performances des circuits numériques. Cependant, comme la miniaturisation de la technologie CMOS commence à atteindre ses limites théoriques, l'ITRS prévoit une nouvelle ère connue sous le nom "Beyond CMOS". Des nouveaux matériaux et dispositifs révèlent une capacité à compléter ou même remplacer le transistor CMOS ou son canal dans les systèmes sur puce à base de silicium. Cela a conduit à l'identification des phénomènes prometteurs tel que la conduction ambipolaire dans les structures quasi uni- et zéro-dimensionnels, par exemple dans les nanotubes de carbone, le graphène et les nanofils de silicium. L'ambipolarité, dans un contexte à double grille (DGFET), signifie qu'un comportement de type N et P puisse être observé dans le même dispositif en fonction de la polarité de la tension de la grille arrière. En plus de leur performance attractive et leur faible consommation de puissance, les dispositifs ambipolaires à double grille indépendantes (Am-IDGFET) permettent le développement des structures logiques ainsi que des paradigmes de conception entièrement inédits. Les techniques classiques de la synthèse logique ne peuvent pas représenter la capacité des Am-IDGFETs de fonctionner soit comme commutateurs de type N ou de type P. Alors des nouvelles techniques doivent être trouvées pour construire une logique optimale.
Le travail de cette thèse explore les techniques de conception pour permettre l'utilisation de ces dispositifs en définissant des approches génériques et des techniques de conception basées sur les Am-IDGFETs. Deux contextes différents sont abordés: (i) l'amélioration de la conception de cellules logiques avec des structures plus compactes et une meilleure performance, ainsi que des techniques de conception à faible consommation qui exploitent la grille arrière du dispositif, et (ii) l'adaptation des techniques classiques de synthèse logique comme les diagrammes de décision binaires (BDDs) ou l'approche de classification des fonctions afin de construire des cellules logiques reconfigurables à base des Am-IDGFETs. Les méthodes et les techniques proposées sont validées et évaluées à travers une étude basée sur le dispositif DG-CNTFET par l'intermédiaire des simulations précises, en utilisant le modèle DG-CNTFET le plus mature disponible dans la littérature.

Chapitre 1
Introduction

Depuis le milieu du 20e siècle, l'apparition du transistor à semi-conducteur a abouti à la naissance de traitement de l'information à grand public. Grâce à un développement continu, cette invention a transformé presque tous les aspects de la vie. Dirigée par la loi de Moore, la miniaturisation des transistors continue pendant le 21e siècle. Il s'avère que les tendances passées en matière de croissance, en doublant la densité du circuit et en augmentant les performances d'environ 40% pour chaque génération de nouvelle technologie [1-13] ne peut être maintenue par la réduction conventionnelle du canal de transistor. Pour avoir un aperçu de l'avenir de l'industrie de semi-conducteur, l'International Technology Roadmap for Semiconductors (ITRS) [1-6] reconnaît l'existence de limites physiques à cette croissance: le canal de transistor CMOS Silicium ne peut pas être réduit au-delà de certaines dimensions qui sont définies par des limites physiques [1-7]. Actuellement, il y a trois limites fondamentales à la miniaturisation des transistors CMOS: des limites matérielles liées à la performance, des limites de la lithographie et des limites économiques.

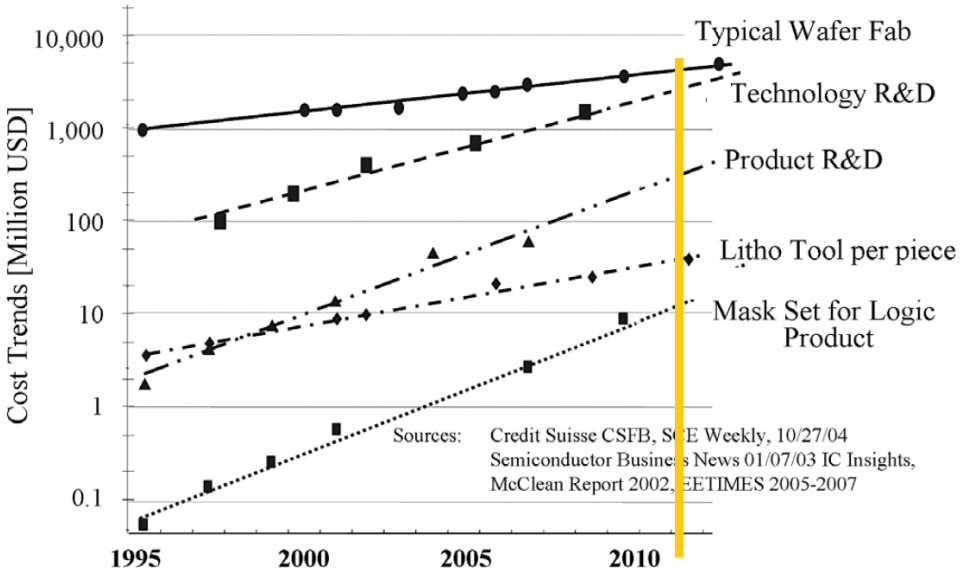


Figure 1-1. Tendances des prix dans l'industrie des semi-conducteurs [1-102]

Les candidats qui sont viables pour un éventuel remplacement de la technologie CMOS, sont généralement appelés les technologies émergentes. Ces solutions provisoires sont fondées sur des nouveaux matériaux, la physique des dispositifs, la conception des circuits etc.
La nouveauté de cette thèse consiste à développer des nouvelles approches de conception et des outils adaptés à un nouveau type de transistors connu sous le nom "transistor ambipolaire". Ce dispositif possède un comportement de conduction ambipolaire, distinct de dispositifs conventionnels et caractérisé par une superposition des courants d'électrons et des courants de trous, expérimentalement signalés dans des nombreux dispositifs post-silicium (nanotubes de carbone, le graphène, nanofils de silicium ...). Un tel comportement n'est pas exploité avec les techniques conventionnelles de conception pour les circuits numériques et analogiques à base de transistors unipolaires. La conversion du comportement ambipolaire à un comportement unipolaire est réalisée, soit au niveau de la fabrication (suppression des barrières Schottky) soit au niveau design (connexion des doubles grilles). Toutefois, il a été démontré que la polarité des dispositifs ambipolaires, c'est à dire, qu'ils sont de type N ou de type P, peut être contrôlée pendant leur fonctionnement. Cela représente une opportunité pour

des nouvelles méthodologies de conception pour les circuits ambipolaires, et qui peuvent être abordés sous plusieurs angles: i) des portes logiques standards ou des architectures reconfigurables, ii) l'optimisation de la consommation ou la vitesse et iii) les styles logiques statiques ou dynamiques. Cette thèse propose plusieurs techniques et méthodologies de conception basées sur ce nouveau type de dispositif ambipolaire avec une structure à double grille. Les approches de conception proposées sont d'abord décrites. Ensuite, les blocs logiques innovants sont dérivés, validées et évaluée à l'aide d'un modèle physique précis d'un transistor à double grille au canal à nanotubes de carbone (DG-CNTFET) réalisé grâce à une synergie entre les équipes de recherche.

1.1 Transistor FET Ambipolaire à Double Grille Indépendamment contrôlées (Am-IDGFET)

Avec la recherche intensive des nouveaux dispositifs et matériaux, un phénomène de conduction ambipolaire a été identifié dans des nombreux technologies post-silicium, tels que les dispositifs de nanotubes de carbone [1-138], de graphène [1-139] et des nanofils de silicium [1-140, de 1-141, 1-42]. La possibilité de sélectionner la polarité (P ou N) en utilisant une deuxième grille [1-135, 1-137] a inspiré certaines équipes de conception pour exploiter les dispositifs Am-IDGFET dans des nouveaux circuits logiques montrant des gains significatifs en termes de surface, puissance et performance [1-146, 1-147, 1-148, 1-149, 1-150].

1.1.1 Fabrication des Am-IDGFETs

Dans le cas de CNTFET à double grille, un dispositif DG-CNTFET a été fabriqué et caractérisé en utilisant une grille avant et une grille arrière [1-135]. Figure 1-2 décrit la structure et les caractéristiques (I-V) du transistor CNTFET à double grille. La grille avant (FG) dans la région A commande la conduction du courant à travers le dispositif, tandis que la grille de polarité (ou grille arrière, BG) dans la région B commande le type de polarité: une haute tension ou basse tension définissent, respectivement, un comportement de type N ou P du transistor.

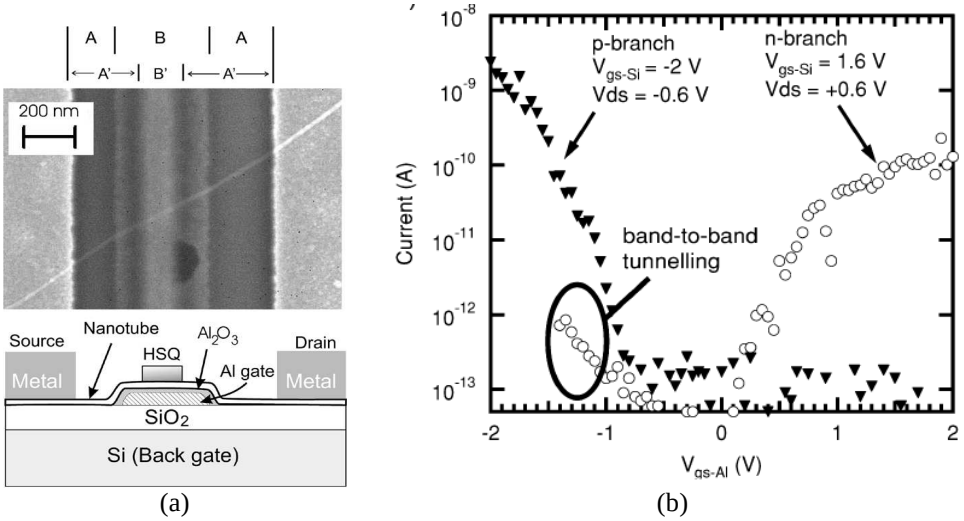


Figure 1-2. Vue d'un transistor ambipolaire à double grille et sa caractérisation [1-135]: (a) Image par MEB de la section transversale d'un CNTFET à double grille. La region A est la grille arrière, B est la grille avant. (b) La courbe I_{DS}-V_{GS} avec une tension fixée de la grille arrière. Pour une tension positive (negative): le dispositif a un comportement de type N- (P-).

Bien que les Am-IDGFETs aient d'abord été démontré avec des nanotubes de carbone, des travaux récents ont été réalisés avec la technologie des nanofils de silicium (SiNW). Dans [1-137], une structure de dispositif exploitant la configuration indépendante des SiNW à double grille a été démontrée. Les figures 1-3 et 1-4 montrent la structure de dispositif ainsi que ses caractéristiques de transfert, respectivement.

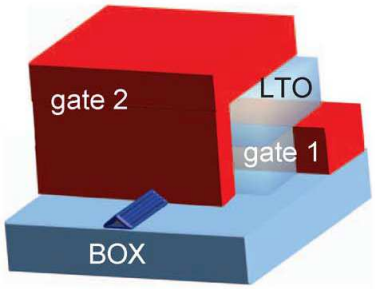


Figure 1-3. Transistor ambipolaire à nanofils de silicium avec double grille [1-137]

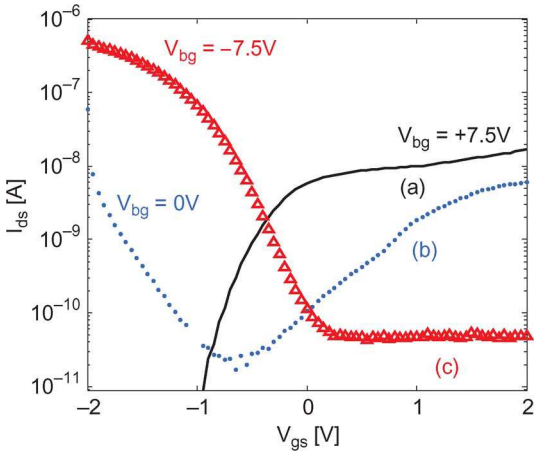


Figure 1-4. Caractéristiques I_{DS}–V_{GS} pour différentes tensions de grille arrière(a) V_{BG} = +7.5 V pour un comportement de type N. (b) V_{BG} = 0 V pour un comportement ambipolaire I_{DS}–V_{GS}. (c) V_{BG} = −7.5 V pour un comportement de type P [1-137]

1.1.2 Structure générique des Am-IDGFETs

Indépendamment de la technologie selon laquelle l'Am-IDGFET est fabriqué, nous visons à explorer le comportement ambipolaire à travers les trois états de dispositif (de type N, de type P ou OFF). Figure 1-5 décrit le comportement générique d'un seul transistor Am-IDGFET. Ce symbole, ainsi que les trois configurations réalisables par l'intermédiaire de la grille arrière (BG), est utilisé tout au long de cette thèse.

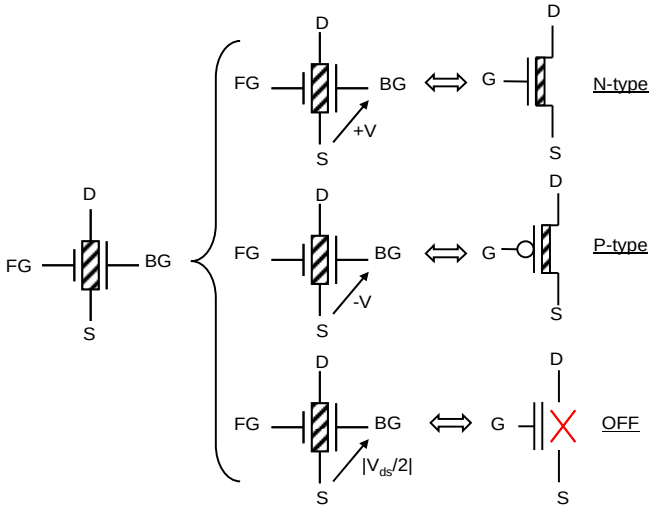


Figure 1-5. Symbole et configurations du dispositif Am-IDGFET

La grille avant FG met le dispositif à l'état ON (passant) ou à l'état OFF (bloqué), de la même manière qu'une grille conventionnelle d'un MOSFET; tandis que la grille arrière BG contrôle la polarité (N ou P) avec une valeur de tension positive (V_{BG}-V_S = + V) ou négatif (V_{BG}-V_S =- V), respectivement. Le dispositif est à l'état OFF (quelle que soit la tension sur la grille avant

FG) si la grille arrière est fixé à $V_0 = |V_{DS}/2|$ (V_{DS} est la tension appliquée entre le drain et la source).

1.2 Défis et contributions de thèse

Dans cette section, nous décrivons brièvement les défis auxquels sont confrontés les outils EDA (Electronics Design Automation) et de leurs origines. Ensuite, nous expliquons comment ce travail propose des méthodologies et outils de conception pour exploiter les capacités de Am-IDGFETs pour construire des paradigmes innovants de conception logique.

1.2.1 Défis

La nouvelle génération des outils de conception EDA pour les puces CMOS nanométriques a commencé à adopter le calcul de la physique quantique (la théorie des fonctions de densité, fonction non-équilibre de Green, la fonction de Wigner) pour s'attaquer aux problèmes nanométriques tels que les courants de fuite et ainsi de suite. Pour les technologies au-delà, de la loi de Moore tels que les nanotubes de carbone, le graphène et les dispositifs moléculaires, les défis sont plus complexes. Parce qu'ils sont encore à leurs balbutiements; la précision de fabrication est faible, ce qui entraîne une variabilité statistiquement significative de leurs propriétés physiques, chimiques et électriques. Ainsi, les applications, les architectures et les modèles doivent avancer en parallèle avec les efforts de dispositifs et de matériaux [1-176].
L'objectif de cette thèse concerne l'exploitation du potentiel d'une nouvelle classe de dispositifs émergents pour amener un nouveau paradigme de calcul avec des fonctionnalités améliorées. Nous présentons des approches de conception et des outils de CAO pour automatiser la synthèse logique et l'optimisation des structures de cellules standards construites à partir des nano-dispositifs émergents. Un autre objectif de la thèse est de valider et d'évaluer les techniques de conceptions proposées par des simulations électriques basées sur des modèles précis de périphériques physiques. Les contributions travail de thèse sont détaillées ci-dessous.

1.2.2 Contributions à la recherche

L'Am-IDGFET forme une nouvelle famille de dispositifs particuliers en vue du fait qu'il associe trois avantages: (i) il est généralement un dispositif électronique unidimensionnel (CNT ou SiNW), ce qui signifie une grande mobilité et densité de courant, (ii) Deux grilles indépendamment contrôlées qui offrent plus des options pour faire de la logique, (iii) le comportement ambipolaire ouvre la voie à une polarité de type N et P dans le même dispositif. La créativité du travail de thèse consiste à considérer cette nouvelle classe de technologie émergente comme une opportunité pour des nouveaux paradigmes de conception. Ainsi, des nombreuses options sont disponibles avec la technologie ambipolaire sans homologues en technologie CMOS. Néanmoins, cette nouvelle classe de technologie nécessite des approches et des outils de conception pour construire une image réaliste et complète de la logique ambipolaire. Donc, il sera nécessaire de réviser ou de réinventer plusieurs outils de synthèse logique, des méthodes de conception, et des techniques d'évaluation afin d'automatiser la conception pour une logique optimisée. Comme le montre la figure 1-6, ce travail propose un nouveau paradigme de méthodologies de conception et des techniques pour aider les concepteurs traitant des technologies émergentes. Les possibilités offertes par les Am-IDGFETs sont exploitées selon deux axes de conception; les cellules standards et la logique reconfigurable avec une évaluation des approches de conception proposées, basée sur un modèle compacte d'un dispositif DG-CNTFET.

Figure 1-6. Diagramme de l'organisation de la thèse

Cellules standard: Basés sur les Am-IDGFETs, nous décrivons une approche de conception pour améliorer la compacité des cellules logiques standards (statiques et dynamiques). Nous montrons aussi une amélioration significative de la performance du circuit. Dans le même contexte des cellules standards, la consommation d'énergie représente un obstacle d'intégration à l'échelle nanométrique. En utilisant les Am-IDGFETs, nous pouvons être en mesure de contourner cet inconvénient en appliquant des techniques de conceptions qui réduisent la consommation d'une manière dynamique.

Logique reconfigurable: Avec les Am-IDGFETs, une perspective novatrice de reconfigurabilité est possible grâce à la deuxième grille. Deux méthodes sont proposées dans

cette thèse. La première méthode exploite la capacité d'Am-IDGFETs pour basculer entre les 3-Etats (N, P et OFF) et utilise l'outil de classification NPN pour manipuler des fonctions booléennes. Basé sur une certaine corrélation entre les structures logiques de classes de fonctions booléennes, des cellules logiques reconfigurables sont conçues. La seconde méthode est inspirée des outils EDA classiques « les BDDs » qui sont remodelés d'une manière à s'adapter à la nouvelle fonctionnalité de Am-IDGFETs.
Validation et évaluation: Pour simuler les circuits logiques générés, nous nous sommes basées sur un modèle compact réalisé par l'équipe de recherche IMS Bordeaux. Il représente le premier modèle physique précis d'un DG-CNTFET avec une convergence et une vitesse de simulation efficaces et compatibles avec la conception de circuits. Aussi, nous comparons les résultats avec le noeud technologique CMOS 16 nm en utilisant un modèle prédictif.

1.3 Organisation de la thèse :

La thèse est organisée selon trois chapitres principaux sans inclure les chapitres de l'introduction et des conclusions.
Dans le **chapitre 2**, nous proposons une approche de conception pour construire des structures logiques compactes selon des styles logiques dynamiques et statiques à haute performance. Ensuite, nous définissons une méthode de conception à faible consommation à l'aide des Am-IDGFETs.
Dans le **chapitre 3**, nous remodelons certains outils de CAO et nous réinventons des techniques de conception pour exploiter la capacité unique des Am-IDGFETs de synthétiser une logique reconfigurable à grain fin.
Dans le **chapitre 4**, nous comparons les circuits logiques conçus tout au long de la thèse, dans le chapitre 2 et 3, avec leurs homologues en CMOS dans les deux contextes de cellules standard et de la logique reconfigurable. Ainsi, nous pourrions mettre en évidence les avantages et les inconvénients des méthodes de conception proposées et envisager les meilleurs scénarios.
Dans le **chapitre 5**, on conclue les travaux et les résultats de la thèse.

Chapitre 2

Utilisation des Am-IDGFETs pour un nouveau paradigme de cellules logiques standards

Résumé

Dans ce chapitre nous traitons les cellules logiques standard sur deux niveaux. Tout d'abord, nous proposons une approche de conception pour réaliser des circuits logiques compacts avec des dispositifs (Am-IDGFET), en fusionnant chaque 2 transistors en séries grâce à la reconfigurabilité offerte par la grille arrière. L'approche démontre une efficacité qui peut améliorer la compacité des structures logiques d'un facteur de 2X, tandis qu'avec un style logique dynamique, un gain de 30% en termes de nombre de transistors est réalisé pour une variété de scénarios d'application. Deuxièmement, nous proposons une approche de conception pour améliorer la consommation d'énergie dans les circuits numériques. On réduit dynamiquement la puissance de court-circuit pendant le mode actif tout en diminuant de manière significative la puissance statique pendant le mode en veille. Des observations préliminaires ont montré une diminution par un facteur de 4X en terme de court-circuit, et de 100X en terme de consommation statique (pendant le mode en veille). Cette technique représente une solution attractive pour les problèmes habituellement présents dans les FETs ambipolaires avec les canaux en nanotubes de carbone, en nanofils de silicium non dopé ou en graphène; (i) Un courant I_{OFF} élevé, qui est une source de courant de fuite élevé, ainsi que (ii) une faible tension de seuil V_{th}, qui est un facteur double tranchant, étant donné qu'elle offre une vitesse élevée, mais elle augmente la puissance de court-circuit.

2.1 Approche générique à base des Am-IDGFETs pour l'amélioration des structures logiques

Dans les cellules logiques CMOS, les structures de transistors en séries existent à la fois dans les réseaux N-et P- pour implémenter les fonctions logiques. La complexité des mintermes ou maxtermes et le nombre de transistors en série augmentent en parallèle avec l'augmentation de l'entrance des portes logiques. Cela engendre une haute résistance dans les branches de structures CMOS et par conséquent ralentit la réponse des portes logiques. Ce point, qui est une clé déterminante de la performance des circuits numériques, peut être efficacement améliorée en utilisant des transistors Am-IDGFET.

2.1.1 Concept général

En plus de la capacité de charge et la capacité drain/source, le nombre de transistors en série est le cœur de l'estimation de temps de retard. En Effet, la résistance équivalente du chemin logique est proportionnelle au nombre de la longueur minimale des transistors en série, et inversement proportionnelle à la largeur moyenne du transistor. Donc les structures de deux transistors en série (TTS : Two Transistors in-Series) jouent un rôle essentiel dans l'optimisation de la résistance du chemin logique et la capacité de grille avec un impact direct sur le temps de retard, la puissance et la surface. La commutation entre les états N et P dans les Am-IDGFETs permet la substitution des structures TTS par un seul transistor Am-IDGFET sans perte de fonctionnalité, comme indiqué dans la figure 2-1 pour une structure deux transistors en séries de type N (NTTS : N-type Two Transistors in-Series). De ce point, l'idée de ce travail est de développer une approche générique pour fusionner tous les deux

transistors en série dans un seul dispositif. L'approche sera abrégée TTSM (Two-Transistors-in-Series-Merger approach).

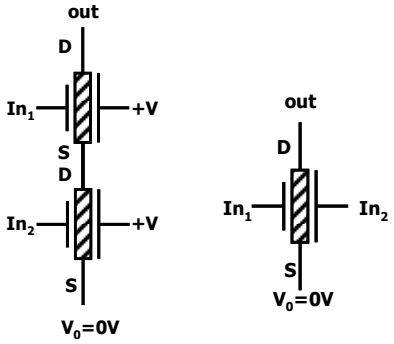


Figure 2-1. Transposition direct d'une structure CMOS-NTTS avec les Am-IDGFETs (a), Un Am-IDGFET equivalent à une structure TTS (b)

Dans la structure initiale NTTS (figure 2-1 (a)), les deux transistors sont de type N puisque la grille arrière BG est fixée à +V et V_0=0V (i.e. V_{BG}-V_S = + V). Dans ce cas, un chemin est établi entre "V_0" et "out" seulement pour In_1In_2 = "11". Dans le cas d'un seul transistor Am-IDGFET, illustré à la figure 2-1 (b), la condition reste la même puisque pour In_2 = "1", la porte arrière BG est fixée à +V de telle sorte que le transistor est de type N et ne sera activé que lorsque In_1 = "1" . Pour les autres combinaisons In_1In_2 = {"01", "10", "00"} le transistor est éteint. Ainsi, la structure NTTS peut être remplacée par un seul Am-IDGFET. Par analogie, la structure PTTS (pour une structure deux transistors en séries de type P) obtient le même avantage puisque les deux transistors sont de type P lorsque la porte arrière est BG à 0V et V_{dd} est fixé à + V (i.e. V_{BG}-V_S =-V).

2.1.2 Cellules logiques statiques à double grille (DGSL)

L'approche TTSM peut être appliquée pour la conception de plusieurs portes logiques. Dans cette section, nous présentons les opportunités de l'utilisation de l'approche d'une manière générique pour des structures basées sur la logique statique complémentaire.

2.1.2.1 Fonction générique

La figure 2-2 illustre un exemple générique décrivant la transformation entre une structure en logique CMOS classique (CSL) et une structure en logique statique à double grille (DGSL) (qui utilise l'approche TTSM). Dans la figure 2-2, les réseaux de transistors sont présentés arbitrairement. Le but de la figure est de montrer que l'approche TTSM peut être employée dans les deux réseaux des transistors (N et P). Un exemple précis est présenté plus tard.

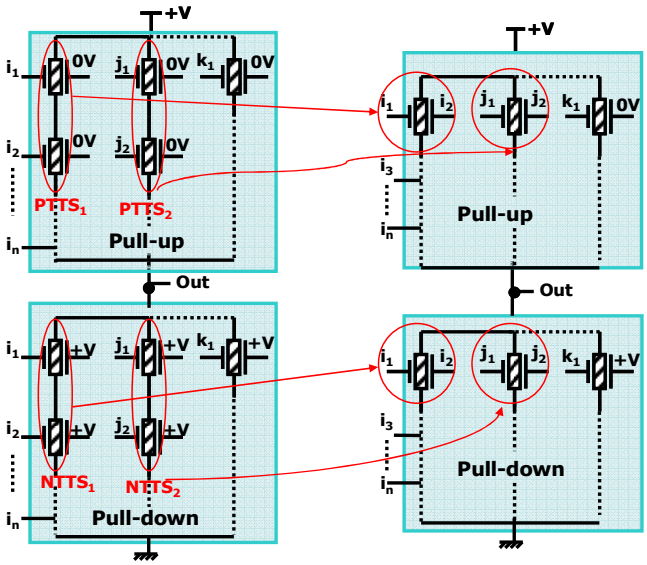


Figure 2-2. Structure CSL (a), structure DGSL (b)

2.1.2.2 Exemples

En appliquant l'approche sur une porte OU-Exclusive (XOR2), la figure 2-3 (b) que chaque structures TTS a été remplacée par un seul Am-IDGFET, conduisant à une réduction de nombre de transistors avec une structure plus compacte de 4 transistors au lieu de 8.

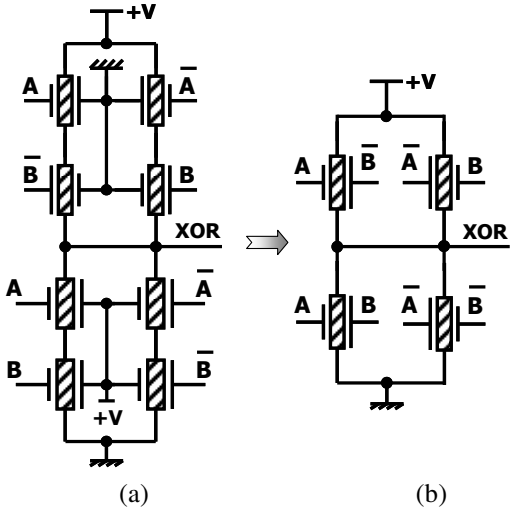


Figure 2-3. Porte logique XOR2: structure CSL (a) structure DGSL

2.1.3 Cellules logiques dynamiques à double grille (DGSL)

Il existe plusieurs variantes structurelles possibles qui peuvent être mises en œuvre pour appliquer l'approche TTSM dans une structure logique dynamique. Pour analyser les avantages et les inconvénients des différents scénarios, nous illustrons leur application à travers l'exemple d'une porte logique à trois entrées (3NAND), comme le montre la figure 2-4. Dans le premier scénario (S1), nous gardons à la fois les transistors d'évaluation et de précharge et on applique l'approche TTSM à l'intérieur du bloc de la fonction logique. Dans le second scénario (S2), nous présentons une structure dynamique avec seulement un transistor de précharge et on fusionne le transistor d'évaluation à l'intérieur du bloc de la fonction

logique. Enfin, le troisième scénario (S3) décrit des cas spécifiques où il est possible de combiner les approches des deux scénarios 1 et 2.

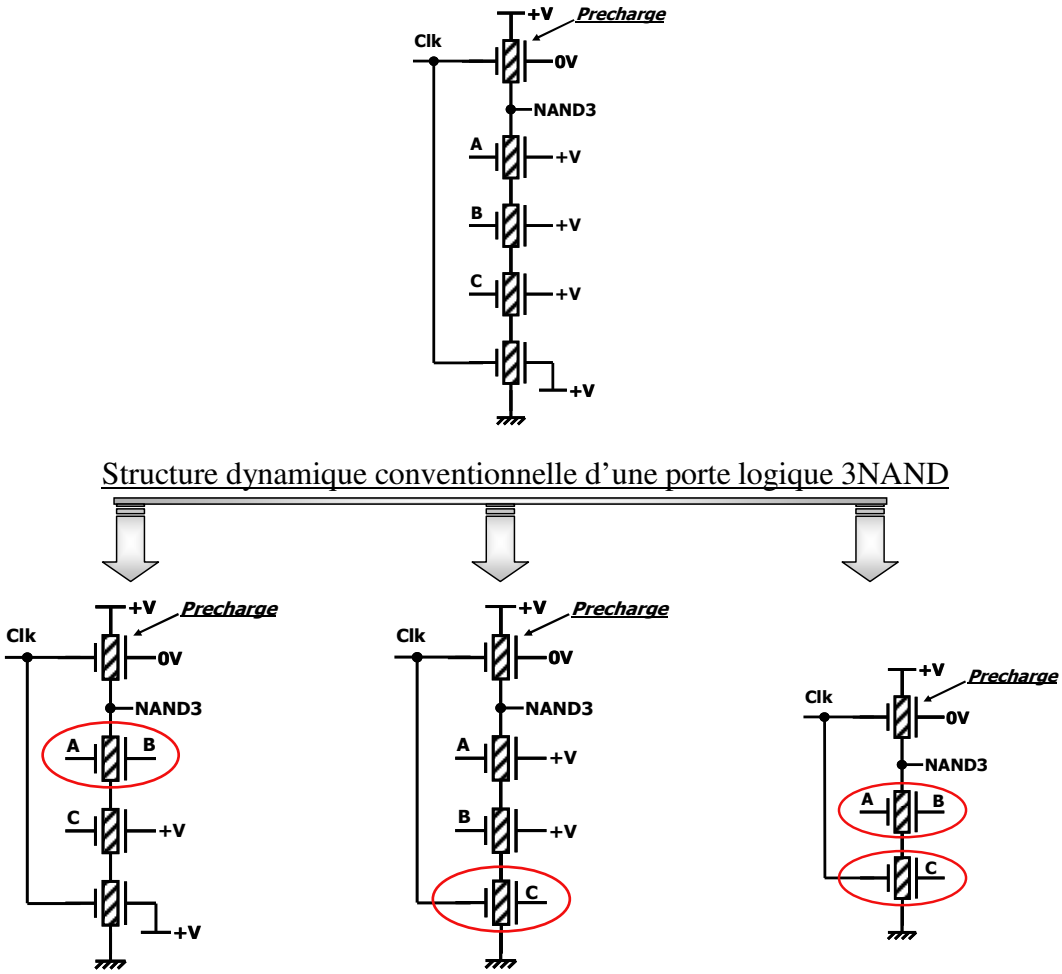


Figure 2-4. Exemple descriptif des 3 scénarios possibles à travers une porte logique 3NAND

Des exemples génériques illustrant les différences entre une structure CMOS classique basée sur la logique dynamique (CDL) et les structure DGDL après l'application de l'approche TTSM, sont montrées aux figures 2-5, 2-6 et 2-7, respectivement pour le scénario 1, scénario 2 et le scénario 3.

2.1.3.1 Scénario 1 (S1): TTSM appliquée à l'intérieur du chemin de la fonction logique

Dans le premier scénario (S1), pour construire une approche générique pour la conception de cellules DGDL, nous appliquons l'approche TTSM dans le bloc de chemin de la fonction tout en conservant les deux transistors de précharge et d'évaluation utilisés dans la logique dynamique conventionnelle (fig. 2-5).

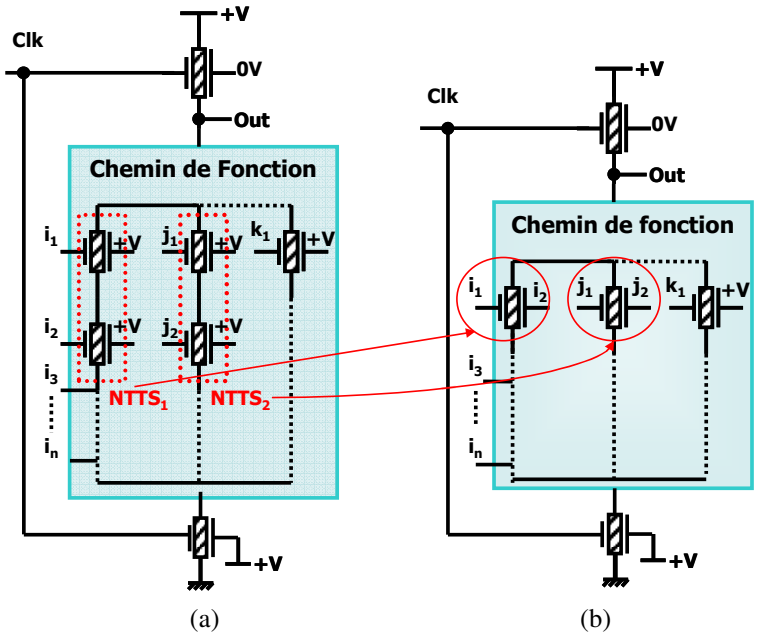


Figure 2-5. structure CDL (a), structure S1-DGDL (b)

2.1.3.2 Scénario 2 (S2): Fusion du transistor d'évaluation avec le chemin de la fonction logique

Dans le deuxième scénario (S2), la structure du chemin de la fonction logique est le même, mais au lieu d'utiliser un transistor d'évaluation on connecte le signal d'évaluation directement aux grilles arrières d'au moins un Am-IDGFET dans chaque branche du chemin de la fonction logique (Fig. 2-6). En fait, tous les transistors du chemin de la fonction logique pourraient être reliés au signal de l'évaluation, ce qui réduirait le courant de fuite mais aussi accroîtrait la charge sur le signal d'horloge d'évaluation.

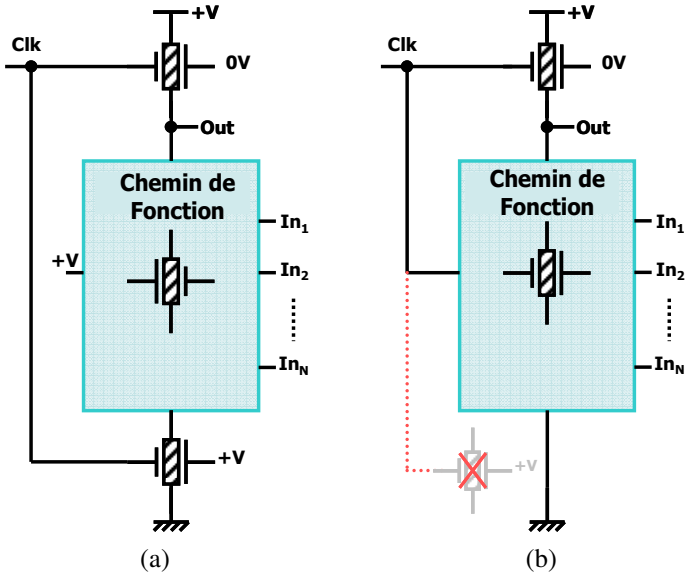


Figure 2-6. structure CDL (a), structure S2-DGDL (b)

2.1.3.3 Scénario 3 (S3): approche TTSM appliquée dans le chemin de la fonction, avec fusion de transistor d'évaluation

Dans le troisième scénario (S3), nous visons à présenter le cas où les deux scénarios 1 et 2 peuvent être fusionnées ensemble pour diminuer d'avantage le nombre de transistors dans les cellules logiques dynamiques (Fig. 2-7).
Ce scénario traite le cas particulier suivant; lorsque le nombre de transistors N_T dans chaque branche-série de chemin de la fonction logique reliant la masse au noeud du sortie est un nombre impair supérieur ou égal à trois ($N_T \geq 3$). Par exemple, dans le cas de la figure 2-7 (a), le chemin de fonction est composé d'une branche de 3 transistors en série, combinés en parallèle avec une branche de 5 transistors en série. En appliquant l'approche TTSM à l'intérieur du chemin de fonction comme dans le scénario 1, trois structures NTTS ont été identifiées et transformées en un seul Am-IDGFET chacune. En outre, nous avons exploité les portes arrières des transistors restants (T_1 et T_2) pour fusionner le transistor d'évaluation et par conséquent réduire davantage le nombre de dispositifs utilisés par l'ensemble de la structure comme dans le scénario 2.

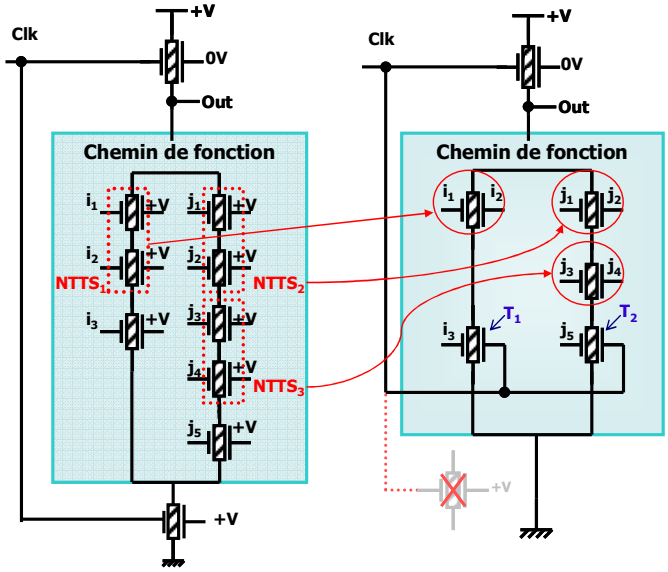


Figure 2-7. structure CDL (a), structure S3-DGDL (b)

2.1.3.4 Comparaison des scénarios

Contrairement à la logique statique complémentaire, l'application de l'approche TTSM à une logique dynamique révèle 3 scénarios différents, conduisant à des gains différents en termes de nombre de transistors, comme le résume le tableau 2-1.
- N: Nombre des entrées de la fonction logique
- m: nombre de structures TTS dans le chemin de fonction

TABLE 2-1. GAIN EN NOMBRE DE TRANSISTORS POUR CHAQUE SCENARIO PAR RAPPORT A LA STRUCTURE DYNAMIQUE CONVENTIONNELLE

Structure logique	Nombre de transistors	Gain
Logique Dynamique Conventionnelle (CDL)	N+2	0
Scénario 1 (S1)	N+2-m	m
Scénario 2 (S2)	N+1	1
Scénario 3 (S3)	N+1-m	m+1

Le gain le plus faible est réalisé par S2 avec un seul transistor. Dans ce scénario, le signal d'horloge est connecté aux grilles arrières des plusieurs transistors, ce qui augmente considérablement la capacité de charge d'horloge et ralentit la réponse du circuit. Cela

engendre aussi d'autres problèmes typiquement liés à l'acheminement complexe des horloges. Scénario S1 offre un gain de transistors m en fonction du nombre de structures TTS dans le chemin de fonction. Scénario S3 offre le meilleur gain (m+1 transistors). Cependant, il ne peut être utilisé dans des cas spécifiques (branches dont le chemin de la fonction logique contient un nombre impair de transistors $N_T \geq 3$). Le pseudo-code suivant décrit comment choisir entre les trois scénarios lors de la construction des portes logiques à partir de l'approche TTSM afin d'obtenir le meilleur bénéfice.
N_T = nombre de transistors dans une branche du chemin de la fonction ($N_T > 0$)
B = nombre de branches dans le chemin de la fonction

```
Pour branche = 1 jusqu'à branche = B
  Si (NT<2) alors utilisez S2  /* Un seul transistor dans le chemin de la
fonction  */
    Sinon
      Si (NT = nombre impair) alors utilisez S3
        Sinon (utilisez S1)
      Fin Si
    Fin Si
  Fin Pour
```

2.2 Technique de conception des circuits logiques à faible consommation à base des les Am-IDGFETs

La consommation totale d'énergie (P_{tot}) est la somme de trois composantes: la puissance statique P_{stat} , la puissance dynamique/active P_{dyn} et la puissance dynamique de court-circuit P_{sc}. Pour abaisser la puissance dynamique, les techniques usuelles sont basées sur la diminution de la tension d'alimentation, des capacités, la réduction de la fréquence et le facteur d'activité de commutation. Dans ce travail, nous proposons une technique supplémentaire à l'aide des Am-IDGFETs, en utilisant la grille arrière pour réduire dynamiquement la puissance de court-circuit pendant le temps de transition des signaux d'entrée. En outre, la technique est capable de réduire la puissance statique.

2.2.1 Réduction de la puissance dynamique

Pour la logique CMOS classique, il a été montré dans [2-56] que le courant de court-circuit peut consommer jusqu'à près de 15% de la puissance totale. Cette composante de la consommation totale est généralement diminuée en utilisant des techniques pour équilibrer le temps de transition (montée et descente) des entrées et de sorties des circuits logiques. Dans notre technique proposée, nous visons à désactiver tous les transistors dans le circuit pendant ce temps de transition afin d'abolir/limiter le courant de court-circuit.

Description de la technique

Au cours de la commutation entre l'état d'équilibre des zones d'opération, un chemin de courant est créé entre l'alimentation V_{dd} et la masse pendant une courte période de temps, directement liée au temps de la montée et de la descente du signal d'entrée. Les deux transistors NMOS et PMOS seront simultanément à l'état ON ; lorsque $V_{THn} < V_{in} < V_{dd} - |V_{THp}|$, comme indiqué dans la Figure 2-8 (a), où nous supposons que $V_{THn} = |V_{THp}| = V_{TH}$, V_{dd} = + V et I_{MAX} est le courant de saturation des transistors P et N qui dépend de leurs tailles, de la technologie de processus, la température, etc

L'idée principale à ce niveau de travail est de forcer les deux transistors NMOS et PMOS à être à l'état OFF pendant les changements sur le signal d'entrée pour éliminer/optimiser le courant de court-circuit comme indiqué dans la Figure 2-8 (c). Une fois que les signaux

d'entrée ont atteint les valeurs de leurs états d'équilibre, des dispositifs sont mis en marche à nouveau et permettent la commutation au niveau du noeud de sortie.

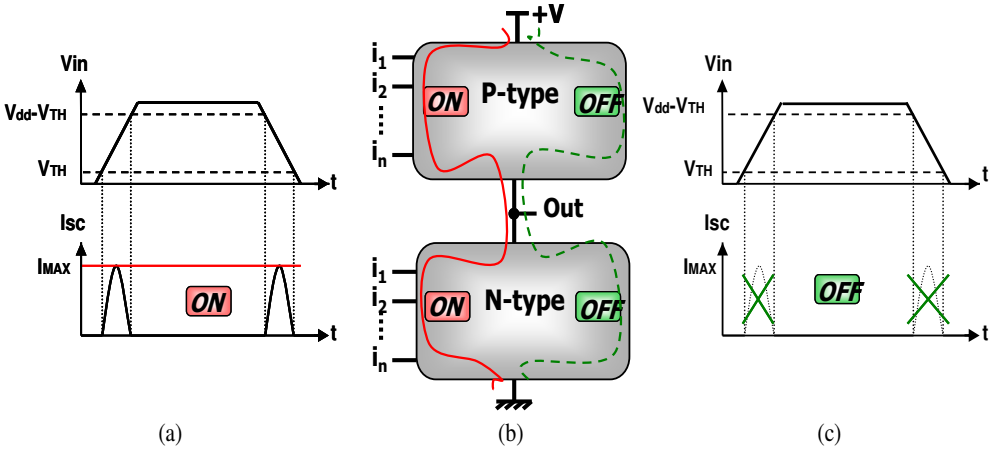


Figure 2-8. Courant de court-circuit quand les deux transistors P/N sont activés(a), Structure logique complémentaire(b) Elimination de court-circuit quand les deux transistors N/P sont éteints (c)

La figure 2-9 montre un exemple générique de l'utilisation des grilles arrière des transistors pour contrôler l'état des dispositifs. Quand les signaux d'entrée sont à l'état des valeurs fixes (« haut » et « bas »), les transistors des blocs logiques « pull-up » et « pull-down » sont configurés P et N, respectivement, et le circuit fonctionne de façon classique. Lors de la commutation du signal d'entrée (transition de 1 → 0 et de 0 → 1), les transistors sont éteints via leurs grilles arrières pour éliminer le court-circuit. Dans le circuit, les grilles avant FG de transistors sont connectées à des entrées de données, tandis que les grilles arrière sont utilisées pour contrôler l'état des transistors. Dans la pratique, cela signifie que deux signaux d'horloge sont utilisés:

- Clk_P est relié à la BG des transistors du réseau « pull-up » (BGP). Lorsque V_{BGP} = +V/2, tous les transistors du réseau « pull-up » sont OFF (pendant les transitions d'entrée), et quand V_{BGP} = 0V, tous les transistors du réseau « pull-up » sont configurés en type P (pendant les états d'entrée stables).
- Clk_N est relié à la BG des transistors du réseau « pull-down » (BGN). Lorsque V_{BGN} = +V/2, tous les transistors du réseau « pull-down » sont OFF (pendant les transitions d'entrée), et quand V_{BGN} = +V, tous les transistors pull-down sont configurés en type N (pendant les états d'entrée stables).

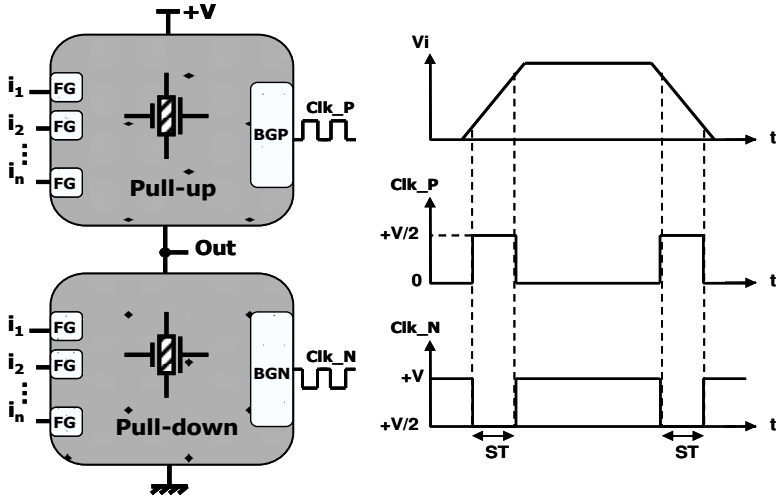


Figure 2-9. Structure des portes logiques à faible consommation d'energie de court-circuit

La largeur d'impulsion d'horloges dépend du temps de montée/descente de signaux d'entrée. Pour démontrer le concept, dans la figure 2-9, nous choisissons une valeur "ST" (temps de commutation) qui est exactement égale à la durée pendant laquelle les deux transistors (N et P sont à l'état ON). En fait la largeur d'impulsion est astreinte à se situer entre ST et T-dt (T période de données d'entrée, dt temps de commutation de la sortie).
La puissance de court-circuit a été estimée à diminuer jusqu'à 6X dans le cas d'un exemple d'un inverseur. Plus de portes logiques sont simulées dans le chapitre 4 de cette thèse.

2.2.2 Réduction de la puissance statique

Pendant le mode veille, nous nous efforçons d'avoir une valeur I_{OFF} aussi basse que possible pour les deux réseaux de transistors (pull-up et pull-down). Certaines techniques conventionnelles utilisent des transistors avec une tension de seuil variable pour réduire la consommation. Partant du même principe, nous visons à utiliser une valeur de tension élevée pour les grilles arrières de transistors de type N (V_{BGN}) et une faible valeur de tension pour les grilles arrières de transistors de type P (V_{BGP}) au cours du mode actif du circuit logique afin d'assurer un courant I_{ON} élevé, et vice-versa pendant le mode veille pour assurer un faible courant I_{OFF} et par conséquent diminuer la puissance statique. Le tableau 2-2 montre les valeurs de tensions de la grille arrière au cours des deux phases de fonctionnement du circuit (mode actif et mode veille). Les valeurs sont choisies pour être les mêmes valeurs que V_{dd} et la masse (à la fois en raison de la disponibilité de ces tensions et à cause de l'optimalité de leur impact).

TABLE 2-2. VALEURS DE LA TESNSION DE LA GRILLE ARRIERE DES TRANSISTORS DURANT LES DEUX MODES DU CIRCUIT

	Actif	Veille
V_{BGN}	+V= 0.9 V	0 V
V_{BGP}	0 V	+V=0.9 V

Les analyses DC d'un inverseur ont montré une diminution de 100X du courant I_{OFF} avec la configuration en mode veille traduite par une diminution de la puissance statique de même facteur 100X. Les mêmes conditions des simulations détaillées dans le chapitre 4 de cette thèse ont été utilisées et plus des portes logiques sont simulées.

2.2.3 Module proposé pour diminuer la puissance totale

Afin d'incorporer les deux techniques de conception à faibles consommations proposées à base des Am-IDGFET, il est nécessaire de contrôler l'action sur les tensions de grille arrière pour diminuer dynamiquement la puissance de court-circuit en mode actif, et la puissance statique pendant le mode veille. Figure 2-10 présente une structure de circuit complète qui permet la mise en oeuvre de deux techniques de conception en utilisant un module de commande pour configurer dynamiquement le bloc du circuit par l'intermédiaire de la grille arrière des transistors au moyen d'une unité simple qui commute entre les deux modes (actif/en veille).

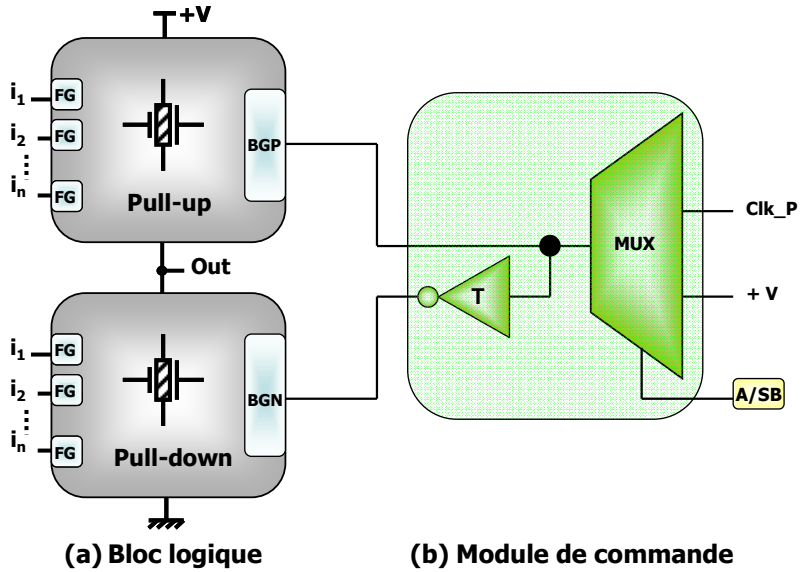


Figure 2-10. Structure dynamique pour des circuits logiques à faible consommation

La sortie du multiplexeur est reliée au réseau des transistors «pull-up» (BGP) et à un inverseur ternaire (T-inverseur). L'inverseur alimente les transistors «pull-down» (BGN) et fonctionne selon {+V → 0V, +V/2 → +V/2, 0V →+V}.
La structure de l'inverseur ternaire utilisée dans le module est présentée dans la Figure 2-11; il est composé de deux transistors et deux résistances de 100kΩ chacune. Cette valeur de résistance est le résultat du compromis au sein d'une plage de valeurs acceptables donnant des marges de bruit ternaires. Une haute valeur de résistance augmente le temps de retard et la surface, tout en diminuant la consommation électrique et de la dépendance de la résistance de canal de l'Am-IDGFET.

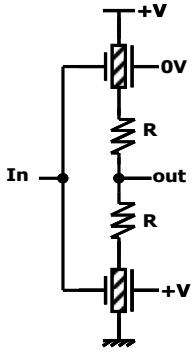


Figure 2-11. Structure de l'inverseur ternaire

Le signal de commande (A/SB) du multiplexeur est utilisé pour basculer entre le mode actif et le mode veille. Pendant le mode actif, Clk_P est selectionné et fournit le signal d'horloge pour inhiber le courant de court-circuit par l'intermédiaire de la grille arrière. Pendant le mode veille, l'entrée +V du multiplexeur est sélectionnée pour diminuer la puissance statique.

2.3 Conclusions

En utilisant les Am-IDGFETs, nous avons décrit deux techniques de conception de circuits. Les deux techniques exploitent la quatrième borne de dispositif pour réaliser un nouveau concept de la conception de portes logiques standards. La première approche (approche TTSM) réduit efficacement le nombre de transistor des cellules logiques selon différents

styles logiques, conduisant à une meilleure densité d'intégration en remplaçant chaque structure des deux transistors en série par un seul Am-IDGFET pour un fonctinnement équivalent. En ce qui concerne le style logique dynamique, nous avons montré comment l'approche TTSM peut être appliquée selon trois scénarios différents, en fonction du nombre de transistors et de leur répartition dans les branches de circuit logique avec 30% moins de transistors. La deuxième approche de conception, présentée dans ce chapitre, traite le problème de la consommation d'énergie sous deux formes (puissance de court-circuit de et puissance statique). On a proposé de commander l'état de transistors en les désactivant au cours des transitions d'entrée via leurs grilles arrières; de manière à diminuer la puissance dynamique (de court-circuit). En outre, nous avons montré que par l'inversion des tensions des grilles arrières pendant le mode veille, le courant de fuite I_{OFF} est réduit par un facteur de 100X. La validation des deux approches de conception et l'évaluation de leurs capacités pour améliorer les performances des cellules standards sont étudiées dans le quatrième chapitre de cette thèse.

Chapitre 3

Techniques de synthèse de la logique reconfigurable basée sur les Am-IDGFETs

Résumé

La synthèse logique est un aspect d'automatisation de la conception électronique (EDA) par lequel une forme abstraite de comportement du circuit désiré est implémentée en portes logiques. En dépit de tous les développements récents de la synthèse logique, les outils actuels ne sont pas en mesure de faire face aux conceptions émergentes. Dans le cas d'Am-IDGFET, les techniques classiques de synthèse logique ne peuvent pas représenter directement la propriété de la reconfigurabilité du dispositif via sa grille arrière comme variable libre. Alors, des nouvelles techniques doivent être trouvées pour construire une logique optimale avec des tels dispositifs. Dans ce chapitre, nous exploitons la classification des fonctions, un outil de construction et l'analyse des fonctions booléennes, afin de construire des blocs logiques reconfigurables en définissant une corrélation hiérarchique entre les structures des classes de fonctions basées sur des dispositifs ambipolaires. Plusieurs cellules logiques à 2 entrées avec une fonctionnalité partielle ou totale sont conçues dans ce chapitre selon deux styles logiques, dynamique et statique.

En outre, les diagrammes de décision binaires (BDDs) ont été utilisés pour décrire une nouvelle méthode de synthèse de la logique reconfigurable avec des dispositifs ambipolaire. Nous proposons un diagramme ambipolaire de décision binaire (AmBDD), en adaptant la technique classique des BDDs aux dispositifs ambipolaires. Nous décrivons comment cette approche offre la possibilité de construire des cellules reconfigurables avec des Am-IDGFETs obtenues à partir d'AmBDD. En utilisant la technique Am-BDD, nous avons conçu une bibliothèque de cellules reconfigurables à 2 entrées avec une fonctionnalité complète et partielle.

3.1 Approche de classification de fonctions pour une logique ambipolaire reconfigurable

Avec n est le nombre de variables d'entrée, il est possible d'obtenir 2^{2^n} fonctions booléennes, dont chacune peut être réalisée en énumérant toutes les combinaisons possibles de valeurs d'entrée et les arrangements de valeurs de sortie. Il existe des approches pour grouper les fonctions selon certaines propriétés bien spécifiques [3-13, 3-14, 3-15, 3-16, 3-17]. Alors toutes les fonctions au sein de cette classe peuvent être générées à partir du même circuit générique [3-18]. Dans notre étude, nous allons utiliser l'approche algébrique pour la classification des fonctions, car c'est l'approche la plus commune et simple utilisé dans la littérature. Elle est abréviée NPN: Négation des variables d'entrée (N), la permutation des variables d'entrée (P) et la négation de la sortie (N).

3.1.1 Les structures correspondantes au chemin de fonction pour chaque classe

Chacune des trois opérations (négation des entrées, permutation des entrées et négation de la sortie) possède sa réalisation équivalente au niveau d'un seul transistor Am-IDGFET grâce ses trois états de commutation (N, P et OFF):

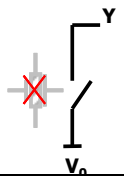
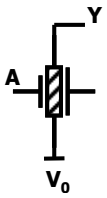
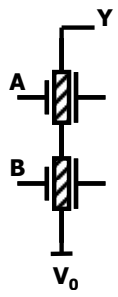
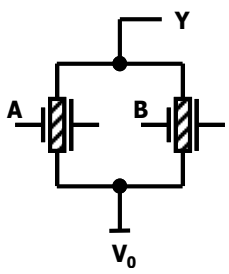
- Négation (complémentation) des entrées: les grilles avants des transistors d'entrées constituant le chemin de la fonction logique ne sont pas complétées (ce qui exigerait un inverseur en plus). L'Am-IDGFET peut être configuré en type P en utilisant la tension

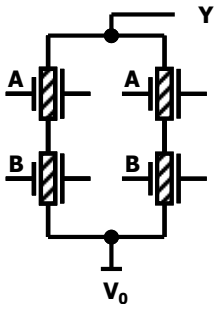
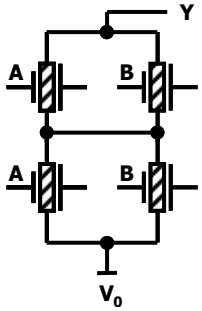
correspondante sur leur grille arrière (i.e. -V). Il en résulte le même effet que si les entrées étaient complémentées.

- Permutation des entrées: l'état OFF du dispositif Am-IDGFET peut être exploitée pour réaliser cette opération de permutation en bloquant le transistor connecté à une entrée.
- Négation (complémentation) de la sortie: cela peut être réalisé au niveau du circuit en plaçant simplement une structure inverseur/suiveur à la sortie Y du chemin de la fonction. Selon la configuration de l'étage inverseur/suiveur, la sortie Y est propagée ou complémentée.

Le tableau ci-dessous (tableau 3-1), décrit le chemin logique de chaque classe de fonctions. Les structures sont génériques, ce qui explique pourquoi la tension grille arrière n'est pas présentée (ceci est utilisé au cours de l'étape de la négation de l'entrée). De même, l'étage inverseur/suiveur à la sortie n'est pas présenté (ceci étant ajouté au cours de l'étape de la négation de sortie). La prochaine étape du travail consiste à déterminer la corrélation entre les différentes structures de classes.

TABLE 3-1. CLASSES DES FONCTIONS A 2 ENTREES ET STRUCTURES DES CIRCUITS GENERIQUES CORRESPONDANTS

<table>
<tr><th>Classe</th><th>Classification NPN</th><th colspan="2">Structure de circuit</th></tr>
<tr><td>1</td><td>T
$\perp$</td><td colspan="2">S1
 
</td></tr>
<tr><td>2</td><td>A
B
$\overline{A}$
$\overline{B}$</td><td colspan="2">S2
 
</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">$\overline{A.B}$
$A.B$
$A.\overline{B}$
$B.\overline{A}$
$\overline{A+B}$
$A+B$
$\overline{A}+B$
$A+\overline{B}$</td><td>Basé-minterm</td><td>Basé-maxterm</td></tr>
<tr><td>S3'
 
</td><td>S3
 
</td></tr>
</table>

4	$A \oplus B$ $\overline{A \oplus B}$	S4′  	S4 

3.1.2 Corrélations hiérarchiques du bas vers le haut entre les structures des classes

A partir des résultats des classes NPN et de leurs structures correspondantes dans le tableau 3-1, on observe clairement que chaque classe a sa propre structure du chemin de fonction. Cependant, des corrélations hiérarchiques peuvent être identifiées à partir du bas vers le haut du tableau.

3.1.2.1 Corrélations hiérarchiques entre les structures maxterm fondées sur (S3, S4)

La couverture de S4: À partir du bas de tableau1-3 et en utilisant les structures maxterms, on peut considérer que la structure S4 contient des doublons de la structure S3. Cela signifie que toutes les fonctions de la classe 3 peuvent être mis en œuvre avec S4 structure. En outre, S4 peut réaliser toutes les fonctions de la classe 2, puisqu'on peut bloquer les transistors reliés à l'entrée inutilisée et d'exploiter celles liées à l'entrée utilisée (par exemple éteindre transistors avec l'entrée B sur leurs grilles d'entrées et exploiter les autres pour réaliser la fonction A). Enfin, quand tous les transistors de la structure S4 sont configurés à l'état OFF, les fonctions de la classe 1 sont obtenues.
Ainsi, nous pouvons écrire: S3 $\subset$S4, S2 $\subset$S4 et S1 $\subset$S4, ce qui signifie que la structure S4 peut réaliser l'ensemble des 16 fonctions.
La couverture S3: La structure S3 peut atteindre les fonctions de la classe 2 en bloquant un seul transistor. Aussi, quand tous les transistors de la structure sont à l'état bloqué, les fonctions de la classe 1 sont obtenues. Ainsi, nous pouvons écrire: S2 $\subset$S3 et S1 $\subset$S3, ce qui signifie que les la structure S3 est capable de réaliser 14 fonctions (l'ensemble des fonctions, sauf celles de la classe 4, XOR/XNOR).
La couverture S2: La structure S2 peut réaliser 4 fonctions (2 fonctions de la classe 1 et 2 fonctions de la classe 2).
De la même manière, nous pouvons identifier les corrélations de couverture basées sur des structures minterms (S3', S4') et même des corrélations entre les structures maxterms et minterms.

3.1.2.2 Corrélations hiérarchiques entre les structures maxterms et minterms

En utilisant la structure maxterm, nous pouvons aller plus loin pour construire des cellules reconfigurables plus compacts en utilisant un seul stage logique (celui de chemin de la fonction) sans mettre en cascade un étage inverseur/suiveur. Un ensemble de 15 fonctions peut être réalisé (sauf pour la fonction «vraie» - inconditionnelle "1").
En fait, S4 peut atteindre les deux fonctions de classe 3, car il est un produit de deux maxterms et chaque transistor est reconfigurable. Par conséquent, les fonctions basées-maxterm de la classe 3 ($A \vee (\neg B)$, $(\neg A) \vee B$, $(\neg A) \vee (\neg B)$, $A \vee B$) sont directement mappés en dupliquant la même configuration de transistors utilisée pour S3 . En ce qui concerne les

fonctions basées sur les mintermes de la même classe 3 (A∧(¬B), (¬A)∧B, (¬A)∧(¬B), A∧B), nous pouvons simplement éteindre deux transistors de la structure S4, dont l'un doit avoir la grille d'entrée connectée à la première entrée (A dans ce cas), et dont l'autre doit avoir la grille d'entrée connectée à la seconde entrée (B dans ce cas). De cette façon, nous obtenons la même structure S3'comme indiqué dans la figure 3-1 (ligne pointillée verte). Pour réaliser les fonctions des classes 2 et 1, nous pouvons bloquer les deux transistors connectés à une entrée identique, et configurer les deux autres en type N ou en type P. Par exemple, la fonction (¬A) peut être obtenue en bloquant les transistors ayant l'entrée B sur leur grille avant, et configurer les autres en type N. Enfin, quand tous les transistors de la structure S4 sont configurés à l'état OFF, la fonction "faux" ou "0" de la classe 1 est achevée. La seule fonction manquante est la fonction "vraie" (inconditionnelle "1").
En supposant que chaque transistor peut avoir l'un des trois états (P, N et OFF), la figure 3-1 montre la présence des différentes structures de classes au sein de la structure S4. S1 n'est pas présentée dans la figure puisque cette structure est réalisée en mettant tous les transistors à l'état OFF.

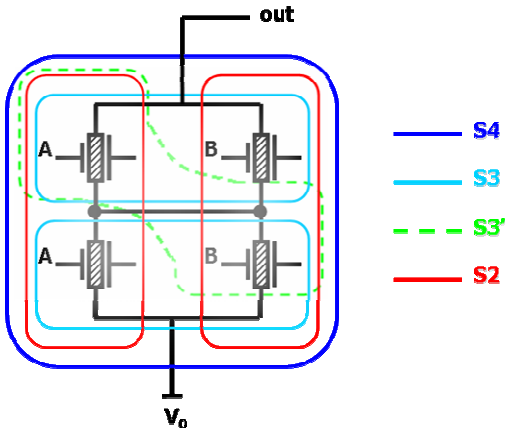


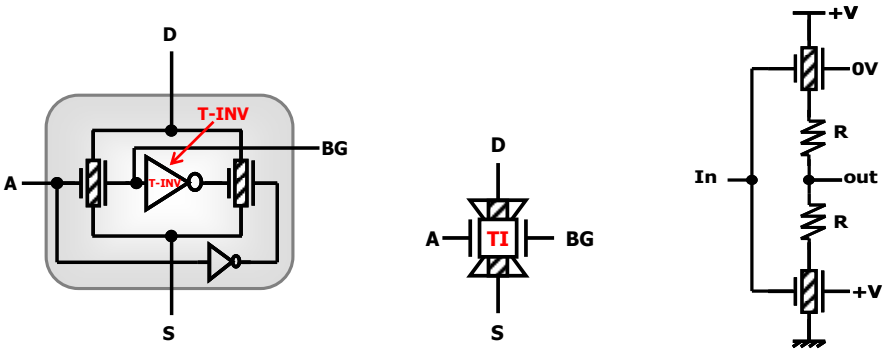
Figure 3-1. Capabilité de la classe S4 d'exprimer les structures des autres classes

3.1.3 Bibliothèque de cellules logiques dynamiquement reconfigurables

Dans cette section, nous appliquons l'approche en décrivant une bibliothèque de cellules dynamiquement reconfigurables basées sur les structures de classes avec des détails sur leur configuration et leur système d'horloge. Afin de fonder cette approche sur des structures physiques vérifiables, nous commençons cette section par la description d'un bloc logique qui sera utilisé pour la conception de toutes les cellules reconfigurables dans ce travail.

3.1.3.1 Porte logique de transmission basée sur les Am-IDGFETs

La cellule reconfigurable, basée sur la logique dynamique, nécessite l'utilisation d'un réseau de portes logiques de transmission pour propager les niveaux logiques sans dégradation et pour avoir une gamme plus large de tension de données et de commande. Nous utilisons une porte logique de transmission formée par deux Am-IDGFETs en parallèle commandés par des signaux complémentaires, pour les données sur la grille avant et la grille arrière comme indiqué dans la figure 3-2 (a). Tandis que les données d'entrée (grille avant) représentent un signal binaire (donc la complémentarité nécessite un simple inverseur), le contrôle (grille arrière) est un signal ternaire et nécessite un inverseur ternaire (T-INV). La structure de la porte logique de transmission qui permet la commutation entre les trois états (N, P et OFF) est représentée sur la figure 3-2 (a) et est abrégé "TI" dans le symbole indiqué à la figure 3-2 (b).



(a) (b) (c)

Figure 3-2. Porte logique de transmission basée sur les Am-IDGFETs: structure (a), symbole (b), (c) structure T-INV

Le T-INV contrôle la grille arrière du dispositif Am-IDGFET et fonctionne selon {+V → 0V, +V/2 → +V/2, 0V → +V}. La structure de la T-INV est représentée sur la figure 3-2; elle est composée de deux transistors et deux résistances de 100kΩ chacune. Cette valeur est le résultat de compromis au sein d'une plage de valeurs acceptables donnant des marges de bruit ternaires.

3.1.3.2 Cellules dynamiquement reconfigurables en logique dynamique

Les structures génériques de cellules reconfigurables correspondant à chaque classe a été présenté dans le tableau 3-1, en supposant que chaque transistor dans le chemin de fonction peut être configurée selon l'un des trois états (N, P, ou OFF). Dans cette section, nous décrivons 4 différentes reconfigurables cellules logiques dynamiques appliquant l'approche des classes de fonctions et utilisant la structure de la porte logique de transmission décrite précédemment.

a. *Cellules reconfigurables à 2 étages*

Dans le tableau 3-2, nous avons présenté et détaillé quatre classes de fonctions à 2 entrées. Ici, nous présentons deux cellules logiques dynamiquement reconfigurables issus de tableau 3-2. La première cellule réalise l'ensemble des 16 fonctions et représente la classe 4 dans le tableau. La seconde, avec moins de transistors, dispose de 14 fonctions et représente la classe 3 dans le tableau. Les deux cellules sont composées de 2 étages: étage de la fonction logique et étage inverseur/suiveur.

- *Cellules reconfigurables à fonctionnalité complète*

La figure 3-3 montre une cellule dynamiquement reconfigurable basée sur la forme somme des produits (SOP) et abrégée SOP-DRLC. Structures TI1 et TI2 du chemin de fonction sont placées en série pour former un premier minterme (ET câblé), tandis TI3 et TI4 forme un second minterme. Les deux structures sont connectées en parallèle (OU câblé) pour permettre l'utilisation potentielle de la somme des deux mintermes. La reconfiguration de la cellule est assuré à l'aide des tensions des grilles arrières $bg_{\{1\text{-}5\}}$ (dont chacun peut prendre l'un des trois niveaux de tension: 0V, V/2 ou + V. Les signaux d'entrée sont les deux entrées booléennes A et B, tandis PC1, EV1, PC2 et EV2 représentent les signaux d'horloge (PC pour precharge et EV pour évaluation). La cellule peut être configurée pour réaliser une de 16 fonctions indiquées dans le tableau 3-2.

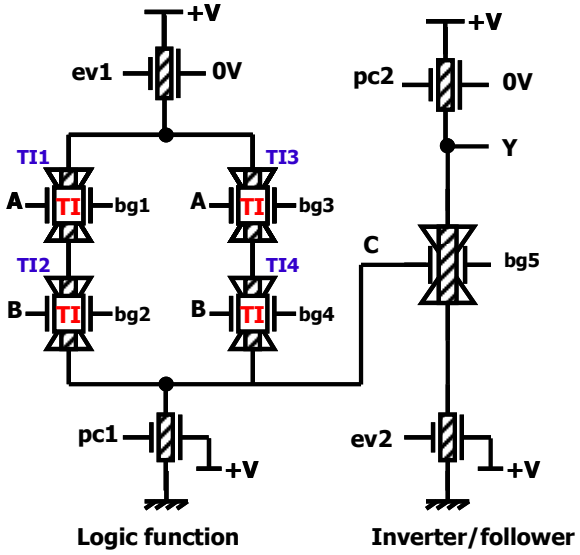


Figure 3-3. Cellule logique dynamiquement reconfigurable SOP-DRLC

TABLE 3-2. TABLEAU DE CONFIGURATION DE LA CELLULE SOP-DRLC

bg1=bg2	bg3	bg4	bg5	Y
V/2	0V	0V	0V	$\overline{A+B}$
V/2	0V	0V	+V	$A+B$
V/2	+V	0V	+V	$\overline{A}+B$
V/2	0V	+V	+V	$\overline{B}+A$
V/2	0V	+V	0V	$\overline{A}\bullet B$
V/2	+V	0V	0V	$\overline{B}\bullet A$
V/2	+V	+V	0V	$A\bullet B$
V/2	+V	+V	+V	$\overline{A\bullet B}$
+V	0V	+V	+V	$\overline{B}$
+V	0V	+V	0V	B
+V	+V	0V	0V	A
+V	+V	0V	+V	$\overline{A}$
0V	+V	+V	0V	$\overline{A\oplus B}$
0V	+V	+V	+V	$A\oplus B$
V/2	V/2	V/2	0V	$\perp$
V/2	V/2	V/2	+V	T

- *Cellules reconfigurables à fonctionnalité partielle*

La cellule précédente SOP-DRLC était une mise en œuvre de la structure logique de la classe 4 du tableau 3-1. La cellule peut réaliser l'ensemble de 16 fonctions. Dans cette section, nous montrons qu'il est également possible de construire des cellules reconfigurables avec des fonctionnalités partielles et nécessitant moins de transistors en utilisant d'autres classes. Nous utilisons la structure générique S3 du tableau 3-1 pour concevoir une cellule logique avec 14 fonctions possibles à la sortie. Cette cellule (fig. 3-4) est composée de deux étapes logiques (fonction logique et inverseur/suiveur) et peut être configuré selon le tableau de 3-3.

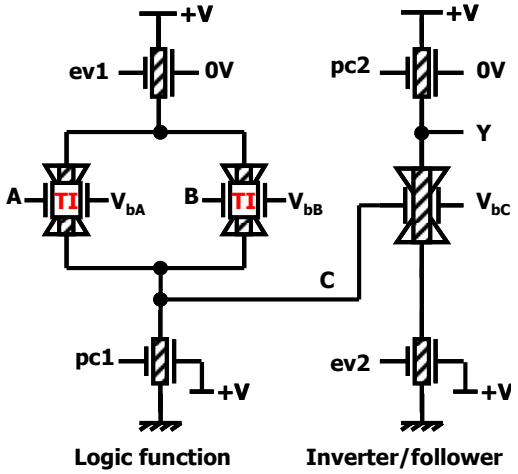


Figure 3-4. Cellule logique dynamiquement reconfigurable (DRLC-7T) [25]

TABLE 3-3. TABLEAU DE CONFIGURATION DE LA CELLULE LOGIQUE DRLC-7T

V_{bA}	V_{bB}	V_{bC}	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	0V	$A+B$
+V	V/2	+V	$\overline{A}$
+V	V/2	0V	A
0V	0V	+V	$A\bullet B$
0V	0V	0V	$\overline{A\bullet B}$
+V	0V	+V	$B\bullet\overline{A}$
+V	0V	0V	$A+\overline{B}$
V/2	+V	+V	$\overline{B}$
V/2	+V	0V	B
V/2	V/2	V/2	T
V/2	V/2	0V	$\perp$
0V	+V	+V	$A\bullet\overline{B}$
0V	+V	0V	$\overline{A}+B$
INACCESSIBLE			$\overline{A\oplus B}$
INACCESSIBLE			$A\oplus B$

b. *Cellule reconfigurable à un seul stage logique*

Cette cellule à 2 entrées utilise un seul stage logique (sans cascader un étage inverseur/suiveur) et réalise l'ensemble de 16 fonctions logiques (sauf la fonction «vrai», ou inconditionnel "1") en exploitant la possibilité d'exprimer une fonction en tant que produit de sommes (POS) ou somme de produits (POS) (promouvoir la forme qui nécessite un nombre moindre de transistor) en utilisant le même circuit. Figure 3-5 illustre l'implémentation au niveau transistor de la cellule logique dynamiquement reconfigurable abréviée SS-DRLC. La cellule peut ainsi être configurée en 15 opérations binaires (tableau 3-4).

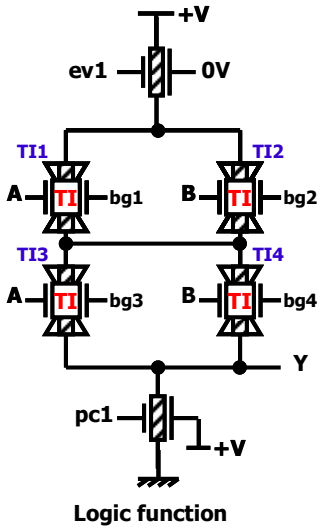


Figure 3-5. Cellule logique dynamiquement reconfigurable à un seul étage SS-DRLC

TABLE 3-4. TABLEAU DE CONFIGURATION DE LA CELLULE LOGIQUE SS-DRLC

bg1	bg2	bg3	bg4	Y
0V	V/2	V/2	0V	$\overline{A+B}$
+V	+V	+V	+V	$A+B$
0V	+V	0V	+V	$\overline{A}+B$
+V	0V	+V	0V	$\overline{B}+A$
0V	V/2	V/2	+V	$\overline{A}\bullet B$
+V	V/2	V/2	0V	$\overline{B}\bullet A$
+V	V/2	V/2	+V	$A\bullet B$
0V	0V	0V	0V	$\overline{A\bullet B}$
V/2	0V	V/2	0V	$\overline{B}$
V/2	+V	V/2	+V	B
+V	V/2	+V	V/2	A
0V	V/2	0V	V/2	$\overline{A}$
+V	0V	0V	+V	$\overline{A\oplus B}$
+V	+V	0V	0V	$A\oplus B$
V/2	V/2	V/2	V/2	$\perp$
INACCESSIBLE				T

3.1.3.3 Cellule dynamiquement reconfigurable en logique statique

La structure dynamique décrite précédemment démontre une flexibilité intéressante pour basculer entre OU câblé et ET câblé. Dans cette section, nous en dérivons une cellule en logique statique, en dupliquant le réseau de pull-up pour réaliser une logique statique complémentaire composée des réseaux de transistors pull-up et pull-down. Figure 3-6 illustre l'implementation au niveau transistor de la cellule logique statique complémentaire dynamiquement reconfigurable abréviée CSL-DRLC. La cellule peut ainsi réaliser 14 opérations binaires (tableau 3-5). Les fonctions «vrai» et «faux» sont manquantes.

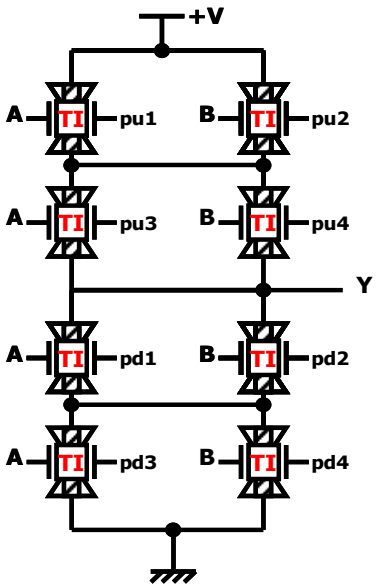


Figure 3-6. Cellule logique dynamiquement reconfigurable en logique statique complémentaire CSL-DRLC

TABLE 3-5. TABLEAU DE CONFIGURATION DE LA CELLULE LOGIQUE CSL-DRLC

pu1	pu2	pu3	pu4	pd1	pd2	pd3	pd4	Y
0V	V/2	V/2	0V	+V	+V	+V	+V	$\overline{A+B}$
+V	+V	+V	+V	0V	V/2	V/2	0	$A+B$
0V	+V	0V	+V	+V	V/2	V/2	0V	$\overline{A}+B$
+V	0V	+V	0V	0V	V/2	V/2	+V	$\overline{B}+A$
0V	V/2	V/2	+V	+V	0V	+V	0V	$\overline{A}\bullet B$
+V	V/2	V/2	0V	0V	+V	0V	+V	$\overline{B}\bullet A$
+V	V/2	V/2	+V	0V	0V	0V	0V	$A\bullet B$
0V	0V	0V	0V	+V	V/2	V/2	+V	$\overline{A\bullet B}$
V/2	0V	V/2	0V	V/2	+V	V/2	+V	$\overline{B}$
V/2	+V	V/2	+V	V/2	0V	V/2	0V	B
+V	V/2	+V	V/2	0V	V/2	0V	V/2	A
0V	V/2	0V	V/2	+V	V/2	+V	V/2	$\overline{A}$
0V	0V	+V	+V	+V	0V	0V	+V	$\overline{A\oplus B}$
+V	0V	0V	+V	0V	0V	+V	+V	$A\oplus B$
INACCESSIBLE								$\perp$
INACCESSIBLE								T

3.2 Diagramme ambipolaire de décision binaire (AmBDD)

Dans cette section, nous explorons l'utilisation des BDDs dans le contexte de la reconfiguration à l'aide des dispositifs Am-IDGFETs. Les BDD classiques, développés pour les transistors unipolaires à trois terminaux, ne peuvent pas être appliqués directement dans le cas d'Am-IDGFET, donc ils doivent être revisés. Nous abordons deux questions principales: (i) comment adapter les BDDs pour représenter le terminal supplémentaire (la grille arrière) et les 3 états de commutations (N, P, OFF) et (ii) comment adapter les BDDs pour représenter la dimension supplémentaire de la reconfigurabilité dans les réseaux de transistors.

3.2.1 BDDs à base des Am-IDGFET pour générer des cellules logiques reconfigurables

Afin d'adapter la technique des BDD au dispositif Am-IDGFET, nous considérons d'abord ses impacts spécifiques sur la représentation des BDDs classiques. Tout d'abord, un nœud peut avoir plus de deux arêtes en fonction des fonctions réalisables à la sortie, d'autre part, une même arête peut prendre des valeurs différentes et, troisièmement, de multiples fonctions puissent être mappé sur le même BDD en partageant la même sortie. Toutes ces considérations sont intégrées dans une méthodologie de conception pour les cellules reconfigurables à n entrées. Les étapes de la méthode proposée sont les suivants:

```
Etape 1
Définir l'ensemble des fonctions à réaliser à la sortie
Etape 2
Tracer les BDDs de toutes les fonctions dans un seul BDD(pour identifier
les noeuds et les arêtes en commun) /* Ce BDD commun pour toutes les
fonctions est abrévié AmBDD (BDD ambipolaire). Toutes les variables
apparaissent dans le même ordre sur tous les chemins depuis la racine vers
les nœuds terminaux. */
Etape 3
Dénommer chaque arête connectant deux noeuds différents dans l'AmBDD.
```

Etape 4
Définir les règles à respecter avant d'implémenter l'AmBDD au niveau transistor. Les arêtes représentées dans l'AmBDD seront présentées en tant que transistors au niveau circuit selon les règles suivantes:

1. *Si une arête est utilisée par toutes les fonctions dans un AmBDD Alors :*
   a. *Si la valeur de l'arête est la même pour toutes les fonctions, le transistor qui présentera cette arête n'a pas besoin d'être reconfigurable.*
   b. *S'il y a une différence entre les valeurs de l'arête, le transistor qui présentera cette arête est reconfigurable, et sera soit de type N soit de type P au niveau circuit.*
2. *Si une arête n'est pas utilisée par toutes les fonctions dans l'AmBDD, alors le transistor qui présentera cette arête est reconfigurable au niveau circuit et dois inclure l'état OFF.*

Etape 5
Tracer le tableau de configuration et identifier les corrélations. /* le tableau contient toutes les fonctions avec les valeurs correspondantes de leurs arêtes. Une corrélation puisse exister entre les valeurs des arêtes.
Etape 6
Implémenter l'AmBDD au niveau transistor /* une valeur '0' de l'arête signifie que le transistor correspondant est configuré en type P (BG=0), tandis qu'une valeur '1' de l'arête signifie que le transistor correspondent est configuré en type N(BG=+V). Si une arête est inutilisée par une fonction, le transistor correspondent sera à l'état OFF. */

3.2.2 Cellules logiques reconfigurables à 2 entrées, générés à partir des AmBDDs

Dans cette section, nous appliquons la technique Am-BDD à plusieurs exemples de cellules reconfigurables à 2 entrées. Nous allons tout d'abord introduire un exemple qui cible de réaliser une cellule reconfigurable à 2 entrées capable de réaliser la totalité des 16 fonctions possibles. Ensuite, deux autres cellules avec une fonctionnalité partielle ont été dérivées à partie de l'AmBDD originale correspondant aux 16 fonctions possibles.

3.2.2.1 Cellule reconfigurable à 16 fonctions (16F-AmBDD)

La structure générale de l'AmBDD visant à réaliser les 16 fonctions différentes est montrée dans la figure 3-7 avec un ordre de variables (A, B). Les valeurs correspondantes des signaux de configuration pour chaque arête sont présentées dans le tableau 3-6. Figure 3-8 représente la mise en oeuvre de circuit finale de la cellule reconfigurable à 2 entrées abréviée 16F-AmBDD.

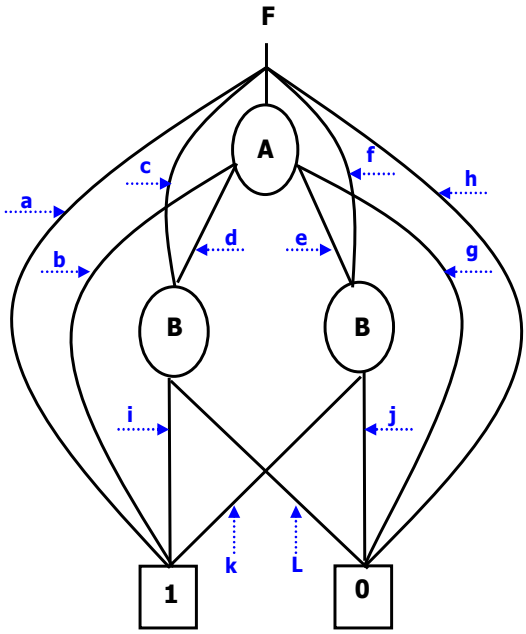


Figure 3-7. Am-BDD d'une cellule reconfigurable à 2 entrées

TABLE 3-6. TABLEAU DE CONFIGURATION POUR LES 16 FONCTIONS

a	b	c	d	e	f	g	h	i	j	k	l	F
V/2	V/2	V/2	0V	V/2	V/2	+V	V/2	0V	V/2	V/2	+V	$\overline{A+B}$
V/2	+V	V/2	V/2	0V	V/2	V/2	V/2	V/2	0V	+V	V/2	$A+B$
V/2	0V	V/2	V/2	+V	V/2	V/2	V/2	V/2	0V	+V	V/2	$\overline{A}+B$
V/2	V/2	V/2	+V	V/2	V/2	0V	V/2	0V	V/2	V/2	+V	$A\bullet\overline{B}$
V/2	+V	V/2	0V	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	$A+\overline{B}$
V/2	V/2	V/2	V/2	0V	V/2	+V	V/2	V/2	0V	+V	V/2	$B\bullet\overline{A}$
0V	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	V/2	T
V/2	V/2	V/2	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	V/2	$\perp$
V/2	V/2	V/2	V/2	+V	V/2	0V	V/2	V/2	0V	+V	V/2	$A\bullet B$
V/2	0V	V/2	+V	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	$\overline{A\bullet B}$
V/2	+V	V/2	V/2	V/2	V/2	0V	V/2	V/2	V/2	V/2	V/2	A
V/2	0V	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	V/2	V/2	$\overline{A}$
V/2	V/2	+V	V/2	V/2	V/2	V/2	V/2	0V	V/2	V/2	+V	$\overline{B}$
V/2	V/2	V/2	V/2	V/2	+V	V/2	V/2	V/2	0V	+V	V/2	B
V/2	V/2	V/2	0V	+V	V/2	V/2	V/2	0V	0V	+V	+V	$\overline{A\oplus B}$
V/2	V/2	V/2	+V	0V	V/2	V/2	V/2	0V	0V	+V	+V	$A\oplus B$

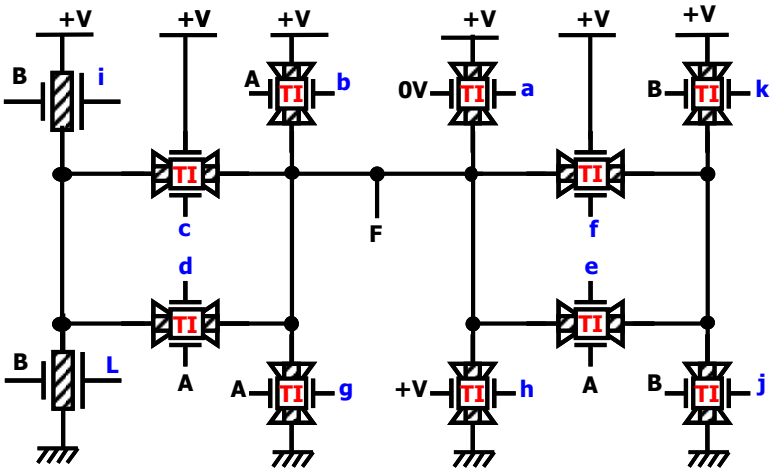


Figure 3-8. Schéma du circuit logique de la cellule logique 16F-AmBDD

3.2.2.2 Cellules reconfigurables à 2 entrées à fonctionnalité partielle

Le problème principal de la cellule 16F-AmBDD est le nombre élevé de signaux de configuration, ce qui peut conduire, au niveau architectural, à une utilisation intensive des interconnexions et des ressources mémoire induisant une augmentation conséquente de la consommation d'énergie, des retards et de la surface. Dans cette section, à partir de schéma complet de l'AmBDD dans la figure 3-7 et le tableau de configuration correspondant, nous construisons des cellules logiques reconfigurables avec des fonctionnalités partielle et qui requièrent par conséquent moins de transistors et des signaux de configuration.
Nous introduisons deux cellules reconfigurables réalisant deux ensembles de fonctions différents. Dans la figure 3-9, la première cellule (abréviée 12F-AmBDD) utilise une structure plus compacte avec moins de transistors et est capable d'achever 12 fonctions (hormis T, ⌐ B, B et ⊥ de l'ensemble complet) selon le tableau de configuration 3-7. La deuxième cellule (abréviée 6F-AmBDD) est une cellule encore plus compacte (figure 3-10), mais ne peut générer que 6 fonctions logiques élémentaires selon le tableau de configuration 3-8.

TABLE 3-7. TABLEAU DE CONFIGURATION DE LA CELLULE 12F-AMBDD

b	d	e	g	i	j	k	l	F
V/2	0V	V/2	+V	0V	V/2	V/2	+V	$\overline{A+B}$
+V	V/2	0V	V/2	V/2	0V	+V	V/2	$A+B$
0V	V/2	+V	V/2	V/2	0V	+V	V/2	$\overline{A}+B$
V/2	+V	V/2	0V	0V	V/2	V/2	+V	$A\bullet\overline{B}$
+V	0V	V/2	V/2	0V	V/2	V/2	+V	$A+\overline{B}$
V/2	V/2	0V	+V	V/2	0V	+V	V/2	$B\bullet\overline{A}$
V/2	V/2	+V	0V	V/2	0V	+V	V/2	$A\bullet B$
0V	+V	V/2	V/2	0V	V/2	V/2	+V	$\overline{A\bullet B}$
+V	V/2	V/2	0V	V/2	V/2	V/2	V/2	A
0V	V/2	V/2	+V	V/2	V/2	V/2	V/2	$\overline{A}$
V/2	0V	+V	V/2	0V	0V	+V	+V	$\overline{A\oplus B}$
V/2	+V	0V	V/2	0V	0V	+V	+V	$A\oplus B$

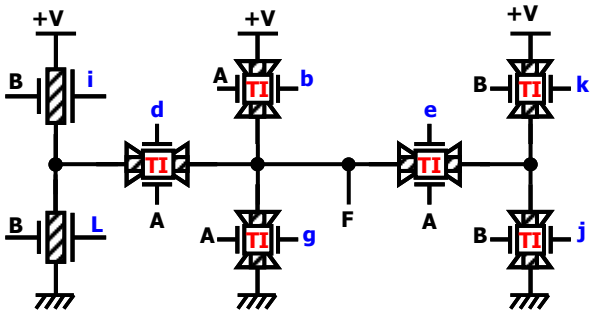


Figure 3-9. Schéma de la cellule logique 12F-AmBDD

TABLE 3-8. TABLEAU DE CONFIGURATION DE LA CELLULE 6F-AMBDD

b	d	g	i	l	F
V/2	0V	+V	0V	+V	$\overline{A+B}$
V/2	+V	0V	0V	+V	$A\bullet\overline{B}$
+V	0V	V/2	0V	+V	$A+\overline{B}$
0V	+V	V/2	0V	+V	$\overline{A\bullet B}$
+V	V/2	0V	V/2	V/2	A
0V	V/2	+V	V/2	V/2	$\overline{A}$

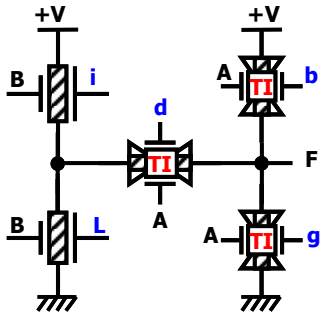


Figure 3-10. Schéma de la cellule logique 6F-AmBDD

3.3 Conclusions

L'Am-IDGFET, représente une nouvelle classe de dispositifs capables de fonctionner comme des transistors de type N ou P en fonction de la tension appliquée à leurs grilles arrières, nous avons défini deux techniques de synthèse de la logique reconfigurable. Nous avons premièrement étudié le concept de classification des fonctions qui représente un outil puissant pour la construction et l'analyse des fonctions booléennes. Nous avons exploité cet outil classique pour construire des blocs logiques reconfigurables en définissant une corrélation hiérarchique entre les structures de classes. Une bibliothèque de cellules logiques dynamiques a été construite en utilisant cette méthode, ainsi qu'une cellule logique statique. En outre, dans le même contexte de techniques de synthèse logique, nous avons proposé un diagramme ambipolaire de décision binaire AmBDD, en adaptant la synthèse logique conventionnelle BDD aux dispositifs Am-IDGFETs. En utilisant la technique Am-BDD, nous avons conçu une cellule reconfigurable à 2 entrées capable de réaliser 16 fonctions et nous avons dérivé des cellules plus compactes avec des fonctionnalités partielles. Lors de l'implémentation au niveau du transistor, nous avons utilisé des portes logiques de transmission à base des Am-IDGFETs comme solution pour éviter la dégradation logique et assurer le bon fonctionnement.

Chapitre 4

Validation et évaluation des méthodologies et techniques de conceptions

4.1 Introduction

Ce chapitre présente une validation et évaluation de l'ensemble des nouvelles approches décrites dans les chapitres 2 et 3 pour concevoir des circuits logiques avec les Am-IDGFETs. Quand il s'agit de l'évaluation des différentes métriques de performances électriques, le modèle du dispositif est d'une importance primordiale. Ce travail peut être réalisé avec tout type d'Am-IDGFET, mais nous choisissons de valider nos circuits générés avec un dispositif DG-CNTFET décrit au début de ce chapitre utilisant le modèle le plus précis dans la littérature. Basés sur un modèle bien décrit, nous validons avec des simulations électriques précises l'ensemble de circuits logiques générés à partir de toutes les théories de conception décrites dans cette thèse:

- L'approche TTSM et la technique de conception à faible consommation pour les cellules standards telles qu'elles étaient décrites dans le chapitre 2
- La technique des AmBDDs et l'approche de classification des fonctions pour les cellules reconfigurables comme elles étaient décrites dans le chapitre 3

4.2 Hypothèses technologiques et modélisation de DG-CNTFET

Les hypothèses technologiques et le modèle physique compact de dispositif DG-CNTFET sont détaillés dans cette section. Récemment, dans [4-6] CEA-LETI a proposé, dans le cadre du projet nanograin, une structure DG-CNTFET avec une grille avant et une grille arrière. Afin d'assurer l'unicité de contrôle, le procédé de fabrication est basé sur la technologie Silicium-Sur-Isolant (SOI- Silicon-On-Insulator). Il est en effet possible avec cette technologie de fabriquer des îlots de silicium entourés d'oxyde. Ces îlots seront les grilles arrière des composants DG-CNFET et seront du fait isolés des autres. Les îlots de silicium peuvent être fortement dopés ou siliciurés afin d'assurer une bonne conductivité de l'électrode. L'oxyde de grille arrière est réalisé par une couche de SiO_2 dont le dépôt précède le transfert de nanotubes de carbone intrinsèques. Enfin, l'oxyde de grille avant (HfO_2) et le métal de grille (Al) avant sont déposés et structurés. Finalement, les contacts des grilles, de source et de drain sont réalisés par gravure et dépôt de métal. Le composant ainsi obtenu est présenté par la figure 4-1.

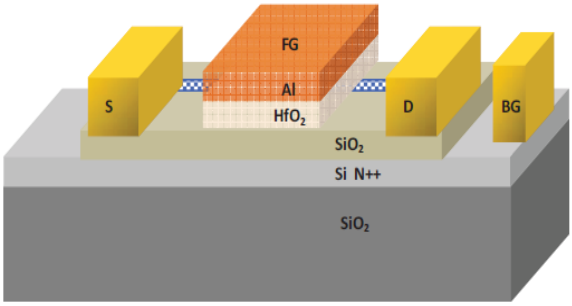


Figure 4-1. Vue d'artiste d'un composant DG-CNFET utilisant le procédé de fabrication proposé et montrant les contacts de source (S), drain (D) et gilles avant- (FG) et arrière (BG) [4-6]

Un modèle compact utile doit permettre la détermination des paramètres aux bornes du dispositif à partir des mesures (ou des simulations électriques de dispositif). Récemment, un

modèle précis a été présenté dans [4-13]. Il représente le premier modèle physique d'un DG-CNTFET avec une bonne précision, une convergence efficace et une vitesse de simulation compatible avec la conception de circuits. Pour les portes CMOS, nous avons utilisé un modèle CMOS 16nm et nous avons calibré la largeur des transistors pour des comparaisons plus réalistes et justes en terme du courant I_{ON}. La figure 4-2 montre les caractéristiques I_{DS}/V_{FGS} du modèle DG-CNTFET et du modèle CMOS 16nm, pour un transistor de type N, où V_{FGS} varie entre 0V et 0.9V, V_D=0.9V et V_S=0V.

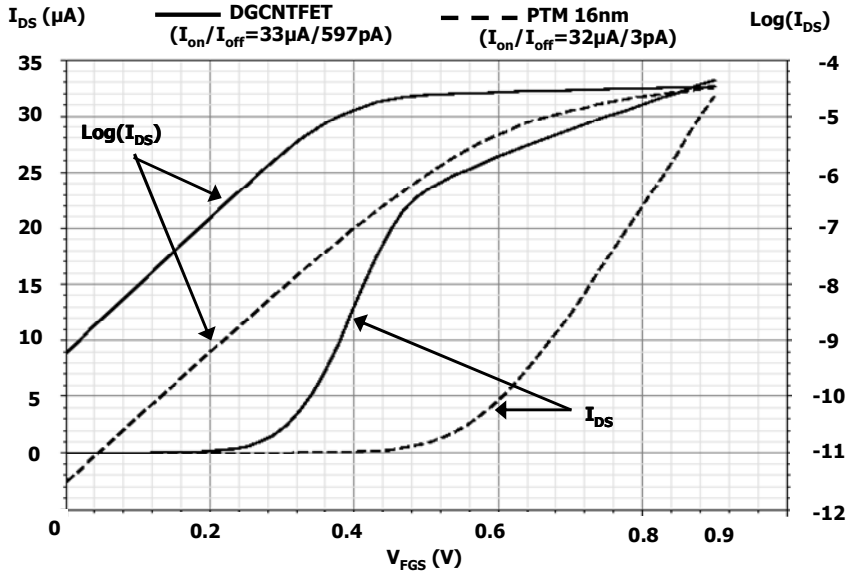


Figure 4-2. caracteristiques I_{DS}/V_{FGS} d'une branche de type N (V_{BG} -V_S = +V= +0. 9V)

Par rapport au CMOS 16nm, le DG-CNTFET montre un courant I_{OFF} élevé (~ 600pA vs 3pA) et une faible tension de seuil V_{th} (~ 0.2V vs ~ 0.4V). En fait, ces deux caractéristiques sont liées à la technologie ambipolaire en général.

4.3 Validation et évaluation de l'approche de conception TTSM:

4.3.1 Résultats de simulations

L'objectif principal de l'utilisation de l'approche TTSM est de réduire le nombre de transistors dans les cellules logiques, avec un impact attendu sur la consommation d'énergie, la surface et le temps de retard (délai). Dans cette section, nous comparons les portes logiques conçues à partir de l'approche TTSM qu'on a abrévié (DGSL) avec leurs équivalentes conçues avec la logique conventionnelle (CSL), en utilisant le même dispositif DG-CNTFET. Nous étendons la comparaison à la logique CMOS classique construite avec la technologie CMOS 16nm (CMOS). Les résultats sont présentés dans la figure 4-3.

Nous comparons également les cellules logiques dynamiques conçues en utilisant l'approche TTSM (DGDL), avec les cellules logiques dynamiques conventionnelles (CDL) et les cellules logiques CMOS construites avec la technologie CMOS 16nm (CMOS). Les résultats sont présentés dans la figure 4-4.

P est la puissance, TD est le temps de retard (délai), PDP est le Produit-Puissance-Délai et Area représente la surface.

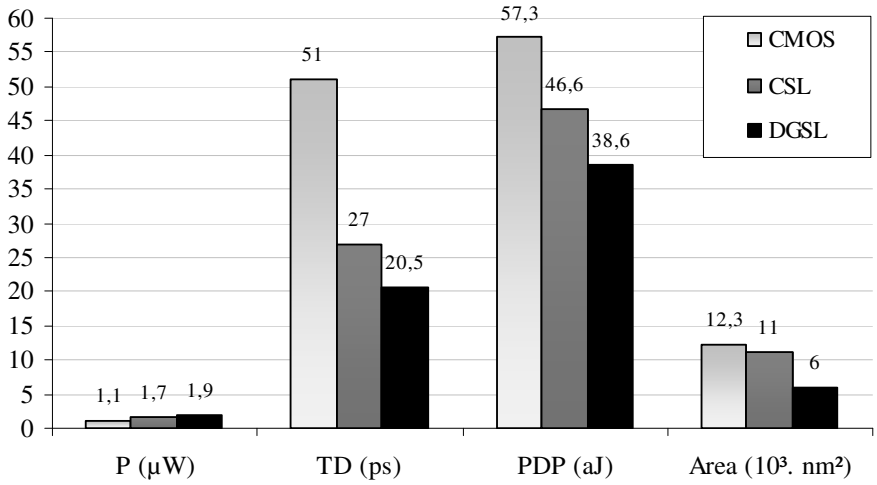


Figure 4-3. Comparaison des portes logiques statiques @ f=1Ghz: CMOS vs CSL vs DGSL

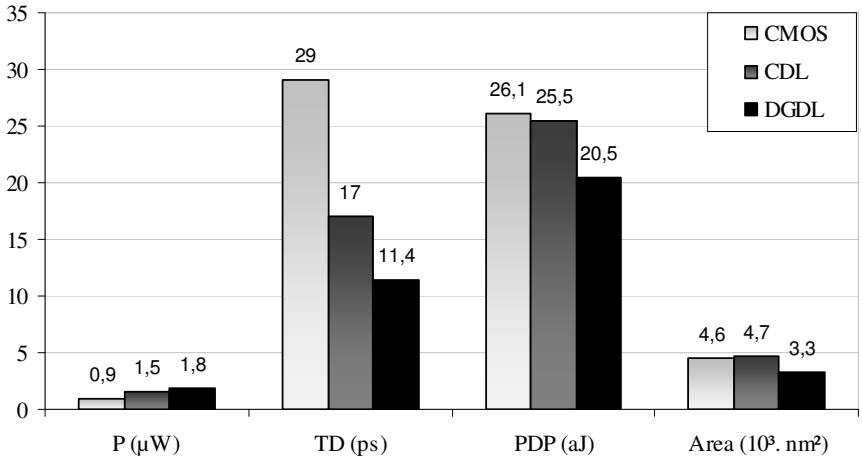


Figure 4-4. Comparaison des portes logiques dynamiques @ f=1Ghz: CMOS vs CDL vs DGDL

4.3.2 Contributions

Nous avons évalué l'approche TTSM décrite dans le chapitre 2, qui exploite notamment la propriété ambipolaire des Am-IDGFETs pour réduire efficacement le nombre de transistors des cellules logiques selon des styles logiques différents, conduisant à une densité d'intégration plus importante. L'approche TTSM a prouvé un gain en surface pouvant atteindre 51% avec les portes logiques statiques. Dans le cas du style logique dynamique, l'approche peut réaliser un gain de près de 30% en terme de surface. Les deux familles logiques, ont été validées par des simulations électriques d'un ensemble de portes logiques en utilisant les modèles des transistors les plus avancés disponibles dans la communauté pour la technologie DG-CNTFET et de la technologie CMOS 16nm afin d'évaluer les avantages des circuits compacts obtenus concernant la consommation d'énergie et de retard. Malgré l'augmentation de la consommation d'énergie observée avec les portes conçues, on obtient une amélioration de 30% en terme de PDP grâce à la diminution du délai (2.5X). L'amélioration remarquable du délai est due essentiellement à la faible tension de seuil V_{th} des DG-CNTFETs ainsi qu'à la diminution de nombre des transistors en série en utilisant l'approche TTSM qui réduit la résistance équivalente du canal et par conséquent la constante du temps.

4.4 Validation et évaluation de la technique de conception à faible consommation:

4.4.1 Résultats de simulations

Nous comparons les portes logiques statiques conçues à partir des Am-IDGFETs pour une faible consommation (abréviées "Clk"), décrit dans la deuxième partie du chapitre 2, avec les portes équivalentes construites selon une logique statique conventionnelle (abrévié "Cnv") en utilisant le même dispositif Am-IIDGFET (DG-CNTFET dans ce cas). En outre, nous étendons la comparaison à la logique CMOS construit avec la technologie CMOS 16nm (abréviée CMOS). P_{SC} est la consommation du court-circuit, P_{tot} est la consommation totale et P_{stat} représente la consommation statique. Les résultats de simulations sont montrés dans la figure 4-5.

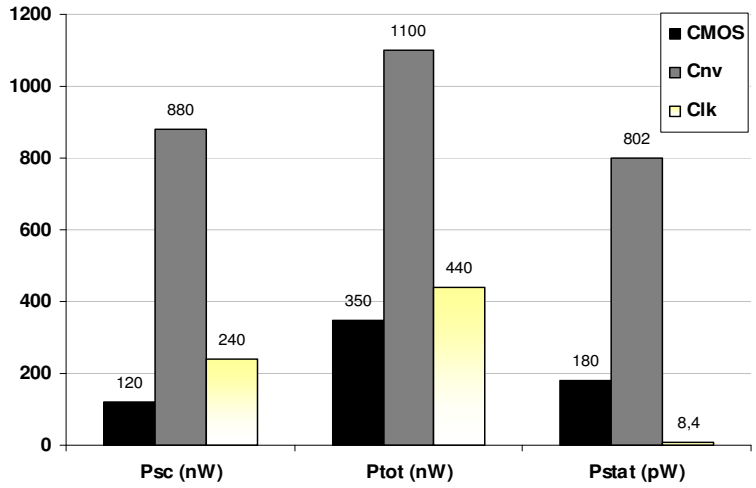


Figure 4-5. Comparaison des différentes composantes de la consommation d'énergie

4.4.2 Contributions

Nous avons évalué la technique de conception des circuits logiques à faible puissance, décrite dans le chapitre 2. La technique consiste à éteindre tous les transistors par l'intermédiaire de leurs grilles arrière pendant le temps de commutation pour abaisser la puissance de court-circuit. Les résultats des simulations montrent une amélioration de 4X en termes de puissance de court-circuit par rapport aux portes classiques. En outre, la consommation totale d'énergie a été améliorée par un facteur de 3X. A travers l'inversion des tensions de la grille arrière de transistor, le courant I_{OFF} est diminué d'un facteur de 100X conduisant à la diminution de la puissance statique avec le même ordre de grandeur. Ainsi, la technique s'est révélée être un moyen efficace pour résoudre le problème de la consommation d'énergie dans les Am-IDGFETs.

4.5 Validation et évaluation des cellules logiques reconfigurables conçues à partir des classes de fonctions et AmBDDs

Dans cette section, nous validons et nous évaluons les méthodologies de conception présentées dans le chapitre 3 pour concevoir de la logique reconfigurable avec les dispositifs Am-IDGFETs. Nous visons à valider le comportement de chaque cellule au moyen des simulations électriques et d'estimer la consommation d'énergie et les délais. Les cellules sont comparées entre elles, ainsi qu'avec des cellules logiques en technologie CMOS 16nm. Nous

discutons les résultats obtenus en mettant l'accent sur les avantages des cellules obtenues à partir de deux approches de conception proposées.

4.5.1 Résultats de simulations

Notre étude porte sur des circuits reconfigurables construites avec les styles logiques dynamiques et statiques. Pour avoir une comparaison aussi juste que possible, nous caractérisons et comparons les cellules dynamiques et les cellules statiques séparément.
Trois cellules logiques dynamiques ont été conçues dans le chapitre 3 (DRLC-7T, SOP-DRLC et SS-DRLC). Le benchmark CMOS est un multiplexeur à quatre entrées et une sortie. Il est basé sur un style logique dynamique et abrévié DL-MUX 4:1 (figure 4-6). Les résultats des comparaisons sont présentés dans les figures 4-9 et 4-10.

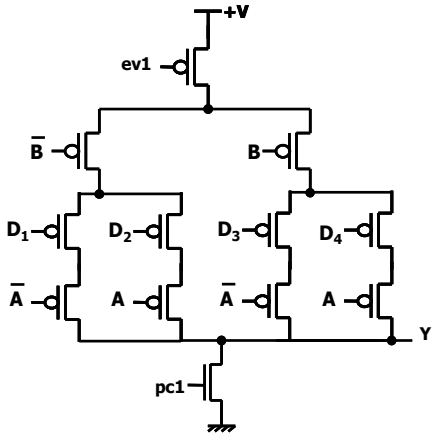


Figure 4-6. Multiplexeur 4:1 en logique dynamique (DL-MUX 4:1)

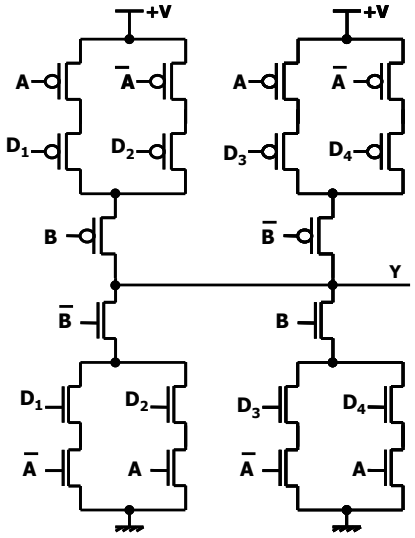


Figure 4-7. Multiplexeur 4:1 en logique statique complémentaire (CSL-MUX 4:1)

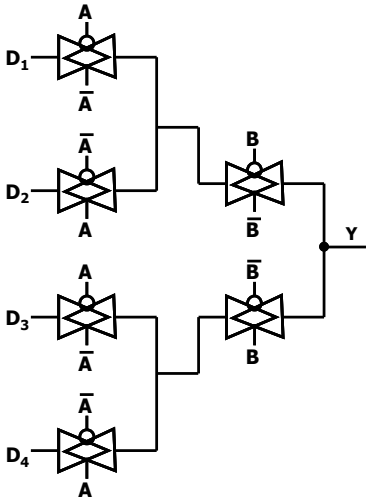


Figure 4-8. Multiplexeur 4:1 en logique statique à portes logiques de transmission (TG-MUX 4:1)

En ce qui concerne les cellules logiques statiques, quatre cellules ont été conçues dans le chapitre 3, la première cellule conçue (CSL-DRLC) a été obtenue à partir de la méthode de classification de fonction, tandis que trois autres cellules (16F-AmBDD, 12F-AmBDD, et 6F-AmBDD) ont été obtenues à partir de l'approche AmBDD. Dans cette section, l'ensemble des cellules logiques statiques sont comparés à deux multiplexeurs en technologie CMOS utilisés comme cellules logiques reconfigurables. Le premier MUX 4:1 est construit avec la logique statique complémentaire et abrévié CSL-MUX 4 :1 montré dans la figure 4-7. Le deuxième MUX est aussi conçu avec un style logique statique, mais utilise des portes logiques de transmission et abrévié "TG-MUX 4 :1" montré dans la figure 4-8. Les résultats des comparaisons sont présentés dans les figures 4-11 et 4-12.

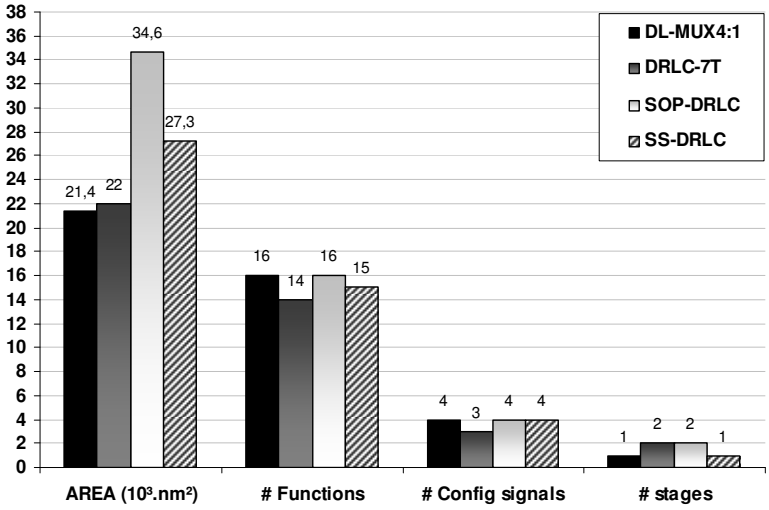


Figure 4-9. Comparaison des cellules logiques dynamiques en termes de surface, nombre de fonctions, signaux de configurations et stages logiques

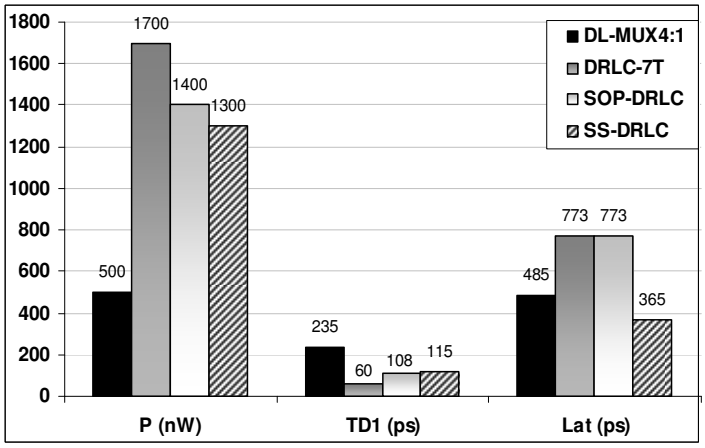


Figure 4-10. Comparaison des cellules logiques dynamiques en termes de puissance, delai et temps de latence

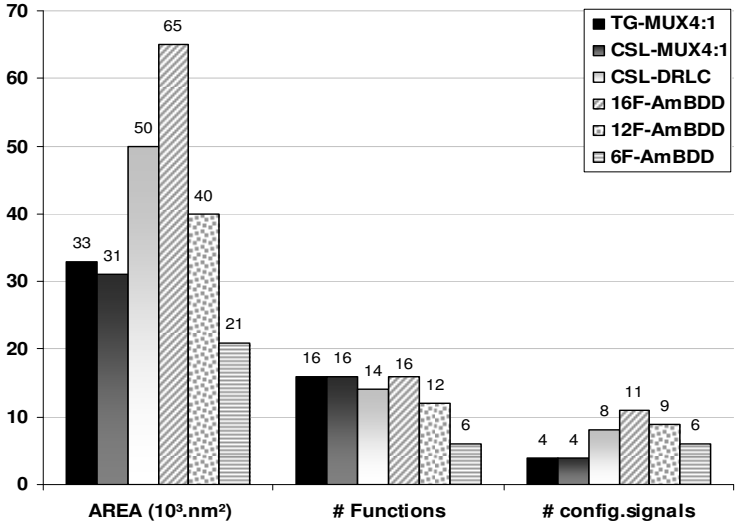


Figure 4-11. Comparaison des cellules logiques statiques en termes de surface, de nombre des fonctions et de signaux de configurations

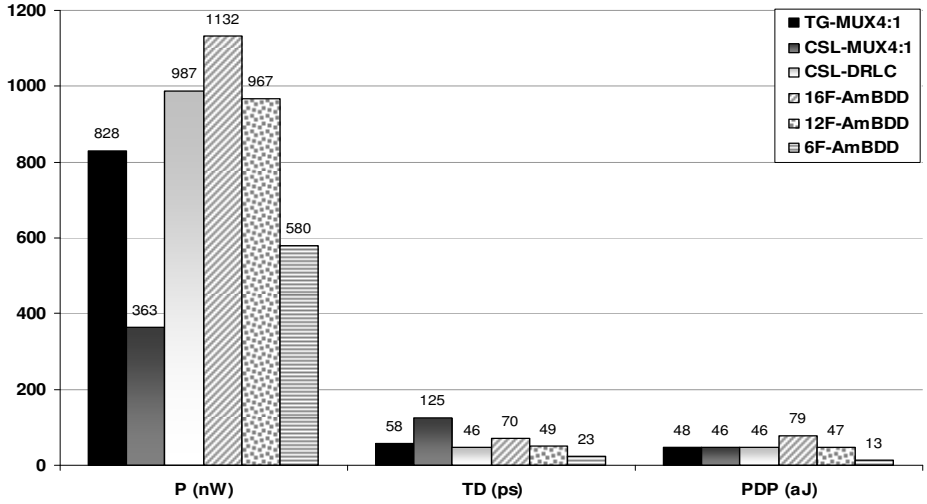


Figure 4-12. Comparaison des cellules logiques statiques en termes de puissance, délai et produit puissance-délai

4.5.2 Contributions

Puisque on a utilisé deux styles logiques (dynamiques et statiques) pour concevoir des cellules reconfigurables, nous avons choisi de comparer les cellules générées avec leurs homologues CMOS 16nm construites avec le même style logique. Des multiplexeurs 4:1 ont été utilisés comme benchmarks car ils présentent les structures CMOS classiques pour de nombreux systèmes logiques reconfigurables. On rappelle que l'utilisation de portes logiques de transmission au lieu d'un seul transistor dans le cas de la technologie DG-CNTFET était nécessaire pour assurer un comportement logique correct (pas de dégradation des niveaux logiques, compatibilité des valeurs de tension assurant le bon fonctionnement de l'ensemble du circuit). D'après les résultats de simulations, cela s'est avéré être une bénédiction mitigée, car une augmentation de 2-3X dans la consommation d'énergie a été observée par rapport à la technologie CMOS 16nm, accentuée par une faible tension de seuil V_{th} caractérisant les Am-IDGFETs. Toutefois, le PDP était presque de la même valeur pour certaines cellules grâce au faible délai offert par la technologie CNT provenant d'une faible tension de seuil V_{th}. Un coût supplémentaire de l'utilisation des portes logiques de transmission est l'augmentation de la surface requise par les circuits logiques. L'inconvénient majeur des cellules logiques statiques générées par les méthodes de conception proposées est le nombre élevé de signaux de configuration. Ce problème est atténué à travers la conception de cellules logiques à fonctionnalité partielle qui améliorent les performances du circuit tout en diminuant la surface. En fait, pour les deux approches (classification de fonctions ou AmBDDs), la première étape est de définir les fonctions que nous nous efforçons d'atteindre à la sortie du circuit. Ainsi, un concepteur peut analyser les fonctions qui devraient être utilisés de façon intensive dans une application, puis générer des cellules à fonctionnalité partielle qui répondent aux besoins de l'application, et par la suite optimiser la surface, le nombre de signaux de configuration et améliore les performances de tout le système logique.

4.6 Conclusions

Dans le cadre de cellules standards, un ensemble de portes logiques dynamiques et statiques a été caractérisé. Les résultats ont été comparés aux portes logiques CMOS classiques. Il a été démontré que l'approche TTSM décrit au chapitre 2 permet la réalisation de portes logiques statiques et dynamiques d'une manière très efficace et compacte, ce qui augmente la compacité de portes logiques par un facteur de 2X par rapport la logique statique

complémentaire. En combinant l'avantage d'utiliser moins de transistors grâce à l'approche TTSM avec les avantages de la technologie CNT, une nette amélioration en terme de délai est obtenue par rapport à la technologie CMOS (2X). Malgré l'augmentation de la consommation d'énergie observée avec les portes logiques conçues, on a conservé une amélioration de PDP (30%). Dans le même contexte de cellules standards, nous avons évalué la technique de conception à faible puissance proposée dans le chapitre 2. Les résultats ont montré une amélioration de la consommation d'énergie pour les deux composantes (statique (100X) et dynamique (3X). Cela peut résoudre deux problèmes majeurs liés aux dispositifs ambipolaire avec les canaux non dopés (courant I_{OFF} élevé et faible tension de seuil V_{th}).

Dans le cadre de circuits reconfigurables obtenus à partir des approches de conception du chapitre 3, les DG-CNTFETs ont montré moins d'efficacité avec les cellules reconfigurables à fonctionnalité complète. Cela était principalement dû à la nécessité d'utiliser des portes logiques de transmission afin de résoudre certains problèmes électriques liés au comportement des Am-IDGFETs en général. Il a été montré que les portes logiques de transmission ; D'une part, offrent une logique reconfigurable très propre et souple (pas de dégradation de niveau logique). D'autre part, elles augmentent la surface des cellules logiques et la consommation d'énergie. En ce qui concerne les délais, la technologie CNT pour la logique reconfigurable garde une amélioration 2-3 X mieux que la technologie CMOS.

La surface, la consommation d'énergie ainsi que le nombre de signaux de configuration limitent l'efficacité de la conception des cellules reconfigurables à partir des Am-IDGFETs. L'utilisation des cellules avec une fonctionnalité partielle pourrait être une alternative aux cellules à fonctionnalité complètes si elles sont judicieusement exploitées à un niveau architectural, la chose qui rend l'approche très intéressante pour les FPGAs à base des Am-IDGFETs.

Chapitre 5
Conclusions

Les matériaux unidimensionnels tels que les CNTS, GNRs et les nanofils de silicium SiNW bénéficient d'une mobilité élevée qui les rend des candidats très prometteurs pour remplacer le canal en silicium dans les transistors CMOS. En outre, à la présence des barrières de Schottky au niveau des points d'accès au canal du drain et la source, ils démontrent un comportement intéressant connu sous le nom "ambipolarité". Pour contrôler un tel comportement, le dopage chimique n'est pas facile et une meilleure alternative est de contrôler électrostatiquement la polarité des dispositifs par l'intermédiaire d'un quatrième terminal (deuxième grille). Ainsi en utilisant des dispositifs ambipolaire dans un contexte à double grille, une nouvelle catégorie des dispositifs a vu le jour. Nous l'appelons "Am-IDGFET" (transistor-ambipolaire-à-effet-de-champ-à-double-grille-indépendante). Ce dispositif est capable de fonctionner en tant qu'un transistor de type N ou de type P en fonction de la tension de polarisation de leur grille arrière. En conséquence, un ensemble d'options de commutation plus riche est disponible avec ce dispositif, sans homologue en technologie CMOS. Cependant, une logique ambipolaire plus riche exige des paradigmes de conception plus innovants, puisque les méthodologies et des techniques classiques basées sur les transistors unipolaires à trois terminaux ne sont plus adaptées pour construire une logique ambipolaire optimale. La contribution de cette thèse consiste à définir des méthodologies systématiques de conception, de synthèse logique et des techniques d'évaluation afin d'obtenir des approches de conception plus universelles qui peuvent exploiter les opportunités offertes par la logique ambipolaire. Cela a été porté sur deux axes principaux: les cellules logiques standards et la logique reconfigurable. Pour chaque axe des méthodologies de conception, et/ou des techniques de synthèse ont été établies. Pour évaluer les avantages et les inconvénients des approches de conception proposées, des simulations électriques précises basées sur un modèle compact d'un dispositif DG-CNTFET ainsi que des comparaisons détaillées avec la technologie CMOS 16nm ont été réalisées. Figure 5-1 résume les contributions de la thèse et décrit les résultats obtenus.

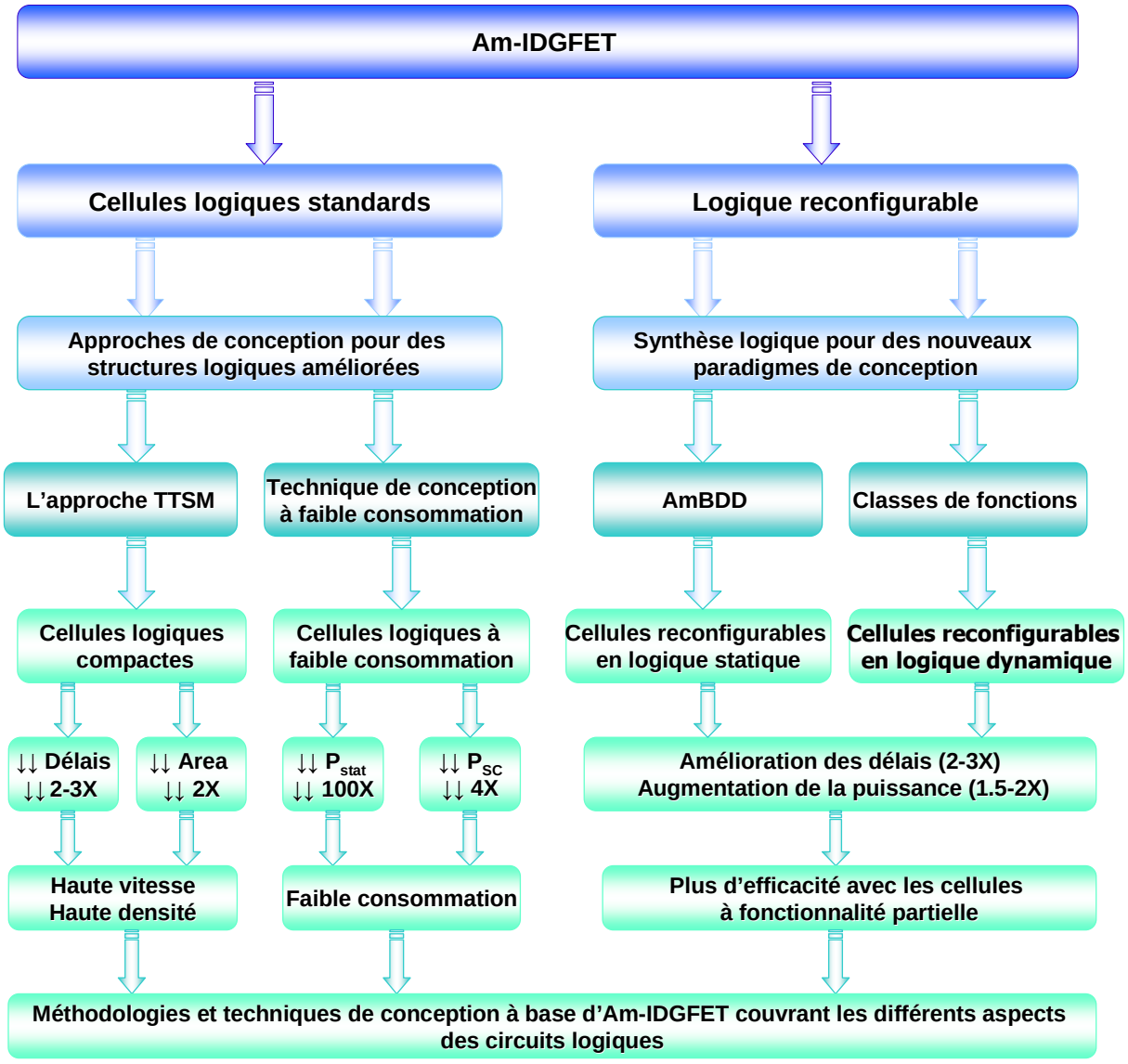


Figure 5-1. Contributions et résultats de la thèse

Cellules logiques standards:

La grille arrière de l'Am-IDGFET a été exploitée pour réaliser deux nouvelles approches de conception de portes logiques standards.

La première approche (TTSM) réduit efficacement le nombre de transistor pour les cellules logiques selon des styles logiques statiques et dynamiques, conduisant à des structures logiques plus compacts, une amélioration de la vitesse et de la surface par rapport aux portes logiques classiques. L'approche TTSM prouve que le nombre de transistors nécessaires pour des structures classiques peut être divisé par 2 dans le cas de certaines portes logiques complémentaires statiques. Le même gain de 2X a été montré concernant les délais. Une telle approche peut être appliquée à construire une bibliothèque entière de cellules logiques standard à haute densité et à haute vitesse.

La deuxième approche est une technique de conception à faible consommation pour résoudre certains problèmes liés aux dispositifs ambipolaires non dopés en général. Le premier problème est celui d'un courant I_{OFF} élevé qui augmente les courants de fuite. Le deuxième problème est celui d'une tension de seuil V_{TH} qui (en plus de l'augmentation de I_{OFF}) accroît aussi le courant de court-circuit comme un effet secondaire à une logique rapide. Pour résoudre ces problèmes, nous avons proposé de contrôler l'état des transistors en les

désactivant pendant les transitions d'entrée via leurs grilles arrières; de manière à diminuer la contribution de court-circuit à la puissance dynamique. Des diminutions de 4X et 3X, respectivement, en termes de puissance de court-circuit et la puissance totale ont été réalisés dans le cas des circuits à base de DG-CNTFET. En outre, nous avons montré qu'en inversant la tension de la grille arrière pendant le mode veille, le courant de fuite I_{OFF} (et par conséquent de puissance statique) est réduit par un facteur de 100X.

Cellules logiques reconfigurables:

Avec les Am-IDGFETs, un nouveau vecteur de reconfigurabilité est possible. Afin de synthétiser une logique optimale, nous avons défini deux méthodes systématiques de conception de la logique reconfigurable. Dans un premier temps, nous avons étudié le concept de classification des fonctions en faisant correspondre chaque classe à sa structure générique, et nous avons montré que chaque structure de classe générique peut réaliser une cellule reconfigurable. En outre, nous avons identifié une corrélation entre les différentes classes, offrant ainsi la possibilité de construire des cellules logiques reconfigurables avec fonctionnalité partielle ou complète. Basé sur un style logique dynamique, nous avons conçu un ensemble de cellules logiques reconfigurables à 2 entrées, ainsi qu'une cellule logique statique.

Nous avons également proposé un diagramme ambipolaire de décision binaire (Am-BDD), pour adapter la synthèse logique conventionnelle BDD aux dispositifs ambipolaires. En utilisant la technique Am-BDD, nous avons conçu une cellule reconfigurable à 2 entrées capable d'achever 16 fonctions et nous avons également dérivé des cellules plus compactes avec des fonctionnalités partielles.

Concernant l'implémentation au niveau transistor des circuits logiques générés à partir de deux approches de conception, nous avons utilisé des portes logiques de transmission au lieu de simples transistors Am-IDGFETs afin de résoudre le problème de la dégradation des niveaux logiques et à assurer le bon fonctionnement des circuits synthétisés. Ensuite nous avons évalué un ensemble de cellules reconfigurables générées à partir des approches de conception proposées selon la logique statique et la logique dynamique en se basant sur une technologie DG-CNTFET. A partir des résultats des simulations, la logique reconfigurable à fonctionnalité complète entraîne a montré une faible efficacité principalement en raison de la nécessité d'utiliser (plusieurs transistors) dans les portes logiques de transmission au lieu d'un simple transistor. Cela entraîne une augmentation de la consommation d'énergie ainsi que de la surface. En ce qui concerne les délais, une amélioration de 2X-3X par rapport aux cellules logiques classiques a été observé. L'augmentation de la consommation d'énergie et la diminution de délai a abouti à un PDP comparable.

Pour résumer, la surface, la consommation d'énergie et le nombre de signaux de configuration limitent l'efficacité approches de conception des cellules reconfigurables. Une alternative pourrait être l'utilisation des cellules à fonctionnalité partielle au lieu des cellules à fonctionnalité complète. Ceci a prouvé être une solution réalisable si les cellules sont judicieusement exploitées à un niveau architectural [5-1, 5-2, 5-3], conduisant à une réduction du nombre de signaux pour faire le routage et rendre l'approche très intéressante pour les FPGAs à base des DG-CNTFET.

En guise de conclusion que les Am-IDGFETs offrent des nouvelles opportunités de conception grâce à la grille arrière. Des cellules logiques compactes et des blocs logiques reconfigurables ont été construits dans cette thèse par l'application des méthodologies et des techniques de conception novatrices. Le résultat commun attractif pour tous les circuits conçus était l'amélioration des délais permettant une logique à haute vitesse. Bien que l'augmentation de la consommation d'énergie a été mentionnée avec les circuits basés sur les Am-IDFETs, nous avons montré la possibilité de diminuer cette consommation en variant la tension de la grille arrière et a obtenu une diminution de 100X en terme de la puissance

statique. La contribution de cette thèse, aux plusieurs niveaux de la conception logique (cellules standards compactes, logique reconfigurable, circuits à haute performance et circuits à faible puissance) pourrait permettre aux concepteurs d'envisager la possibilité de construire une plate-forme hétérogène où de nombreux blocs peuvent être mises en œuvre ensemble pour obtenir le maximum de bénéfices de la technologie Am-IDGFET.

Liste de travaux publiés durant la thèse

Brevets

- **K. Jabeur**, I. O'Connor, "Porte logique statique programmable à transistors ambipolaires et équipement électronique associé," Brevet français n° 10 59363, 15 novembre 2010
- **K. Jabeur**, I. O'Connor, "Porte logique dynamique programmable," Brevet français n° 10 59364, 15 novembre 2010

Chapitre de livre

- I. O'Connor, J. Liu, **K. Jabeur**, N. Yakymets, R. Daviot, D. Navarro, P.-E. Gaillardon, F. Clermidy, M. Amadou, G. Nicolescu, "Emerging Technologies and Nanoscale Computing Fabrics", VLSI-SoC: Technologies for Systems Integration, IFIP Advances in Information and Communication Technology, Springer, vol. 360, pp.1-20, 2011.

Conférences Invitées

- N. Yakymets, **K.Jabeur**, I.O'Connor and S.Le Beux, "Interconnect topology for cell matrices based on low-power nanoscale devices" Invited paper, IEEE conference on TFTC, July 2011.
- I. O'Connor, **K. Jabeur,** S. Le Beux, D. Navarro, "Ambipolar Independent Double Gate FET Logic ", IEEE/ACM International Symposium (NanoArch), July 4-6-2012, Amsterdam, the Netherlands

Conférences Internationales

- **K. Jabeur**, P.-E. Gaillardon, D. Navarro, I. O'Connor, M. H. Ben-Jamaa, F. Clermidy, "Reducing transistor count in clocked standard cells with ambipolar double-gate FETs", IEEE/ACM International Symposium (NanoArch), June 17-18 - 2010, Anaheim (CA), USA.
- I.O'Connor, **K. Jabeur**, D. Navarro, N. Yakymets, P.-E. Gaillardon, M. H. Ben-Jamaa, F. Clermidy, "Logic cells and interconnect strategies for nanoscale reconfigurable computing fabrics", IEEE International Conference on Electronics, Circuits and Systems (ICECS), 12-15 December 2010, Athens, Greece.
- **K. Jabeur**, N. Yakymets, I. O'Connor and S. Le Beux. " Fine-Grain Reconfigurable Logic Cells Based on Double-gate CNTFETs", IEEE/ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI), Lausanne, June, 2011.
- N.Yakymets, **K.Jabeur**, I.O'Connor and S. Le Beux. "Mapping Methodology and Analysis of Matrix-Based Nanocomputer Architectures", In IEEE International Conference on New Circuits and Systems (NEWCAS), Bordeaux, June, 2011. **(BEST PAPER AWARD)**
- **K. Jabeur**, N.Yakymets, I.O'Connor and S.Le Beux. "Ambipolar double-gate FET binary-decision- diagram (Am-BDD) for reconfigurable logic cells", IEEE International Symposium on Nanoscale Architectures (NANOARCH), San Diego, June, 2011.
- N.Yakymets, S.Le Beux, **K.Jabeur** and I.O'Connor. "Multi-Objective Mapping for Matrix-Based Nanocomputer Architectures", 6th International Workshop on (ReCoSoC), Montpellier, June, 2011.
- **K. Jabeur**, I. O'Connor, N. Yakymets, S. Le Beux. "High performance 4:1 multiplexer with ambipolar double-gate FETs", IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2011.
- **K. Jabeur**, I. O'Connor, N.Yakymets and S. Le Beux. "Ambipolar double-gate FETs for the design of compact logic structure", IEEE/ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI), Salt Lake City, May, 2012.
- **K. Jabeur,** I. O'Connor, D. Navarro, S. Le Beux, "Low-power design technique with ambipolar double gate devices", IEEE/ACM International Symposium (NanoArch), July 4-6-2012, Amsterdam, the Netherlands
- **K. Jabeur,** I. O'Connor, S. Le Beux, D. Navarro, "Ambipolar double gate CNTFETs based reconfigurable Logic cells", IEEE/ACM International Symposium (NanoArch), July 4-6-2012, Amsterdam, the Netherlands

-Invited Talk- (Tutorial à EPFL Lausanne)

- "Ambipolar double-gate transistor logic circuit design-methods and techniques", Integrated Systems Centre SI with Prof. G. De Micheli, 29 May 2012, EPFL, Lausanne, Suisse.

Séminaires et colloques

- **K. Jabeur,** I. O'Connor, S. Le Beux, "Logic Design with Ambipolar Double-Gate FETs", GDR SoC SiP, june 2012, Paris, France.
- **K. Jabeur**, I. O'Connor, N. Yakymets, " Nanocoputing with Double-Gate CNT devices", Journées Electroniques, October 2011, Université Montpellier 2, France.
- **K. Jabeur,** I. O'Connor, N. Yakymets, " Reconfigurable Logic based on Double-Gate CNTFETs", GDR SoC SiP, june 2011, Lyon, France.
- **K. Jabeur,** I. O'Connor, N. Yakymets, " Nano-Reconfigurable Logic Clusters", JNRDM, May 2011, ENS Cachan, Paris, France.
- R. Daviot, P.E. Gaillardon**, K.Jabeur,** D. Navarro, I. O'Connor, N. Yakymets, " Reconfigurable architectures using Double Gate CNTFETs", Colloque LIA-LN2**,** Sherbrooke, Canada.

dernière page de la thèse

AUTORISATION DE SOUTENANCE

Vu les dispositions de l'arrêté du 7 août 2006,

Vu la demande du Directeur de Thèse

Monsieur I. O'CONNOR

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Monsieur J-O. KLEIN
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Monsieur JABEUR Kotb

est autorisé à soutenir une thèse pour l'obtention du grade de **DOCTEUR**

Ecole doctorale ELECTRONIQUE, ELECTROTECHNIQUE, AUTOMATIQUE

Fait à Ecully, le 7 septembre 2012

P/Le directeur de l'E.C.L.
La directrice des Etudes

ECOLE CENTRALE DE LYON SCOLARITE 3ème Cycle

M-A. GALLAND

Abstact

The continuous growth of global demand for semiconductor products (in a broad range of sectors, such as security, healthcare, entertainment, connectivity, energy, etc.) has been both enabled and fuelled by Moore's law and regular doubling of circuit density and performance increases. However, as CMOS technology scaling begins to reach its theoretical limits, the ITRS predicts a new era known as "Beyond CMOS". Novel materials and devices show an ability to complement or even replace the CMOS transistor or its channel in systems on chip with silicon-based technology. This has led to the identification of promising phenomena such as ambipolar conduction in quasi one- and zero-dimensional structures, for example in carbon nanotubes, graphene and silicon nanowires. Ambipolarity, in a dual-gate context (DG-FETs), means that n- and p-type behavior can be observed in the same device depending on the back gate voltage polarity. In addition to their attractive performances and the low power consumption, ambipolar double gate devices enable the development of completely new circuit structures and design paradigms. Conventional logic synthesis techniques cannot represent the capability of DG-FETs to operate as either n-type or p-type switches and new techniques must be found to build optimal logic.

The work in this thesis explores design techniques to enable the use of such devices by defining generic approaches and design techniques based on ambipolar DG-FETs. Two different contexts are tackled: (i) improving standard cell logic design with more compact structures and better performance, as well as low-power design techniques exploiting the fourth terminal of the device, and (ii) adapting conventional logic synthesis and verification techniques such as Binary Decision Diagrams or Function Classification to ambipolar DG-FETs in order to build reconfigurable logic cells. The proposed methods and techniques are validated and evaluated in a case study focused on DG-CNTFET through accurate simulations, using the most mature and recent DG-CNTFET model available in the literature.

Résumé

La croissance continue de la demande mondiale des produits semi-conducteurs (dans un large éventail de secteurs, tels que la sécurité, la santé, le divertissement, la connectivité, l'énergie, etc) a été conduite par la loi de Moore en doublant régulièrement la densité et les performances des circuits numériques. Cependant, comme la miniaturisation de la technologie CMOS commence à atteindre ses limites théoriques, l'ITRS prévoit une nouvelle ère connue sous le nom "Beyond CMOS". Des nouveaux matériaux et dispositifs révèlent une capacité à compléter ou même remplacer le transistor CMOS ou son canal dans les systèmes sur puce à base de silicium. Cela a conduit à l'identification des phénomènes prometteurs tel que la conduction ambipolaire dans les structures quasi uni- et zéro-dimensionnels, par exemple dans les nanotubes de carbone, le graphène et les nanofils de silicium. L'ambipolarité, dans un contexte à double grille (DG-FET), signifie qu'un comportement de type N et P puisse être observé dans le même dispositif en fonction de la polarité de la tension de la grille arrière. En plus de leur performance attractive et leur faible consommation de puissance, les dispositifs ambipolaires à double grille indépendantes (Am-IDGFET) permettent le développement des structures logiques ainsi que des paradigmes de conception entièrement inédits. Les techniques classiques de synthèse logique ne peuvent pas représenter la capacité des Am-IDGFETs de fonctionner soit comme commutateurs de type N ou de type P. Alors des nouvelles techniques doivent être trouvées pour construire une logique optimale.

Le travail de cette thèse explore les techniques de conception pour permettre l'utilisation de ces dispositifs en définissant des approches génériques et des techniques de conception basées sur les Am-IDGFETs. Deux contextes différents sont abordés: (i) l'amélioration de la conception de cellules logiques avec des structures plus compactes et une meilleure performance, ainsi que des techniques de conception à faible consommation qui exploitent la grille arrière du dispositif, et (ii) l'adaptation des techniques classiques de synthèse logique comme les diagrammes de décision binaires (BDDs) ou l'approche de classification des fonctions afin de construire des cellules logiques reconfigurables à base des Am-IDGFETs. Les méthodes et les techniques proposées sont validées et évaluées à travers une étude basée sur le dispositif DG-CNTFET par l'intermédiaire des simulations précises, en utilisant le modèle DG-CNTFET le plus mature disponible dans la littérature.