Optimisation du procédé de réalisation pour l'intégration séquentielle 3D des transistors CMOS FDSOI

Cuiqin Xu

UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Nanoélectronique et Nanotechnologies**
Arrêté ministériel :7 août 2006

Présentée par

Cuiqin XU

Thèse dirigée par **Mireille MOUIS** et
codirigée par **Perrine BATUDE** et **Maud VINET**

préparée au sein des **Laboratoire CEA-LETI et IMEP-LAHC**
dans **l'École Doctorale EEATS**

Optimisation du procédé de réalisation pour l'intégration séquentielle 3D des transistors CMOS FDSOI

(Process optimization for 3D sequential integration of FDSOI CMOS transistors)

Thèse soutenue publiquement le **09 Octobre 2012**,
devant le jury composé de :

M. Francis CALMON
Professeur des Universités, INSA Lyon (Président)
M. Emmanuel DUBOIS
Directeur de Recherche, CNRS/IEMN (Rapporteur)
M. François OLIVIE
Professeur des Universités, Université Paul Sabatier Toulouse (Rapporteur)
M. Filadelfo CRISTIANO
Chargé de recherche, CNRS/LAAS (Membre)
M. Scott LUNING
Ingénieur, Docteur, Globalfoundries, USA (Membre invité)
Mlle. Perrine BATUDE
Ingénieur, Docteur, CEA-LETI (Membre)
Mme. Maud VINET
Ingénieur, Docteur, CEA-LETI (Membre)
Mme. Mireille MOUIS
Directeur de Recherche, CNRS/IMEP-LAHC (Membre)

Abstract

Process optimization for 3D sequential integration of FDSOI CMOS transistors

Low temperature (LT) process is gaining interest in the frame of 3D sequential integration where limited thermal budget (<650 ºC) is needed for top FET to preserve bottom FET from any degradation and also in the standard planar integration for achieving ultra-thin EOT and work function control with high-k metal gate without gate-last integration scheme. In this work, LT Solid Phase Epitaxial Regrowth (SPER) has been investigated for reducing the most critical thermal budget which is dopant activation.

From previous works, LT activated devices face several challenges: First, higher junction leakage limits their application to high performance devices. Secondly, strong deactivation of the metastable activated dopants was observed with post anneals. Thirdly, the dopant weak diffusion makes it difficult to connect the channel with S/D.

In this work, it is shown that the use of FDSOI enables to overcome junction leakage and Boron deactivation issues thanks to the defect cutting off and sinking effect of buried oxide. As a consequence, dopant deactivation in FDSOI devices is no longer an issue. Finally, implants conditions of LT transistors have been optimized to reach similar performance than its standard high temperature counterparts.

Keywords: 3D sequential integration, Solid Phase Epitaxial Regrowth, low temperature process, deactivation, fully depleted devices.

Résumé

Optimisation du procédé de réalisation pour l'intégration séquentielle 3D des transistors CMOS FDSOI

L'activation à basse température est prometteuse pour l'intégration 3D séquentielle où le budget thermique du transistor supérieur est limité (<650 ºC) pour ne pas dégrader le transistor inférieur, mais aussi dans le cas d'une intégration planaire afin d'atteindre des EOT ultra fines et de contrôler le travail de sortie de la grille sans recourir à une intégration de type « gate-last ». Dans ce travail, l'activation par recroissance en phase solide (SPER) a été étudiée afin de réduire le budget thermique de l'activation des dopants.

L'activation à basse température présente plusieurs inconvénients. Les travaux précédents montrent que les fuites de jonctions sont plus importantes dans ces dispositifs. Ensuite, des fortes désactivations de dopants ont été observées. Troisièmement, la faible diffusion des dopants rend difficile la connexion des jonctions source et drain avec le canal.

Dans ce travail, il est montré que dans un transistor FDSOI, l'augmentation des fuites de jonctions et la désactivation du Bore peuvent être évités grâce à la présence de l'oxyde enterré.

De plus les conditions d'implantation ont été optimisées et les transistors activés à 650 ºC atteignent les performances des transistors de référence.

Mots-clés: Intégration 3D séquentielle, recroissance en phase solide, procédés à faible budget thermique, désactivation, transistors totalement déplétés.

Acknowledgement

Thinking about my PhD study in the past three years, I am sure that I could not make it without the supports from my lab, colleagues, friends and family.

I would like to express my thanks to my lab CEA-LETI for the great opportunity to enjoy such an interesting project. My supervisors, Ms. Perrine Batude, Maud Vinet and Mireille Mouis have given me persistent support and guidance: not only about specific scientific topics related to this project, but also about how to become a good researcher.

Also, I would like to thank all my colleagues for their support and help:

(1) Bernard Previtali, Jean-Michel Hartmann, Francois Andrieu, Jean Guerrero, Karim Yckache and Vincent Mazzocchi have helped me a lot on the fabrication of electrical batches and samples in the clean rooms.

(2) Claude Tabone, Mikaël Cassé, Xavier Garros, Jacque Cluzel, Patrick Grosgeorges, Cyrille Le Royer, Louis Hutin, Rabah Kies, Fabine Allain, Alain Toffoli, Laurent Brunet, Jean Coignus and Jocelyn Berthoz have given me so much assistance on device characterization, parameter extraction and performance analysis. Xavier Mescot, Sorin Cristoloveanu and Fanyu Liu have assisted me a lot on the four point probe and Hall Effect tests.

(3) Quentin Rafhay, Benoit Sklénard, Krunoslav Romanjek, Marie-Anne Jaud, Pierette Rivallin and Jérôme Mazurier have helped me a lot on device simulation and modelling.

All the jury members are greatly appreciated for their precious time reviewing my thesis: Mr. Emmanuel Dubois from CNRS/IEMN, Mr. Filadelfo Cristiano from CNRS/LAAS, Prof. Francis Calmon from INSA-Lyon, Mr. Scott Luning from Globalfoundries.

Also, I would like to thank all my friends from different countries I got to know in the past three years. I will miss the happy time in Grenoble: hiking, picnic, the nice dinners/beers/wine, camping, swimming, cycling and so on. In addition, I get the interesting chance to know more about different cultures.

All my friends out of France who have supported, helped and encouraged me are all appreciated. I am so happy to have such good friends like you.

In the end, I would like to thank my family for their love. Special thanks to my parents and my husband.

Contents

List of Symbols 3

List of Abbreviations 6

Chapter I :Introduction 8

I.1 Why 3D? 9
I.2 How to obtain 3D? 11
I.2.1 3D Parallel integration 11
I.2.2 3D Sequential integration 12
I.2.2.1 Top active layer: Seed Window based Recrystallization/Epitaxy 13
I.2.2.2 Top active layer: Molecular bonding 14
I.2.3 Why 3D sequential integration with wafer bonding for top active layer? 15
I.3 Challenges of 3D sequential integration 16
I.4 Remaining challenges at the beginning of this PhD 17
I.5 Context of this work 18

Chapter II : Optimization of LT FDSOI transistors 20

II.1 LT SPER activation 21
II.2 Challenges of LT SPER FDSOI 27
II.2.1 Full pre-amorphization of Si 27
II.2.2 LDD to gate underlap 28
II.3 LT FDSOI performance optimization 30
II.3.1 nFET performance optimization 30
II.3.1.1 nFET Fabrication 30
II.3.1.2 I_{OFF}-I_{ON} and SCE control 32
II.3.1.3 L_G dependence of device performance 34
II.3.1.4 Access resistance analysis 35
II.3.1.5 Gate to channel interface quality 36
II.3.1.6 EOT-L_G extraction 37
II.3.1.6.1 Theory of EOT extraction on small FDSOI transistors 38
II.3.1.6.2 Experimental extraction of EOT 40
II.3.1.7 Explanation of performance dependence on L_G 41
II.3.2 LT FDSOI optimization: pFETs 41
II.3.2.1 pFETs fabrication 41
II.3.2.2 Gate stack quality 44
II.3.3 Work function engineering for V_{TH} tuning 45
II.4 Conclusions 47

Chapter III : GIDL optimization of LT transistors 49

III.1 Gate Induced Drain Leakage (GIDL) 50
III.1.1 GIDL and its generation mechanisms 50
III.1.2 Influence of LT SPER on GIDL 52
III.2 Discrimination of GIDL mechanism 53
III.2.1 Traditional method 53
III.2.2 Improved approach 56
III.2.3 Theoretical variation of the new approach 59
III.3 Experimental GIDL mechanism discrimination in SOI 61
III.3.1 Specific challenges of SOI 61

III.3.1.1 Gate current identification 61
III.3.1.2 SRH identification 64
III.3.2 Experimental results on FDSOI 65
III.4 GIDL improvement by defect engineering 67
III.5 Conclusions 70

Chapter IV : Deactivation of LT SPER activated dopants 72

IV.1 Defect evolution and dopant deactivation 73
IV.1.1 Defect evolution during post activation anneal 73
IV.1.2 Dopant deactivation mechanisms 74
IV.1.2.1 Solid solubility 74
IV.1.2.2 Boron deactivation mechanism 75
IV.1.2.3 Arsenic deactivation mechanism 77
IV.2 Boron activation and deactivation: Experiment and results 80
IV.2.1 Experiment 80
IV.2.2 Boron activation study 82
IV.2.3 Boron deactivation study 83
IV.3 Arsenic activation and deactivation: Experiment and results 85
IV.3.1 Experiment 85
IV.3.2 Arsenic activation: LT SPER versus spike 86
IV.3.3 Deactivation of LT SPER arsenic on SOI 87
IV.4 Conclusions 88

Chapter V : Conclusions and perspectives 90

V.1 Conclusions 90
V.2 Perspectives 93

Résumé en français 95

References 103

Publications 121

List of Symbols

Symbol	Meaning	Unit
B	Parameter of gate induced drain leakage model	MV/cm
$C^{sol}_{As,tot}$	Solid solubility of Arsenic	cm^{-3}
C^{sol}_{As+}	Active solid solubility of Arsenic	cm^{-3}
C_{if}	Inner fringing capacitance	F
C_{gc}	Gate to channel capacitance	F
C_{of}	Outer fringing capacitance	F
C_{OV}	Overlap capacitance	F
C_{OX}	Gate capacitance	F
$C_{OX\ A}$	Gate capacitance normalized by gate area	F/cm^{-2}
C_{par}	Parasitic capacitance	F
D_{it}	Interface State Density	cm^{-2}
DIBL	Drain Induced Barrier Lowering	mV
E	Effective electric field	M/cm
Eg	Band gap of Silicon	eV
E_a	Activation energy of current	eV
E_i	Intrinsic energy level	eV
E_t	Energy level of traps	eV
F	Electric Field	V/cm
G_{max}	Maximum conductance	µS/µm
I_D	Drain current normalized by the channel width	A/µm or µA/µm
I_{Dlin}	On state current in linear regime, normalized by the channel width	A/µm or µA/µm
I_S	Source current normalized by the channel width	A/µm or µA/µm
I_G	Gate current normalized by the channel width	A/µm or µA/µm

I_{Dmin}	Minimum drain current achievable	A/µm or µA/µm
I_{ON}	On state current normalized by the channel width	A/µm or µA/µm
I_{OFF}	Off state current normalized by the channel width	A/µm or µA/µm
k/k_b	Boltzmann's constant	$J.K^{-1}$
L_G	Gate length	nm or µm
L_{Gmask}	Gate length designed on mask	nm or µm
m*	Effective tunneling mass of carriers	kg
N_0	Doping concentration in the channel	cm^{-3}
N_D	drain doping concentration in the gate to drain extension overlap region	cm^{-3}
Ns	Active dose of dopants	cm^{-2}
q	Elementary charge	C
R_{access}	Access resistance	Ω.µm
Rs	sheet resistance	Ohm/square
R_{TOT}	V_D/I_D ate $\|V_D\|$=50 mV and a gate overdrive of 0.8V	Ω.µm
R_{Tunnel}	Local generation rate of tunneling	cm^{-3}
SS	Subthreshold Swing	mV/dec
T	temperature	°C
$T_{a\text{-}Si}$	Thickness of amorphous Silicon	nm
$T_{EOR\ BOX}$	Distance between top of EOR defects band and BOX	nm
T_{HfO2}	Thickness of HfO_2	nm
T_{Si}	Si thickness	nm
T_{Seed}	Seed thickness	nm
T_{ILD}	Thickness of inter layer dielectric	nm
W	Gate width	nm/µm
W_{mask}	Gate width designed on mask	nm or µm
V_{bi}	Build in potential of the junction	V

V_D	Drain Voltage	V
V_{DG}	Drain to Gate Voltage	V
V_{fb}	Flat band voltage in the gate to drain overlap region	V
V_G	Gate Voltage	V
V_{GS}	Gate to Source Voltage	V
V_{TG}	Gate voltage where gate current equals one critical gate current	V
V_{TH}	Threshold Voltage	V
V_S	Source Voltage	V
ΔIdsat	Variation of drain current in saturation regime	-
ΔV_{TH}	Difference between Threshold Voltages	mV
μ	carrier mobility	cm^2/Vs
μ_{eff}	effective carrier mobility	cm^2/Vs
θ	Implant tilt	°
ψ_S	Surface potential	V
ε_{ox}	Permittivity of SiO_2	$F.m^{-1}$
ε_{Si}	Permittivity of Si	$F.m^{-1}$
$\hbar$	Reduced Plank's constant	J.s
σ	Fitting parameter in the model of gate induced drain leakage	-
Γ	Fitting parameter in the model of gate induced drain leakage	-
γ	Fitting parameter in the model of gate induced drain leakage	-

List of Abbreviations

Abbreviation	Meaning
ALD	Atomic Layer Deposition
BEOL	Back End Of Line
BTBT	Band To Band Tunneling
BOX	Buried Oxide
CMP	Chemical Mechanical Polishing
CTRIM	Crystal TRIM
EOR	End Of Range
EOT	Equivalent Oxide Thickness
FDSOI	Fully Depleted Silicon On Insulator
FEOL	Front End Of Line
FE SRH	Field Enhanced Shockley-Read-Hall recombination
FET	Field- Effect Transistor
GIDL	Gate Induced Drain Leakage
HDD	Highly Doped Drain
High-k	Material with a high dielectric constant (compared to SiO_2)
HT	High Temperature
IC	Integrated Circuits
ILD	Inter Layer Dielectric
ITRS	International Technology Roadmap for Semiconductors
KMC	Kinetic Monte Carlo
KOZ	Keep Out Zone
LDD	Lowly Doped Drain
LT	Low Temperature
MOSFET	Metal-Oxide-Semiconductor Field- Effect Transistor

nFET	Field-Effect Transistor with a n-type conduction channel
PAI	Pre-Amorphization Implant
pFET	Field-Effect Transistor with a p-type conduction channel
RC	Resistance Capacitance
RTA	Rapid Thermal Anneal
RSD	Raised Source and Drain
SCE	Short Channel Effects
S/D	Source and Drain
SEM	Scanning Electron Microscopy
SOI	Silicon-On-Insulator
Si_i	Si interstitials
Si_v	Si vacancies
SPER	Solid-Phase Epitaxial Regrowth
SRH	Shockley-Read-Hall recombination
SW	Seed Window
T	Temperature
TAT	Trap-Assisted Tunneling
TED	Transient Enhanced Diffusion
TEM	Transmission Electron Microscopy
TSV	Through Silicon Via
XTEM	Cross-Sectional Transmission Electron Microscopy
a-	Amorphous
a/c	amorphous/crystalline
c-	Crystalline

Chapter I : **Introduction**

Abstract- The MOSFET scaling is vital for the unprecedented development of integrated circuits (IC). However, the scaling of MOSFET has been suffering from the short-channel effect (SCE) and the increasing interconnection delay. Another difficulty for further scaling is the increasing production cost from technologies for achieving small dimension. One attractive way to alleviate these challenges and to continue Moore's law would be 3D integration *i.e.* stacking devices on top of each other.

In this introduction chapter, we will recall the challenges of device scaling and explain why 3D integration is interesting. In the second section, different approaches of 3D integration (3D parallel/sequential integration) will be reviewed and compared, and the advantages of 3D sequential integration will be highlighted. In the third section, the challenges of 3D sequential integration will firstly be reviewed. Then solutions achieved in the previous work will be reviewed. In the end, the remaining challenges at the beginning of this PhD project and the motivations of this work will be described.

I.1 Why 3D?

In last few decades, life has been dramatically changed in various aspects by the development of electronic devices, such as the personal computer, digital camera, cell phone and multimedia players, which have been getting faster, more portable, more functional, without increasing the cost [Haselman'10]. All of these are realized based on the scaling of the metal-oxide-semiconductor field-effect-transistor (MOSFET) which constitutes the basic unit of the integrated circuits (IC). Since the 1960s, the physical dimensions of MOSFET have been continuously scaled down following Moore's law (Fig.I.1), which predicts that the number of transistors per IC is doubled every 18 months [Moore'65].

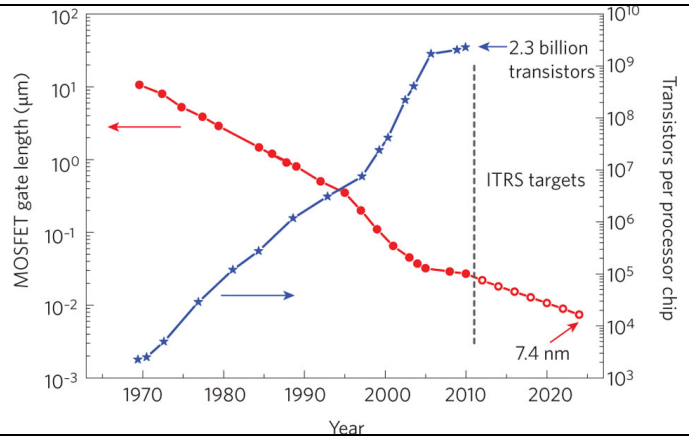


Fig.I.1 Trends in digital electronics [Schwierz'10]. The evolution of MOSFET gate length in production-stage integrated circuits (filled red circles) and International Technology Roadmap for Semiconductors (ITRS) targets (open red circles). As gate lengths have decreased, the number of transistors per processor chip has increased (blue stars).

The further scaling of MOSFET on 2D IC is impeded by the following limitations:

(I) Device performance: Short Channel Effect (SCE) of scaled MOSFET tends to be more serious, which will strongly increase the leakage current and power consumption [Roy'03, Yang'08]. To continue the miniaturization of MOSFET, introduction of new technologies has been necessary (Fig.I.2): (a) high-k/metal gate, strained silicon, gate-last structure have been needed [Kuhn'12, Nishikawa'09]; (b) some changes are now required in the MOS architecture for better electrostatic control: fully depleted silicon-on-insulator (SOI) [Skotnicki'11, Planes'12, Khakifirooz'12, Faynot'10] and multi-gates structures [Bohr'11] are brought up into production; (c) and high mobility materials for enhanced carrier mobility are forecasted to keep up with the performance increase requirements [Kuhn'12].

(II) Fabrication limitations: In front end of line (FEOL) process, the miniaturization of device feature requires more complex photolithography and etching systems, raising the production cost [Khorram'12]. Reliability and variability [Kuhn'11, Mazurier'11] are also becoming serious concerns as device scales down.

(III) System performance: Device engineers have been boosting device performance at the cost of device leakage [Haensch'08]. Moreover, the interconnection length is getting longer and longer. As a result, the power consumption and RC delay increase dramatically.

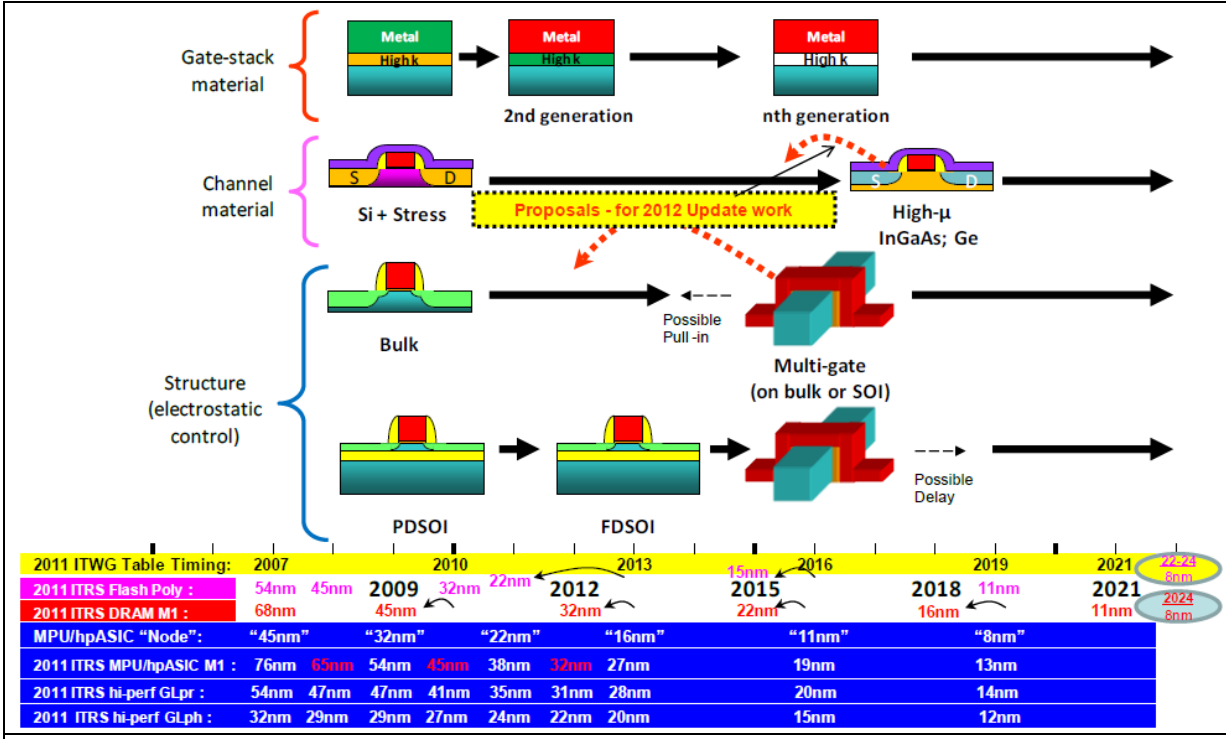


Fig.I.2. Scaling trend and evolution of technologies projected by ITRS 2011 [ITRS'11].

To push the limits of Moore's law, 3D integration is very attractive [Iyer'09]. 3D integration can help to shorten the long horizontal interconnections into vertical connections, which can help to reduce power dissipation and RC delay. In addition, depending on the 3D integration approach, 3D integration might offer the following benefits: increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, reduced overall cost, multi-functionality and flexible heterogeneous integration [Lu'09]. As shown in Fig.I.3, future 3D integration enables multi-functionalities IC with high integration density.

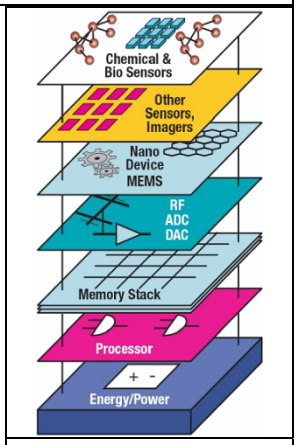


Fig.I.3 A vision of future 3D hyper-integration [Lu'09].

I.2 How to obtain 3D?

In this thesis, we focus on the wafer level 3D integration with crystalline Si on both bottom and top layer. The basic concept of 3D integration is to stack multiple 2D active layers to achieve higher integration density and shorter interconnections. Based on this concept, there are different manufacturing technologies to realize 3D integration: (I) 3D parallel integration where the chips/wafers are firstly preprocessed, followed by the bonding and connections between layers; (II) 3D sequential integration where the active layers and the devices on different active layer are fabricated sequentially one after the other.

I.2.1 3D Parallel integration

In the parallel 3D integration, multiple 2D chips are firstly fabricated in parallel by standard CMOS processes. Considering the realization of bonding and connection of different layers, there are different techniques. Through-Silicon-Via (TSV) is one interesting way. There are mainly four integration schemes for TSV, e.g. via first, via middle and via last [Knickerbocker'08]. A schematic plot of 3D integration by via middle is shown in Fig.I.4.

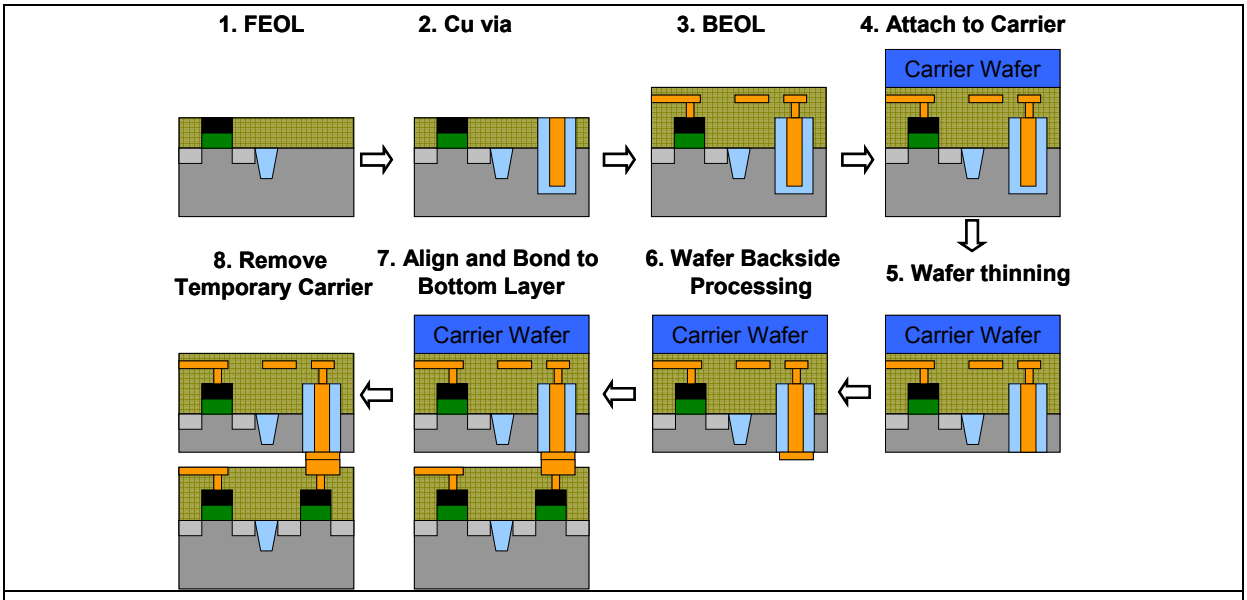


Fig.I.4. Schematic view of the 3D stack fabricated by 3D parallel integration process with via middle scheme [I-micronews].

3D parallel integration is challenged by the following factors:

(I) The interconnection density is limited by the alignment precision of bonding [Koyanagi'09]. In 3D parallel integration the best bonding alignment reported is

in the range of 0.18 µm [Topol'05] to 0.5 µm [Chen'07, Koyanagi'09]. Even for an alignment of 0.1 µm, the maximum TSV density is limited to be around $2x10^8$ vias/cm^2, which is much lower than 10^{10} contacts/cm^2, the contact density in planar integration of 45 nm node [Batude'09a]. So the highest integration density and yield achievable in a 3D design are limited, due to the large landing area required to yield the 3D vias [Steen'07].

(II) The TSV trench has extremely high aspect ratio (up to 10) [Wolf'08] and thus imposes challenges on the fabrication processes, such as dry etching, deposition and filling of vias.

(III) TSV generates stress which can degrade the carrier mobility, reliability and variability of transistors in the vicinity of the TSV [Ryu'12]. To avoid these degradations, devices should be located outside the Keep Out Zone (KOZ) surrounding each TSV [Ryu'12, Mercha'10]. In [Mercha'10], KOZ of TSVs with 5.3 µm diameter and 40 µm depth are studied: KOZ is demonstrated to be 20 µm for a single TSV and increases to 200 µm for a large TSV matrix for analog FETs with 0.5% ΔIdsat threshold. This seriously limits utilization of the third dimension.

I.2.2 3D Sequential integration

Unlike 3D parallel integration, in 3D sequential integration, the devices on different layers are fabricated sequentially. As illustrated in Fig.I.5, the bottom devices are firstly fabricated (Fig.I.5-a). Then, Inter Layer Dielectric (ILD) and top active layer are realized (Fig.I.5-b). Thirdly, top FETs are fabricated.

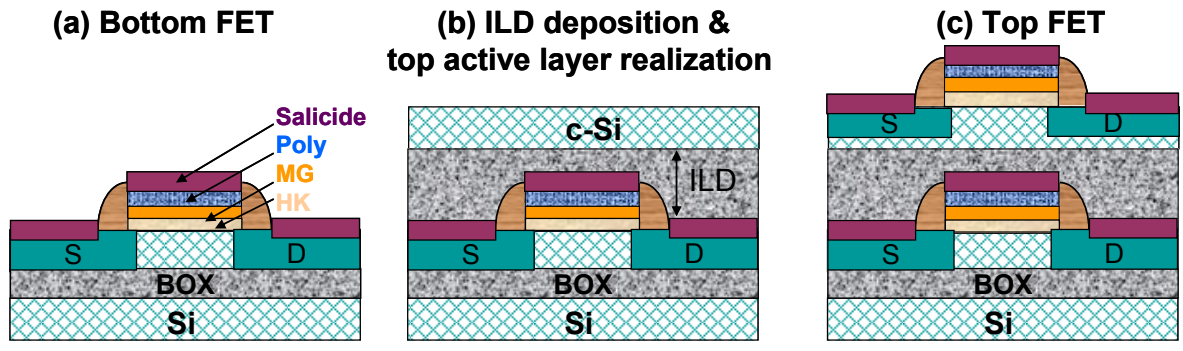


Fig.I.5. Schematic plot of 3D sequential integration: (a) fabrication of bottom FETs; (b) deposition of Inter Layer Dielectric (ILD) and realization of top active layer; and (c) fabrication of top FETs.

Depending on how the top crystalline active layer is achieved, there are mainly two approaches of 3D sequential integration: the concept will be briefly introduced in the following sub-sections. In [Batude'09a], detailed review of the history of 3D sequential integration is made. In 3D sequential integration, the alignment between top and bottom layers is limited by lithography. Alignment around 10 nm can be achieved, which is much better than that of 3D parallel integration [Batude'11b].

I.2.2.1 Top active layer: Seed Window based Recrystallization/Epitaxy

Seed Window (SW) based techniques mainly have two groups:

(I) SW based recrystallization (Fig.I.6): (a) Seed Window formation; (b) Deposition of amorphous Si (a-Si); (c) re-crystallization (by laser anneal [Jung'10] or RTP @ 600°C [Kumar'01]) with the seed information through SW.

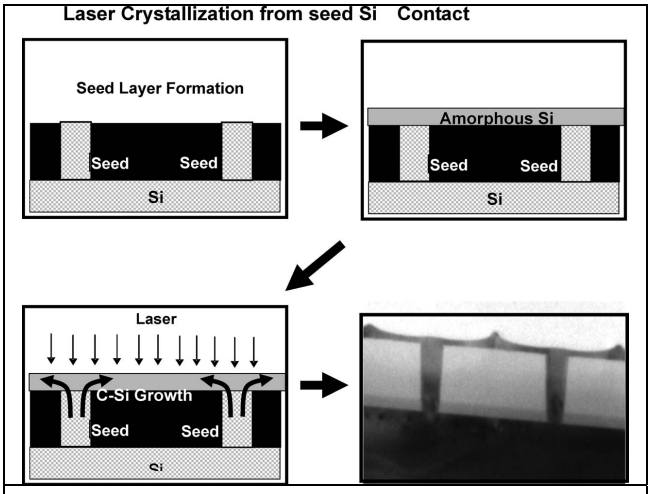


Fig.I.6. Vertical schematic illustrations and TEM image of a laser-crystallized single-crystalline Si layer on ILD [Jung'10].

(II) SW based epitaxial regrowth (Fig.I.7): (a) Seed Window growth; (b) formation of Damascene channel and epitaxy growth of crystalline Si (c-Si); (c) Planarization of top active c-Si. The SW based epitaxial regrowth can also be applied to achieve top Ge layer [Feng'06].

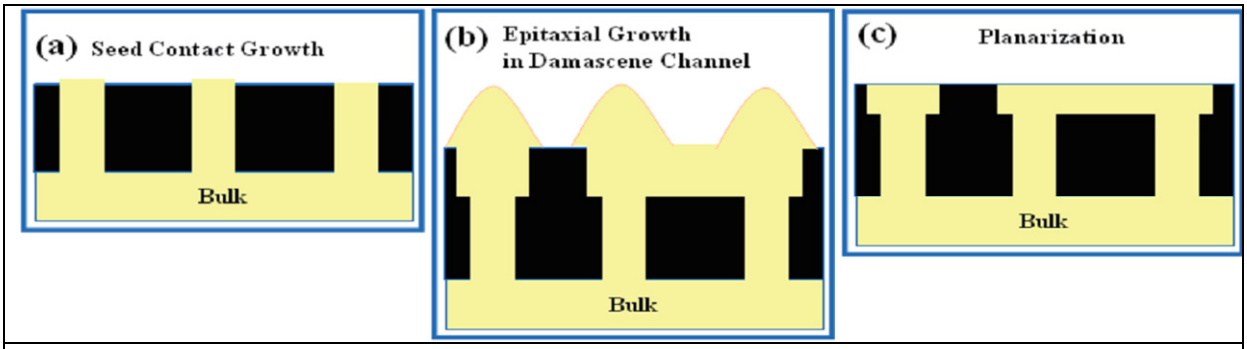


Fig.I.7 Vertical Schematics of the formation of single-crystalline Si layer on Inter Layer Dielectrics (ILD) [Jung'07].

The main disadvantages of SW methods are summarized below:

(I) The integration density is limited. Since seed windows are needed for the recrystallization of the amorphous layer, and grain boundaries [Jung'10] exist in the middle of two seed windows, the coverage of top active layer over the bottom substrate is limited.

(II) The control of thickness of top active layer is poor. As a consequence, this approach is not suitable for the fabrication of Fully Depleted Silicon On Insular (FDSOI) devices.

(III) The quality of top active layer is poor. Defects have been observed in the regrown top Si layer between two seed window [Jung'10] and the regrown Ge layer in the seed window region [Feng'06].

I.2.2.2 Top active layer: Molecular bonding

To overcome the limitation of the former approach for realizing top active layer, molecular bonding is a promising technique. CEA-LETI has demonstrated molecular bonding for the realization of top active layer with high crystalline quality, as illustrated in Fig.I.8 [Batude'11b].

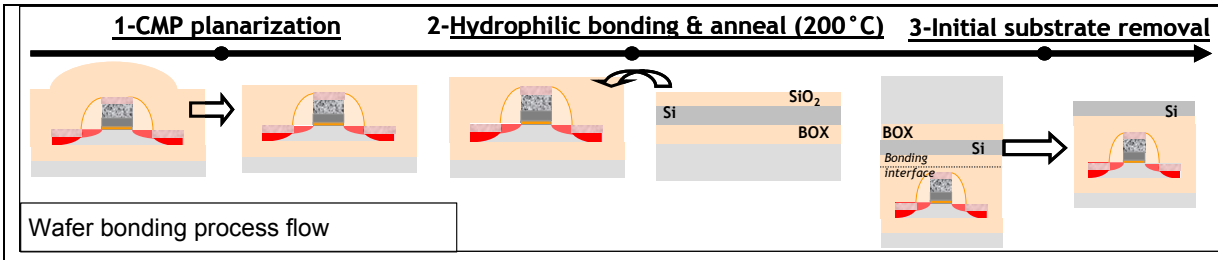


Fig.I.8.Description of the process flow of molecular wafer bonding in 3D sequential integration at CEA-LETI [Batude'11b].

Firstly, after the fabrication of the bottom MOSFET using the standard FDSOI process, inter layer dielectric is deposited and then planarized by chemical mechanical polishing. Secondly, hydrophilic bonding of SOI substrate is carried out, a low temperature annealing (200 ºC) was performed to strengthen the bonding interface. Then, the initial substrate (handle wafer) is removed by selective etching, and top active layer with high crystalline quality is realized for the fabrication of top FET. Also, molecular bonding offers the possibility to co-

integrate different surface and channel orientations such as <100> for bottom active layer and <110> for top layer without any additional process challenges [Vinet'11].

I.2.3 Why 3D sequential integration with wafer bonding for top active layer?

Considering the realization of top active layer, the molecular bonding technique can offer the following advantages with respect to the recrystallization/regrowth technique:

(I) SW is avoided and higher integration density can be achieved.

(II) The bonded top active layer offers better thickness control and better quality than that of top active layer by the recrystallization/regrowth technique. In addition, the film thickness can be accurately controlled.

(III) It allows independent optimization of pFETs and nFETs by fabricating them on different layers, through different choices on channel orientation/material and strain options [Vinet'11].

(IV) The process temperature is much lower. The thermal budget of the molecular bonding is 200 ºC, which avoids degrading the performance of bottom devices.

Comparing to 3D parallel integration, 3D sequential integration with wafer bonding for top active layer offers the following advantages:

(I) It offers higher integration density thanks to its much higher alignment (~10 nm with respect to 0.5 μm).

(II) In addition, 3D sequential integration allows the interconnection at transistor scale and thus makes full use of the third direction.

(III) The fabrication of TSV with high aspect ratio is avoided.

3D sequential integration with the top active layer by wafer bonding is the best candidate for high density 3D IC integration [Batude'09a, Batude'11b]. Bottom and top FETs scaled down to 50 nm with an ultrathin ILD of 23 nm have been demonstrated (Fig.I.9) [Batude'11a]. The transfer voltage characteristic of functional 3D inverter with a pFET (L_G=50 nm) stacked on top of an nFET (L_G=50 nm) is shown in Fig.I.10, which stands for the inverter with the smallest transistors achieved in 3D sequential integration scheme [Batude'11a].

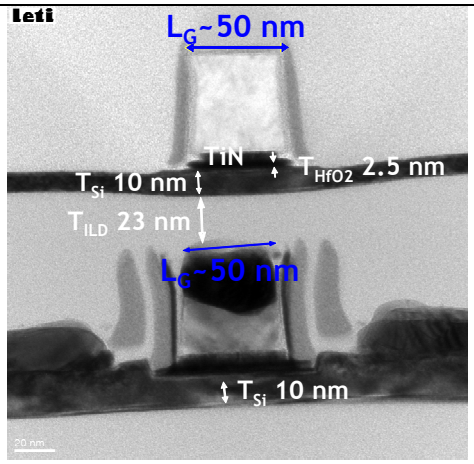


Fig.I.9 TEM cross-sections of stacked transistors with record L_G=50 nm and ultra thin interlayer dielectric T_{ILD}=23 nm, T_{Si}=10 nm [Batude'11a].

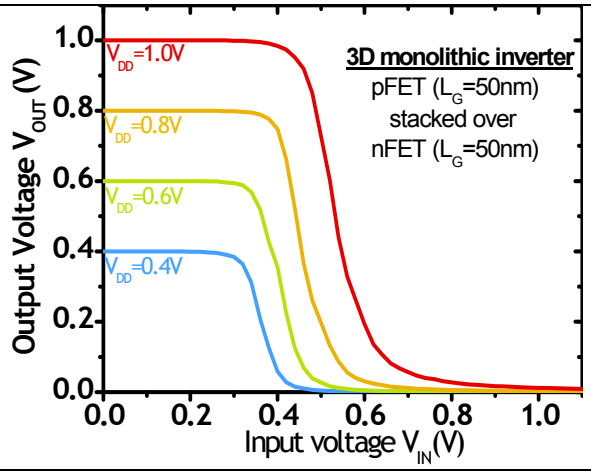


Fig.I.10 Inverter transfer voltage characteristic with pFET (L_G=50 nm) stacked over nFET (L_G=50 nm) [Batude'11a].

I.3 Challenges of 3D sequential integration

Compared to 3D parallel integration, 3D sequential integration faces some challenges in fabrication. The bottom FETs have to go through the realization of top active layer and the fabrication of top FETs, whose thermal budget can degrade the bottom transistor:

(I) The silicide of bottom FETs can be degraded. As shown in Fig.I.11, after annealing at 650 ºC anneal for 10 minutes, NiSi agglomerates and the sheet resistance is greatly increased (Fig.I.11).

(II) Extra dopants diffusion in bottom transistor can be induced, which will result in serious short channel effect in consequence.

In the previous work at CEA-LETI [Batude'09a], efforts to overcome the challenges have been made mainly in two aspects:

(I) Improving the thermal stability of silicide: NiSi has been stabilized up to 40 minutes anneal at 650 ºC, by Platinum incorporation together with the Fluorine and Tungsten implantation (Fig.I.11). The thermal stability of NiSi sets the maximum temperature allowed for top FET fabrication to be 650 ºC. So for the realization of top active layer and the fabrication of top FET, the processing temperature should remain below 650 ºC.

(II) Using low thermal budget process for the realization of top active layer and the fabrication of top FET: (a) The molecular bonding of top active layer has been

realized with a maximum thermal budget of 200 ºC; (b) Considering the fabrication of standard FDSOI FETs, the highest thermal budget is the source/drain dopants activation (>1000 ºC). To avoid such a high thermal budget, Low Temperature (LT @ 600 °C) Solid Phase Epitaxial Regrowth (SPER) has been applied to replace conventional spike anneal which features a peak temperature above 1000 ºC.

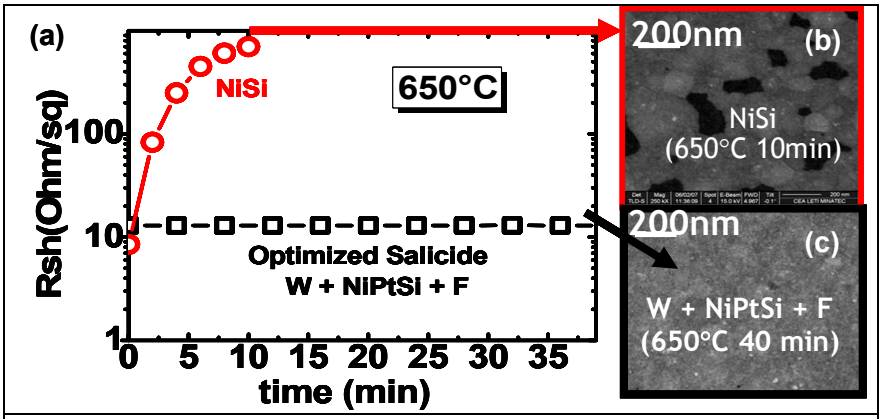


Fig.I.11 Evolution of silicide sheet resistance with annealing duration at 650 ºC (a) and SEM observations of (b) NiSi after (650 ºC, 10 minutes) anneal and (c) NiSi+Pt+W+F after (650 ºC, 40 min) anneal [Batude'08].

However, with the introduction of LT SPER for dopants activation of top FETs, 3D sequential integration faces new challenges which will be discussed in the following section.

I.4 Remaining challenges at the beginning of this PhD

At the beginning of this PhD project, 3D sequential integration faces the challenges of optimizing LT SPER process.

LT SPER activation has the following properties:

(a) Low diffusion which allows shallow junction;

(b) High dopant activation above solid solubility at thermal equilibrium;

(c) Residual End Of Range (EOR) defects.

Due to the specific properties of LT SPER, the main challenges of its application for FDSOI device fabrication are:

(1) Full pre-amorphization of the active Si layer, which can prevent the amorphous layer from recrystallization during LT SPER anneal;

(2) Source/drain to gate overlap might not be achieved, due to the weak diffusion of LT SPER activation. This tends to degrade the access resistance and I_{ON} performance in consequence;

(3) High Gate Induced Drain Leakage (GIDL) current can be induced either due to the abrupt junction or due to the residual defects;

(4) The LT SPER activated dopants are not thermally stable and tend to deactivate during post activation anneals. In addition, this deactivation can be enhanced by the residual EOR defects.

In this work, we have focused on overcoming the challenges above and the context of this work will be introduced in the following section.

I.5 Context of this work

In Chapter II, the mechanism and process flow of LT SPER will firstly be introduced, followed by the review of the properties of LT SPER and the challenges for its application for FDSOI fabrication.

After that, process optimization of n&p FDSOI FETs will be discussed to overcome the first two challenges: to avoid full pre-amorphization of active layer and to obtain source/drain to gate overlap in LT SPER process. The modification of effective work function of metal gate during activation anneal will be compared in LT and HT processed devices. This can help to gain some insight into the possibility of using LT SPER activation with gate first integration scheme for the fabrication of small scale transistors, instead of using gate-last integration which increases the complexity and cost of fabrication process.

In Chapter III, the third challenge of high GIDL current in LT SPER will be discussed. Firstly, it is shown that, for devices on thick SOI, the minimum drain current achievable of LT activated devices is 1.5 decades higher than that on conventional spike activated devices. The higher leakage can be induced either by the higher EOR defects density or by the higher junction abruptness. Then, an improved method is proposed for distinguishing the dominant generation mechanisms of higher GIDL current in LT SPER activated transistors: the EOR defects are found to play a major role. After that, GIDL performance of LT SPER activated FDSOI devices on extremely thin SOI will be compared to its HT counterparts.

In Chapter IV, the forth challenge, about deactivation of LT SPER activated dopants, will be discussed. To gain insight into the possibility of applying LT SPER activation in 3D sequential integration for both bottom and top FETs, the deactivation of LT SPER activated boron and arsenic on SOI samples with different Si thickness was studied.

In the end, the conclusions of our work and perspectives of 3D sequential integration will be shown.

Chapter II : **Optimization of LT FDSOI transistors**

Abstract- As discussed in Chapter I, in the 3D sequential integration scheme, the top FET can not be fabricated with conventional FDSOI process, due to its high thermal budget. In conventional FDSOI fabrication, the most critical thermal budget is the dopant activation anneal. Generally, the dopants are activated by spike anneal with a peak temperature around 1050 ºC. If conventional FDSOI process is applied for top FET, the bottom FETs will suffer from the high thermal budget of top FET. As a consequence, the bottom FET performance will be degraded. Particularly, a salicide agglomeration is expected to occur and degrade the access resistance seriously. Moreover, the dopants of bottom FET will diffuse, which will deteriorate the SCE control.

To avoid such a high thermal budget of top FET, High Temperature (HT, ~1050 ºC) dopant activation has been replaced by Low Temperature (LT, <650°C) Solid Phase Epitaxial Regrowth (SPER).

In this chapter, the mechanism and properties of LT SPER are briefly introduced in the first section. In the second section, the challenges of applying LT SPER for dopant activation of top FDSOI devices will be discussed in detail. In the third section, for both nFET and pFET, we will present the process optimizations required to reach similar performance to standard high temperature process: (1) The influence of LDD implant tilt on the trade-off between I_{OFF}-I_{ON} and SCE control will be analyzed for optimization; (2) The influence of activation anneals on the quality of gate to channel interface will be studied, proposals are also given to optimize device performance. In addition, in terms of effective work function modification and threshold voltage tuning, the additional advantage of LT SPER activation will be analyzed. This allows the further application of gate first integration scheme for the fabrication of high performance FDSOI at 20 nm node. Conclusions are given in the fourth section.

II.1 LT SPER activation

In standard MOSFETs, conventional high temperature activation is applied for dopant activation. However, as devices scale down, conventional HT anneal is facing the following challenges:

(I) The diffusion of dopant atoms during the activation anneal can degrade the short channel effect (SCE) control [Falepin'05];

(II) Dopant activation level is limited by the solid solubility, which confines the optimization of access resistance and I_{ON} performance [Foggiato'06];

(III) For scaled transistors, higher equivalent oxide thickness (EOT) is induced by the regrowth of interfacial SiO_2, consequently SCE control and I_{ON} are further degraded [Batude'09c, Gusev'06];

(IV) Challenge of threshold voltage (V_{TH}) tuning: during HT (700-900 ºC) [MacKenzie'07] anneal, the effective work function of metal gate tends to migrate towards mid-gap, which imposes challenges to achieve high performance devices with low V_{TH} [Wen'05, Hasan'07].

To overcome the challenges of HT anneal described above, LT SPER activation appears to be a promising alternative technique. In this section, the mechanism and properties of LT SPER activation will be described. As illustrated in Fig.II.1, LT SPER includes 3 steps [Olson'88, Colombeau'04a]:

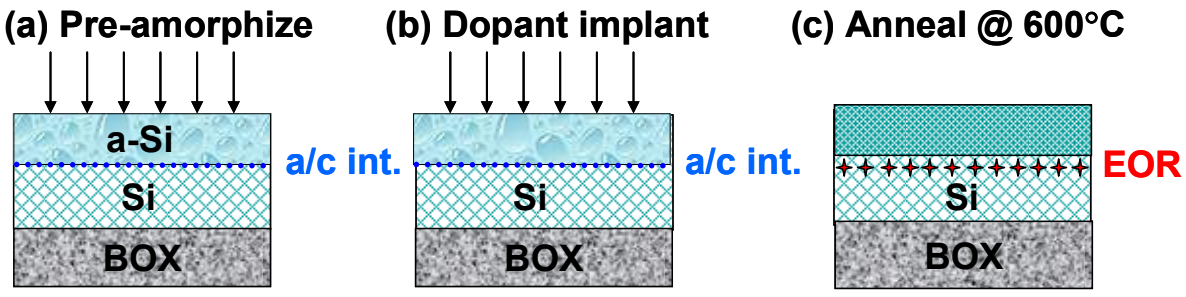


Fig.II.1 Schematic plot of LT SPER process: (a) the active layer is partially pre-amorphized; (b) dopant atoms are implanted into the semiconductor layer; (c) low temperature activation anneal (500-600 ºC), the pre-amorphized region recrystallizes and dopant atoms get activated. a/c int.: amorphous-crystalline interface. EOR: End Of Range defects.

(a) Pre-Amorphization- During ion implantation into single crystalline Si, the implanted ions tend to lose energy initially through elastic collisions with electrons of Si atoms

(electronic stopping), and then through inelastic collisions with the nuclei of Si atoms (nuclear stopping) [Ziegler'98]. During nuclear collision, if the energy transferred to a lattice Si atom exceeds a certain value (displacement energy for Si), the lattice Si atom will be displaced, meanwhile, a Si interstitial and a vacancy are generated and named as "Frenkel pair" [Nastasi'96]. Not only the primary implanted ions, but also the recoiled lattice atoms can collide with lattice atoms and introduce Frenkel pairs, this process is called collision cascade. In the collision cascade, many Frenkel pairs are recombined and only a fraction of the Frenkel pairs remain. The number of Si interstitials and vacancies that remain after ion implantation is dependent on the implant conditions (ion mass/dose, wafer temperature, and implantation dose rate). Higher defect density is expected for higher ion masses, energies and doses.

In the surface region of the implanted Si layer, when the generated defects accumulate into successive cascades, the highly damaged c-Si would become amorphous [Pelaz'04]. Generally, heavy atoms (e.g. Si, Ge) are used for Pre-Amorphization Implant (PAI). However, for heavy dopant atoms, (e.g. BF_2, As), pre-amorphization implant is not applied, since the dopant implant itself can amorphize the active layer.

(b) Dopant implant- Following pre-amorphization, dopant atoms are implanted into the active region. Thanks to the pre-amorphization implant, channeling effect is avoided. As a result, a shallower dopant profile can be achieved after the implant.

(c) LT SPER anneal- During the LT anneal, in order to minimize the free energy, the amorphous Si layer re-crystallizes, taking the underlying crystalline Si layer as a seed. Also, in the previous amorphous region, dopant atoms take the substitutional lattice position and become activated, as shown in Fig.II.2 (b). Frenkel pairs tend to recombine during the LT SPER anneal. In the crystalline Si region, the amount of Si vacancies is not enough to recombine with all the Si interstitials, so a band of Si_i.remains just below the previous a-c interface. During LT SPER anneal, the Si_i agglomerate into larger extended defects (such as defects clusters, {311}, dislocation loops) which are more stable [Claverie'02, Colombeau'04a, Kah'08]. Due to the facts that defect agglomeration/nucleation is faster than the LT SPER rate and self-diffusivity of Si is smaller in a-Si than in c-Si, the residual defects after LT SPER are located just below the former a/c interface, in the "end of range" region of

the pre-amorphization implant [Colombeau'04a, Pawlak'04a]. The residual defects are named End Of Range (EOR) defects.

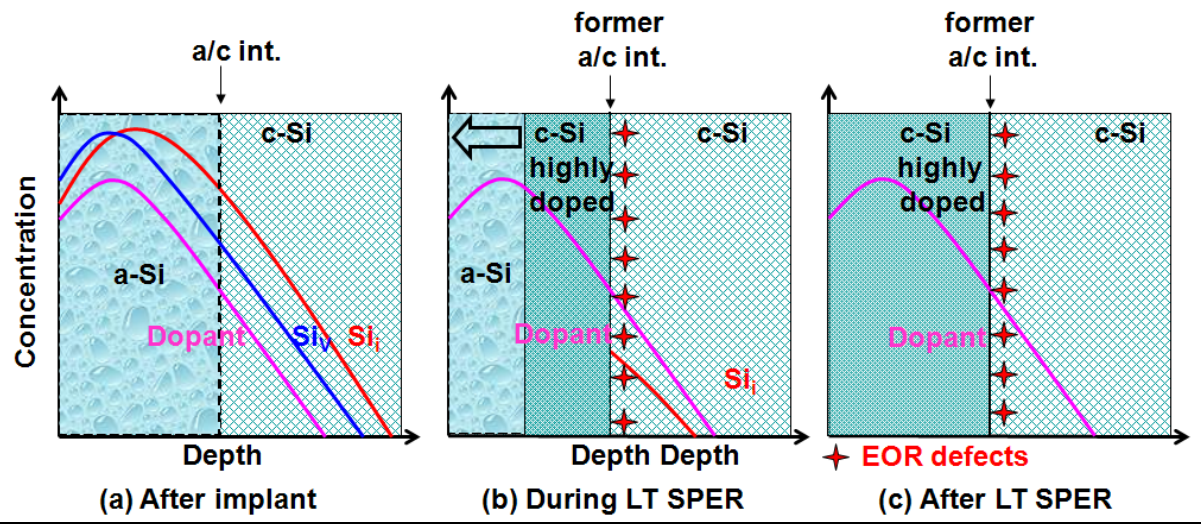


Fig.II.2 Defects and dopant profile evolution during LT SPER process. (a) Distribution of dopant, Si vacancies (Si_v) and Si interstitials (Si_i) after PAI and dopant implants. (b) During LT SPER anneal, with the bottom c-Si as a seed, a-Si recrystallizes towards its surface. (c) After LT SPER, dopants are highly activated and EOR defects are left below the former a/c interface [Cowern'05]. a/c int.: amorphous-crystalline interface. EOR defects: End Of Range defects.

Regrowth speed- LT SPER can occur at temperatures as low as 500 °C [Suni'82]. The regrowth rate is independent on the energy of pre-amorphization implant. However it is dependent on annealing temperature, crystal orientation and dopant incorporation. The regrowth rate increases with annealing temperature, as illustrated in Fig.II.3 [Johnson'07]. It is reported that for undoped crystalline Si, the regrowth rate is about 2.5 times higher in <001> Si than that in <110> Si [Csepregi'75]. Considering the influence of dopant incorporation, boron (B), arsenic (As), phosphorus (P) and aluminum (Al) are all shown to enhance SPER rate (Fig.II.3). And the incorporation of boron is shown to induce the strongest enhancement of SPER rate (Fig.II.3) [Johnson'07].

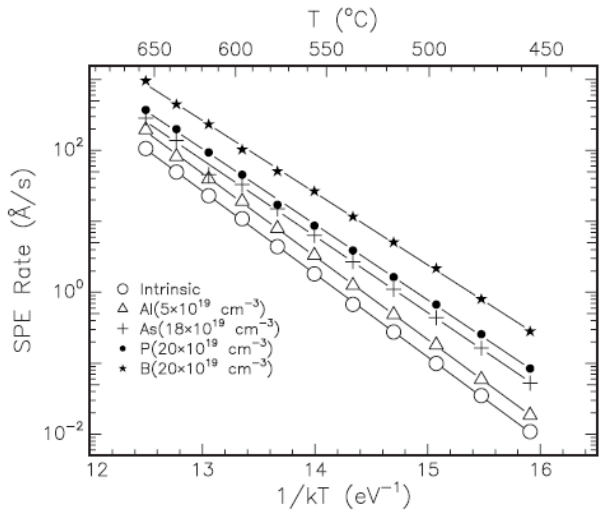


Fig.II.3 Arrhenius plot showing the temperature dependence of the SPER rate for intrinsic and uniformly doped a-Si layers. The incorporation of aluminum (Al), arsenic (As), phousphorous (P) and boron (B) increases the regrowth speed [Johnson'07].

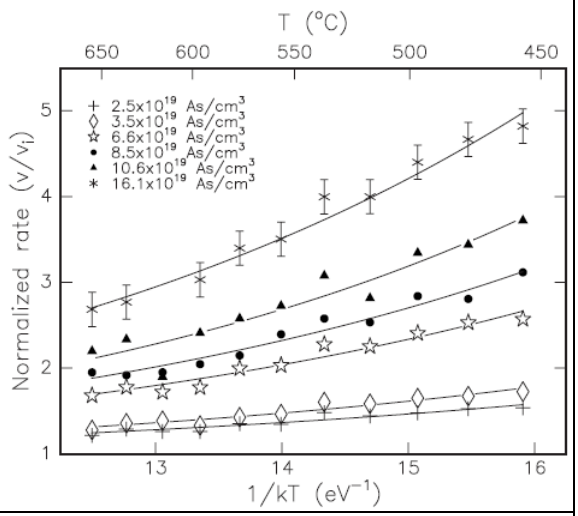


Fig.II.4 Arsenic-enhanced SPER rates for the front interfaces of buried a-Si layers normalized to the corresponding intrinsic SPER rate from [McCallum'99].

What's more, it is reported that the enhancement of the regrowth rate increases with the dopant concentration (Fig.II.4) and implanted dose (Table.II.1). In our LT FDSOI process, to ensure the successful regrowth of an entire a-Si layer around 20 nm, LT SPER anneal is carried out at 600 ºC for 1 minute.

Table.II.1 Comparison of regrowth rates after $1 \cdot 10^{15}$ cm^{-2} Ge PAI implants in Bulk Si and SOI, both without and with 500 eV boron implants with doses from $2 \cdot 10^{13}$ cm^{-2} to $2 \cdot 10^{15}$ cm^{-2} [Hamilton'05b].

	Regrowth rate (Å/sec)			
Boron dose (cm^{-2})	**8KeV Ge Bulk**	**8KeV Ge SOI**	**20KeV Ge SOI**	**20KeV Ge SOI**
0	**N/A**	**N/A**	**2.7**	**2.6**
$2x10^{13}$	**3.5**	**3.7**	**3.7**	**3.9**
$2x10^{14}$	**4.0**	**4.2**	**4.0**	**4.4**
$2x10^{15}$	**5.2**	**4.8**	**5.2**	**5.0**

Boron dose increases ↓ — **Regrowth rate increases** ↓

Advantages of LT SPER- Considering the junction, LT SPER offers the following two advantages:

(I) Abrupt junction can be achieved by optimizing the PAI implant and dopant implant. Thanks to the low diffusion of dopants at this temperature (500-600 ºC), the activated dopants are mainly confined in the previous amorphous region [Jin'02];

(II) High dopant activation is introduced by the non-thermal equilibrium activation process. The activated dopant atoms are in the metastable phase and high activation level, above solid solubility, can be achieved [Lindsay'04a].

Moreover, at device level, LT SPER activation is promising for two additional advantages:

(III) Smaller EOT has been reported, thanks to the lower regrowth of interfacial SiO_2 during the lower thermal budget anneal [Batude'09c] [Ragnarsson'06];

(IV) Better work function control is expected, thanks to its low thermal budget [MacKenzie'07]. By replacing the high temperature thermal anneal, the migration of effective work function towards mid gap can be avoided. Thus, a wider choice of materials is expected for effective work function tuning.

The advantages above make LT SPER a great candidate for ultra-shallow junction formation in advanced CMOS nodes [Lindsay'04b, Ragnarsson'06].

Disadvantage of LT SPER- However, the drawback of LT SPER is that due to the low thermal budget, End OF Range (EOR) defects can not be fully healed out after LT SPER anneal. As shown in Fig.II.5, the residual EOR defects are located just below the former a/c interface [Colombeau'04a].

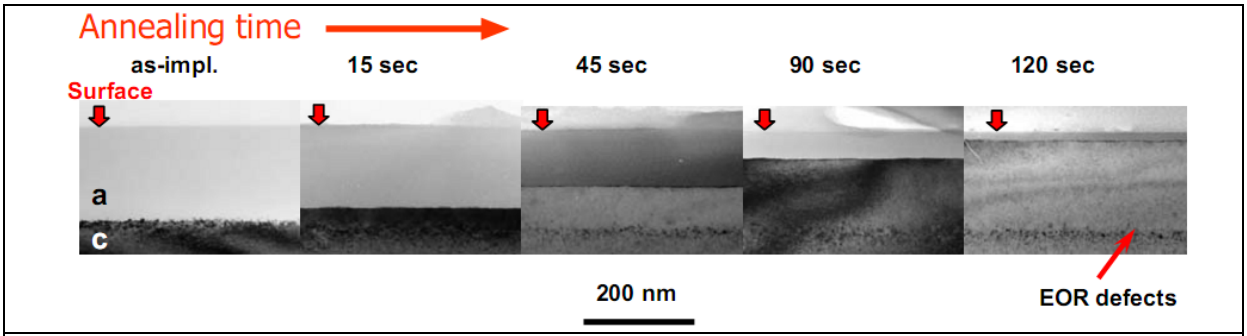


Fig.II.5 XTEM micrographs of SPER isothermally annealed at 600 ºC [Colombeau'04a]. After LT SPET anneal, EOR defects are left below the a/c interface.

During post anneal, the EOR defects evolve and act as a source of Si interstitials (Si_i) [Hamilton'07, Hamilton'05a]. The presence of Si_i can influence the dopant profile and device performance in three aspects:

(I) Dopant deactivation: The LT SPER activated dopants are in a meta-stable state [Lindsay'04a] and tend to deactivate during post activation anneals. As a result, LT SPER might lose its advantage in terms of high dopant activation. For activated boron atoms, due to the formation of Boron Interstitial Clusters (BICs), the activated boron atoms can be deactivated [Colombeau'04b]. The deactivation of boron in the temperature range of 700-900 ºC has been widely reported [Hamilton'06b, Hamilton'07, Pawlak'04b]. The activated arsenic atoms tend to become deactivated through the formation of As-Si vacancy clusters. Arsenic deactivation has been observed at temperatures around 550 ºC over 20hours [Nobili'99].

(II) Transient Enhanced Diffusion (TED): TED is a transient effect observed during the initial stage of post implantation anneals, and the diffusion coefficient is much higher than the typical value [Claverie'96, Claverie'03]. As shown in Fig.II.6, the TED of boron mainly occurred very quickly. After the initial 35 minutes, the dopant profile is stabilized and the diffusion during the following 145 minutes is negligible [Michel'87]. It has been proven that the TED of boron is induced by the emission of Si interstitials from EOR defects [Eaglesham'94], which poses one challenge to the formation of ultra-shallow junction.

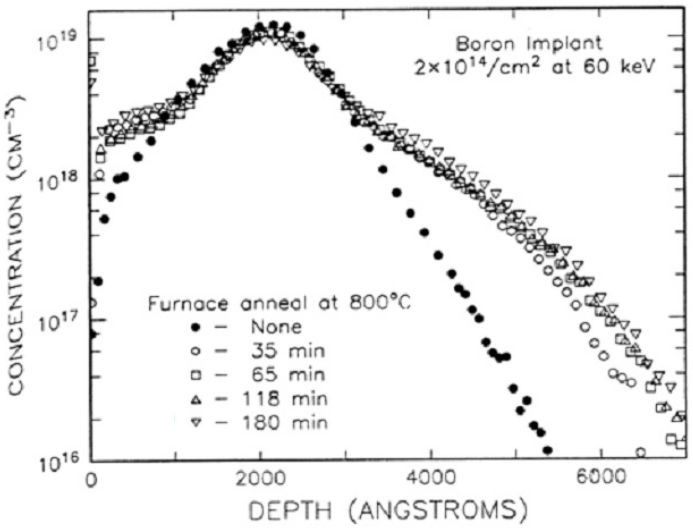


Fig.II.6 Isothermal anneals of B in Si showing transient effect of transient enhanced diffusion [Michel'87]. The TED of boron mainly occurs during the initial post anneal, and the boron diffusion after the initial 35 minutes can be neglected.

(III) Leakage increase: The EOR defects might induce higher leakage through the trap assisted tunneling and SRH generation [Chang'95]. On the other hand, thanks to

the low thermal budget of LT SPER, very abrupt junction can be achieved. However, the abrupt junction might induce higher electric field and increase the band to band tunneling leakage [Endoh'90].

In this section, the general challenges of LT SPER anneal on bulk device have been reviewed. In the following section, the specific challenge of LT SPER for FDSOI fabrication will be discussed.

II.2 Challenges of LT SPER FDSOI

II.2.1 Full pre-amorphization of Si

For scaled FDSOI devices, channel thickness should be decreased to maintain good electrostatic control of gate over channel and to suppress short channel effect. For a gate length of 20 nm, the Si thickness (T_{Si}) should be below 6 nm. Since the activated dopants are confined in the amorphous region, the active region should be amorphized as deep as possible (Fig.II.7), to improve access resistance and I_{ON} performance as a consequence.

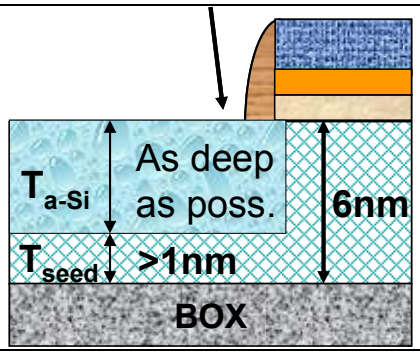


Fig.II.7 Schematic plot of a-Si and seed layer after LDD implant for access resistance reduction .

However, it is mandatory to avoid full pre-amorphization of the implanted active region. In our work, it is demonstrated that, for successful regrowth of the amorphous layer, the minimum crystalline Si seed thickness allowed is 1 nm [Xu'10]. As shown in Fig.II.8, lateral recrystallization is unable to promote S/D regrowth. In Fig.II.9, the sheet resistance of arsenic doped (3keV through 3 nm SiO_2) Si film is plotted as a function of Si thickness (T_{Si}) for several doses. Sheet resistance follows the theoretical $1/T_{Si}$ law up to a critical thickness (dependent on the dose) for which the film is fully amorphized during implantation, leading to

a dramatic increase of sheet resistance. From these data and atomistic Crystal TRIM (CTRIM) [Posselt'94] simulations providing amorphization thickness, it is deduced that the minimum silicon thickness required for efficient recrystallization is around 1 nm.

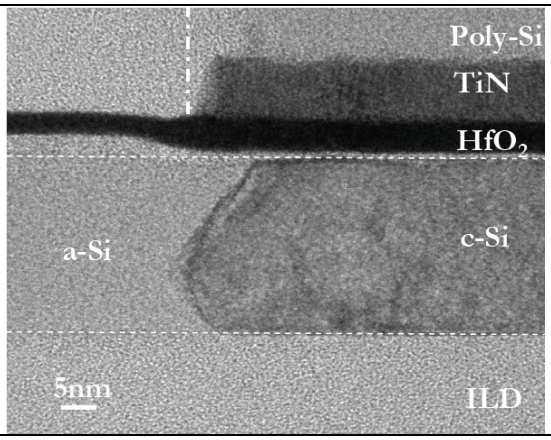


Fig.II.8 XTEM of a FDSOI FET after amorphizing implantation and 600 °C annealing. No lateral recrystallization is observed outside the gate.

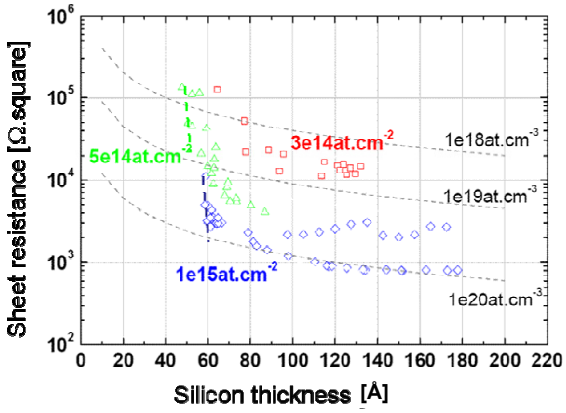


Fig.II.9 Sheet resistance as a function of Silicon thickness of a As implanted (3keV through 3 nm screen oxide) SOI film.

Thus the scaling down of FDSOI imposes challenges to the integration of LT FDSOI, especially when LDD is implanted before Raised Source and Drain (RSD) epitaxy. To overcome this challenge, the integration scheme should be modified [Grenouillet'11]. One way is extension last, that is to do amorphization implant after RSD epitaxy. The other way is extension first, in which amorphization implant is made before RSD epitaxy, but with a SiN capping layer on top of the active region. However, for both integration schemes, it is necessary to carry out accurate CTRIM or KMC (Kinetic Monte Carlo [Mok'07]) simulations to predict the amorphous Si thickness and to define the proper LDD implant energy.

II.2.2 **LDD to gate underlap**

In conventional high temperature FDSOI process, extension last is applied. As shown in Fig.II.10-(a), the LDD implant is carried out after the fabrication of first spacer and RSD fabrication, with a tilt of 20 °. During the following HT activation anneal, the dopant atoms get activated and diffuse towards the channel. In consequence, LDD to gate overlap is formed (Fig.II.10-(b)). However, in LT FDSOI process, due to the low diffusion of LT SPER

activation, LDD to gate underlap can occur, as illustrated in Fig.II.10-(c). The underlap will degrade the access resistance and I_{ON} performance in consequence.

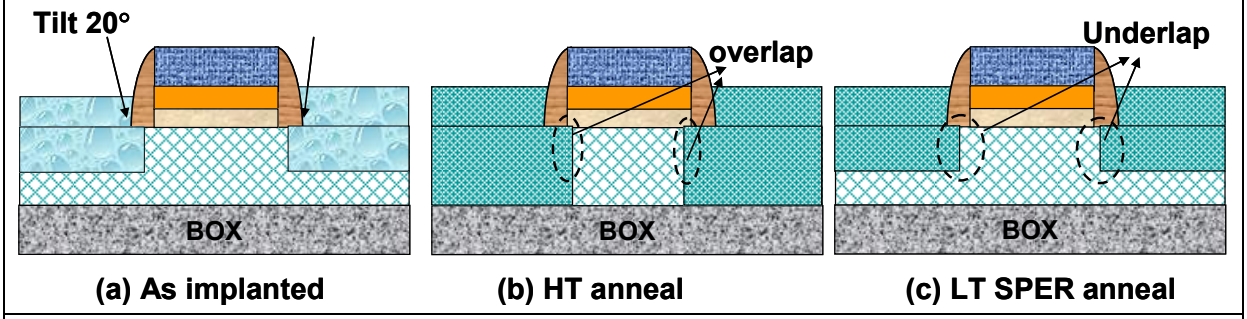


Fig.II.10 Schematic of as implanted dopant profile (a), LDD to gate overlap achieved in HT activation anneal (b), and LDD to gate underlap occurred in LT SPER activation anneal (c).

To overcome the challenge above, there are two possible solutions. The first possible solution is extension first: make LDD implant with low tilt of 7/10 ° before first spacer and RSD epitaxy (Fig.II.11-(a)). However, SCE control might be degraded due to the lateral spreading of implanted dopant atoms. In addition, the gate stack tends to be damaged due to the amorphization implant. The second possible solution is extension last, where higher tilt is applied to achieve wider as-implanted profile in the lateral direction [Shibahara'07, Kentaro'07]. Thus LDD to gate overlap may be achieved after LT SPER anneal, as shown in Fig.II.11 (b). In addition, the gate stack can be protected from being damaged by the LDD implant.

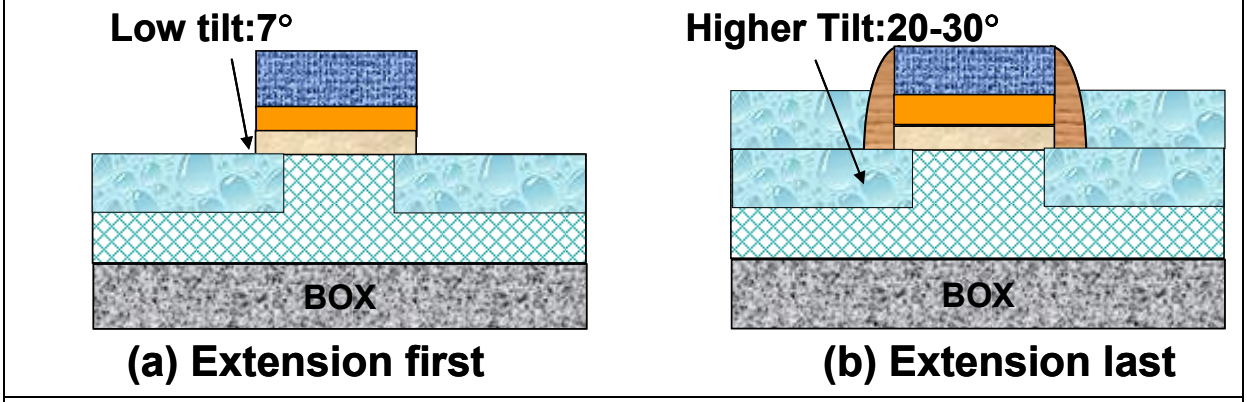


Fig.II.11 Schematic plots of possible solutions to maintain LDD to gate overlap with LT SPER activation process: (a) LDD implant before the first spacer; (b) LDD implant with higher tilt between 20 ° and30 ° after RSD epitaxy.

II.3 LT FDSOI performance optimization

The goal of this work is to get over the challenges above and find process conditions for achieving HT device performance with a LT (<650 ºC) process. In this section, we will focus on surmounting the two challenges of LT process: full pre-amorphization of active Si and LDD to gate underlap. The fabrication and optimization of LT nFETs and LT pFETs will be discussed in III.3.1 and III.3.2, respectively.

II.3.1 nFET performance optimization

II.3.1.1 nFET Fabrication

The full process flow of LT/HT FDSOI nFETs (T_{Si}~6 nm) is presented in Fig.II.12. The gate stack includes SiO_2(0.8 nm, plasma oxidation)/HfSiON(~1.9 nm)/TiN(5 nm, atomic layer deposition). The HfSiON layer is obtained by plasma nitridization (at 950 ºC) of atomic layer deposited HfSiO. The first SiN spacer is about 8 nm. Arsenic only LDD implant is applied, since arsenic can self-amorphize the implanted active region. To overcome the first challenge (full amorphization of active Si layer), arsenic implant is made after Si RSD epitaxy. Also, the implant energy has been optimized with KMC simulation, to ensure a residual seed thickness about 2 nm. Generally, LDD implant tilt of 20 º is used for HT process. However, to solve the second challenge of LT SPER (LDD to gate underlap), higher tilt might be required. So in LT splits, a split with LDD implant tilt of 30 º is processed in addition to the split with LDD tilt of 20 º. Considering dopants activation anneal, standard HT spike anneal with a peak temperature of 1080 °C is applied in standard HT process, whereas, in LT integration scheme, dopants are activated using LT SPER anneal at 600 °C for 1 minute.

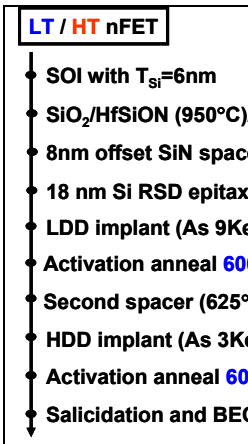


Fig.II.12 Process flow of LT/HT FDSOI nFETs.

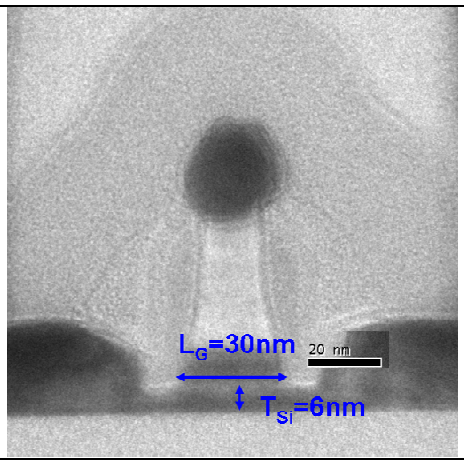


Fig.II.13 TEM coross section of LT FDSOI nFET with Si RSD. The TEM is taken after the salicidation step. The nFET features a gate length (L_G) of 30 nm, and the Si thickness (T_{Si}) in the channel is about 6 nm.

TEM cross section of LT nFET is shown in Fig.II.13. The nFET features a gate length of around 30 nm and a Si channel thickness around 6 nm. Also, the TEM figure shows good quality of RSD, which indicates the successful regrowth of amorphous Si layer during LT SPER activation.

Considering the electrical performance, for LT/HT nFETs with the same LDD implant tilt of 20° and L_G/W=30 nm/10 µm, I_D-V_G and I_D-V_D performances are firstly compared. For intuitive comparison, I_D-V_G and I_D-V_D curves of LT/HT devices with close V_{TH} are shown in Fig.II.14 and Fig.II.15, respectively. There are two phenomena unexpected: (I) The I_{Dmin} of LT/HT devices are close to each other, unlike the 1.5 decade higher I_{Dmin} in our former LT devices [Xu'10]; (II) For L_G/W=30 nm/10 µm, the LT activated devices overtake their HT counterparts. This is more obvious from the comparison of I_D-V_D curves at different gate bias overdrive (Fig.II.15). This indicates that the S/D can be connected to channel without increasing the implant tilt.

As we discussed in section II.2, due to the low diffusion of LT SPER activation, higher LDD implant tilt might be required to maintain the LDD to gate overlap. However, it is observed that without increasing the LDD implant tilt, even better performances are achieved in LT process. So, what is the optimized implant tilt for LT activation? To find the solution

and gain more insight into these phenomena, in the following sections, we will statistically analyze the electrical performance of different splits in detail.

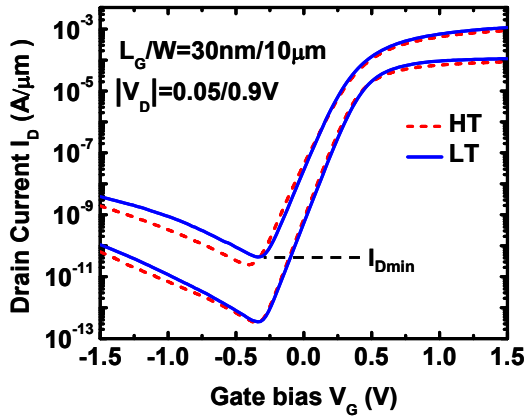


Fig.II.14 I_D-V_G curves of LT/HT nFETs (tilt=20 °, L_G=30 nm/W=10 µm), with LDD implant tilt of 20 °, at $|V_D|$=0.05/0.9 V. Similar device performances are achieved.

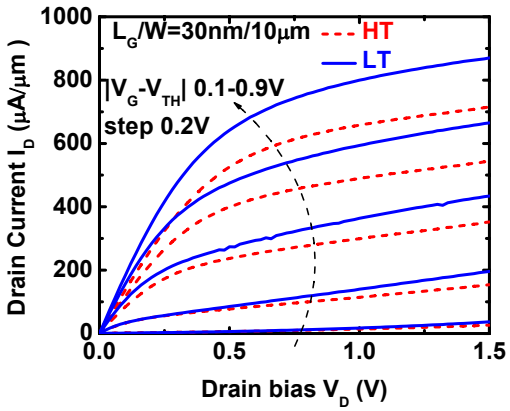
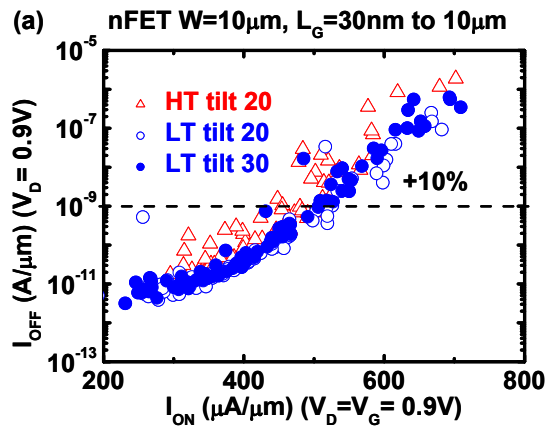


Fig.II.15 I_D-V_D characteristics of LT/HT nFETs (tilt=20 °, L_G=30 nm/W=10 µm) at different gate bias overdrive. LT nFET outperforms its HT nFET counterpart.

II.3.1.2 I_{OFF}-I_{ON} and SCE control

To optimize the LDD implant tilt of LT FDSOI nFETs, statistical analysis of I_{OFF}-I_{ON} and SCE control of different LT/HT nFETs will be carried out in this section.

Fig.II.16-(a) shows the statistical I_{OFF}-I_{ON} characteristic of LT/HT nFETs with various gate length and implant tilt. LT nFETs feature a better I_{ON}/I_{OFF} ratio than HT nFETs.



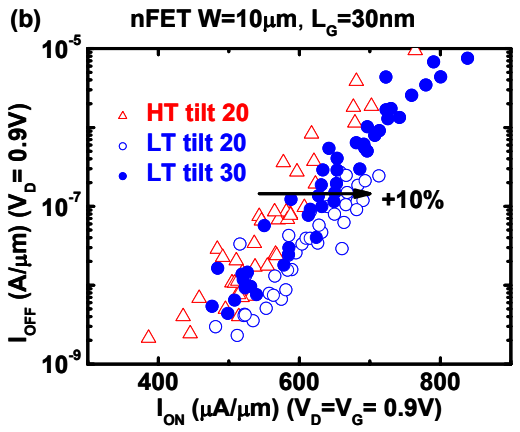


Fig.II.16 I_{OFF}-I_{ON} trade-off of HT/LT nFETs with W=10 µm, L_G between 30 nm and 10µm in (a). For W=10 µm, L_G=30 nm, the I_{OFF}-I_{ON} trade-off is highlighted in (b). At a constant I_{OFF} of 10^{-9} A/µm, I_{ON} of LT nFETs are ~ 10% higher than that of HT nFETs.

For a constant I_{OFF} of 10^{-9} A/µm, I_{ON} of LT nFETs are about 10% higher than that of HT nFETs. Fig.II.16-(b) highlights the 10% improvement of I_{OFF}-I_{ON} trade-off of LT splits with L_G=30 nm, W=10 µm.

To gain more insight into the trade-off between access resistance (R_{access}) and SCE control, the R_{TOT} (V_D/I_D at $|V_D|$=50 mV/$|V_G-V_{TH}|$=0.8V) vs. DIBL trade-off of LT/HT nFETs is compared in Fig.II.17. The LT/HT splits show similar R_{access} and SCE control trade-off, which indicates that the LDD extension is overlapped to gate for LT nFET splits with implant tilts of 20 ° and 30 °.

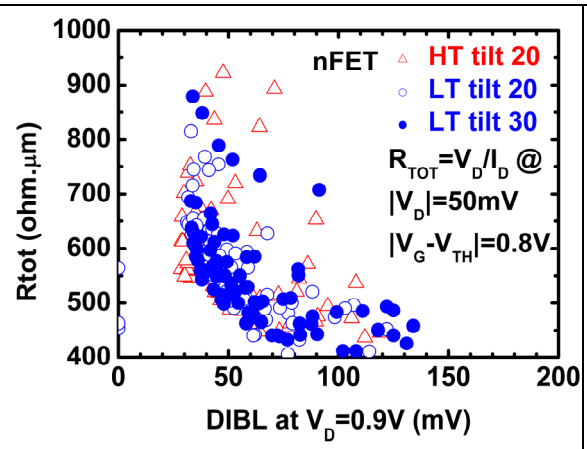


Fig.II.17 R_{TOT}-DIBL of HT/LT nFETs with W=10 µm, L_G between 30 nm and 100 nm. LT nFETs show similar R_{TOT}-DIBL trade-off as that of HT nFETs.

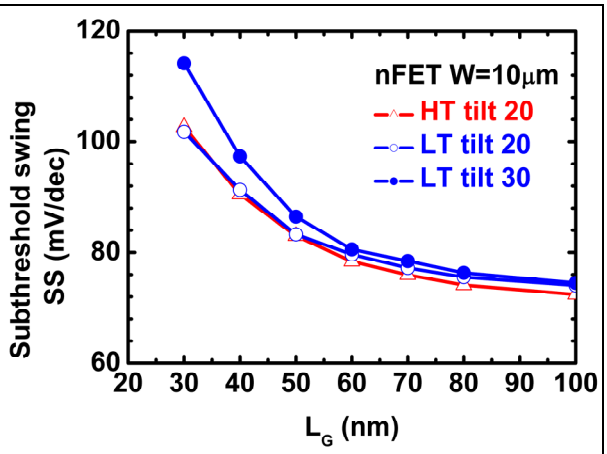


Fig.II.18 Subthreshold swing (SS) versus L_G roll-off for LT/HT nFETs with W=10 µm. Similar SS-L_G are observed for LT/HT nFETs with LDD implant tilt of 20 °. LT with higher tilt of 30 ° induce higher extension to gate overlap and degrade the SS.

However, the two comparisons above are not sufficient to conclude about which implant tilt (20 ° or 30 °) is better optimized for LT nFETs. In order to find the optimized LDD implant tilt, the SCE control of different nFET splits need to be compared and discussed in detail.

From the subthreshold swing (SS) versus L_G plot (Fig.II.18), threshold voltage (V_{TH}) versus L_G plot (Fig.II.19) and DIBL-L_G plot (Fig.II.20), it is observed that similar SCE control is achieved in LT/HT nFETs with the same implant tilt of 20 °. The LT nFETs with higher tilt of 30 ° degrades the SCE seriously, as indicated by the higher SS (Fig.II.18), degraded V_{TH} roll-off (Fig.II.19) and higher DIBL (Fig.II.20). This degradation can be explained by the higher lateral spreading of as-implanted profile, which induces higher LDD

to gate overlap and shorter effective gate length. In addition, as discussed previously, for the two LT splits with tilt 20 ° and 30 °, the increase of tilt does not improve the I_{ON}-I_{OFF} trade-off. So we can conclude that, contrarily to our initial expectation, to achieve the same R_{access} and SCE control trade-off as its HT counterparts, there is no need to increase the LDD implant tilt in LT nFETs.

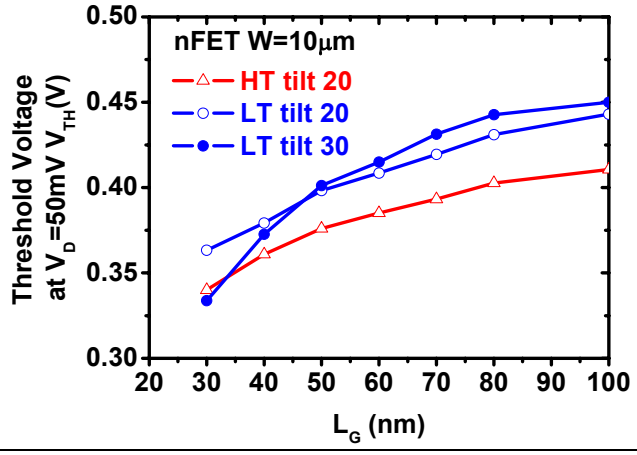


Fig.II.19 V_{TH} versus L_G roll-off for LT/HT nFETs with W=10 µm. Similar V_{TH}-L_G are observed for LT/HT with tilt 20 °. For LT split with higher tilt of 30 °, V_{TH} roll-off is degraded due to the higher LDD to gate overlap.

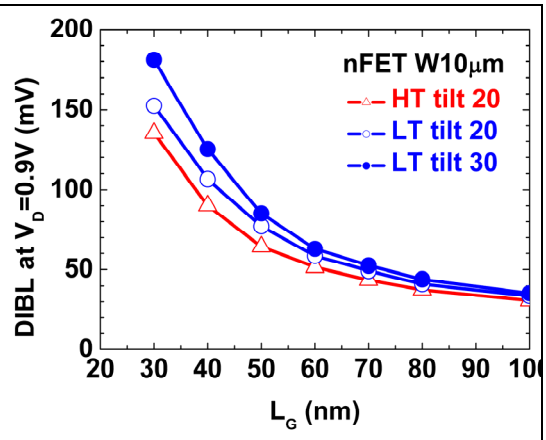


Fig.II.20 DIBL versus L_G roll-off of LT/HT nFETs with W=10 µm. With the same LDD tilt of 20 °, similar DIBL-L_G are observed for LT/HT nFETs. For LT splits, higher LDD implant tilt of 30 ° degrades the DIBL-L_G characteristic, which indicates that higher LDD to gate overlap is obtained.

II.3.1.3 L_G dependence of device performance

Very interesting L_G dependence of device performance has been observed. In Fig.II.21 and Fig.II.22, the maximum conductance (G_{max}) at V_D=50 mV and I_{Dlin} (@ V_D=0.05V, V_G= 0.9 V) are plotted as a function of L_G, respectively. It is observed that for L_G>70 nm, the HT split shows better device performance than the LT split. However, for L_G≤70 nm, G_{max} and I_{Dlin} of LT nFETs overtake that of HT nFETs. As highlighted in Fig.II.21 and Fig.II.22, for L_G=30 nm, 17% and 13% enhancement of G_{max} and I_{Dlin} are obtained on LT splits.

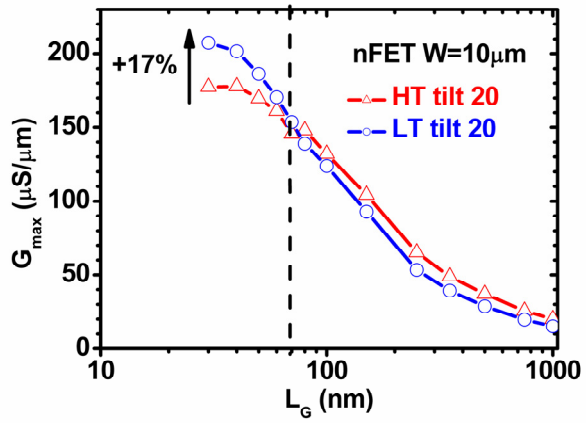


Fig.II.21 G_{max}(@V_D=50 mV)-L_G plot of LT/HT nFET with the same tilt of 20 °. For L_G≤70 nm, G_{max} of LT split outperforms that of HT split.

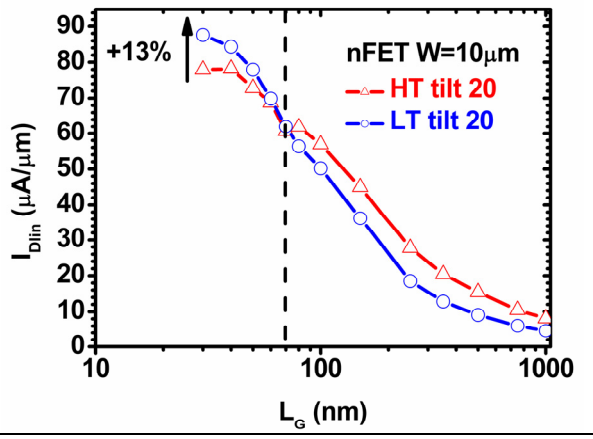


Fig.II.22 I_{Dlin} (I_D at V_G=0.9 V and V_D=50 mV) versus L_G plot of LT/HT nFETs with the same LDD implant tilt of 20 °. For L_G≤70 nm, I_{Dlin} of LT nFETs outperforms that of HT nFETs.

What are the possible causes of this interesting phenomenon? On one hand, considering the different device performance of long transistors in LT split, there might be two reasons:

(I) Due to a difference in the access resistance achieved by LT/HT activation;

(II) Due to a difference in the interface quality and carrier mobility;

On the other hand, considering the performance enhancement of LT short transistors, a third possible cause related to the regrowth of interfacial SiO_2 layer might be responsible for the performance improvement on LT short transistors.

(III) As discussed in section II.2, LT SPER activation is expected to offer better control of the interfacial SiO_2 regrowth, which tends to increase the EOT of short transistors. As a consequence, device performance enhancement is expected on LT short transistors.

In the following sections, the three aspects above will be discussed in detail.

II.3.1.4 Access resistance analysis

To understand why the ON state performance of LT long devices (L_G>80 nm) is not as good as their HT counterparts, the analysis and comparison of access resistance (R_{access}) offer an interesting insight. Using Y function method [Ghibaudo'88], the extraction of R_{access} of LT/HT nFETs is plotted in Fig.II.23. It is observed that the access resistances values are 270Ω.µm and 280Ω.µm for HT and LT process, respectively. The difference of R_{access} between HT and LT splits is not large enough to explain the gate length dependence of device

performance. Also, it is confirmed that, in LT SPER activation, LDD extension is overlapped to gate without increasing the LDD implant tilt.

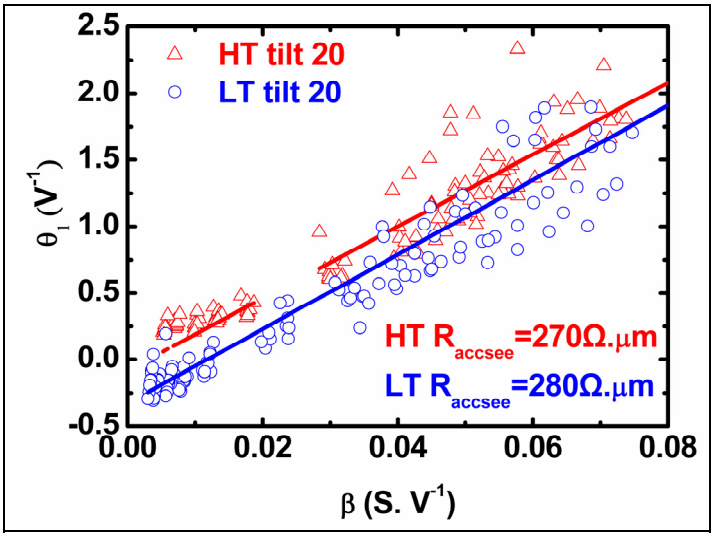


Fig.II.23 Extraction of access resistance of LT/HT nFETs with tilt 20 °. Close access resistance are obtained in LT SPER and conventional HT process. This extraction is based on Y function method [Mourrain'00, Ghibaudo'88], where β is the transconductance gain and θ_1 is the mobility attenuation factor acounting for the mobility decrease with the tranverse electric field.

II.3.1.5 Gate to channel interface quality

The activation anneal can also influence the gate to channel interface quality and carrier mobility in consequence. The effective carrier mobility (μ_{eff}) versus effective field (E_{eff}) plot is very useful to analyze whether the interface quality and the transport of carriers are degraded.

Based on the measurement of C_{gc}-V_G and I_D-V_G curve at low V_D, μ_{eff} can be extracted as a function of E_{eff}, the extracted μ_{eff} of LT/HT nFETs (L_G=W=10 μm) are compared in Fig.II.24. It is found that at an E_{eff} value 0.1 MV/cm, μ_{eff} of LT split is decreased by 30%. This decrease might be induced by higher remote Coulomb scattering, which might indicate higher interface state density (D_{it}) in LT split.

To confirm the hypothesis above, the D_{it} value of LT/HT splits are extracted and compared using the conductance method. D_{it} of LT and HT split is about $9.5x10^{11}$ cm^{-2} and $2x10^{11}$ cm^{-2}, respectively. The higher D_{it} of LT split is in agreement with the conclusions from

μ_{eff} analysis above (Fig.II.24). In addition, the higher D_{it} can explain the higher SS of LT splits. As shown in Fig.II.25, for L_G>100 nm, SS of LT nFETs are about 5 mV/dec higher than that of HT nFETs.

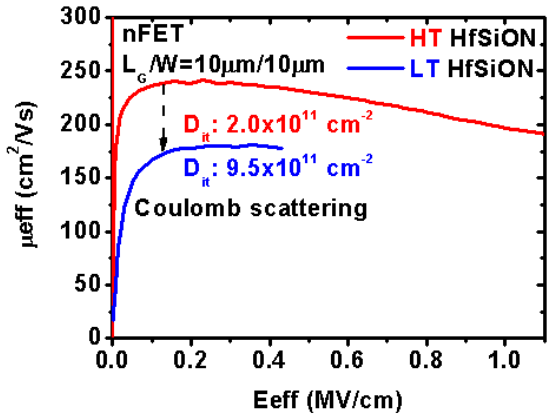


Fig.II.24 Extracted μ_{eff}-E_{eff} plot using the split C-V method. The μ_{eff} of LT nFET is degraded due to higher remote Coulomb scattering, which is consistent with the higher D_{it} of LT split.

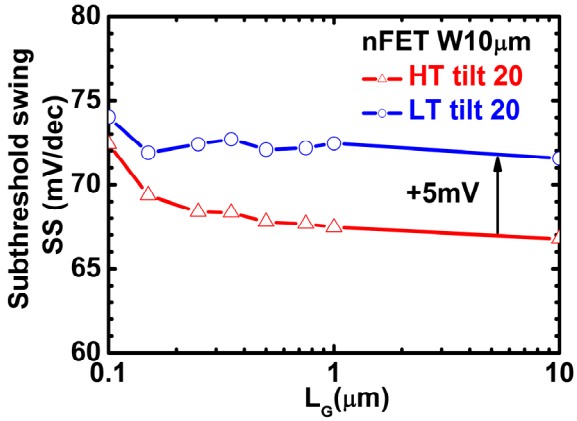


Fig.II.25 SS-L_G plot of LT/HT splits of long transistors with L_G>100 nm. The subthreshold swing of LT devices are about 5 mV/dec higher than that of HT devices.

In LT process, the lack of HT activation anneal degrade the gate to channel interface quality, mobility and SS performances as a consequence. For our future study, to further improve the gate to channel interface quality, forming gas anneal (FGA) should be optimized. Indeed, higher pressure FGA with pure H_2/D_2 anneal has been reported to be effective to reduce D_{it} [Diouf'12, Park'05].

However, for the LT SPER activated splits, the better performance of short transistors can not be explained by its similar access resistance and degraded interface state quality, compared to its HT counterparts. In the following section, EOT of LT and HT activated splits will be compared.

II.3.1.6 EOT-L_G extraction

There is standard capacitance-voltage method for EOT extraction on big transistors. However, for short transistors, accurate EOT extraction is very challenging, due to the lack of exact gate length and the enhanced influence of parasitic capacitance. In this section, an

improved method will firstly be introduced and then applied experimentally for the extraction of EOT on small FDSOI transistors.

II.3.1.6.1 **Theory of EOT extraction on small FDSOI transistors**

Firstly, a brief introduction about different components of gate to channel capacitance (C_{gc}) will be given. As illustrated in Fig.II.26, the main contributions include [Balestra'10, Lacord'12]:

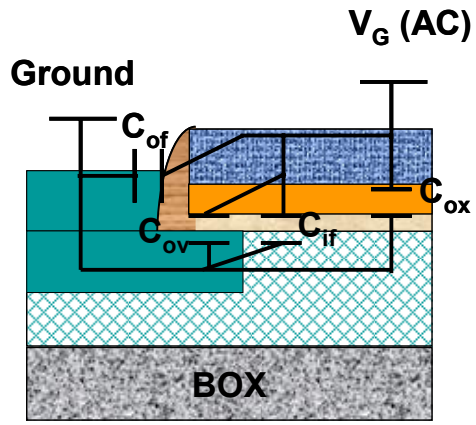


Fig.II.26 Identification of the contributions to gate to channel capacitance (C_{gc}) of a metal gate SOI MOSFET.

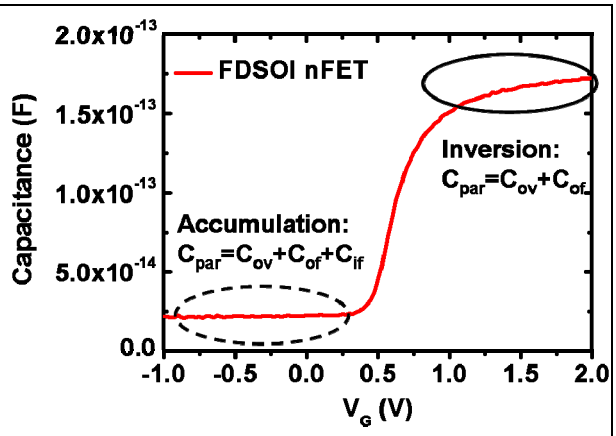


Fig.II.27 Identification of the parasitic capacitance components in the inversion and accumulation region of FDSOI nFET.

C_{ox}: gate capacitance, due to gate dielectric. C_{ox} depends on the thickness of gate dielectric and its dielectric constant. Also, quantum effect can decrease the gate capacitance slightly.

C_{ov}: total contribution of the overlap capacitance, due to the overlap between S/D extension and gate. The overlap is strongly dependent on the integration process (LDD implant tilt/energy, thermal process and so on). C_{ov} is independent on L_G, however it is inversely proportional to EOT. C_{ov} is proportional to W and L_{ov}. Since V_G can change the charge state of the overlap region, C_{ov} also varies with V_G.

C_{of}: total contribution of the outer fringing capacitance, due to fringing fields between gate and RSD/SDE, through the vertical spacers and filling oxide. C_{of} is independent on L_G and EOT. Also, it does not vary with V_G since the RSD region is highly doped and can be taken as a metal layer.

C_{if}: total contribution of the inner fringing capacitance, which is due to the fringing fields between gate and SDE through the semiconductor. For bulk nFET, in the inversion and accumulation region, C_{if} is shielded to zero due to the electron/hole gas. However, as illustrated in Fig.II.27, for FDSOI nFETs under accumulation bias, due to the lack of hole source, there is no hole gas in the channel and the contribution of C_{if} can not be neglected. So, for FDSOI devices in accumulation the total parasitic capacitance (C_{par}) includes C_{ov}, C_{of} and C_{if}. In the inversion region, C_{if} disappears due to the existence of electron gas, C_{par} includes C_{ov} and C_{of} only [Ben Akkez'11, Ben Akkez'12]. C_{if} is also influenced by EOT of gate stack.

The different dependence of C_{ox}, C_{ov}, C_{of}, C_{if} on V_G, L_G, EOT, W and L_{ov} (LDD to gate overlap length) are summarized in Table.II.2. All 4 components are proportional to gate width.

Table.II.2Dependence of C_{ox}, C_{ov}, C_{of}, C_{if} on V_G, L_G, EOT, W and L_{ov} (LDD to gate overlap length).

Dependence on	V_G	L_G	EOT	W	L_{ov}
C_{ox}	Yes	Prop.	Yes	Prop.	No
C_{ov}	Yes	No	Yes	Prop.	Prop.
C_{of}	No	No	No	Prop.	No
C_{if}	Yes	No	Yes	Prop.	No

EOT can be extracted by fitting between measured C_{ox}-V_G curves and simulated C_{ox}-V_G curves with quantum effect taken into consideration. For devices with long L_G (e.g. 10 μm) and wide W (e.g. 10 μm), L_G and W can be taken as equal to the mask defined gate length (L_{Gmask}) and gate width (W_{mask}). Neglecting the contribution of C_{if} in the minimum capacitance of the full C_{gc}-V_G cuve (C_{min}) and the dependence of C_{ov} on V_G, the gate capacitance normalized by the gate area (C_{ox}_A) can be calculated using the following equation:

$$C_{ox}\_A = \frac{C_{gc} - C_{\min}}{L_{Gmask} \times W_{mask}} \qquad \text{(Eq.II.1)}$$

However, for small scale transistors (L_G<100 nm), the lack of knowledge on the exact value of L_G can introduce huge errors on the calculation of C_{ox}_A. Especially for our samples, where gate stack trimming (wet etching) is carried out to get the targeted gate length. The

inaccurate C_{ox}_A calculation will in turn induce errors in EOT extraction. In addition, the contribution of C_{if} in C_{min} and the dependence of C_{ov} on V_G can not be neglected anymore. Therefore, Eq.II.1 is not applicable to calculate C_{ox}_A of small scale transistors.

For two short devices with close gate length (L1, L2, ΔL~10 nm) and same gate width, EOT of the two devices are close to each other and the influence of threshold mismatch can be neglected [Romanjek'04]. As a result, the parasitic capacitances and their dependence on V_G can be taken as the same, and the gate capacitance can be calculated using the following equation:

$$C_{ox}\_A = \frac{C_{gc}^{L2} - C_{gc}^{L1}}{(L2_{Gmask} - L1_{Gmask}) \times W_{mask}} \qquad \text{(Eq.II.2)}$$

In this method, due to the limitation of C-V test equipment, W_{mask} should be as high as possible.

II.3.1.6.2 **Experimental extraction of EOT**

In our experiment, C_{gc}-V_G of devices with different L_G (30/40/50/60/70/80 nm and 10 µm) and 10 µm gate widths are measured. To improve the measurement accuracy, long integration time is applied for short devices with L_G≤80 nm. The extracted EOT of LT/HT devices with different L_G are plotted in Fig.II.28.

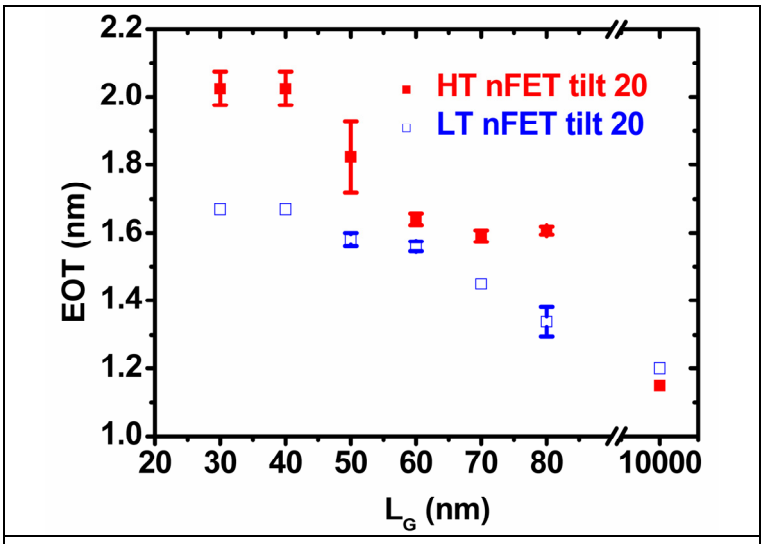


Fig.II.28 Extracted EOT as a function of L_G in LT/HT nFETs. As device scales down, the EOT regrowth is smaller for LT process.

It is obvious that for both LT and HT devices, there is an increase of EOT as devices scale down, which is consistent with the assumption that the SiO_2 regrows mainly in the boundary of the gate to channel interface. However, the EOT increment of LT split is lower than that of HT split. This phenomenon is consistent with the better control of interfacial SiO_2 regrowth in LT process [Batude'09c, Ragnarsson'06].

II.3.1.7 Explanation of performance dependence on L_G

To summarize, the L_G dependent performance can be explained by the joint influence of EOT, mobility and their dependence on gate length. Firstly, for LT long transistors, the slightly higher EOT (Fig.II.28) and much lower carrier mobility result in smaller G_{max} and I_{ON} than that of HT split. Secondly, as L_G decreases to less than 80 nm, EOT of LT transistors are smaller than that of HT nFET (Fig.II.28), which can help to improve the conductance of LT device relatively. However, still the influence of lower mobility of LT device due to higher D_{it} is dominant, so G_{max} and I_{ON} of LT devices are still lower than that of HT devices. Thirdly, for LT nFETs with $L_G \leq 70$ nm, the benefits of lower EOT dominates over the drawback of higher interface state density and the performance of LT devices outperforms that of HT split in consequence.

II.3.2 LT FDSOI optimization: pFETs

II.3.2.1 pFETs fabrication

Fig.II.29 shows the fabrication of LT/HT FDSOI pFETs (T_{Si}~6 nm). For HT split, the gate stack consists of SiO_2(0.8 nm, plasma oxidation)/HfSiON(1.9 nm)/TiN(5 nm, ALD). The HfSiON layer is achieved by plasma nitridization (950 ºC° of HfSiO. However, in LT splits, the plasma nitridization is suppressed and HfSiO layer is used. The first spacer is about 8 nm, followed by the epitaxy of SiGe (30%) raised source and drain. Then, Ge pre-amorphization implant is carried out with optimized energy to avoid full amorphization of active region. After that, B LDD implant is followed. Considering the LDD implant tilt of LT splits, two implant tilts of 30 º and 20 º are used. While only the one split of tilt 20 º is used for standard HT pFET. After second spacer fabrication and HDD implant, activation anneal is made. Spike

anneal (peak T=1050 °C) is applied in standard HT pFET, while LT SPER anneal (600 °C/1 min) is used for LT pFET splits.

Fig.II.30 illustrates the TEM cross section of FDSOI pFET with SiGe RSD. The TEM is made after LDD implant. On this batch, the Si channel is around 6 nm. However, due to the weak selectivity of SiGe epitaxy, SiGe has grown not only above the c-Si in the S/D region, but also above the poly-Si of gate. In consequence, there is a SiGe "mushroom" on top of the gate. The black capping layer on top of the SiGe mushroom and RSD is introduced during TEM sample preparation. As we can see from Fig.II.30, the SiGe mushroom introduces an additional layer above the original gate stack and the fist spacer. As a consequence, more serious shadow effect and much larger shadow area [Kim'00, Jeong'07] are expected in the LDD implant with tilt, than the case without SiGe mushroom.

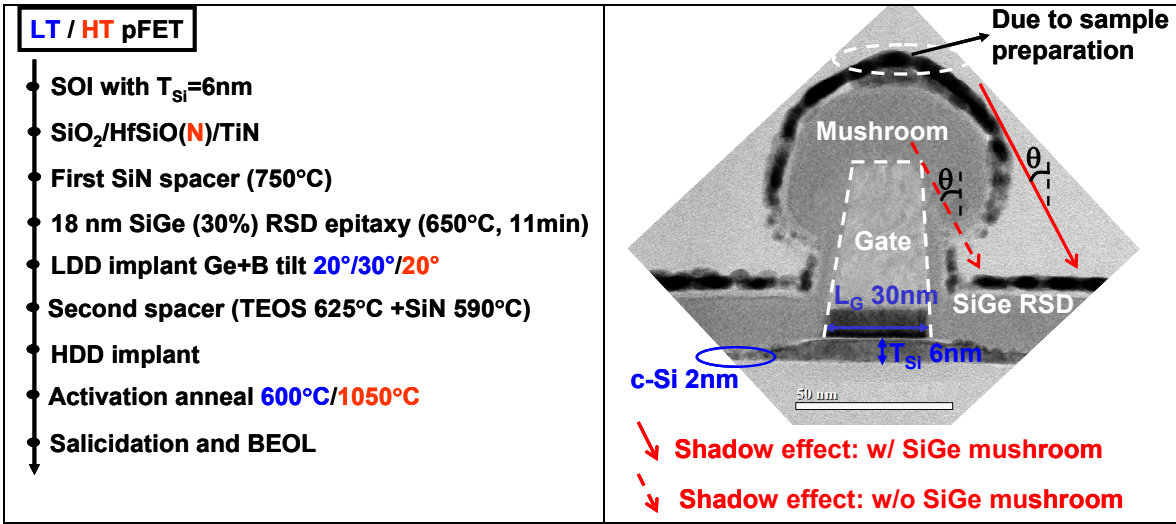


Fig.II.29 Process flow of LT/HT FDSOI pFETs. Ge PAI is carried out before dopant implant. boron atoms in the LT split are activated by LT SPER anneal at 600 ºC.

Fig.II.30 TEM coross section of FDSOI device with SiGe (30%) RSD. The TEM is made after LDD implant.

For pFETs with L_G of 30 nm, I_D-V_G and I_D-V_D curves of LT (tilt 30 º) and HT (tilt 20 º) pFETs are compared in Fig.II.31 and Fig.II.32, respectively. It is observed that the I_D-V_G and I_D-V_D performances of LT pFET are similar to that of HT pFET.

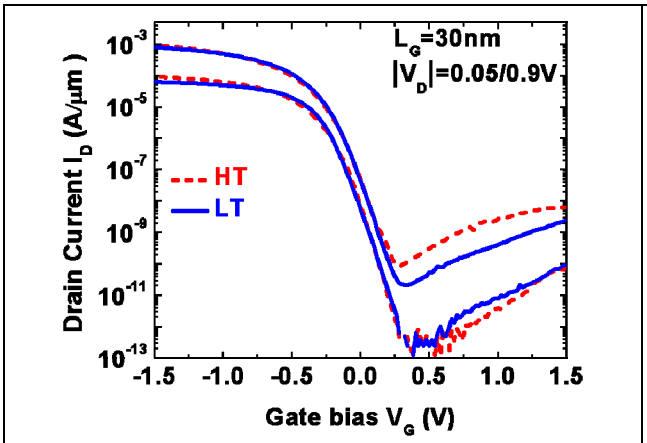


Fig.II.31 I_D-V_G curves of LT (tilt 30 °) and HT (tilt 20 °) pFETs with L_G/W=30 nm/80 nm at $|V_D|$=0.05/0.9 V. Similar I_D-V_G performances are achieved.

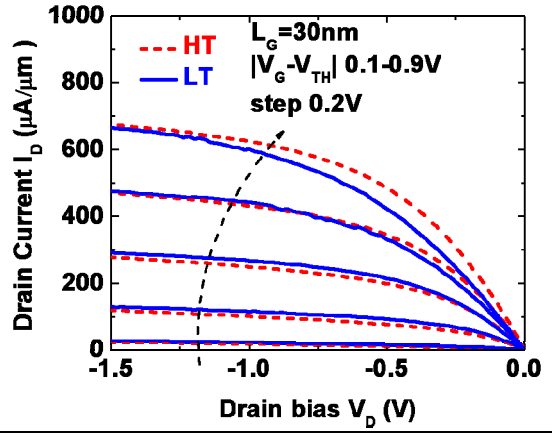


Fig.II.32 I_D-V_D (@different gate overdrive) of LT (tilt 30 °) and HT (tilt 20 °) pFETs (L_G/W=30/80 nm).Similar performances of LT/HT pFETs are demonstrated.

To optimize the LDD implant tilt of LT pFETs, the trade-off between I_{OFF}-I_{ON} and SCE control of different splits have to be statistically analyzed. Firstly, the I_{OFF}-I_{ON} performances of LT/HT pFETs are compared in Fig.II.33. Similar I_{OFF}-I_{ON} trends have been demonstrated for LT (tilt 20 °/30 °) and HT (tilt 20 °) pFETs. However, from the R_{TOT}-DIBL plot (Fig.II.34), it is observed that LT splits degrade the R_{TOT} of devices, especially for the LT split with lower tilt of 20 °. For LT pFETs with higher LDD tilt of 30 °, the R_{TOT}-DIBL performance is closer to that of HT pFETs.

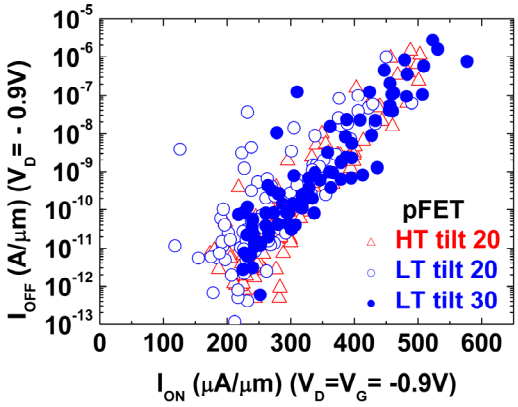


Fig.II.33 I_{OFF}-I_{ON} trade-off of LT/HT pFETs with L_G between 30 nm and 100 nm, W=80 nm. Similar performances are achieved in LT (tilt 30 °) and HT (tilt 20 °) pFETs.

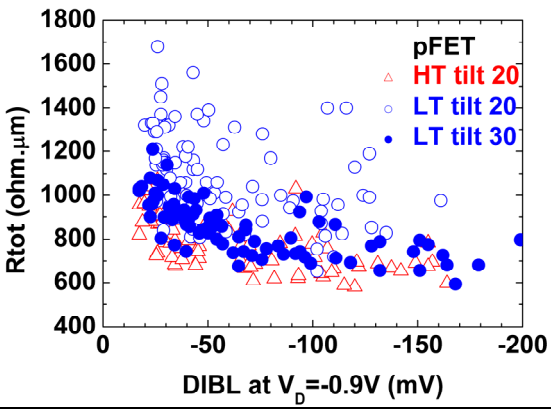


Fig.II.34 R_{TOT}-DIBL of LT/HT pFET with L_G between 30 nm and 100 nm, W=80 nm. LT devices show higher R_{TOT} than conventional HT split.

Secondly, to analyze the dependence of SCE on process parameters, the SS-L_G and DIBL-L_G characteristics of different splits are compared in Fig.II.35 and Fig.II.36,

respectively. It is shown that similar SCE control is achieved in LT pFETs with LDD implant tilt of 30 ºand HT pFETs with LDD tilt of 20 º.

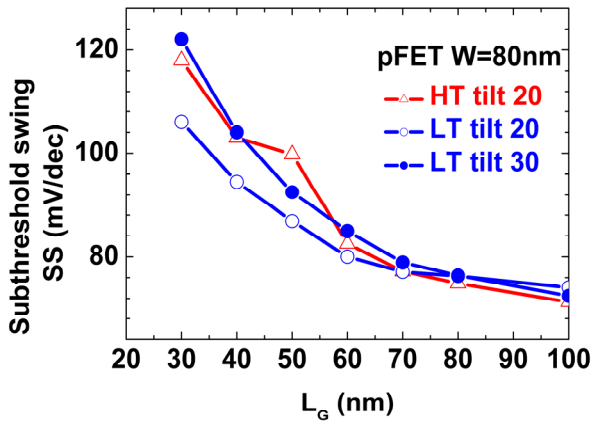


Fig.II.35 Subthreshold swing (SS) versus L_G roll-off for LT/HT pFETs. Similar SS-L_G are observed for LT tilt 30 º and HT tilt 20 º.

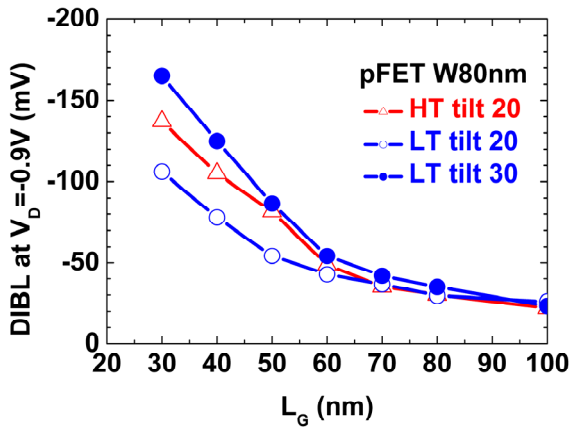


Fig.II.36 DIBL versus L_G roll-off for LT/HT pFETs. Similar DIBL-L_G are observed for LT tilt 30 º and HT tilt 20 º.

Taking both I_{OFF}-I_{ON} and SCE control into consideration, for LT pFETs, higher tilt of 30 º is required to get similar device performance as its HT counterparts. However, in this batch, there is a SiGe "mushroom" on top of the gate, which induces serious shadow effect during LDD implant. In our future work, LT SiGe epitaxy with good selectivity is mandatory. In such a case, getting rid of the strong shadow effect due to the "mushroom", the optimized LDD tilt required for LT SPER activated pFETs should be lower than 30 º.

II.3.2.2 Gate stack quality

The activation anneal might influence the gate to channel interface quality. For LT/HT splits, the distribution of interface states are extracted using the charge pumping method. As shown in Fig.II.37, LT splits show higher D_{it} than HT splits, however, the energy level of the interface states are mainly located close to the conduction band. D_{it} values for interface states close to the valence band are very low and close to each other.

The effective mobility of holes are also extracted and compared in Fig.II.38. It is observed that the μ_{eff} of LT splits is slightly degraded compared to that of HT split. For pFETs under inversion gate bias, only the interface states with energy level close to the valence band can influence the effective mobility of holes. The slight degradation of μ_{eff} in LT process

might be related to the fact that the high-k dielectrics in LT/HT splits are different and the charge state in them might be different.

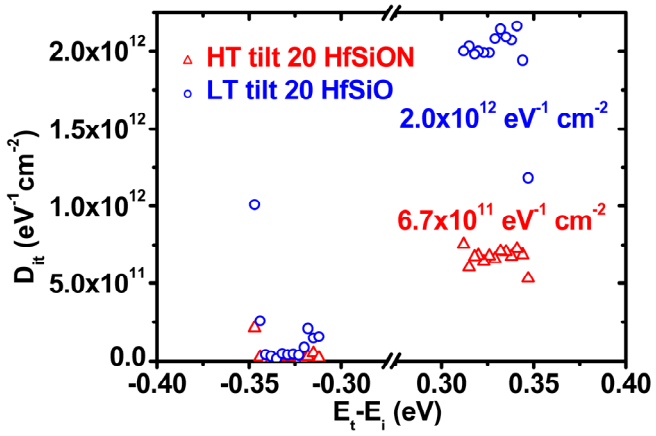


Fig.II.37 D_{it} distribution as a function of trap energy on LT/HT pFETs. The mean D_{it} value of LT/HT process are $2.0x10^{12}$ eV^{-1} cm^{-2} and $6.7x10^{11}$ eV^{-1} cm^{-2}.

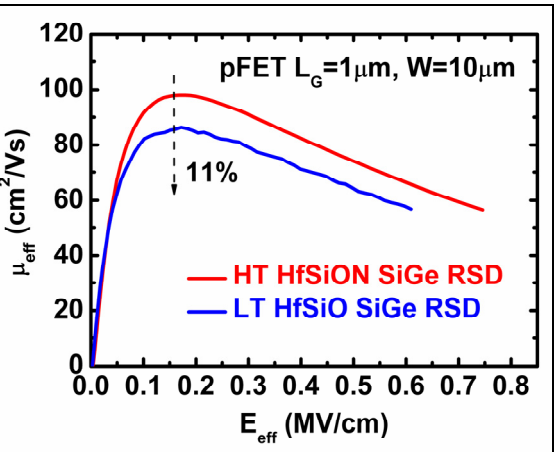


Fig.II.38 Extracted effective mobility (μ_{eff}) of holes as a function of effective electric field of LT/HT pFETs.

II.3.3 Work function engineering for V_{TH} tuning

In the gate first integration scheme, the HT dopants activation anneal tends to move the effective work function of metal gate towards mid-gap. As a result, it is very challenging to modify the threshold voltage for High Performance (HP) application, especially for pFET. Thus, the possibility of tuning V_{TH} with different metal gate materials is limited. To overcome this challenge and broaden the range of material choices for effective work function tuning, gate-last is proposed [Veloso'11]. However, gate-last process is more complex, the removal and replacement of dummy gate stack and the deposition of the metal fill in narrow gate trench opening have presented challenges [Maszara'05, Young'11]. LT activation anneal is attractive for its compatibility with the thermal budget requirement of HK/MG [Girginoudi'08]. It might enable the continuous application of gate first integration scheme for HP FDSOI device for future advanced technology node.

Our experiment is summarized in Fig.II.39. 0.8nm interfacial SiO_2 is achieved by plasma oxidation. In LT/HT processes, HfSiO/HfSiON is used as high-k dielectrics, respectively. 5 nm TiN is realized by atomic layer deposition.

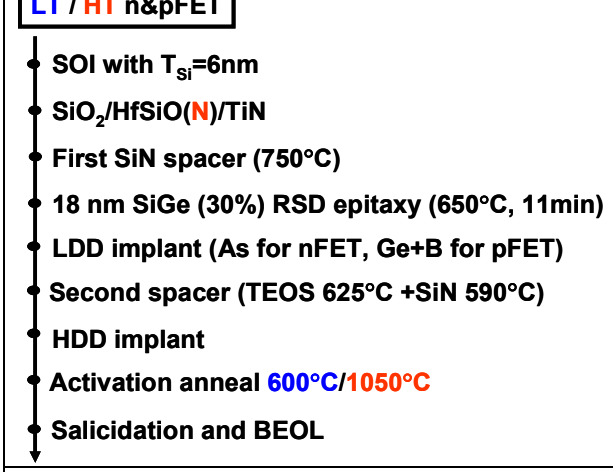


Fig.II.39 The process flow of LT/HT n&pFETs. In HT split, HfSiON is used, while HfSiO is applied for LT split.

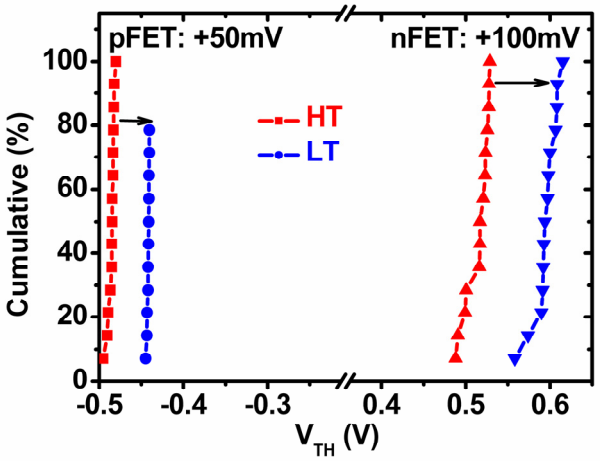


Fig.II.40 Cumulative distribution of V_{TH} of LT/HT n&p FETs (L_G=W=10 µm). Compared to HT devices, V_{TH} of LT devices migrate towards positive direction: +50 mV for pFET, and +100 mV for nFET.

The metal gate consists of 5 nm TiN by ALD. The V_{TH} of LT/HT n&p FETs are compared in Fig.II.40. It is found that, for HT n&p FET, the V_{TH} distribution is symmetric. This indicates that, in HT process, the work function of metal gate is close to mid-gap. However, for LT n&p FET, it is found that V_{TH} moves towards the positive direction: +50 mV for LT pFET and +100 mV for LT nFET. This indicates that the effective work function of TiN metal gate with LT process is higher than that with HT process. For LT nFET, the V_{TH} migration is 50 mV higher than that of LT pFET. This might be explained by the D_{it} distribution (Fig.II.37). We assume that above mid-gap, D_{it} is uniform with a concentration of $2.1\text{x}10^{12}$ eV^{-1} cm^{-2} (D_{it}_LT) and $6.7\text{x}10^{11}$ eV^{-1} cm^{-2} (D_{it}_HT) for LT and HT devices. The influence of different D_{it} distribution on V_{TH} of nFETs can be calculated by:

$$\Delta V_{TH} = \frac{q \times \left(D_{it}\_LT - D_{it}\_HT\right) \times \frac{Eg}{2}}{C_{ox}\_A} \qquad \text{(Eq.II.3) [Cristoloveanu'95]}$$

where q stands for elementary electric charge, Eg the Si band gap. ΔV_{TH} is calculated to be about 52 mV, which corresponds to the amplitude difference in V_{TH} migration. Since the D_{it} close to the valence band is very low, its influence on V_{TH} migration of pFETs can be neglected.

So we can conclude that, the effective work function of LT process is 50 mV higher than that of HT process, which explains the 50 mV higher V_{TH} of LT pFETs. With LT SPER activation, the metal gate work function moves less towards the mid-gap, this increases the

possibility of V_{TH} tuning by allowing more material choices for metal gate. Also LT SPER offers the possibility of maintaining gate first integration scheme, which can help to reduce the integration cost.

II.4 Conclusions

In this chapter, we have reviewed the mechanism and properties of LT (<600 ºC) SPER anneal. For the application of LT SPER in FDSOI fabrication, the challenges are discussed in detail: (1) Full amorphization of active region; (2) LDD to gate underlap due to the weak diffusion of LT SPER; (3) Leakage increase due to EOR defects; (4) Dopant deactivation during post activation anneals . Considering the first two challenges, possible solutions are explored to achieve similar device performance (I_{OFF}-I_{ON} and SCE control) in LT/HT devices: Firstly, to avoid the first challenge, making LDD implant after RSD regrowth together with accurate prediction of implant energy by CTRIM or KMC simulations is efficient. Considering the second challenge, the modification of LDD implant tilt is shown to be an effective way to modify the LDD to gate overlap.

With the two approaches above, we obtain LT n&p FETs (L_G=30 nm) with similar performances as its HT counterparts. Similar I_{OFF}-I_{ON} and SCE control can be achieved by optimizing the LDD implant tilt.

For nFET, there is no need to increase the LDD implant tilt in LT split. For LT/HT nFETs with the same LDD implant of 20 º, similar I_{OFF}-I_{ON} and SCE control are achieved. Also, it is found that LT SPER anneal can help to control the regrowth of interfacial SiO_2 and to improve the device performance of small scale devices. However, for the same gate stack (SiO_2/HfSiON/TiN), LT SPER activation induces higher interface state density. As a result, in LT nFET, the effective mobility of electrons is seriously degraded. However, thanks to the low thermal budget, better EOT control are experimentally observed on LT split with short gate length, which accounts for their better performance than that of its HT counterparts..

For LT pFET with 8 nm first spacer and SiGe “mushroom” on top of gate, a higher LDD implant tilt of 30° is required to get similar performance as for HT pFET. For further optimization, selective SiGe epitaxy at low temperature is required. Then, the shadow effect is expected to be weakened and the optimized LDD tilt required for LT pFET might be lower

than 30 º. In addition, for LT/HT pFETs, LT splits show much higher D_{it}, but the interface states mainly locate close to the conduction band. Similar distributions of interface states close to the valance band are observed.

In LT process, to further improve the quality of gate to channel interface, further improvements of forming gas anneal (e.g. higher pressure forming gas anneal) are interesting.

In addition, it is observed that the LT SPER activation helps to avoid the problem of effective work function modification during HT process, which is one of the main reasons why gate-last technology is raised. This allows us to broaden the metal gate material choice for work function tuning for different applications and increase the possibility of maintaining gate first integration scheme.

Chapter III : **GIDL optimization of LT transistors**

Abstract- As discussed in Chapter II, LT SPER anneal can offer highly doped abrupt junction, but EOR defects are left below the previous a/c interface. These two properties can introduce challenges to maintain the gate induced drain leakage (GIDL) at a low level. On one hand, the abrupt junction can induce high electric field and high band to band tunneling leakage as a consequence. On the other hand, the residual EOR defects can increase trap induced leakage.

In this chapter, we will firstly briefly remind the definition of the GIDL current and the generation mechanisms of GIDL. Then, we will show that, for FDSOI MOS transistors on thick SOI, LT SPER activated devices show much higher GIDL than standard HT activated devices. To improve the leakage performance, it is mandatory to figure out the dominant mechanism responsible for the GIDL increase of LT SPER activated devices. As a consequence in the second section, we will review the traditional method for GIDL mechanism discrimination. However, the traditional method is limited by the lack of accurate tunneling model and knowledge of electric field. In this work, one novel approach will be proposed to distinguish the dominant GIDL mechanism. This method is theoretically verified. However, to apply it on FDSOI, there are additional challenges. So, a detailed methodology for GIDL extraction will be derived specifically for FDSOI MOS transistors.

By using the GIDL analysis method, it is found that, for LT SPER activated FDSOI MOS transistors on 25 nm SOI, the higher GIDL is induced by the residual EOR defects. Defect engineering has to be made to further improve GIDL performance of LT SPER activated devices. In the end, we will show that by thinning the Si thickness in the channel, the EOR defects density and GIDL leakage in consequence can be reduced. This improvement is introduced by the enhanced defect cutting off effect and defect sinking effect of BOX.

III.1 Gate Induced Drain Leakage (GIDL)

In this section, we will firstly recall what GIDL is and how GIDL influences device performance. Then the GIDL generation mechanism will be reviewed in detail.

III.1.1 GIDL and its generation mechanisms

The gate induced drain leakage was firstly studied in MOSFET in the late 80s by the Berkeley group [Chan'87, Chen'87]. For a MOSFET under accumulation bias (Fig.III.1), GIDL arises from the gate to drain overlap region. GIDL mainly impacts the device performance by limiting the minimum drain current achievable (I_{Dmin}), as shown in Fig.III.2 [Xu'10].

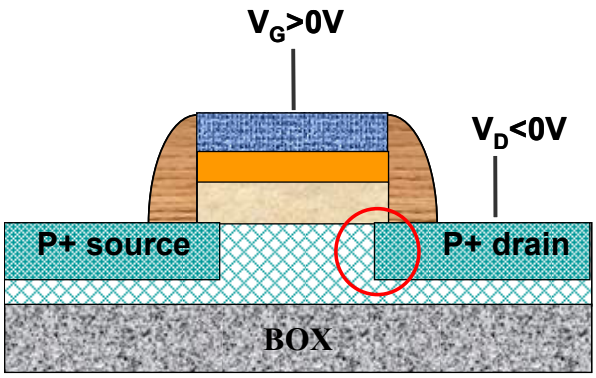


Fig.III.1 Schematic plot of GIDL occurrence in the gate to drain overlap region of a pFET under accumulation bias.

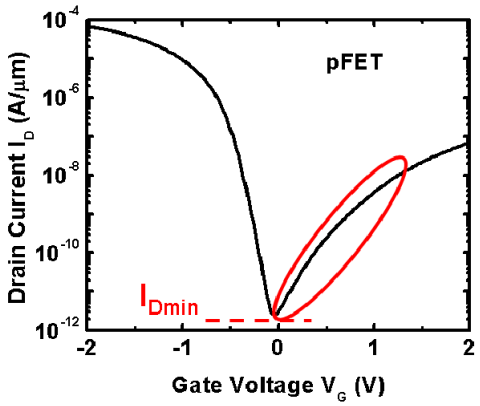


Fig.III.2 Schematic plot of GIDL and its influence on the drain current vs. gate voltage characteristic. The minimum I_D achievable (I_{Dmin}) is limited by GIDL.

Fig.III.3 shows the generation mechanisms of GIDL. With the downscaling of MOSFETs, the gate dielectric thickness is decreased and the drain doping concentration is increased [ITRS'11, Wang'98]. As a consequence, in the gate to drain overlap region, the electric field is enhanced both in the vertical and lateral direction. On one hand, under strong electric field, the surface of the overlap region is deeply depleted. As shown in Fig.III.3-(b), electron-hole pairs can be generated by Band To Band Tunneling (BTBT), Trap Assisted Tunneling (TAT) and Shockley-Read-Hall (SRH) recombination in the vertical direction [Wang'98, Yuan'07, Chen'89]. On the other hand, under large $|V_{DG}|$ bias, the channel and drain forms one reverse biased p-n junction in the lateral direction. BTBT, TAT and SRH

recombination in the space charge region can also contribute to gate induced drain leakage (Fig.III.3-(c)) [Yuan'07, Huang'97, Chang'95].

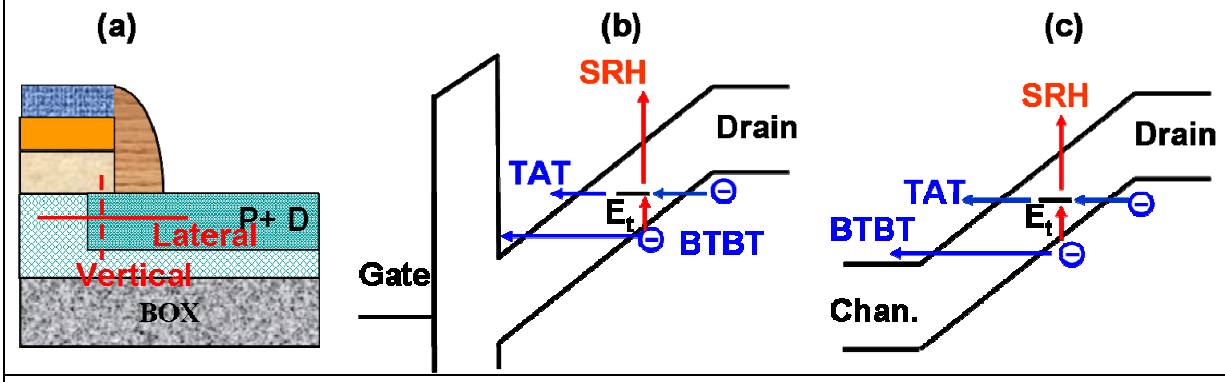


Fig.III.3 Schematic of the location of lateral channel to drain junction and vertical gate to channel junction in the gate to drain overlap region (a). Band diagram of band to band tunneling, trap assisted tunneling and SRH recombination in the vertical gate to drain extension overlap (b) and lateral channel to drain junction (c).

Table.III.1 Dependence of BTBT, TAT and SRH recombination on Temperature (T), electric field and junction quality (abruptness/trap density).

Mechanisms	Temperature (T)	Field (F)	Junction quality
BTBT	insensitive	dependent	Abruptness
TAT	insensitive	dependent	Trap density
SRH Recombination	dependent	insensitive	Trap density

GIDL is influenced by the temperature, electric field and junction quality. As summarized in Table.III.1, BTBT, TAT and SRH recombination have different dependence on temperature (T), electric field (F) and junction quality (abruptness and defect density). BTBT is insensitive to temperature. However, BTBT increases dramatically with electric field [Kane'60], which is larger for more abrupt junction [Czerwinsk'03]. As a consequence, BTBT is stronger for more abrupt junction. Similar as BTBT, TAT is independent on T and dependent on F. However, as the influence of junction quality is concerned, TAT generation is strongly dependent on the trap density [Weber'06]. Unlike BTBT and TAT, SRH recombination is very sensitive to temperature and insensitive to electric field. Also, SRH recombination is more influenced by the trap density [Hurkx'92].

III.1.2 Influence of LT SPER on GIDL

In our experiment, p&n FDSOI MOS transistors were fabricated on thin SOI wafers (T_{Si} around 25 nm) with an HfO_2/TiN metal gate stack. The process flow is shown in Fig.III.4. Process splits are summarized in Fig.III.5-(a). In processes A and B, dopants were activated at 600 ºC through LT SPER. Process A is used for the fabrication of top FET in 3D monolithic integration (Fig.III.5-b), in order to protect bottom transistors (Process C) from any degradation. In process C, dopants were activated by means of a standard HT spike anneal with a peak temperature around 1050 ºC. Processes A/C and B respectively feature a 5 nm and 3 nm dielectric thickness. Also, the HfO_2/TiN/Poly-Si gate stack was processed below 600 ºC in order to ensure that the overall thermal budget of the LT transistors is kept below 600 °C.

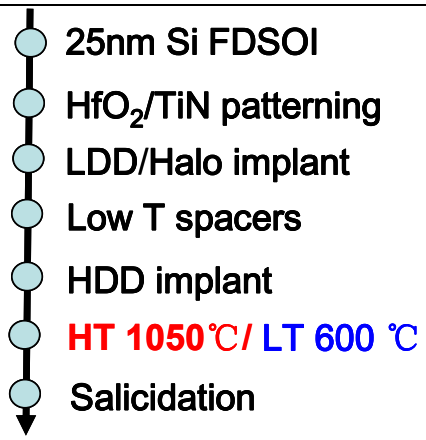


Fig.III.4 Process flow of LT/HT FDSOI devices on 25 nm Si.

(a)

Samples	A	B	C
T_{HfO2}(nm)	5	3	5
Activation	LT	LT	HT

(b)

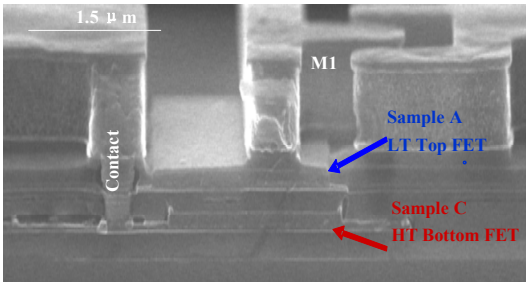


Fig.III.5 (a) Table of samples with process splits (b) MEB cross section of devices with process A (top FET) and C (bottom FET).

As discussed in Chapter II, the drain junction of LT SPER activated device has two properties: (1) highly doped abrupt junction; (2) EOR defects left below the junction. As a result, LT SPER can increase GIDL [Xu'10]. On one hand, the highly doped and abrupt junction results in high electric field and high BTBT leakage consequently. On the other hand, the residual EOR defects can increase the GIDL leakage by enhancing TAT and SRH recombination.

In this experiment on 25nm SOI, LT SPER activated devices show much higher GIDL than standard HT activated devices. Fig.III.6 shows typical I_D-V_G curves of LT/HT activated n&p FETs in the saturation region. It is obvious that LT SPER activated devices show much higher GIDL current. Fig.III.7 shows the statistical plot of I_{Dmin} (at $|V_D|$=1 V). It is found that I_{Dmin} of LT SPER activated devices are about 1.5 decades higher than HT activated devices. To decrease the leakage, it is mandatory to identify the dominant GIDL mechanism (trap induced leakage or tunneling leakage).

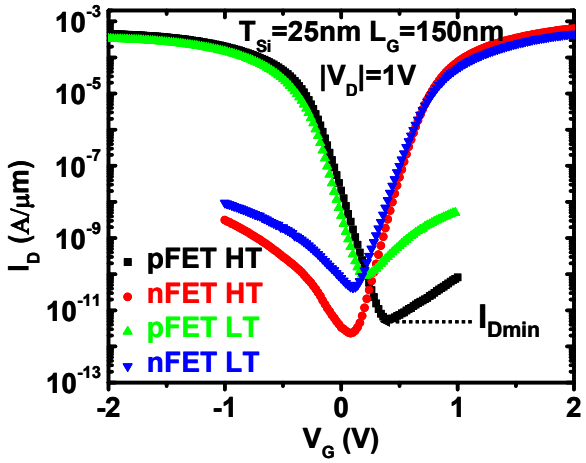


Fig.III.6 I_D-V_G (@$|V_D|$=1V) curves of LT SPER/HT spile activated n&p FETs with L_G=150 nm. The Si thickness in the channel is about 25 nm.

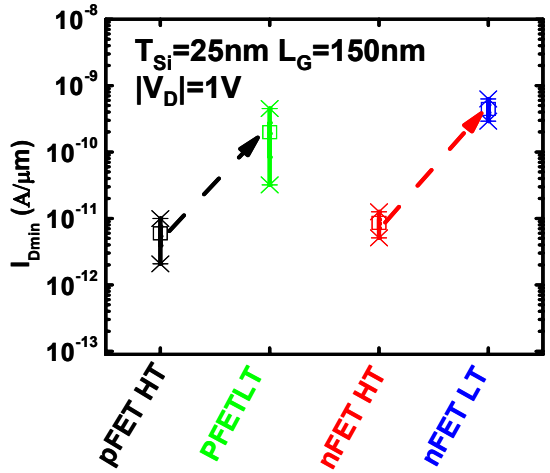


Fig.III.7 Statistical I_{Dmin} at room temperature of n&p FETs activated by RTP and LT SPER. I_{Dmin} is the smallest I_D achieved at $|V_D|$=1V.

III.2 Discrimination of GIDL mechanism

In this section, we will firstly review the traditional method for GIDL generation mechanism analysis and its limitations. Secondly, a new method will be proposed for proper analysis of GIDL generation mechanism.

III.2.1 Traditional method

The analysis of GIDL generation mechanism has two main challenges: (1) BTBT modeling is still under debate, and it is often difficult to link comprehensive but complex numerical simulations with simple current based electrical extraction [Chen'01]; (2) BTBT is

a strong field dependent mechanism [Kane'60, Keldysh'58]. However, little is known about the actual electric field in the device.

To cope with these two difficulties, conventional extraction methods proceed with two main assumptions: (I) analytical model of GIDL current; (II) model of the electric field in the analytical expression of GIDL current. We will firstly review the assumption about GIDL current model. The local generation rate of tunneling component can be expressed by the following equation [Kane'60, Keldysh'58]:

$$R_{Tunnel} = A' E_g(T)^{\sigma} F(x,y)^{\Gamma} \exp\left(-\frac{B}{F(x,y)}\right) \qquad \text{(Eq.III.1)}$$

where A' is the tunneling pre-exponential constant dependent on the effective mass of electron/hole and the energy band gap of Si [Kane'60]. F(x,y) stands for the local electric field. The unknown/unsure constants, σ and Γ, are used to reflect the overall disagreement of the literature on the form of the pre-exponential factor. σ is reported to be -0.5 in [Kane'61] or -1.75 in [Keldysh'58, Tanaka'94]. Considering the value of Γ: for BTBT, 2 and 3 are reported in [Kane'61] and [Schenk'93], respectively; For TAT, 2.5 in [Keldysh'58, Tanaka94] or 3.5 in [Schenk'93] are reported.

A large consensus has been obtained on the exponential term in Eq.III.1. B is a parameter proportional to the effective band gap raised to 1.5 [Keldysh'58, Tanaka'94], Kane'61]. For band to band tunneling, B is proportional to $E_g^{1.5}$, and its theoretical value is about 21 MV/cm for silicon [Chan'87]. However, for trap assisted tunneling, B is a constant proportional to $(E_g-E_t)^{1.5}$, where E_t is the energy level of traps. Compared to band to band tunneling, a smaller B value is expected in trap assisted tunneling [Chang'95]. The extraction of B value is taken as an effective way to gain some insight into the generation mechanism, and especially to discriminate BTBT and TAT.

Despite the discrepancies about the values of σ and Γ, the total GIDL current is obtained from the double integral of Eq.III.1 over space:

$$I_{GIDL} = \int\int R_{Tunnel} dxdy \qquad \text{(Eq.III.2)}$$

However, there is no a priori information on the 2D electric field. The electrical extraction of B must rely on a more simple expression of GIDL current. Normally, F is

assumed to be a constant independent on space and GIDL current is simply expressed as [Chan'87, Chen'87, Endoh'90, Yuan'08]:

$$I_{GIDL} = AE_g(T)^{\sigma} F^{\gamma} \exp\left(-\frac{B' Eg(T)^{\frac{3}{2}}}{F}\right) = AE_g(T)^{\sigma} F^{\gamma} \exp\left(-\frac{B}{F}\right) \qquad \text{(Eq.III.3)}$$

where F is the effective electric field, independent of space. The value of γ differs between literatures. Indeed, γ=1 is used in [Chan'87, Endoh'90, Jomaah'96], while γ=4 was used in [Bouhdada'97]. For the extraction of B, the following equation can be obtained based on Eq.III.3:

$$\ln\left(\frac{I_{GIDL}}{F^{\Gamma}}\right) = \ln\left(AE_g(T)^{\sigma}\right) - \frac{B}{F} \qquad \text{(Eq.III.4)}$$

Assuming a given value of Γ (Eq.III.1), B can be obtained from the derivative of the left hand side of (Eq.III.4) with respect to 1/F.

The second assumption made by these methods is a consequence of (Eq.III.4). To experimentally extract B value, an assumption is required on the modeling of the electric field under different gate and drain bias (V_G, V_D). Also, the extracted B value is strongly dependent on the calculation of the electric field. Since tunneling can happen in both the vertical gate to channel junction and the lateral channel to drain p-n junction, different equations have been used to model F in the vertical and lateral direction. In the literature, F is widely taken as the maximum electric field in the vertical [Chen'87, Chan'87] and lateral direction [Yuan'08]:

$$F_{\max\_vertical} = \frac{V_{DG} - \Delta V}{3EOT} \qquad \text{(Eq.III.5)}$$

$$F_{\max\_lateral} = \sqrt{\frac{qN_0}{\varepsilon_{Si}}(V_{DG} + V_{bi})} \qquad \text{(Eq.III.6)}$$

In equation (Eq.III.5) and (Eq.III.6), EOT is the equivalent oxide thickness, q the electron charge, N_0 the doping concentration in the channel and V_{bi} the built-in potential of the junction, V_{DG} is the drain to gate voltage difference. ΔV correspond to the potential difference required to obtain corresponding states in the valence and conduction band and thus enable BTBT. ΔV is often taken constant and equal to 1.2 V in the early papers [Chen'87, Chan'87]. However, this expression does not take the flat band voltage and doping profile in the overlap

region into consideration. Much work has been done to improve the electric field calculation. Considering the influence of the flat band voltage and assuming that the drain doping profile is uniform [Chen'01], the maximum vertical electric field could be expressed as:

$$F_{\max\_vertical} = \frac{V_{DG} - V_{fb} - \psi_S}{3EOT} \qquad \text{(Eq.III.7)}$$

where V_{fb} is the flat band voltage in the overlap region. ψ_S is the surface potential in the overlap region expressed by:

$$\psi_S = V_{DG} - V_{fb} + \frac{qN_D EOT^2 \varepsilon_{Si}}{\varepsilon_{ox}^2} - \sqrt{\left(V_{DG} - V_{fb} + \frac{qN_D EOT^2 \varepsilon_{Si}}{\varepsilon_{ox}^2}\right)^2 - \left(V_{DG} - V_{fb}\right)^2} \qquad \text{(Eq.III.8)}$$

where N_D is the drain doping concentration in the gate to drain extension overlap region. This method offers more accurate calculation of vertical electric filed [Chen'01]. However, experimentally, it is difficult to get accurate information about the doping profile in the overlap region. The doping profile in the drain to gate overlap region is assumed to be uniform, which can also introduce errors.

To summarize, the traditional method for B extraction is limited by the assumptions on the tunneling model and electric field model. For accurate extraction of B value, the inaccurate assumption about γ should be overcome. Also, it is necessary to improve the extraction of electric field under different gate and drain biases, which is the purpose of next section [Rafhay'11, Rafhay'12].

III.2.2 Improved approach

The aim of the new approach proposed in this work is to minimize the assumptions made on the GIDL current. The basic equivalence of (Eq.III.1) and (Eq.III.2) will be kept. However, the model of $F(V_G,V_D)$ will be experimentally tested instead of being assumed as an a priori and the value of γ will be extracted experimentally.

Prior to the extraction of B, the test of the field model is carried out using the activation energy of the leakage current. In many papers [Tieman'63, Rosar'00, Jang'99, Saino'00, Eneman'09, Weber'06, Czerwinski'03], activation energy (E_a) of GIDL has been used to discriminate or identify the mechanisms involved in junction leakage or tunneling current. The activation energy of GIDL current is defined by:

$$E_a = -\frac{\partial \ln\left[I_{GIDL}(T)\right]}{\partial\left(1/k_b T\right)}\Big|_F \qquad \text{(Eq.III.9)}$$

It is well known that SRH current is characterized by a large activation energy (a few hundreds of meV, i.e. close to Eg/2) [Rideau'10]. On the contrary, the activation energy of BTBT is small (below 0.1eV), like most tunneling mechanisms [Saino'00, Eneman'09]. These phenomena have been well observed [Jang'99] and modeled in MOS tunneling diodes [Lin'01], where both mechanisms have been found to occur at different regime. To further illustrate this discrepancy, the activation energy of field enhanced SRH [Weber'06, Hurkx'92] and BTBT [Kane'61] have been calculated as a function of electric field Fig.III.8-(a). For field enhanced SRH recombination [Weber'06], the activation energy is calculated by:

$$E_a = \frac{Eg}{2} + \left|E_t - E_i\right| - \frac{3}{2}k_b T - 3k_b T\left(\frac{F}{F_\Gamma}\right) \qquad \text{(Eq.III.10)}$$

where $$F_\Gamma = \frac{\sqrt{24 m^* (k_b T)^3}}{q\hbar} \qquad \text{(Eq.III.11)},$$

with k_B being Boltzmann's constant, T the absolute temperature, m* the effective tunneling mass, q the elementary electron charge and ħ the reduced Plank's constant. For BTBT, the activation energy is calculated based on Kane's model, with the dependence of Si energy band gap on temperature taking into account (Eq.III.3).

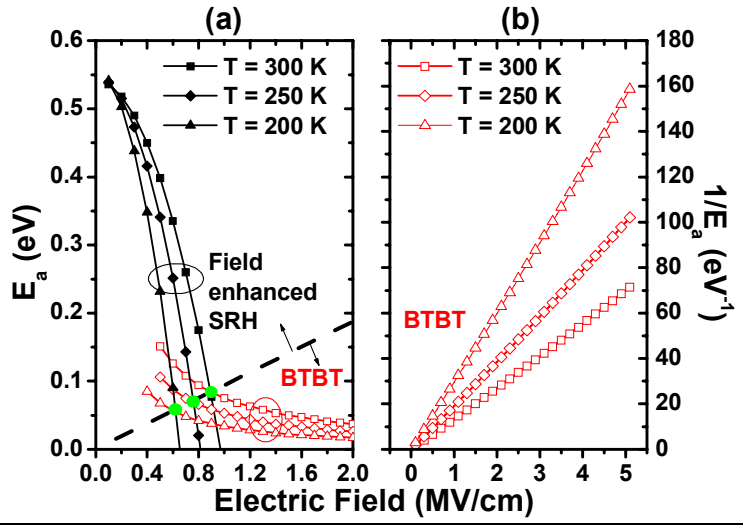


Fig.III.8 (a) Activation energy (E_a) of field enhanced SRH current [Weber'06] and BTBT [Kane'61] as a function of the electric field. (b) Inverse of E_a of BTBT [Kane'61] as function of the electric field.

In the case of tunneling dominated GIDL, the activation energy can be calculated from (Eq.III.3) and (Eq.III.9), as:

$$E_a = -\frac{\partial \ln\left[I_{GIDL}(T)\right]}{\partial\left(1/k_b T\right)}\Big|_{V_G,V_D} = -\frac{\partial \ln\left[AF^{\gamma}\right]}{\partial\left(1/k_b T\right)} - \sigma\frac{\partial \ln\left[Eg(T)\right]}{\partial\left(1/k_b T\right)} + \frac{1}{F}\frac{\partial B}{\partial\left(1/k_b T\right)}\Big|_{V_G,V_D} \qquad \text{(Eq.III.12)}$$

If we assume that the electric field is independent on temperature, then (Eq.III.12) can be simplified as:

$$E_a = -\sigma\frac{\partial \ln\left[Eg(T)\right]}{\partial\left(1/k_b T\right)} + \frac{1}{F}\frac{\partial B}{\partial\left(1/k_b T\right)}\Big|_{V_G,V_D} \qquad \text{(Eq.III.13)}$$

For tunneling dominated GIDL current, the activation energy can be approximated by the following equation:

$$E_a \approx \frac{1}{F}\frac{\partial B}{\partial\left(1/k_b T\right)}\Big|_{V_G,V_D} \qquad \text{(Eq.III.14)}$$

Therefore, for tunneling dominated GIDL, the left hand side term in (Eq.III.14), which can be obtained from I-V-T measurements, is inversely proportional to the field F, as illustrated in Fig.III.8-(b). Hence, the dependency of the electric field with the external bias could be deduced from plot of the inverse of E_a versus F, V_G or V_{DG}. If a linear dependency of $1/E_a$ with V_G or V_{DG} is obtained, this suggests that F follows equation (Eq.III.5). In this case, the ΔV parameter of (Eq.III.5) could be extracted from the measurement, instead of being fixed to an arbitrary value [Chan'87, Chen'87]. This can help to reduce the error made on the field modeling. Other field model could also be adjusted using this approach. However, note that an absolute extraction of F is not possible unless a hypothesis on B is made. Since the aim of the extraction method is to determine B, only relative bias trends could be extracted from the inverse of the active energy.

After the partial validation of the field model presented above, we can write (Eq.III.3) as:

$$\frac{\partial \ln\left[I_{GIDL}(T)\right]}{\partial\left[\dfrac{1}{F\left(V_G, V_D\right)}\right]} = \gamma F\left(V_G, V_D\right) + B \qquad \text{(Eq.III.15)}$$

which can also be written as:

$$\frac{\partial \ln\left[I_{GIDL}(T)\right]}{\partial F\left(V_G, V_D\right)} F\left(V_G, V_D\right)^2 = \gamma F\left(V_G, V_D\right) + B \qquad \text{(Eq.III.16)}$$

γ and B can be extracted respectively from the slope and the intercept of the straight line obtained by plotting the left hand side term in (Eq.III.16) as a function of the field F. Hence, contrary to the previous method, this approach does not make any assumption on γ to extract B. The following section will illustrate the influence on B extraction of an a priori assumption on γ, as done in the conventional method.

III.2.3 Theoretical variation of the new approach

In this section, the robustness of the new approach presented in section III.2.2 will be tested and benchmarked with the extraction methods proposed in the literature [Chan'87, Chen'87, Endoh'90, You'99, Jomaah'96].

To this end, the GIDL current will be calculated using (Eq.III.1) and (Eq.III.2). Two simple field profiles will be considered for the double integral (Eq.III.2) of BTBT generation rate: a constant one and a linearly varying one. The extraction of B will then be carried out on the calculated currents, using either the conventional (Eq.III.4) or the new approach (Eq.III.14) and (Eq.III.16).

Firstly, a constant field is considered. Fig.III.9 shows the relative errors between the set value of B in (Eq.III.1) and the extracted value of B by (Eq.III.4) and (Eq.III.16), as a function of the set values of B. As expected, in the constant field case, the GIDL currents are the same in (Eq.III.2) and (Eq.III.3). As a result, both methods manage to accurately extract B and the relative errors of extracted B equals to zero (Fig.III.9). Using the slope of $(d\ln(I_{GIDL})/dF)\cdot F^2$, the new method also enables to extract the accurate value of γ used for the calculation of BTBT generation rate (Eq.III.1). When Γ in (Eq.III.1) is set to 2, γ of (Eq.III.3) has been extracted to be 2 (other Γ value gave the same agreement between set and estimated values).

Then, a linearly varying field (parabolic potential) is considered for the integral in (Eq.III.2). In this case, (Eq.III.2) is no longer equal to (Eq.III.3). In addition, a particular choice of field value must be performed to use the extraction methods. It appears that using the maximum field of the profile, as done in [Chan'87, Chen'87], ensures the best extraction

of B with the new approach (Eq.III.16). However, an overestimation of B has been obtained when using the conventional methods (Fig.III.9).

In these conditions, the γ value extracted with the slope of $(d\ln(I_{GIDL})/dF)\cdot F^2$ is not strictly equal to Γ of (Eq.III.1), due the double integral over space of (Eq.III.2). For example, if Γ is set 2, the γ extracted is found equal to 2.5. This difference between the Γ field exponent of the BTBT generation rate and the γ one of the GIDL current has already been underlined in [Bouhdada'97]. Therefore, γ depends not only on the physics of the constant field BTBT generation rates, but also on complex 2D field profile in the device. As this field profile is unknown and differs between technologies, the experimental extraction of γ is hence compulsory. In particular, this slight difference between Γ and γ causes a significant overestimation of B by the conventional method, as illustrated in Fig.III.9.

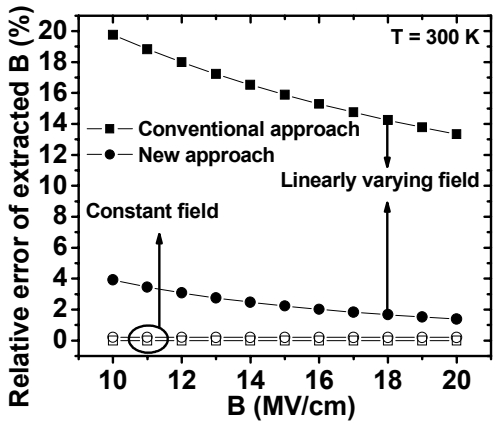


Fig.III.9 Relative error of B extraction as a function of B values set in (Equ.III.1).

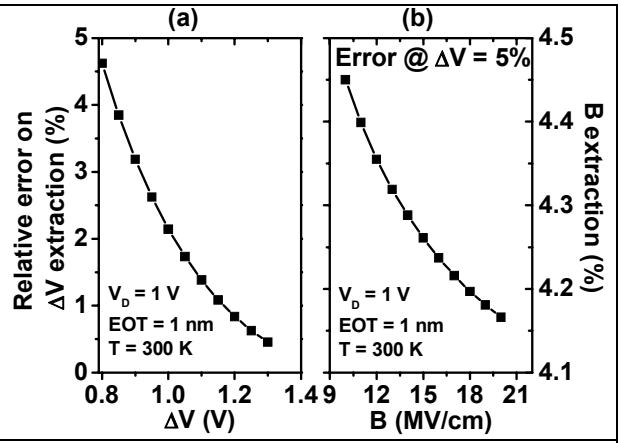


Fig.III.10 (a) Relative errors on the ΔV extraction as a function of the set ΔV. (b) Relative error on the B extraction assuming 5% error on ΔV.

The small extraction error obtained with the new method tends to confirm that (Eq.III.2) can be approximated by (Eq.III.3) provided that the maximum field of the profile is used (e.g. instead of a mean field). In other terms, weak fields do not significantly contribute to the GIDL current compared to the maximum one, because of the steep exponential GIDL dependence with field.

Also, the extraction of ΔV is tested by assuming a constant field, defined as in (Eq.III.5). Fig.III.10-(a) plots the error between the ΔV set in (Eq.III.5) and the one extracted using the

inverse of E_a, as a function of the set ΔV. It shows that, although the field is constant, the extraction of ΔV is not strictly exact. An error of 5 % can be obtained if $\Delta V = 0.8$ V. This is a consequence of the approximation carried out in (Eq.III.4) where $\sigma \cdot d\ln(E_g(T))/d(1/k_bT)$ has been neglected.

Finally, the consequence on the extraction of B with a 5 % error on ΔV, is shown in Fig.III.10-(b). It can be seen that the overestimation of B is kept below 5%, which indicates that the new method does not amplify the error made on the field on the extraction of B.

III.3 Experimental GIDL mechanism discrimination in SOI

The new approach proposed for GIDL analysis is very attractive. However, compared to bulk devices, to make GIDL mechanism analysis on FDSOI MOS transistors, there are additional challenges. In this section, firstly, for FDSOI devices, the flow of GIDL generated carriers will be compared to that of bulk devices. Then, the additional challenges for GIDL analysis on FDSOI will be discussed. A practical methodology will be proposed to overcome the additional challenges enabling the new approach to be properly used for GIDL mechanism analysis on FDSOI MOS transistors.

III.3.1 Specific challenges of SOI

III.3.1.1 Gate current identification

Compared to bulk device, the GIDL current on SOI devices can not be measured directly as there is no contact to the body. For thin gate oxide MOSFETs biased in the accumulation regime, the apparent GIDL may contain a certain amount of tunneling current through the gate. Fig.III.11 compares the different carrier flows on bulk and SOI pFETs under accumulation bias. In bulk devices, the GIDL current can be easily identified by substrate current measurements, since tunneling generated electrons naturally flow through the reverse biased drain-to-substrate junction, toward the substrate. However, in FDSOI MOS transistors, the generated electrons can either recombine with holes injected from the source and gate, or tunnel through the gate.

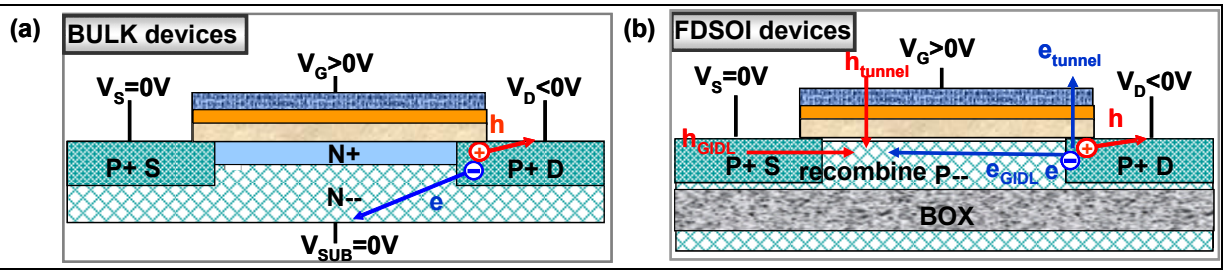


Fig.III.11 Schematic plot of electron and hole flows under accumulation bias, on bulk (a) and FDSOI device (b).

To investigate this effect in FDSOI, full current-voltage (I-V_G) measurements have been performed on pFET samples of A and B. Fig.III.12-(a) shows the I-V characteristics of all three terminals (source, drain and gate) for sample A, which features a 5 nm thick HfO_2 layer. It shows that drain current (I_D) is equal to source current (I_S) in the accumulation regime, while gate current (I_G) is at least two decades smaller. I_G contribution to I_D can therefore be neglected and drain current is hence dominated by carrier generation at the junction. To confirm that I_G contribution to I_D can be neglected, the dependence of gate current with gate voltage overdrive ($V_G - V_{TG}$), is compared at different V_D Fig.III.13-(a). It is found that, at the same gate voltage overdrive ($V_G - V_{TG}$), I_G at different V_D are the same, which indicates that contribution of I_G in GIDL current can be neglected.

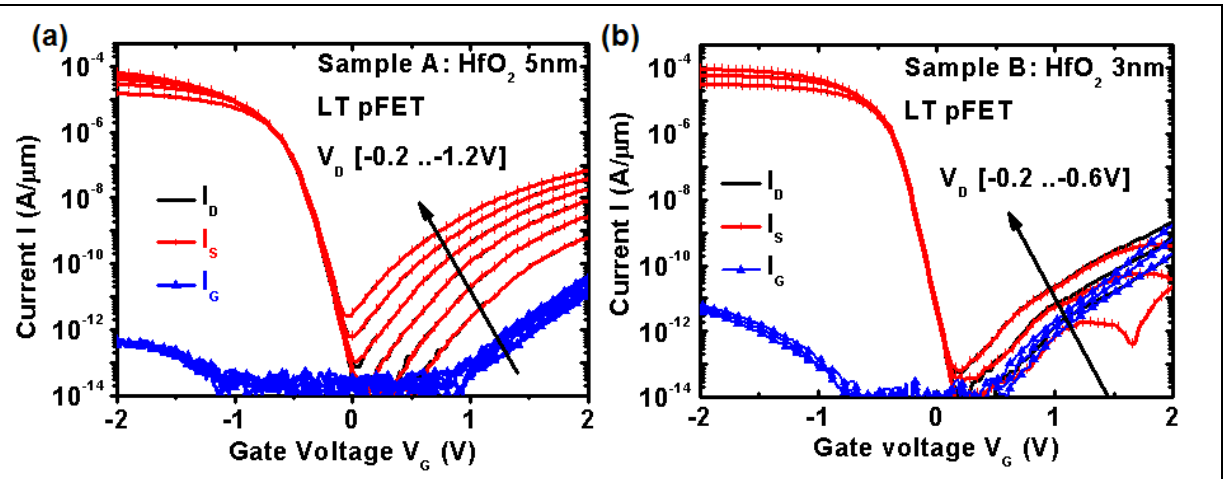


Fig.III.12 Absolute drain (I_D), source (I_S) and gate (I_G) current for pFETs from process A with 5 nm HfO_2 (a) and B with 3 nm HfO_2 (b). The source is grounded and the drain is biased at -0.2 V to -1.2 V, with a step of -0.2 V.

The same analysis was carried out on sample B which features a thinner HfO_2 layer of 3 nm. The I-V characteristics are shown in Fig.III.12-b. For large V_G, I_G gets closer to I_D and I_S begins to depart from I_D. Fig.III.13-b plots I_G against V_G-V_{TG} for sample B. For (V_G – V_{TG}) > 0.5 V, I_G increases if V_D decreases ($|V_D|$ increases). This increase of I_G corresponds to the contribution of electrons that are generated at the junction and flow through the gate.

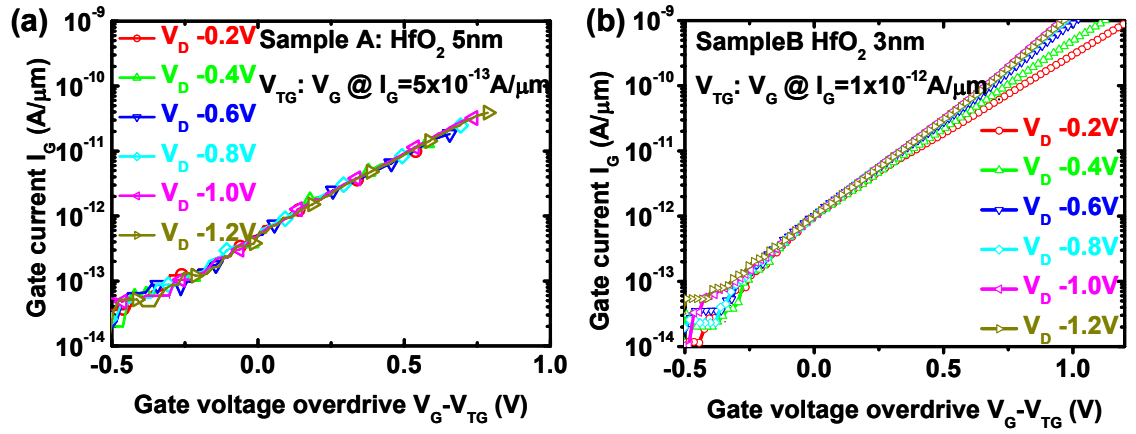


Fig.III.13 Gate current (I_G) versus gate voltage overdrive (V_G-V_{TG}) of samples A and B. V_{TG} is defined as the gate voltage where the gate current equals one critical gate current ($5x10^{-13}$ and $1x10^{-12}$ A/µm for sample A and Sample B, respectively)

To gain more insight into this effect, the source currents were plotted as a function of gate voltage for different values of V_D in Fig.III.14. Source current is the sum of a positive GIDL component with a negative gate tunneling component. Therefore I_S can be negative if dominated by gate tunneling or positive if dominated by GIDL carrier generation at the junction. From Fig.III.14-(a), it is clear that in device A, the source current is always dominated by the positive tunneling GIDL component. However, in device B (Fig.III.14-(b)), for intermediate V_D values (-0.4 or -0.6 V), source current is first dominated by the tunneling GIDL at low V_G values (current takes positive values). At higher V_G, this positive contribution is then decreased by gate tunneling: this confirms that in this thin oxide device, for the bias conditions highlighted in Fig.III.14-(b), part of the GIDL generated electrons can then tunnel through the thin gate oxide or be recombined by holes injected from the gate if the vertical field is large enough.

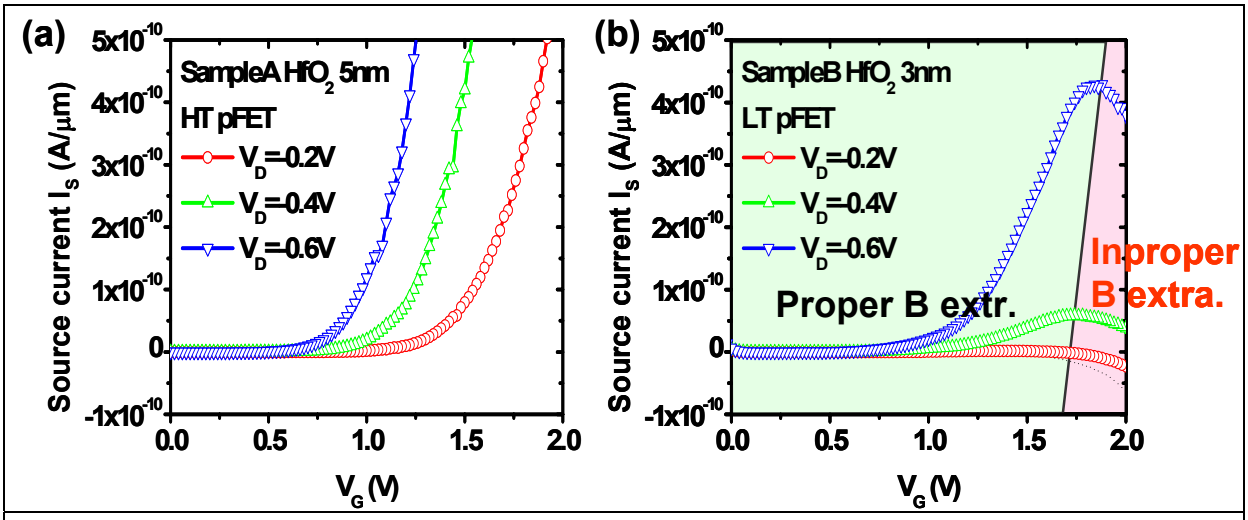


Fig.III.14 I_S-V_G characteristics of (a) sample A (HT pFET, 5 nm HfO_2) and (b) sample B (LT pFET, 3 nm HfO_2).

In conclusion, to ensure correct extraction of the GIDL parameter B, it is first mandatory to determine the bias conditions (V_G, V_D) where I_D is dominated by the GIDL current. Plotting $I_G(V_G-V_{TG},V_D)$ and $I_S(V_G)$ is an effective and simple way to determine these bias ranges. In our experiment, sample B can not be used for GIDL mechanism analysis due to the contribution of gate tunneling leakage.

III.3.1.2 SRH identification

In both the traditional approach and new approaches, it is assumed that GIDL is dominated by tunneling contributions (BTBT and TAT). However, the apparent GIDL current can be dominated by field enhanced SRH current [Weber'06], instead of tunneling current. The presence of field enhanced SRH generation can cause severe errors on the extraction of B. In order to distinguish between SRH and tunneling (BTBT and TAT), it is useful to extract the activation energy of currents. As discussed before, SRH current is strongly dependent on temperature [Czerwinski'03], contrary to BTBT even when trap assisted [Eneman'09]. As shown in Fig.III.8-(a) before, to quantify this discrepancy, the activation energies of BTBT [Kane'60] and field enhanced SRH [Weber'06] have been calculated as a function of the electric field. The universal shape of these curves shows that, at low field (lower than 0.9 MV/cm), activation energy is much larger for the SRH process than for BTBT. In contrast, at higher field (larger than 0.9 MV/cm), the activation energy of BTBT is smaller than the

field enhanced SRH one. Therefore, if the value of activation energy is larger than around 0.1 eV, it can be conclude that GIDL current is dominated by field enhanced SRH. While for E_a values smaller than 0.1 eV, GIDL current is dominated by BTBT [Weber'06, Czerwinskia'03, Eneman'09].

In conclusion, B extraction should be extracted in the regimes where the activation energy is smaller than 0.1 eV, in order to ensure that field enhanced SRH is negligible compared to tunneling.

III.3.2 Experimental results on FDSOI

In our experiment, we have focused on the GIDL mechanism discrimination of sample A and C with 5 nm HfO_2, where the gate tunneling components can be neglected. $I_D(V_G)$ measurements at different V_D and different temperatures were carried out (Fig.III.15).

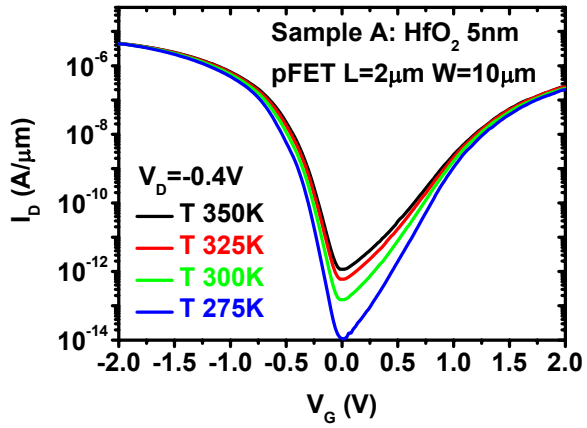


Fig.III.15 Drain current versus gate voltage (I_D-V_G) characteristics of a pMOSFET from process A at different temperature (T).

On this device, I_G has been confirmed to be much lower than I_D and independent on V_D, as in Fig.III.12. After a required threshold voltage shift, which eliminates the field dependence with temperature, activation energies have been calculated and plotted in Fig.III.16, as a function of V_{GS} (a) or V_{DG} (b) for different V_D. At low V_{GS} or V_{DG}, i.e. in low field conditions, the activation energy is found to be larger than 0.1 eV and to strongly decrease with increasing V_G and $|V_D|$. At higher bias (i.e. higher field), E_a was smaller than 0.1 eV. According to the models used in Fig.III.8-a, it is thus concluded that the current is

governed by field enhanced SRH for V_{DG} values below 1.2 V and by tunneling for larger values. Extraction of B has therefore been carried out above 1.2 V.

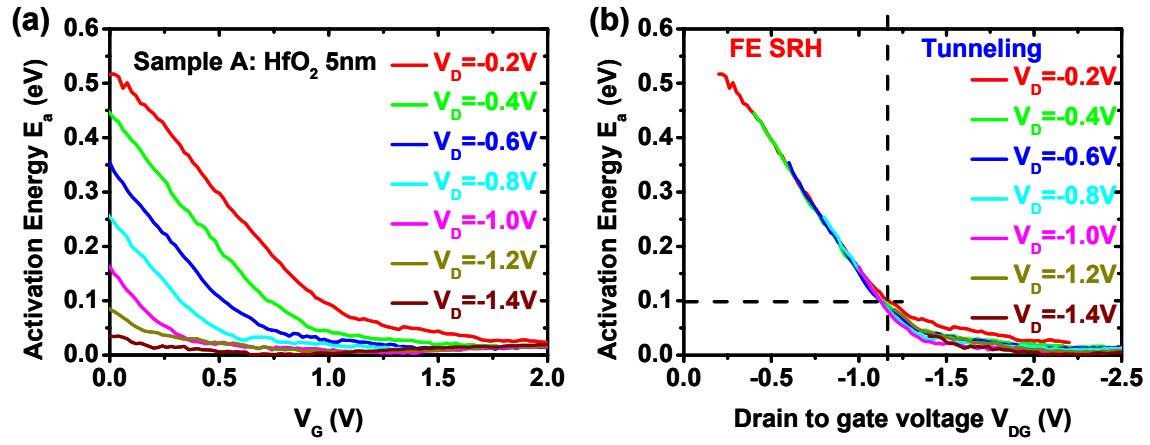


Fig.III.16 Activation energy (E_a) versus (a) gate voltage (V_G) (b) drain to gate voltage (V_{DG}) plotted for different V_D biases (pFET).

Following the identification of the suitable range of bias voltages for B extraction, the inverse of the activation energy has been used to study the dependence of the field with V_{DG}. In most cases, E_a^{-1} has been found to be a linear function of V_{DG}, as shown in Fig.III.17. These results suggest that the field model $F= (V_{DG}–\Delta V)/3EOT$ used by conventional methods [Chan'87, Endoh'90] is correct, provided that ΔV is extracted from the intercept of E_a^{-1} with the V_{DG} axis for each V_D and each temperature. This procedure is illustrated in Fig.III.17.

The $(d\ln(I_D)/dF)\cdot F^2$ function has been calculated using the field obtained with the extracted ΔV. The results are shown in Fig.III.18 for pFETs of sample A and C. The parameter B has been found equal to 11 MV/cm for LT pFET and 20 MV/cm for HT pFET. Also, for nFETs the same analysis is carried out on LT/HT nFET with 25 nm Si channel (Fig.III.19 and Fig.III.20). Also, B value (12 MV/cm) of LT nFET is found to be lower than that of HT nFET (25 MV/cm).

As discussed before, the value of B is proportional to the effective band gap raised to 1.5, thus the lower B value of LT process indicates that the effective band gap has been lowered by the traps. This is in accordance with our expectation: in LT SPER activation, EOR defects are not fully healed out due to the low thermal budget, leaving a higher density of residual EOR defects below the LT SPER junction. This suggests the presence of a larger defect

density in LT SPER junctions. In contrast, B takes an almost ideal value in HT activated devices, confirming the absence of defects for the standard high temperature spike anneal.

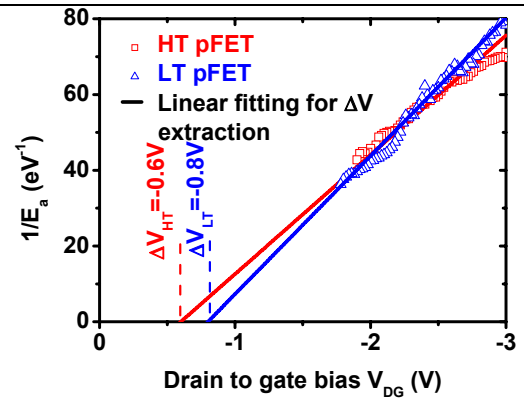


Fig.III.17. Extraction of ΔV using the inverse of E_A versus drain-to-gate voltage (V_{DG}) plot (pFETs with 25 nm Si channel).

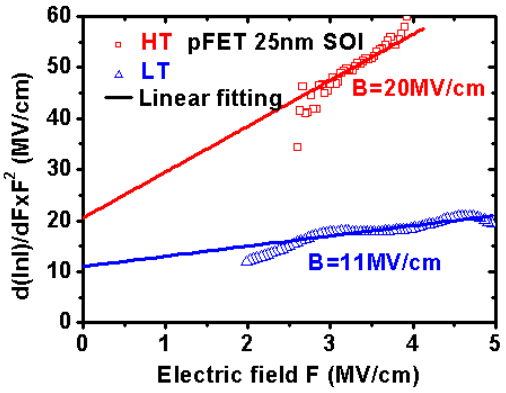


Fig.III.18. Extraction of B from the $d(\ln(I_D))/dF \cdot F^2$ versus F characteristic (pFETs with 25 nm Si channel).

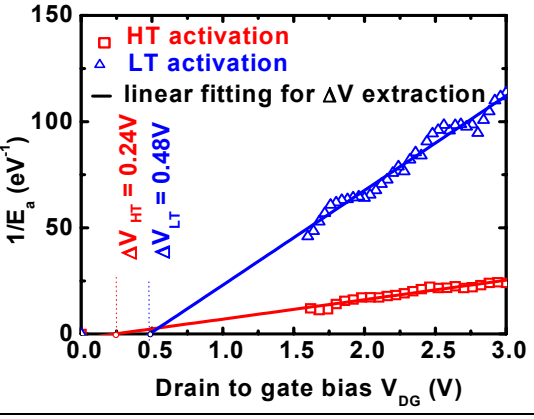


Fig.III.19. Extraction of ΔV using the inverse of E_A versus drain-to-gate voltage (V_{DG}) plot (nFETs with 25 nm Si channel).

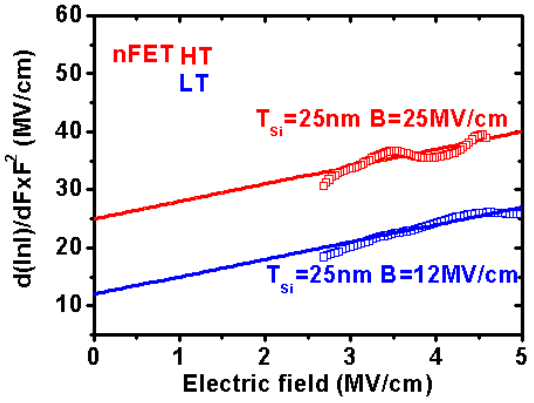


Fig.III.20. Extraction of σ and B from the $d(\ln(I_D))/dF \cdot F^2$ versus electric field characteristic (nFETs with 25 nm Si channel).

III.4 GIDL improvement by defect engineering

As shown in the section above, for LT SPER activated device, higher GIDL leakage is induced by the EOR defects. To control the GIDL current in LT SPER activated devices, defect engineering has to be carried out to reduce the residual EOR defects density. The use of extremely thin SOI (ETSOI), i.e. with a thickness around 10 nm and below, is an effective way to reduce the EOR defects density.

It has been reported that SOI can help to reduce the EOR defect density by two effects. (I) Defect profile is cut off effect thanks to the BOX [Hamilton'07, Fazzini'08a, Saavedra'02]:

compared to bulk sample, on SOI samples, after implantation, part of Si interstitials (Si_i) go into the BOX and get blocked there. Thus, the initial Si interstitials available for the formation of EOR defects is lower, and less EOR defects are formed after EOR activation anneal. (II) Defect sinking effect of BOX during the post activation anneals [Fazzini'08b, Aboy'07, Bazizi'10, Hamilton'06a]: During the post activation anneals, the EOR defects will evolve as a source of Si_i. On bulk sample, the Si_i tend to move toward the top surface of active Si layer, which acts as a defect sink. However, for SOI samples, the BOX can act as an additional defect sink, competing with the top surface of active Si layer. As a result, the EOR defect density is expected to be lower in LT SPER SOI process. Moreover, for the same implant, the defect cut off effect and defect sinking effect can be enhanced by thinning the thickness of SOI. This offers us one interesting way to reduce defect density in LT SPER process.

In our experiment, GIDL performance of LT SPER is greatly improved on ETSOI of 6 nm. As shown in Fig.III.21, similar cumulative distribution of I_{Dmin} is obtained on LT/HT nFETs. The GIDL improvement on ETSOI might indicate lower EOR defects density than that on 25 nm SOI. To confirm this hypothesis, the B value has been extracted to figure out the dominant GIDL generation mechanism. As shown in Fig.III.22, B is extracted to be 18 $MV.cm^{-1}$ and 12 $MV.cm^{-1}$ for 6 nm and 25 nm SOI, respectively. Compared to the nFET on 25 nm SOI, the higher B value of ETSOI (6 nm) indicates that the effective band gap is higher, which in turn indicates that the EOR defects density has been greatly reduced.

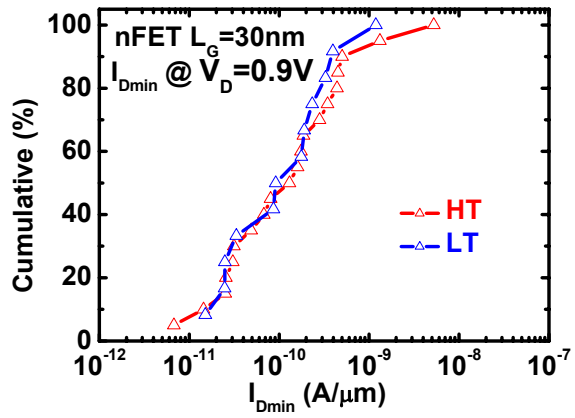


Fig.III.21. Cumulative distribution of the I_{Dmin} value for LT and HT devices with 6 nm Si channel.

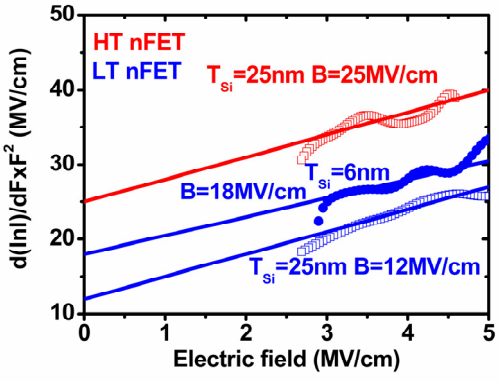


Fig.III.22. GIDL current parameter B extraction of different HT/LT nFETs with different Si channel thickness.

This phenomenon is in accordance with the KMC process simulations [Sklénard'12]. With 2D KMC simulations, it is observed that, after LT SPER activation, the EOR defects density on 6 nm ETSOI is much lower than that on 25 nm SOI. The reduction is explained by the enhanced defect cutting off effect of BOX on ETSOI [Sklénard'12].

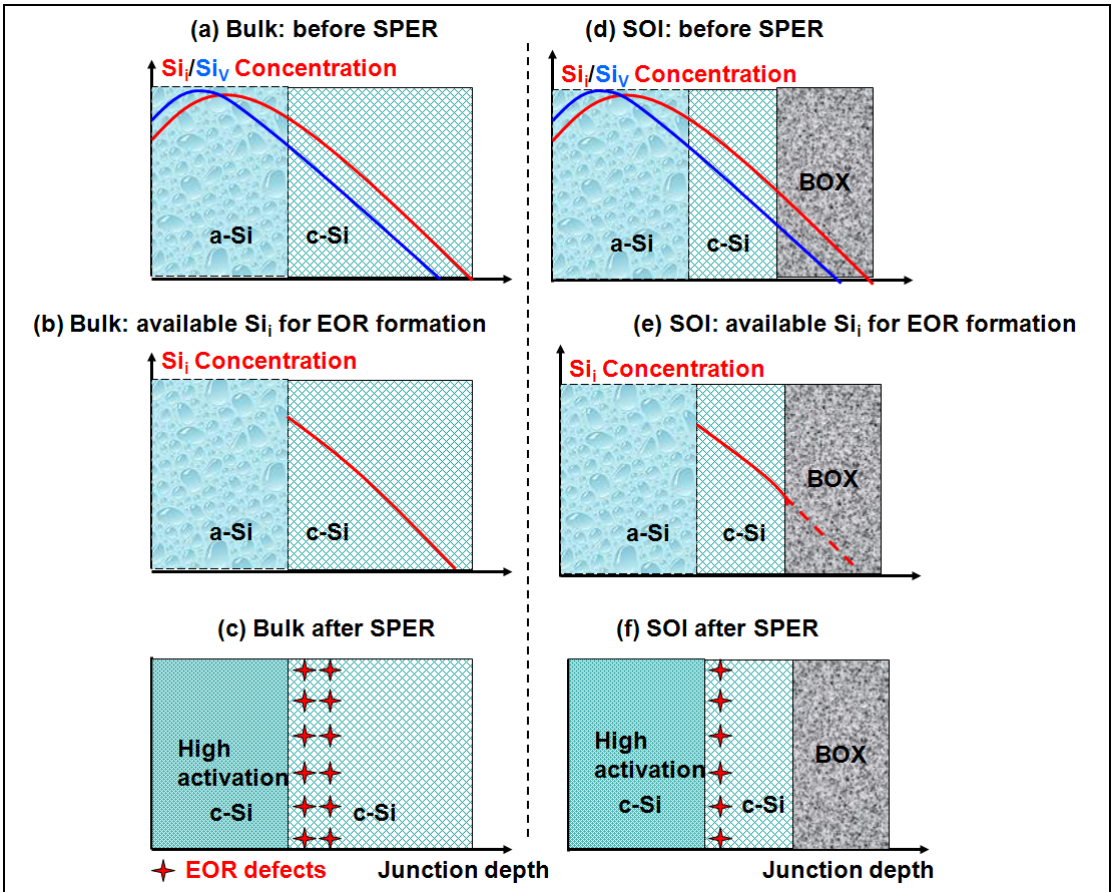


Fig.III.23 Schematic plot showing (a, d) implantation induced surface amorphization (a-Si layer) and Si_i distribution before LT SPER, (b, e) available Si_i for EOR formation and (c, f) recrystallized surface and residual EOR defects after LT SPER anneal, for bulk and SOI samples, respectively. In SOI, part of Si_i are blocked by BOX (as shown by the dashed line in (e)), the initial number of Si_i available for EOR formation is lower, and less EOR defects are formed (f) than that on bulk samples (c).

Compared to bulk sample, the BOX on SOI sample can cut off the as implanted profile of Si interstitials. As shown in Fig.III.23-(e), part of Si interstitials go into the BOX and are blocked within the BOX. As a result, the Si_i available for the formation of EOR defects are less than that of bulk, and lower EOR defect density can be achieved after LT SPER activation anneals. Compared to bulk, LT SPER on SOI samples offers the benefits of lower EOR defects for the same pre-amorphization implant [Fazzini'08a, Fazzini'08b, Saavedra'02].

For the same amorphization implant, the defect cutting off effect is enhanced with the decrease of Si thickness.

III.5 Conclusions

In this chapter, the definition of gate induced drain leakage is firstly recalled. Then , the three possible mechanisms of GIDL current are reviewed: band to band tunneling, trap assisted tunneling and SRH recombination. Experimentally, LT SPER devices on 25 nm SOI show higher GIDL than HT activated devices. Theoretically, this increase can be induced by either the higher EOR defects density or the abrupt junction from LT SPER. For the optimization of GIDL leakage on LT SPER devices, it is very important to analyze the dominant leakage mechanism on LT SPER devices.

Considering the method for GIDL mechanism analysis, firstly the limits of traditional characterization of GIDL were reviewed, namely the lack of accurate model of GIDL current and the inaccurate calculation of electric field. An improved approach has been proposed for GIDL mechanism analysis that overcomes these limitations by proposing an experimental determination of the electrical field. Relying on the determination of γ and ΔV, which are significant modeling parameters of the GIDL current, the new approach proposed in this work has been found to lead to weaker error than the previously proposed methods. To properly apply the new approach for GIDL analysis to FDSOI MOS transistors, a detailed methodology of the correct extraction conditions has been proposed: simple and efficient $I_D(V_G)$, $I_S(V_G)$ and $I_G(V_G)$ curves are used to identify the devices, bias ranges and temperatures for which the GIDL current is dominated by tunneling. The application of this methodology has shown that GIDL characterization can provide a relevant and effective feedback about junction quality. With the extraction of the parameter B, we can distinguish whether GIDL is dominated by TAT or BTBT.

Using the new approach with the methodology proposed, we were able to demonstrate that the B value of LT SPER devices is lower than that of HT devices. It indicates that the effective band gap is reduced by the defects and LT SPER activation results in a larger defect density which is responsible for the higher GIDL.

To reduce the EOR defects density and device leakage of LT SPER activated device, ETSOI is demonstrated to be an effective way. This improvement is due to the enhanced defect cutting off effect and defect sinking effect of BOX by locating the EOR defect band as close to the BOX as possible. Same I_{Dmin} performance has been achieved on LT/HT nFETs with 6 nm SOI. Extraction of B is consistent with I_{Dmin} improvement in LT SPER devices on ETSOI. Indeed, B of LT SPER activated devices on ETSOI (6 nm) devices is much higher than that on 25 nm SOI. The higher B value of LT ETSOI devices is consistent with the higher effective band gap and lower defect density expected.

Chapter IV : **Deactivation of LT SPER activated dopants**

Abstract- In 3D sequential integration, LT dopant activation of top FET is mandatory to protect bottom FET. LT SPER is a suitable technique for the activation of top FET. As shown in Chapter II, similar device performance has been achieved by optimizing the LDD implantation conditions: implant tilt and implant energy. As detailed in Chapter III, by using the defect cutting off effect and defect sinking effect of BOX, similar leakage performance can be achieved with LT activated device as with HT devices. In addition, thanks to its low thermal budget, LT process also shows better EOT regrowth control [Batude'09c, Ragnarsson'06, Sklénard'12] and allows more material choices for threshold voltage tuning [MacKenzie'07]. So, it is very interesting to use LT activation for dopant activation not only of top FETs, but also of bottom FET.

However, one challenging issue for LT SPER is that the activated dopants are metastable and tend to deactivate during the post anneal: the activated dopants tend to form clusters with defects and become deactivated [Pawlak'04b]. In 3D sequential integration, for top FET, the activated dopants will endure the thermal budget of salicidation (450 ºC) and Back End Of Line (BEOL) process (400 ºC). For bottom FETs, the activated dopants will endure the following thermal budget: (1) BEOL of bottom FETs (400 ºC); (2) Wafer bonding (200 ºC); (3) Top FET fabrication (600 ºC); (4) BEOL of top FETs (400 ºC). One of the main challenges of LT SPER is the dopant deactivation during post activation anneal, which will in turn degrade the access resistance and I_{ON} in consequence. So, to apply LT SPER for dopant activation, it is necessary to study the deactivation of dopants in the temperature range of 400 ºC to 600 ºC.

In this chapter, we will firstly review the defect evolution and dopant (boron and arsenic) deactivation mechanisms. Then, compared to bulk devices, the possible advantage of BOX in FDSOI will be discussed. In the third section, the design of experiments for deactivation analysis will be shown. In the forth section, we will compare the activation of dopants in LT/HT activation. In the end, the deactivation of boron and arsenic on SOI and its dependence on the distance between EOR defects and BOX will be analyzed.

IV.1 Defect evolution and dopant deactivation

The thermal stability of LT SPER activated dopants is strongly related to the existence of EOR defects after LT SPER anneal [Solmi'02, Colombeau'04]. In this section, we will firstly review how the defects evolve during the post activation anneal. Then, the deactivation mechanisms of boron and arsenic will be reviewed, respectively.

IV.1.1 Defect evolution during post activation anneal

As discussed in the former chapters, due to the low thermal budget of LT SPER, EOR defects are left below the previous a-c interface after the LT SPER activation anneal. During the post activation anneals, the EOR defects tend to evolve with the emission of Si interstitials (Si_i) [Hamilton'06a].

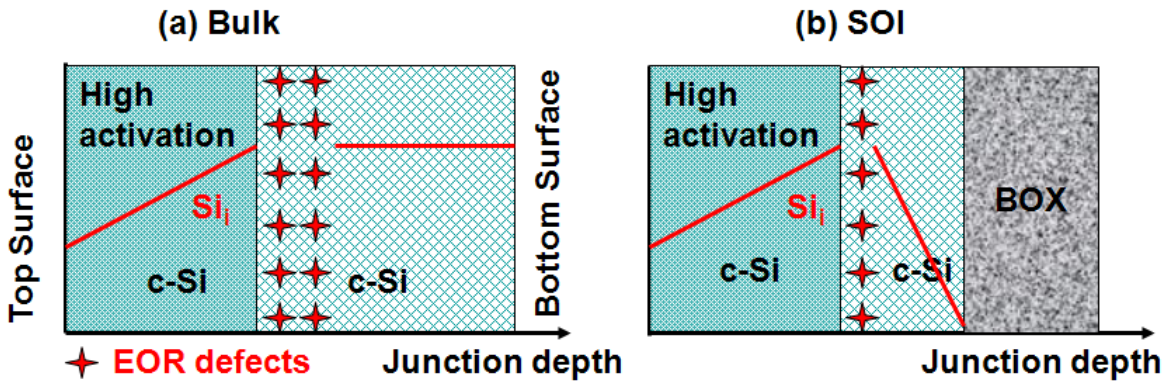


Fig.IV.1 Si_i concentrantion during post activation anneal on bulk [Hamilton'06a] (a) and SOI [Fazzini'08a] (b) samples. On bulk sample, most of the Si_i flows to the top surface, whereas the Si_i can flow either to the Si top surface or the Si/BOX interface on SOI sample.

The Si interstitials can migrate towards the available defect sinks, like the Si top surface and Si bottom surface on bulk samples, as shown in Fig.IV.1-(a). The migration of Si_i is dependent on the distance between the EOR defects band and the defect sink, which influences the supersaturation gradient of Si_i. For very thick bulk samples, most of the Si_i diffuse towards the top surface, which is located closer to the EOR defects band and results in a higher defects gradient, compared to the bottom Si surface. However, for SOI samples, the Si interstitials can move towards either the Si surface or the BOX (Fig.IV.1-(b)). The fluxes of Si interstitials flowing towards the Si top surface and Si/BOX interface is dependent on their distances to the EOR defects band, respectively [Hamilton'06b]. A model for calculating

the Si interstitial fluxes towards the two defect sinks has been proposed in [Fazzini'08a]. The flux of Si interstitials towards the closer defect sink is higher.

IV.1.2 Dopant deactivation mechanisms

During LT SPER anneal, high dopant activation level, above solid solubility, can be achieved. However, the activated dopants are in a metastable state and tend to become deactivated via the formations of clusters with defects. In this section, we will first introduce the solid solubility of impurity at different temperatures. Then the deactivation mechanism of boron and arsenic will be reviewed respectively.

IV.1.2.1 Solid solubility

At a given temperature, there is an upper limit to the amount of an impurity which can be absorbed by silicon, which is called the solid solubility limit for the impurity. In addition, at a given temperature, there is also an upper limit to the amount of an impurity which can be electrically activated in Si, which is called the solid solubility of electrically active dopant. In Fig.IV.2, for boron, phosphorus, antimony and arsenic, the solid solubility of dopant atoms and electrically active dopant atoms are plotted as a function of diffusion temperature, in the temperature range of 900-1200 °C [Fair'77]. When the temperature is below 1000 °C, smaller solid solubility of both dopant atoms and electrically

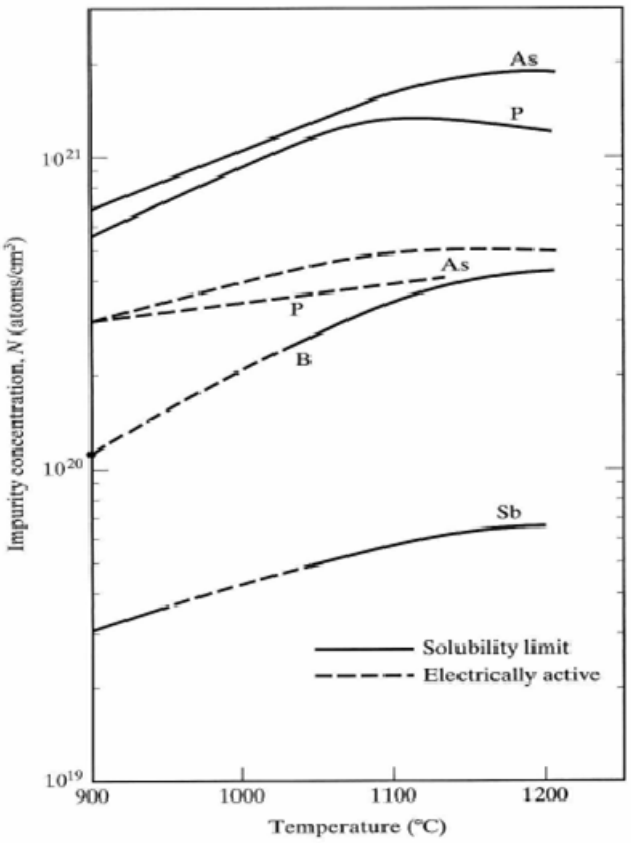


Fig.IV.2 Solid solubility and electrically active impurity concentration limits in silicon for arsenic (As), phosphorus (P), boron (B) and antimony (Sb) [Fair'77].

active dopant atoms are expected as temperature decreases. In [Vick'69], it is reported at 700 °C, the solid solubility of active boron in c-Si is approximated $2.0x10^{19}$ cm^{-3}.

IV.1.2.2 Boron deactivation mechanism

For boron, high activation levels around $1.5\text{-}2x10^{20}$ cm^{-3} have been reported by LT SPER [Duffy'04, Cristiano'04, Lerch'05, Aboy'05]. This activation level is well above the equilibrium solid solubility. In [Cristiano'04], for LT SPER anneal at 650 °C, boron activation around $1.5x10^{20}$ cm^{-3} has been demonstrated which is a decade higher than the solid solubility of boron in Si at 650 °C ($1.5x10^{19}$ cm^{-3}). The boron concentration above the activation level is electrically inactive even after full recrystallization by LT SPER. The inactive boron atoms exist in the form of immobile Boron Interstitial Clusters (BICs) which are formed during the regrowth of the amorphized layer [Aboy'06, Pelaz'09, Aboy'11].

Even though high activation level can be achieved, the activation state realized during LT SPER is metastable. There is a high risk that the activated boron atoms in the regrown Si layer tend to deactivate during the post activation anneals. After post anneal at 700 °C for 100 seconds, 40% deactivation of SPER activated boron has been observed [Mokhberi'02].

There is one important question raised: how do the active boron atoms get deactivated during the post activation anneal? As discussed in section IV.1.2, during the post activation anneal, Si_i are emitted from EOR defects and move towards the top surface of Si, going through the highly activated boron region (Fig.IV.3). During this process, inactive BICs are formed and part of the activated boron atoms is deactivated. The reaction can be written as:

$$B + Si_i \Leftrightarrow BIC \qquad \text{(Eq.IV.1)}$$

The deactivation process will continue until the concentration of Si_i drops to its equilibrium values at the anneal temperature. Then the dissolution of BICs start to be dominant, with the emission of active boron atoms (boron reactivation) [Aboy'06]. Consequently the dose of active boron starts to increase. The critical post anneal when the BICs dissolution becomes dominant depends on many process parameters: the implant, the post anneal duration and temperature. It has been reported that for one specified implant, as

the anneal temperature decreases, a longer anneal duration is required for the BICs dissolution to occur [Aboy'06, Cristiano'06], as illustrated in Fig.IV.4.

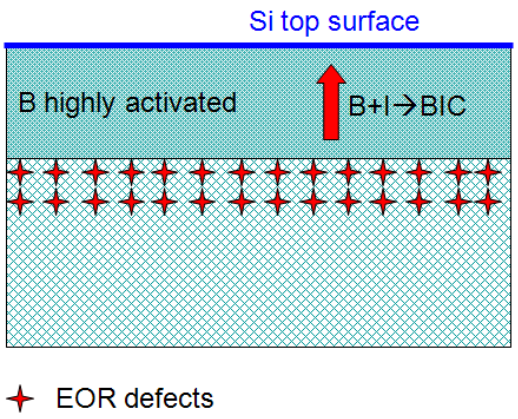


Fig.IV.3 Schematic of EOR defects evolution and of Si_i flux for LT SPER activated boron on bulk sample during post activation anneal. Si_i flow towards the Si top surface and deactivate boron through the formation of inactive BICs. Reducing Si_i flux towards Si top surface is thus important to prevent boron deactivation.

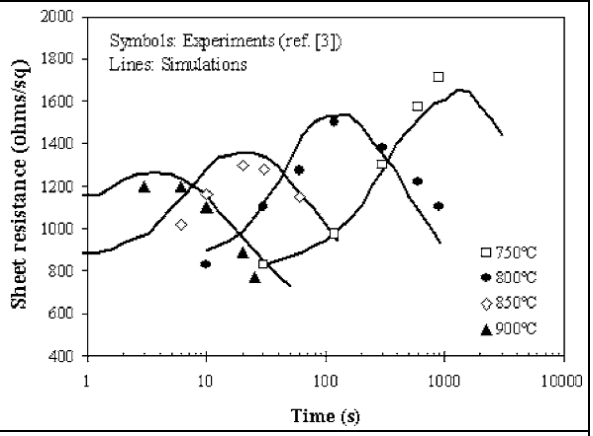


Fig.IV.4 Time evolution of the Rs of a 0.5keV, 10^{15} cm^{-2} boron implant during annealing at different temperatures ranging from 750 to 900 °C subsequent to SPER [Aboy'06]. Experimental data (symbols) are taken from [Lerch'05].

Compared to bulk samples, SOI structure offers the possibility to control the deactivation of LT SPER activated boron. On one hand, as illustrated in Fig.III.23, part of the defect profile is cut off by the BOX. So the initial number of Si_i is lower and the EOR density after SPER is lower than that in bulk [Hamilton'07, Fazzini'08, Saavedra'02]. On the other hand, the Si/BOX interface can also act as a defect sink (Fig.IV.1 and Fig.IV.5), competing with the Si top surface [Ferri'07, Aboy'07, Bazizi'10]. For both the Si top surface and the Si/BOX interface, the defect sinking efficiency is dependent on its distance to the EOR defects band: the smaller the distance is, the stronger the sinking effect will be [Hamilton'07, Bazizi'10]. Theoretically, by locating the EOR as close to the BOX as possible, the Si_i flux flowing to the Si/BOX interface can be increased. As a consequence, the net Si_i flux moves towards the top Si surface is smaller and boron deactivation get decreased. As shown in the literature, boron deactivation has been widely studied in the temperature range of 700 °C to 900 °C [Hamilton'07, Fazzini'08, Aboy'07, Bazizi'10].

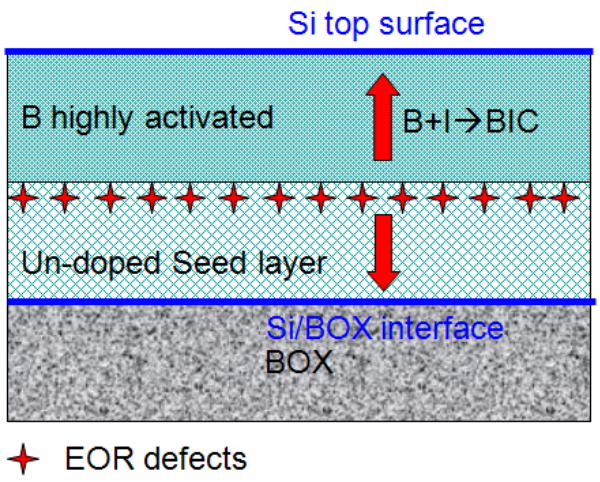


Fig.IV.5 Schematic of EOR defects evolution and of Si_i flux for LT SPER activated boron on SOI during post activation anneal. Si_i can flow either to the Si top surface or to the Si/BOX interface. In the doped region, boron is deactivated through inactive BICs formation with the Si_i flowing to the Si top surface.

However, in the case of 3D sequential integration, the temperatures of interest are much lower than that in the previous works. For the top FETs, the post activation anneals correspond to LT salicidation anneal (450 °C) and back end processing (~400 °C). For the bottom FETs, the maximum processing temperature is reached during LT top FET dopant activation (~600 °C). In this work, boron deactivation was studied between 400 °C and 600 °C, in order to verify the possibility of using LT SPER in 3D sequential integration for bottom and top pFETs. Moreover, the sheet resistance of boron doped LT SPE junction will be analyzed to figure out the potential of using LT SPER for ultra-shallow (~10 nm) junction formation.

IV.1.2.3 Arsenic deactivation mechanism

With the continuous scaling down of device dimensions, highly doped, abrupt junctions are needed. Arsenic has been widely used for the fabrication of nFET, thanks to its low diffusivity and good solid solubility. As devices scales down, high arsenic activation is required to reduce the access resistance. This might be achieved by using non-equilibrium activation techniques (e.g. flash or laser anneal, LT SPER) [Giubertoni'10, Martinez-Limia'08].

LT SPER anneal after an amorphizing arsenic implant is a viable alternative to conventional spike anneal thanks to its high activation above active solid solubility and low dopant diffusion [Martinez-Limia'08]. In [Lietoila'80, Lietoila'81], after LT (560 °C) SPER anneal for 4 minutes, the concentration of active arsenic reaches $5x10^{20}$ cm^{-3} which is more than 2 decades higher than $2x10^{18}$ cm^{-3} (calculated according to [Nobili'99]), the solid solubility of electrically active arsenic in Si at 560 °C. In addition, the LT SPER activated arsenic atoms mainly locate in the former amorphous Si region thanks to its weak dopant diffusion.

After LT SPER, in the former a-Si region, arsenic atoms exist mainly in three forms: (1) activated arsenic (As^+); (2) inactive AsV clusters; (3) inactive SiAs precipitates [Giubertoni'10]. In [Martinez-Limia'08, Pichler'08], a model has been proposed to describe the three different forms of arsenic atoms in the previous a-Si region (Fig.IV.6):

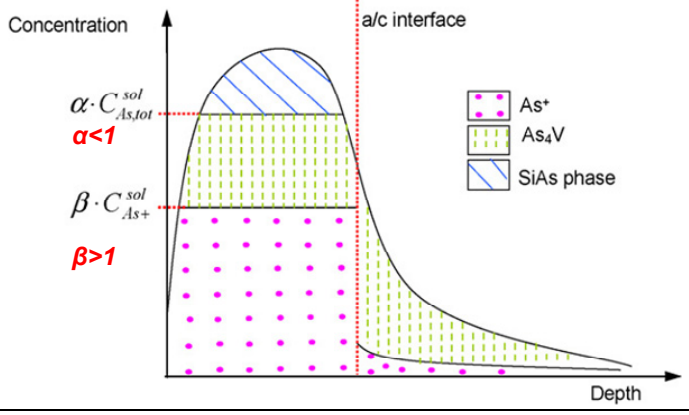


Fig.IV.6 Activation state after SPER. C^{sol}_{As+} and $C^{sol}_{As,tot}$ are the active solubility concentration and the solid solubility concentration for the SPER temperature, respectively [Martinez-Limia'08, Pichler'08].

(I) Active As^+: its concentration is well above the limiting value for equilibrium conditions, which is named as the active solubility concentration ($C_{As+}{}^{sol}$).

(II) Inactive AsV clusters: they exist for arsenic concentration above the As^+, up to a concentration exceeding the solid solubility (α>1).

(III) Inactive SiAs precipitates: which exist at even higher concentrations than the AsV clusters and As^+.

The solid solubility ($C^{sol}_{As,tot}$) and active solid solubility of arsenic (C^{sol}_{As+}) can be expressed by the following equations:

$$C_{As,tot}^{sol} = 1.3\times10^{23}\times\exp\left(\frac{-0.42}{kT}\right)\text{cm}^{-3} \qquad \text{(Eq.IV.2)}$$

$$C_{As+}^{sol} = 2.2\times10^{22}\times\exp\left(\frac{-0.47}{kT}\right)\text{cm}^{-3} \qquad \text{(Eq.IV.3)}$$

where kT is in eV [Nobili'99].

However, as for boron after LT SPER, the highly activated arsenic by LT SPER is not thermally stable and will deactivate towards the active arsenic solubility at equilibrium during the subsequent anneals [Giubertoni'10, Nobili'99]. In [Lietoila'81], for LT SPER samples annealed at 570 °C for 4 minutes, an additional anneal of 36 minutes at 560 °C introduces 24% deactivation of the initial active arsenic dose. So the deactivation of LT SPER activated dopants is a critical challenge for its application in nFET fabrication. For the metastable activated arsenic above the equilibrium solid solubility, deactivation tends to continue until reaching the solid solubility at thermal equilibrium. In [Nobili'99], the deactivation of the laser annealed arsenic is studied: High arsenic activation above 10^{20} cm^{-3} was achieved and the implantation induced defects ware removed by high power laser anneal. It is found that the deactivation of arsenic lasts for more than 160 hours during post anneal at 500 ºC towards the thermal equilibrium solid solubility.

The dominant deactivation mechanism is the formation of As-Vacancy (V) clusters with the injection of Si_i [Rousseau'98, Tsamis'05]. Theoretical studies have suggested that AsV, As_2V, As_3V, As_4V, As_2V_2 and As_3V_2 all may play a role in arsenic deactivation [Harrison'04]. However, most of the As-Vacancy clusters exist in the form of As_2V, As_3V and As_4V, which are more energetically favored [Kong'08, Skarlatos'07, Pinacho'05]. The deactivation mechanism can be described by the following macroscopic reaction:

$$nAs \Leftrightarrow As_nV + Si_i \qquad \text{(Eq.IV.4)}$$

where n stands for the arsenic atoms participating in the clusters with values between 2 and 4 [Tsamis'05, Skarlatos'07]. As shown in (Eq.IV.4), Si interstitials are injected during the deactivation, which has been experimentally reported in [Rousseau'98, Tsamis'05, Skarlatos'07].

In order to figure out the possibility of applying LT SPER activation for the fabrication of FDSOI nFETs, it is important to confirm that high activation of arsenic is achieved not only after LT SPER but also after the subsequent annealing during the further processing of device. However, until now, there is little study on the deactivation of LT SPER activated arsenic on ETSOI.

During the LT SPER, residual EOR defects are left below the previous a-c interface and tend to act as a source of Si interstitials during post activation anneal. From (Eq.IV.4), it might be expected that the super-saturation of Si interstitials tends to make the reaction move backward and delay arsenic deactivation. On the opposite, if there is a lack of Si interstitials, the deactivation reaction might tend to move forward, resulting in the decrease of carrier concentration and the increase of sheet resistance. As discussed in Section.IV.2, on SOI samples, thanks to the defects cutting effect and defect sinking effect of BOX, by locating the EOR band close the BOX: less EOR defects will be formed after LT SPER and the Si_i flux towards the Si top surface is reduced during post anneal. Does this lower Si interstitial flux enhance the arsenic deactivation on SOI compared to bulk? Does arsenic deactivation limit the application of LT SPER?

In the following sections, we will compare the sheet resistances of boron/arsenic doped junctions by LT SPER and conventional HT process, to figure out the possibility of using LT SPER to replace conventional HT process. Also we will analyze the influence of Si/BOX interface on the deactivation of LT SPER activated arsenic during the post activation anneal between 400 °C and 600 °C, to study the possibility for using SPER for the fabrication of top and bottom nFETs in 3D sequential integration. Boron and arsenic will be discussed in section IV.2 and IV.3, respectively.

IV.2 Boron activation and deactivation: Experiment and results

IV.2.1 Experiment

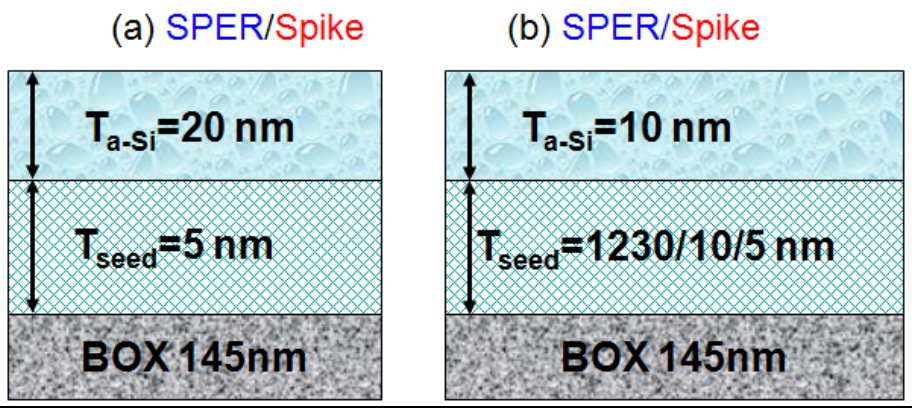


Fig.IV.7 Schematic representation of the experimental P splits with $T_{a\text{-}Si}$ the amorphized Si thickness and T_{seed} the residual crystalline Si layer(which will act as a seed layer during the following SPER anneal).

SOI wafers with a BOX of 145 nm and different Si thickness (T_{si}) are used in the experiment. Different pre-amorphization implantations are used to achieve different amorphous Si thickness ($T_{a\text{-}si}$) and seed thickness (T_{seed}). The splits are schematically summarized in Fig.IV.7. For LT SPER activated splits, the EOR defects are located just below the a-c interface, so the distance from the top of EOR band to the BOX (T_{EOR_BOX}) can be approximated taken as T_{seed}.

To compare boron activation between LT SPER and HT spike anneal, samples of type (a) were fabricated (Fig.IV.7). In spike split, BF_2 (9 kev/1x10^{15} cm^{-2}) is implanted. In SPER split, a 1x10^{15} cm^{-2} dose of Ge was implanted at 11 kev, to pre-amorphize 20 nm Si. In order to obtain the same as-implanted boron profile as spike split, boron (2 kev/1x10^{15} cm^{-2}) was implanted for SPER split. Then the samples were activated by either LT SPER (600 °C for 1 min in N_2) or HT spike (1050 °C).

To study the thermal stability of LT activated dopants and its dependence on the distance between the EOR defects layer and the BOX, experiments were carried out on SOI samples (Fig.IV.7-(b)), with three different Si thicknesses (1240 nm, 20 nm, and 15 nm). To pre-amorphize 10 nm Si, Ge (4 kev/1x10^{15} cm^{-2}) was implanted, followed by boron implant (1 kev/1x10^{15} cm^{-2}). As shown in Fig.IV.7-(b), there are three different crystalline Si seed thicknesses (1230 nm, 10 nm and 5 nm). LT SPER anneal is applied to activate the boron atoms. All the samples were post-annealed in N_2. Different temperatures (400 °C, 500 °C, 600 °C) and anneal durations (0, 2, 10 hours) have been experimented.

The sheet resistance (Rs) of each sample was measured by four point probe method. Moreover, active dopant dose and carrier mobility were extracted independently from Hall measurements.

IV.2.2 Boron activation study

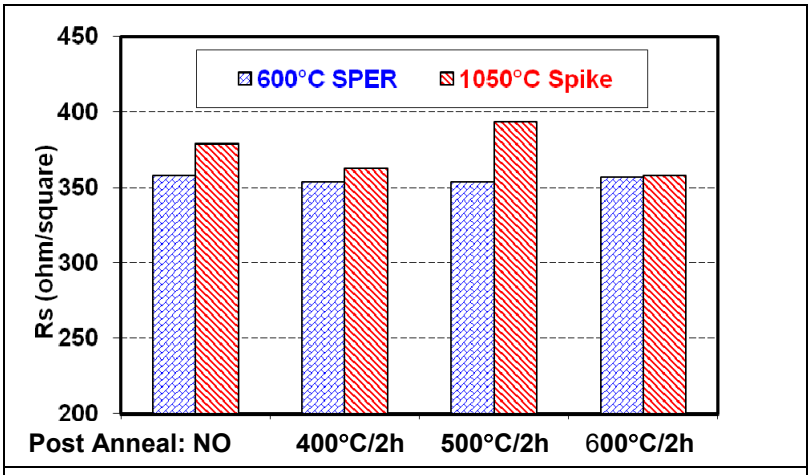


Fig.IV.8 Rs comparison of LT SPER and HT spike activation for the same as-implanted boron profile. In LT SPER split, 20 nm of Si was pre-amorphized on 25 nm SOI.

The Rs values of SPER and spike activated samples are compared in Fig.IV.8. It is shown that, in both the initial activated and post annealed samples, LT SPER samples of group (a) always show lower Rs than HT spike samples. Our implant condition is close to the LDD implant in standard FDSOI device, and we can conclude that LT SPER can provide similar or even slightly lower sheet resistance as the standard HT process at CEA-LETI. In conventional HT process, BF_2 is implanted, and the boron profile is overlapped to that of F, boron tend to form clusters with F and become deactivated [Cowern'05, Harrison'07].

For one of the samples in group (b), 10 nm was pre-amorphized on 15 nm SOI (Fig.IV.7-(b)). From Hall Effect measurement, the active boron dose is about 3.3×10^{14} cm^{-2}, and the average active boron concentration value is around 2×10^{20} cm^{-3}, which is in accordance with the literature [Jain'04]. To conclude, for the fabrication of ultra-shallow junction, LT SPER Boron is suitable for the fabrication of FDSOI pFETs.

IV.2.3 Boron deactivation study

To analyze boron deactivation, Rs values before and after post activation anneals were compared. In Fig.IV.9, sheet resistance values are plotted as a function of post activation anneal duration at 400 °C and shown to be stable at this temperature. This means that the access resistance of LT top pFETs in 3D sequential integration is stable through the back end process.

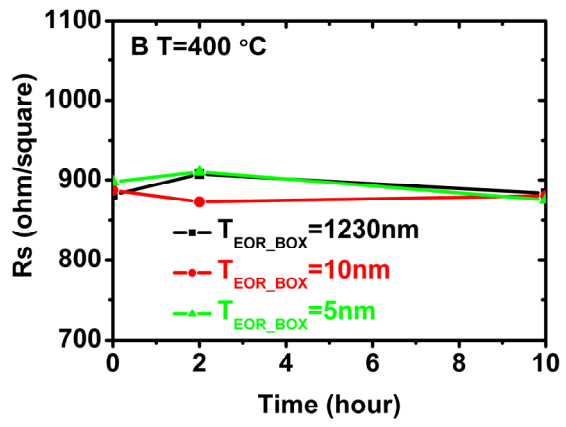


Fig.IV.9 Sheet resistance evolution of boron doped junction as a function of anneal time at 400 ºC. Boron is shown to be stable at this temperature.

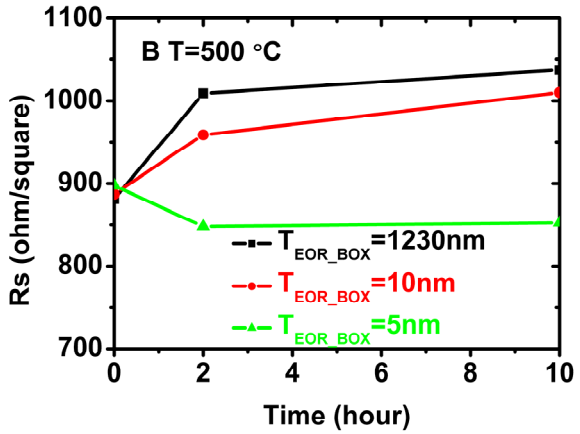


Fig.IV.10 Sheet resistance evolution of boron doped junction as a function of anneal time at 500 °C. During the initial phase of anneal, Rs increases for T_{EOR_BOX} =1230 nm and 10 nm, whereas it decreases for T_{EOR_BOX}=5 nm.

However, at 500 °C, it is shown in Fig.IV.10 that an increase of Rs is observed during the first 2 hours of the post anneal for high T_{EOR_BOX} (1230 nm and 10 nm) samples, while a decrease was observed for the low T_{EOR_BOX} (5 nm) samples. To gain more insight on this phenomenon, Fig.IV.11 plots Rs as a function of anneal temperature for the same 2 hours duration. For T_{EOR_BOX}=1230 nm or 10 nm, Rs starts to increase with anneal temperature above 500 °C. In contrast, for T_{EOR_BOX}=5 nm, smaller Rs values can be reached after a post activation anneal at 500 °C or 600 °C for 2 hours.

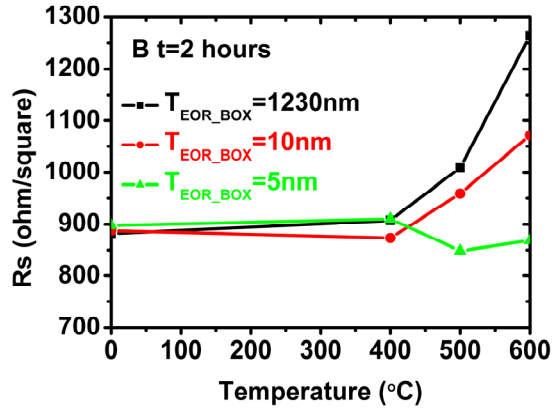


Fig.IV.11 For boron doped junctions by LT SPER activation, sheet resistance evolution with boron doped junction with 2 hours annealing. Above T=500 °C, Rs start to increase with T for T_{EOR_BOX}=1230 nm or 10 nm, while it decreases slightly for T_{EOR_BOX}=5 nm.

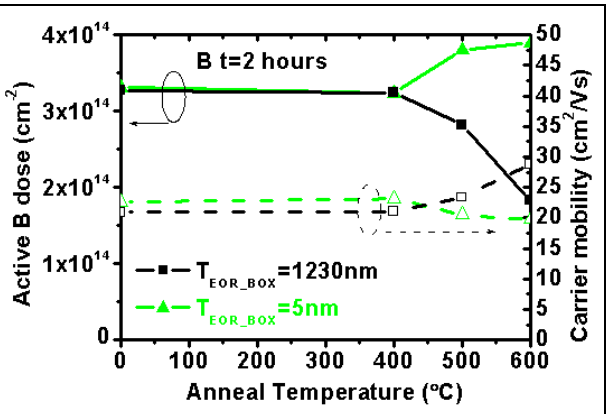


Fig.IV.12 For boron doped junctions by LT SPER activation, the active dose and carrier mobility extracted from Hall effect tests and plotted as a function of post activation anneal temperature (annealing time t=2hours).

Indeed, sheet resistance can be expressed by [Cristiano'04]:

$$Rs = \frac{1}{q\int_0^{Xj} \mu(x)C(x)dx} \qquad \text{(Eq.IV.5)}$$

where X_j is the junction depth, C(x) the carrier concentration along depth direction x, μ(x) the concentration dependent carrier mobility and q the electronic charge. According to (Eq.IV.5), Rs reduction can result from either higher carrier concentration or higher carrier mobility.

To distinguish between the two possible causes of Rs variation, Hall Effect measurements were performed to extract active dose Ns and carrier mobility μ (Fig.IV.12). For T_{EOR_BOX}=5 nm, higher Ns and slightly lower μ were observed after anneal at 500 °C or 600 °C for 2 hours. The higher Ns is an indication of boron reactivation. Our interpretation is that low T_{EOR_BOX} samples benefit from two phenomena (Fig.IV.13): (i) the initial EOR defects density is lower than that of thicker samples due to the defects profile cutting effect of BOX, and (ii) EOR defects are located closer to the BOX, so that the sinking effect of Si/BOX interface is stronger than that of Si top surface. As a result, most Si_i are absorbed by the BOX, and the concentration of Si_i is decreased. As a consequence, the boron deactivation reaction (Eq.IV.1) is reversed, and boron get reactivated.

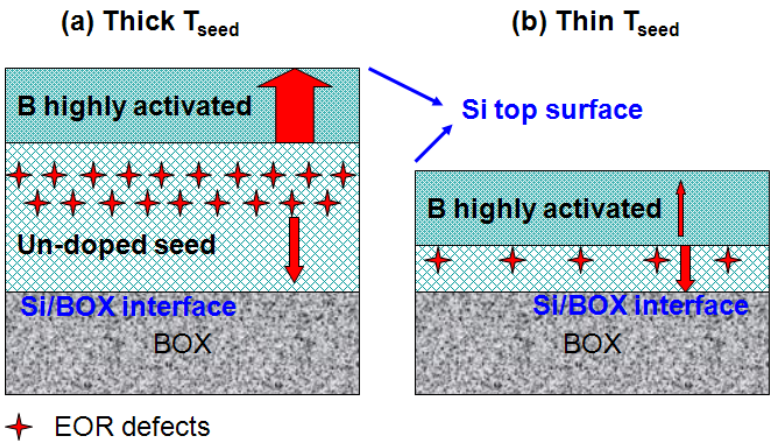


Fig.IV.13 For the same pre-amorphization, Si_i flux during post anneal on LT SPER boron samples with high (a) and low T_{EOR_BOX} (b).

As T_{EOR_BOX}=5 nm corresponds to the LDD implant in our LT FDSOI process, we can conclude that LT boron SPER activation is compatible with the fabrication of top and bottom FDSOI pFETs in LT 3D sequential integration. Compared to boron deactivation on thick T_{Si} samples, FDSOI offers one solution to overcome the challenge of boron deactivation, which is challenging for the LT fabrication of scaled pFETs.

IV.3 Arsenic activation and deactivation: Experiment and results

IV.3.1 Experiment

Schematic plots of N splits are summarized in Fig.IV.14. Same as boron splits discussed in the section above, SOI wafers with 145 nm BOX and different Si thickness (T_{Si}) are used in the experiment. In group (a), arsenic (10kev/1E15cm^{-2}) implantations are used for $T_{a\text{-}si}$=20 nm. While in group (b), for $T_{a\text{-}si}$=10 nm, arsenic self-amorphization (4kev/1E15cm^{-2}) is used. Then the samples are activated by either LT SPER (600 °C/1min/N_2) or spike (1080 °C). After activation, to study the thermal stability of the activated dopants, the samples are post-annealed at 400/500/600 °C for 2h and 400/500 °C for 10h in N_2.

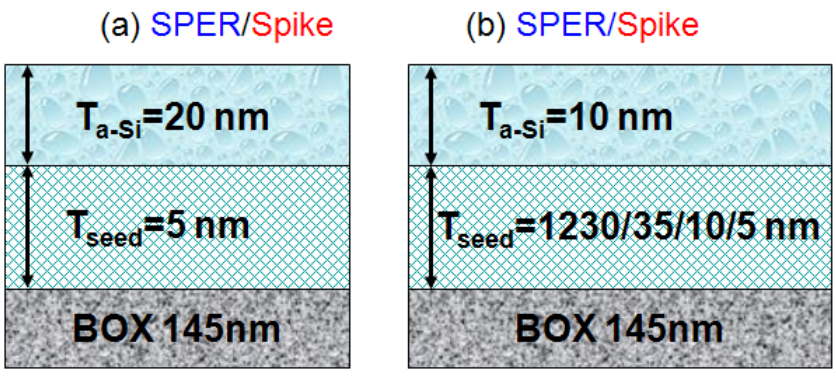


Fig.IV.14 Schematic representation of the experimental N splits with $T_{a\text{-}Si}$ the amorphized Si thickness and T_{seed} the residual crystalline Si layer(which will act as a seed layer during the following LT SPER anneal).

IV.3.2 Arsenic activation: LT SPER versus spike

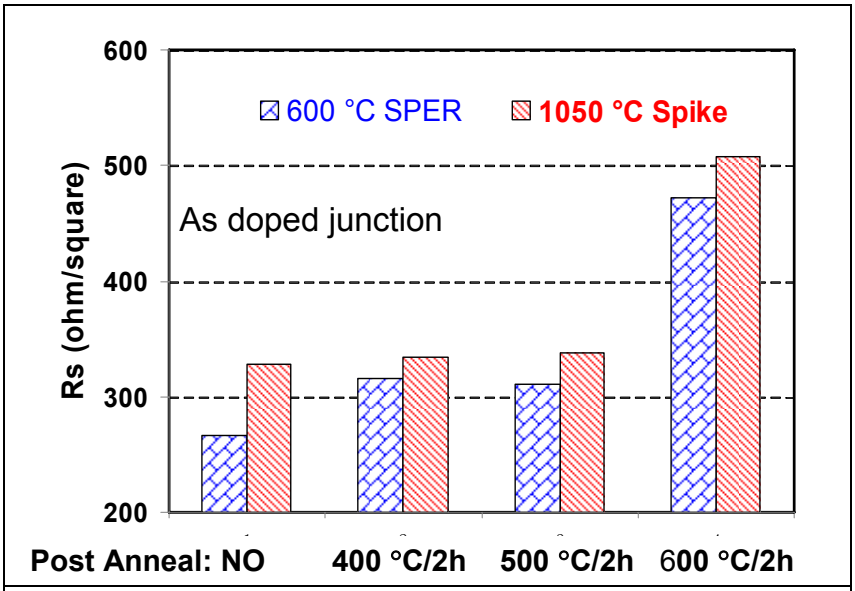


Fig.IV.15 Rs comparison of LT SPER and HT spike activation for samples with the same arsenic implantation. 20 nm of Si was pre-amorphized on 25 nm SOI.

In Fig.IV.15, the sheet resistance values of LT SPER and spike activated samples are compared, before and after different post activation anneals. It is found that the sheet resistance of LT SPER and HT spike samples are similar, both just after the activation (no post anneal) and after post activation anneals. Since this implant condition is close to the LDD implant in standard FDSOI nFETs, and we can conclude that LT SPER can provide similar or

even slightly lower sheet resistance as the standard HT FDSOI nFETs process at CEA-LETI. LT SPER activation of arsenic is applicable for the fabrication of FDSOI nFETs in 3D sequential integration.

IV.3.3 Deactivation of LT SPER arsenic on SOI

For LT SPER activated arsenic, as shown in Fig.16, it is found that arsenic is stable at 400 °C. So LT SPER activated arsenic is suitable for the fabrication of top nFETs, for it can survive to the back end process of top FET. However, for post activation anneal at 500 °C (Fig.IV.17), Rs increases with anneal duration which indicates dopant deactivation. In addition, it is observed that the deactivation increases with anneal temperature (Fig.IV.17).

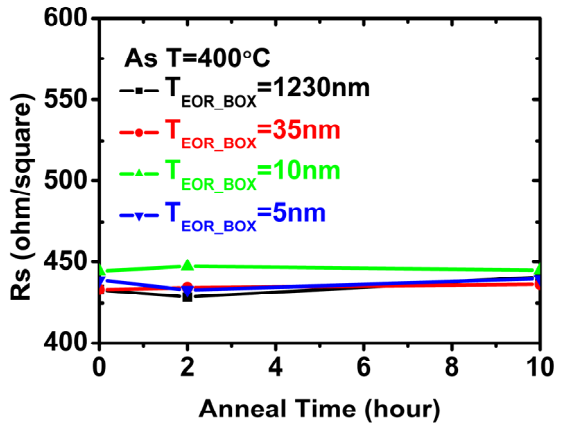


Fig.IV.16 Rs of arsenic doped junction as a function of post activation anneal time at 400 ºC. Arsenic is stable at 400 ºC.

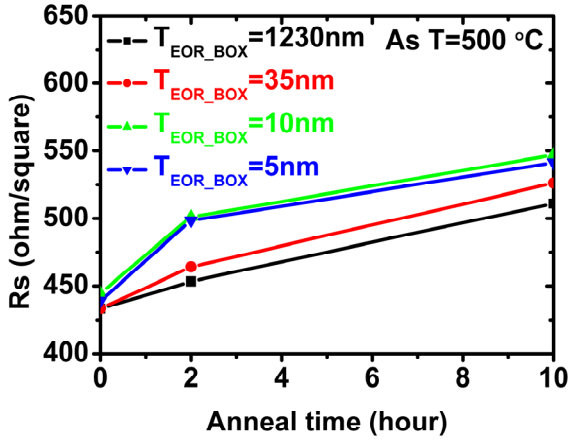


Fig.IV.17 Rs as a function of post activation anneal time at 500 ºC. Rs increases with anneal duration.

Also, from Fig.17 and Fig.IV.18 it is found that Rs increase is even higher for the case of lower T_{EOR_BOX}. This might be interpreted by the fact that arsenic deactivation is caused by the formation of AsV clusters with the emission of Si interstitials. On samples with lower T_{EOR_BOX}: (I) the initial EOR defects density is lower thanks to the stronger defects cutting-off effect; (II) the concentration of Si interstitial is even lower due to the stronger defect sinking effect of the Si/BOX interface. As a consequence, the arsenic activation reaction (Eq.IV.4) might tend to move in the forward direction and arsenic deactivation is enhanced on samples with smaller T_{EOR_BOX}.

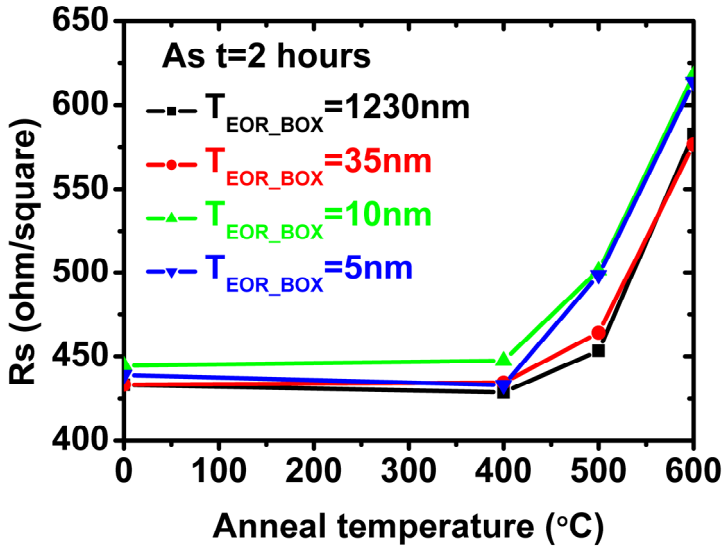


Fig.IV.18 For As doped junction activated with LT SPER, from T=500 °C, Rs increases with T, for the same anneal duration of 2 hours.

We can conclude that LT SPER activated arsenic are not stable during post anneal at 500-600 ºC. In contrast with boron, on ETSOI samples, deactivation of LT SPER activated arsenic is enhanced. However, as shown in Section.IV.3.2, we still managed to achieve similar sheet resistance in LT SPER samples and standard HT process, which allows us to use LT SPER in 3D sequential integration for FDSOI nFETs on both the top and bottom layers in 3D sequential integration.

IV.4 Conclusions

In this Chapter, to gain insight on the possibility the activation and thermal stability of LT SPER activated dopants (both boron and arsenic) is compared to that of conventional HT processes.

For boron:

It is found that the LT SPER activated boron is stable at 400 °C and suitable for the fabrication of top FDSOI pFETs in 3D sequential integration.

Based on the analysis of Rs result and Hall effect test results, we can conclude that, for the application of LT SPER on SOI, boron deactivation are well controlled and boron reactivation is observed after 500 °C/600 °C anneal for 2 hours. This is obtained by locating the EOR band as close to the Si/BOX interface as possible: the Si_i cutting off effect of BOX

and strong defect sinking effect of the Si/BOX interface is enhanced, which help to well control boron deactivation and make reactivation to be the dominant reaction.

In addition, for the implantation into 25 nm SOI structure, which is similar to the LDD implant in FDSOI: it is observed that the sheet resistance of LT SPER activated junction is similar to that of conventional spike activated junction, both initially after the activation anneal and after post activation anneal between 400 °C and 600 °C.

So we can conclude that LT SPER activated boron is suitable for the fabrication of both top and bottom FDSOI pFETs in the 3D sequential integration scheme.

For arsenic:

Unlike boron, since arsenic is deactivated through the formation of As-Vacancy clusters, arsenic deactivation can not be reduced by reducing T_{EOR_BOX} and even higher arsenic deactivation is observed for smaller T_{EOR_BOX}.

However, considering the activation of arsenic in the case of FDSOI application, LT SPER activated junctions show similar sheet resistance as that of conventional spike activate junctions, both initially after the activation anneal and after the post activation anneal in the temperature range between 400 °C and 600 °C. So the LT SPER activated arsenic can be applied for the fabrication of bottom and top FDSOI nFETs in the 3D sequential integration scheme.

Chapter V : Conclusions and perspectives

V.1 Conclusions

3D sequential integration with wafer bonding of top active layer is the only solution to make full use of the third dimension. It can help to reduce the length of interconnection wire, RC delay and power dissipation. It also allows independent optimization of top and bottom transistors for improving system performance.

However, LT (<600 °C) process is mandatory for the fabrication of top FET. Low temperature solid phase epitaxial regrowth is an interesting candidate for dopants activation thanks to its following advantages: (1) High dopants activation level above the solid solubility limit at thermal equilibrium; (2) Abrupt and ultra-shallow junctions induced by its low diffusion; (3) Its low thermal budget broadens the choice of materials for metal gate work function tuning.

So, it is interesting to apply the LT SPER activation technique for the fabrication of FDSOI devices on both the bottom and the top layers in 3D sequential integration scheme. However, it is also very challenging. In this thesis, we have reviewed the challenges and found the solutions to overcome the main challenges.

In Chapter II, the mechanism and properties of LT SPER anneal is firstly reviewed. Then, we focused on solving two of the challenges for its application for FDSOI FETs.

(I) Preventing full pre-amorphization of active layer: Crystalline seed layer is necessary for successful recrystallization of the previous amorphized layer. For FDSOI, the active layer is very thin, integration scheme and implant conditions should be optimized. In our work, the following two ways were successfully applied to avoid the full amorphization of the thin active Si layer of FDSOI devices: (a) LDD implant is carried out after the epitaxy of raised source and drain; (b) Accurate prediction of implant energy by KMC simulation.

(II) Preventing LDD to gate underlap: Due to the low diffusion of LT SPER, LDD and gate might be underlapped, the access resistance and device performance might be degraded. The modification of LDD implant tilt is expected to be an efficient way to adjust the LDD to gate overlap. In our work, similar

performances are achieved on LT and HT devices with short gate length (L_G=30 nm). Similar I_{OFF}-I_{ON} and SCE control can be achieved by optimizing the LDD implant tilt.

(1) For LT FDSOI nFETs, the LDD implant tilt does not need to increase. With the same LDD implant of 20 °, similar IOFF-ION and SCE control are achieved. Thanks to the low thermal budget of LT SPER activation, it is found that the regrowth of interfacial SiO2 at the boundary of gate to channel interface is well controlled. This helps to improve the device performance of small scale devices in LT process. However, higher interface state density is found in LT SPER process.

(2) For pFETs with 8 nm first spacer and a SiGe "mushroom" on top of gate, a higher LDD implant tilt of 30° is required for similar device performance of LT and HT pFETs. For further optimization, LT SiGe epitaxy with high selectivity is mandatory to whittle the shadow effect of gate stack. Consequently, the optimized LDD tilt required for LT pFET might be lower than 30 °. In addition, LT splits show higher mean value of D_{it} which mainly locate close to the conduction band.

In addition, it is observed that the LT SPER activation might help to avoid the problem of effective work function migration during HT activation. This allows us to broaden the choice of metal gate materials for work function tuning of different applications.

In Chapter III, the possible mechanisms of GIDL current are firstly reviewed. Then the experimental observation and possible causes of 1.5 decades higher GIDL current of LT SPER devices on thick SOI (25 nm) are introduced: higher trap assisted tunneling due to the higher EOR defects density or higher band to band tunneling due to the abrupt junction. It is important to distinguish the mechanism responsible for the leakage increase of LT activated devices. To do this, one interesting way is to extract GIDL parameter B, which is dependent on the effective band gap of Si. And smaller B vale is expected for trap induced leakage.

Then, the limits of traditional mechanism analysis of GIDL are reviewed: the lack of accurate model of GIDL current and the inaccurate calculation of electric field. An improved approach is proposed for GIDL mechanism analysis, overcoming the limitations of traditional method by experimental determination of the electrical field. To properly apply the new

approach for GIDL analysis to FDSOI devices, a detailed methodology for proper extraction conditions has been proposed: $I_D(V_G, T)$, $I_S(V_G, T)$ and $I_G(V_G, T)$ curves are used to identify the devices, bias ranges and temperatures for which the GIDL current is dominated by tunneling and the contribution of gate leakage is neglectable.

For devices on 25 nm SOI, using the new approach with the methodology proposed it is found that the high GIDL current of LT transistors is due to the residual EOR defects. Compared to HT devices, lower B value is observed on LT devices, which indicates that the effective band gap is reduced due to the existence of residual EOR defects which attribute to the GIDL generation.

To reduce the EOR defects density and the GIDL leakage of LT SPER transistors on SOI, extremely thin SOI is demonstrated to be an efficient way. On extremely thin SOI, the defect cutting off effect and defect sinking effect of BOX can be enhanced, the density of residual EOR defects is much lower than that on thick SOI. Same I_{Dmin} performance has been achieved on LT/HT nFETs with 6 nm SOI. Extraction of the GIDL parameter B is consistent with I_{Dmin} reduction in LT SPER devices. B value of LT SPER activated devices on ETSOI (6 nm) is much higher than for 25 nm SOI, which indicates the higher effective band gap and lower EOR defect density on ETSOI.

In Chapter IV, the activation and thermal stability of LT SPER activated boron and arsenic is studied. To confirm whether LT SPER activation is compatible with the 3D sequential integration scheme, we explored the deactivation of LT SPER activated dopants in the temperature range of 400 °C to 600 °C.

Considering the thermal stability of LT SPER activated dopants on SOI samples:

For boron, it is found that by locating the EOR band as close to the Si/BOX interface as possible, boron deactivation is well controlled and boron reactivation is observed after 500 °C/600 °C anneal for 2 hours. On one hand, the EOR defects density is lower thanks to the Si interstitial cutting off effect of BOX. On the other hand, the defect sinking effect of the Si/BOX interface is stronger, which helps to limit the boron deactivation and to make reactivation to be the dominant reaction.

On the contrast, since arsenic is deactivated through the formation of As-Vacancy clusters, arsenic deactivation can not be reduced by reducing T_{EOR_BOX} and slightly higher deactivation is observed for smaller T_{EOR_BOX}.

However, in the case of FDSOI source drain fabrication, for both boron and arsenic, it is observed that the sheet resistances of LT SPER and HT activated junction are similar, both initially after the activation anneal or after the post activation anneals at different temperatures between 400 °C and 600 °C. So LT SPER appears to be suitable for the fabrication of both bottom and top FDSOI transistors.

V.2 Perspectives

Based on the working experience of the author, future works in the following aspects are proposed, for the goal of applying LT SPER for the fabrication of sub-22nm devices:

(I) Considering the gate stack: Higher interface state density has been observed in the LT splits. To further improve the performance of LT SPER activated devices, it is necessary to improve the quality of gate to channel interface in LT process. Further optimization of forming gas anneal (higher pressure/longer duration or pure H_2) are interesting. This is very critical for achieving LT fabricated devices with good reliability. In addition, there is lack of research about V_{TH} tuning with different metal gate materials in LT process for different applications. This can help to optimize the systemic performance of 3D sequential integration, e.g. matched V_{TH} of nFET and pFET are critical to ensure good static noise margin performance of SRAM.

(II) Considering junction profile: On LT SPER activated nFETs, surprisingly, it is found that LT S/D are overlapped to gate without increasing the LDD tilt, compared to that in HT process. This might be caused by the transient enhanced diffusion of arsenic towards the channel? It is very interesting to quantify the 2D dopant profile. Also, accurate TCAD simulation of LT SPER processed MOSFET is interesting for offering guideline to optimize process parameters.

(III) Considering LT FDSOI pFETs, to ensure high hole mobility and low device leakage, optimization of LT SiGe RSD epitaxy with high selectivity is required for high quality of the interface between SiGe RSD and Si channel.

Résumé en français

Chapitre I: Introduction

L'augmentation de densité d'intégration des technologies CMOS est vitale pour poursuivre le développement des circuits intégrés (IC). Cependant, la réduction des dimensions du transistor MOS se heurte à l'augmentation des effets canal court (SCE, pour *Short Channel Effects*), à l'allongement des délais d'interconnexion et à la croissance des coûts de production. Un bon moyen de remédier à ces défis et de poursuivre la loi de Moore serait l'intégration 3D, qui consiste à empiler les composants les uns au dessus des autres.

Nous expliquons comment une intégration 3D séquentielle, mettant en jeu une technique de collage de plaques pour réaliser la couche active supérieure, est la seule solution pour tirer pleinement parti de la troisième dimension. Elle peut aider à réduire la longueur des lignes d'interconnexions, les constantes de temps RC associées et la dissipation de puissance. Elle permet également d'optimiser indépendamment les transistors supérieur et inférieur pour améliorer les performances du système.

Toutefois, avec cette approche, il est indispensable d'utiliser des procédés de fabrication à basse température (<600 °C) pour fabriquer les transistors de la couche supérieure. La recroissance épitaxiale en phase solide (SPER, pour *Solid Phase Epitaxial Regrowth*) à basse température (LT) est une technique intéressante pour l'activation des dopants. Elle présente les avantages suivants: (1) bonne activation des dopants, au-dessus de la limite de solubilité solide à l'équilibre thermique, (2) faible diffusion des dopants permettant la réalisation de jonctions abruptes ultra fines; (3) faible bilan thermique, élargissant le choix des matériaux pour l'ajustement du travail de sortie de la grille métallique.

En raison de ses propriétés spécifiques, les principaux défis posés par l'utilisation de la technique LT SPER pour la fabrication de transistors SOI totalement désertés (FDSOI) sont les suivants:

(1) En cas d'amorphisation complète du film SOI, il peut être impossible de recristalliser correctement la couche amorphe pendant le recuit SPER à basse température;

(2) Du fait de la fable diffusion des dopants pendant l'activation SPER à basse température, il peut être nécessaire de redimensionner les étapes de réalisation des régions dopées de source/drain pour assurer leur recouvrement par la grille, sous peine de dégrader la résistance d'accès et la performance I_{ON} du transistor;

(3) En raison de la raideur des jonctions ou de la présence de défauts résiduels, on risque d'observer de forts courants de fruite, et en particulier du GIDL (pour Gate Induced Drain Leakage, fuite de drain induite par la grille);

(4) Les dopants activés par LT SPER ne sont pas dans des états thermodynamiquement stables et tendent à se désactiver lors des recuits ultérieurs. La désactivation peut en outre être renforcée par la présence résiduelle de défauts d'implantation enterrés (défauts EOR, pour End Of Range) non recuits.

Dans ce travail, nous avons cherché à résoudre les quatre défis ci-dessus.

Chapitre II: Optimisation des transistors FDSOI activés à basse température

Dans ce chapitre, nous rappelons les mécanismes mis en jeu pendant le recuit LT SPER. Nous nous concentrons ensuite sur la résolution des deux premiers défis mentionnés plus haut pour l'application de cette technique à la fabrication de transistors FDSOI.

(I) Pré-amorphisation de la couche active: En FDSOI, la couche active est très mince. La méthodologie d'intégration et les conditions d'implantation doivent être optimisées pour en éviter l'amorphisation complète. Dans notre travail, nous avons combiné avec succès les deux méthodes suivantes: (a) l'implantation LDD est effectuée après l'épitaxie des source et drain surélevés; (b) l'énergie d'implantation est prédite avec exactitude par simulation KMC (Kinetic Monte-Carlo).

(II) Recouvrement de grille: l'objectif est d'assurer le recouvrement des zones de source et drain par la grille.. L'ajustement de l'angle d'implantation LDD (pour Lightly Doped Drain, zones faiblement dopées de source et drain) devrait être un moyen efficace pour régler le recouvrement de grille. Dans notre travail, nous avons obtenu des performances similaires pour des composants LT et HT à grille courte (L_G=30 nm). L'optimisation de l'angle d'implantation LDD permet d'atteindre des performances similaires en termes de compromis I_{OFF}-I_{ON} et de contrôle des effets de canal court.

(1) Pour les transistors nFET FDSOI activés à basse température, il n'est pas nécessaire d'augmenter l'angle d'implantation LDD. Avec la même implantation LDD à 20º, on atteint des I_{OFF}-I_{ON} et un contrôle SCE similaires à basse et haute température (Fig.1 et Fig.2). L'analyse détaillée des résultats a permis d'identifier la raison de ce résultat inattendu. On constate que, grâce à son faible bilan thermique, l'activation SPER, permet de mieux contrôler la recroissance de SiO_2 à l'interface entre canal et diélectrique de grille. Cela contribue à améliorer les performances des dispositifs à grille courte réalisés à basse température. Cependant, on obtient des densités d'états d'interface plus élevées avec le procédé LT SPER.

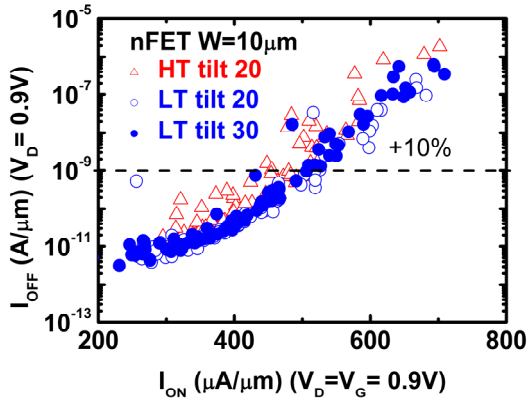


Fig.1 Compromis I_{OFF}-I_{ON} pour les nFETs, de largeur W=10 µm, et de longueur de grille L_G comprise entre 30 nm et 10 µm. A courant I_{OFF} donné, de 10^{-9} A/µm, I_{ON} est environ 10% plus grand dans les nFETs LT que dans les nFETs HT.

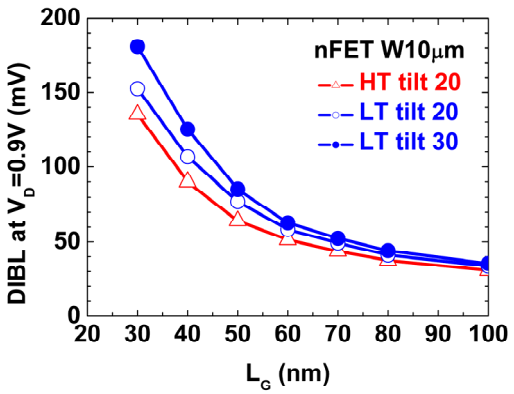


Fig.2 Dérive du DIBL à faible longueur de grille pour les nFETs LT et HT. W=10 µm. Pour un même angle d'implantation de 20 º, on obtient des courbes DIBL-L_G similaires pour les deux types de transistors. Pour les dégroupages à basse température, la caractéristique DIBL-L_G est dégradée par l'utilisation d'un angle d'implantation de 30 º, ce qui est le signe d'un recouvrement de grille plus important (canal plus court).

(2) Pour les transistors pFET, qui avaient été réalisés avec un premier espaceur de 8 nm de largeur, et présentaient une excroissance SiGe en forme de champignon sur le dessus de la grille, un angle d'implantation LDD de 30° a été nécessaire pour obtenir des transistors pFET LT présentant des performances similaires aux pFETs HT. Pour poursuivre l'optimisation, il sera nécessaire de recourir à une épitaxie à basse température de SiGe, avec une sélectivité plus grande que dans le procédé actuel, afin de limiter l'effet d'ombrage de l'empilement de grille. L'angle optimal d'implantation LDD des pFETs LT pourra alors être

éventuellement inférieur à 30º. Par ailleurs, pour les transistors LT, on a obtenu une densité d'états d'interface (D_{it}) supérieure, principalement localisée près de la bande de conduction.

En outre, on a constaté que l'activation LT SPER pourrait aider à éviter le problème de la migration du travail de sortie effectif vers le milieu de la bande interdite qui est observée lors de l'activation HT. Cela nous permet d'élargir le choix des matériaux pour le réglage du travail de sortie de la grille métal, en fonction des applications.

Chapitre III: Optimisation du GIDL dans les transistors activés à basse température

Dans ce chapitre, nous passons d'abord en revue les mécanismes susceptibles de provoquer l'apparition d'un courant de fuite GIDL. Les résultats expérimentaux font apparaître un courant GIDL plus grand de 1,5 ordres de grandeur dans les transistors réalisés par SPER LT sur SOI épais (25 nm). Nous en analysons les causes possibles: augmentation du courant tunnel assisté par pièges en raison de la densité de défauts EOR plus élevée ou augmentation du courant tunnel bande à bande en raison de la jonction abrupte. Il est important d'identifier le mécanisme responsable de cette augmentation des fuites dans les dispositifs LT. Pour ce faire, une technique intéressante consiste à extraire l'un des paramètres du courant GIDL, le paramètre B (équation Eq.III.1 de la page 54), qui dépend de la largeur de bande effective de silicium. Un courant tunnel assisté par pièges se traduit par une plus petite valeur de B.

Ensuite, les limites de l'analyse traditionnelle du mécanisme de GIDL sont examinées: manque de précision du modèle de courant et calcul imprécis du champ électrique. Une méthodologie détaillée a été mise en place pour déterminer les conditions d'extraction appropriées: dans le cas des composants FD-SOI, l'ensemble des courbes $I_D(V_G, T)$, $I_S(V_G, T)$ et $I_G(V_G, T)$ sont utilisées pour identifier les composants, plages de tension et gammes de température pour lesquels le courant de fuite de drain est dominé par le courant GIDL et la fuite directe de grille est négligeable. Nous proposons pour l'analyse du mécanisme de GIDL une approche améliorée qui surmonte les limites de la méthode traditionnelle pour la détermination expérimentale du champ électrique.

Pour les dispositifs sur SOI 25 nm, la nouvelle méthodologie proposée montre que le courant GIDL élevé observé dans les transistors LT est dû à des défauts EOR résiduels. Par rapport aux dispositifs HT, on extrait pour B des valeur inférieures dans les composants LT (Fig. 3), ce qui indique que la largeur de bande effective est réduite en raison de l'existence de défauts EOR résiduels qui contribuent à la génération GIDL.

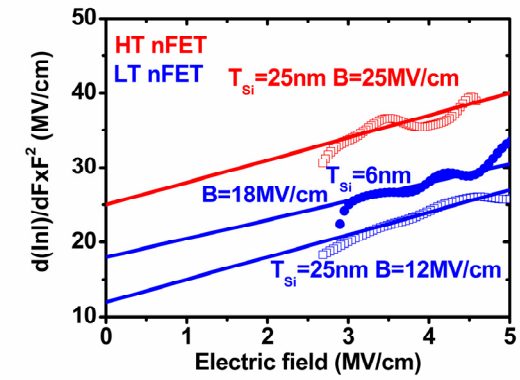


Fig.3. Extraction du paramètre B du courant GIDL pour des transistors nFETs HT et LT présentant des épaisseurs de canal (épaisseur du film SOI) différentes.

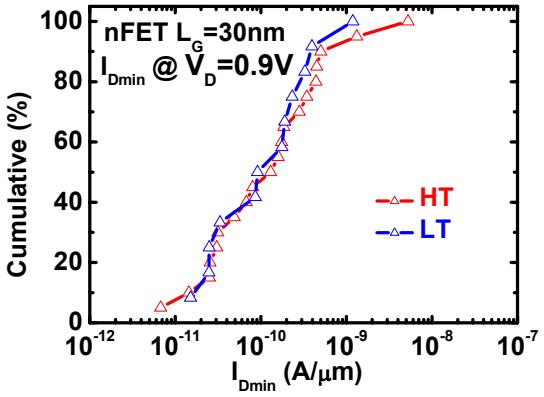


Fig.4. Fonction de répartition du courant de drain minimum I_{Dmin} pour des transistors nFETs HT et LT sur film SOI de 6 nm d'épaisseur.

Pour réduire la densité de défauts EOR et le courant de fuite GIDL des transistors activité par LT SPER, l'utilisation de films SOI extrêmement minces SOI s'avère un moyen efficace. Sur SOI très mince, l'oxyde enterré coupe une partie de la distribution des défauts ponctuels générés lors de l'implantation et joue le rôle de surface recombinante pour les défauts pendant les recuits. La densité de défauts EOR résiduels qui en résulte est significativement plus faible que sur SOI épais. De fait, sur des films SOI de 6nm d'épaisseur, il a été possible d'atteindre les même performances en termes de courant I_{Dmin} pour des NFET LT et HT (Fig.4). La valeur extraite pour le paramètre B du GIDL est compatible avec la réduction de I_{Dmin} pour ces dispositifs SPER LT sur SOI mince. En effet, la valeur de B extraite pour les dispositifs LT activés par SPER sur ETSOI (6 nm) est beaucoup plus grande que pour un SOI épais de 25 nm (Fig. 3). Cette valeur plus élevée de B est le signe d'une plus grande largeur de bande effective et d'une plus faible densité de défauts EOR sur ETSOI.

Chapitre IV: Désactivation des dopants activé par LT SPER

Dans ce chapitre, nous étudions l'activation et la stabilité thermique du bore et de l'arsenic après activation par LT SPER. Pour vérifier si l'activation LT SPER est compatible avec le schéma d'intégration 3D séquentielle, nous avons exploré la désactivation des dopants activés par LT SPER dans une gamme de température allant de 400 °C à 600 °C, plus faible que celle généralement étudiée dans la littérature, mais qui est celle pertinente pour notre technologie.

En ce qui concerne la stabilité thermique des dopants activés par LT SPER sur des échantillons SOI, nous avons obtenu les résultats suivants:

Pour le bore, on constate qu'en localisant la zone de défauts EOR aussi près que possible de l'interface Si / BOX, la désactivation du bore est bien contrôlée. On peut même observer une réactivation pour des recuits de 2 heures à des températures supérieures à 500 °C-600 °C (Fig.5). L'explication proposée est la suivante. D'une part, la densité de défauts EOR est inférieure du fait que le BOX tronque la distribution spatiale des atomes Si interstitiels. D'autre part, l'effet recombinant de l'interface Si/BOX est d'autant plus fort que cette interface est proche des défauts EOR, favorisant ainsi le flux des interstitiels vers le BOX plutôt que vers la surface supérieure de la zone dopée. Sachant que le mécanisme principal de désactivation du bore est lié à la formation d'agglomérats bore-interstitiel (BIC, pour Boron Interstitial Clusters), on comprend que cette modification de la direction du flux d'interstitiels permet de limiter la désactivation du bore, voire de le réactiver.

En revanche, l'arsenic est désactivé par la formation d'agglomérats As-lacune. De ce fait, la désactivation d'arsenic ne peut pas être réduite en diminuant la distance T_{EOR_BOX} entre défauts EOR et BOX. On observe une désactivation légèrement plus élevée pour les petits T_{EOR_BOX} (Fig.6).

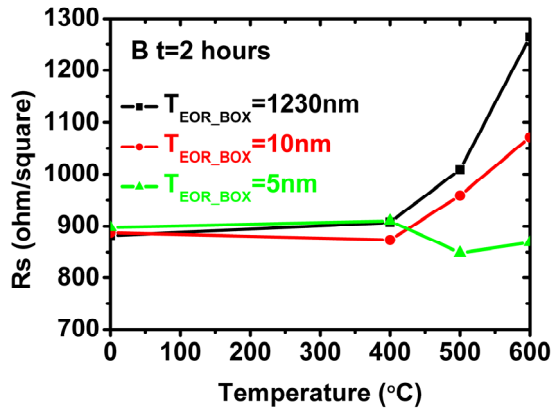


Fig.5 Résistivité (en Ω/carré) pour une jonction dopée bore, activée par SPER LT puis recuite pendant 2h à différentes températures.

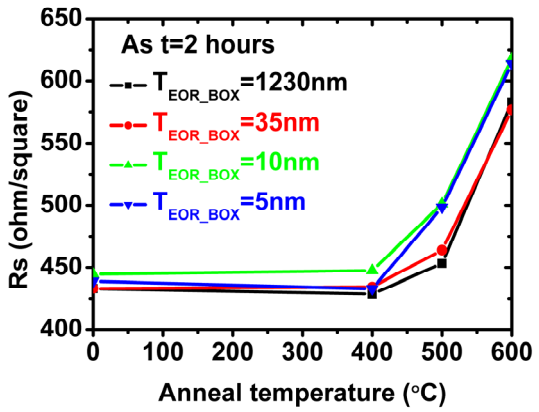


Fig.6 Résistivité (en Ω/carré) pour une jonction dopée As, activée par SPER LT puis recuite pendant 2h à différentes températures. L'abscisse à l'origine correspond à la résistivité après activation.

Dans tous les cas, tant pour le bore que pour l'arsenic, on observe que la résistance de couche mesurée pour des jonctions source/drain FD-SOI activées par SPER LT est similaire à celle obtenue par activation HT, aussi bien au début, juste après le recuit d'activation, qu'après des recuits post-activation à différentes températures entre 400°C et 600°C. En conséquence, la SPER LT semble convenir pour la fabrication des transistors FDSOI des couches inférieure et supérieure.

Chapitre V: Conclusions et perspectives

L'activation à basse température est prometteuse pour l'intégration 3D séquentielle, où le bilan thermique du transistor supérieur est limitée (<650 °C) pour ne pas dégrader le transistor inférieur, mais aussi dans le cas d'une intégration planaire afin d'atteindre des épaisseurs équivalentes d'oxyde (EOT) ultra fines et de contrôler le travail de sortie de la grille sans recourir à une intégration de type « gate-last ». Dans ce travail de thèse, l'activation par recroissance en phase solide (SPER) a été étudiée afin de réduire le bilan thermique de l'activation des dopants.

L'activation à basse température présente plusieurs inconvénients. Les travaux précédents montrent que les fuites de jonctions sont plus importantes dans ces dispositifs. Ensuite, des fortes désactivations de dopants ont été observées. Troisièmement, la faible

diffusion des dopants peut rendre difficile la connexion des jonctions source et drain avec le canal.

Nous avons montré que, dans un transistor FDSOI, l'augmentation des fuites de jonction et la désactivation du bore peuvent être évités grâce à la présence de l'oxyde enterré. De plus les conditions d'implantation ont été optimisées et les transistors activés à 650 °C atteignent les performances des transistors de référence.

Enfin, les perspectives d'optimisation que nous proposons pour la suite de ce travail concernent notamment la qualité de l'interface, l'optimisation du profil de jonction et l'utilisation d'une épitaxie de SiGe à basse température pour réaliser les source et drain surélevés.

References

[Aboy'05] M. Aboy, L. Pelaz, L. A. Marques, P. Lopez, J. Barbolla, and R. Duffy, "Atomistic analysis of the evolution of boron activation during annealing in crystalline and preamorphized silicon," *Journal of Applied Physics,* vol. 97, p. 103520, 2005.

[Aboy'06] M. Aboy, L. Pelaz, P. Lopez, L. A. Marques, R. Duffy, and V. C. Venezia, "Physical insight into boron activation and redistribution during annealing after low-temperature solid phase epitaxial regrowth," *Applied physics letters,* vol. 88, p. 191917, 2006.

[Aboy'07] M. Aboy, L. Pelaz, J. Montserrat, F. J. Bermúdez, and J. J. Hamilton, "Boron diffusion and activation in SOI and bulk Si: The role of the buried interface," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms,* vol. 257, pp. 152 - 156, 2007.

[Aboy'11] M. Aboy, L. Pelaz, E. Bruno, S. Mirabella, and S. Boninelli, "Kinetics of large B clusters in crystalline and preamorphized silicon," *Journal of Applied Physics,* vol. 110, p. 073524, 2011.

[Balestra'10] F. Balestra, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization," (London: Wiley-ISTE), 2010

[Batude'08] P. Batude, M. Vinet, A. Pouydebasque, L. Clavelier, C. LeRoyer, C. Tabone, B. Previtali, L. Sanchez, L. Baud, A. Roman, V. Carron, F. Nemouchi, S. Pocas, C. Comboroure, V. Mazzocchi, H. Grampeix, F. Aussenac, and S. Deleonibus, "Enabling 3D Monolithic Integration," *ECS Transactions,* vol. 16, pp. 47-54, 2008.

[Batude'09a] P.Batude, "Intégration à trois dimensions séquentielle :Etude, fabrication et caractérisation", *PhD thesis*, Institut National Polytechnique de Grenoble, 2009.

[Batude'09b] P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, L. Clavelier, S. Michaud, A. Valentian, O. Thomas, O. Rozeau, P. Coudrain, C. Leyris, K. Romanjek, X. Garros, L. Sanchez, L. Baud, A. Roman, V. Carron, H. Grampeix, E. Augendre, A. Toffoli, F. Allain, P. Grosgeorges, V. Mazzochi, L. Tosti, F. Andrieu, J.-M. Hartmann, D. Lafond, S. Deleonibus, and O. Faynot, "GeOI and SOI 3D monolithic cell integrations for high density applications," *Proceedings of the 2009 VLSI Technology Symposiumin*, pp. 166 -167, 2009.

[Batude'09c] P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, J.-M. Hartmann, L. Sanchez, L. Baud, V. Carron, A. Toffoli, F. Allain, V. Mazzocchi, D. Lafond, O. Thomas, O. Cueto, N. Bouzaida, D. Fleury, A. Amara, S. Deleonibus, and O. Faynot, "Advances in 3D CMOS sequential integration," *Proceedings of the 2009 International Electron Devices Meeting*, pp. 1 -4, 2009.

[Batude'11a] P. Batude, M. Vinet, C. Xu, B. Previtali, C. Tabone, C. Le Royer, L. Sanchez, L. Baud, L. Brunet, A. Toffoli, F. Allain, D. Lafond, F. Aussenac, O. Thomas, T. Poiroux, and O. Faynot, "Demonstration of low temperature 3D sequential FDSOI integration down to 50 nm gate length," *Proceedings of the 2011 VLSI Technology Symposium*, pp. 158 - 159, 2011.

[Batude'11b] P. Batude, M. Vinet, B. Previtali, C. Tabone, C. Xu, J. Mazurier, O. Weber, F. Andrieu, L. Tosti, L. Brevard, B. Sklenard, P. Coudrain, S. Bobba, H. Ben Jamaa, P. Gaillardon, A. Pouydebasque, O. Thomas, C. Le Royer, J. Hartmann, L. Sanchez, L. Baud, V. Carron, L. Clavelier, G. De Micheli, S. Deleonibus, O. Faynot, and T. Poiroux, "Advances, challenges and opportunities in 3D CMOS sequential integration," *Proceedings of the 2011 International Electron Devices Meeting*, pp. 7.3.1 -7.3.4, 2011.

[Bazizi'10] E.M. Bazizi, P.F. Fazzini, A. Pakfar, C. Tavernier, B. Vandelle, H. Kheyrandish, S. Paul, W. Lerch and F. Cristiano, "Modeling of the effect of the buried Si-SiO2 interface on transient enhanced boron diffusion in silicon on insulator," *Journal of Applied Physics,* vol 107, pp. 074503 - 074503-4, 2010.

[Ben Akkez'11] I. Ben Akkez, A. Cros, C. Fenouillet-Beranger, P. Perreau, A. Margain, F. Boeuf, F. Balestra, and G. Ghibaudo, "Characterization and modeling of capacitances in FD-SOI devices," *Proceedings of the 2011 International Conference on Ultimate Integration of Silicon (ULIS 2011)*, pp. 1 -4, 2011.

[Ben Akkez'12] I. Ben Akkez, A. Cros, C. Fenouillet-Beranger, P. Perreau, A. Margain, F. Boeuf, F. Balestra, and G. r. Ghibaudo, "Characterization and modeling of capacitances in FD-SOI devices," *Solid-State Electronics,* vol. 71, pp. 53 - 57, 2012.

[Bohr'11] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era," *Proceedings of the 2011 International Electron Devices Meeting*, pp. 1.1.1 -1.1.6, 2011.

[Bouhdada'97] A. Bouhdada, S. Bakkali, and A. Touhami, "Modelling of gate-induced drain leakage in relation to technological parameters and temperature," *Microelectronics Reliability,* vol. 37, pp. 649 - 652, 1997.

[Chan'87] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," *Proceedings of the 1987 International Electron Devices Meeting*, pp. 718 – 721, 1987.

[Chang'95] T.-E. Chang, C. Huang, and T. Wang, "Mechanisms of interface trap-induced drain leakage current in off-state n-MOSFET's," *IEEE Transactions on Electron Devices,* vol. 42, pp. 738 -743, Apr 1995.

[Chen'87] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, "Subbreakdown drain leakage current in MOSFET," *IEEE Electron Device Letters,* vol. 8, pp. 515 - 517, Nov 1987.

[Chen'89] I.-C. Chen, C. W. Teng, D. J. Coleman, and A. Nishimura, "Interface trap-enhanced gate-induced leakage current in MOSFET," *IEEE Electron Device Letters,* vol. 10, pp. 216 -218, May 1989.

[Chen'01] J.-H. Chen, S.-C. Wong, and Y.-H. Wang, "An analytic three-terminal band-to-band tunneling model on GIDL in MOSFET," *IEEE Transactions on Electron Devices,* vol. 48, pp. 1400 -1405, Jul 2001.

[Chen'07] C. K. Chen, K. Warner, D. R. W. Yost, J. M. Knecht, V. Suntharalingam, C. L. Chen, J. A. Burns, and C. L. Keast, "Scaling Three-Dimensional SOI Integrated-Circuit Technology," *Proceedings of the 2007 International SOI Conference*, pp. 87 -88, 2007.

[Christel'81] L. A. Christel, J. F. Gibbons, and T. W. Sigmon, "Displacement criterion for amorphization of silicon during ion implantation," *Journal of Applied Physics,* vol. 52, pp. 7143-7146, 1981.

[Claverie'96] A. Claverie, C. Bonafos, M. Omri, B. De Mauduit, G. Ben Assayag, A. Martinez, D. Alquier and D. Mathiot (1996). "Transient Enhanced Diffusion of Dopants in Preamorphised Si Layers," *MRS Proceedings*, vol. 438, 3, Dec 1996.

[Claverie'02] A. Claverie, F. Cristiano, B. Colombeau, E. Scheid, and B. De Mauduit, "Thermal evolution of interstitial defects in implanted silicon,". *Proceedings of the 14th International Conference on Ion Implantation Technology*, 2002, pp. 538 -543.

[Claverie'03] A. Claverie, B. Colombeau, B. De Mauduit, C. Bonafos, X. Hebras, G. Ben Assayag and F. Cristiano, "Extended defects in shallow implants,". *Appl. Phys. A,* vol. 76, pp.1025–1033, 2003.

[Colombeau'04a] B. Colombeau, A.J. Smith, N.E.B. Cowern, B.J. Pawlak, F. Cristiano, R. Duffy, A.Claverie, C.J. Ortiz, P. Pichler, E. Lampin, C. Zechner, "Current understanding and modeling of B diffusion and activation anomalies in preamorphized ultra-shallow junctions," in *Mat. Res. Soc. Symp. Proc. 810 C3.6.1*, 2004.

[Colombeau'04b] B. Colombeau, A. J. Smith, N. E. B. Cowern, W. Lerch, S. Paul, B. J. Pawlak, F. Cristiano, X. Hebras, D. Bolze, C. Ortiz, and P. Pichler, "Electrical deactivation and diffusion of boron in preamorphized ultrashallow junctions: interstitial transport and F co-implant control," *Proceedings of the 2004 International Electron Devices Meeting*, pp. 971 – 974, 2004.

[Colombeau'07] B. Colombeau, K. R. C. Mok, S. H. Yeong, F. Benistant, M. Jaraiz, and S. Chu, "Predictive Simulations and Optimization of Advanced Ultra-Shallow Junction formation for Nano-CMOS devices," *Proceedings of the 7th International Workshop on Junction Technology (IWJT 2007)*, pp. 17 -22, 2007.

[Colombeau'09] B. Colombeau, T. Thanigaivelan, E. Arevalo, T. Toh, R. Miura, and H. Ito, "Ultra-shallow Carborane molecular implant for 22-nm node p-MOSFET performance boost," *Proceedings of the 9th International Workshop on Junction Technology (IWJT 2009)*, pp. 27 -30, 2009.

[Cowern'05] N. E. B. Cowern, B. Colombeau, J. Benson, A. J. Smith, W. Lerch, S. Paul, T. Graf, F. Cristiano, X. Hebras, and D. Bolze, "Mechanisms of B deactivation control by F co-implantation," *Applied physics letters,* vol. 86, p. 101905, 2005.

[Cristiano'04] F. Cristiano, N. Cherkashin, P. Calvo, Y. Lamrani, X. Hebras, A. Claverie, W. Lerch, and S. Paul, "Thermal stability of boron electrical activation in preamorphised ultra-shallow junctions," *Materials Science and Engineering: B,* vol. 114–115, pp. 174 - 179, 2004.

[Cristiano'06] F. Cristiano, Y. Lamrani, F. Severac, M. Gavelle, S. Boninelli, N. Cherkashin, O. Marcelot, A. Claverie, W. Lerch, S. Paul, N. Cowern, "Defects evolution and dopant activation anomalies in ion implanted silicon" Nucl*ear* Instrum*ents and* Methods *in* Phys*ics* Res*earch*. B, 253, pp. 68–79, 2006.

[Cristoloveanu'95] S. Cristoloveanu and S. S. Li, "Electrical Characterization of SOI Materials and Devices," Boston, MA: Kluwer, 1995

[Csepregi'75] L. Csepregi, J. W. Mayer, and T. W. Sigmon, "Chaneling effect measurements of the recrystallization of amorphous Si layers on crystal Si," Physics Letters A, vol. 54, pp. 157 - 158, 1975.

[Czerwinski'03] A. Czerwinski, E. Simoen, A. Poyai, and C. Claeys, "Activation energy analysis as a tool for extraction and investigation of p--n junction leakage current components," *Journal of Applied Physics,* vol. 94, pp. 1218-1221, 2003.

[Duffy'04] R. Duffy, V. C. Venezia, A. Heringa, B. J. Pawlak, M. J. P. Hopstaken, G. C. J. Maas, Y. Tamminga, T. Dao, F. Roozeboom, and L. Pelaz, "Boron diffusion in amorphous silicon and the role of fluorine," *Applied physics letters,* vol. 84, pp. 4283-4285, 2004.

[Diouf'12] C. Diouf, A. Cros, P. Morin, S. Renard, X. Federspiel, M. Rafik, A. Bianchi, J. Rosa, and G. Ghibaudo, "On the understanding of the effects of high pressure deuterium and hydrogen final anneal," *Proceedings of the 13th International Conference on Ultimate Integration on Silicon (ULIS 2012)*, pp. 9 -12, 2012.

[Eaglesham'94] D. J. Eaglesham, P. A. Stolk, H.-J. Gossmann, and J. M. Poate, "Implantation and transient B diffusion in Si: The source of the interstitials," *Applied physics letters,* vol. 65, pp. 2305-2307, 1994.

[Endoh'90] T. Endoh, R. Shirota, M. Momodomi, and F. Masuoka, "An accurate model of subbreakdown due to band-to-band tunneling and some applications," *IEEE Transactions on Electron Devices,* vol. 37, pp. 290 - 296, Jan 1990.

[Eneman'09] G. Eneman, B. De Jaeger, E. Simoen, D. P. Brunco, G. Hellings, J. Mitard, K. De Meyer, M. Meuris, and M. M. Heyns, "Quantification of Drain Extension Leakage in a Scaled Bulk Germanium PMOS Technology," *IEEE Transactions on Electron Devices,* vol. 56, pp. 3115 -3122, Dec 2009.

[Fair'77] R. B. Fair, "Recent Advances in Implantation and Diffusion Modeling for the Design and Process Control of Bipolar ICs," *ECS Silicon Symposium* pp.968. 41, 1977

[Falepin'05] A. Falepin, T. Janssens, S. Severi, W. Vandervorst, S. B. Felch, V. Parihar, and A. Mayur, "Ultra shallow junctions formed by sub-melt laser annealing," Proceedings of the *13th IEEE International Conference on Advanced Thermal Processing of Semiconductors*, pp. 87-91, 2005.

[Faynot'10] O. Faynot, F. Andrieu, O. Weber, C. Fenouillet- Béranger, P. Perreau, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenouillet, J.-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, Cassé, M. , X. Garros, M.-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brevard, C. Tabone, P. Gaud, S. Barraud, T. Ernst, and S. Deleonibus, "Planar Fully depleted SOI technology: A powerful architecture for the 20nm node and beyond," *Proceedings of the 2010 International Electron Devices Meeting*, pp. 3.2.1 -3.2.4, 2010.

[Fazzini'08a] P. F. Fazzini, F. Cristiano, C. Dupré, A. Claverie, T. Ernst, and M. Gavelle, "Defect evolution after germanium preamorphization in silicon on insulator structures," *Journal of Vacuum Science \& Technology B: Microelectronics and Nanometer Structures,* vol. 26, pp. 342-346, 2008.

[Fazzini'08b] P. F. Fazzini, F. Cristiano, C. Dupré, S. Paul, T. Ernst, H. Kheyrandish, K. K. Bourdelle, and W. Lerch, "Evolution of end-of-range defects in silicon-on-insulator substrates," *Materials Science and Engineering: B*, vol. 154–155, pp. 256 - 259, 2008.

[Feng'06] J. Feng, Y. Liu, P. B. Griffin, and J. D. Plummer, "Integration of Germanium-on-Insulator and Silicon MOSFETs on a Silicon Substrate," *IEEE Electron Device Letters,* vol. 27, pp. 911 -913, Nov 2006.

[Ferri'07] M. Ferri, S. Solmi, D. Giubertoni, M. Bersani, J. J. Hamilton, M. Kah, K. Kirkby, E. J. H. Collart, and N. E. B. Cowern, "Uphill diffusion of ultralow-energy boron implants in preamorphized silicon and silicon-on-insulator," *Journal of Applied Physics,* vol. 102, p. 103707, 2007.

[Foggiato'06] J. Foggiato and W. S. Yoo, "Implementation of flash technology for ultra shallow junction formation: Challenges in process integration," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures,* vol. 24, pp. 515-520, Jan 2006.

[Ghibaudo'88] G. Ghibaudo; "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, No. 9, pp. 543-545, 1988.

[Girginoudi'08] D. Girginoudi and C. Tsiarapas, "Impact of fluorine co-implantation on B deactivation and leakage currents in low and high energy Ge preamorphised p+n shallow junctions," *Materials Science and Engineering: B,* vol. 154â€"155, pp. 268 - 274, 2008.

[Giubertoni'10] D. Giubertoni, G. Pepponi, M. A. Sahiner, S. P. Kelty, S. Gennaro, M. Bersani, M. Kah, K. J. Kirkby, R. Doherty, M. A. Foad, F. Meirer, C. Streli, J. C. Woicik, and P. Pianetta, "Deactivation of submelt laser annealed arsenic ultrashallow junctions in silicon during subsequent thermal treatment," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures,* vol. 28, pp. C1B1-C1B5, Jan 2010.

[Grenouillet'11] L. Grenouillet, S. Ponoth, N. Loubet, V. Destefanis, Y. Le Tiec, S. Mehta, A. Kumar, Q. Liu, B. Haran, K. Cheng, N. Berliner, J. Fullam, J. Kuss, G. Shahidi, O. Faynot, B. Doris, M. Vinet, "Enabling epitaxy on ultrathin implanted SOI," *Proceedings of the 2011 International Conference on Solid State Devices and Materials (SSDM),* 2011.

[Gusev'06] E. P. Gusev, V. Narayanan, and M. M. Frank, "Advanced high-k dielectric stacks with polySi and metal gates: recent progress and current challenges," *IBM J. Res. Dev.,* vol. 50, pp. 387-410, July 2006.

[Haensch'08] W. Haensch, "Why should we do 3D integration?," *Proceedings of the 45th Design Automation Conference (DAC 2008)*, pp. 674 -675, 2008.

[Hamilton'05a] J. J. Hamilton, E. J. H. Collart, B. Colombeau, M. Bersani, D. Giubertoni, J. A. Sharp, N. E. B. Cowern, and K. J. Kirkby, "Understanding the role of buried Si/SiO2 interface on dopant and defect evolution in PAI USJ," *Materials Science and Engineering: B,* vol. 124–125, pp. 215 - 218, 2005.

[Hamilton'05b] J. J. Hamilton, E. J. H. Collart, B. Colombeau, C. Jeynes, M. Bersani, D. Giubertoni, J. A. Sharp, N. E. B. Cowern, and K. J. Kirkby, "Electrical activation of solid-phase epitaxially regrown ultra-low energy boron implants in Ge preamorphised silicon and SOI," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms,* vol. 237, pp. 107 - 112, 2005.

[Hamilton'06a] J. J. Hamilton, B. Colombeau, J. A. Sharp, N. E. B. Cowern, K. J. Kirkby, E. J. H. Collart, M. Bersani, and D. Giubertoni, "Effect of buried Si/SiO2 interface on dopant and defect evolution in preamorphizing implant ultrashallow junction," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures,* vol. 24, pp. 442 -445, Jan 2006.

[Hamilton'06b] J. J. Hamilton, N. E. B. Cowern, J. A. Sharp, K. J. Kirkby, E. J. H. Collart, B. Colombeau, M. Bersani, D. Giubertoni, and A. Parisini, "Diffusion and activation of ultrashallow B implants in silicon on insulator: End-of-range defect dissolution and the buried Si/SiO2 interface," *Applied physics letters,* vol. 89, pp. 042111 -042111-3, Jul 2006.

[Hamilton'07] J. J. Hamilton, N. E. B. Cowern, K. J. Kirkby, E. J. H. Collart, M. Bersani, D. Giubertoni, S.0 Gennaro and A. Parisini, "Boron deactivation in pre-amorphised silicon-on-insulator: Efficiency of the buried oxide as an interstitial sink," *Applied Physics Letters*, vol. 91, pp.92122-92122-3, aug 2007.

[Harrison'07] S. A. Harrison, T. F. Edgar, and G. S. Hwang, "Prediction of B-Si_i-F complex formation and its role in B transient enhanced diffusion suppression and deactivation," *Journal of Applied Physics,* vol. 101, p. 066102, 2007.

[Hasan'07] M. Hasan, H. Park, J. M. Lee, M. Jo, and H. Hwang, "Band-edge metal gate materials for atomic-layer-deposited HfO2 for future CMOS technology," *Microelectronic engineering,* vol. 84, pp. 2205 - 2208, 2007.

[Haselman'10] M. Haselman and S. Hauck, "The Future of Integrated Circuits: A Survey of Nanoelectronics," *Proceedings of the IEEE,* vol. 98, pp. 11 - 38, Jan 2010.

[Huang'97] L. Huang, P. T. Lai, J. P. Xu, and Y. C. Cheng, "Mechanism analysis of gate-induced drain leakage in off-state n-MOSFET," *Proceedings of the 1997 International Electron Devices Meeting*, pp. 94 -97, 1997.

[Hurkx'92] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Transactions on Electron Devices,* vol. 39, pp. 331 -338, feb 1992.

[I-micronews] http://www.i-micronews.com/upload/Rapports/3D%20flyer.pdf

[ITRS'11] http://www.itrs.net/Links/2011ITRS/Home2011.htm

[Iyer'09] S. S. Iyer, T. Kirihata, M. R. Wordeman, J. Barth, R. H. Hannon, and R. Malik, "Process-design considerations for three dimensional memory integration," *Proceedings of the 2009 VLSI Technology Symposium*, pp. 60 -63, 2009.

[Jain'04] S. H. Jain, P. B. Griffin, J. D. Plummer, S. Mccoy, J. Gelpey, T. Selinger, and D. F. Downey, "Metastable boron active concentrations in Si using flash assisted solid phase epitaxy," *Journal of Applied Physics,* vol. 96, pp. 7357-7360, 2004.

[Jang'99] S.-A. Jang, I.-S. Yeo, and Y.-B. Kim, "Junction leakage characteristics in modified LOCOS isolation structures with a nitride spacer," *IEEE Transactions on Electron Devices,* vol. 46, pp. 145 -150, Jan 1999.

[Jeong'07] U. Jeong, Z.Y. Zhao, B.N. Guo, G. Li, and S. Mehta, "Requirements and Challenges in Ion Implanter for Sub-100nm CMOS Device Fabrication", *Proceedings of the 17th international Conference of Application of Accelerators in Research and Industry*, Denton, TX, , pp.697-700, Nov 2003.

[Jin'02] J.-Y. Jin, J. Liu, U. Jeong, S. Mehta, and K. Jones, "Study of reverse annealing behaviors of p^+/n ultrashallow junction formed using solid phase epitaxial annealing," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures,* vol. 20, pp. 422-426, Jan 2002.

[Johnson'07] B. C. Johnson and J. C. McCallum, "Dopant-enhanced solid-phase epitaxy in buried amorphous silicon layers," *Phys. Rev. B,* vol. 76, p. 045216, Jul 2007.

[Jomaah'96] J. Jomaah, G. Ghibaudo, and F. Balestra, "Band-to-band tunnelling model of gate induced drain leakage current in silicon MOS transistors," *Electronics Letters,* vol. 32, pp. 767 -769, Apr 1996.

[Jung'07] S.-M. Jung, H. Lim, C. Yeo, K. Kwak, B. Son, H. Park, J. Na, J.-J. Shim, C. Hong, and K. Kim, "High Speed and Highly Cost effective 72M bit density S3 SRAM Technology with Doubly Stacked Si Layers, Peripheral only CoSix layers and Tungsten Shunt W/L Scheme for Standalone and Embedded Memory," *Proceedings of the 2007 VLSI Technology SymposiumVLSI Technology,* pp. 82 -83, 2007.

[Jung'10] S.-M. Jung, H. Lim, K. H. Kwak, and K. Kim, "A 500-MHz DDR High-Performance 72-Mb 3-D SRAM Fabricated With Laser-Induced Epitaxial c-Si Growth Technology for a Stand-Alone and Embedded Memory Application," in *IEEE Transactions on Electron Devices*, vol. 57, pp. 474 - 481, 2010.

[Kah'08] M. Kah, A. J. Smith, J. J. Hamilton, J. Sharp, S. H. Yeong, B. Colombeau, R. Gwilliam, R. P. Webb, and K. J. Kirkby, "Interaction of the end of range defect band with the upper buried oxide interface for B and BF2 implants in Si and silicon on insulator with and without preamorphizing implant," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures,* vol. 26, pp. 347 -350, Jan 2008.

[Kane'60] E. O. Kane, "Zener tunneling in semiconductors," *Journal of Physics and Chemistry of Solids,* vol. 12, pp. 181 - 188, 1960.

[Kane'61] E. O. Kane, "Theory of Tunneling," *Journal of Applied Physics,* vol. 32, pp. 83-91, 1961.

[Keldysh'58] L. V. Keldysh, "Behavior of Non-Metallic Crystals in Strong Electric Fields," *Soviet Journal of Experimental and Theoretical Physics,* vol. 6, p. 763, 1958.

[Kentaro'07] S. Kentaro and M. Nobuhide, "Gate-Extension Overlap Control by Sb Tilt Implantation(Junction Formation and TFT Reliability, <Special Section> Fundamentals and Applications of Advanced Semiconductor Devices)," *IEICE transactions on electronics,* vol. 90, pp. 973-977, 2007.

[Khakifirooz'12] A. Khakifirooz, K. Cheng, T. Nagumo, N. Loubet, T. Adam, A. Reznicek, J. Kuss, D. Shahrjerdi, R. Sreenivasan, S. Ponoth, H. He, P. Kulkarni, Q. Liu, P. Hashemi, P. Khare, S. Luning, S. Mehta, J. Gimbert, Y. Zhu, Z. Zhu, J. Li, A. Madan, T. Levin, F. Monsieur, T. Yamamoto, S. Naczas, S. Schmitz, S. Holmes, C. Aulnette, N. Daval, W. Schwarzenbach, B.-Y. Nguyen, V. Paruchuri, M. Khare, G. Shahidi, and B. Doris, "Strain engineered extremely thin SOI (ETSOI) for high-performance CMOS," *Proceedings of the 2012 VLSI Technology Symposiumin*, pp. 117 -118, 2012.

[Khorram'12] H. R. Khorram, K. Nakano, N. Sagawa, T. Fujiwara, Y. Iriuchijima, T. Sei, T. Takahiro, K. Nakamura, K. Shiraishi, and T. Hayashi, "Cost of Ownership/Yield Enhancement of High Volume Immersion Lithography Using Topcoat-Less Resists," *IEEE Transactions on Semiconductor Manufacturing,* vol. 25, pp. 63 -71, Feb 2012.

[Kim'00] N.-S. Kim, I.-G. Kim, S.-H. Ok, D.-C. Kim, S.-J. Choi, J.-H. Choi, H.-Y. Kwen, D.-Y. Park, and J.-B. Kim, "Optimization of n-junction through ion beam shadowing and buffering effect by tilt implantation with rotation for improving the retention time," Proceeding of the international conference on Ion Implantation Technology, pp. 50 -53, 2000.

[Knickerbocker'08] J.U. Knickerbocker, P.S. Andry, B. Dang, R.R. Horton, C.S. Patel, R.J. Polastre, K. Sakuma, E.S. Sprogis, C.K. Tsang, B.C. Webb, S.L. Wright, "3D silicon integration," Proceedings of 58th Electronic Components and Technology Conference, pp. 538–543, 2008.

[Kong'08] N. Kong, T. A. Kirichenko, Y. Kim, M. C. Foisy, and S. K. Banerjee, "Physically based kinetic Monte Carlo modeling of arsenic-interstitial interaction and arsenic uphill diffusion during ultrashallow junction formation," *Journal of Applied Physics,* vol. 104, p. 013514, 2008.

[Koyanagi'09] M. Koyanagi, "New 3D integration technology and 3D system LSIs," *Proceedings of the 2009 VLSI Technology Symposium*, pp. 64 -67, 2009.

[Kuhn'11] K. J. Kuhn, M. D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S. T. Ma, A. Maheshwari, and S. Mudanai, "Process Technology Variation," *IEEE Transactions on Electron Devices,* vol. 58, pp. 2197 -2208, Aug 2011.

[Kuhn'12] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Transactions on Electron Devices,* vol. 59, pp. 1813 -1828, July 2012.

[Kumar'01] M. Kumar, H. Liu, J. K. O. Sin, J. Wan, and K. L. Wang, "A 3-D BiCMOS technology using selective epitaxial growth (SEG) and lateral solid phase epitaxy (LSPE)," *Proceedings of the 2001 International Electron Devices Meeting*, pp. 33.2.1 -33.2.4, 2001.

[Lacord'12] J. Lacord, G. Ghibaudo, and F. Boeuf, "Comprehensive and Accurate Parasitic Capacitance Models for Two- and Three-Dimensional CMOS Device Structures," *IEEE Transactions on Electron Devices,* vol. 59, pp. 1332 -1344, May 2012.

[Lerch'05] W. Lerch, S. Paul, J. Niess, F. Cristiano, Y. Lamrani, P. Calvo, N. Cherkashin, D. Downey, and E. Arevalo, "Deactivation of solid phase epitaxy-activated boron ultrashallow junctions," *Journal of the Electrochemical Society,* vol.152, pp. G787-G793, 2005.

[Lietoila'80] A. Lietoila, J. F. Gibbons, and T. W. Sigmon, "The solid solubility and thermal behavior of metastable concentrations of As in Si," *Applied physics letters,* vol. 36, pp. 765-768, 1980.

[Lietoila'81] A. Lietoila, R. B. Gold, J. F. Gibbons, T. W. Sigmon, P. D. Scovell, and J. M. Young, "Metastable As-concentrations in Si achieved by ion implantation and rapid thermal annealing," *Journal of Applied Physics,* vol. 52, pp. 230-232, 1981.

[Lin'01] C.-H. Lin, B.-C. Hsu, M. H. Lee, and C. W. Liu, "A comprehensive study of inversion current in MOS tunneling diodes," *IEEE Transactions on Electron Devices,* vol. 48, pp. 2125 -2130, Sep 2001.

[Lindsay'04a] R. Lindsay, K. Henson, W. Vandervorst, K. Maex, B. J. Pawlak, R. Duffy, R. Surdeanu, P. Stolk, J. A. Kittl, S. Giangrandi, X. Pages, and K. van der Jeugd, "Leakage optimization of ultra-shallow junctions formed by solid phase epitaxial regrowth," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 22, pp. 306-311, 2004.

[Lindsay'04b] R. Lindsay, S. Severi, B. J. Pawlak, K. Henson, A. Lauwers, X. Pages, A. Satta, R. Surdeanu, H. Lendzian, and K. Maex, "SPER junction optimisation in 45 nm CMOS devices," *Proceedings of the 4th International Workshop on Junction Technology (IWJT 2004)*, pp. 70 – 75, 2004.

[Lu'09] J.-Q. Lu, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems," *Proceedings of the IEEE,* vol. 97, pp. 18 -30, Jan. 2009.

[MacKenzie'07] M. MacKenzie, A. Craven, D. McComb, S. D. Gendt, F. Docherty, C. McGilvery, and S. McFadzean, "Advanced nanoanalysis of a Hf-based high-k dielectric stack prior to activation," *Electrochemical and Solid State Letters,* vol. 10, pp. G33-G35, 2007.

[Martinez-Limia'08] A. Martinez-Limia, P. Pichler, W. Lerch, S. Paul, H. Kheyrandish, A. Pakfar, and C. Tavernier, "Experimental investigations and simulation of the deactivation of arsenic during thermal processes after activation by SPER and spike annealing," in *Mat. Res. Soc. Symp. Proc.,* pp.211-215, 2008.

[Maszara'05] W. P. Maszara, "Fully Silicided Metal Gates for High-Performance CMOS Technology: A Review," *Journal of The Electrochemical Society,* vol. 152, pp. G550-G555, 2005.

[Mazurier'11] J. Mazurier, O. Weber, F. Andrieu, F. Allain, L. Tosti, L. Brevard, O. Rozeau, M.-A. Jaud, P. Perreau, C. Fenouillet-Beranger, F. A. Khaja, B. Colombeau, G. De Cock, G. Ghibaudo, M. Belleville, O. Faynot, and T. Poiroux, "Drain current variability and MOSFET parameters correlations in planar FDSOI technology," *Proceedings of the 2011 International Electron Devices Meeting*, pp. 25.5.1 -25.5.4, 2011.

[McCallum'99] J. C. McCallum, "The kinetics of dopant-enhanced solid phase epitaxy in H-free amorphous silicon layers," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms,* vol. 148, pp. 350 - 354, 1999.

[Mercha'10] A. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos, N. Minas, S. Domae, D. Perry, M. Choi, A. Redolfi, C. Okoro, Y. Yang, J. Van Olmen, S. Thangaraju, D. S. Tezcan, P. Soussan, J. H. Cho, A. Yakovlev, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k / metal gate CMOS performance," Proceedings of the 2010 International Electron Devices Meeting, pp. 2.2.1 -2.2.4, 2010.

[Michel'87] A. E. Michel, W. Rausch, P. A. Ronsheim, and R. H. Kastl, "Rapid annealing and the anomalous diffusion of ion implanted boron into silicon," *Applied physics letters,* vol. 50, pp. 416-418, 1987.

[Mok'07] K. R. C. Mok, B. Colombeau, F. Benistant, R. S. Teo, S. H. Yeong, B. Yang, M. Jaraiz, and S.-F. S. Chu, "Predictive Simulation of Advanced Nano-CMOS Devices Based on kMC Process Simulation," *IEEE Transactions on Electron Devices,* vol. 54, pp. 2155 -2163, Sept. 2007.

[Mokhberi'02] A. Mokhberi, L. Pelaz, M. Aboy, L. Marques, J. Barbolla, E. Paton, S. McCoy, J. Ross, K. Elliott, J. Gelpey, P. B. Griffin, and J. D. Plummer, "A physics based approach to ultra-shallow p+-junction formation at the 32 nm node," *Proceedings of the 2002 International Electron Devices Meeting*, pp. 879 – 882, 2002.

[Monolithic3d] http://www.monolithic3d.com/2/post/2012/01/fine-grain-3d-integration-why-how.html

[Moore'65] G. E. Moore, "Cramming More Components Onto Integrated Circuits"; *Electronics Magazine*; Vol. 38, No. 8, pp. 114-117; 1965

[Mourrain'00] C. Mourrain, B. Cretu, G. Ghibaudo, and P. Cottin, "New method for parameter extraction in deep sub-micrometer MOSFETs," *Proceedings of 2000 International. Conference on Microelectronic Test Structure (ICMTS 2000)*, Kobe, Japan, 2000, pp.181–186.

[Nastasi'96] M.Nastasi, J.Mayer, and J.Hivonen , Cambridge Solid State Science Series: Ion-Solid Interactions, 1996.

[Nishikawa'09] M. Nishikawa, K. Okabe, K. Ikeda, N. Tamura, H. Maekawa, M. Umeyama, H. Kurata, M. Kase, and K. Hashimoto, "Successful integration scheme of cost effective dual embedded stressor featuring carbon implant and solid phase epitaxy for high performance CMOS," *Proceedings of the 2009 International Symposium on VLSI Technology, Systems and Applications*, pp. 26 -27, 2009.

[Nobili'99] D. Nobili, S. Solmi, M. Merli, and J. Shao, "Deactivation Kinetics in Heavily Arsenic-Doped Silicon," *Journal of The Electrochemical Society,* vol. 146, pp. 4246-4252, 1999.

[Olson'88] G. L. Olson and J. A. Roth, "Kinetics of solid phase crystallization in amorphous silicon," *Materials Science Reports,* vol. 3, pp. 1 - 77, 1988.

[Park'05] H. Park, M. S. Rahman, M. Chang, B. B. Lee, M. Gardner, C. D. Young, and H. Hwang, "Effect of high pressure deuterium annealing on electrical and reliability characteristics of MOSFETs with high-k gate dielectric," *Proceeding of the 43rd International Reliability Physics Symposium*, pp. 646 – 647, 2005.

[Pawlak'04a] B. J. Pawlak, R. Lindsay, R. Surdeanu, B. Dieu, L. Geenen, I. Hoflijk, O. Richard, R. Duffy, T. Clarysse, B. Brijs, W. Vandervorst, and C. J. J. Dachs, "Chemical and electrical dopants profile evolution during solid phase epitaxial regrowth," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 22, pp. 297-301, 2004.

[Pawlak'04b] B. J. Pawlak, R. Surdeanu, B. Colombeau, A. J. Smith, N. E. B. Cowern, R. Lindsay, W. Vandervorst, B. Brijs, O. Richard, and F. Cristiano, "Evidence on the mechanism of boron deactivation in Ge-preamorphized ultrashallow junctions," *Applied physics letters,* vol. 84, pp. 2055 -2057, mar 2004.

[Pelaz'04] L. Pelaz, L.A. Marqués and J. Barbolla, "Ion-beam-induced amorphization and recrystallization in silicon", *Journal of Applied Physics*, vol. 96, pp. 5947-5976, 2004.

[Pelaz'09] L. Pelaz, L.A. Marqués, M. Aboy, P. López, and I. Santos, "Front-end process modeling in silicon," *The European Physical Journal B - Condensed Matter and Complex Systems,* vol. 72, pp. 323-359, 2009.

[Pichler'08] P. Pichler, A. Martinez-Limia, C. Kampen, A. Burenkov, J. Schermer, S. Paul, W. Lerch, J. Gelpey, S. McCoy, H. Kheyrandish, A. Pakfar, C. Tavernier, and D. Bolze, "Process models for advanced annealing schemes and their use in device simulation," *Proceedings of the 8th International Workshop on Junction Technology (IWJT 2008)*, pp. 120 - 125, 2008.

[Pinacho'05] R. Pinacho, M. Jaraiz, P. Castrillo, I. Martin-Bragado, J. E. Rubio, and J. Barbolla, "Modeling arsenic deactivation through arsenic-vacancy clusters using an atomistic kinetic Monte Carlo approach," *Applied physics letters,* vol. 86, pp. 252103 -252103-3, jun 2005.

[Planes'12] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P.-O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Beranger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M.-A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, and M. Haond, "28nm FDSOI technology platform for high-speed low-voltage digital applications," *Proceedings of the 2012 VLSI Technology Symposium,* pp. 133 -134, 2012.

[Posselt'94] M. Posselt, "CRYSTAL-TRIM AND ITS APPLICATION TO INVESTIGATIONS ON CHANNELING EFFECTS DURING ION-IMPLANTATION," *Radiation Effects and Defects in Solids*,Vol. 130-131, pp. 87-119, 1994.

[Rafhay'12] Q. Rafhay, C. Xu, P. Batude, M. Mouis, M. Vinet, and G. Ghibaudo, "Revisited approach for the characterization of Gate Induced Drain Leakage," *Solid-State Electronics,* vol. 71, pp. 37 - 41, 2012.

[Ragnarsson'06] L.-A. Ragnarsson, S. Severi, L. Trojman, K. D. Johnson, D. P. Brunco, M. Aoulaiche, M. Houssa, T. Kauerauf, R. Degraeve, A. Delabie, V. S. Kaushik, S. De Gendt, W. Tsai, G. Groeseneken, K. D. Meyer, and M. Heyns, "Electrical characteristics of 8-/spl Aring/ EOT HfO/sub 2//TaN low thermal-budget n-channel FETs with solid-phase epitaxially regrown junctions," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1657 -1668, July 2006.

[Rideau'10] D. Rideau, V. Quenette, D. Garetto, E. Dornel, M. Weybright, J. P. Manceau, O. Saxod, C. Tavernier, and H. Jaouen, "Characterization & Modeling of Gate-Induced-Drain-Leakage with complete overlap and fringing model," *Proceedings of 2010 International Conference on Microelectronic Test Structures*, March 22-25, Hiroshima, Japan. pp. 210 -213, March.2010.

[Romanjek'04] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Improved split C-V method for effective mobility extraction in sub-0.1 μm Si MOSFETs," *IEEE Electron Device Letters,* vol. 25, pp. 583 - 585, Aug 2004.

[Rosar'00] M. Rosar, B. Leroy, and G. Schweeger, "A new model for the description of gate voltage and temperature dependence of gate induced drain leakage (GIDL) in the low electric field region [DRAMs]," *IEEE Transactions on Electron Devices,* vol. 47, pp. 154 -159, Jan 2000.

[Rousseau'98] P. M. Rousseau, P. B. Griffin, W. T. Fang, and J. D. Plummer, "Arsenic deactivation enhanced diffusion: A time, temperature, and concentration study," *Journal of Applied Physics,* vol. 84, pp. 3593-3601, 1998.

[Roy'03] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE,* vol. 91, pp. 305 - 327, Feb 2003.

[Ryu'12] S.-K. Ryu, K.-H. Lu, T. Jiang, J.-H. Im, R. Huang, and P. S. Ho, "Effect of Thermal Stresses on Carrier Mobility and Keep-Out Zone Around Through-Silicon Vias for 3-D Integration," *IEEE Transactions on Device and Materials Reliability,* vol. 12, pp. 255 -262, June 2012.

[Saavedra'02] A. F. Saavedra, J. Frazer, K. S. Jones, I. Avci, S. K. Earles, M. E. Law, and E. C. Jones, "Influence of the surface Si/buried oxide interface on extended defect evolution in silicon-on-insulator scaled to 300 Å," *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures,* vol. 20, pp. 2243 -2247, Nov 2002.

[Saino'00] K. Saino, S. Horiba, S. Uchiyama, Y. Takaishi, M. Takenaka, T. Uchida, Y. Takada, K. Koyama, H. Miyake, and C. Hu, "Impact of gate-induced drain leakage current on the tail distribution of DRAM data retention time," *Proceedings of the 2000 International Electron Devices Meeting*, pp. 837 -840, 2000.

[Schenk'93] A. Schenk, "Rigorous theory and simplified model of the band-to-band tunneling in silicon," *Solid-State Electronics,* vol. 36, pp. 19 - 34, 1993.

[Schwierz'10] F. Schwierz, "Graphene transistors," *Nature Nanotechnology*, pp. 487 - 496. may 2010.

[Shibahara'07] K. Shibahara and N. Maeda, "Gate-Extension Overlap Control by Sb Tilt Implantation," IEICE TRANSACTIONS on Electronics, Vol.E90-C No.5 pp.973-977, 2007.

[Skarlatos'07] D. Skarlatos and C. Tsamis, "Modeling of low energy-high dose arsenic diffusion in silicon in the presence of clustering-induced interstitial generation," *Journal of Applied Physics,* vol. 102, p. 043532, 2007.

[Sklénard'12] B. Sklénard, C. Xu, P. Batude, B. Previtali, C. Tabone, Q. Rafhay, B. Colombeau, F.-A. Khaja, Martín-Bragado, J. Berthoz, F. Allain, A. Toffoli, R. Kies, M.-A. Jaud, P. Rivallin, S. Cristoloveanu, C. Tavernier, O. Faynot and T. Poiroux, "FDSOI devices: a solution to achieve low junction leakage with low temperature processes (≤ 650ºC)", *Proceedings of the 2012 International Conference on Ultimate Integration of Silicon (ULIS 2012)*, pp.169-172, 2012

[Skotnicki'11] T. Skotnicki, "Competitive SOC with UTBB SOI". SOI Conference (SOI), 2011 IEEE International, pp. 1-61,2011.

[Solmi'02] S. Solmi, M. Attari, and D. Nobili, "Effect of vacancy and interstitial excess on the deactivation kinetics of As in Si," *Applied physics letters,* vol. 80, pp. 4774-4776, 2002.

[Steen'07] S. E. Steen, D. LaTulipe, A. W. Topol, D. J. Frank, K. Belote, and D. Posillico, "Overlay as the key to drive wafer scale 3D integration," *Microelectronic engineering,* vol. 84, pp. 1412 - 1415, 2007.

[Stolk'97] P. A. Stolk, H.-J. Gossmann, D. J. Eaglesham, D. C. Jacobson, C. S. Rafferty, G. H. Gilmer, M. Jaraiz, J. M. Poate, H. S. Luftman, and T. E. Haynes, "Physical mechanisms of transient enhanced dopant diffusion in ion-implanted silicon," *Journal of Applied Physics,* vol. 81, pp. 6031 - 6050, may 1997.

[Suni'82] I. Suni, G. Göltz, M.-A. Nicolet, and S. S. Lau, "Effects of electrically active impurities on the epitaxial regrowth rate of amorphized silicon and germanium," *Thin Solid Films,* vol. 93, pp. 171 - 178, 1982.

[Tanaka'94] S. Tanaka, "A unified theory of direct and indirect interband tunneling under a nonuniform electric field," *Solid-State Electronics,* vol. 37, pp. 1543 - 1552, 1994.

[Tiemann'63] J. J. Tiemann and H. Fritzsche, "Temperature Dependence of Indirect Interband Tunneling in Germanium," *Phys. Rev.,* vol. 132, pp. 2506-2514, Dec 1963.

[Topol'05] A. W. Topol, D. C. La Tulipe, L. Shi, S. M. Alam, D. J. Frank, S. E. Steen, J. Vichiconti, D. Posillico, M. Cobb, S. Medd, J. Patel, S. Goma, D. DiMilia, M. T. Robson, E. Duch, M. Farinelli, C. Wang, R. A. Conti, D. M. Canaperi, L. Deligianni, A. Kumar, K. T. Kwietniak, C. D'Emic, J. Ott, A. M. Young, K. W. Guarini, and M. Ieong, "Enabling SOI-based assembly technology for three-dimensional (3d) integrated circuits (ICs)," *Proceedings of the 2005 International Electron Devices Meeting*, pp. 352 -355, 2005.

[Tsamis'05] C. Tsamis, D. Skarlatos, G. BenAssayag, A. Claverie, W. Lerch, and V. Valamontes, "Interstitial injection in silicon after high-dose, low-energy arsenic implantation and annealing," *Applied physics letters,* vol. 87, p. 201903, 2005.

[Veloso'11] A. Veloso, L.-A. Ragnarsson, M. J. Cho, K. Devriendt, K. Kellens, F. Sebaai, S. Suhard, S. Brus, Y. Crabbe, T. Schram, E. Rohr, V. Paraschiv, G. Eneman, T. Kauerauf, M. Dehan, S.-H. Hong, S. Yamaguchi, S. Takeoka, Y. Higuchi, H. Tielens, A. Van Ammel, P. Favia, H. Bender, A. Franquet, T. Conard, X. Li, K.-L. Pey, H. Struyf, P. Mertens, P. P. Absil, N. Horiguchi, and T. Hoffmann, "Gate-last vs. gate-first technology for aggressively scaled EOT logic/RF CMOS," *Proceedings of the 2011 VLSI Technology Symposium*, pp. 34 -35, 2011.

[Vick'69] G. L. Vick and K. M. Whittle, "Solid Solubility and Diffusion Coefficients of Boron in Silicon," *Journal of The Electrochemical Society,* vol. 116, 1969.

[Vinet'11] M. Vinet, P. Batude, C. Tabone, B. Previtali, C. LeRoyer, A. Pouydebasque, L. Clavelier, A. Valentian, O. Thomas, S. Michaud, L. Sanchez, L. Baud, A. Roman, V. Carron, F. Nemouchi, V. Mazzocchi, H. Grampeix, A. Amara, S. Deleonibus, and O. Faynot, "3D monolithic integration: Technological challenges and electrical results," *Microelectronic engineering,* vol. 88, pp. 331 - 335, 2011.

[Wang'98] T. Wang, C. F. Hsu, L. P. Chiang, N. K. Zous, T. S. Chao, and C. Y. Chang, "Voltage scaling and temperature effects on drain leakage current degradation in a hot carrier stressed n-MOSFET," *Proceedings of the 36th International Reliability Physics Symposium,* 1998, pp. 209 - 212, 1998.

[Weber'06] A. Weber, A. Birner, and W. Krautschneider, "Retention Tail Improvement for Gbit DRAMs through Trap Passivation confirmed by Activation Energy Analysis," *Proceedings of the 36st European Solid-State Device Research Conference (ESSDERC 2006)*, pp. 250-253, 2006.

[Wen'05] H.-C. Wen, K. Choi, P. Majhi, H. Alshareef, C. Huffman, and B. H. Lee, "A systematic study of the influence of nitrogen in tuning the effective work function of nitrided metal gates," *Proceedings of the 2005 International Symposium on VLSI Technology, Systems and Applicationsin*, pp. 105 – 106, 2005.

[Witters'11] L. Witters, J. Mitard, A. Veloso, A. Hikavyy, J. Franco, T. Kauerauf, M. Cho, T. Schram, F. Sebai, S. Yamaguchi, S. Takeoka, M. Fukuda, W.-E. Wang, B. Duriez, G. Eneman, R. Loo, K. Kellens, H. Tielens, P. Favia, E. Rohr, G. Hellings, H. Bender, P. Roussel, Y. Crabbe, S. Brus, G. Mannaert, S. Kubicek, K. Devriendt, K. De Meyer, L.-A. Ragnarsson, A. Steegen, and N. Horiguchi, "Dual-channel technology with cap-free single metal gate for high performance CMOS in gate-first and gate-last integration," *Proceedings of the 2011 International Electron Devices Meeting*, pp. 28.6.1 -28.6.4, 2011.

[Wolf'08] M. J. Wolf, P. Ramm, A. Klumpp, and H. Reichl, "Technologies for 3D wafer level heterogeneous integration," in *Design, Test, Integration and Packaging of MEMS/MOEMS, 2008. MEMS/MOEMS 2008. Symposium on*, 2008, pp. 123 -126.

[Xu'10] C. Xu, P. Batude, C. Rauer, C. Le Royer, L. Hutin, A. Pouydebasque, B. Previtali, M. Mouis, and M. Vinet, "Ion-Ioff performance analysis of FDSOI MOSFETs with low processing temperature," *Proceedings of the 2010 International Conference on Solid State Devices and Materials (SSDM)*, Tokyo, Japan, p. 01-02, 2010.

[Yang'08] J.-H. Yang, G.-F. Li, and H.-L. Liu, "Off-state leakage current in nano-scale MOSFET with Hf-based gate dielectrics," *Proceeding of the 2nd International Nanoelectronics Conference (INEC 2008)*, pp. 1189 -1192.

[Yoshinaga'10] T. Yoshinaga, M. Nomura, "Trends in R&D in TSV Technology for 3D LSI packaging", *QUARTERLY REVIEW*, pp. 26-39, No. 3 7; 2 0 1 0

[Young'11] T. Young, H. Yin, Q. Xu, C. Zhao, J. F. Li, and D. Chen, "Dummy Poly Silicon Gate Removal by Wet Chemical Etching," *ECS Transactions,* vol. 34, pp. 361-364, 2011.

[Yuan'08] X. Yuan, J.-E. Park, J. Wang, E. Zhao, D. C. Ahlgren, T. Hook, J. Yuan, V. Chan, H. Shang, C.-H. Liang, R. Lindsay, S. Park, and H. Choo, "Gate-Induced-Drain-Leakage Current in 45-nm CMOS Technology," *IEEE Transactions on Device and Materials Reliability,* vol. 8, pp. 501 - 508, sept. 2008.

[Ziegler'98] J. F. Ziegler, "Ion Implantation: Science and Technology," Boston Academic Press, 2nd Edition, 1998.

Publications

[1] **C. Xu**, P. Batude, C. Rauer, C. Le Royer, L. Hutin, A. Pouydebasque, B. Previtali, M. Mouis, and M. Vinet, "Ion-Ioff performance analysis of FDSOI MOSFETs with low processing temperature," *Proceedings of the 2010 International Conference on Solid State Devices and Materials (SSDM)*, Tokyo, Japan, pp. 01 -02, 2010.

[2] **C. Xu**, P. Batude, K. Romanjek, C. Le Royer, C. Tabone, B. Previtali, M. Jaud, X. Garros, M. Vinet, T. Poiroux, Q. Rafhay, and M. Mouis, "Improved extraction of GIDL in FDSOI devices for proper junction quality analysis," *Proceedings of the 41st European Solid-State Device Research Conference (ESSDERC 2011)*, pp. 267 -270, 2011.

[3] **C. Xu**, P. Batude, B. Sklenard, M. Vinet, M. Mouis, B. Previtali, F. Y. Liu, J. Guerrero, K. Yckache, P. Rivallin, V. Mazzocchi, S. Cristoloveanu, O. Faynot, and T. Poiroux, "FDSOI: A solution to suppress boron deactivation in low temperature processed devices," *Proceedings of the 12th International Workshop on Junction Technology (IWJT 2012)*, pp. 69 -72, 2012.

[4] **C. Xu**, P. Batude, M. Vinet, M. Mouis, M. Casse, B. Sklenard, B. Colombeau, Q. Rafhay, C. Tabone, J. Berthoz, B. Previtali, J. Mazurier, L. Brunet, L. Brevard, F. A. Khaja, J. Hartmann, F. Allain, A. Toffoli, R. Kies, C. Le Royer, S. Morvan, A. Pouydebasque, X. Garros, A. Pakfar, C. Tavernier, O. Faynot, and T. Poiroux, "Improvements in Low Temperature (<625°C) FDSOI Devices down to 30nm gate length," *Proceedings of the 2012 International Symposium on VLSI Technology, Systems and Applications*, pp. 1 -2, april.2012.

[5] Q. Rafhay, **C. Xu**, P. Batude, M. Mouis, M. Vinet, and G. Ghibaudo, "Revisited approach for the characterization of Gate Induced Drain Leakage," *Solid-State Electronics*, vol. 71, pp. 37 - 41, 2012.

[6] B. Sklénard, **C. Xu**, P. Batude, B. Previtali, C. Tabone, Q. Rafhay, B. Colombeau, F.-A. Khaja, Martín-Bragado, J. Berthoz, F. Allain, A. Toffoli, R. Kies, M.-A. Jaud, P. Rivallin, S. Cristoloveanu, C. Tavernier, O. Faynot and T. Poiroux, "FDSOI devices: a solution to achieve low junction leakage with low temperature processes (≤ 650ºC)", *Proceedings of the 2012 International Conference on Ultimate Integration of Silicon (ULIS 2012)*, pp.169-172, 2012

[7] P. Batude, M. Vinet, **C. Xu**, B. Previtali, C. Tabone, C. Le Royer, L. Sanchez, L. Baud, L. Brunet, A. Toffoli, F. Allain, D. Lafond, F. Aussenac, O. Thomas, T. Poiroux, and O. Faynot, "Demonstration of low temperature 3D sequential FDSOI integration down to 50 nm gate length," *Proceedings of the 2011 VLSI Technology Symposiumin*, pp. 158 -159, 2011.

[8] P. Batude, M. Vinet, B. Previtali, C. Tabone, **C. Xu**, J. Mazurier, O. Weber, F. Andrieu, L. Tosti, L. Brevard, B. Sklenard, P. Coudrain, S. Bobba, H. Ben Jamaa, P. Gaillardon, A. Pouydebasque, O. Thomas, C. Le Royer, J. Hartmann, L. Sanchez, L. Baud, V. Carron, L. Clavelier, G. De Micheli, S. Deleonibus, O. Faynot, and T. Poiroux, "Advances, challenges and opportunities in 3D CMOS sequential integration," *Proceedings of the 2011 International Electron Devices Meeting*, pp. 7.3.1 -7.3.4, 2011.

[9] L. Hutin, M. Cassé, C. Le Royer, J.-F. Damlencourt, A. Pouydebasque, **C. Xu**, C. Tabone, J.-M. Hartmann, V. Carron, H. Grampeix, V. Mazzocchi, R. Truche, O. Weber, P. Batude, X. Garros, L. Clavelier, M. Vinet, and O. Faynot, "20nm Gate Length Trigate pFETs on Strained SGOI for High Performance CMOS", *Proceedings of the 2010 VLSI Technology Symposiumin*, pp.37-38, 2010.