Développement de nouveaux procédés d'isolation électrique par anodisation localisée du silicium

Ahmed Garbi

To cite this version:

Ahmed Garbi. Développement de nouveaux procédés d'isolation électrique par anodisation localisée du silicium. Autre. INSA de Lyon, 2011. Français. NNT : 2011ISAL0072 . tel-00694394

HAL Id: tel-00694394
https://theses.hal.science/tel-00694394

Submitted on 4 May 2012

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

No d'ordre: 2011-ISAL-0072 Année 2011

THESE

Présentée devant

L'INSTITUT NATIONAL DES SCIENCES APPLIQUEES DE LYON

Pour obtenir le grade de

DOCTEUR

ECOLE DOCTORALE : Electronique, Electrotechnique, Automatique (EEA)
SPECIALITE : Dispositifs de l'Electronique Intégrée

Par

Ahmed GHARBI

Développement de nouveaux procédés d'isolation électrique par anodisation localisée du silicium

Soutenue le 08 juillet 2011 devant la Commission d'Examen

BARBIER Daniel	Professeur, INSA de Lyon	Président du jury
NASSIOPOULOU Androula	Directeur de recherche, IMEL, Grèce	Rapporteur
VENTURA Laurent	Professeur, Université de Tours	Rapporteur
HALIMAOUI Aomar	Ingénieur STMicroelectronics	Examinateur
SOUIFI Abdelkader	Professeur, INSA de Lyon	Directeur de thèse
REMAKI Boudjemaa	Maître de conférence–HDR, Univ. Lyon 1	Directeur de thèse

Cette thèse a été préparée à l'Institut des Nanotechnologies de Lyon (INL)
Cofinancement CNRS-STMicroelectronics

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Order No.: 2011-ISAL-0072 Year 2011

THESIS

Submitted to

NATIONAL INSTITUTE OF APPLIED SCIENCE OF LYON

For the degree of

PhD DOCTOR

DOCTORAL SCHOOL: Electronique, Electrotechnique, Automatique (EEA)
SPECIALITY: Integrated Electronic Devices

By

Ahmed GHARBI

Development of a new process for electrical isolation of ULSI CMOS circuits based on local anodization of silicon

Defended on July 8th, 2011

BARBIER Daniel	Professor, INSA Lyon	President
NASSIOPOULOU Androula	Research Director, IMEL, Greece	Reporter
VENTURA Laurent	Professor, University of Tours	Reporter
HALIMAOUI Aomar	Engineer STMicroelectronics	Examiner
SOUIFI Abdelkader	Professor, INSA Lyon	Director of thesis
REMAKI Boudjemaa	Assistant Professor–HDR, Univ. Lyon 1	Director of thesis

This project has been performed at the Lyon Institute of Nanotechnology (INL)
in the frame of CNRS/STMicroelectronics partnership

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

SIGLE	ECOLE DOCTORALE	NOM ET COORDONNEES DU RESPONSABLE
CHIMIE	**CHIMIE DE LYON** **http://www.edchimie-lyon.fr** Insa : R. GOURDON	M. Jean Marc LANCELIN Université de Lyon – Collège Doctoral Bât ESCPE 43 bd du 11 novembre 1918 69622 VILLEURBANNE Cedex Tél : 04.72.43 13 95 directeur@edchimie-lyon.fr
E.E.A.	**ELECTRONIQUE, ELECTROTECHNIQUE, AUTOMATIQUE** **http://edeea.ec-lyon.fr** Secrétariat : M.C. HAVGOUDOUKIAN eea@ec-lyon.fr	M. Gérard SCORLETTI Ecole Centrale de Lyon 36 avenue Guy de Collongue 69134 ECULLY Tél : 04.72.18 60 97 Fax : 04 78 43 37 17 Gerard.scorletti@ec-lyon.fr
E2M2	**EVOLUTION, ECOSYSTEME, MICROBIOLOGIE, MODELISATION** **http://e2m2.universite-lyon.fr** Insa : H. CHARLES	Mme Gudrun BORNETTE CNRS UMR 5023 LEHNA Université Claude Bernard Lyon 1 Bât Forel 43 bd du 11 novembre 1918 69622 VILLEURBANNE Cédex Tél : 04.72.43.12.94 e2m2@biomserv.univ-lyon1.fr
EDISS	**INTERDISCIPLINAIRE SCIENCES-SANTE** **http://ww2.ibcp.fr/ediss** Sec : Safia AIT CHALAL Insa : M. LAGARDE	M. Didier REVEL Hôpital Louis Pradel Bâtiment Central 28 Avenue Doyen Lépine 69677 BRON Tél : 04.72.68 49 09 Fax :04 72 35 49 16 Didier.revel@creatis.uni-lyon1.fr
INFOMATHS	**INFORMATIQUE ET MATHEMATIQUES** http://infomaths.univ-lyon1.fr	M. Johannes KELLENDONK Université Claude Bernard Lyon 1 LIRIS - INFOMATHS Bâtiment Nautibus 43 bd du 11 novembre 1918 69622 VILLEURBANNE Cedex Tél : 04.72. 43.19.05 Fax 04 72 43 13 10 infomaths@bat710.univ-lyon1.fr
Matériaux	**MATERIAUX DE LYON**	M. Jean-Yves BUFFIERE Secrétaire : Mériem LABOUNE INSA de Lyon École Doctorale Matériaux Mériem LABOUNE Bâtiment Antoine de Saint-Exupéry 25bis Avenue Jean Capelle 69621 VILLEURBANNE Tel : 04 72 43 71 70 Fax : 04 72 43 72 37 ed.materiaux@insa-lyon.fr
MEGA	**MECANIQUE, ENERGETIQUE, GENIE CIVIL, ACOUSTIQUE (ED n°162)**	M. Philippe BOISSE Secrétaire : Mériem LABOUNE Adresse : INSA de Lyon École Doctorale MEGA Mériem LABOUNE Bâtiment Antoine de Saint-Exupéry 25bis Avenue Jean Capelle 69621 VILLEURBANNE Tel : 04 72 43 71 70 Fax : 04 72 43 72 37 mega@insa-lyon.fr Site web : http://www.ed-mega.com
ScSo	**ScSo*** M. OBADIA Lionel Sec : Viviane POLSINELLI Insa : J.Y. TOUSSAINT	M. OBADIA Lionel Université Lyon 2 86 rue Pasteur 69365 LYON Cedex 07 Tél : 04.78.69.72.76 Fax : 04.37.28.04.48 Lionel.Obadia@univ-lyon2.fr

*ScSo : Histoire, Geographie, Aménagement, Urbanisme, Archéologie, Science politique, Sociologie, Anthropologie

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Résumé

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

La miniaturisation extrême des dispositifs CMOS est une des préoccupations majeures de l'industrie microélectronique. Il a fallu donc chercher des solutions innovantes pour répondre aux défis de cette miniaturisation soit en proposant de nouvelles architectures de circuits soit en utilisant de nouveaux matériaux ou aussi de nouveaux procédés de fabrication. Par exemple, la fabrication de l'oxyde permettant l'isolation électrique entre les transistors a nécessité sans cesse d'être améliorée. Ainsi, on est passé du procédé d'isolation par oxydation localisée de silicium (LOCOS) au procédé d'isolation par tranchées (STI) qui est utilisée maintenant pour la technologie la plus avancée en production. En STI, une gravure localisée des tranchées dans le substrat de silicium est réalisée. Cette étape est suivie d'une oxydation et d'un dépôt de silice. Le procédé se termine par une planarisation par polissage mécano-chimique (CMP). L'avantage de ce procédé est lié à la possibilité d'isoler les dispositifs avec des tranchées profondes de manière quasi-anisotrope alors que dans le cas du LOCOS, le procédé est isotrope, ce qui limite la profondeur de l'isolation au risque de consommer le silicium des zones actives par extension latérale du processus d'oxydation. Cependant, pour les technologies en développement, le STI commence à montrer quelques limitations.

Le premier problème, qui est illustré à la Figure 1, est lié au remplissage par la silice de tranchées de moins en moins larges. En effet, lorsqu'on diminue la largeur des tranchées, leur remplissage par la silice devient incomplet laissant des cavités d'air (Voiding). Le deuxième problème est lié à l'étape de planarisation qui conduit à un ''surpolissage'' des zones les plus larges (Dishing). De nouvelles approches sont envisagées pour remplacer le procédé STI. L'anodisation électrochimique est une piste prometteuse. En effet, cette technique utilisant un électrolyte à base d'acide fluorhydrique (HF) permet de rendre localement poreux le silicium en profondeur. Un recuit oxydant permet ensuite de transformer le silicium poreux en silice. Dans cette approche (Si poreux), la silice permettant l'isolation est obtenue par oxydation et non pas par dépôt ce qui écarte tout risque de voiding et limite l'extension latérale. Par ailleurs, cette approche ne nécessite aucune étape de CMP, éliminant ainsi le problème de dishing. Cette technique proposée a constitué le point de départ de nos travaux de thèse qui s'est focalisée sur deux axes principaux : d'une part la maîtrise du procédé d'anodisation électrochimique pour la formation du silicium poreux et d'autre part l'optimisation du procédé d'oxydation.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

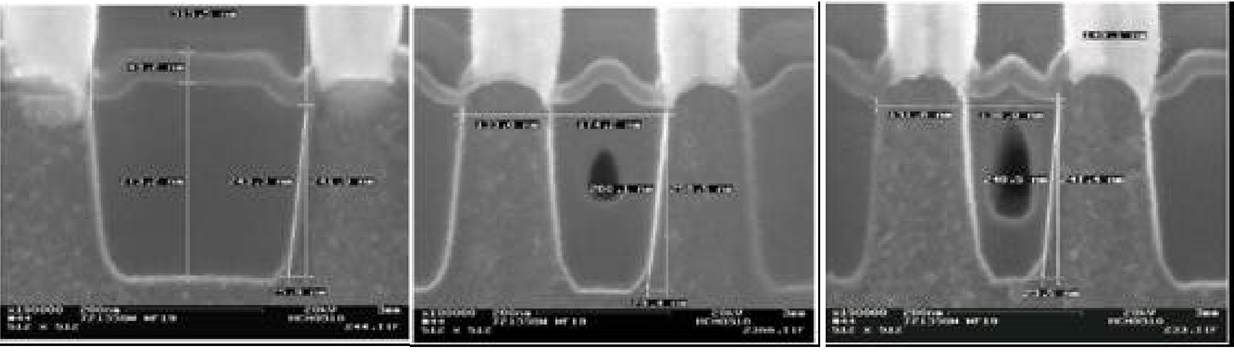


Figure 1 Image MEB illustrant une limitation du procédé STI quand on diminue la largeur des tranchées (voiding)

Dans **le premier chapitre** de ce mémoire de thèse, nous nous présentons le contexte du sujet travers une brève introduction sur l'évolution de la microélectronique et sa course continue pour la miniaturisation. On y trouve ainsi un rappel sur les réalisations importantes qui ont marqué l'histoire dans ce domaine telles que les premiers transistors commercialisés en 1954 puis l'invention des circuits intégrés (ICs) suite au développement du procédé de fabrication planaire en 1959 jusqu'à l'apparition du premier microprocesseur en 1971 [Sif04, Gil90]. Il est à noter que ce dernier exploit a lancé vraiment la croissance de l'industrie microélectronique et a ouvert la voie à la réalisation de microprocesseurs de hautes performances et de meilleure fiabilité, soutenue par la maturation du processus de fabrication et la miniaturisation continue des transistors. En effet, cette miniaturisation permet d'obtenir des ICs (i) plus rapides (fréquence de fonctionnement plus élevée), (ii) moins chers à fabriquer comme il est possible de monter plus de circuits sur une plaque de silicium et (iii) de consommation plus faible car les porteurs de charge ont tout simplement une distance plus courte à parcourir. Dans ce contexte, Gordon Moore, l'un des fondateurs d'Intel, a prédit que le nombre de transistors sur une plaque de silicium doublerait tous les deux ans [Moo75]. Cette prédiction, connue aussi sous la dénomination loi de Moore, a tenu bon pendant plus de quatre décennies et devrait être valable pour au moins une autre. Cette évolution impose de trouver des solutions à de nombreux et difficiles problèmes technologiques. Par exemple, la miniaturisation du transistor MOS nécessitait la réduction de l'épaisseur de son oxyde de grille (à base d'oxyde thermique de silicium SiO_2) pour maintenir les mêmes performances du dispositif (Loi de Dennard) [Den74]. Toutefois, pour les technologies les plus avancées, comme la longueur de grille a diminué en dessous de 130 nm, l'épaisseur d'oxyde de grille a dû être réduite d'environ 2 nm. Cela semble être une limitation fondamentale car le courant de fuite (courant tunnel grille-canal) devient très élevé (aussi grand que le courant de fuite

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

source-drain à l'état bloqué du transistor qui est d'environ 10 nA/µm^2 [Wol99]) rendant impossible la réalisation des MOS de haute performance. Pour cette raison, il a fallu remplacer le dioxyde de silicium par les matériaux high-k (matériaux de grande permittivité diélectrique) tels que l'oxyde d'aluminium Al_2O_3 ($\varepsilon = 9$), l'oxyde de zirconium ZrO_2 ($\varepsilon = 25$) et l'oxyde d'hafnium HfO_2 ($\varepsilon = 24$), ce qui permet d'obtenir les mêmes capacités avec de plus grandes épaisseurs physiques. De la même façon, le procédé de fabrication de l'oxyde d'isolation entre les transistors PMOS et NMOS dans une technologie CMOS a subi lui aussi des améliorations pour résoudre certaines limitations indiquées ci-dessus. On est passé ainsi du LOCOS au STI pour arriver à d'autres alternatives telles que l'approche Si poreux.

Dans une deuxième partie de ce premier chapitre, nous nous intéressons au silicium poreux qui est un matériau nanostructuré composé d'un réseau de cristallites de Si et de pores interconnectés. On présente tout d'abord les conditions expérimentales permettant sa formation. Le Si poreux est tout simplement obtenu en appliquant une polarisation positive (anodisation) à une plaque de silicium immergée dans de l'acide fluorhydrique (HF), ce qui conduit à une réaction entre les porteurs libres électroniques (les trous) et les ions négatifs fluor F^- à l'interface semiconducteur/électrolyte, puis une dissolution d'atomes de silicium du réseau du substrat. Dans le cas du silicium de type-n, l'apport de trous pourrait être assuré par illumination (photogénération de trous) ou application d'une forte tension d'anodisation. Certaines mesures doivent être prises en considération pour assurer une bonne expérience d'anodisation électrochimique, notamment une bonne homogénéité en profondeur de la couche poreuse (même diamètre de pore et même épaisseur de couche) avec une meilleure reproductibilité (un bon contrôle de la porosité et de l'épaisseur) d'une manip à l'autre, surtout quand il s'agit d'une porosofication profonde (> 2µm).

Par exemple, la cathode de platine (ou d'or) dans une cellule d'anodisation simple bain (Figure 2), qui est utilisé dans ce travail, devrait être de même taille, colinéaire et assez loin de l'anode du silicium afin d'obtenir une distribution de lignes de potentiel plus uniforme et assurer donc une gravure électrochimique homogène [Leh02]. De plus, au cours de la réaction d'anodisation, il y a dégagement gazeux de bulles de dihydrogène qui se collent à la surface de silicium et s'accumulent au fond des pores où se produit la réaction de dissolution, ce qui pourrait empêcher la progression de la gravure et induire une inhomogénéité latérale et/ou en profondeur. La solution à ce problème est d'ajouter un agent mouillant (communément l'éthanol) à la solution de HF qui favorise l'infiltration de l'électrolyte et donc l'élimination

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

de gaz. D'autre part, il est généralement conseillé d'utiliser un agitateur mécanique pour accélérer la libération de ces bulles de dihydrogène ou encore de remplacer le régime d'anodisation continu (courant continu appliqué) par un mode pulsé qui permet la régénération des ions fluore F^- dans les pores pendant les temps de repos et évite alors toute diminution de la concentration locale de HF et maintient une vitesse de gravure homogène [Hou96, Pop05]. Pour certaines applications, le contrôle de la température pendant l'anodisation électrochimique s'avère aussi essentiel et un système d'échangeur de chaleur devrait donc être intégré. Il a été démontré [Leh02] par exemple que la densité de courant d'électropolissage varie en fonction de la température selon un comportement de type Arrhenius avec une énergie d'activation de 0,345 eV pour du silicium de type-p anodisé avec une concentration de HF de 1 à 10%. Guillermain [Gui07] a également révélé que la température ambiante n'est pas le meilleur choix pour une bonne homogénéité de la couche poreuse. A basse température, la viscosité de l'électrolyte augmente ce qui conduit à une meilleure mouillabilité et facilite donc la libération du digydrogène. En outre, la vitesse de gravure diminue avec la température (vitesse de gravure à -40 °C est presque 30 à 100 fois inférieure à celle à la température ambiante pour une même porosité) et permet ainsi non seulement un contrôle précis de l'épaisseur mais aussi une bonne homogénéité de la couche poreuse puisque l'électrolyte trouverait le temps de se régénérer. Setzu et al. [Set98] ont aussi signalé une diminution importante de la rugosité de l'interface Si/Si poreux en diminuant la température concluant ainsi que c'est un bon moyen pour obtenir du Si poreux de bonne qualité de point de vue structural.

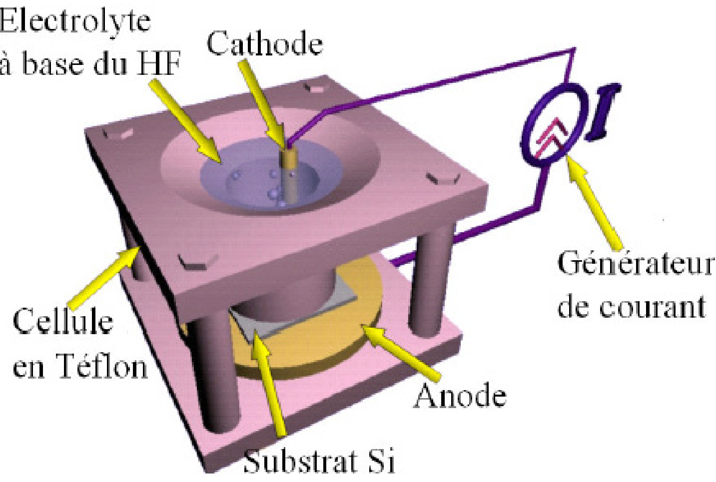


Figure 2 Cellule d'anodisation électrochimique simple-bain

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Par la suite, nous donnons un aperçu des principales propriétés structurales du Si poreux (porosité, surface spécifique, taille des pores, épaisseur de la couche) et les méthodes qui permettent leur caractérisation en soulignant leur variation avec les paramètres d'anodisation (concentration HF, densité de courant, type et niveau de dopage du substrat).

Le Si poreux peut prendre différentes formes morphologiques (spongieuse, colonnaire…) qui sont principalement déterminées par le type et le niveau de dopage du substrat initial. La taille moyenne des pores (ou des nanocristallites) peut varier du micromètre à quelques nanomètres. On peut alors distinguer du macroporeux (taille de pore comprise entre 0.1-1µm), du méso-poreux (structure colonnaire fortement anisotrope avec un diamètre de pore de quelques dizaines de nanomètre) et du nanoporeux (structure spongieuse avec un réseau aléatoire de pores de quelques nanomètre de diamètre). Il faut aussi mentionner que chaque nanocristallite conserve la structure cristalline du substrat initial avec la même orientation [Bar84]. On note également que pour le Si de type-n faiblement dopé, l'orientation cristallographique semble avoir un effet significatif sur la morphologie de la couche poreuse [Fol02,Lev93]. Il en résulte des macropores qui ne sont pas forcément perpendiculaire à la surface mais qui croissent plutôt selon la direction des plans cristallins <100> et <113> [Ron99], ce qui donne une morphologie finale sous forme d'un pore principale dans l'une de ces deux directions avec des branches dans les autres directions. La distribution en taille des pores peut être déterminée à l'aide des mesures d'absorption de gaz [Her87] ou avec la microspectroscopie Raman [Bru97,Isl01] ou par des mesures de rayon X [Bel96,Leh93].

La surface spécifique d'une couche poreuse représente toute la surface interne de cette couche par unité de masse ou par unité de volume [Roq94]. Elle peut être déterminée à partir de mesures d'absorption de gaz [Bom88] ou par comparaison de la vitesse de gravure du silicium poreux dans le HF avec celle du substrat de silicium [Hal94]. La surface spécifique du Si poreux peut varier de 50 à 1000 m^2/cm^3.

La porosité d'une couche poreuse est définie comme la fraction volumique du vide. Elle peut varier de 30% à 90% et peut être déterminée par gravimétrie ou par mesure de l'indice de réfraction en FTIR (spectroscopie infrarouge à transformée de Fourier). Il est à noter que la porosité augmente avec la densité de courant d'anodization et diminue en augmentant la concentration de HF. Cependant, il a été observé qu'à faible densité de courant, la porosité augmente quand la densité de courant diminue. Ceci peut être expliqué par la

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

dissolution chimique qui commence à devenir importante par rapport à la dissolution électrochimique à faible courant [Nyc06]. D'autre part, la porosité dépend aussi de la concentration de dopants du substrat. Pour des même conditions d'anodisation (densité de courant et concentration en HF), les couches nanoporeuses obtenues par exemple à partir du silicium de type-p faiblement dopé sont reconnu comme étant de plus grande porosité que les couches mesoporeuse ou macroporeuse [Leh00].

Quant à la vitesse de formation du Si poreux (ou vitesse de gravure électrochimique), elle varie quasi linéairement avec le courant sauf pour le cas du Si de type-n faiblement dopé où elle est reste constante mais elle diminue avec la concentration de HF. Il faut mentionner également que cette vitesse d'attaque dépend peu de la concentration de dopage du substrat sauf pour le type-n moyennement et fortement dopé où elle croît en diminuant la densité de courant.

Toute application du Si poreux nécessite une bonne compréhension de la formation de ce matériau permettant ainsi une maîtrise parfaite de ses propriétés avec les paramètres d'anodisation. **Le deuxième chapitre** de ce manuscrit s'attache à l'étude de l'une des propriétés qui est la dépendance de la formation du Si poreux avec la concentration de dopants. Pour cela, une analyse détaillée des caractéristiques courant-tension I-V est menée sur le Si durant son anodisation électrochimique.

Notre dispositif expérimental est représenté sur la Figure 3. La surface de l'échantillon de silicium en contact avec l'électrolyte est de 0,5 cm^2 (0,8 cm de diamètre) et la contre-électrode est une grille de platine (ou or) cylindrique, parallèle et assez loin de l'électrode de silicium. Pour relever des caractéristiques I-V dans un milieu électrochimique, un montage bipolaire simple avec deux électrodes ne sera pas suffisant. Il permet uniquement de relever la différence de potentiel entre les deux électrodes, et non le potentiel de chaque électrode (par rapport à une référence commune), en général nécessaire pour une interprétation fiable et complète. Comme une couche de Helmholtz peut être formée sur l'électrode de platine et peut modifier considérablement son potentiel en fonction du temps [Bar80, Shy96], les caractéristiques I-V enregistrées seront en quelque sorte faussées et ne donneront pas la bonne information sur l'électrode de silicium (distribution de potentiel de la jonction silicium/électrolyte) qui nous intéresse. Pour cette raison, une troisième électrode, qui est une électrode de référence Ag/AgCl, est utilisé. Le courant est donc fourni entre l'électrode de travail et la contre-électrode, et le potentiel de l'électrode de travail est mesuré par rapport à

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

l'électrode de référence en utilisant un sourcemètre Keithley 2602 contrôlé par un programme Labview via une carte GPIB. La connexion électrique ainsi obtenue peut être considérée comme similaire au montage quatre pointes utilisé dans la caractérisation de dispositifs électroniques. Le deuxième avantage de l'électrode de référence est qu'elle peut être placée au plus près de la contre électrode, ce qui permet de s'affranchir de la chute de potentiel dans l'électrolyte qui pourrait devenir importante par rapport à la tension appliquée. D'autre part, le contact face arrière silicium/plaque de cuivre doit être ohmique. Il est assuré par un dépôt d'aluminium sous vide suivie d'un recuit thermique rapide à 700 °C sous atmosphère d'azote. Dans le cas du silicium faiblement dopé, un fort dopage de la face arrière des échantillons est aussi effectué.

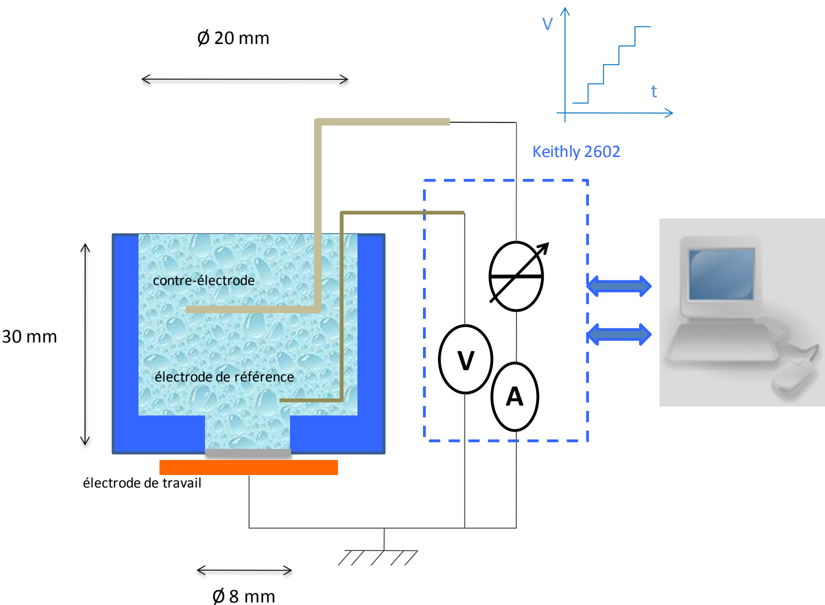


Figure 3 Connexion électrique de la cellule d'anodisation électrochimique

D'après la caractéristique I-V montrée à Figure 4, on peut distinguer trois régimes d'anodisation électrochimique : le régime de porosofication (ou de formation de pores), le régime d'électroplissage (aucune nanostructuration de la surface) et le régime de transition qui est une compétition entre la porosofication et l'électroplolissage. Ces régimes dépendent de la concentration de HF et de la densité de courant appliquée. Par exemple, la formation de Si poreux se fait à forte concentration de HF et à faible densité de courant tandis que l'électroploissage se produit à forte densité de courant et à faible concentration de HF.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

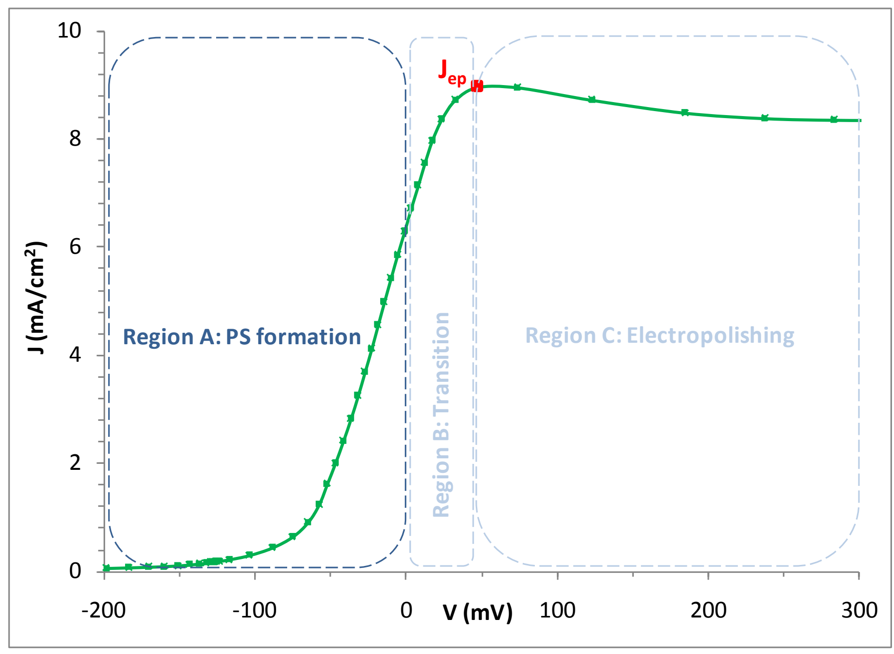


Figure 4 Caractéristique I-V de l'anodisation électrochimique de silicium montrant les trois régimes de porosofication, électropolissage et transition

On s'intéresse dans ce travail au régime de formation du Si poreux. Pour le Si de type-p, la représentation semi-logarithmique des caractéristiques I-V montre, sur un intervalle de 1 à 100 mA/cm^2, une variation linéaire de la densité de courant en fonction de la tension avec une pente de 59 mV/décade, en accord avec un contact classique métal/semiconducteur de pente (kT/q) x Ln(10) (où q est la charge élémentaire, k la constante de Boltzmann et la T température absolue). Ce résultat révèle, comme suggéré par plusieurs auteurs [Gas89, Leh00 et Smi92], que le courant au cours de la porosofication de p-Si est déterminé par une émission thermoïonique des trous à travers une barrière Schottky à la surface de la zone de silicium déplétée. Cependant, cela n'explique pas le décalage observé des caractéristiques I-V vers les tensions négatives quand la concentration de dopage du substrat augmente (Figure 5). Gaspard et al. [Gas89] ont attribué ce décalage à une augmentation de la chute de potentiel à travers la couche d'Helmholtz présente à l'interface électrolyte/silicium. Cet effet a été modélisé avec succès en considérant la capacité due à la couche d'Helmholtz en série avec la zone déplétée dans le silicium. Cette approche a été vérifiée expérimentalement et a été à l'origine du développement d'une technique simple d'extraction du profil de dopage dans le silicium de type-p par voie électrochimique. En effet, au cours de l'anodisation d'un échantillon de Si type-p présentant des variations de concentration en dopants en marches d'escalier, les variations de tensions enregistrées peuvent être converties en concentrations de

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

dopants utilisant la relation ci-mentionnée, et l'échelle de temps d'anodisation en profondeur connaissant la vitesse de gravure.

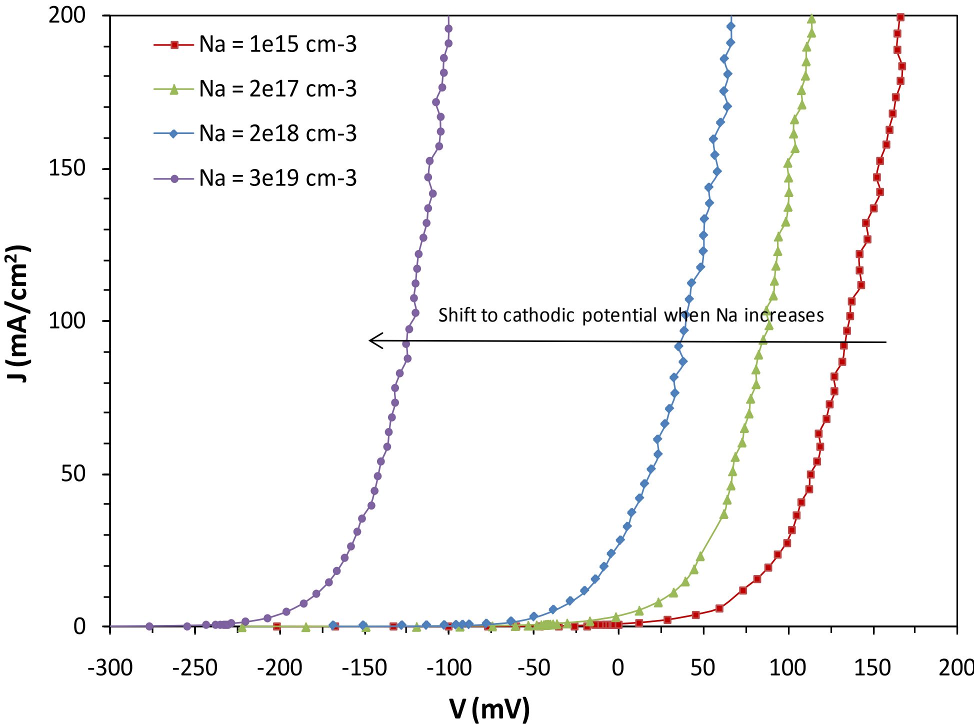


Figure 5 Caractéristiques I-V de l'anodisation du silicium de type-p dans le HF pour différents concentrations de dopage du substrat

Le profil de dopage obtenu est représenté à la Figure 6 et comparé au profil mesuré avec l'analyse SIMS (spectroscopie de masse d'ions secondaires). Un très bon accord entre la technique électrochimique et la mesure SIMS est obtenu pour la partie descendante du profil (les trois premières marches). On montre également que la résolution en profondeur de cette technique est liée au niveau du dopage et s'approche de celle du SIMS pour les fortes concentrations avec une valeur estimée de 60 nm/décade. Cependant, la technique présente quelques limitations. Elle est d'une part limitée au Si de type-p. D'autre part, elle ne peut pas fournir le bon profil de dopage lorsque le niveau de concentration des impuretés à analyser est inférieure à celui de la couche sous-jacente (partie ascendante du profil où les concentrations de dopage mesurées par la méthode électrochimique ne suivent plus les variations en marche d'escalier). Ce dernier problème peut être expliqué par l'inhomogénéité du front de gravure de la réaction électrochimique.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

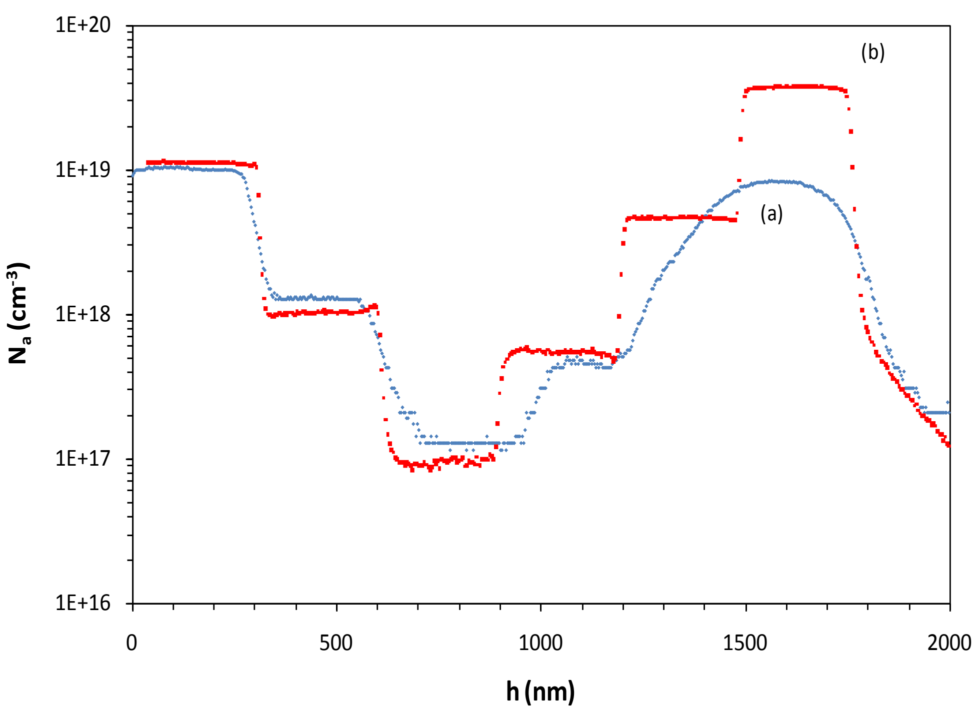


Figure 6 Profil de dopage d'un échantillon déterminé par (a) la technique Si poreux et (b) l'analyse SIMS

En ce qui concerne l'anodisation du Si de type-n en obscurité, la jonction Si/électrolyte étant en inverse, le passage de courant donnant lieu à la formation du Si poreux ne se produit qu'après claquage de la région de charge d'espace à la surface de l'électrode par un fort champ électrique fournissant ainsi les trous nécessaires à la dissolution du silicium. En fonction de la concentration de dopage et de la tension appliquée, on peut distinguer deux mécanismes de transport de charge à l'origine de ce claquage: l'effet tunnel et l'effet d'avalanche. Les caractéristiques I-V pour le n-Si ont montré elles-aussi un décalage vers les tensions négatives quand la concentration de dopage augmente. Par contre, on n'a pas pu quantifier ce décalage sur toute la gamme de concentration étudiée ce qui rend impossible d'appliquer la technique de profilométrie décrite précédemment au silicium de type-n. D'autant plus, le potentiel d'anodisation, à densité de courant constante et pour une concentration de dopage donnée, n'est pas fixe au cours du temps car il est affecté par un claquage prématuré dû à une rugosité très importante de l'interface Si/Si poreux.

Après avoir étudié la formation du Si poreux, nous nous intéressons dans **le troisième chapitre** à son oxydation. Nous essayons d'optimiser les conditions d'anodisation et d'oxydation permettant d'obtenir un Si poreux oxydé localisé de bonne qualité diélectrique.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

L'oxydation est réalisée dans un four SEMCO standard à oxydation sèche sous pression atmosphérique. Pour oxyder le Si poreux, nous avons utilisé un procédé d'oxydation à deux étapes similaire à celui décrit par plusieurs groupes [Bom88, Lin86 et Mol05]. Dans ce procédé, le Si poreux subit d'abord une étape primordiale de pré-oxydation à des températures assez basses (environ 300 °C) afin de stabiliser sa structure initiale contre toutes transformations irréversibles lors d'un traitement thermique élevé. En effet, pour des températures supérieures à 400 °C, une désorption des atomes d'hydrogène couvrant la couche interne se produit, ce qui entraîne la migration en surface des atomes de silicium et l'effondrement des pores [Gup88]. On se retrouve alors avec une structure composée de larges pores entourés par de murs de silicium très épais dont l'oxydation complète devient très difficile, voire impossible. La pré-oxydation permet donc de résoudre ce problème en couvrant toute la surface interne du Si poreux par une mince couche d'oxyde thermique (1-3 nm d'épaisseur) qui vient stabiliser la texture contre toute restructuration à haute température. En revanche, il est bien évident que cette étape de pré-oxydation n'est pas aussi suffisante pour assurer l'oxydation complète de la couche poreuse, même si un long temps d'oxydation est appliqué. En fait, la température n'est pas assez élevée pour permettre la diffusion de l'oxygène à travers la couche superficielle d'oxyde formée. Pour cela, une deuxième étape d'oxydation à des températures plus élevés est réalisée.

Pour cette étape, l'obtention du Si poreux totalement oxydé (c'est-à-dire n'ayant pas de résidu de Si) et non poreux dépend du choix des paramètres d'anodisation (densité de courant et concentration de HF…) et d'oxydation (température et temps d'oxydation). Le tableau ci-dessous (Table 1) présente la composition (en Si, SiO_2 et air) de l'oxyde final de plusieurs échantillons obtenus après différents temps et températures d'oxydation et à partir du Si poreux de différentes porosités. Cette composition est donnée sous formes de fractions volumiques calculées à partir de la mesure (par spectroscopie FTIR) de l'indice de réfraction de la couche du Si poreux oxydé et en s'appuyant sur le modèle de Landau-Lifshitz-Looyenga des milieux effectifs. La fraction oxydée, définie comme le pourcentage de silicium de la couche poreuse ayant oxydé, est aussi donnée.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Table 1 Résultats des mesures par spectroscopie FTIR

		Conditions d'oxydation		Mesures FTIR			
éch. n°	**P %**	**(T,t)**	**t_{ox} (nm)**	**f_{SiO2}**	**f_{Si}**	**f_{air}**	**ξ_{ox}**
1	82	(1000°C,1h)	120	0.38	0	0.62	1
2	73			0.62	0	0.38	1
3	58			0.87	0.03	0.1	0.92
4	47			0.84	0.16	0	0.7
5	46	(1000°C,2h)	125	0.85	0.15	0	0.7
6	65	(800°C,1h)	50	0.39	0.18	0.43	0.5
7	60			0.56	0.15	0.29	0.62
8	50			0.62	0.22	0.15	0.55
9	58	(800°C,2h)	52	0.54	0.18	0.27	0.57
10	57	(800°C,4h)	55	0.56	0.18	0.26	0.58

Il est bien clair d'après ce tableau que la cinétique d'oxydation du Si poreux dépend à la fois de la température et du temps d'oxydation. On peut remarquer que la fraction oxydée ξ_{ox} augmente avec la température et sature après 1 heure d'oxydation à 800 °C ou à 1000 °C. Une valeur de saturation de 0,5 à 0,6 (échantillons n° 8, 9 et 10) est enregistrée à 800 °C tandis qu'une oxydation totale (ξ_{ox} = 1) est obtenue à 1000 °C (échantillons n° 1, 2 et 3). Cependant, il paraît qu'une oxydation totale de la couche poreuse ne puisse être atteinte que si la porosité initiale est suffisamment élevée. Par exemple, pour les échantillons n° 4 et 5, ξ_{ox} vaut seulement 0,7 après 1 h ou 2 h d'oxydation à 1000 °C et le matériau final est composé uniquement de silicium et de dioxyde de silicium sans air. Compte tenu du taux d'expansion volumique du SiO_2, une porosité d'environ 56% (échantillon n° 3) est un optimum théorique corroboré par l'expérience pour assurer une oxydation complète du Si poreux (avoir un oxyde final sans Si résiduel qui pourrait dégrader les propriétés d'isolation électrique et thermique) et obtenir un oxyde avec une porosité minimale. Un oxyde poreux n'est pas préférable car il pourrait provoquer des problèmes lors de processus de fabrication ultérieurs (capture des impuretés et gravure rapide au HF). D'autre part, une telle porosité permet aussi d'éviter toute déformation possible du silicium et le développement des défauts causés par le taux

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

d'expansion du dioxyde de silicium. Il a été démontré en fait que le Si poreux subit un changement de volume après oxydation (expansion si la porosité est inférieure à 56% et contraction si supérieur) qui pourrait introduire des contraintes élastiques [Barl86, Hol83]. Enfin, il est à noter que même une porosité initiale de 56% ne peut pas éviter un caractère un peu poreux de l'oxyde final avec la présence de cavités d'air nanométriques en raison de la nature chaotique de la structure initiale du poreux. Par conséquent, un recuit à haute température pourrait être envisagé afin d'obtenir un oxyde dense similaire au SiO_2 thermique. Cette dernière étape de densification, telle que proposée par certains auteurs [Bom88, Yon87], est réalisée par un écoulement visqueux de silice et exige des températures supérieures à 1000° C. Pour des raisons de limitation de la température de notre four, nous n'avons pas accompli cette étape.

Dans une deuxième partie du chapitre 3, nous mettons en évidence la formation localisée du silicium poreux oxydé (Figure 7) en exploitant la propriété de dépendance de la formation du Si poreux avec la concentration de dopage, déjà étudié au premier chapitre. En effet, un choix judicieux du potentiel d'anodisation permet de rendre poreux sélectivement des régions fortement dopées implantées dans un substrat de silicium faiblement dopé (sans recours à un masque). Ces régions sont ensuite transformées en oxyde par un recuit oxydant.

Par ailleurs, nous donnons quelques recommandations utiles pour la fabrication d'un oxyde final localisé relativement plan et uniforme, tirant profit des études d'optimisation de formation du Si poreux et son oxydation bien contrôlée détaillées ci-avant (dans les parties précédentes). A titre d'exemple, il semble que le silicium de type-n est mieux adapté à être utilisé que le type-p dans la mesure où il présente une plus grande sélectivité pour la formation du Si poreux et qu'il montre moins de variation de la porosité avec la densité de courant ce qui permet d'obtenir une structure poreuse plus homogène en profondeur et d'avoir des résultats plus reproductibles. De plus, outre le réglage des paramètres d'anodisation pour obtenir une porosité de 56%, il est conseillé d'utiliser un régime potentiostatique pour l'anodisation avec une tension appliquée suffisamment faible pour éviter le claquage de la surface de silicium.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

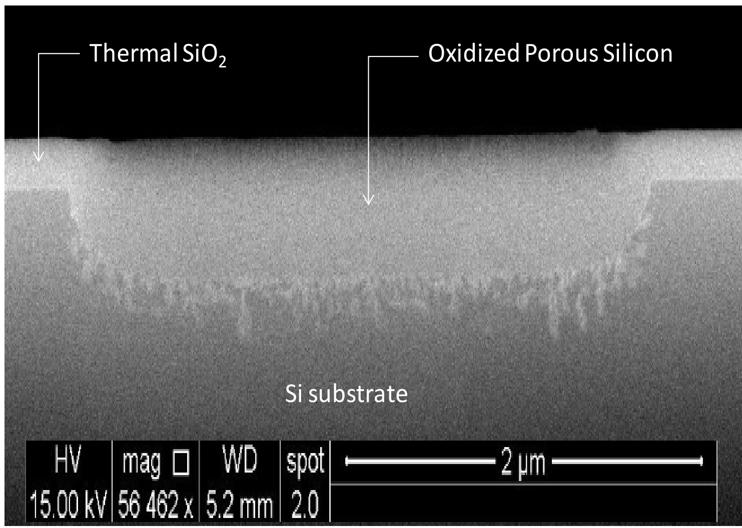


Figure 7 Image MEB: formation localisée du silicium poreux oxydé

Enfin, on a pu montrer également que la composition du Si poreux oxydé peut être aussi déterminée à partir des mesures électriques capacité-tension C-V complémentaires. Alors que dans le FTIR, on mesure l'indice de réfraction, avec les mesures C-V, on détermine la constante diélectrique de la couche du Si poreux oxydé. Par ailleurs, nous avons montré, à partir de la caractérisation I-V que le Si poreux oxydé peut être considéré comme un bon isolant diélectrique, présentant une résistivité électrique assez élevée ($\rho = 2.10^{13}$ Ωcm) et un courant de fuite raisonnable (de l'ordre de 1 µm/cm^2 à une polarisation de 10V).

En conclusion, le Si poreux est un matériau très intéressant qui offre des propriétés prometteuses conduisant à une grande variété d'applications. Dans ce travail, nous nous sommes intéressés à la propriété de dépendance de la formation du Si poreux avec la concentration de dopants. Grâce à l'étude des caractéristiques I-V au cours de l'anodisation électrochimique, il a été constaté que cette dépendance est contrôlée, pour le silicium de type-p, par la chute de potentiel à travers la couche de Helmholtz qui est présente à l'interface Schottky électrolyte/silicium polarisée en direct.

Ce dernier résultat a été à l'origine du développement d'une méthode très simple de profilométrie des impuretés dans le silicium de type-p à l'aide de l'anodisation électrochimique. En effet, il a été démontré que pendant l'anodisation à courant constant d'un échantillon de Si de type-p présentant une variation de concentration en dopants en marches d'escalier, les variations de la tension d'anodisation pouvaient être converties en variations de concentration de dopage grâce au modèle ''Schottky + Helmoltz'', et l'échelle de temps

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

d'anodisation en échelle de profondeur connaissant la vitesse de gravure. Nous avons exploité cette propriété pour former localement du Si poreux oxydé apportant ainsi une précieuse avancée à notre objectif de départ. En effet, nous avons pu vérifier que lorsqu'une plaque de Si avec des régions de différentes concentrations de dopage est anodisée à potentiel constant bien choisi, le courant de dissolution ne circule que dans les zones de dopage les plus élevées et par conséquent le Si poreux est uniquement formé dans ces zones. Nous avons également essayé d'optimiser les procédés d'anodisation et d'oxydation afin d'obtenir un oxyde final de bonne qualité. Néanmoins, la formation du Si poreux oxydé dépend de plusieurs paramètres au cours des trois principales étapes de sa fabrication: l'implantation ionique, l'anodisation électrochimiques et l'oxydation. Par conséquent, il sera nécessaire d'optimiser encore mieux chacune de ces étapes afin d'obtenir un oxyde final présentant des propriétés diélectriques fiables comparable à celles de l'oxyde obtenu par CVD qui est utilisé en STI. Ensuite, pour confirmer la faisabilité de la technique Si poreux pour les technologies CMOS au-delà de 65 nm, des transistors MOS doivent être réalisés puis caractérisés et comparées à ceux fabriquées par STI.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Contents

GENERAL INTRODUCTION......................................1

CHAPTER 1: STATE OF THE ART................................5

INTRODUCTION..7

1. MINIATURIZATION..8

1.1. MICROELECTRONICS EVOLUTION..8

1.2. MINIATURIZATION: A FEW KEY FIGURES..9

1.3. MOSFET SCALING..10

2. LIMITATIONS AND CHALLENGES OF SCALING..12

2.1. ULTRATHIN OXIDE: HIGH-K MATERIAL..13

2.2. FIELD OXIDE: CMOS ISOLATION..15

2.2.1 LOCOS..*15*

2.2.2 STI..*16*

2.2.3 STI by PS approach..*18*

2.3. SOI..20

3. POROUS SILICON: FABRICATION, PROPERTIES AND APPLICATIONS.....**23**

3.1. ANODIZATION CONDITIONS AND PARAMETERS..24

3.1.1 Anodization cell..*24*

3.1.2 Electrolyte..*26*

3.1.3 Current density..*27*

3.1.4 Other experimental considerations..*30*

3.2. STRUCTURAL PROPERTIES OF PS..30

3.2.1 Microstructure..*31*

3.2.2 Specific surface area..*33*

3.2.3 Porosity..*34*

3.2.4 Growth rate..*35*

3.3. PS APPLICATIONS..37

3.3.1 Optical-optoelectronic applications..*38*

3.3.2 Sensor applications..*38*

3.3.3 Micromachining applications..*38*

CONCLUSION..**40**

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

CHAPTER 2: INVESTIGATION OF CURRENT-VOLTAGE CHARACTERISTICS OF SILICON IN HF SOLUTION.............41

INTRODUCTION..43

1. EXPERIMENTAL SET UP..44

1.1. EXPERIMENTAL CONDITIONS..44

1.2. ELECTRICAL CONNECTION..45

1.3. SAMPLE PREPARATION – BACK SIDE OHMIC CONTACT...47

1.4. DESCRIPTION OF SAMPLES..47

2. GENERAL CURRENT-VOLTAGE CHARACTERISTICS OF SILICON IN HF SOLUTION...................................48

2.1. ELECTROCHEMICAL REGIONS OF THE SI/HF SYSTEM...49

2.1.1 Cathaodic polarization..50

2.1.2 Anodic polarization...50

2.2. ANODIC DISSOLUTION REGIONS IN P-SI AND DEPENDENCE ON THE ANODIZATION PARAMETERS..................51

3. CHARGE EXCHANGE MECHANISM DURING PS FORMATION OF P-TYPE SILICON........................53

3.1. THE ANODIZATION POTENTIAL IS DETERMINED AT THE SI/HF INTERFACE.................................54

3.2. THE “SCHOTTKY BARRIER + HELMOLTZ LAYER” MODEL...56

3.3. THE ANODIZATION POTENTIAL DEPENDENCE TOWARD THE DOPING CONCENTRATION.............................59

4. APPLICATION: P-TYPE SILICON DOPING PROFILING USING ELECTROCHEMICAL ANODIZATION.................61

4.1. THE METHOD PRINCIPLE: POTENTIAL VARIATIONS DURING PS FORMATION..............................61

4.2. CONVERSION OF POTENTIAL VARIATIONS DURING ANODIZATION TO DOPING PROFILING.......................63

4.3. LIMITATION OF PROFILING METHOD BY ELECTROCHEMICAL ANODIZATION...............................65

5. CHARGE CARRIER TRANSFER DURING PS FORMATION OF N-TYPE SILICON..............................67

5.1. HIGHLY DOPED N-SI..67

5.2. LOW DOPED N-SI...69

5.3. MODERATELY DOPED N-SI...70

6. APPLICATION: N-TYPE SILICON DOPING PROFILING USING ELECTROCHEMICAL ANODIZATION.................73

CONCLUSION..78

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

CHAPTER 3: OXIDIZED POROUS SILICON: PROCESS OPTIMIZATION, LOCALIZATION AND DIELECTRIC PROPERTIES 79

INTRODUCTION **81**

1. POROUS SILICON OXIDATION PROCESS **82**

1.1. PRE-OXIDATION 83

1.2. TOWARD A COMPLETE OXIDATION OF PS 84

1.2.1 OPS characterization using FTIR *84*

1.2.2 Complementary characterization using CV measurements *90*

2. FABRICATION OF LOCAL OPS **93**

2.1. ELECTROCHEMICAL ANODIZATION 95

2.2. OXIDATION 97

3. DIELECTRIC PROPERTIES OF OPS: INVESTIGATION OF CURRENT-VOLTAGE CHARACTERISTICS **99**

3.1. PRE-OXIDIZED PS SAMPLES 100

3.2. OXIDIZED PS SAMPLES 104

CONCLUSION **106**

GENERAL CONCLUSION 109

APPENDICES 113

REFERENCES 118

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

General introduction

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Device miniaturization has become the main concern of the microelectronic industry from a long period of time. Therefore, researchers are always trying to find innovative solutions for technological challenges by proposing either new materials or new designs or new fabrication processes. For example, the oxide allowing the isolation between devices in an electronic chip has been also scaled down and has then exhibited different technological processes. The latest process which is widely used in the most advanced in-production CMOS (complementary metal oxide semiconductor) technologies is the STI (shallow trench isolation) process. It is based on three main steps: trench etching, filling with CVD (chemical vapor deposited) oxide and planarization by CMP (chemical mechanical polishing), and it came to replace the LOCOS (local oxidation of silicon) process which encountered a primary problem known as bird's beak encroachment that limits the circuit packing density.

However, for sub-65 nm technologies under development, STI begins to show some limitations: voiding and dishing. In fact, filling of narrow trenches with CVD oxide cannot be perfect and voids can possibly be left between active areas. In addition, CMP planarization may only work for the narrow gaps and leads to a non-planar surface that will not be well suited for further lithography steps. An alternative solution, which is based on local anodization of silicon and further oxidation of the formed porous silicon, is proposed to overcome these limitations of voiding and dishing. The approach, in which neither dry etching nor CMP are required, seems to be promising.

In this context, our PhD project is defined. It focuses on the study of porous silicon (PS) in order to take advantage of its interesting properties. The properties and characteristics of this material have been extensively investigated since its discovery six decades ago leading to a large variety of applications. In our work, we will rather interest in the properties of (i) PS formation dependence with silicon doping concentration and (ii) its high rate of oxidation for the application of electrical isolation.

The manuscript is divided into three chapters which are organized in the following manner.

The first chapter or the state of the art chapter introduces the main purpose of our work. It first focuses on the art of miniaturization in microelectronics through some key figures and examples of technological challenges. We describe in particular the different fabrication processes used for electrical isolation of CMOS devices and discuss their

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

limitations. We propose hence the PS method as an alternative solution that deserves investigation. The chapter also provides an introduction to PS with special emphasis putted on its properties and their dependence on the anodization parameters.

The second chapter is devoted to the well understanding of PS formation through the investigation of current-voltage characteristics of n- and p-type silicon electrodes during electrochemical anodization. It highlights the property of PS formation dependence with silicon doping concentration which is exploited for the application of doping profiling by electrochemical anodization.

The last chapter deals with the oxidation of PS. Electrical and optical characterizations are performed on oxidized PS in order to determine its structural and dielectric properties and thus optimize its fabrication process. A particular attention is also given to the fabrication of local oxidized PS.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Chapter 1: State of the art

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Introduction

In this introductory chapter, we first present a brief summary of the microelectronic evolution and its continual need for miniaturization. We give some examples of important limitations and technological challenges for the most advanced technologies. This leads us to introduce both the FIPOS process which seems to be a promising alternative to the STI process in CMOS isolation, and the SOI technology based on PS formation which becomes to be intensively investigated by the semiconductor industry. In a second time, a special interest is given to the porous silicon material. After presenting experimental conditions allowing PS formation, we go through the structural properties of this material giving an overview of their characterization and underlining their dependence on the anodization parameters.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

1. Miniaturization

In this first part, we present a historical review of major devices and achievements in the field of the microelectronic industry which is still ruled up to now by the law of miniaturization or scaling.

1.1. Microelectronics evolution

Since the "big-bang" of electronics in 1947 when J. Bardeen, W. Brattain, and W. Shockley discovered for the first time that when electrical contacts were applied to a crystal of germanium, the output power was larger than the input [Wei73], much research efforts of scientists and engineers have devoted to the developing of semiconductor devices. This quest led to the emergence of a new branch of electronics, called the semiconductor industry, which experienced tremendous growth over the following decade announced by the fabrication of several different types of innovative devices going from the first commercial silicon junction transistor produced by Texas Instruments in 1954 to the first MOS (metal oxide silicon) transistor built at Bell Labs in 1960 [Sif04].

The year 1959 was marked by the development of the planar process which resulted in the invention of integrated circuits (ICs). From that date, one could say that the capabilities of the transistor begun to be fully utilized with the large number of devices integrated within the silicon and the vast variety of circuit functions implemented. Later, the need of producing ICs with higher yield and hence lower cost, greater performance and enhanced reliability have pushed manufacturers to do efforts to improve the fabrication process and propose new logic-style families such as transistor-transistor logic (TTL), diode-transistor logic (DTL) in 1962 and complementary metal oxide semiconductor (CMOS) in 1963 [Pav08]. The increased complexity of ICs and the great requirement of developing circuits suitable for generalized applications instead of designing each IC to serve a single application have led then to the apparition of the first microprocessor in 1971 namely the 4004 with 2800 transistors and 60000 instructions per second [Gil90].

This achievement have boosted the growth of the semiconductor industry and opened the way to fascinating improvements of microprocessors with higher performance and higher reliability, driven by the maturation of the manufacturing process and supported by the continual scaling of transistors. In this context, Gordon Moore, one of the founders of Intel,

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

predicted in 1965 that the number of transistors on a silicon wafer would double every eighteen months [Moo65] before altering his projection in 1975 to a doubling every two years [Moo75]. Anyway, this prediction, referred to as Moore's Law, has held good for more than four decades and is expected to hold true for at least another as illustrated in Figure 1.

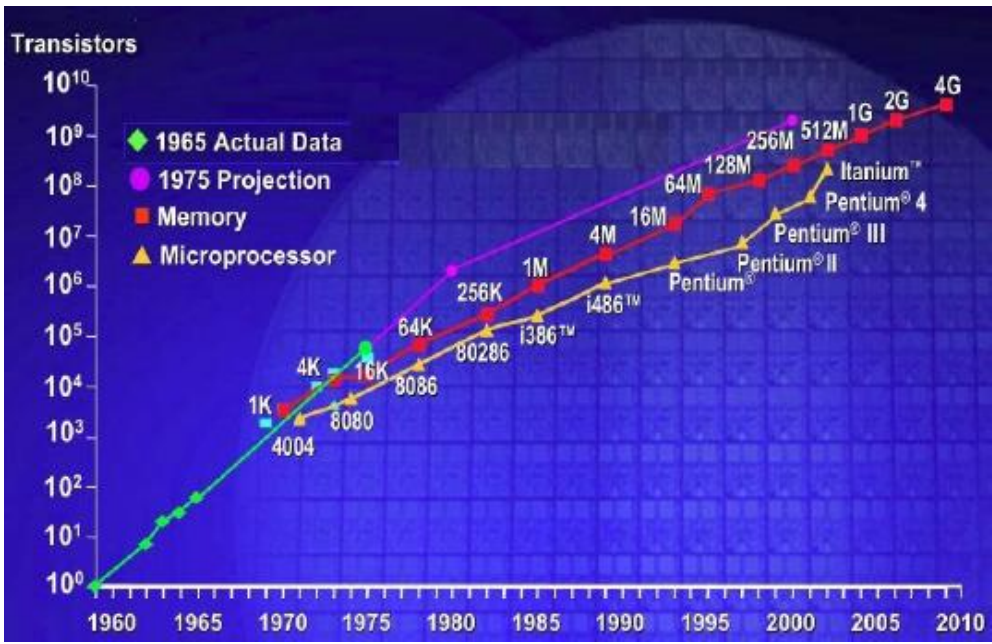


Figure 1 Illustration of Moore's law through the evolution of Intel microprocessors and memories[1]

1.2. Miniaturization: a few key figures

Device miniaturization has become then the major concern of the semiconductor industry for a long time. Indeed, it results in chips that are (i) faster (of higher operation frequency), (ii) cheaper to make as it is possible to fit more integrated circuits on a silicon wafer and (iii) of lower power consumption because the charge carriers have simply a shorter distance to move.

For example, the cost per bit of memory chips has halved every 2 years for successive generations of dynamic random access memories (DRAMs). The device speed has improved by a few orders of magnitude since 1959 and digital ICs are able now to perform numerical

[1] According to the Intel web site: www.intel.com

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

computation at terabit-per-second rates. The energy dissipated per logic gate has decreased by over one million times since 1959 [Sze01].

The minimum device dimension of an integrated circuit, also called the minimum line width, has been reduced at an annual rate of about 13% i.e., a reduction of 30% every 3 years. The half-pitch (i.e., half the distance between identical features in an array of a memory cell), to which the name of the technology node is associated, was decreased for example from 0.8 µm in the year 1989 to 0.13 µm in 2002 and will shrink to 22 nm around 2015 according to the prediction of the International Technology Roadmap for Semiconductors (ITRS). The Table 1 below gives scaling examples of some physical and electrical parameters.

Table 1 The technology generation from 1989 to 2002[2] and future scaling trends adapted from 2009 ITRS[3]

Year of production	1989	1999	2002	2010	2012	2015	2020
Technology node	800	180	90	45	32	22	12
Physical gate length (nm)	-	130	50	18	22	15.3	10.7
Equivalent gate oxide thickness: EOT (nm)	-	-	-	1.4	1.2	1.1	0.8
Supply voltage: V_{DD} (V)	5	2	1.8	1	0.9	0.81	0.68
Clock frequency (MHz)	40	1200	1600	2500	4000	6600	12500

1.3. MOSFET scaling

Since the beginning of the microelectronics era, it was noticeable that the connections among active devices of a circuit presented an important obstacle for increasing circuit performance. The invention of the integrated circuit considerably alleviated interconnect-related problems by bringing the interconnects on-chip reducing then the interconnect length and thus decreasing significantly the delay and the power consumption. Over the next decades, on-chip interconnects were not the major focus of the IC design process, as performance improvements reaped from scaling the devices were much greater than any degradation caused by the interconnects [Pav08].

[2] Intel microprocessors
[3] According to the ITRS web site: www.itrs.net

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Here, we try to take the example of the metal oxide semiconductor field effect transistor (MOSFET) as it is the dominant device in ULSI (ultra large scale integration) ICs and as it can be scaled to smaller dimensions than other types of devices [Sze01]. The table above gives an overview of this drastic scaling rate through the gate length.

Electrical characteristics of the MOS transistor can be described mainly by two parameters: the saturation current I_{ON} and the leakage current I_{OFF} [Web05]. A low current I_{OFF} will help limit the consumption and the static power dissipation ($P_s = V_{DD} \times I_{OFF}$) in a circuit while the operation frequency or the switching speed of logic gates will be governed by (i) the resistance and capacity of interconnection wires and (ii) the delay of the transistor τ given by

$$\tau = \frac{V_{DD} \times C_{gate}}{I_{ON}}$$

where C_{gate} is the gate capacitance.

For the transistor device itself (without interconnections), It is noticeable that a high current I_{ON} allows a high switching frequency but it is not a sufficient condition. Indeed, according to the last equation and the expression of the drain current-voltage I_D-V_D at saturation[4], one can note that if the current increases by a variation of the gate capacitance C_{gate} (i.e. by reducing the gate oxide thickness or increasing the width W of the transistor), the intrinsic delay will remain constant. Scaling of the gate length L can however improve I_{ON} and thus τ. It is on this simple principle which improves both the integration density and the performance of transistors that is based Moore's Law.

Nevertheless, reducing L is still associated with some unwanted parasitic or side effects referred to as short channel effects which mainly cause degradation of I_{OFF}. To avoid such a problem, Dennard [Den74] has proposed a scaling rule for optimizing the device performance which consists of scaling down all dimensions and voltages of the MOSFET so that the internal electric fields are kept the same. This constant field scaling is shown in Table 2 along with the real scaling used in the semiconductor industry [Sze06].

---

[4] $I_{ON} = I_{Dsat} = \mu C_{gate} \frac{W}{2L} V_{Dsat}^2$ where μ is the carriers mobility, W and L are the gate width and length, respectively.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Table 2 MOSFET scaling rules according to Dennard [Den74] and real scaling [Web05, Bak10, Ngu09]

	Scaling factor	
Parameter	**Dennard's law** ($\alpha<1$)	**Actual** ($\alpha < \lambda < 1$)
Gate length, width: L,W	α	α
Gate oxide thickness: t_{ox}	α	α
Junction depth: X_j	α	α
Substrate doping: N_A, N_D	$1/\alpha$	λ/α^2
Electric field: E	1	λ/α
Supply voltage: V_{DD}	α	λ
ON current: I_{ON}	1	λ^2/α^2
Active power: P	α^2	λ^3/α
Transistor delay: τ	α	λ^2/α

2. Limitations and challenges of scaling

Challenges of new technologies beyond 100 nm include for example the formation of ultra shallow source/drain junction with low sheet resistance which can be achieved by employing low energy and high dosage ion implantation. In addition, as the dimension of the device size scales down, the delay time (RC) resulting from multilevel interconnection increases significantly and hence low speed operation is achieved. Consequently, to overcome this problem, both high-conductivity metals, such as copper Cu (1.7 µΩcm compared with 2.7 µΩcm of aluminum Al), and low-dielectric constant (low-k) insulators, such as organic (polyimide) or inorganic (fluorine doped oxide) materials should be used instead of the conventional Al and oxide [Sze01]. Another important issue is the gate material: since the mid-1970s, the metal (Al) MOSFET gate is replaced by the polysilicon gate [Wol99] that offers a self-aligned structure but as the gate lengths were scaled down, the resistance of the polysilicon lines became too large to be effective in their secondary role as a local interconnect (even when they were doped as heavily as possible). That's why it became necessary to use a metal silicide layer on top surface of the poly film. The Ti-silicide process

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

had then been widely used until it encountered limitations for deep sub-micron technologies because the sheet resistance of a $TiSi_2$ line is found to increase with decreasing line width. $CoSi_2$ and NiSi processes seem to be the promising candidates.

Many other important issues have also paid great attention when MOSFET scaling is in question in order to ensure a well optimized performance of the device. Among these issues, one can also mention tailoring of the channel doping profile in both lateral and vertical directions to control the threshold voltage, and adjusting the formation of the p/n-type wells and the drain structure to avoid parasitic effects and inter device leakage currents. For more details, it can be referred for example to [Wol99, Sze01]. In the following sections, we have chosen to discuss in more details scaling limitations related to two features: the gate oxide and the field oxide. In fact, the first is widely studied recently at least in our laboratory in the frame of several theses while the second will be useful to introduce the general context of our work.

2.1. Ultrathin oxide: high-k material

MOSFET transistors have been continually scaled since they were first introduced and hence the gate oxide, made by thermally grown silicon dioxide SiO_2, had also to be progressively thinner to maintain the device performance. However, for the most advanced technologies, since the gate length shrank below 130 nm, the gate oxide thickness had to be reduced around 2 nm. This seems to be a fundamental limitation because the gate-to-channel tunneling leakage current becomes very high (approximately as great as the off-state source-to-drain leakage current of about 10 $nA/\mu m^2$ [Wol99]) leading infeasible to build high performance logic MOSFETs.

For this reason, to allow the scaling of gate lengths (below 100 nm) and permit further miniaturization of devices, high-k dielectric materials such as aluminum oxide Al_2O_3 ($\varepsilon = 9$), tantalum pentoxide Ta_2O_5 ($\varepsilon = 26$), zirconium oxide ZrO_2 ($\varepsilon = 25$) and hafnium oxide HfO_2 ($\varepsilon = 24$) are suggested as alternative candidates for the gate dielectric to replace silicon dioxide. With these materials, thicker dielectric layers can be used resulting in less carrier tunneling with maintaining the same MOSFET capabilities (Figure 2). In fact, it can be possible to achieve the same equivalent oxide thickness EOT as required for SiO_2, according to:

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

$$C_{ox} = C_{high-k} \rightarrow \mathrm{EOT} = \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} \times t_{high-k}$$

where C_{ox}, C_{high-k} are the gate oxide capacitances with SiO_2 and the high-k dielectric, respectively, t_{high-k} is the thickness of the high-k dielectric, ε_{ox} and ε_{high-k} are the relative permittivities of SiO_2 and the high-k, respectively. For example, a high-k gate insulator with a thickness t_{high-k} of 10 nm and a dielectric constant ε_{high-k} of 20 will behave in the same way in a MOSFET as a SiO_2 layer with a thickness of 2 nm.

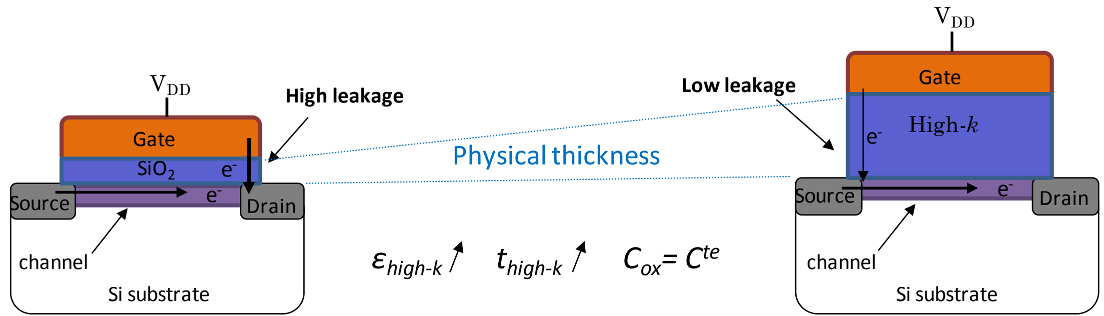


Figure 2 Reducing the tunneling current using high-k material

However, one of the drawbacks of using high-k dielectrics is that if they are deposited directly on silicon they tend to have a high level of interface states [Sze06,Ngu09]. The interface states density can be reduced by growing a thin layer of silicon dioxide (1-2 atomic layers i.e. 0.8-1.6 nm thickness) on the silicon to passivate the surface. This interfacial layer will however limit the highest possible gate stack capacitance or, equivalently, the minimum achievable EOT value as this latter will never be less than that of the high-k layer according to the equation below:

$$\frac{1}{C_{equ}} = \frac{1}{C_{ox}} + \frac{1}{C_{high-k}} \rightarrow \mathrm{EOT} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} \times t_{high-k}$$

A bilayer approach necessarily limits the use of high-k materials and let the scaling of the gate dielectric a greatest challenge to be investigated in order to find the ideal gate dielectric stack that seems to be the good compromise between many factors like compatibility with the actual fabrication process, reducing EOT and obtaining high quality Si/dielectric interface.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

2.2. Field oxide: CMOS isolation

The dominant technology for MOSFET is the CMOS (complementary MOSFET) technology, in which both n-channel and p-channel MOSFETs (called NMOS and PMOS, respectively) are provided on the same chip. CMOS technology is particularly attractive for ULSI circuits because it has the lowest power consumption of all IC technologies. One of the tasks of CMOS miniaturization is to reduce the isolation distance between NMOS and PMOS. This isolation is of primary importance for suppressing leakage current between the devices (NMOS and PMOS) that must be kept electrically isolated from one another.

One of the simplest methods of isolation is to fabricate the CMOS such that a reverse-bias pn-junction is formed between the transistors. Oppositely doped regions (n-well adjacent to p-well) can be electrically isolated by tying the n-region to the most positive potential in the circuit and the p-region to the most negative. As long as the reverse-bias is maintained and the breakdown voltage is not exceeded for all operating conditions, a small reverse diode saturation current accounts for the leakage current. However, as this leakage current is directly proportional to the junction area, for relatively large p- and n-regions in modern devices, junction isolation alone becomes not adequate [Bak10]. Hence, a second method of isolation is proposed which is related to the formation of a thick dielectric region between transistors. The region without the thick dielectric, where transistors reside, is known as the active area. The relatively thick oxide that is formed between the active areas is called the field oxide (FOX). There are two general approaches of forming FOX regions which are extensively used in the semiconductor industry: LOCOS and STI.

2.2.1 LOCOS

Local oxidation of silicon (LOCOS) isolation was developed in the early 1970s and it remained, for its simplicity, the conventional isolation process for CMOS ICs during 30 years until these technologies reached the 0.35 µm generation [Fra04,Wol99]. In LOCOS, a silicon nitride layer (100-200 nm) is deposited and patterned over a thin pad oxide (10-50 nm) to define active and field oxide areas. The pad oxide serves as a stress relief layer; it diminishes the stress-induced dislocations that a thick nitride exerts in silicon. Nitride acts as a diffusion barrier for oxygen; areas under nitride will not be oxidized. LOCOS process flow is pictured in Table 3.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

The primary limitation of LOCOS is the lateral extension of the oxide that encroaches into the active area and thereby reduces the achievable circuit packing density. This problem is known as bird's beak encroachment as the lateral oxide feature resembles in cross-section a bird's beak (Figure 3). A thinner pad oxide would help minimize bird's beak but at the expense of silicon damage from nitride stress.

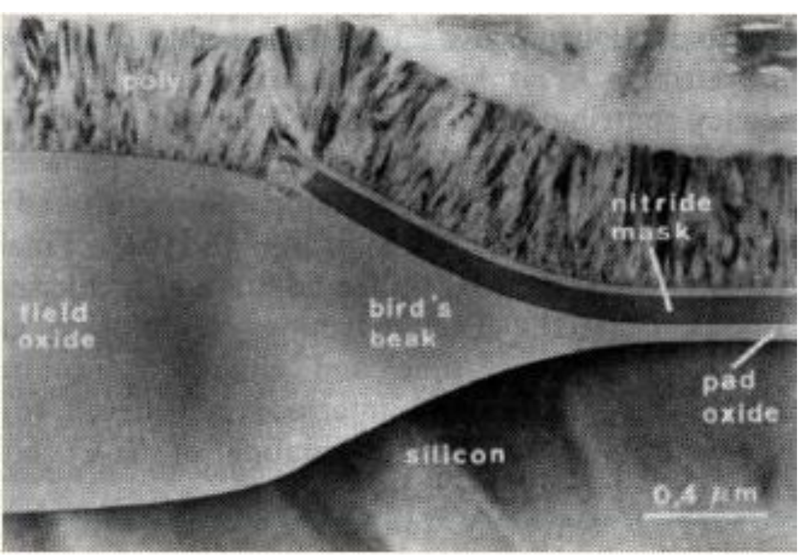


Figure 3 TEM picture of a bird's beak obtained by using classical LOCOS [Cla84]

Moreover, LOCOS requires a high temperature and a long time process which can result in significant diffusion of previously introduced dopants. The resulting non planar topography is also a matter that makes subsequent optical lithography (depth-of-focus problems) and deposition steps not easy (e.g. in multi-level metallization for advanced ICs, via-hole etching and sputtering become difficult because holes will be of different depths). Recessed LOCOS [Fra04] with additional etching step had been used to make the surface more planar after oxidation resulting in approximately equal surface heights for oxide and silicon. The shallow trench isolation (STI) technology can avoid all these problems and has become the mainstream technology for isolation, precisely in IC generation beyond 0.35 µm.

2.2.2 STI

Table 3 shows the process sequence of forming a shallow trench isolation structure. In STI, there are four main steps: after patterning, trenches are etched and filled with oxide deposited by CVD (chemical vapor deposition) to form the FOX region. CMP (chemical mechanical polishing) is finally used to remove the oxide on the nitride and to get a flat

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

surface. Due to its high resistance to polishing, the nitride acts as a stop-layer for the CMP process. After the polishing, the nitride layer and the oxide layer can be removed by phosphoric H_3PO_4, and hydrofluoric HF acids, respectively. It should be mentioned that the planarization step is helpful for subsequent patterning and planarization in the multilevel interconnection processes.

From a processing perspective, STI is complex but it has overcome LOCOS problems and brought interesting benefits to CMOS fabrication. Since the isolation material is deposited by CVD, it does not need high and long time temperature process. So, it has a relatively low thermal budget, avoids unwanted dopant diffusion and eliminates wasting area from bird's beak lateral extent. The process takes also advantage of CMP, which offers planarity of the final structure.

The STI process, even if it is still used for the most advanced in-production CMOS technology, has however some disadvantages that make it unsuitable for sub-65 nm technologies under development. Trenches are becoming of high aspect ratio: for 65 nm node, there are 90 nm wide and 350 nm deep. In fact, filling of narrow trenches cannot be perfect and voids can possibly be left between active areas as illustrated in Figure 4. It causes hence bad quality isolation and poses reliability problems as residues from processing can be trapped in these crevasses [Til06,Nan98,Nak01 and Kli06]. This phenomenon, that it can be referred as voiding, is similar to the problem of poor or non conformal step coverage of some metals when they are sputtered into via holes in the metallization process [Fra04]. In addition, CMP planarization has to be able to polish narrow and large areas at the same rate. If a large area polish rate is higher, planarization will only work for the narrow gaps and result in non planar surface that is critical for further lithography steps. This is known as dishing [Boy96, Che97, Bon02 and Yu92]. It must be remembered that various etchback processes have also been tried for planarization instead of CMP, but they have pattern size and pattern density effects similar or worse than CMP, and results are therefore no better.

An alternative solution based on local anodization of silicon (or selective PS formation) is proposed to overcome these limitations of voiding and dishing encountered in the STI process. The approach seems to be promising and has aroused our motivation to be comprehensively studied.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

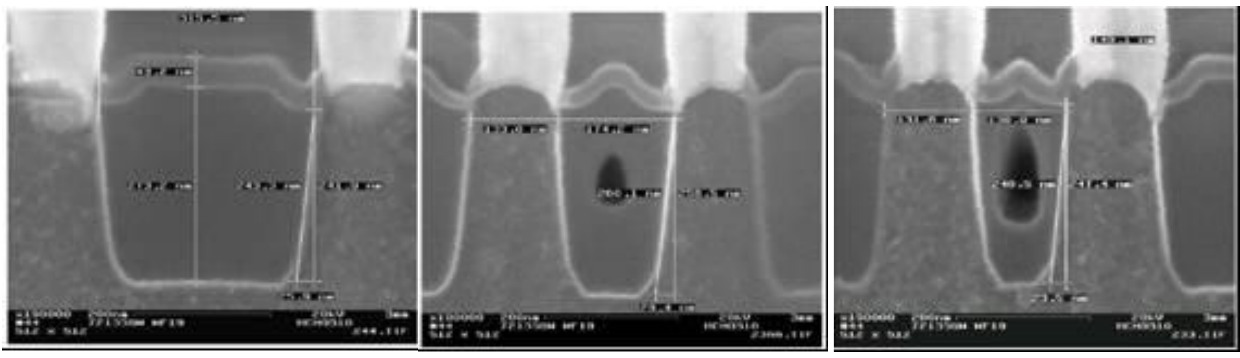


Figure 4 STI limitation: voiding when isolation width is reduced, SEM image courtesy A. Halimaoui, ST microelectronics

2.2.3 STI by PS approach

The STI by PS approach is also known as FIPOS (full isolation by porous oxidation of silicon) process. It should be mentioned that the idea of using PS for device isolation process was suggested in several patents in the mid-1970s [Can97] and feasibility of FIPOS was successfully demonstrated in CMOS fabrication by Imai et al. [Ima84] in 1984. The method was however not putted, in our knowledge, into production since STI has still shown satisfying performances for many years.

The strong dependence of PS formation rates on type and dopant concentration of silicon (e.g. only heavily doped p+ regions containing in a lightly doped p-type wafer are turned into PS during anodization), along with the extremely high chemical reactivity of PS, particularly its rapid oxidation in comparison with that of bulk silicon, have made feasible thick oxidized PS (OPS) films with possible associated dielectric properties equivalent to those of conventional thermal silica.

In the FIPOS process, as it is described in Table 3, a p-type wafer with a nitride layer is first patterned by a resist and then implanted by boron ions to form highly doped p-type regions in the unmasked areas. After rapid thermal annealing (RTA) and resist stripping, these areas are converted into PS by electrochemical anodization in hydrofluoric acid (HF) solution while the lightly doped regions remain unetched. Finally, a wet or dry thermal oxidation transforms the PS into silica resulting in silicon regions fully embedded in oxide. According to this process, it is noticeable that silica allowing isolation is obtained by oxidation and not by deposition which eliminates any risk of voiding. Furthermore, no CMP step is required excluding thus the problem of dishing. The process is also simple to integrate in the standard

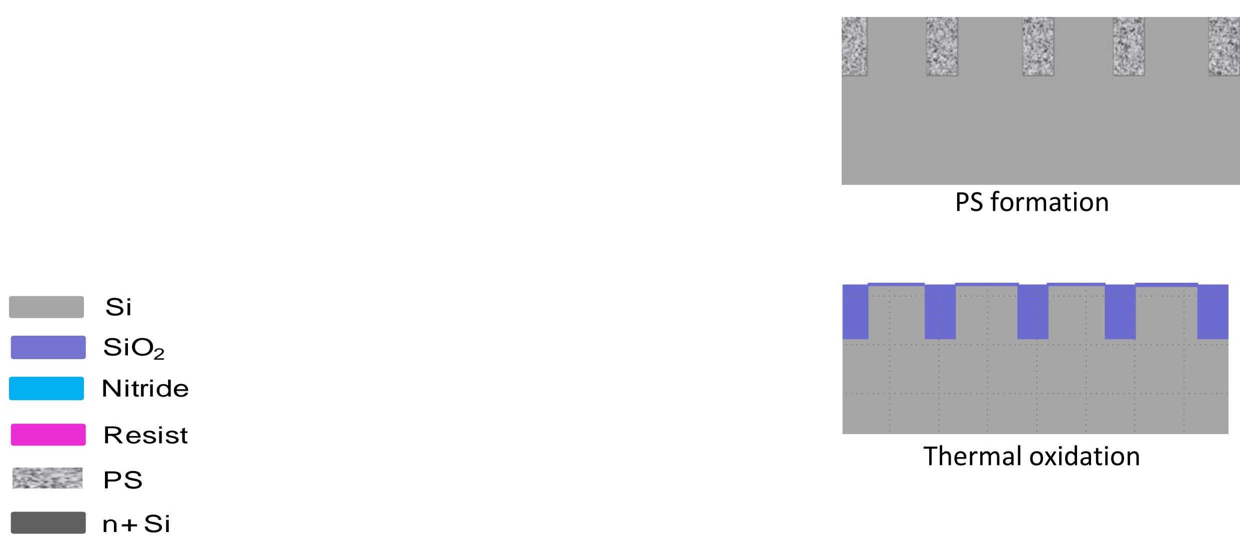
Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

process flow. Another application which can be derived from is the fabrication of silicon on insulator (SOI) substrate by forming silicon islands on a silicon dioxide layer [Can97]. Even more, it could be possible to fabricate any semiconductor on insulator substrates and this represents a major challenge for co-integration of heterogeneous electronic circuits.

Table 3 Process flow for different isolation techniques: LOCOS, STI and STI by PS approach

LOCOS	STI	STI by PS approach
Pad oxide (thermal) & pad nitride (LPCVD) deposition	Pad oxide (thermal) & pad nitride (LPCVD) deposition	Pad oxide (thermal) & pad nitride (LPCVD) deposition
Patterning and stack etching	Patterning and trench etching	Patterning and stack etching
Resist stripping & thermal oxidation	Resist stripping & trench filling (CVD oxide deposition)	Doping and thermal activation
Nitride etching	CMP planarization of the oxide (polish stop at nitride) & etch pad oxide+nitride	Resist stripping

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



2.3. SOI

CMOS technology had largely been built on so-called bulk-Si wafers. In such wafers, the devices are isolated from one another by a combination of isolation structures at the silicon surface and p-n junctions in the silicon bulk. SOI wafers began to be used instead of bulk Si wafers since the late 1960's for military integrated circuit applications before they have been widely commercialized after more than 30 years [Wol99]. SOI technology offers significant improvements over bulk wafers in many ways. First, the leakage currents through the bulk are eliminated among devices which can hence operate at higher temperature around 300 °C as opposed to bulk devices which fail above ca. 125 °C [Fra04]. Second, parasitic circuit elements associated with the CMOS structure (such as source-to-substrate and drain-to-substrate capacitances) are reduced which lead to lower power and higher speed. Third, the fabrication process in SOI wafers is simplified as more processing has been already done to the wafer to begin with. Although SOI wafers are more expensive to fabricate than bulk Si wafers (their cost is ca. 10 times the cost of bulk wafers), this cost disadvantage is compensated by other factors like smaller chip size, higher performance and easier processing (less process steps).

Manufacturers use very different technologies for making SOI structures. One of the most promising is based upon the formation of PS. The idea was first patented by Watanabe and Sakain in 1969 [Bon05] and since that date a variety of techniques have been intensively investigated in order to obtain large SOI wafers with low defects [Yak00, Ben86, Oul92,

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Lin86, Mol05, Ima84, Bom88 and Bom89]. Figure 5 shows the number of US patents published per year during the period from 1976 up to 2003 and dedicated to applications of PS for SOI. All known SOI fabrication methods exploiting PS can be classified into two main groups. The first is based on preferential anodization of n+ (or p+) layer within an epitaxial n-/n+/n- (or p-/p+/p-) structure followed by an oxidation of the PS formed in the accessible and buried layer. The second is based on the ability to grow under certain conditions an epitaxial silicon layer over a PS film which is then oxidized. Technological steps of both approaches are schematically shown in Table 4. Using this type of SOI structure, circuits with good electrical characteristics have already been fabricated in CMOS technology [Bar86]. However, even if the process by PS approach is simple, it has low cost and allows the fabrication of thick insulating oxide with less rough silicon surface (as no CMP is required), it presents a chief constraint for technologists and circuit designers who prefer to work on full wafer SOI structures and not on a predetermined configuration dictated by a mask. In fact, both of the described methods, the selective anodization or the epitaxial growth of PS on Si, require access to the buried layer: in the first case to form and to oxidize PS, in the second case to oxidize PS, which thus leads to form just silicon islands over a silicon dioxide layer. In addition, there are more or less important limitations that can be improved by process optimization such as thickness non uniformity of the OPS layer, induced wafer warpage after oxidation and mainly the OPS non uniformity underneath the silicon islands where the PS fronts in the lateral direction overlap (problem with the first approach).

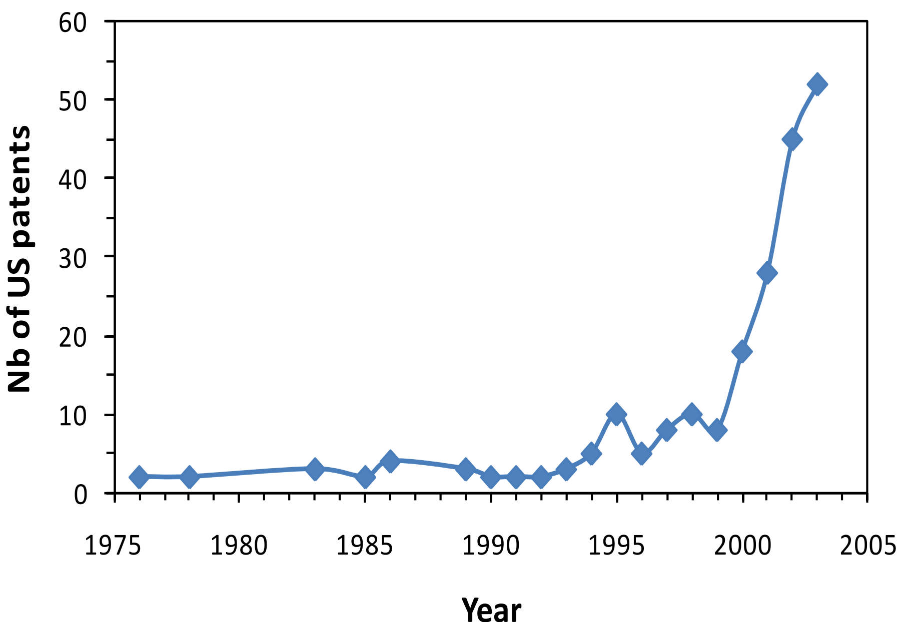
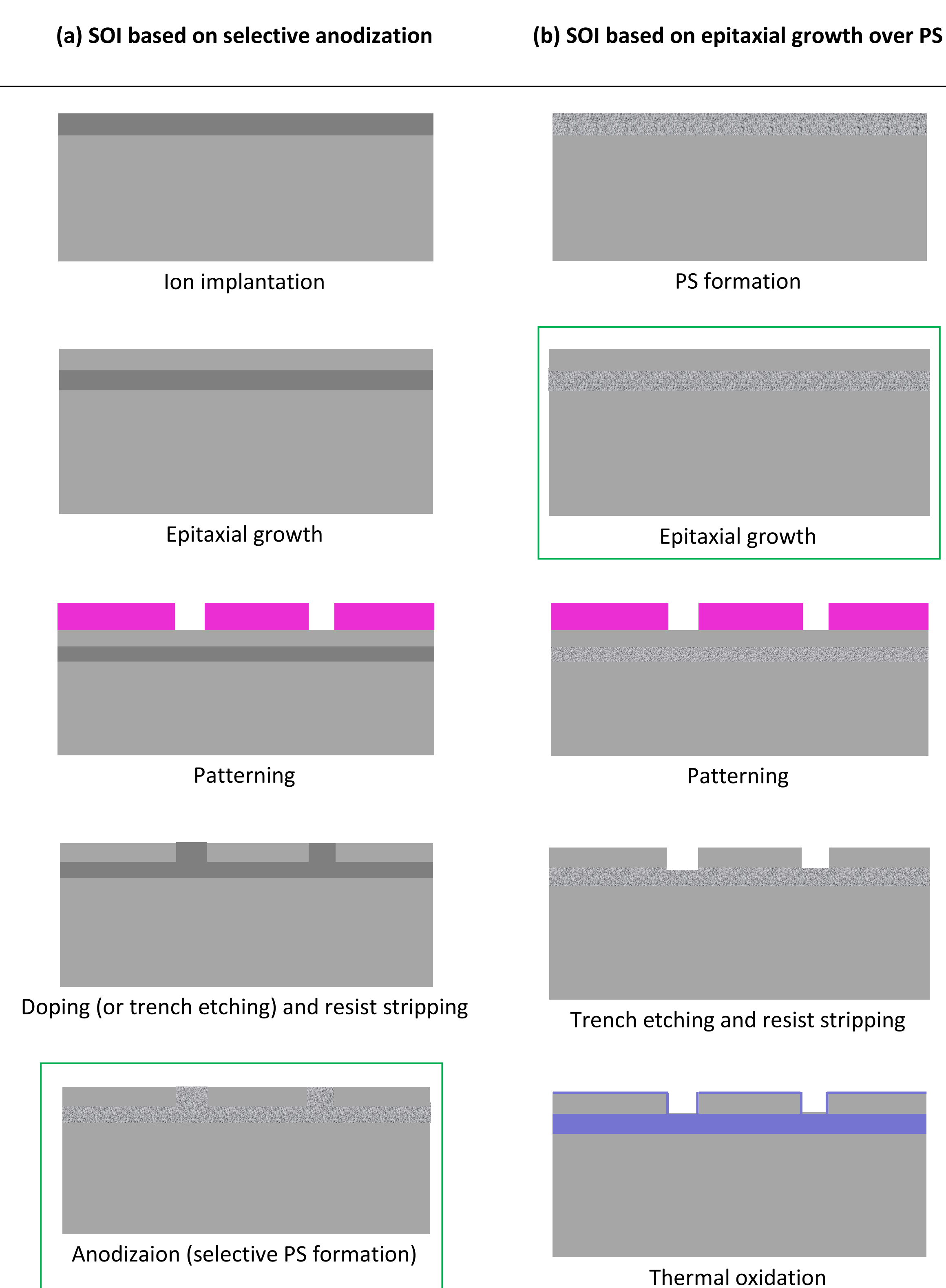


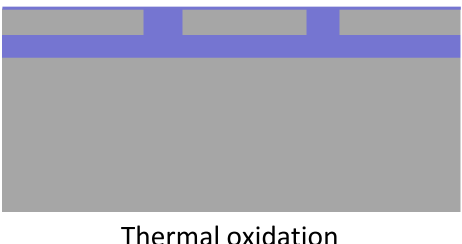
Figure 5 The number of US patents devoted to SOI based on PS and published per year, redrawn from [Bon05]

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Table 4 Process flow of two different PS approaches involved in the fabrication of SOI structure, based on: (a) the selective anodization of a buried n+ Si layer and (b) the epitaxial growth of Si over PS, surrounded in green is the most critical step of each approach



Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



3. Porous silicon: fabrication, properties and applications

PS is a sponge like structure (Figure 6) obtained by electrochemical anodization of silicon in hydrofluoric acid solution (HF). Simply, it is realized by applying an anodic bias to a wafer immersed in HF leading to a reaction of electronic holes with negative fluoric ions at the semiconductor/electrolyte interface and then a dissolution of silicon atoms from the substrate lattice.

The material was first discovered over 40 years ago during the electropolishing of silicon in aqueous HF acid, and has since been studied extensively [Smi92]. Many important applications have been emerged taking advantage of the new properties offered by PS compared to single crystal silicon and its compatibility with the semiconductor fabrication industry. They have then made of PS a versatile material in today's technology. It has just to know that anodic dissolution of silicon in HF came to its greatest prominence when visible photoluminescence (PL) from PS was observed at room temperature in 1990 by Canham [Can90].

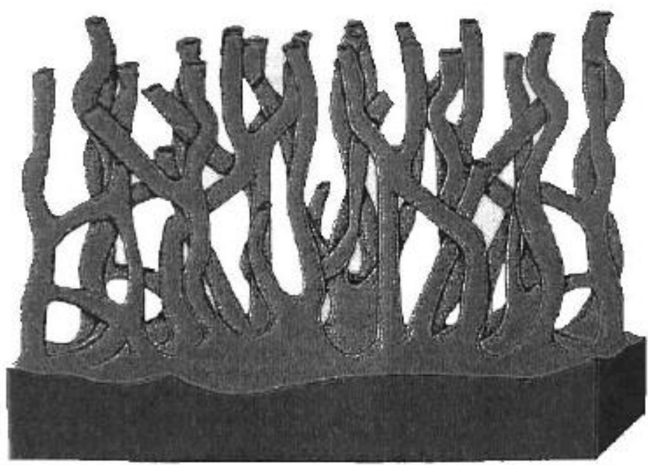


Figure 6 A schematic view of a PS layer over a single crystal silicon substrate

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

3.1. Anodization conditions and parameters

In this part, we present the essential requirements to fabricate PS and we go through some important details that are necessary for a successful experiment.

3.1.1 Anodization cell

The two different cell designs available in our laboratory and which are commonly used in literature as they offer a sufficiently good uniformity of porous layer are shown in Figure 7.

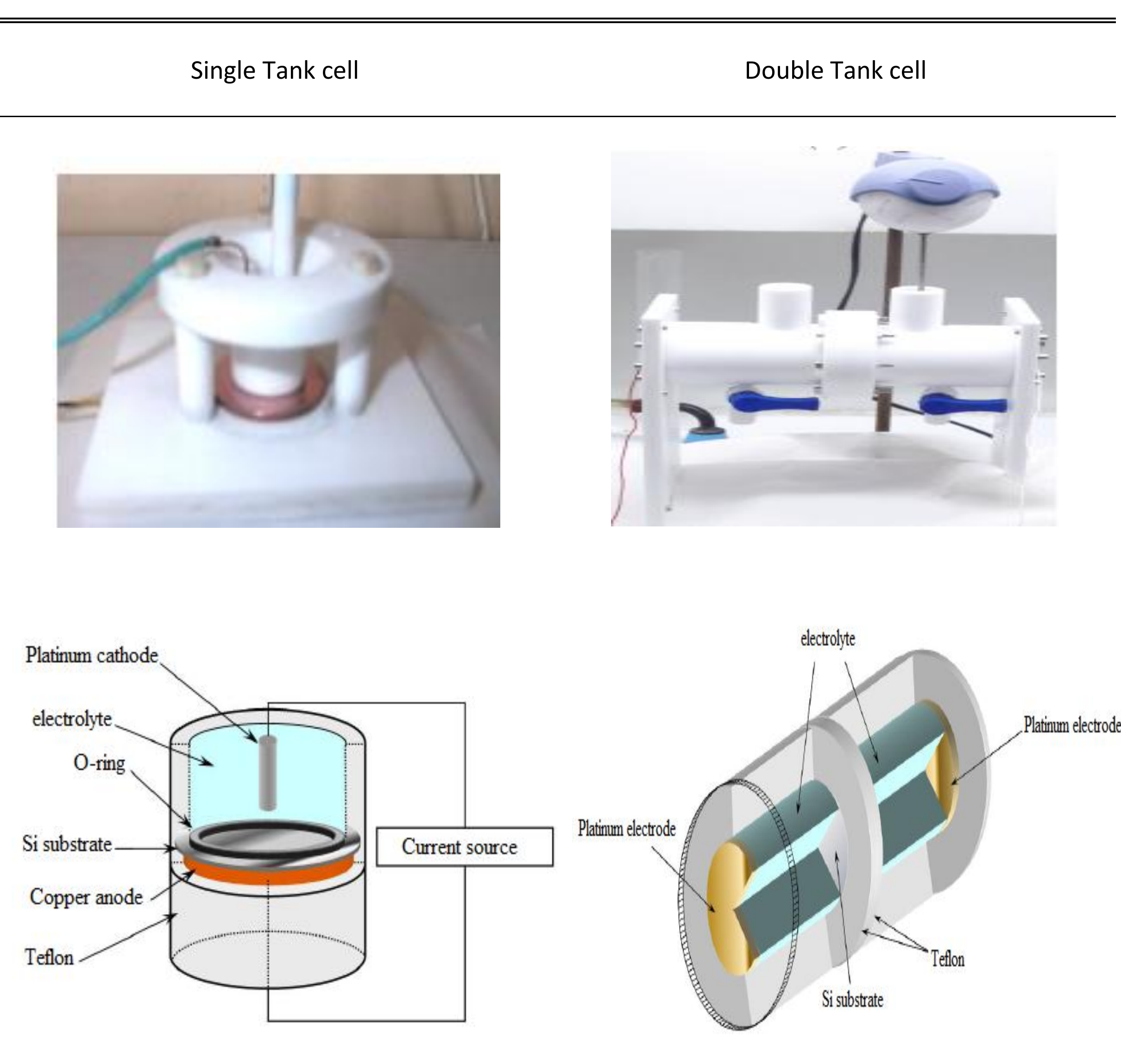


Figure 7 Anodization cells images and their schematic cross sectional views

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

The cell body is made of highly HF-resistant polymer which is polytetrafluoroethylene (PTFE), commercially well known by the brand name Teflon. The simplest cell, shown on the left of the figure, is the single tank cell also known as the O-ring cell. In such a configuration, the silicon wafer serves as the anode and the cathode is made of platinum or any HF-inert and conducting material (gold, carbon plate, highly doped silicon wafer…). The silicon sample is putted on a metal plate and pressed against the O-ring with screws in order to seal the cell. Only the front side is exposed to the anodizing electrolyte. The position and geometry of the cathode is crucial for the resulting etching structure. It should be of the same size, in-plane orientation and far enough with respect to the anode in order to ensure a homogeneous potential distribution along the silicon surface and thereby uniform porous layer with a good control of both thickness and porosity. However, at a distance very close to the O-ring (of about the wafer thickness), the current flow is not normal to the surface and the current density is therefore slightly enhanced there. This effect has been found to be responsible for thickness inhomogeneities of porous layers. To reduce such inhomogeneities, the O-ring should be of a diameter in excess of a centimeter and its section thickness as small as possible [Leh02].

The second type of cell, used on a large scale fabrication, is the double tank cell in which the metal plate of the O-ring cell is replaced by an electrolytic back-side contact. This type of set up consists of two half-cells separated by the silicon wafer and in which symmetrical and large platinum electrodes are immersed in HF. In other words, HF is used for both anodization of the polished side of silicon and as a back contact. Consequently, no metallization of the back-side is required and the as-anodized wafer can then be used for further technological processes, particularly heating and chemical treatment, without any risk of metallic contamination. In addition, the uniformity of the layers obtained with this system is sufficiently good and comparable to that obtained with a single-tank cell. However, the drawback is that the potential of the wafer is not known leading the current-voltage investigation of silicon during anodization impossible.

There are also other cell designs which are developed in order to fulfill different specific requirements or avoid some problems encountered in previously described cells. One can mention for example cells with electrolyte circulation using PTFE pumps and valves which can reduce HF concentration gradients at the electrode surface and allow a better temperature control. Cells with rotating disk anode are also designed to provide stirring of the

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

electrolyte for bubble removal or for enhancement of the reaction rates. They are essentially conceived to study kinetic processes [Leh02].

Furthermore, for the anodization of n-type silicon, an added illumination set up (with the energy light above the bandgap of the silicon) is used. In this case, some points related to the intensity and the direction (backside or topside) of illumination have to be taken into consideration for homogenous and controllable porous layer. A high intensity is needed to generate the sufficient amount of holes necessary for silicon dissolution, the back side contact must be at the edge of the sample for back side illumination, and the cell must have a light transparent window for front side illumination. Many light sources of different properties can be used depending on the desired application. For example, filament lamps with a broad spectrum and high intensity are useful if a whole wafer has to be illuminated homogeneously but the high IR intensity heats up the silicon. Sodium lamps show a better light to heat ratio but tuning of the light intensity is a major problem. Lasers are favorable if local illumination with monochromatic light is desirable and the intensity can be regulated very fast and over a wide range [Leh02]. In any case, the set up of these cells is quite complex and shows experimental inflexibility.

3.1.2 Electrolyte

Electrolytes commonly used for electrochemical processing of silicon can be categorized according to their constituents or according to their pH. Aqueous electrolytes dominate the electrochemical processing of silicon rather than organic ones. Aqueous electrolytes of high pH etch silicon even at open circuit potential conditions. The etch rate can be enhanced or decreased by application of anodic or cathodic potentials, respectively. While the use of high pH electrolytes in electrochemical applications is limited mainly in the field of etch-stop techniques, at low pH silicon is quite inert because under anodic potentials a thin passivating oxide film is formed. This oxide film can only be dissolved if HF is present. The dissolution rate of bulk Si in HF at open circuit potential, however, is negligible and an anodic bias is required for dissolution. These special properties of HF account for its prominent position among all electrolytes for silicon dissolution.

Pure HF is liquid in nature and has a melting point of -83.36 °C and a boiling point of 19.46 °C at ambient pressure. The electrical resistivity of HF in water at 0 °C is lower than 2 Ωcm for concentrations below 50% wt. and it has been found to fit [Leh02]

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

$$\rho\ (\Omega cm) = \frac{1}{0.0104\ c}$$

where c is the concentration of HF in % wt.

It must be emphasized that aqueous solutions of HF are usually not prepared from pure HF and water, but by dilution from commercially available aqueous solutions of higher concentration, e.g. 50% wt. of HF in our case.

However, when purely aqueous HF solutions are used for PS formation, there is evolution of hydrogen bubbles that stick to the silicon surface and prevents the progress of the etching process inducing lateral and in-depth inhomogeneity. One of the most appropriate means to overcome this problem and readily eliminate these bubbles is to add a surfactant agent to the HF solution. The most widely used surfactant is absolute ethanol (or methanol). Mirasol or acetic acid can be also used as wetting agents. In fact, due to wettability and capillary phenomena, ethanoic HF solution completely infiltrates the pores while a purely aqueous solution does not leading to the reduction of HF concentration inside pores especially at tips, where the dissolution reaction basically takes place. This slows down the etching process resulting in interface roughness and thickness inhomogeneity. A simple experiment has shown that a drop of ethanol putted on the top surface of a free standing PS film infiltrates the pores and crosses the layer while a drop of pure water remains on the surface even for a long period of time [Via03].

3.1.3 Current density

At constant HF concentration, depending on the magnitude of the applied current density, three regimes of electrochemical anodization can be distinguiched: PS formation, electropolishing and transition regime.

3.1.3.1 Anodic dissolution regimes

PS formation regime is favored at high HF concentrations and low current densities; a concentration of 15 to 40% wt. of HF and a current density of 1 to 100 mA/cm^2 are standard for PS fabrication [Spl01]. The electropolishing regime, where the silicon surface retains a relatively smooth and planar morphology after it has been covered by an oxide layer, is favored at low HF concentrations and high current densities. The intermediate regime called

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

as transition regime is a competition between pore formation and electropolishing for control over the surface morphology. The resulting structure within this region is generally porous in nature but the pore diameters increase rapidly as the electropolishing current density is approached [Smi92]. This region is exploited for example to produce localized silicon nanocrystals on the surface [Aya09].

Figure 8 shows a topological distribution map for the different regions of silicon dissolution as a function of current density and HF concentration.

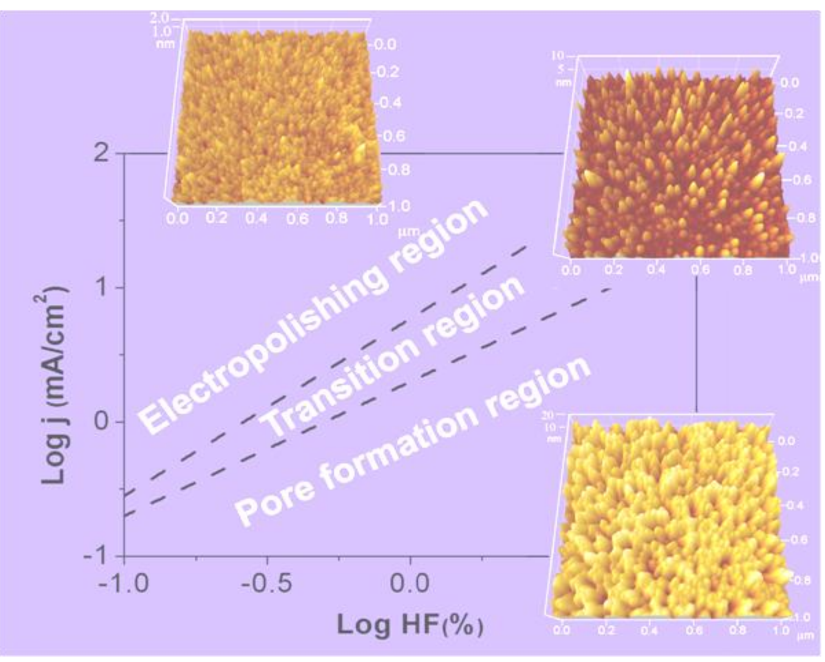


Figure 8 Topological log(j) vs. log(%HF) mapping of the pore formation, transition and electropolishing regions of silicon [Nyc06]

3.1.3.2 Dissolution chemistry

The mechanisms of silicon dissolution can be correlated with the magnitude of current density meaning the rate of hole supply. Different models have been proposed in literature to describe the dissolution chemistries of silicon. Among them, Lehmann and Gösele [Leh91] have predicted the following reaction model shown in Figure 9.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Figure 9 Schematic representation of the dissolution mechanism of silicon in HF proposed by Lehmann and Gösele [Leh91]

For low anodic current densities (below electropolishing current densities), a hole capture from the bulk to the silicon/electrolyte interface and subsequent electron injection lead to the divalent dissolution of one silicon atom and thus to PS formation. One molecule of hydrogen is also generated. This mechanism is supported by the observed dissolution valence[5] of two and the IR spectroscopy which confirms the presence of Si-H surface bonds during PS formation [Leh02].

If the current is increased allowing additional holes to reach the surface silicon atoms, a tetravalent (four exchanged holes) electrochemical dissolution of a single silicon atom occurs now leading to the passivation of the silicon electrode with an anodic oxide which will be chemically dissolved in HF. In fact, it is more likely that hydride (Si-H) coverage during PS formation inhibits oxide formation and thereby preferentially promotes a divalent charge transfer mechanism and pore formation over the formation of surface oxide and electropolishing [Smi92].

---

[5] The dissolution valence of the electrochemical reaction is the ratio of exchanged carriers per dissolved silicon atom. It can be calculated according to: $v = \frac{It \times e}{\Delta m / m_{Si}}$ where I is the applied current, t the anodization time, e the elementary charge, Δm the corresponding weight loss of the sample measured gravimetrically and m_{Si} the atomic mass of silicon.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

3.1.4 Other experimental considerations

Extra factors have to be taken into account in the anodization experiment in order to ensure a more in-depth homogeneous PS layer (same pore diameter and constant layer thickness over the electrode area) and to obtain reproducible results (a better control of porosity and thickness from run to run) especially if deep pores are to be etched.

For example, it is usually advisable to cover the cell to prevent any solvent evaporation which might change the concentration of HF and to integrate a mechanical stirrer in open cell designs or to use an ultrasonic cleaner [Ohw95,Tao05] to accelerate the release of hydrogen bubbles generated during the anodic reaction. In addition, the DC constant current density commonly used for PS formation can be replaced by a pulsed current mode [Hou96,Pop05]. In fact, during the period of pause of anodic current, the bubbles desorption and the HF species regeneration inside pores will occur, which may avoid any decrease of local concentration of HF there and possibly maintain an almost constant etch rate [Tho96].

Moreover, for some applications, control of the temperature is essential and so a heat exchanger system should be part of the experiment apparatus. It has been found [Leh02] for example that the electropolishing current density versus temperature variation follows a typical Arrhenius-type behavior with an activation energy of 0.345 eV for p-type silicon anodized in 1 to 10% wt. of HF. Guillermain [Gui07] has also revealed that room temperature is not the best choice for a good homogeneity of PS layer. At low temperature (-40 °C for example) the electrolyte viscosity increases which yields to a better wettability and easier removal of hydrogen gas. Furthermore, decreasing temperature lowers the etching rate (etch rate at -40 °C is almost 30 to 100 times less than that at room temperature for a same porosity) and thus enables not only a precise control of thickness but also a good homogeneity of the porous layer as the electrolyte has the time to regenerate. Setzu et al. [Set98] have reported the important decrease of the interface roughness with reducing temperature concluding that it is a good way to obtain high quality porous silicon from the points of view of both roughness and structure.

3.2. Structural properties of PS

All the parameters that characterize a PS layer such as porosity, thickness and pore diameter are strongly dependent on the anodization conditions discussed before. We try to

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

present in this section an overview of the most important parameters with highlighting this dependence and mentioning the way they can be characterized.

3.2.1 Microstructure

PS shows various textures or forms of appearance which are mainly determined by the type and the doping level of silicon. Typical pore dimensions can vary from the micrometer range down to few nanometers and morphologies from spong-like to perfect-cylindrical [Fol02]. Although its complicated structure with asymmetric crystal lattice, it should be cautioned that the silicon remaining between pores retains its original crystallinity [Bar84] (i.e. it remains single crystalline with the same orientation as the substrate) indicating that pore formation occurs by a direct dissolution of the bulk material, and not by some redeposition or restructuring process.

In literature, PS is generally defined regarding the geometry of pores (i.e. the average pore diameter and average distance between pores) and one can thus distinguish macroporous, mesoporous and nanoporous silicon. The Table 5 below summarizes the different morphologies encountered under standard anodization conditions with varying the initial silicon substrate. Note for example that macroporous can also be obtained from low doped p-type silicon [Leh99,Pon98] by changing the electrolyte composition (HF containing acetonitrile can be used).

The microstructure can be investigated by electron microscopy observations (SEM or TEM: scanning or transmission electron microscopy) or with the analysis of gas adsorption isotherms which is an extensively used technique for extracting the crystallites and pores size distribution [Her87]. The micro-Raman spectroscopy [Bru97,Isl01] or X-ray measurements [Bel96,Leh93] could be also used to determine the size distribution of pores.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Table 5 Description of different PS morphologies showing the dependence on the type and the level of silicon substrate

silicon substrate	resulting PS	microstructure
p+ ($\rho < 50$ mΩcm) n+[6]	mesoporous	long voids perpendicular to the surface pore diameter: tens of nanometer
p n (under illumination)	nanoporous	isotropic microstructure: random arrays and small holes pore diameter: few nanometers
n (in the dark)	macroporous	anisotropic microstructure: cylindrical pores parallel to each other with a small branching density and very small porosity pore diameter: 0.1-1µm

Figure 10 shows some examples of PS layers obtained at different anodization conditions demonstrating the variety of morphologies found in PS. Furthermore, it should be noted that for low doped n-type silicon, the crystallographic orientation seems to have a significant effect on the morphology of the porous layer [Fol02,Lev93]. The resulting macropores are not necessarily perpendicular to the surface as it can be expected that they grow directly towards the source of the holes. It has been shown [Ron99] that the growth direction of macropores was found to be <100> and <113> and the final morphology is thus describable as a main pore in one of this two directions with side pores or branches in some of the other directions (Figure 10.d). Although a detailed understanding of crystallographic orientation dependence of pore growth in silicon is still elusive, it may be beneficial for some applications in an indirect way.

[6] It should be noted that in the case of highly doped n-type Si anodized in the dark, Williams et al. [Wil97] found that the porous layer consists of two distinctive layers: an upper mesporous and a lower macroporous.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

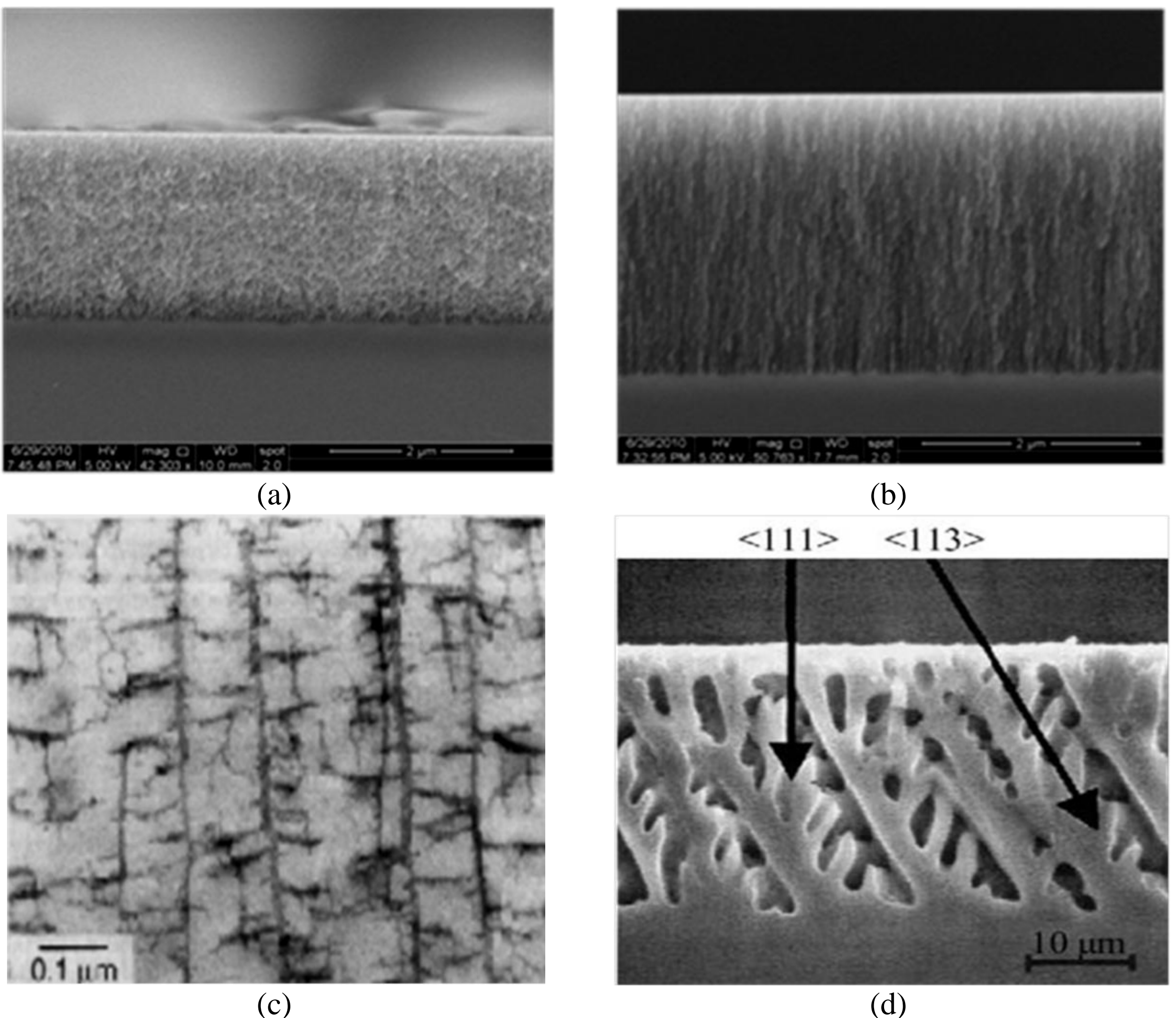


Figure 10 SEM cross sectional view of PS layers of different morphologies: (a) nanoporous, (b) mesoporous, (c) macroporous after [Smi92] (substrate orientation is <100>) and (d) substrate orientation is <111> after [Fol02]

3.2.2 Specific surface area

The surface area of a PS layer commonly known as the specific surface is defined as the accessible (or detectable) area of solid surface per unit mass or volume of material [Roq94]. It is determined either by gas adsorption measurements [Bom88] or just by comparing PS etch rate in HF with that of bulk silicon [Hal94].

The specific surface mainly depends on the texture of the porous layer: porous films formed on n+ or p+ substrates exhibit specific surfaces in the range of 200-250 m^2/cm^3, whereas films formed on lightly doped p substrates have a much higher surface in the order of

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

600 m^2/cm^3, attesting to the much finer texture of this material[7] [Bom88]. Halimaoui [Hal94] had studied the variation of the surface area with porosity and showed that it decreases from 900 m^2/cm^3 for 52% porosity samples to about 50 m^2/cm^3 for 95% porosity layers.

3.2.3 Porosity

Porosity P is defined as the volume fraction of void within the PS layer:

$$P = \frac{V_{void}}{V_{PS}} = \frac{V_{PS} - V_{Si}}{V_{PS}}$$

where V_{PS} is the total volume of the porous layer and V_{Si} is the volume of remaining silicon after electrochemical dissolution. Obtainable porosities may range from 30% up to 90% [Nyc06].

Porosity can be easily determined gravimetrically or optically. The former method which is usually used in literature is described below, whereas the latter which is based on the determination of the refractive index of PS layer from its FTIR (Fourier transform infrared) spectra response and which is mostly utilized in our work will be presented in chapter 3.

For the gravimetrical technique, the sample is first weighed before anodization, then just after anodization to determine the silicon dissolved mass and finally after removal of the whole porous layer in 1% wt. KOH or NaOH solution (a high selective etchant of PS relatively to bulk Si). Porosity can then be calculated using the following equation:

$$P = \frac{m_1 - m_2}{m_1 - m_3}$$

where m_1 is the wafer weight before anodization, m_2 the wafer weight just after anodization and m_3 the wafer weight after dissolution of PS layer in NaOH or KOH aqueous solution.

It is commonly known that porosity increases with increasing current density and decreases with increasing HF concentration as illustrated in Figure 12. However, at lower current densities, it had been found [Nyc06,Can97] that a sharp increase in porosity is observed when the current density decreases as marked by dashed lines. This has been

---

[7] The specific surface is generally expressed in literature in m^2/cm^3. But, with a simple conversion, one can wisely note that 600 m^2/cm^3 = 0.6 nm^{-1}, a value that approaches the specific surface of one single silicon atom (Si atomic radius is 110 pm)!!!

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

attributed according to [Nyc06] to the extra pure chemical dissolution of the layer as the time required to form a given thickness is much higher at low current density. Halimaoui [Can97] has however shown that the difference in anodization time is considered as small and should lead to only a difference of a few percent in porosity. He has suggested from specific surface areas measurements of layers obtained at high and low current densities that the high value of porosity obtained at low current density is due to a much finer microstructure.

In addition, it must be emphasized that porosity is much higher for the thicker layer due to the effect of the chemical dissolution. In fact, the thicker the layer is, the longer the anodization time is and thus the much higher the mass of chemically dissolved silicon from the porous layer is. This effect is more pronounced for porous layers obtained from lightly doped wafers due to their higher specific surface area compared to that of layers obtained from low resistivity silicon.

Furthermore, it is worth mentioning that porosity is sensitive to the substrate doping concentration. For given anodization conditions (current density and HF concentration), nanoporous layers obtained for example with lightly p-doped silicon are commonly found to be of higher porosity than mesporous or macroporous layers [Leh00].

3.2.4 Growth rate

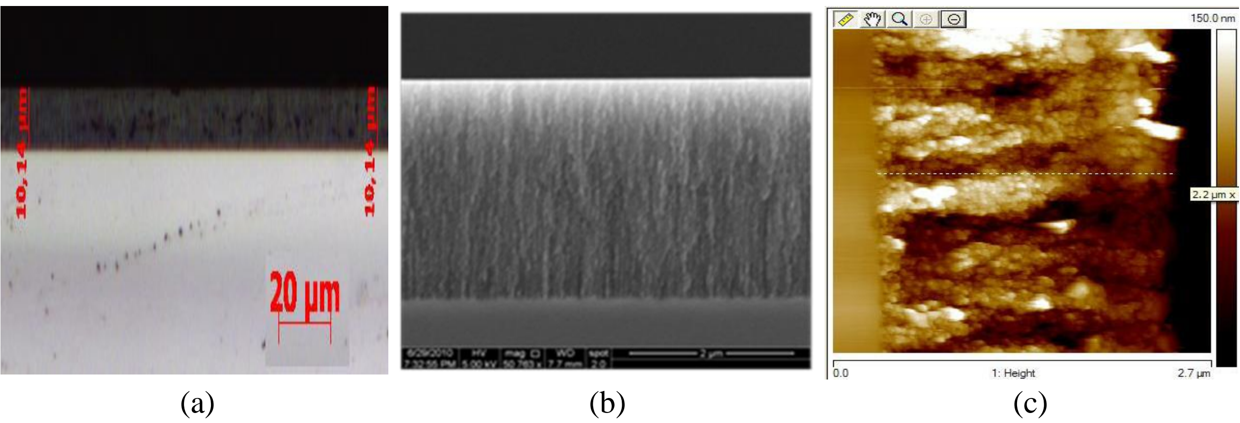
The thickness of a porous layer can be determined by weight measurements as well according to:

$$P = \frac{m_1 - m_3}{S \times D}$$

where S is the wafer area exposed to HF during anodization and D the density of bulk silicon.

It can be also directly determined from microscopic observations as shown in Figure 11. The atomic force microscopy (AFM) image is obtained after beveling the sample using a Mecapol P300 polisher. On beveled samples, the PS layer is artificially magnified by geometrical means which allows the characterization of very small layer thicknesses. A support for polishing with an angle of 5 44' is used here corresponding to an amplification factor of 10 [Lig10].

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



(a) (b) (c)

Figure 11 Different techniques allowing the measurement of PS layer thickness: (a) optical microscopy (magnification x100), (b) SEM and (c) AFM after sample beveling

Other techniques can also be used for thickness determination such as ellipsometry (especially for thin layers) or step measurement but they need further work on modelling for the prior and sample preparation for the latter [Via03].

From measured thicknesses at different anodization times, one calculates the growth rate of PS. As shown in Figure 12, for mesoporous silicon (highly p- and n-type doped substrates), the growth rate is first constant with depth and shows an almost linear dependence as a function of anodization current density. This is in stark contrast to macropore formation (for lightly doped n-type silicon), where the growth rate has been found [Leh02] to be constant with the applied current density but it decreases with decreasing HF concentration. It has been also noticeable that pore growth rate shows little dependence on substrate doping concentration expect for highly and moderate doped n-type silicon (for mesoporous formation) where it increases monotonically with decreasing doping density approaching the constant macro PS growth rate [Leh00].

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

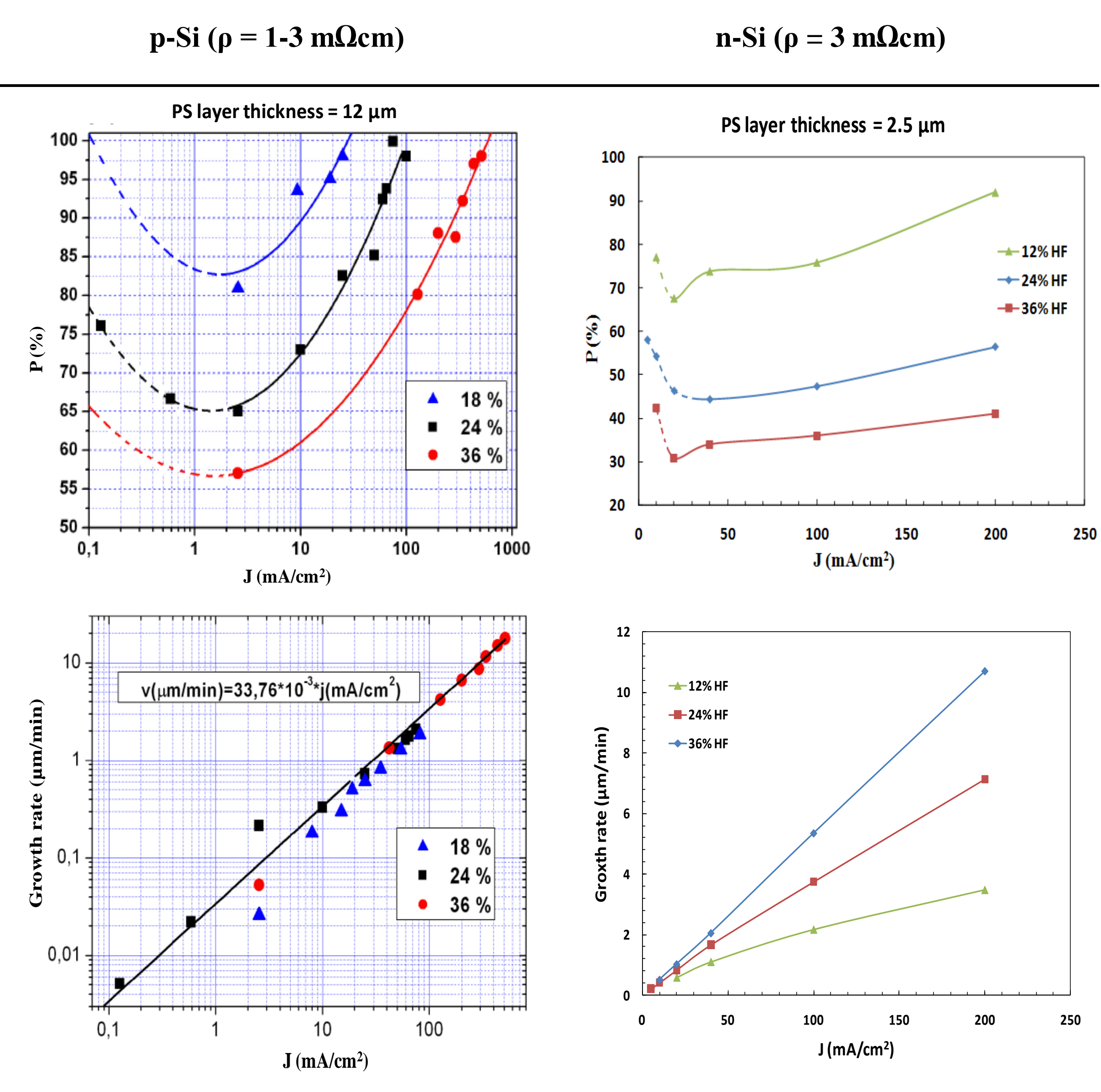


Figure 12 PS calibration curves obtained from anodized highly p- (after data from [Nyc06]) and n-type silicon substrates

3.3. PS applications

Besides its microelectronic applications (electrical isolation, buffer subsurface layer for epitaxial growth…), PS has many other kinds of interesting applications in various fields. A brief review of some important ones is provided in this section.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

3.3.1 Optical-optoelectronic applications

In contrast to conventional dielectric materials, the refractive index of PS can be varied continuously over a wide range just by varying the porosity. This allows the realization of passive optical components like interference filters. One can mention for example Bragg reflectors, Fabry-Perot filters and Rugate filters which are fabricated by alternating PS layers of different refractive indexes. These interference filters can be used as independent optical components or integrated in silicon optoelectronic devices. As example, the Bragg reflectors and Fabry-Perot filters are used as color-selective layers in color-sensitive silicon photodetectors [Can97].

Furthermore, since the discovery of intense visible luminescence of PS (a property not possessed by bulk silicon), great efforts have been devoted to integrate the material in optoelectronic circuits. The benefits come from increased reliability, the compatibility with conventional silicon fabrication technologies and mainly the cost reduction compared to III-V compound semiconductors-based circuits. Many optoelectronic devices based on PS have been developed such as light emitting devices (LEDs), integrated waveguides and photodetectors.

3.3.2 Sensor applications

The high surface area of PS has led to perform gas sensors. In fact, a variation in PS properties upon absorption of chemical species at the large internal surface is exploited for sensing. Several different transducers have been proposed, based on changes in capacitance, resistance, or also the photoluminescence properties of PS. Sensitivity to vapors of water, ammonia, and various organic compounds have been reported, and discrimination between different molecules has been achieved. For example, the capacitance variation is explained by a change in the dielectric constant of the matrix while a decrease in resistivity is attributed to detrapping of charge carriers from surface states [Can97,Leh02].

3.3.3 Micromachining applications

The high chemical reactivity of PS to KOH solutions (high etch rate ratio to bulk silicon) makes this material very attractive for use as sacrificial layer for microelectromechanical systems (MEMS) applications. Several fabrication processes, in which PS is selectively removed underneath a free standing silicon membrane, have been

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

successfully approved in the fabrication of mechanical sensors such as a capacitive accelerometer or a thermal sensor for radiation (bolometer).

Moreover, as PS is found to be a biocompatible and biodegradable material, it has been used for medical and biological applications such as for penicillin sensing or biochips used in genomics. It can be also exploited as hydrogen source for portable device energy supply.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Conclusion

The chapter has offered the opportunity to remind some important dates and features that marked the history of microelectronics. After reporting some salient challenges arisen from technological limitations in this field, it has introduced the context of our research work which relies on the understanding of the FIPOS process as an alternative to the STI process for electrical isolation in CMOS circuits.

This leads us to make a general introduction of PS pointing out the increasing interest to this material. We have then presented the experimental set up allowing PS elaboration with comparing it to that affordable in our laboratory. In addition, we have reviewed the different characterization procedures of PS and we have established calibration curves of the porosity and the PS etching rate as a function of electrochemical anodization parameters, which will be useful for the following chapters, mainly chapter 3.

Finally, it can be said that the chapter did not only present the state of the art but it has also given a preliminary study of PS formation which will be considered in more details in the next chapter.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Chapter 2: Investigation of current-voltage characteristics of silicon in HF solution

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Introduction

All porous silicon (PS) applications require a complete understanding of the formation of this material allowing hence a perfect control of its properties with the anodization parameters (silicon doping concentration, current density, HF concentration…). The chapter emphasizes one of the most promising properties which is the dependence of PS formation toward silicon doping concentration. For this, a detailed experimental analysis of current-potential I-V characteristics measured on n- and p-type silicon electrodes during PS formation by electrochemical anodization is presented. It allows us first to understand the correlation existing between the anodization potential and the silicon doping concentration which explains the property of PS formation dependence with doping level, and second to make a calibration of our experimental set up which is necessary for further PS applications investigated in this work.

In addition, the chapter describes a first application emerged from this property which deals with silicon doping profiling by electrochemical anodization and it also discusses its limitations.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

1. Experimental set up

This section deals with the experimental set up with special emphasis on some points that are extremely important when current-voltage characteristics of silicon in hydrofluoric acid (HF) solution are measured.

1.1. Experimental conditions

Anodization of silicon samples was performed in a single-tank Teflon cell (presented in Figure 6 of chapter 1), in the dark, at room temperature and without stirring. It was verified that stirring has no important effect on our experimental current-potential data but it becomes necessary when in-depth homogeneity of a thick porous layer is in question. The silicon sample surface area in contact with the electrolyte was 0.5 cm^2 (0.8 cm diameter) and the counter electrode was a cylindrical platinum grid, parallel and far enough to the silicon electrode to ensure uniform anodic current distribution.

The anodizing solutions are prepared from a 50% wt. HF solution, by dilution in absolute ethanol as a wetting agent. The concentration in percent given in the text and often used in the literature corresponds neither to a percentage in weight nor in volume but is a mixture of the two according to this expression:

$$HF\ (\%) = \frac{50\% \times \mathrm{V_{HF}}}{\mathrm{V_{HF}} + \mathrm{V_{C_2H_6O}}}$$

where V_{HF} is the volume of the 50% wt. HF solution and $V_{C_2H_6O}$ is the volume of the absolute ethanol solution. The Table 1 below gives the exact composition of some ethanoic HF solutions used in this work.

Table 1 Composition of the ethanoic HF solutions

HF concentration	Volume of 50% wt. HF	Volume of added ethanol
5%	1	9
15%	3	7
25%	1	1
35%	7	3

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

1.2. Electrical connection

Some factors have to be taken into consideration when potentials are measured in electrolytes as that is not as easy as it is for solid state devices. To take potentiostatic (i.e. scanning of the potential) current-voltage I-V characteristics of the silicon electrode, a simple circuit with just only two electrodes will not be sufficient, even if we bring closer the platinium counter electrode to the silicon working electrode in order to minimize the potential drop caused by ohmic losses due to the electrolyte resistivity. In such configuration, a Helmholtz layer is also formed on the platinum electrode and can significantly modify its potential [Bar80, Shy96]. So, the I-V characteristics recorded are in some way distorted as they cannot give the correct potential distribution at the silicon electrode/electrolyte interface. For this reason, a third electrode, which is an Ag/AgCl reference electrode, is used; the current is supplied between the working and the counter electrode and the potential of the working electrode is measured against the reference electrode using a Keithley 2602 dual channel sourcemeter which is controlled by a Labview program through GPIB (general purpose interface bus) line. We found ourselves with a final electrical connection, as illustrated in Figure 1, similar to the four-point probe used for solid state devices or also to a potontiostat used for electrochemical experiments. The difference comparing to the latter case is that for our system the applied voltage between the working and the counter electrode is not controlled by the voltage measured between the working and the reference electrode.

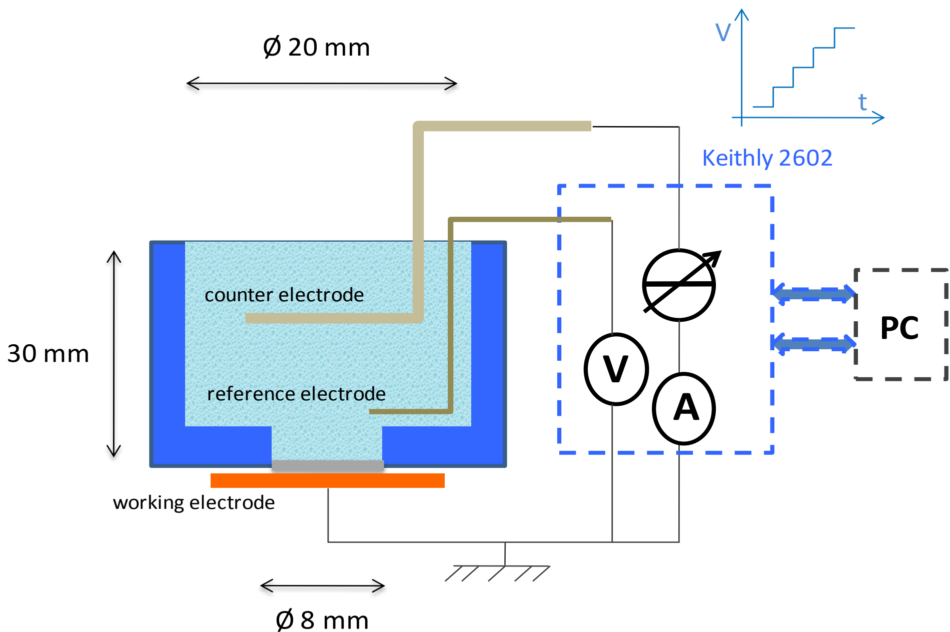


Figure 1 Electrical connection of the electrochemical cell

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Taking advantage of its small dimension and its resistivity to HF degradation, the reference electrode is maintained close to the anodized silicon surface. So, there is no need for ohmic drop correction due to the electrolyte resistivity; Figure 2 shows I-V characteristics for different position of this electrode relative to the working electrode highlighting the effect of the electrolyte resistance that may hinder the specific behavior of the studied electrochemical system. It must be kept in mind that a few tenths of an ohm on this resistance can correspond to potential of several tens of millivolts at current densities of about 100 mA/cm^2. The conductivity of the solution may be improved by adding salts e.g. NH_4Cl but it may influence the etching process in unpredictable ways, too [Fol02].

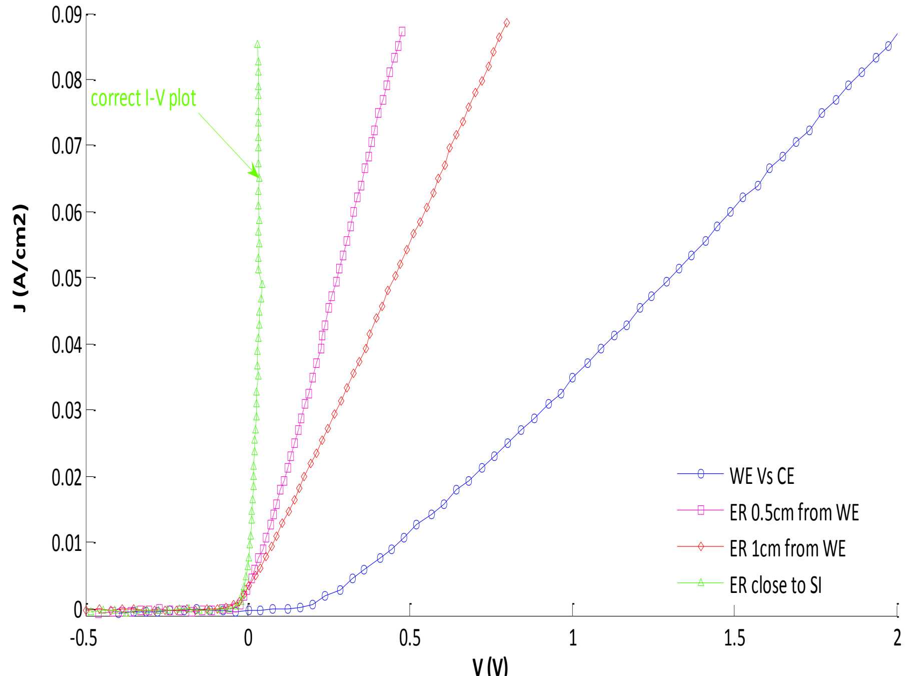


Figure 2 I-V plots of the working electrode WE vs. the reference electrode RE for different positions of the RE & I-V plot of the WE Vs the counter electrode CE (p-type silicon sample with doping concentration of 5 x 10^{18} cm^{-3} is used)

All potentials values and the notation V given later in the text are referred to the working electrode potential vs. the reference electrode.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

1.3. Sample preparation – Back side ohmic contact

As the silicon/electrolyte interface is our focus of study, the back side contact of the silicon sample must be ohmic when taking current-voltage measurements since just putting silicon on a metal plate is mostly not good enough, especially for low doped samples (i.e. the contact resistance should be negligible that can pass the current with a small voltage drop compared to the voltage across the studied region). This is achieved by aluminum vacuum deposition followed by a rapid thermal annealing at 700 °C under nitrogen atmosphere. Before that, samples are etched in diluted HF solution to remove the reminder of the native oxide layer and rinsed in distilled water. In the case of high resistivity silicon wafer, highly boron/phosphorous doping on the back side was performed, too. Rubbing InGa eutectic on the back side, together with some scratching, usually suffices but it is not practical in our case as it contaminates the cell.

The Table 2 shows the contact resistivity measured with the transmission line method (TLM) described in appendix A. Presented values would also present the contact resistance for our experiment as the sample surface area is about 1 cm^2. It is obvious that higher is the doping concentration of the back side silicon layer better is the contact resistance. A contact resistance for moderate p-type doping concentration can be acceptable. For n-type silicon, the back side contact is of no great importance since the silicon/Al junction is forward biased during anodization.

Table 2 Contact resistivity measured by TLM for n- and p-type silicon of different doping concentrations

Back side silicon	Contact resistivity ρ_c ($\Omega.cm^2$)
p++ ($N_a = 3.10^{19} cm^{-3}$)	5.10^{-7}
p+ ($N_a = 2.10^{17} cm^{-3}$)	10^{-4}
n++ ($N_d = 2.10^{19} cm^{-3}$)	1
n+ ($N_d = 5.10^{16} cm^{-3}$)	16

1.4. Description of samples

All wafers are Czochralski (Cz) grown, <100> oriented, either boron or phosphorous doped silicon. Two different types of samples are studied, presenting different kinds of

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

doping concentrations. The first type is bulk silicon substrates presenting uniform and homogenous doping densities. Substrates of different doping levels ranging between 10^{15} cm^{-3} and 3.10^{19} cm^{-3} are analyzed. The second type of samples presents a doping profile in depth obtained by either ion implantation or by epitaxial growth. They will be described in more details with giving the corresponding secondary ion mass spectrometry (SIMS) profiles when they will later appear in the text.

The Table 3 below is an overview of all samples used in this chapter.

Table 3 Overview of used samples

	Sample description	
	Bulk substrates (doping concentrations)	Specially designed wafers
p-type	- $N_a = 3.10^{19}$ cm^{-3} - $N_a = 2.10^{18}$ cm^{-3} - $N_a = 2.10^{17}$ cm^{-3} - $N_a = 1.10^{15}$ cm^{-3}	- "p-maya": six p-type layers of different doping concentrations grown over a p-type silicon substrate (staircase doping profile).
n-type	- $N_d = 2.10^{19}$ cm^{-3} - $N_d = 5.10^{18}$ cm^{-3} - $N_d = 2.10^{18}$ cm^{-3} - $N_d = 3.10^{17}$ cm^{-3} - $N_d = 5.10^{16}$ cm^{-3} - $N_d = 1.10^{15}$ cm^{-3}	- samples of different n-doped epitaxial layers grown over a low n-doped silicon substrate - Implanted phosphorous into a low-doped boron wafer. - "n-maya": n-type layers of different doping concentrations grown over a p-type substrate (staircase doping profile).

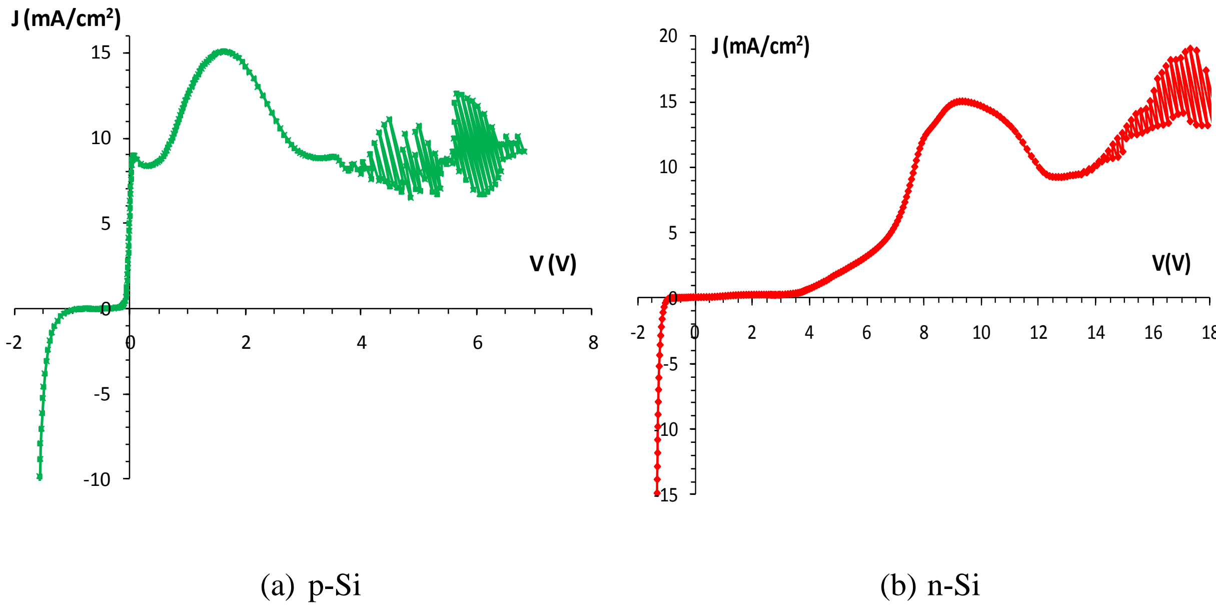
2. General current-voltage characteristics of silicon in HF solution

In this section, we outline the basic features of current-voltage I-V characteristics of p- and n-type silicon in HF solutions and we delegate further analysis about the charge carrier

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

transport and interfacial potential distribution during porous silicon formation to the next sections.

Figure 3 shows the I-V curves for p and n-type silicon in HF which seem to be similar to the classical Schottky diode behavior expected from a semiconductor/electrolyte interface. However, there are some important anomalies attributed to the behavior of silicon in aqueous environment. For example, a much higher reverse bias current than normal Schottky diode expectation is reported which indicates possible surface state contributions. Another anomaly involves the presence of current peaks and oscillations at high anodic overpotentials which is associated with the formation of an anodic surface oxide [Smi92].



(a) p-Si (b) n-Si

Figure 3 I-V characteristics for n- and p-type silicon in HF solution, the doping concentration for p-Si and n-Si samples are 2.10^{18} cm^{-3} and 3.10^{17} cm^{-3}, respectively and the HF concentration is 1%

2.1. Electrochemical regions of the Si/HF system

When a potential is applied to silicon in HF, a measurable current is induced to flow through the system. This current must first change from electronic to ionic charge carriers to pass the silicon/electrolyte interface. One can understand from here that a conversion is needed which is accomplished by means of a specific chemical redox reaction at the silicon interface. The question now is about the nature of carriers involved in this electrochemical reaction.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

2.1.1 Cathaodic polarization

Under cathodic polarizations (negative sign of V) for both n and p types, silicon is normally stable i.e. silicon does not dissolve and the only important cathodic charge transfer reaction observed in the silicon/HF system is liberation of hydrogen gas [Leh02] according to:

$$2\,e- + 2\,H^{+} \longrightarrow 2\,H_2$$

It has been shown that the rate of hydrogen evolution is strongly dependent on the excess of electron concentration at the silicon electrode surface and not on the H^+ concentration in the solution. Therefore, it only occurs at significantly high cathodic potentials for low doped p-type silicon where breakdown process is supposed to provide electrons required for the reaction.

2.1.2 Anodic polarization

Since it is only under anodic polarization (forward-biased Schottky for p-type and reverse-biased Schottky for n-type) that silicon dissolution occurs, one can note that holes are certainly necessary for initiating the process. The details about the chemistry dissolution reactions have been already given in chapter 1. In the case of n-type silicon, where holes are the minority carriers, the dissolution of silicon can be observed either at high anodic voltages or under illumination where a hole/electron pairs can be generated. The measured current in the last case and eventually the dissolution rate will strongly depend on the illumination intensity [Fol02, Leh96]. It has also been mentioned that the I-V curve under illumination at anodic potential regime looks like the one obtained for p-type silicon in the dark.

Now, depending on the magnititude of the anodic potential, different morphologies result: at low anodic potentials PS is formed while at high anodic overpotentials, the silicon surface electropolishes.

The oscillations observed at high anodic potentials, after a current density peak, are attributed to fluctuations in the thickness of the oxide formed at the silicon surface during anodization. In fact, as proposed by Föll [Fol91], under constant current conditions, oxide growth (with a rate faster than its chemical dissolution rate) increases the voltage to maintain current flow until it exceeds the oxide breakdown field strength and halts the oxide formation

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

mechanism. The oxide is then chemically etched back by HF to a reasonable thickness while another electrochemical reaction takes place. The potential also drops during this time returning the system to its original state where the cycle starts again.

The Table 4 below summarizes the electrochemical features discussed above for both p- and n-type silicon.

Table 4 The major electrochemical features of the silicon/HF system

	Cathodic polarization	**Anodic polarization**
p-type Si	- No silicon dissolution - H_2 evolution - Reverse-biased Schottky	- Silicon dissolution: Pore formation at low potentials Electropolishing at high potentials - H_2 evolution - Forward-biased Schottky - Two current peaks: 1st peak indicates electropolishing outset 2nd peak followed by oscillations
n-type Si	- No silicon dissolution - H_2 evolution - Forward-biased Schottky	- Silicon dissolution: Pore formation at low potentials Electropolishing at high potentials - H_2 evolution - Reverse-biased Schottky - Single current peak: oscillations

2.2. Anodic dissolution regions in p-Si and dependence on the anodization parameters

From the Figure 4 which shows the anodic polarization portion of the I-V characteristic of Figure 3.a, one can distinguish more exactly the different dissolution regions of p-type silicon described in section 3.1.3.1 of chapter 1. Region A is the PS formation regime which will be our focus in the next section. Region C which is marked by a first current density maximum (known as the electropolishing current density J_{ep}) and associated with negative impedance corresponds to electropolishing. Region B is the transition region which starts upon a deviation in the I-V curve slope [Smi92].

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

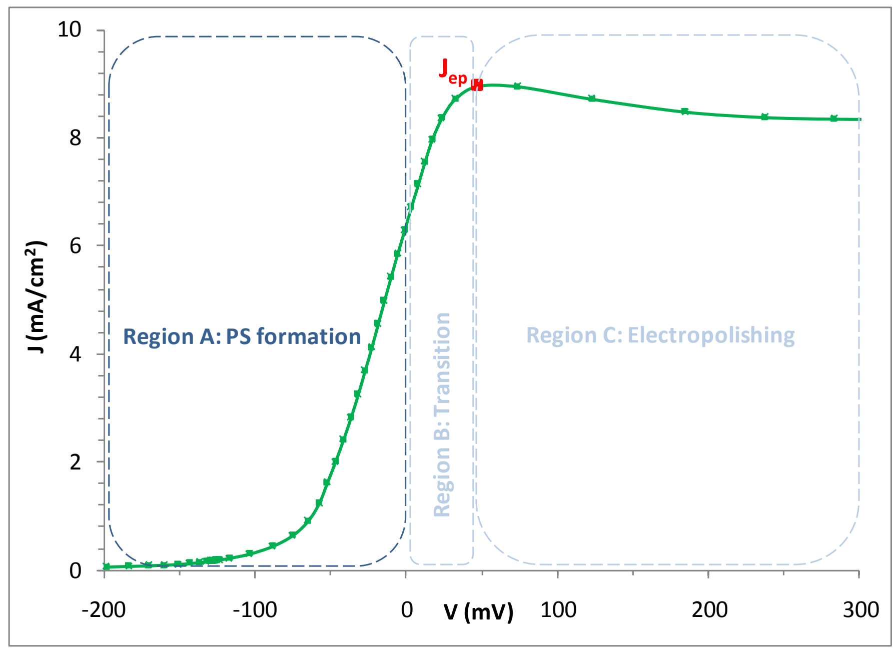


Figure 4 Anodic I-V characteristic of silicon in HF showing the different dissolution regions, J_{ep} is the electropolishing current density

The electropolishing current density J_{ep} depends mostly on the solution composition and little on the substrate [Wij08,Zha89 and Can97] as shown in Figure 5.

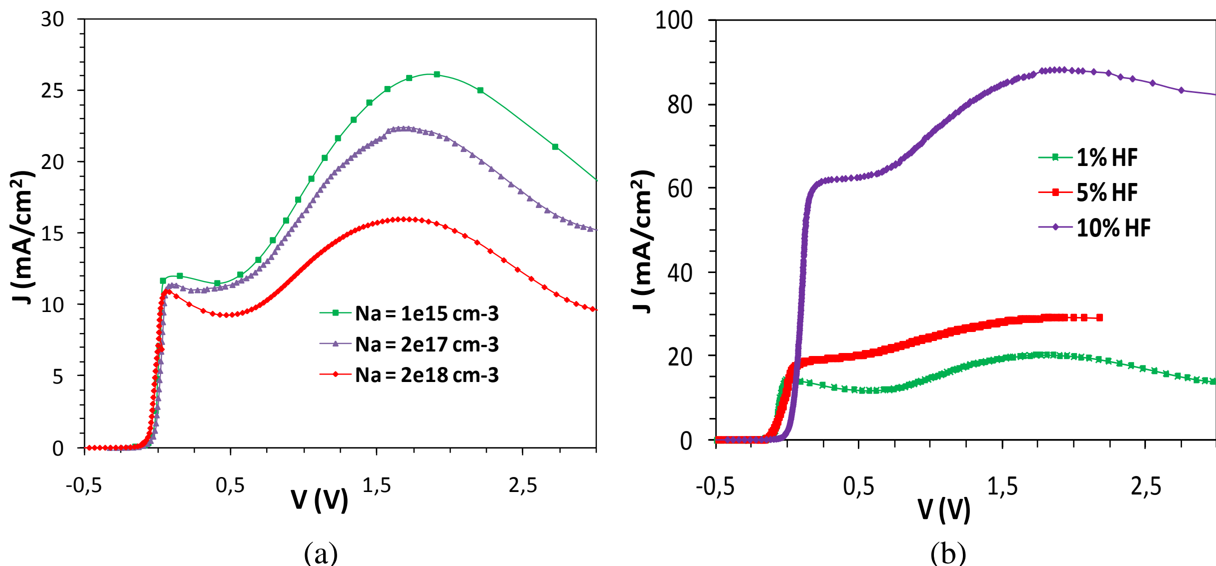


Figure 5 Anodic I-V characteristics for p-type silicon (a) of different doping concentrations in 1% HF, (b) of 2.10^{18} cm^{-3} doping concentration in different HF concentrations

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

From these I-V curves, the well-known topological distribution map for the different regions of silicon dissolution can be plotted as a function of current density and HF concentration as shown in Figure 6.

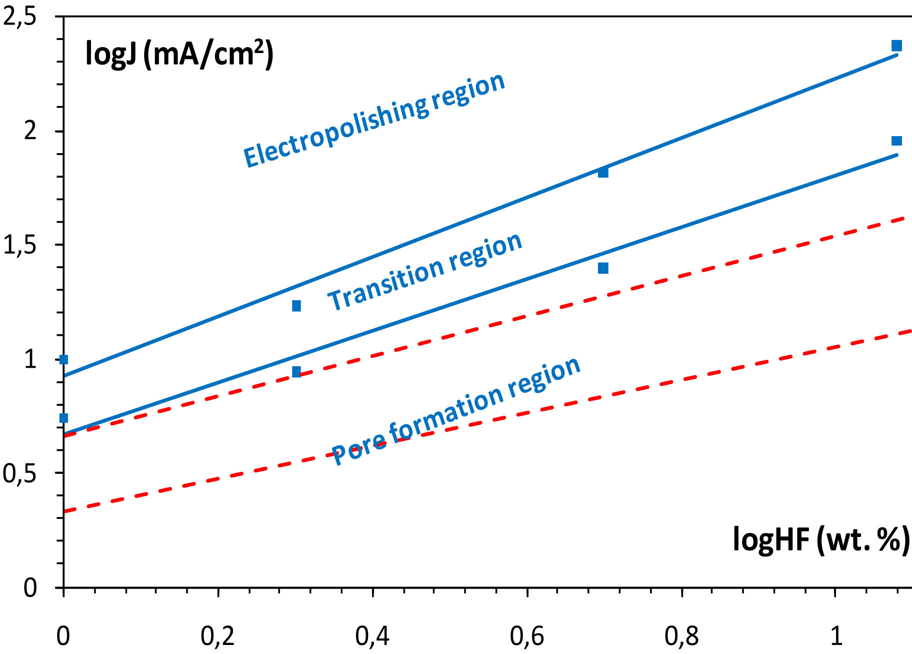


Figure 6 Topological representation log(J)-log(%HF) of the pore formation, transition and electropolishing regions of p-type silicon. The dashed lines are redrawn from results of [Smi92]

It will be a judicious choice to use later a 25% HF concentration when studying the charge exchange mechanism during PS formation so that a relatively high current is obtained before reaching electropolishing regime. For example, an electropolishing current density J_{ep} of 16 mA/cm^2 is reported for 5% HF while it is 600 mA/cm^2 for 25% HF.

3. Charge exchange mechanism during PS formation of p-type silicon

This part is devoted to the analysis of current-voltage I-V characteristics measured on p-type silicon electrode during anodization in the regime of PS formation. It allows us to understand the charge carrier transport mechanism responsible for silicon dissolution and know more about the interfacial potential distribution of the HF/silicon system in that regime.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

It should be mentioned that there are two different manners in literature for studying PS formation mechanism. The first deals with the material structure and it has been investigated by means of high resolution scanning (SEM) and transmission electron (TEM) microcopies in order to explain the distinctive morphologies of PS obtained with different conditions. Lehmann [Leh02] summarizes well the current understanding of the pore formation mechanism under a wide range of morphologies. In our work, we will rather interest in the second manner which deals with electrical characterizations that try to give a model of the charge exchange between silicon and electrolyte during PS formation.

Figure 7 shows typical anodic current-voltage characteristics for p-type silicon substrates of different doping concentrations.

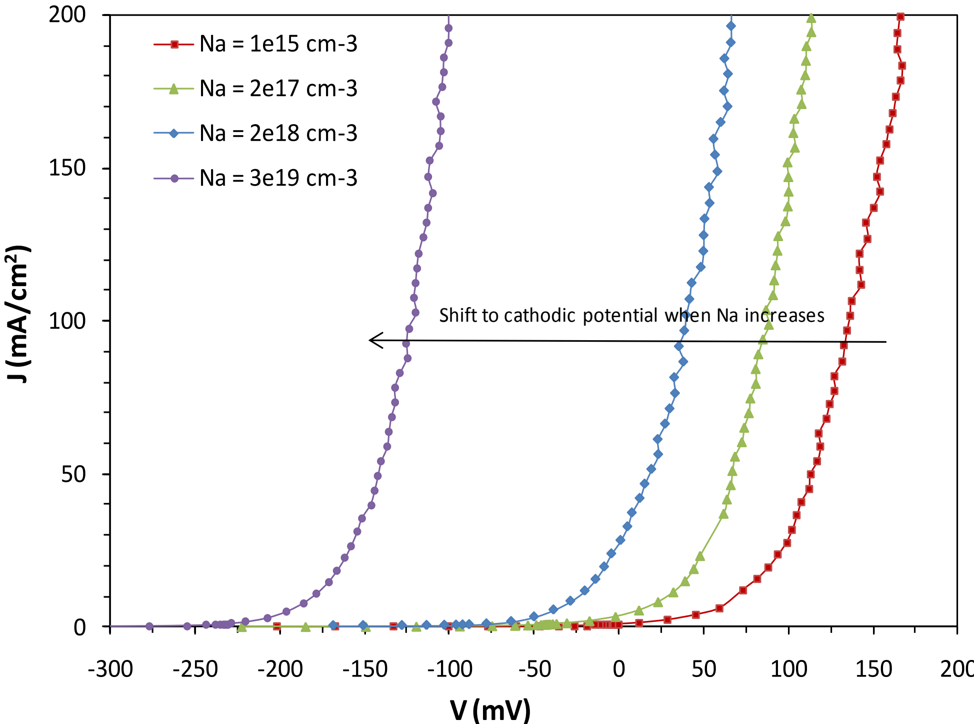


Figure 7 Anodic current-voltage characteristics of p-type silicon in hydrofluoric acid solution for substrates of different acceptor doping concentrations N_a

3.1. The anodization potential is determined at the Si/HF interface

It must be pointed out that successive potential sweeps on the same electrode lead to reproducible I-V characteristics. This suggests that the potential drop in the electrolyte within the PS network can be neglected which means that the anodization potential is not modified

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

by the thickness of the formed PS layer and is only determined by the electrochemical reaction at the silicon electrolyte interface.

The scanning electron microscopy (SEM) graph in Figure 8 also argues with the last assumption showing 5 sub layers which correspond to five successive applied potential sweeps on a silicon sample. In fact, an almost similar thickness between these subs layers gives evidence of a same PS formation rate from one sweep to another and so an independence of the I-V characteristics toward the thickness of the formed porous layer, at least for thickness below 13 µm corresponding to the first five sweeps. In addition, with an approximate calculation, one can verify that the thickness of a sub layer corresponds well to one potential sweep: From an I-V plot, we have measured a current density of [0 to 100 mA/cm^2] relative to an applied voltage of [-0.2 to 2 V]. A step voltage of 40 mV gives 45 levels of applied potential as well as for measured current density J_i. As the sweep delay is 2 s and the etch rate for highly doped p-type silicon according to [Nyc06], is given by

$$\text{v}\ (\mu/\text{min}) = 33.76 \times 10^{-3} \times J(mA/cm^2)$$

one calculates the total thickness h of a sub layer:

$$\text{h} = \sum_{i=1}^{45} 33.76\ \times 10^{-3} \times t \times J_i = 1.125 \times 10^{-3} \times \sum_{i=1}^{45} J_i = 2.8\ \mu m$$

which is close to the measured value shown below.

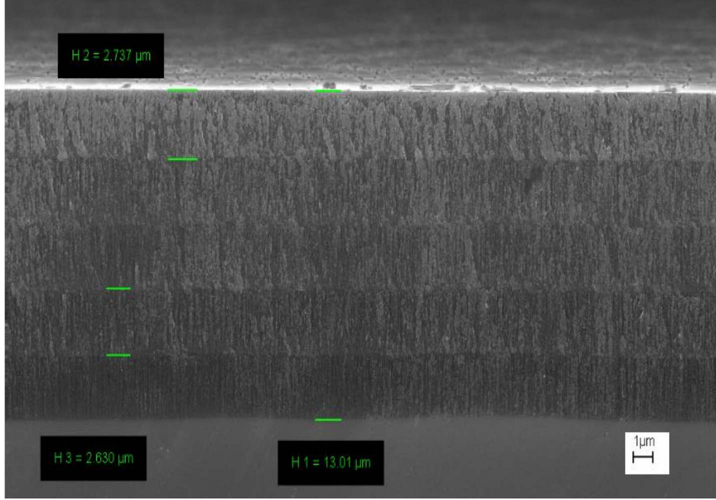


Figure 8 SEM cross-sectional micrograph of PS layer obtained after five successive potential sweeps, silicon doping concentration is 2.10^{18} cm^{-3}

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

3.2. The "Schottky barrier + Helmoltz layer" model

Three different regimes can be distinguished from the semi logarithmic plot of the I-V curves as shown in Figure 9. The regime observed for current densities of about 1 mA/cm^2 to 100 mA/cm^2 corresponds to a linear variation with a slope of 59 mV/decade at room temperature, in agreement with a classical metal/semiconductor contact slope of (kT/q) x Ln(10) (where q is the electron charge, k the Boltzmann constant, and T the absolute temperature). This result is indicative, as suggested by several authors [Gas89, Leh00 and Smi92], of a current which flows during PS formation regime over the Schottky barrier at the depleted silicon surface through thermionic emission.

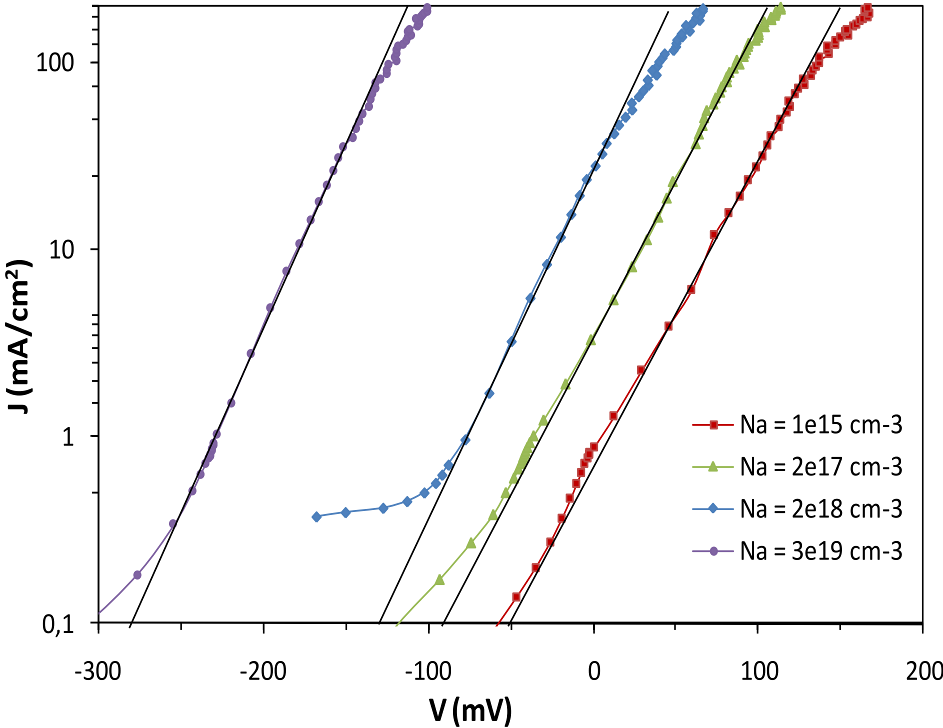


Figure 9 Logarithmic variations in anodic current as a function of anodization potential. Full line is drawn with a slope corresponding to a variation of 59 mV/decade

The regime corresponding to low current densities below 1 mA/cm^2, and in which no PS is formed, is attributed to the leakage current of the junction. Whereas, the one obtained at higher current densities, and in which the current increases vs. the electrode potential slows down, is related to either the ohmic drop due mainly to the substrate resistivity or a supposed change in the transport mechanism from thermionic process to tunneling.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

However, the simple Schottky theory cannot solely explain the shift observed in the I-V characteristics toward negative potential when the doping concentration increases. Gaspard et al. [Gas89] have attributed that to an increase in the potential drop across the Helmholtz layer present at the silicon electrolyte interface as shown in Figure 10 which presents the energy band diagram and the related potential distribution through the metal/semiconductor/electrolyte system upon an anodic polarization V applied to the silicon electrode against the reference electrode.

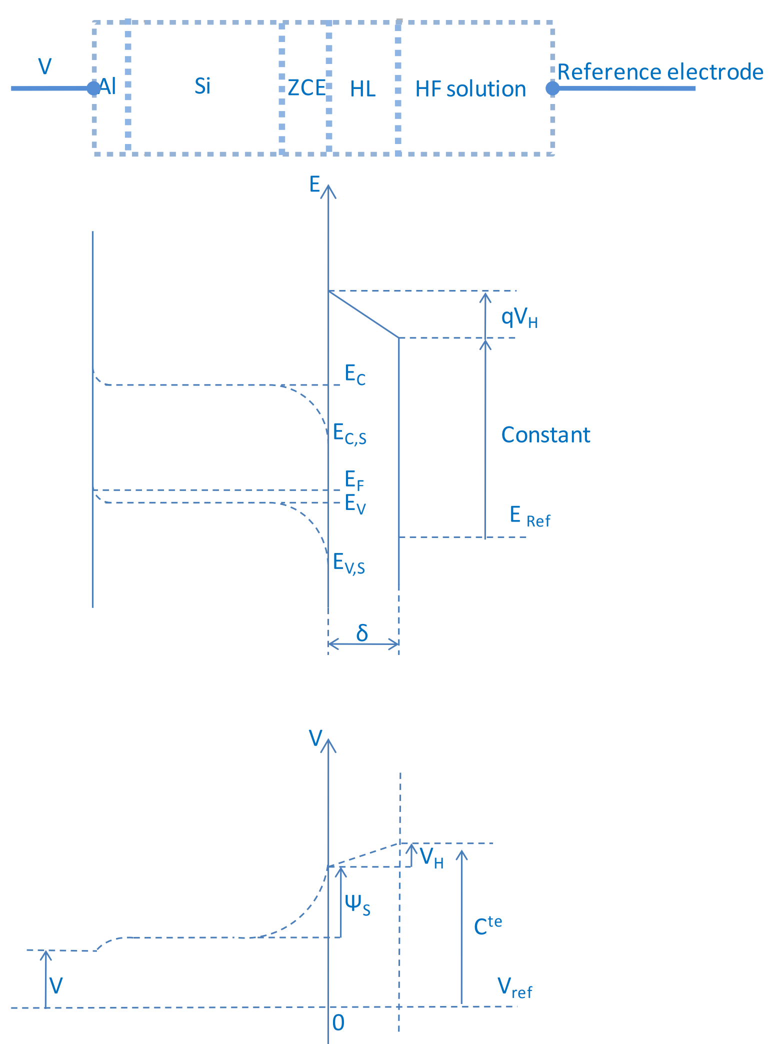


Figure 10 Energy band diagram and related potential distribution of the metal/semiconductor/electrolyte system

In fact, according to the Schottky model, the current which is limited by the majority carriers supply over the surface potential barrier Ψ_s at the silicon surface can be expressed as

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

$$I = K\, p_0\, e^{-\frac{q\Psi_s}{kT}} = K\, N_a\, e^{-\frac{q\Psi_s}{kT}} \tag{1}$$

where K is a proportionality constant and N_a is the acceptor doping concentration which is assumed to be equal to the hole density p_0 in the bulk silicon.

Furthermore, by assuming that there are no voltage variations in the electrolyte and that the (ohmic) back contact voltage drop is negligible, the electrode polarization V is only shared between Ψ_s and the Helmholtz voltage drop V_H according to

$$C = \Psi_s + V_H + V \tag{2}$$

where C is a constant which mainly depends on the chosen reference electrode, and so the expression of the anodic current density becomes

$$\mathrm{I} = K' e^{\frac{q\,(V+V_H)}{kT}} = K''(Na)\, e^{\frac{qV}{kT}} \tag{3}$$

The variations in the Helmholtz voltage drop V_H, corresponding to an increase of the current density from 1 mA/cm^2 to 100 mA/cm^2, remain very small compared to the applied anodic potential as shown in Table 5 below. Therefore, the linear regime in the semi logarithmic plot of the I-V characteristic is always obtained whatever the doping concentration is. On the other hand, the doping level influences the value of K'' through V_H, and so the different characteristics obtained for different doping concentrations will be shifted with respect to each other by an amount equal to the V_H variations resulting from the concentration variations. As example, this voltage drop is of the order of a few millivolt for low doped silicon but it increases up to hundreds of millivolt for the highest doping concentration.

Table 5 Calculated values of the surface potential barrier Ψ_s and the Helmholtz voltage drop V_H showing their variation with the silicon doping concentration and the current density

	$N_a = 10^{15}$ cm^{-3}		**$N_a = 3.10^{19}$ cm^{-3}**	
I (mA/cm^2)	1	100	1	100
Ψs (mV)	500*	380	770	650
V_H (mV)**	1.86	1.62	400	367

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

* A likely value of Ψs at equilibrium (and so at 1 mA/cm^2) for a doping concentration substrate of 10^{15} cm^{-3} as shown by interfacial impedance measurements [Ron91, Mem61], all other values of Ψs can be calculated according to equation (1)
** All values of V_H are determined according to equation (6) assuming a Helmoltz capacity of 7 µF/cm^2

3.3. The anodization potential dependence toward the doping concentration

Using the expression of the electric field E_S at the depleted silicon surface[1]:

$$E_S = \sqrt{\frac{2qN_a}{\varepsilon_s}\Psi_S} \qquad (4)$$

where ε_s is the dielectric permittivity of silicon, and the conservation equation at the boundary:

$$\varepsilon_s E_S = \varepsilon_H E_H \qquad (5)$$

where E_H and ε_H are the corresponding electric field and dielectric permittivity in the Helmholtz layer, respectively, the Helmoltz voltage drop V_H can be written as

$$V_H = E_H\delta = \frac{\varepsilon_s}{\varepsilon_H}E_S\delta = \frac{\varepsilon_s E_S}{C_H} = \frac{1}{C_H}\sqrt{2qN_a\varepsilon_s\Psi_S} \qquad (6)$$

where δ and C_H are the thickness and the capacity of the Helmholtz layer, respectively.

Therefore, it can be demonstrated from equations (3) and (6), that at constant current density the shift observed in the anodization potential V is proportional to the square root of the doping concentration according to the following expression

$$V = C^t - \frac{1}{C_H}\sqrt{2q\varepsilon_s\Psi_S}\sqrt{N_a} \qquad (7)$$

---

[1] A more accurate expression of E_s can be written by adding the correction factor of kT/q which arises from the contribution of the majority carrier distribution tail near the edge of the depletion region [Sze06].

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf

© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

It is noticeable here that at constant current density, Ψ_s also varies with N_a according to equation (1) but it is only proportional to the logarithm of N_a. So that, its related variation does not markedly influence the shape of the curve $V = f(\sqrt{N_a})$, which is thus expected to be very close to a straight line.

Figure 11 shows the plot of the calculated values of the anodization potential according to equation (7) compared to the experimental values for a current density of 40 mA/cm^2 and corresponding to different electrodes of doping concentrations varying from 10^{15} cm^{-3} to 3.10^{19} cm^{-3}. For the calculated curve, a likely value of 0.5 V can be chosen for Ψ_s at 1 mA/cm^2 for a doping concentration of $N_a = 10^{15}$ cm^{-3} as it has been found by interfacial impedance measurement [Ron91, Mem61] and so all values of Ψ_s for one particular doping concentration and current density can be known according to equation (1).

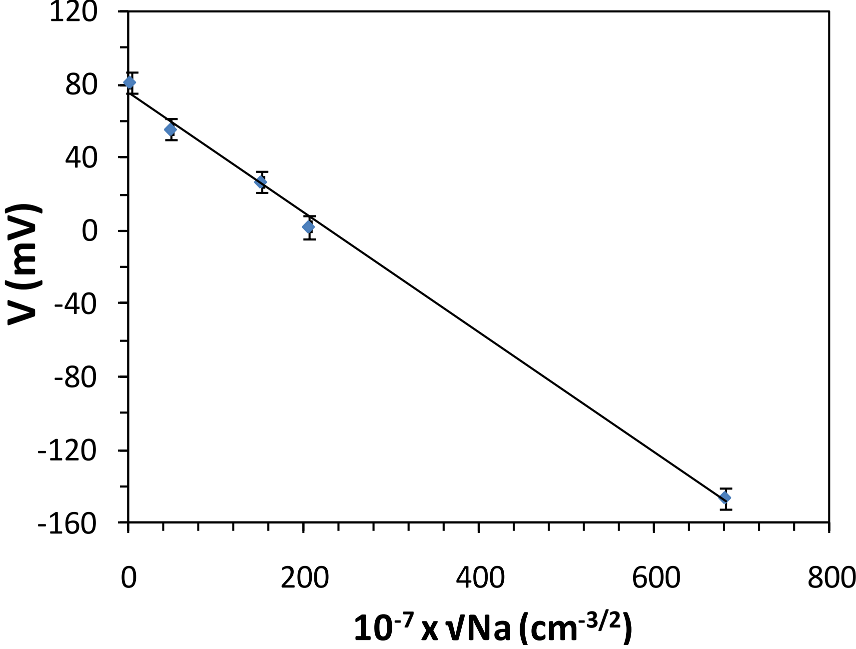


Figure 11 Variations of anodization potential V for a current density of 40 mA/cm^2 as a function of the square root of the silicon doping concentration N_a. Full line is the calculated curve according to Eqs. (7) and (1)

It appears that the experimental data fits quite satisfactorily the calculated curve with a corresponding value of $C_H = 7$ µF/cm^2 which seems to be a very likely value compared to that found by [Ron91]. The curve $V = f(\sqrt{Na})$ is of interest in that it will be used in the next part as a calibration curve for the application of doping impurity profiling using electrochemical anodization.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf

© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

4. Application: p-type silicon doping profiling using electrochemical anodization

The aim of this part is to present an impurity profiling method based on simple potential measurements during the electrochemical anodization of a p-type silicon sample which presents staircase doping concentration variations. The secondary ion mass spectrometry (SIMS) profile of this sample is given below in Figure 12. It consists of six p-type layers of about 250 nm thickness each with doping concentrations between 10^{17} cm^{-3} and 3.10^{19} cm^{-3} which are grown by RP-CVD (reduced pressure chemical vapor deposition) over a p-type substrate of 5.10^{15} cm^{-3} doping concentration.

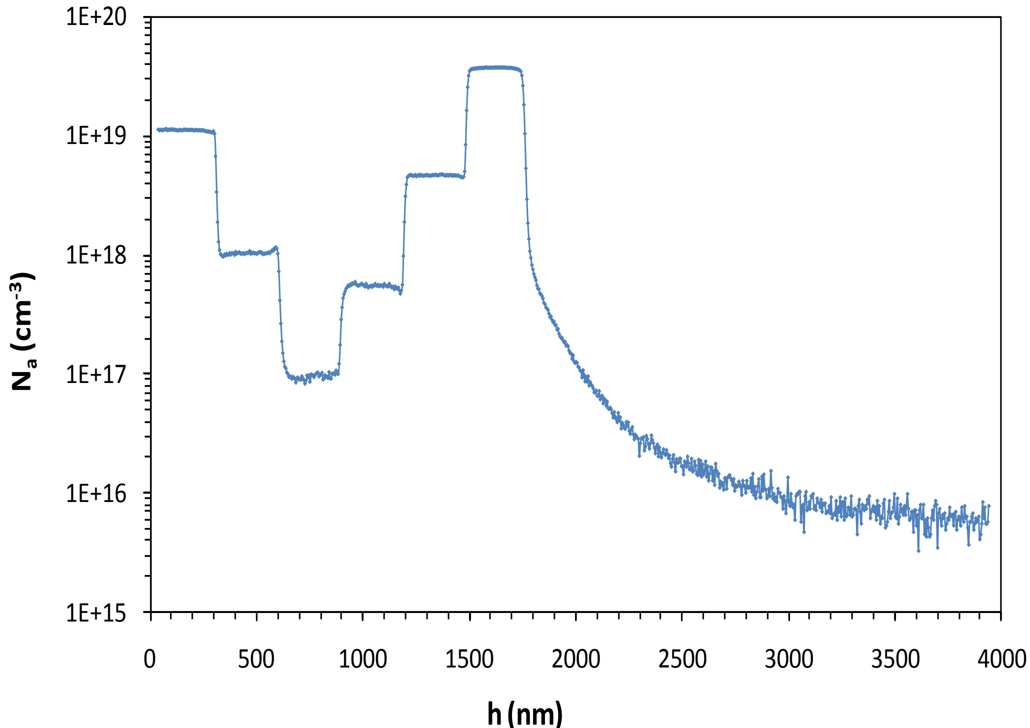


Figure 12 Impurity profile of the staircase p-type doping sample obtained by SIMS analysis

4.1. The method principle: potential variations during PS formation

As discussed before, the anodization potential corresponding to the PS formation regime is found to be determined by the interface electrochemical reaction and dependent on the silicon doping level.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

The recording of the anodization potential versus the electrolysis time during PS formation at constant current density (J = 10 mA/cm^2) for substrates of different doping concentrations (Figure 13) also confirms that the potential remains constant up to several microns of formed porous layer thickness and it is found to decrease when the doping level increases. So, its value is then directly characteristic of the silicon doping concentration at the interface, that is to say at the pore tips where the reaction takes place. Consequently, if PS is formed at a constant current density in silicon presenting dopant concentration variations, the anodization potential is expected to vary according to the concentration profile.

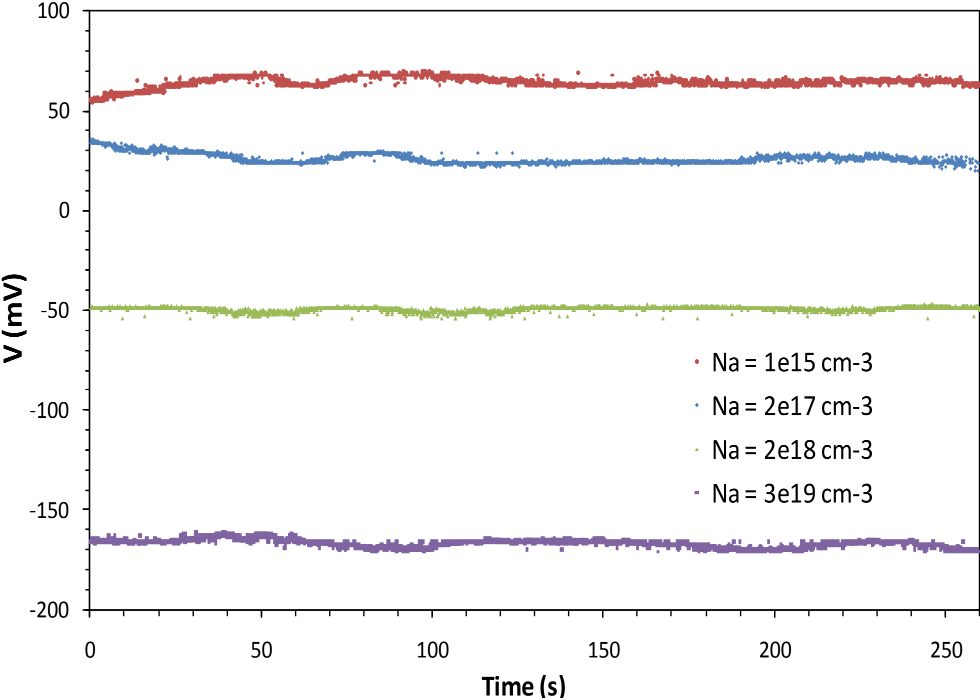


Figure 13 Electrode potential vs. electrolysis time during PS formation on homogeneously p-doped substrates of different doping concentrations at constant current density J = 10 mA/cm^2

Figure 14 shows the recording of potential variations during the anodization of the staircase doping sample at a constant current density of 40 mA/cm^2. These variations correspond well to the penetration of PS/Si interface into a depth of varying doping level. Then, a constant potential is observed when reaching the bulk silicon where the doping concentration is constant.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

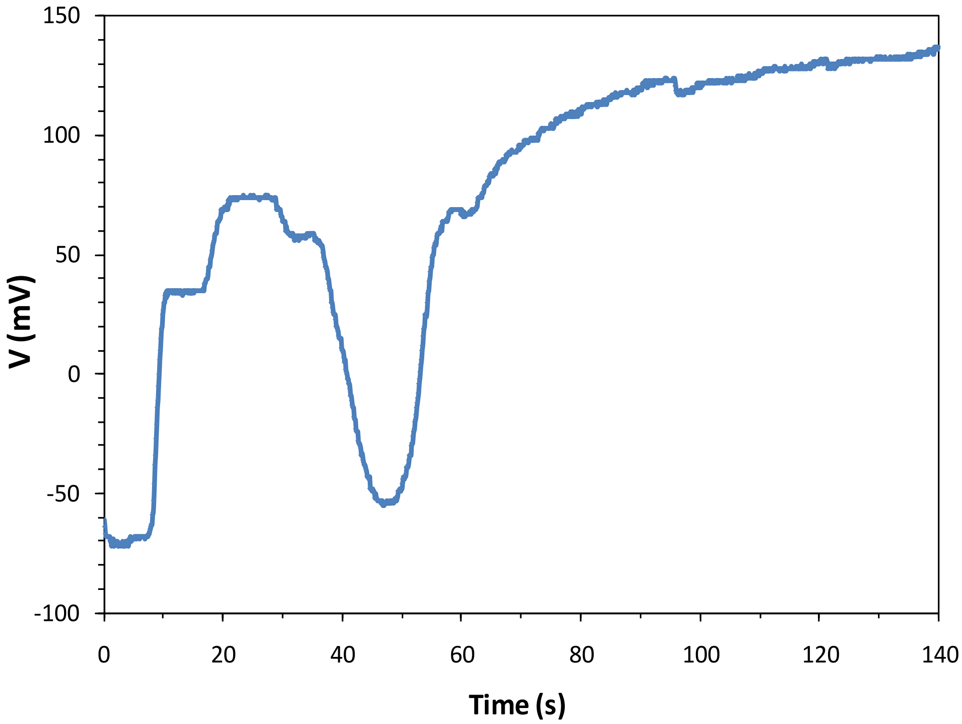


Figure 14 Potential variations during anodization of a staircase doping sample at constant current density J = 40 mA/cm^2

4.2. Conversion of potential variations during anodization to doping profiling

The question now is how to transform this potential recording into an impurity profile representation. This is achieved by means of two conversions: potentials to doping concentrations and time to depth [Lig89]. The first conversion "potentials to doping concentrations" can be done using the calibration curve of Figure 11. It must first be emphasized that the determination of an absolute potential for each doping concentration, which depends on the cell configuration through the ohmic voltage drop, is not necessary. In fact, as in practical profile analysis where the bulk concentration is generally known, one can have the doping concentration of the staircase sample substrate as a known value. Consequently, taking the constant potential corresponding to the bulk of the sample as a reference and knowing the slope of the curve V = f(√Na), one can determine all doping concentrations related to each measured potential at a given time of anodization just by measuring the potential shift from the reference value. It is obvious here that the position of the reference electrode relative to the silicon electrode is not important and has no effect on this calculation as it just adds the same ohmic voltage drop of the electrolyte for all potentials recorded on the same sample.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Concerning the second conversion "time to depth", it must just determine the rate of PS formation. It is well known in the literature that the rate of PS formation is expected to depend both on the current density and on the doping level, just like the porosity but at this particular current density of 40 mA/cm^2, it varies little over the whole range studied of doping concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} [Leh02,Nyc06]. SEM cross sectional observations are performed on bare p-type silicon samples of different doping concentrations anodized at a constant current density of 40 mA/cm^2 for different times and showed that the rate of PS formation is first constant with depth, at least for thickness below 10 µm and varies from 1.8 to 2.3 µm/min in our experimental conditions. For reasons of simplifications, we will then assume for the "time to depth" conversion a same PS rate at 40 mA/cm^2 equal to 2 µm/min for all doping levels in the staircase sample.

The resulting impurity profile is shown in Figure 15 and compared to the SIMS analysis.

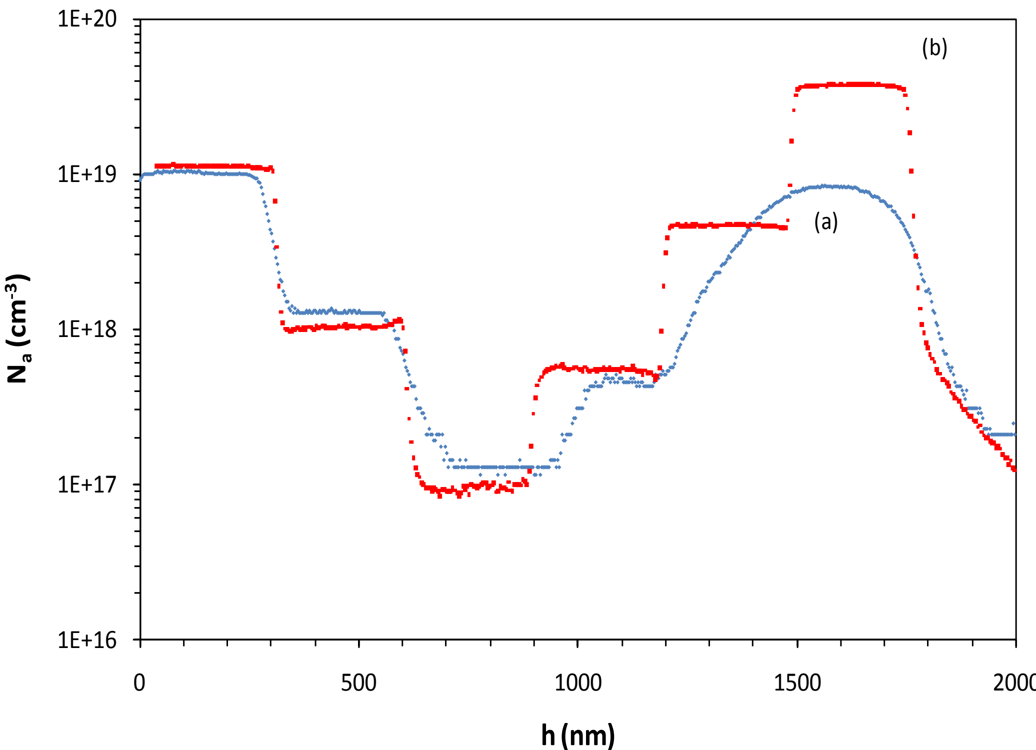


Figure 15 Impurity profile of the staircase doping sample as determined by the PS method (curve a) and compared to the SIMS analysis (curve b)

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf

© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

4.3. Limitation of profiling method by electrochemical anodization

A very good agreement is obtained for the descending part of the profile (the first three stairs) with relatively accurate doping concentrations comparable to SIMS measurements. However, it was difficult with the electrochemical profiling method to detect interface abruptness between the different doped regions. In fact, the doping concentration is measured as the space charge between the electrolyte front and the silicon electrically neutral region. So, at first approaches, the depth resolution corresponds to the space charge width of the electrolyte/silicon junction formed at the PS/Si interface. The method is somehow similar to capacitance-voltage carrier profiles techniques using solid Schottky junctions [Sze01]. The main advantage is the quasi unlimited prospected depth but the method is destructive. In our case, the space charge width calculated using Schottky model is estimated from 10 to 100 nm when the doping concentration decreases from 10^{19} down to 10^{17} cm^{-3} while the experimental resolution, given by the slope of the doping profile at the transition between two successive decreasing doping levels, is about 60 to 180 nm/decade. The space charge extend appears as the basic limitation of the resolution. However, as the technique gives in fact carriers profiles rather than dopant atoms ones, the resolution is lowered by the spatial redistribution of holes due to the diffusion mechanism (increasing of the transition region between two doping levels). For high doping densities, the depth resolution of our electrochemical method is comparable to that of the SIMS analysis which is evaluated to 19 nm/decade at a working kinetic energy of accelerated ions of 8 kV [Gau96].

Furthermore, difficulties arise for the ascending part, where doping concentrations measured by the electrochemical anodization method are no longer following stair variations. This can be explained by both the inhomogeneity of the anodic reaction front and the high selectivity of PS formation with doping concentration. In fact, when PS is forming on the layer of lower doped concentration, it is very likely that one pore will first reach the bottom layer of highly doped concentration. At this time, the current lines will concentrate in this pore and so the dissolution reaction will preferentially proceed at a higher rate at the pore tip i.e. in the highly doped region. The potential measured here will decrease becoming determined by the HF/high doped silicon interface. Its value will continue then to decrease progressively as the local current density will increase following the increase of the surface of the bottom layer in contact with the electrolyte when the pore branches or/and other pores reach this layer. The same phenomenon will happen again when reaching another layer of

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

higher doping concentration. The effect on the anodic potential variations seen in the ascending part of the profile is illustrated on the diagram of Figure 16 by referring to the I-V characteristics obtained before; t_1 and t_2 are considered as the instants when the electrochemical attack begins in a layer of new doping concentration.

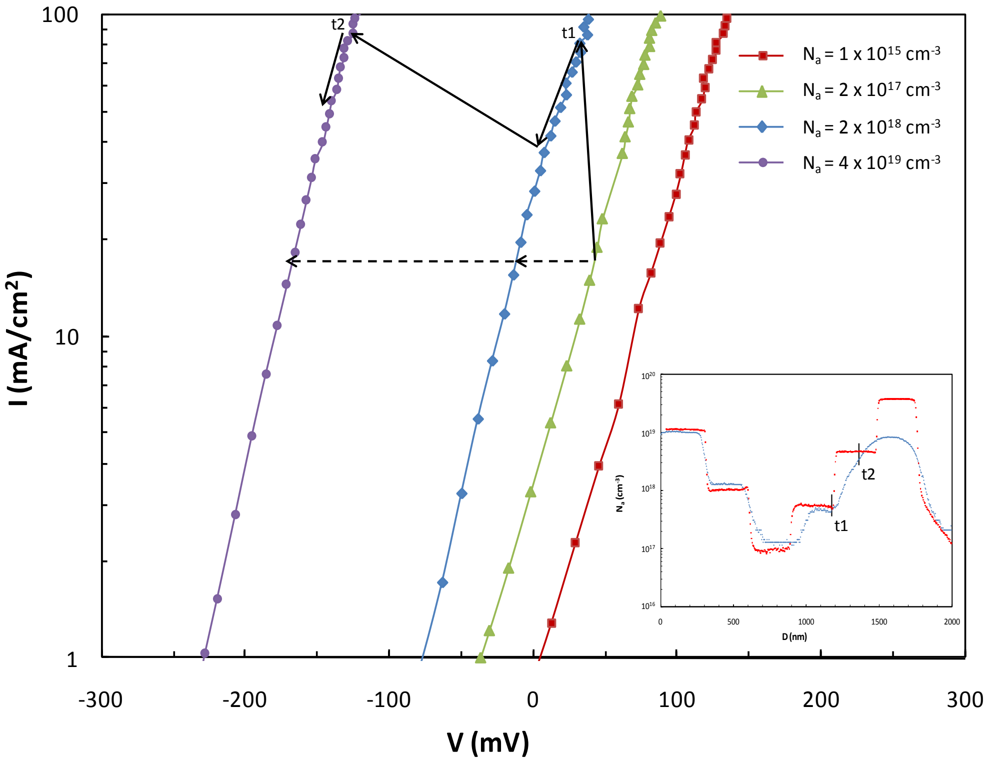


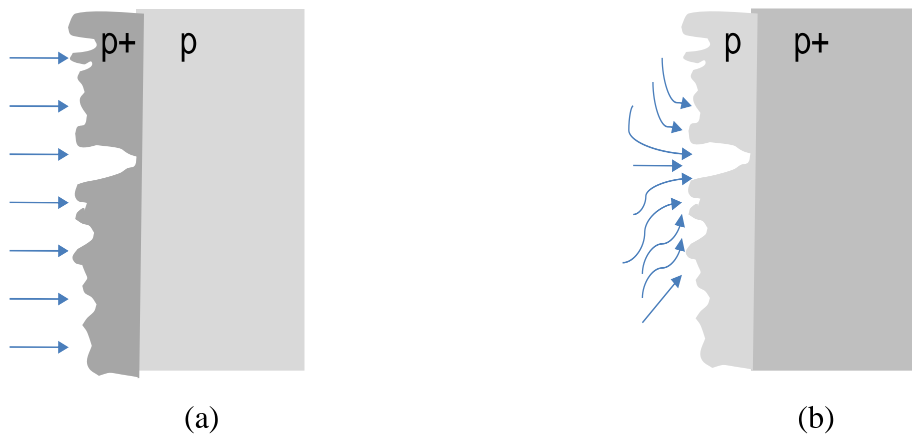
Figure 16 I-V characteristics during PS formation on silicon substrates of various homogenous doping concentrations. Dashed arrows show the expected potential variations for anodization at constant current density of the last two doping layers of the staircase sample. Full line arrows show the potential variations in the case of uncontrolled current density

It can also be noticeable that the highest doping concentration determined by the PS method in the ascending part of the profile is lower than expected from SIMS measurement for the same reason of uncontrolled local current density; as the effective anodic current density is not actually constant, potential variations deviating upward from those expected from a constant current density, lead to a lower potential shift and then to lower measured doping concentration.

In contrast, when analyzing layers of decreasing doping levels as it is the case for the three first stairs of the profile, the measured potential corresponding to the anodization of a highly doped top layer will not vary even if a pore reaches first a region of lower doping

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

concentration. In such a case, the current lines don't markedly change and the electrochemical attack still progresses in the highly doping region as illustrated in Figure 17. However, it was difficult with the electrochemical profiling method to detect the abrupt transition between two regions of different doping concentrations. This low resolution comparing to SIMS analysis can also be explained by the inhomogeneity of the reaction front. Changing the electrochemical anodization parameters such as the temperature or the chemical composition of the electrolyte could be a solution to obtain a homogenous reaction front.



(a) (b)

Figure 17 Representation of current lines during anodization of two layers of different doping concentrations: (a) the top layer is the highly doped, (b) the top layer is the lightly doped

5. Charge carrier transfer during PS formation of n-type silicon

An n-type silicon electrode anodized in the dark is under reverse bias and so only small current density is normally observed. However, the dark current may increase by orders of magnitude, giving rise to PS formation, if breakdown of the space charge region at the electrode surface occurs providing the necessary holes for the silicon dissolution. Depending on the doping concentration and the applied voltage, there are two mechanisms which are responsible for breakdown: tunneling and avalanche multiplication (or impact ionization).

5.1. Highly doped n-Si

Tunneling effect is the more likely mechanism suggested in literature [Leh02, Jak07, Jun02 and Cam98] as a cause of pore formation in highly doped n-type silicon ($N_d > 10^{18}$ cm^{-3}). In fact, upon applying a small positive potential at the silicon electrode, a relatively large

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

band bending occurs. The thickness of the space charge region (SCR) becomes then very small and the electric field becomes very strong, so that valence band electrons can tunnel through SCR from the silicon atoms on the surface into the conduction band in the bulk semiconductor and thus result in holes formation at the surface and silicon dissolution.

Figure 18 shows the current-voltage characteristics for n-type silicon samples of different highly doping concentrations in the condition of PS formation.

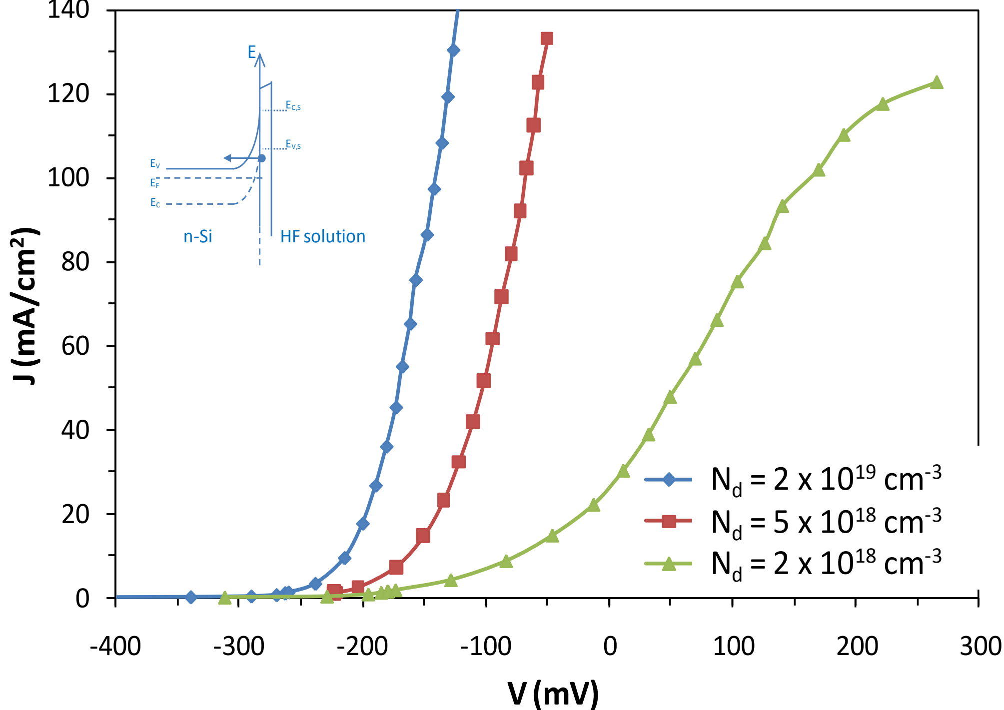


Figure 18 Anodic current-voltage characteristics of n-type silicon in HF solution for substrates of different donor doping concentrations N_d. The inset shows the charge transfer mechanism expected to occur and which is at the origin of PS formation in highly doped n-Si

A shift of the current onset toward more positive potentials is observed with decreasing doping concentration. In fact, higher doping density induces higher potential barrier at equilibrium and so higher electric field strength and lower depletion region width which enables charge carriers to pass through SCR upon a lower applied potential. In Table 6, the estimated surface barrier potentials at equilibrium $\Psi_{s,equ}$ for different doping concentrations together with the calculated semiconductor space charge widths W_{SCR} and the resulting electric fields at the silicon surface E_{max} according to [Sze01] are summarized. The value of $\Psi_{s,equ}$ is deduced from the flat band potential V_{FB} and the rest potential of the silicon electrode (also known as the open circuit potential OCP) which is about -250 mV. Taking into

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

account the Fermi level shift with increasing doping concentration, all flat band potentials are extrapolated from the flat band potential V_{FB} = -450 mV (vs. an Ag/AgCl reference electrode) of a doping concentration $N_d = 8.10^{14}$ cm^{-3} which has been measured by Mott-Schottky plots in [Ron91] where the authors have practically used the same experimental conditions as in our work.

Table 6 Flat band potential, surface barrier potential, space charge width and maximum electric field at equilibrium for different n-Si doping concentrations

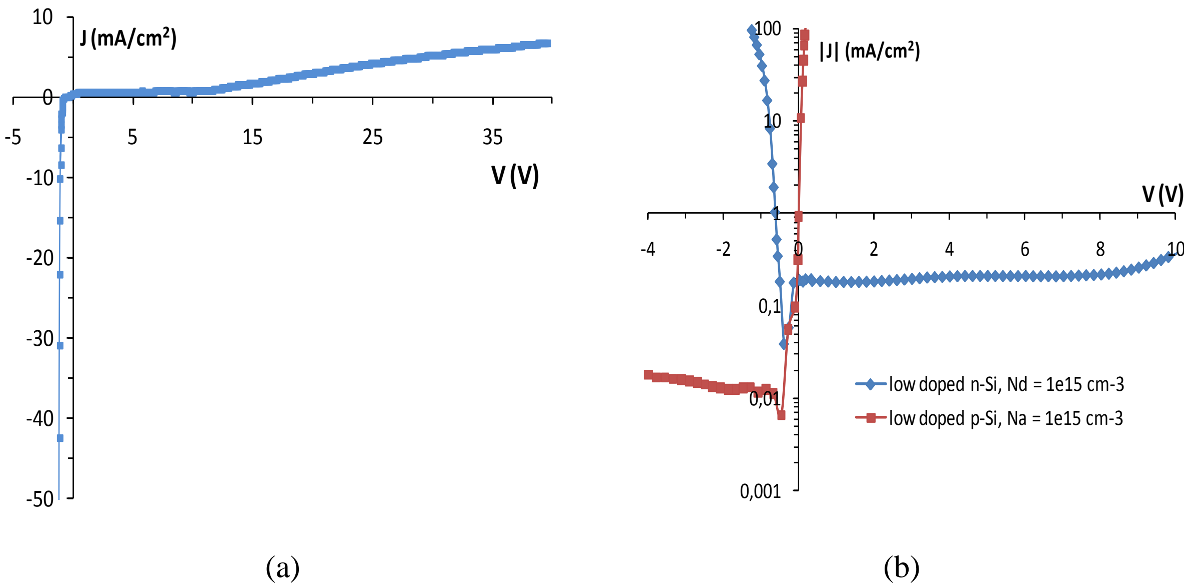
N_d (cm^{-3})	V_{FB} (mV)	$\Psi_{s,equ}$ (mV)	W_{SCR} (nm)	10^{-5} E_{max} (V/cm)
2.10^{19}	-705	-455	5.4	16.6
5.10^{18}	-677	-427	10.6	8.06
2.10^{18}	-650	-400	22.3	3.49

5.2. Low doped n-Si

As shown in Figure 19.a, for low doped n-type silicon samples in the range of 10^{15} cm^{-3} doping concentration, the current density still almost equal to 0 for high applied potential up to 12 V and thus no PS formation is observed. The charge transfer mechanism expected to occur for higher voltages is avalanche breakdown. The breakdown bias corresponding to this doping level is in excess of 100 V according to Sze [Sze01].

On the other hand, by representing the current voltage characteristic in a logarithmic scale and comparing it with the one obtained for low doped p-type silicon as reported in Figure 19.b, one can see that in the range of potential corresponding to the charge carrier depletion, the reverse current density of an n-type silicon electrode is higher by about one order of magnitude than of p-type silicon. This is attributed to a higher density of surface states present on n-type silicon electrode in acidic solution than on p-type surface which is more stable by hydrogen termination (passivation) in the cathodic regime [Che05, Bel98 and Yab86].

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



(a) (b)

Figure 19 (a) I-V characteristic of a low doped n-Si in HF ($N_d = 10^{15}$ cm^{-3}), (b) logarithmic variation of current as a function of applied potential for low doped n- and p-Si in HF

5.3. Moderately doped n-Si

In the case of moderately doped n-Si, both tunneling and avalanche multiplication mechanisms are observed.

The current-voltage characteristic for a substrate of 3.10^{17} cm^{-3} doping concentration for example (Figure 20) shows an exponential rise of the anodic current in the range of 0-1 V corresponding to charge carrier transfer by tunneling effect, immediately followed by a bending due to the formation of a highly resistive depletion layer and then a second rise above 4 V caused by avalanche multiplication process. Sze [Sze06] has reported that breakdown below 4.4 V for planar silicon substrate of 5.10^{17} cm^{-3} doping concentration is dominated by tunneling effect while above 6.6 V avalanche multiplication dominates. For bias between these limits a mixture of both mechanisms is observed.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

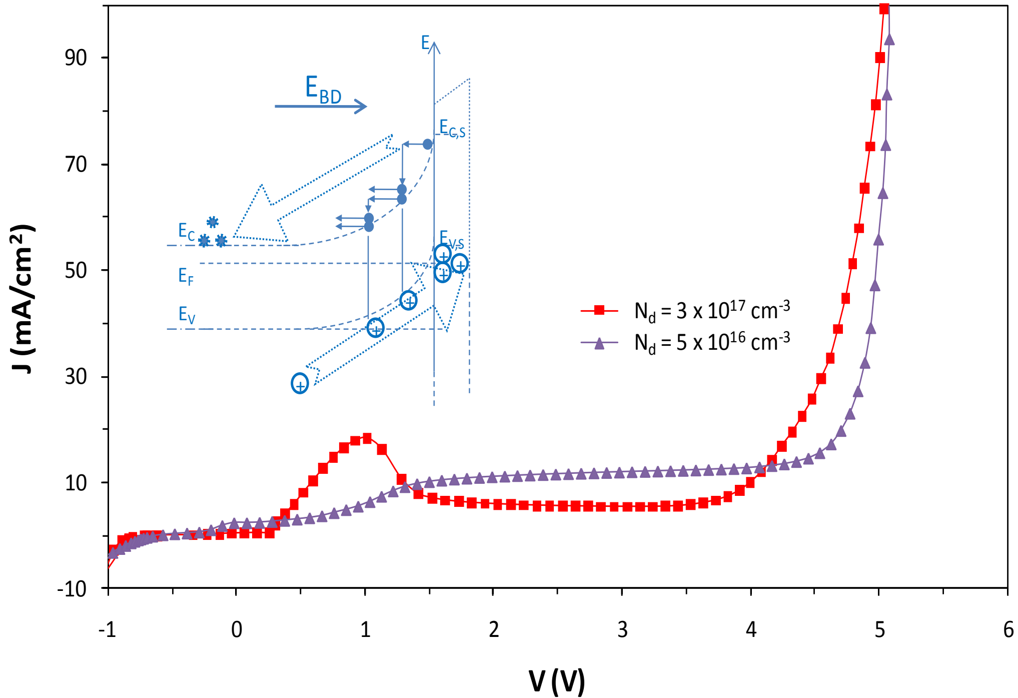


Figure 20 Anodic I-V characteristics for moderately doped n-Si substrates of two different doping concentrations in HF, scan rate is 0.1 V/s. The inset shows the avalanche multiplication process supposed to be dominant at high voltages

In addition, it has been suggested that the avalanche breakdown voltage V_{BD} is inversely proportional to the donor doping concentration N_d according to the following equation:

$$V_{BD} = \frac{\varepsilon_s \, E_{BD}^2}{2qN_d}$$

where E_{BD} is the maximum electric field at breakdown in silicon supposed to vary very slowly with N_d according to:

$$E_{BD} = \frac{4 \times 10^5}{1 - \frac{1}{3}\log\left(\frac{\mathrm{N_d[cm^{-3}]}}{10^{16}}\right)} \; [V/cm]$$

This dependence is hardly pronounced in our case as shown in Figure 20. In fact, it is important to mention that the formation of pores in an initially flat silicon electrode due to the low current density at low voltages prior to avalanche affects the I-V characteristics. As the silicon surface is no longer planar and since the junction breakdown onset does not only depend on doping concentration and on applied bias, but also on junction perimeter [Sze06],

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

around a depression in the electrode the depletion region width is decreased and the field strength is increased, which leads to a premature breakdown and thereby to a local current density there. In other words, the avalanche breakdown voltage is becoming determined by pores geometry and not only doping concentration.

It should be cautioned that a reproducible I-V curve in the common sense does not exist for moderately doped n-type silicon in HF. It is found to be sensitive to scan speed as shown in Figure 21. Zhang [Zha91] has reported that at a pore bottom the field is the largest at the pore tip because there the radius of curvature is the smallest. Therefore, slower scan rate leads to lower breakdown bias due to a decrease of the radius of curvature of the pore tip for prolonged anodization.

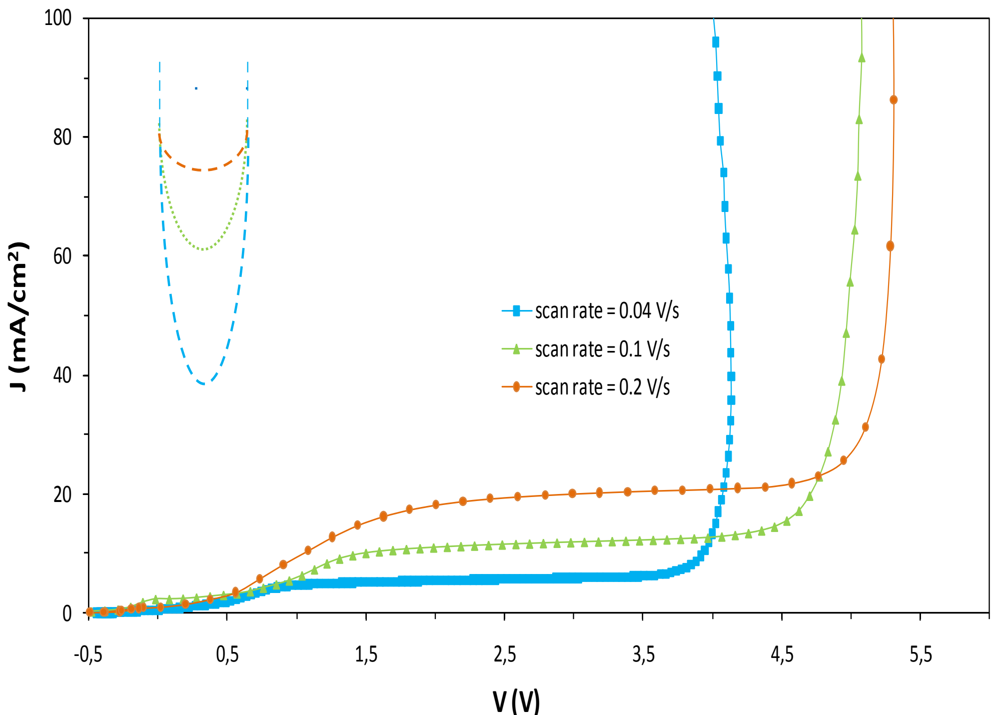


Figure 21 Anodic I-V characteristics for n-type doped substrate at different scan rates, $N_d = 5.10^{16}$ cm^{-3}. Evolution of the radius of curvature of the pore tip with anodization time is shown in the inset

Lehmann et al. [Leh00] have related the different morphologies observed in n-type PS to the formation mechanisms and have also concluded, according to a computer simulation of the breakdown conditions at the pore tip whose geometry is assumed to be hemispherical, that breakdown for highly doped n-type silicon is always dominated by tunneling which is expected to produce structures of mesoporous size. In contrast, avalanche multiplication is

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

found to be responsible for the formation of macropores in moderate and low doped n-type substrates.

Finally, it has to say that evidence for tunneling or avalanche multiplication mechanisms cannot only be confirmed from simple I-V analysis. Study of temperature effect could be useful in order to distinguish the two mechanisms by the sign of their temperature coefficient. Since the energy bandgap in silicon decreases with increasing temperature, the breakdown voltage due to tunneling has a negative temperature coefficient, that is, the breakdown voltage decreases with increasing temperature while avalanche mechanism has a positive temperature coefficient [Sze06]. However, it remains difficult for us to install a cryogenic measuring system in a fume hood.

6. Application: n-type silicon doping profiling using electrochemical anodization

Figure 22 is a superposition of the different current-voltage I-V characteristics represented previously for n-type silicon wafers of different doping concentrations in HF solution in the regime of PS formation.

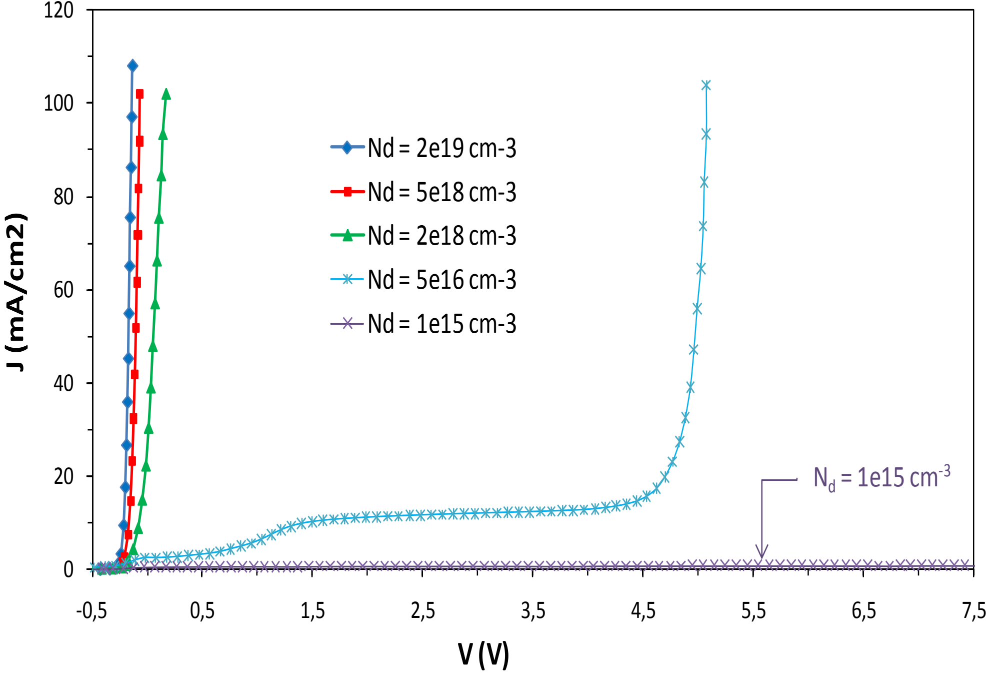


Figure 22 Anodic current-voltage characteristics of n-type silicon in hydrofluoric acid solution for substrates of different doping concentrations

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

At first sight, the distinct and pronounced shift of I-V curves toward more positive potentials with decreasing doping concentration seems worthwhile to be exploited for doping profiling, as in the case of p-type silicon. However, the lack of an unique quantitative model that could be valid for highly doped as well as for low doped n-type silicon, and the non reproducibility of current voltage measurements in moderate doped samples due to the change of the interface morphology by pore formation during anodization makes difficult the task of an accurate doping profile determination.

Let's take an example of samples of different n-doped epitaxial layers grown over a low n-doped silicon substrate in the range of 10^{15} cm^{-3} doping concentration. The SIMS profiles of these samples are shown below in Figure 23.

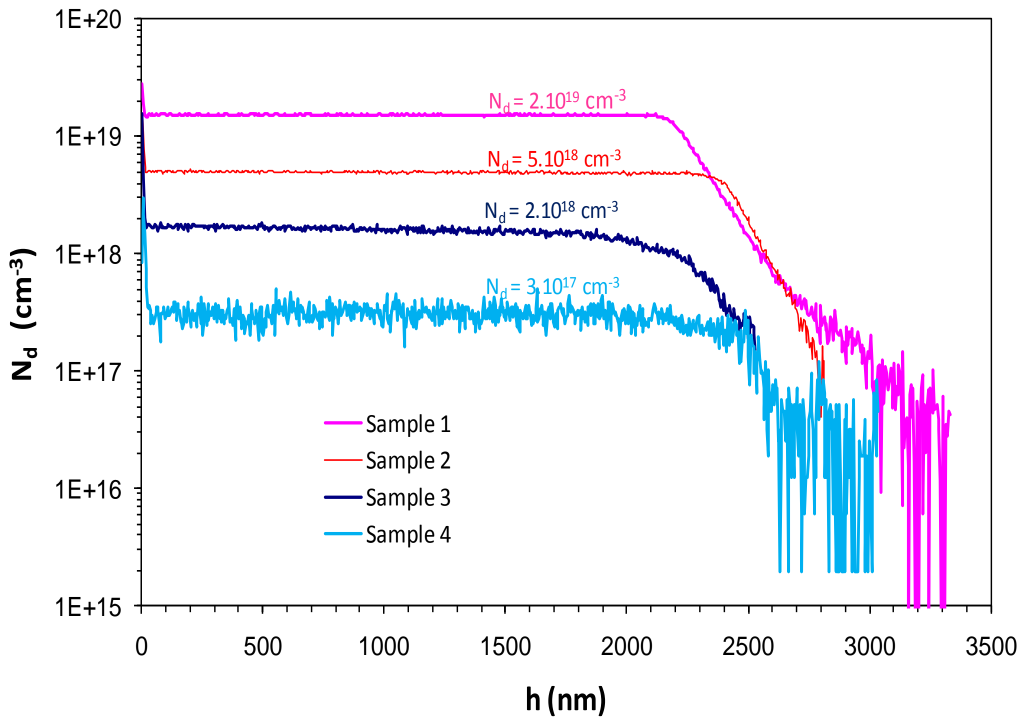


Figure 23 Impurity profiles of samples made by epitaxial growth of an n-doped layer over a low n-doped silicon substrate, layers are of different doping concentrations

The recording of anodization potentials during electrolysis of these samples at a constant current density is given in Figure 24.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

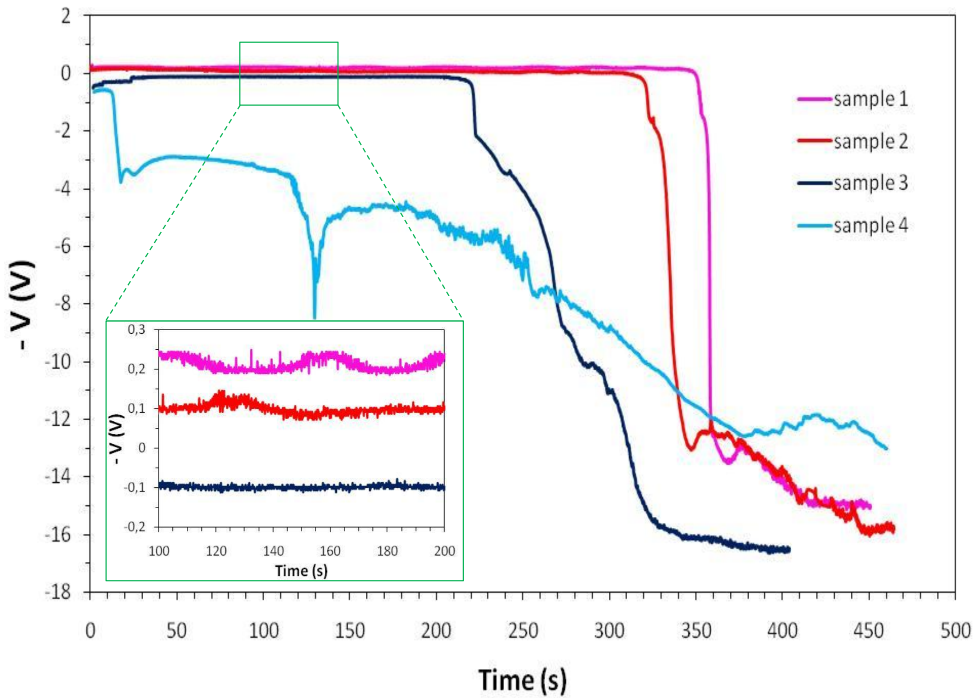


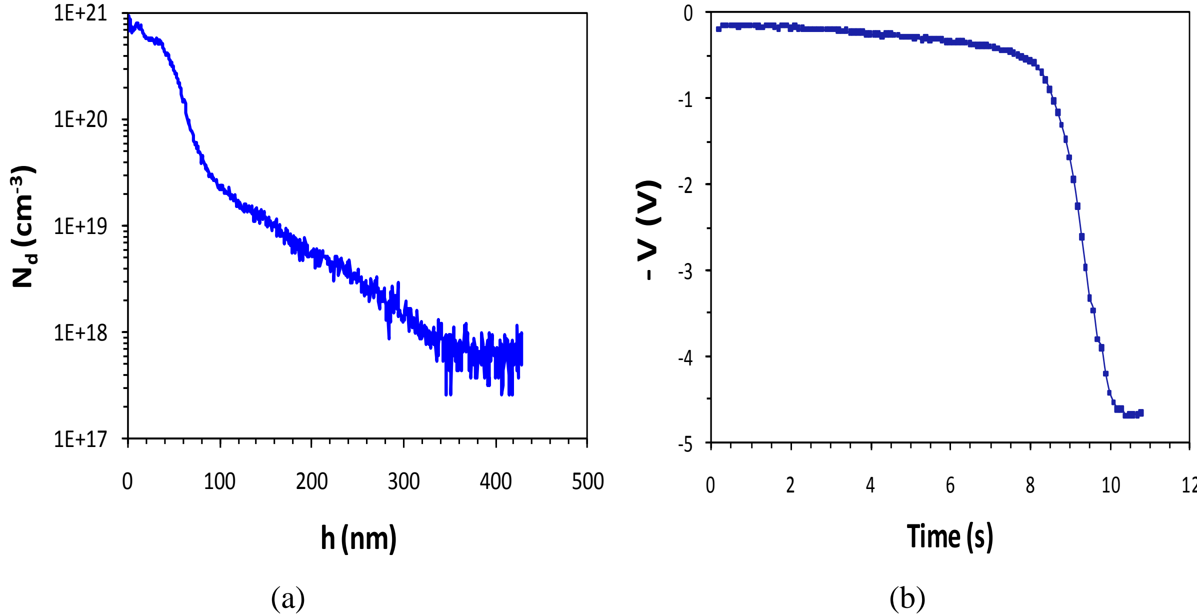
Figure 24 Potential variations during anodization of samples of an epitaxial layer grown over a low n-doped silicon substrate (layers are of different doping concentrations) during anodization at constant current density J = 10 mA/cm^2

The potential variation in the sample of the lowest n-doped epitaxial layer seems to be somehow unstable and cannot then be related to the anodized structure. This is explained, as discussed before, by pore formation that significantly changes the electrode surface and leads to local breakdown at pore tips. However, for other samples, it can be seen that a high and almost constant potential is found in a first regime, which corresponds to the formation of PS in the epilayer. A sharp decrease is then observed at the transition between the epilayer and the substrate, followed by a regime where the anodization potential becomes corresponding to the electrochemical attack of the bulk semiconductor. Although these later variations are well understood and the distinct anodization potentials values between the different layers are qualitatively in agreement with doping concentrations as pointed out in the inset of Figure 24, a precise doping profile remains difficult to be deduced using the same methodology as in p-Si profiling previously described. In fact, there is first no quantitative model that can govern the anodization potential dependence with the whole range of n-doping concentration. Second, the potential corresponding to the bulk etching is found to be not constant with time and is also greater than expected from the I-V curve of Figure 19.a as it is affected by premature breakdown due to the very large roughness of the porous epilayer/bulk interface. It cannot then be used as a reference potential to determine the exact doping concentration of the

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

epilayer. Concerning the time to depth scale conversion, it can always be easily achieved if a calibration of the porous layer growth rate with n-type silicon doping and applied current density is performed. In conclusion, even though an accurate impurity concentration profile is hardly to be obtained from the potential variations recorded during anodization of such samples, the electrochemical method is still useful for an easy determination of the actual thickness of the epilayer and the flatness of the doping level, particularly at the high range.

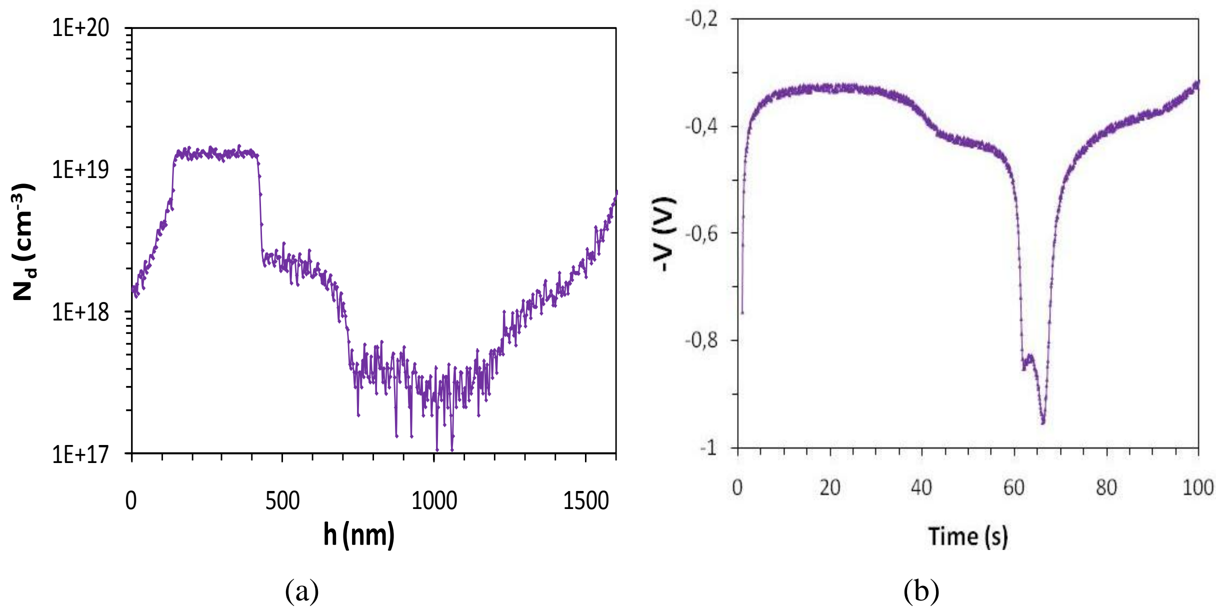
Below are two examples of samples with different doping profiles. The first sample is obtained by ion implantation of phosphorous into 10^{15} cm^{-3} boron-doped wafer and subsequent annealing in dry oxygen at 1000 °C during 15 min. The second one presents a staircase doping profile containing n-type layers with doping concentrations between 3.10^{17} cm^{-3} and 2.10^{19} cm^{-3} which are grown by RP-CVD (reduced pressure chemical vapor deposition) over a p-type substrate of 10^{15} cm^{-3} doping concentration. The SIMS profiles as well as corresponding potential variations for both samples during anodization at constant current density are given in Figure 25 and Figure 26.



(a) (b)

Figure 25 n-type implanted sample: (a) The SIMS profile, (b) potential variations during anodization at constant current density of 40 mA/cm^2

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



(a) (b)

Figure 26 Staircase n-dope sample: (a) The SIMS profile, (b) potential variations during anodization at constant current density of 10 mA/cm^2

The Table 7 below gives some points of comparison between the two techniques of silicon doping profiling: the SIMS analysis and the electrochemical method.

Table 7 Comparison between SIMS and electrochemical profiling techniques

	SIMS	**Electrochemical method**
Detection	atoms	carriers
Cartographic type	1D	1D
Resolution	19 nm/decade [Gau96]	60 nm/decade for highly doped concentrations [this work]
Possible quantification	Yes, using calibration samples	Yes, only for p-type doping

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Conclusion

It has been shown that the mechanism at the origin of PS formation on p-type silicon in concentrated hydrofluoric acid (HF) solution is determined by the charge exchange at the silicon surface over the Schottky barrier through a thermionic emission process. Whereas, for n-type silicon it is probably due to junction breakdown either by tunneling effects or impact ionization mechanism.

Furthermore, the anodic current-voltage characteristics of silicon measured for different substrate resistivities during PS formation have shown a negative potential shift with increasing doping concentration. This shift has been attributed for p-type Si to the potential drop across the Helmoltz layer present at the electrolyte/silicon interface and it has been found to be proportional to the square root of the doping concentration at a constant current density. This has then allowed the determination of the concentration profile in a wafer presenting staircase p-type dopant variations. In fact, during the electrochemical anodization of the wafer at a constant current density, recorded potential variations are converted to silicon doping variations using this square root dependence of the potential with the doping concentration and the electrolysis time scale is converted to a depth scale knowing the PS formation rate.

In the light of our results, it can be concluded that profiling using PS formation seems to be interesting as it is a quite sensitive method and much simpler than other techniques; it only requires a very simple electrochemical anodization in a hydrofluoric acid solution and no complex apparatus or sophisticated calculations are needed. However, this technique still presents two major limitations; first, it is restricted to p-type doping impurities and second, it cannot provide an accurate doping profile when the impurity concentration level to analyze is lower than that of the underlying layer.

Finally, even if we have not been able to use the PS doping profiling method for n-type silicon, the dependence of I-V characteristics with doping concentration observed for the n-type will be more suited to be exploited for the selective formation of PS. In fact, with a correct choice of the applied potential during anodization of a sample presenting different doping concentrations, the dissolution reaction will only be restricted to regions of higher doping level. The next chapter will focus on this application in the intention of forming selective oxidized PS.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Chapter 3: Oxidized Porous Silicon: Process optimization, localization and dielectric properties

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Introduction

Having studied the formation of porous silicon (PS), we will now focus on its oxidation. After a description of the oxidation process of PS, we will try to optically characterize the formed oxide in order to optimize our experimental conditions of anaodization and oxidation. We will then highlight the selective formation of oxidized porous silicon. Finally, we will perform a current-voltage I-V investigation on oxidized porous silicon samples in order to study the electrical behavior of the material and to determine its dielectric properties.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

1. Porous silicon oxidation process

To oxidize PS, we have employed a two-step oxidation process similar to that described by several groups [Bom88,Lin86 and Mol05]. The aim is to transform the PS layer into a homogenous oxide film with dielectric properties similar or close to those of the standard thermal silicon dioxide (SiO_2). In this process, PS is first subjected to a pre-oxidation step at quite low temperatures (around 300 °C) in order to stabilize its initial structure against irreversible transformations (sintering), and then followed by an oxidation at higher temperature for complete conversion into silicon dioxide. Later in the text, the resulting oxide is referred to as OPS: oxidized porous silicon. The overall process of PS oxidation is schematically drawn below in Figure 1. The oxidation is performed in a standard oxidation furnace SEMCO under atmospheric pressure dry oxygen. The risetime and the fall time, which are driven in inert atmosphere (nitrogen), are limited by the furnace kinetics (about 10 °C/min).

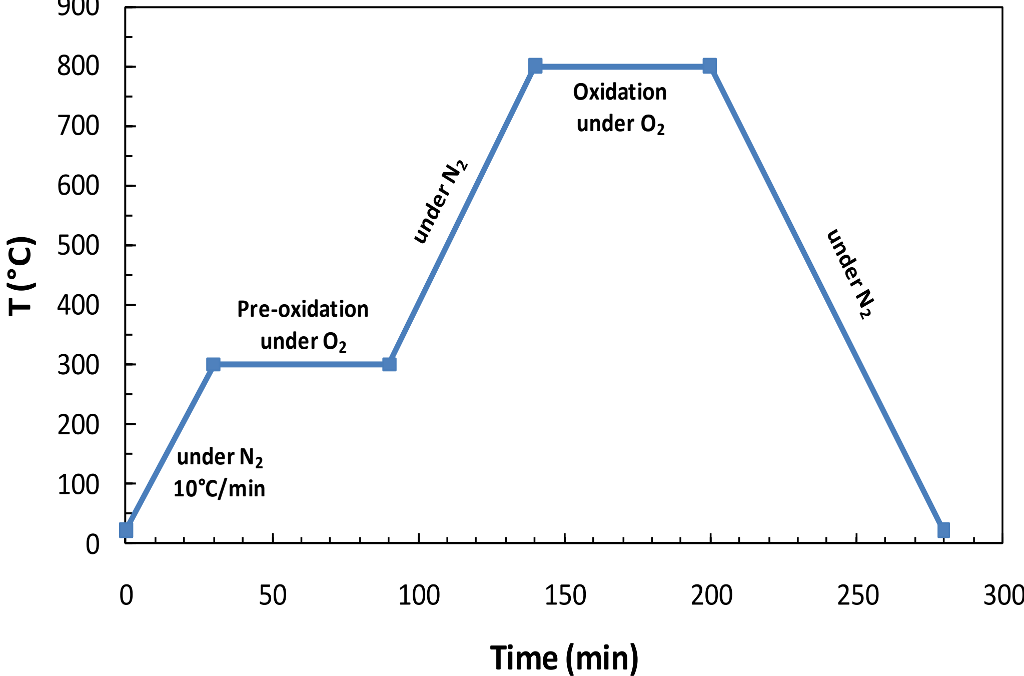
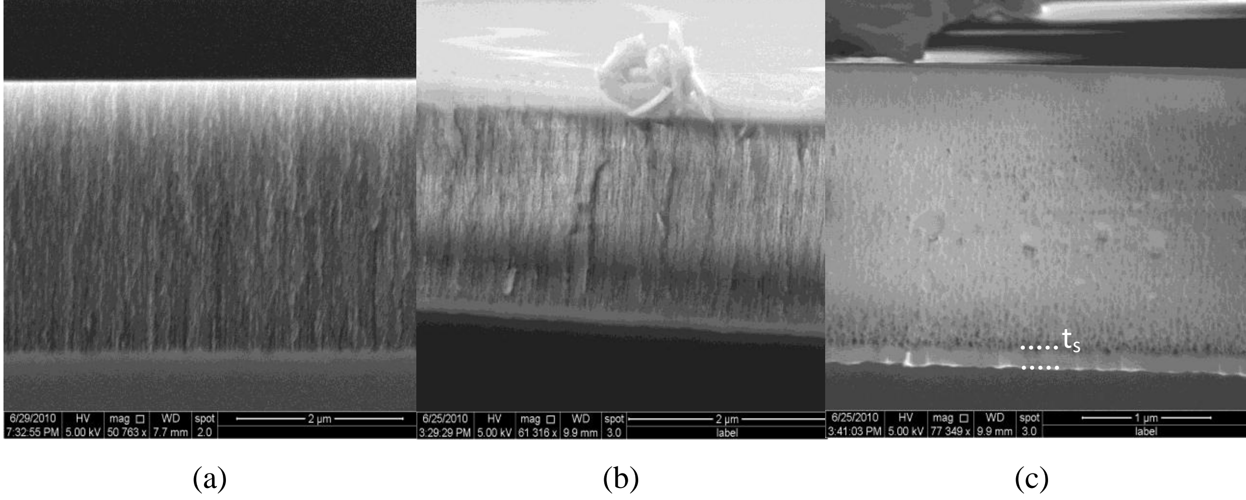


Figure 1 Temperature profile of the PS oxidation process with time

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

1.1. Pre-oxidation

Due to its large specific surface area and its very thin silicon walls, oxidation of PS may appear at first sight to be an easy task; a thick porous layer is expected to be oxidized in a relatively short time due to the easy access of oxygen gas into pores throughout the whole volume as well as the silicon thickness to oxidize does not exceed the pore wall thickness. However, the material seems to be unstable upon high thermal treatment. For temperature above 400 °C, coarsening of the porous texture occurs [Her84,Lab86] and drastically increases with temperature which considerably reduces the surface area and consequently reduces the reactivity of PS to oxidation. We can imagine that large voids (of about 1 µm) are formed in the material at high temperature, surrounded by thick silicon walls and so a complete oxidation of such a coarsened structure becomes very difficult if not impossible (Figure 2). This coarsening of PS texture obtained by progressive collapsing of pores is attributed to surface diffusion of silicon atoms along the pore walls when the temperature exceeds 400 °C. In fact, the as prepared PS surface is largely covered with hydrogen atoms that prevents the surface migration of silicon atoms but this covering is stable up to a critical temperature from which hydrogen desorption occurs [Gup88]. Silicon-hydrogen bonds appear therefore as a stabilizing factor for the structure at low temperatures up to ca. 400 °C.



(a) (b) (c)

Figure 2 SEM cross section of PS layers (a) without thermal treatment, (b) after oxidation at 1000 °C for 1h (c) after pre-oxidation at 300 °C for 1h + oxidation at 1000 °C for 1h, t_s is the thickness of the oxide grown in the bulk of Si at the bottom of the porous layer

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Fortunately, to overcome this problem, the PS texture can be stabilized against any restructuration at higher temperature by a first pre-oxidation step at low temperature in the range of 300 °C where the whole internal surface becomes covered by a thin oxide layer thermally stable (of 1-3 nm thickness). This has been verified by comparing the pore size distribution of samples pre-oxidized and then annealed for 1 hour at 800 °C under vacuum with that of as prepared PS samples. It appears that the pore size distribution is the same in both cases with a small shift toward smaller radii for the pre-oxidized samples due to the presence of the oxide layer grown along the pore walls [Her84].

It is obvious that the pre-oxidation step is not sufficient to ensure a full oxidation of the porous layer even if heating is performed for long periods of time. In fact, the temperature is not high enough to allow diffusion of oxygen through the formed surface oxide layer. We have recorded a saturation value of the oxidized fraction (which is defined as the percentage of silicon oxidized in the porous film) at around 20% after 1 hour of oxidation at 300 °C (calculation will be detailed in the next paragraph). Therefore, the complete oxidation of such a stabilized PS layer can only be obtained at high temperatures.

1.2. Toward a complete oxidation of PS

After anodization, all our PS samples of different porosities are subjected to a pre-oxidation of 1 h at 300 °C and then oxidized at different higher temperatures for different durations. Resulting oxides are then optically and electrically characterized in order to determine their quality and thus to optimize anodization and oxidation conditions (porosity, oxidation time and temperature).

1.2.1 OPS characterization using FTIR

In the following, we give the details of the procedure that allows us to determine the exact composition of OPS in silica, air and silicon using Fourier Transform InfraRed (FTIR) spectroscopy. We will thereafter try to answer to the questions: is PS completely oxidized? If not, for which conditions can we obtain a completely oxidized PS?

1.2.1.1 Measurement procedure

FTIR measurements are realized with a Brucker 80 spectrometer in the 400-5000 cm^{-1} (2-25 µm) spectral range in the reflection mode at room temperature in ambient conditions.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Before oxidation and just after anodization, porosity of each sample is determined through the measurement of its refractive index with FTIR. In fact, as shown in Figure 3, interferences of the infrared light on an as prepared PS layer, or more precisely constructive and destructive interferences between the beam reflected at the PS/air interface and the beam reflected at the Si/PS interface, are clearly manifested on the FTIR spectra by sinusoidal fringes. Assuming a normal incidence of incoming light, positions of the interference maxima satisfy the following equation:

$$p\,\lambda_{max}(p) = 2\,d\,n_{PS}, p \in \mathbb{N} \tag{1}$$

where n_{PS} is the refractive index of the PS layer, d is its thickness, λ_{max} is the wavelength corresponding to an interference maxima and p is an integer number corresponding to the maximum order. Consequently, the difference between numbers p_1 and p_2 related to any two maxima of the interference fringes allows to calculate the refractive index of the material according to the following equation:

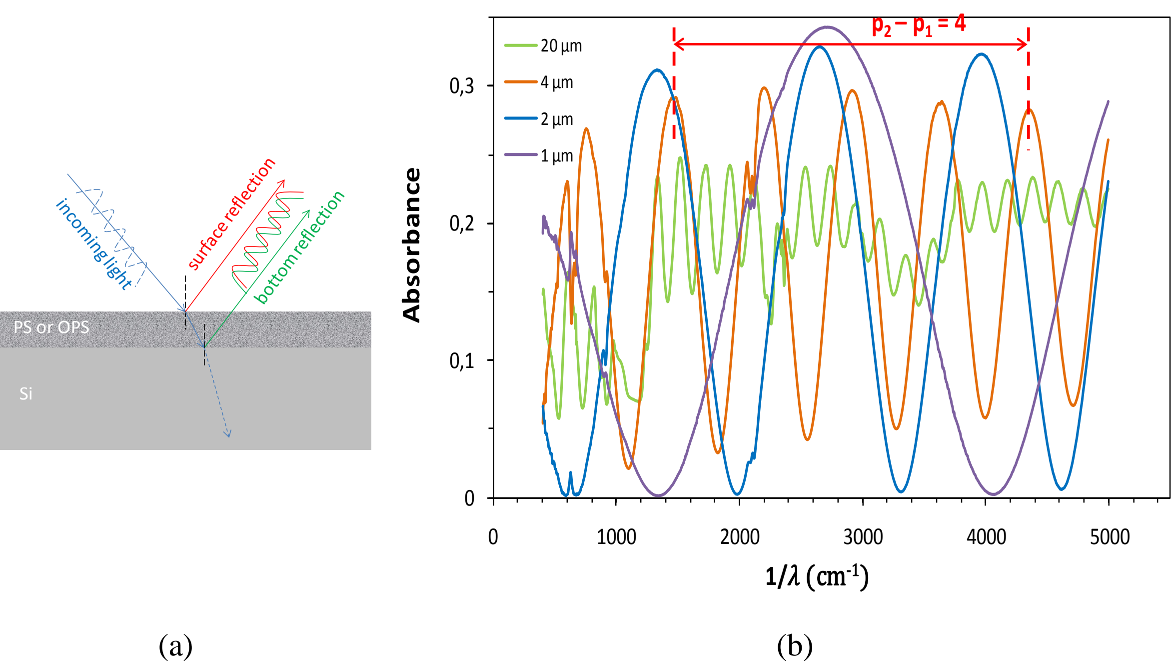
$$n_{PS} = \frac{p_2 - p_1}{2d} \times \left(\frac{1}{\lambda_{max}(p_2)} - \frac{1}{\lambda_{max}(p_1)}\right)^{-1} \tag{2}$$

The thickness d is a known parameter. While porosity is changed from one sample to another by changing the anodization current during the PS formation process, we have tried to maintain an almost constant PS layer thickness of 2 µm for all studied samples (see calibration charts in chapter 1). This value, which is also measured by cross sectional MEB observations, is chosen so that it approaches the thin thickness in the STI process but it also permits to obtain sufficient interference fringes for calculation in our 400-5000 cm^{-1} spectral range (Figure 3). Finally, according to the Landau-Lifshitz-Looyenga (3L) effective media model, one can estimate the porosity P of the PS sample that is interrelated to the refractive index as follows [Ale07]:

$$n_{PS}^{2/3} = (1 - P)\,n_{Si}^{2/3} + P\,n_{air}^{2/3} \tag{3}$$

where $n_{Si} = 3.4$ and $n_{air} = 1$ are the refractive index of silicon and air, respectively.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



(a) (b)

Figure 3 (a) A schematic view of optical interference on PS layer and (b) corresponding fringes on FTIR spectra for different layer thicknesses

It must be emphasized that we have verified porosities values obtained by FTIR measurements of some samples with those obtained by gravimetric measurements (described in chapter 1) and it appears that they are in a good agreement. This encouraged us to use the FTIR method for the characterization of the OPS structure. In fact, the 3L model can easily be applied to a multicomponent nanodispersed structure containing as many components as one may wish without any computing complications [Ale07]. The refractive index n can hence be expressed as follows:

$$n^{2/3} = \sum_i f_i \, n_i^{2/3} \qquad (4)$$

where n_i are the refractive indexes and f_i are the volume fractions of different components constituting a given nanodispersed system. Additionally, the condition $\sum_i f_i = 1$ should be satisfied.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

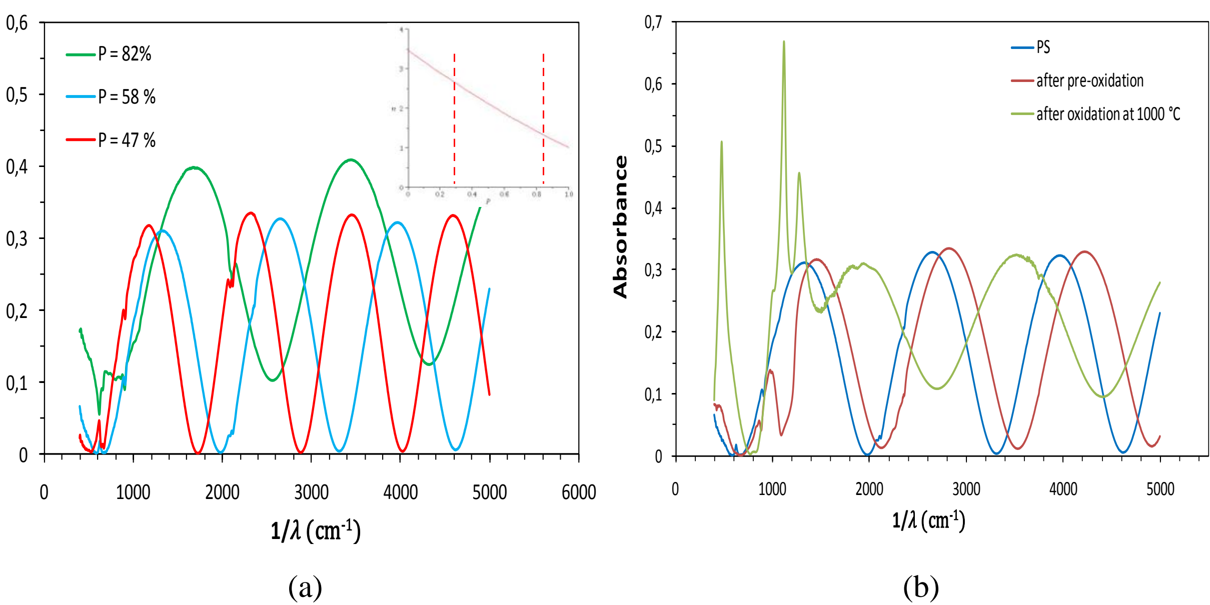


Figure 4 (a) FTIR spectra of PS layers with different porosities, shown in the inset the variation of the porosity with the refractive index and (b) FTIR spectra of PS after different thermal treatments

In the case of an oxidized PS layer, only three phases constitute the OPS nanostructure: silicon, silicon dioxide and air that fills the empty nanopores. Therefore, according to the 3L model given by equation 4, the refractive index n_{OPS} of such a system can be expressed as follows:

$$n_{OPS}^{2/3} = f_{Si} n_{Si}^{2/3} + f_{SiO_2} n_{SiO_2}^{2/3} + f_{air} n_{air}^{2/3} \quad (5)$$

where $n_{SiO2} = 1.5$ is the refractive index of silicon dioxide, f_{Si}, f_{SiO2} and f_{air} are the volume fractions occupied by silicon, silicon dioxide and air, respectively. The volume fractions of these three phases must satisfy the following equation:

$$f_{Si} + f_{SiO_2} + f_{air} = 1 \quad (6)$$

The aim being to determine f_{Si}, f_{SiO2} and f_{air} by measuring n_{OPS}, a third and last equation has to be added to Eqs. (5) and (6) to resolve our system of three unknowns. This equation comes from considering the volume expansion of the partially oxidized Si nanocrystallites. Indeed, the volume fraction of the reacted silicon $f_{Si}^{(R)}$ can be related to the volume fraction of the formed SiO_2 due to

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

$$f_{Si}^{(R)} = \frac{M_{Si}\rho_{SiO_2}}{M_{SiO_2}\rho_{Si}} f_{SiO_2} = 0.44 f_{SiO_2} \tag{7}$$

where M_{Si} = 28 g/mol, M_{SiO2} = 60 g/mol are the molar masses of silicon and silicon dioxide, respectively, ρ_{Si} = 2.33 g/cm^3 and ρ_{SiO2} = 2.2 g/cm^3 are the densities of silicon and silicon dioxide, respectively. Therefore, the volume fraction of the remaining (non oxidized) silicon f_{Si} can be expressed as

$$f_{Si} = f_{Si}^{*} - f_{Si}^{(R)} = (1-P) - f_{Si}^{(R)} = 1 - P - 0.44 f_{SiO_2} \tag{8}$$

where f_{Si}^{*} is the volume fraction of silicon nanocrystallites in the initial as prepared PS sample (before oxidation). From Eqs. (6) and (8), one can also express f_{air} as follows:

$$f_{air} = P - 0.56 f_{SiO_2} \tag{9}$$

Finally, taking into account Eqs. (3), (5), (8) and (9), the following relation can be derived allowing the determination of f_{SiO2} in an OPS layer (and thus f_{Si} and f_{air} according to Eqs. (8) and (6)) just by calculating the difference between measured refractive indexes of PS before (n_{PS}) and after oxidation (n_{OPS}).

$$n_{PS}^{2/3} - n_{OPS}^{2/3} = f_{SiO_2}\left(0.44\, n_{Si}^{2/3} - n_{SiO_2}^{2/3} + 0.56\, n_{air}^{2/3}\right) \tag{10}$$

The oxidized fraction which is defined as the percentage of silicon oxidized in the porous film can then be expressed as follows

$$\xi_{ox} = \frac{f_{Si}^{(R)}}{f_{Si}^{*}} = \frac{0.44 f_{SiO_2}}{1-P} \tag{11}$$

1.2.1.2 Results and Discussion

Table 1 shows FTIR measurement results of some investigated samples after anodization and oxidation under different conditions. We decided to give in the table the corresponding thickness of silicon dioxide grown on a bare Si sample for each oxidation process and which is measured by ellipsometry. In fact, we are not sure of the mass flow value of oxygen in our furnace (problem with the flow meter) which may lead to uncontrolled

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

oxide growth. It should also be mentioned that no dispersion of light path (nxd) values is observed in the plane direction for FTIR measurement on a same sample, that is to say, nearly the same FTIR spectra is obtained when changing the position of the light spot (of about 1-2 mm of diameter) over the sample surface (of about 1 cm^2). The main source of error in the determination of the refractive index of the (oxidized) PS layer, and then the volume fractions of its different components, comes from the determination of its exact thickness.

Calculation is done by resolving above equations (Eqs. (3), (6), (8), (10) and (11)) in MATLAB.

Table 1 FTIR measurement results

		Oxidation conditions		**FTIR measurement**			
Sample #	**P %**	**(T,t)**	**t_{ox} (nm)**	**f_{SiO2}**	**f_{Si}**	**f_{air}**	**ξ_{ox}**
1	82	(1000°C,1h)	120	0.38	0	0.62	1
2	73			0.62	0	0.38	1
3	58			0.87	0.03	0.1	0.92
4	47			0.84	0.16	0	0.7
5	46	(1000°C,2h)	125	0.85	0.15	0	0.7
6	65	(800°C,1h)	50	0.39	0.18	0.43	0.5
7	60			0.56	0.15	0.29	0.62
8	50			0.62	0.22	0.15	0.55
9	58	(800°C,2h)	52	0.54	0.18	0.27	0.57
10	57	(800°C,4h)	55	0.56	0.18	0.26	0.58

It is well expected that oxidation kinetics of PS depend on both oxidation time and temperature. The oxidized fraction ξ_{ox} is found to increase with temperature and saturates after 1 hour of oxidation at 800 °C or 1000 °C. A saturation value of 0.5 - 0.6 (samples # 8, 9 and 10) is recorded at 800 °C while a complete oxidation (ξ_{ox} = 1) is reached at 1000 °C (samples # 1, 2 and 3). However, it appears that full oxidation of PS layer can only be achieved if the initial porosity is high enough. For example, for samples # 4 and 5, ξ_{ox} equals

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

only 0.7 after 1 h or 2 h of oxidation at 1000 °C and the final material is only composed from silicon and silicon dioxide without air. The structure can be represented as remnants of Si crystallites immersed in SiO_2 matrix and whose oxidation becomes more difficult because the diffusion of oxidation species is hindered by the formed oxide.

In conclusion, the oxidation of PS and hence the characteristics of the resulting oxide is shown to be determined by the oxidation conditions and the initial porosity of the layer after anodization. Porosity around 56% (sample # 3) seems to be optimum to ensure full oxidation of PS (i.e. having an oxide without residual Si crystallites that may degrade its electrical and thermal isolation properties) and to obtain an oxide with minimum porosity. A porous oxide is not preferable since it may cause some problems during subsequent IC fabrication processes; it can capture impurities and may also be etched off easily in HF (a dissolution rate in buffered hydrofluoric acid BHF solution can be many times higher than that expected from standard thermal oxide). On the other hand, the 56% porosity permits to avoid any possible wafer warpage and defects development that can be caused by elastic stresses due a change in the volume of PS after oxidation (expansion if the porosity is lower than 56% and contraction if higher). Finally, it should be noted that even a 56% of initial porosity cannot avoid a somewhat porous character of the final OPS with the presence of microscopic closed cavities of a few nanometers due to the chaotic nature of the initial PS structure. So, annealing at high temperature can be performed in order to be sure to obtain a dense oxide, with characteristics similar to standard thermal SiO_2. This last step of densification, as proposed by some authors [Bom88,Yon87], is achieved by a viscous flow of silica and requires temperatures higher than 1000 °C. For reasons of temperature limitation in our furnace, we have not done this step.

1.2.2 Complementary characterization using CV measurements

The OPS samples are also subjected to capacitance-voltage C-V measurements. For that, rectangular and circular aluminum pad contacts of various dimensions (areas between 0.25 - 2.5 mm^2) are deposited on the top of the OPS layer through a shadow metallic mask by conventional thermal evaporation. No annealing is performed and the ohmic back side contact is made by scratching the silicon surface with a diamond tip and rubbing InGa eutectic.

The capacitance measurements are carried out in a probe station at room temperature in air at darkness using a 4284A Hewlett Packard impedance analyzer. The frequency is set at

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

100 kHz, 50 mV of signal amplitude and 50 mV of voltage step are used. Figure 5 shows the C-V characteristics obtained for different samples with capacitance values normalized to 1 cm^2 area and 1 µm thickness of the layer.

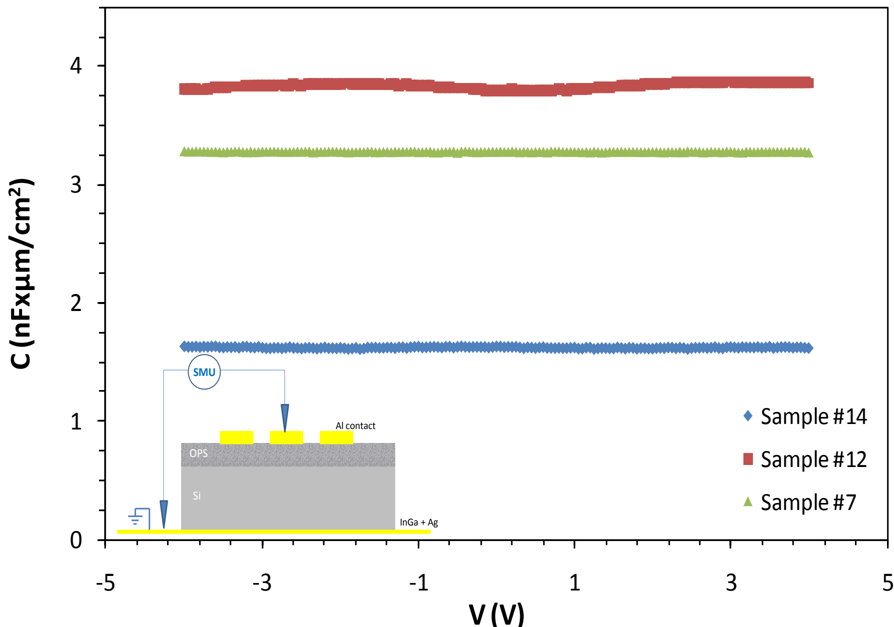


Figure 5 Capacitance-voltage characteristics of OPS samples. The inset shows a schematic representation of investigated samples

It is obvious that the measured capacitance of the fabricated MIS device with the oxidized PS as an insulator is kept constant with voltage and is also frequency independent in the 100 Hz - 1 MHz frequency range. In fact, this value corresponds to the oxide capacitance:

$$C_{OPS} = \frac{\varepsilon_{OPS}\, S}{d} \tag{12}$$

where S, d are the surface and the thickness of the OPS layer, respectively and ε_{OPS} is its corresponding dielectric constant. There is no contribution of the space charge region to the total dielectric response over the whole range of voltage because the space charge region width is still negligible compared to the 2 µm OPS thickness, mainly for highly doped silicon substrate (the maximum width of the surface depletion region is equal to 30 nm for the investigated wafers of 5 x 10^{18} cm^{-3} doping concentration [Sze01]). From C_{OPS}, one calculates the dielectric constant of OPS (according to Eq. 12). We neglect in our calculation the capacitance of the silicon dioxide grown on the substrate at the bottom of the OPS layer (Figure 2.c). Actually, this capacitance is connected in series with the OPS capacitance and it

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

is very large as the corresponding layer thickness t_s is very small (less than 150 nm in the worst case).

For the analysis of experimental data, we have compared measured OPS dielectric constants with ones calculated using the Maxwell-Garnett's effective medium theory. The latter describes the macroscopic properties of a composite mixture based on the properties and the relative fractions of its components. It considers the averaging effects between local electric fields of inclusions (air and silicon dioxide in our case) randomly embedded in a host medium (silicon), in the presence of external electric field [Mer99,Hua06]. In the Maxwell-Garnett's model, the OPS dielectric constant can be expressed as follows:

$$\frac{\varepsilon_{OPS} - \varepsilon_{Si}}{\varepsilon_{OPS} + 2\varepsilon_{Si}} = f_{SiO_2} \frac{\varepsilon_{SiO_2} - \varepsilon_{Si}}{\varepsilon_{SiO_2} + 2\varepsilon_{Si}} + f_{air} \frac{\varepsilon_{air} - \varepsilon_{Si}}{\varepsilon_{air} + 2\varepsilon_{Si}} \quad (13)$$

where f_{Si}, f_{SiO2} and f_{air} are the volume fractions occupied by silicon, silicon dioxide and air, respectively and which are previously determined by FTIR measurements. $\varepsilon_{SiO2} = 3.9$, $\varepsilon_{Si} = 11.9$ and $\varepsilon_{air} = 1$ are the dielectric constants of silicon dioxide, silicon and air, respectively. Table 2 shows measured and calculated dielectric constants of selected samples. A good agreement between experimental and calculated values is observed.

Table 2 Experimental and calculated values of the dielectric constant of some OPS samples

Sample #	ε_{OPS} (theo.)	ε_{OPS} (exp.)
7	3.92	3.48
3	3.79	3.75
9	4.16	3.82
4	4.96	4.26
11	4.16	4.17
12	3.11	3.31
13	2.11	1.86

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf

© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

In conclusion, the CV measurement can be utilized as a second method to determine the composition of the OPS structure. Whereas in FTIR we measure the refractive index, in the CV method we measure the dielectric constant. This latter can be tuned by controlling both the volume fraction of constitutes and the starting porosity of the PS material. Figure 6 shows a chart of OPS dielectric constant variations for three different starting PS porosities obtained according to Eqs (6), (7) and (13). The chart could be useful for a preliminary study when one wants to set the dielectric constant of an OPS layer.

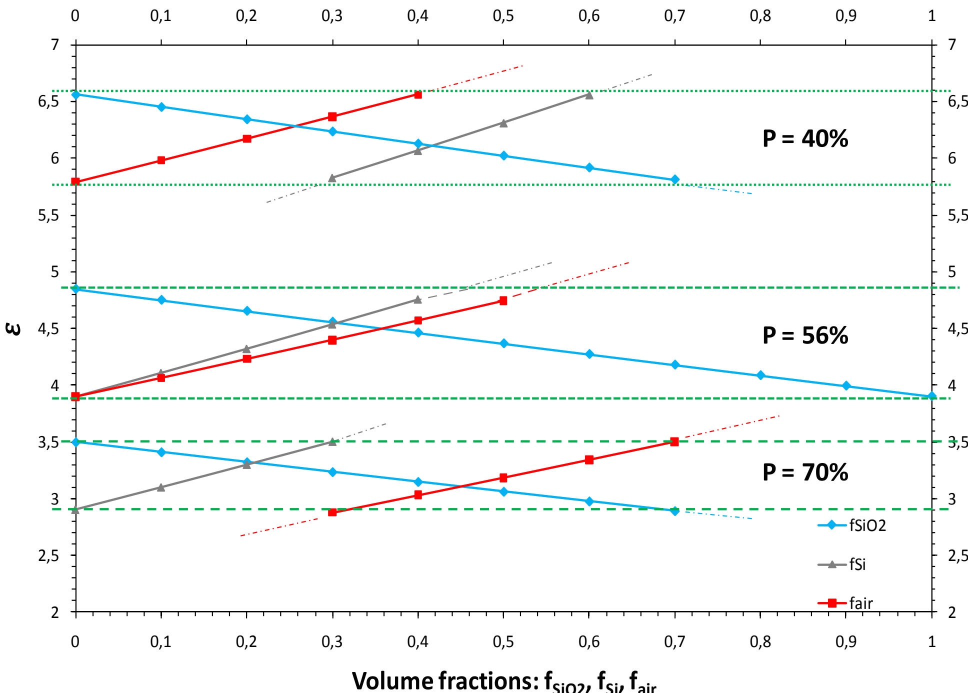


Figure 6 OPS dielectric constant variations with silicon dioxide, silicon and air volume fractions for three different starting PS porosities, green dashed line delimits the calculation domain validity. The structure composition can be easily determined if a ruler is placed horizontally over the chart

2. Fabrication of local OPS

In this section, we highlight the selective formation of oxidized PS with giving the optimized conditions of anodization and oxidation processes that were studied in the previous parts.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Figure 7 shows the I-V characteristics of both p- and n-type silicon during PS formation for different doping concentrations. The shift observed toward the doping level of silicon, and whose the origin was explained in chapter 2, will be exploited here to selectively form PS in differently doped regions. In fact, when a silicon wafer of different regions of doping concentration is anodized at a fixed current or potential, the dissolution current will only flow through regions of higher doping level and PS formation can only take place there.

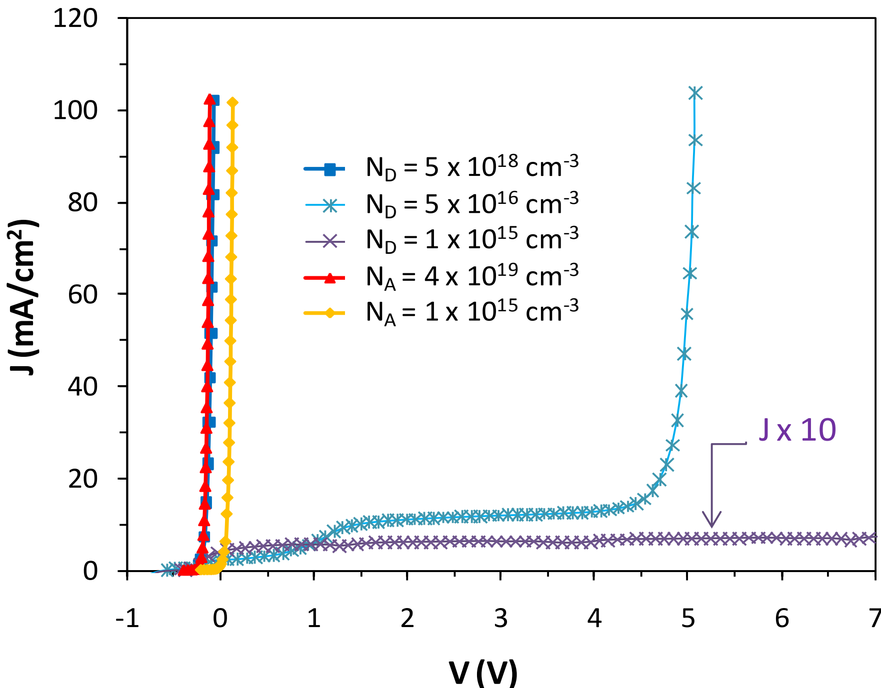


Figure 7 Anodic current-voltage characteristics of n and p-type silicon in hydrofluoric acid (HF) solution for substrates of different doping concentrations, V is referred to the silicon electrode potential vs. an Ag/AgCl reference electrode

The structures to be oxidized are arrays of squares of different dimensions (from 0.5 to 5 µm side) which are heavily implanted with phosphorous in a low n-doped silicon wafer ($N_D = 10^{15}$ cm^{-3}) through a patterned mask of silicon dioxide. The n-type substrates are preferred rather than the p-type considering their higher selectivity as shown above in Figure 7.

It should be also noted that there is less significant variations of the porosity with the current density for n-type silicon rather than p-type (see calibration curves in chapter 1) which it can ensure a homogenous in-depth porosity when the sample is anodized at a constant potential and allow more reproducible results from run to run. The implanted dose (D = 5 x 10^{14} cm^{-2}) and energy (E = 50 keV) with the drive-in conditions (900 °C during 5 min) are

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

chosen such that the doping concentration will be relatively uniform (10^{19} cm^{-3}) throughout a depth of about 200 nm and so the resulting PS would exhibit a uniform porosity. Figure 8 shows the simulation of the doping profile using ICECREM tool. ICECREM (from Fraunhofer Institute, Erlangen) is an advanced one-dimensional analytical simulator that can offer quite good results [Fra04]. It had been shown that it just presents a discrepancy with the SIMS data in the tail of the doping distribution due to model deficiencies and mainly to the ion channeling phenomenon which is not readily implemented in analytic simulators.

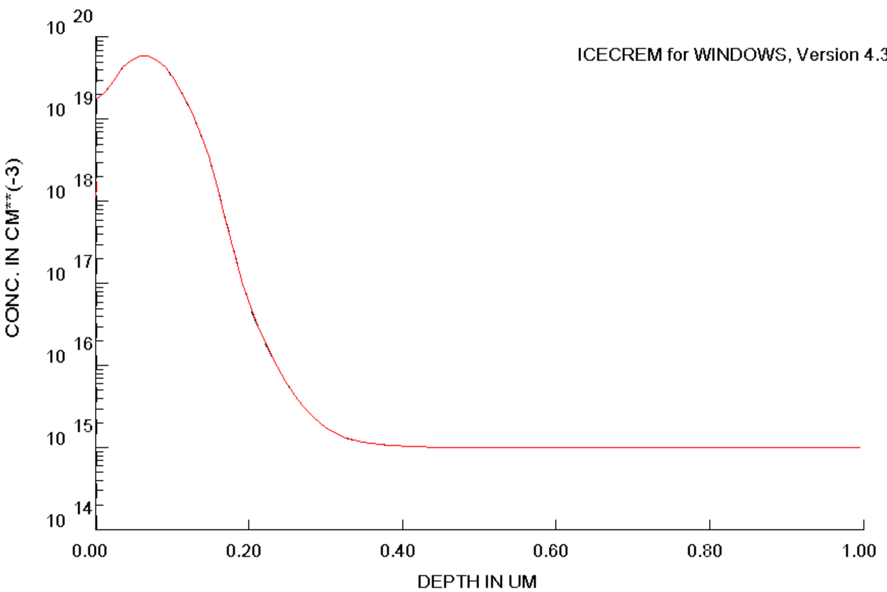


Figure 8 Simulation of phosphorous implantation (50 keV energy and $5x10^{14}$ cm^{-2} dose) into <100> n-type silicon (of 10^{15} cm^{-3} doping concentration) followed by annealing at 900°C during 5 min

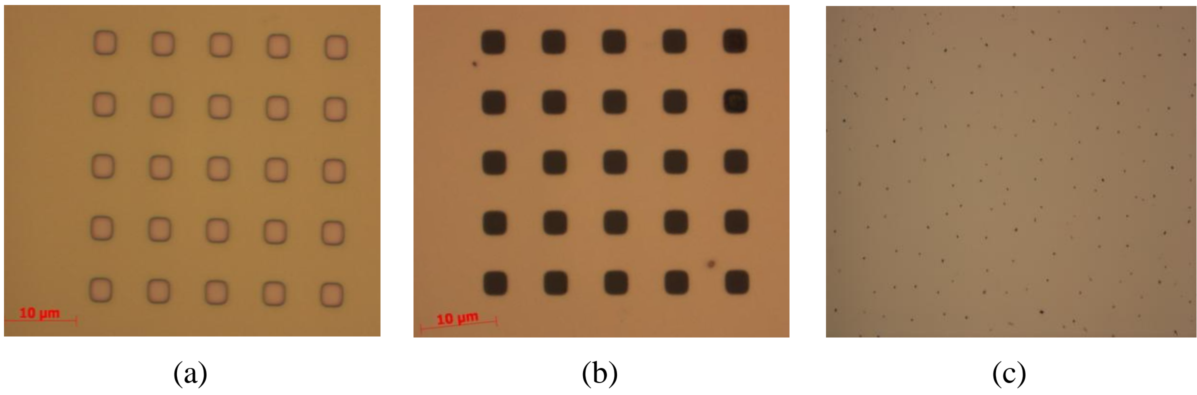
2.1. Electrochemical anodization

At this stage, it is worth mentioning that samples, as provided by STMicroelectronics, have a schematic representation similar to that described in Table 3 of chapter 1 after the resist stripping step.

After SiO_2 stripping, the wafer is anodized in hydrofluoric acid (HF) at a well chosen constant voltage that allows the dissolution reaction to be only restricted to the higher doping regions. Potentiostatic regime (or anodization at a constant potential) is preferred as it does not need any determination of the current to be applied and thus no hard calculation of the exposed area expected to be anodized is required. The etch time is 20 s which is largely

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

sufficient to form PS over the entire depth of the highly doped region. The anodizing conditions (HF concentration and current density) are adjusted according to the calibration curves of chapter 1 so that as far as possible the PS layer has a porosity around 56%. Such a porosity allows first a full oxidation of the layer as demonstrated before and second avoids wafer warpage due to the expansion rate of silicon dioxide. It has been shown that the porous layer exhibits a volume change after oxidation (expansion if the porosity is lower than 56% and contraction if higher) which it can introduce elastic stresses [Barl86,Hol83]. Furthermore, the applied voltage should not be very high (< 1 V) to avoid breakdown of the silicon surface (Figure 9.c). We have noticed for example a breakdown with applied voltages of 2.95 V (corresponding to a current density of 40 mA/cm^2) and 2.58 V (corresponding to a current density of 200 mA/cm^2) for 12% HF and 25% HF, respectively.

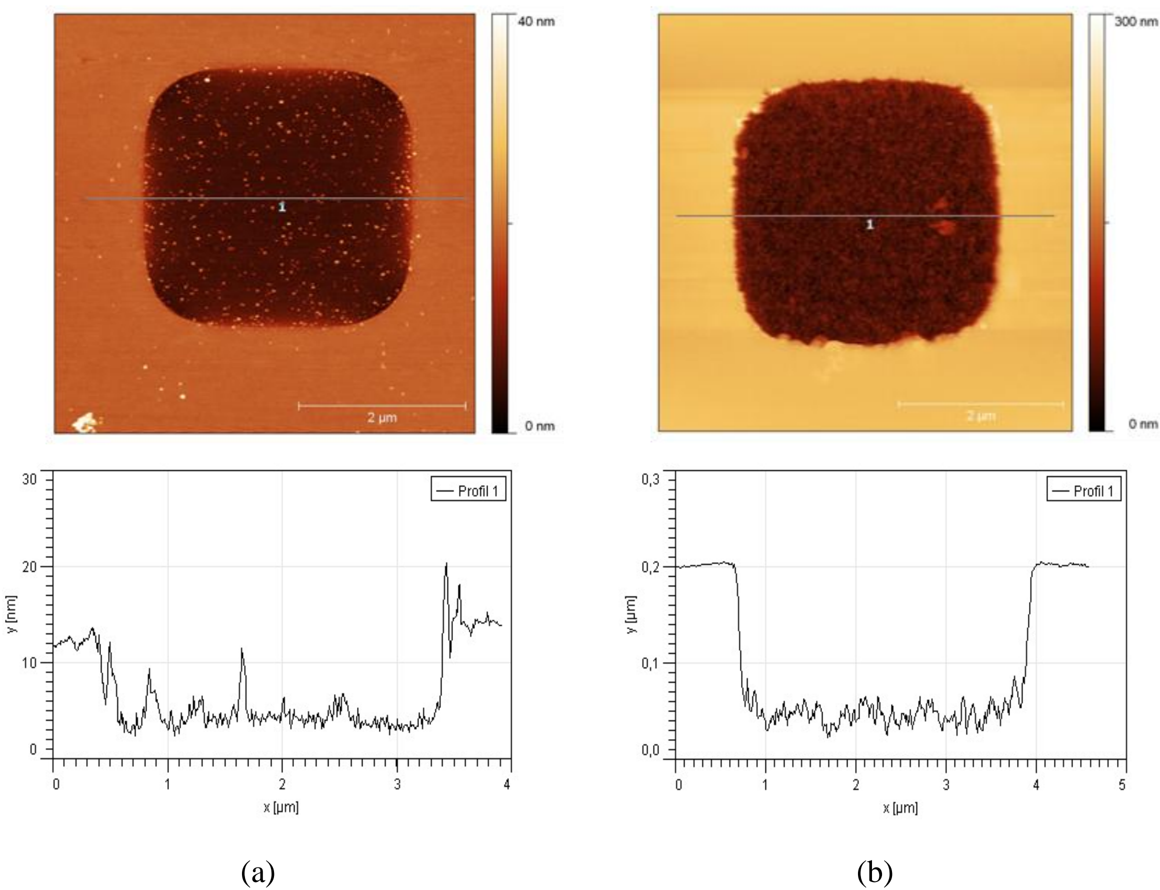


(a) (b) (c)

Figure 9 Top view (optical microscopy) of the sample (a) before SiO_2 stripping (b) after anodization and (c) with a breakdown surface after anodization at high voltage

Figure 10 shows the atomic force microscope (AFM) topography images of the sample with their profiles after anodization and after immersion in KOH solution (a high selective etchant of PS relatively to bulk Si). It can be revealed that PS is formed exclusively in the n+ doped regions; the etching process occurring only in those regions and self-stopping on the lightly doped regions is in a good agreement with the implantation profile.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



(a) (b)

Figure 10 AFM topography images with profiles of the sample after anodization (a) before and (b) after KOH etching

2.2. Oxidation

After anodization, the wafer exhibits a two-step oxidation process as described before. A pre-oxidation at 300 °C for 1 h to stabilize the porous structure against any restructuration at higher temperature (pores collapsing and texture coarsening) followed by an oxidation at 1000 °C during 2 h to transform completely the PS into silicon dioxide.

Figure 11 also confirms that OPS is locally formed in the highly doped regions of the wafer.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

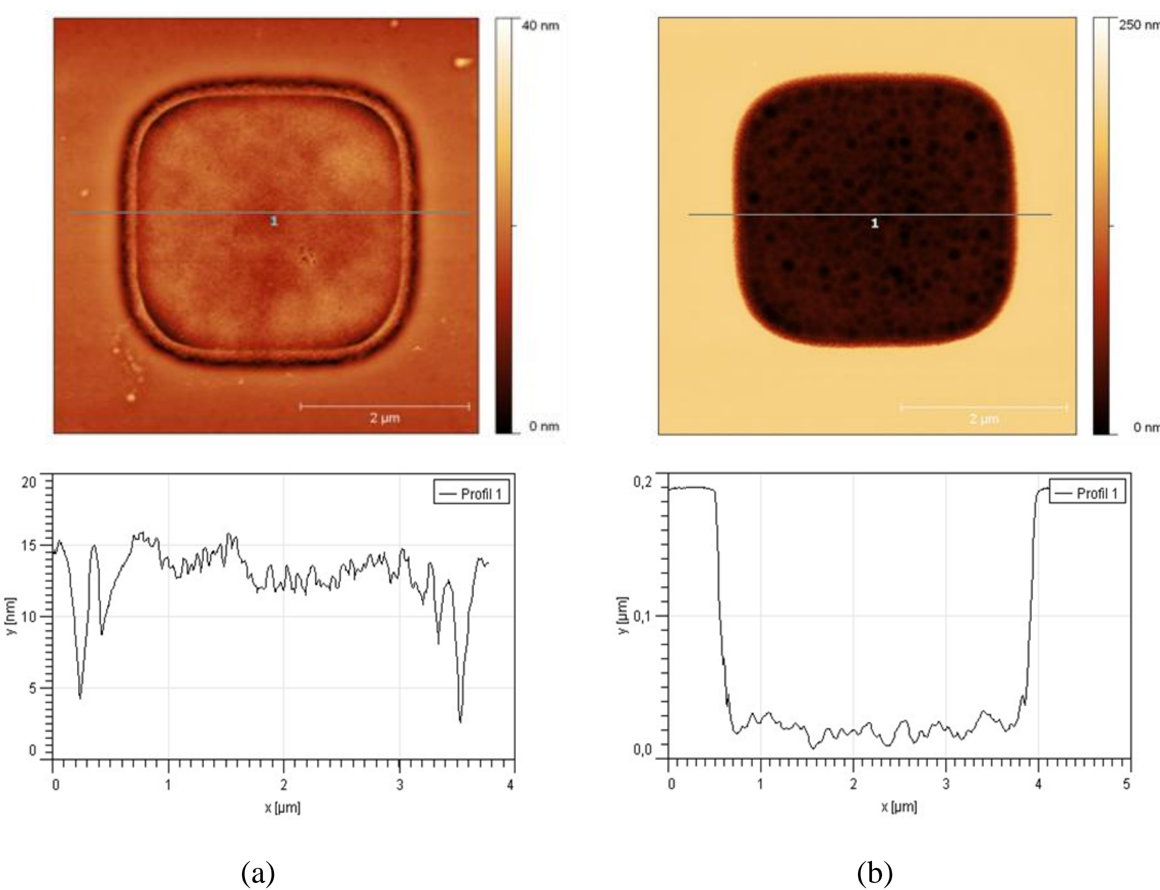


Figure 11 AFM topography images with profiles of the sample after anodization and oxidation (a) before and (b) after buffered HF etching

Scanning electron microscopic (SEM) inspection of the OPS sample shows a relatively planar and uniform structure (Figure 12). This has been ensured by adjusting the anodization conditions to produce a PS layer with porosity around 56% so that wafer warpage due to the expansion rate of silicon dioxide can be avoided. On the other hand, stalks of oxide are however observed at the bottom of the OPS layer which may lead to a high level of defects and poorer electrical properties of the Si/oxide interface. These stalks correspond more likely to the oxidation of silicon macro crystallites after PS formation in the lightly doped n-Si substrate. In fact, the anodization process does not stop as soon as the whole n+ layer has been converted into PS but it continues to proceed slowly in the low doped region. As the porous epilayer/bulk interface is not planar and since the junction breakdown onset does not only depend on the doping concentration and the applied bias, but also on the junction geometry [Sze06], around a depression in the low doped silicon surface the depletion region width is decreased and the field strength is increased, which leads to a premature breakdown and thereby to a local current density there. Optimizing anodization conditions, in

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

particular the etching time, could overcome this problem. Finally, one can also mention a slight lateral extension of the OPS which presents a chief constraint for CMOS isolation due to active areas losses. We believe that this effect is rather dependent on the lateral straggle of doping (the deviation of implanted ions from the incident direction) and it is not due to the isotropic nature of PS formation. It can be hence reduced by tailoring the ion implantation process.

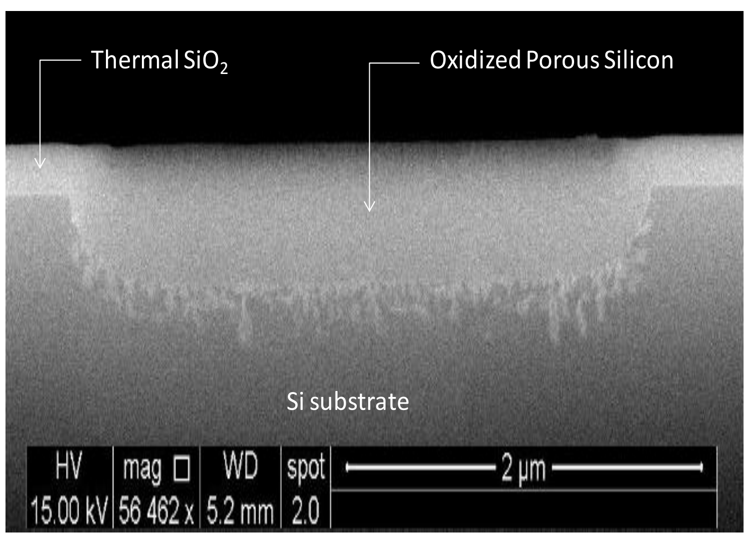


Figure 12 SEM cross-sectional image of an oxidized porous silicon layer

3. Dielectric properties of OPS: investigation of current-voltage characteristics

This section is particularly dedicated to study the electrical behavior of oxidized porous silicon (OPS) through the investigation of current-voltage I-V characteristics. We try to determine the dielectric properties of OPS and to compare them to those of standard thermal silicon dioxide. In addition, even if it is not our main concern, pre-oxidized samples have also been characterized.

I-V measurements are performed under dark conditions in a two-terminal configuration as shown in the inset of Figure 5. The voltage is applied between the metallic contact on top and the ohmic back contact grounded, and the current is recorded using a Keithly 4200-SMU system. For the temperature dependence of the I-V characteristics,

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

measurements are carried out in the range of 100-300 K inside a gaz-nitrogen cryostat. The samples are placed on a heater stage inside a vacuum chamber (10^{-4} mTorr pressure) and the temperature is stabilized by a Lakeshore 331 controller. It should be cautioned that at room temperature, characterization of pre-oxidized samples is realized in vacuum in order to obtain reproducible I-V characteristics. In fact, the electrical behavior of these porous samples is very sensitive to the ambient atmosphere due to their large contact area with air.

3.1. Pre-oxidized PS samples

Our purpose here is to discuss the potential distribution across the pre-oxidized porous sample and to examine the possible charge carriers transport mechanisms. As the structure is a pre-oxidized porous layer sandwiched between a metal contact and the Si substrate, one can consider that current could be limited either by the "bulk" OPS, or the OPS/Si heterointerface, or also the Schottky barrier between the OPS and the metal electrode. Figure 13 shows the I-V characteristics of Al/OPS/(20 mΩcm)-p-Si structures with OPS layer of different thicknesses. The forward bias corresponds to the case where a negative bias is applied to the top of Al contact. It is remarkable that the I-V characteristic of the structure with relatively thin (0.5 μm) OPS layer differs significantly from those of thick layers. It follows at forward bias an exponential dependence with an ideality factor n of 5: $I = I_0 (\exp(qV/nkT) - 1)$ (where I_0 is the pre-exponential factor, q the electron charge, k the Boltzman constant and T the temperature).

According to several authors [Ben95,Bal01,Bala01,Gie95,Isl07 and Yar04], this rectifying behavior originates from a band bending and a depletion inside the Si substrate at the OPS/Si heterojunction. In fact, it could be supposed that oxidation results in a high density of charged states in the oxide layer that is formed over the surface and so, the OPS/Si interface behaves like a Schottky diode, where the OPS plays the role of a metal. In other words, since the pre-oxidized PS has a high density of states, no depletion should occur at the metal/OPS interface where this contact should behave almost in an ohmic manner, while on the other hand, the high density of states might pin the Fermi level at the other heterojunction (the OPS/Si boundary) and results in a band bending inside the Si. This assumption is supported by the fact that I-V characteristics had been shown to be insensitive to the type of the metal used, as well as other photovoltaic effects observed in oxidized PS layers [Ben95]. Nevertheless, some other papers [Der95,Dim95,Mar92,Rem03 and Sim95] have suggested

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf

© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

that a rectifying I-V characteristic of a metal/OPS/Si structure is rather due to the Schottky barrier at the metal/OPS interface.

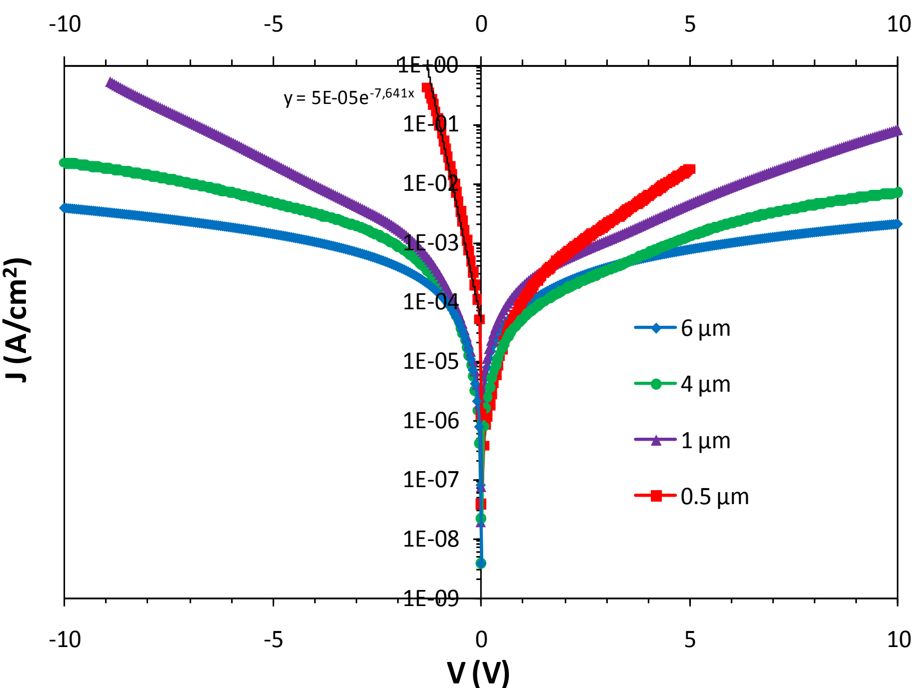


Figure 13 I-V characteristics at room temperature of pre-oxidized Al/PS/(20 mΩcm)-p-Si structures of different OPS layer thicknesses. The structures were fabricated with a PS of about 60% porosity. The area of the Al electrode was about 10^{-2} cm^2.

At relatively low forward biases where the I-V curves are shown to be close to the linear regime (ohmic), one can determine the activation energy of conductivity E_A for pre-oxidized PS from temperature dependences. Figure 14 shows a thermally activated behavior: $\sigma = \sigma_0 \exp(-E_A/kT)$ (where σ_0 is the conductivity pre-factor). We have found an activation energy $E_A = E_C - E_F = 0.28$ eV which is very close to that obtained in [Bal01 and Yar04]. A schematic band diagram of the pre-oxidized Al/PS/p-Si structure is then shown in the inset of Figure 14 as proposed by [Bal01].

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

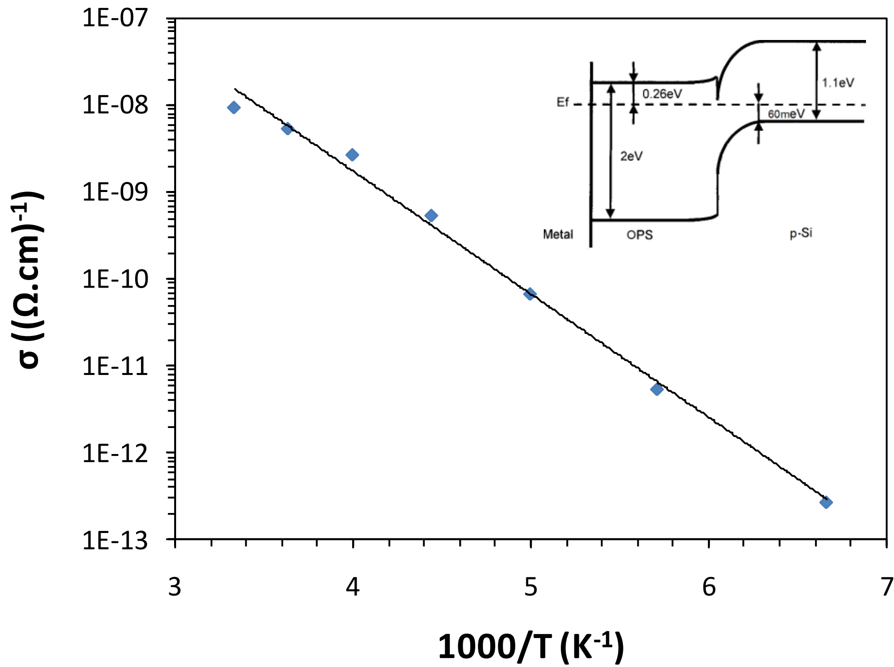


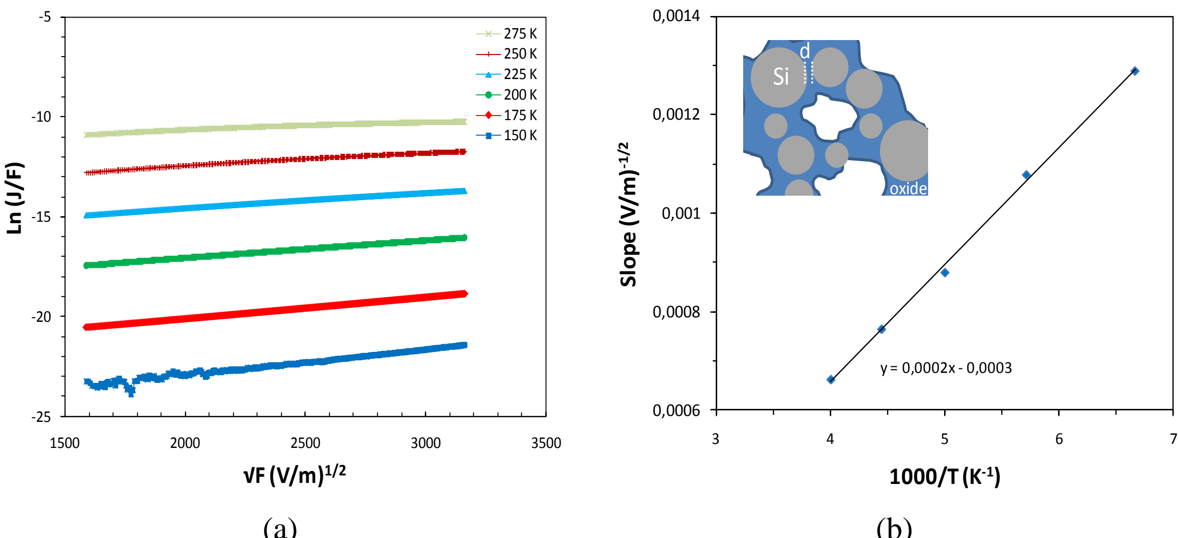
Figure 14 Temperature dependences of the conductivity of a 2 µm thick pre-oxidized PS layer, made from p-type substrate and 60% porosity of PS. Inset shows the energy band diagram of an oxidized Al/PS/p-Si structure as proposed by [Bal01].

The fact that the ideality factor is large for the I-V characteristic of the structure with relatively thin (0.5 µm) OPS layer suggests that the applied bias does not only drop across the barrier, but also on the PS layer. This could explain that the main cause of deviation from rectifying behavior for the I-V curves of thick structures is due to an increase of the series resistance R_{PS} of the PS layer. That is to say, when the 'bulk' porous layer becomes thick, the total voltage drops on this resistance R_{PS} that limits the current and hinders the potential barrier effect. Consequently, the I-V characteristic will not exhibit a rectifying behavior but will be symmetric with respect to the voltage polarity (i.e. the current will have almost the same magnitude for both voltage polarities). It should be noted that R_{PS} is voltage dependent as it can be seen from the non-linearity dependence of the current on the applied voltage. This dependence is considered in order to determine the conduction limiting mechanism. By analyzing the forward I-V characteristics at sufficiently high bias as a function of temperature, we found that the current is thermally activated and Ln(J/F) is proportional to the square root of the applied electric field F as shown in Figure 15.a, which leads us to assume that the current is predominantly controlled by a Poole-Frenkel conduction (Figure 16.a). A simple Poole-Frenkel model is given by [Bus01]:

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

$$J_{PF} = A_{PF}.F.e^{\frac{B_{PF}.\sqrt{F}}{k.T}} \; with \; B_{PF} = \sqrt{\frac{q}{\alpha_{PF}.\varepsilon_{ox}.\pi}}$$

where J_{PF} is the current density, A_{PF} a pre-exponential constant, F the applied electric field and ε_{ox} the oxide permittivity. The extracted parameter α_{PF} gives the average distance between charge states using the chart of Figure 16.b [Bus01]. We found α_{PF} equals to 3-3.5 which corresponds to a distance in the 1-2 nm range. This later value is consistent with the fact that the transport mechanism in the pre-oxidized PS volume is due to Poole-Frenkel conduction between states confined at the interface between Si crystallites and the thermally grown oxide (Figure 15.b).

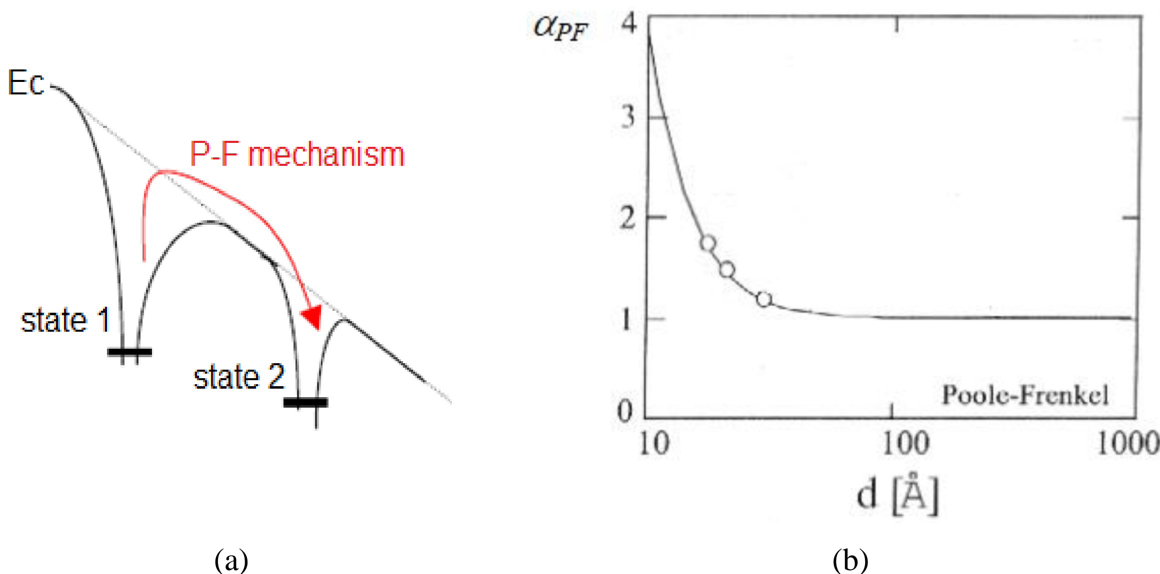


(a) (b)

Figure 15 Ln(J/F) vs. √F (Poole-Frenkel plot) at high forward electric fields of the pre-oxidized Al/PS/Si structure for different temperatures, (b) Slope of Poole-Frenkel plots as a function of a reciprocal temperature. The inset shows a schematic representation of the pre-oxidized PS structure consisting of silicon crystallites immersed in an oxide matrix

Finally, it should be noted that our study, assuming a Poole-Frenkel-like behavior of the conductivity in the non-linear regime, is in agreement with the work of Wu et al. [Wu96]. However, there are other studies on transport in thermally oxidized PS that describe the results with other models (a free carrier or trap filled space charge limited current (SCLC) conduction mechanism [Bal01,Bal00,Rem03 and Yar04], or also a generation/recombination process in the Si depletion region [Bala01 and Dim95]).

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés



(a) (b)

Figure 16 (a) Energy band diagram showing the Poole-Frenkel conduction mechanism. The emission of electrons from the states into the conduction band is a thermionic emission process. (b) Variation of the parameter α_{PF} with the distance between traps, after [Bus01]

3.2. Oxidized PS samples

I-V measurements are used to characterize OPS as well. Figure 17 shows the I-V characteristics at room temperature of an OPS layer compared to a pre-OPS layer of a same thickness (2 µm). It is clear that the current density is deceased by 3-4 orders of magnitude after oxidation of the sample at high temperature. From the lower current density region, we have estimated the resistivity of the layer to be on the order of 10^8 Ωcm for pre-OPS against 2.10^{13} Ωcm for OPS (Table 3). Moreover, the leakage current density of the OPS layer as measured between the top Al pad and the silicon substrate is less than 1 µm/cm^2 at 10 V bias. This value is found to be close to that reported in the work of Holmstrom [Hol83] and Yako [Yak00] which is of 0.1-0.5 µA/cm^2 at 10 V for an almost OPS layer thickness.

Table 3 Comparison between resistivity values of pre-OPS, OPS and thermal silicon dioxide

Pre-oxidized PS	Oxidized PS	Thermal silicon oxide
10^8 Ωcm	2.10^{13} Ωcm	10^{15} Ωcm

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

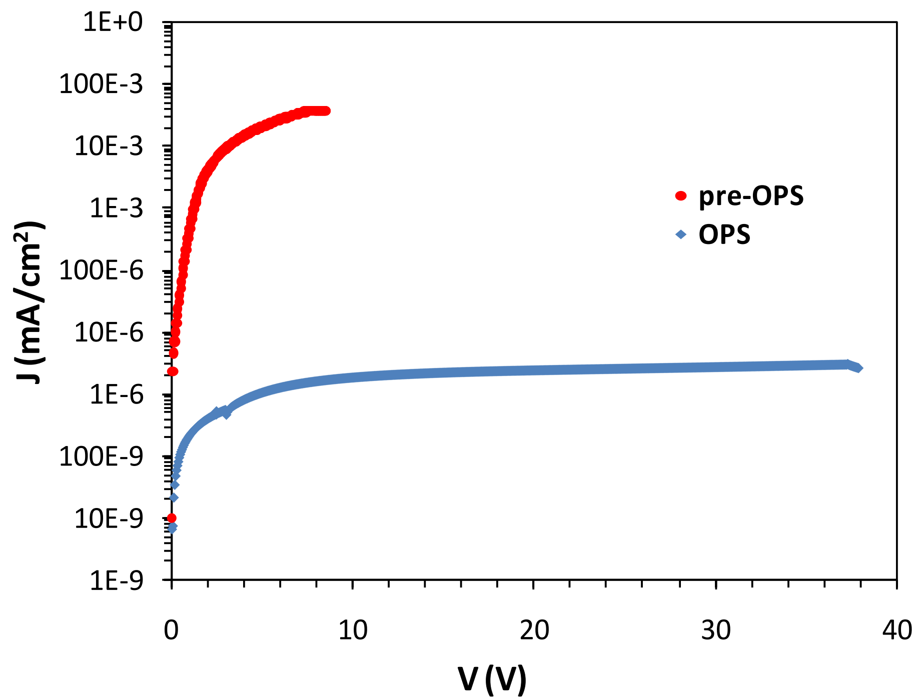


Figure 17 I-V characteristics of 2 µm pre-oxidized and oxidized PS layers at room temperature

In summary, it can be said that good electrical isolation properties (resistivity and leakage current) are obtained for OPS and they can approach those of standard thermally grown oxide with 10^{15} Ωcm resistivity. We believe that these good properties are due, in large part, to the presence at the OPS/Si interface of a thin oxide layer which grows in the substrate during oxidation of the porous layer and which stabilizes the interface (Figure 2.c). Therefore, they can be further improved if a cleaning step of the silicon surface is well performed before processing or the anodization step is more optimized.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Conclusion

FTIR measurements have allowed the characterization of oxidized porous silicon and hence the study of the oxidation kinetic of PS. Actually, through the measurement of the refractive index of an OPS layer, we have determined for various anodization and oxidation conditions the volume fractions of the three components (silicon, air and silicon dioxide) constituting the layer using the 3L effective media model. In the light of FTIR results presented in this chapter, it clearly appears that complete oxidation of PS is at least achieved by two oxidation steps: a primordial pre-oxidation step to stabilize the texture against any restructuration during further heat treatment followed by an oxidation at higher temperature to fully transform the porous layer to oxide. A last step of densification at temperatures higher than 1000 °C could also be envisaged in order to obtain a more dense oxide. On the other hand, the electrochemical anodization parameters have to be settled to produce a PS layer with porosity approaching 56%. Such a value is required to ensure a good quality oxide without residual Si crystallites and with minimum porosity.

Furthermore, the chapter has shed the light on the selective formation of OPS due to the dependence of PS formation with the silicon doping concentration. From SEM and AFM observations, we have shown that OPS is exclusively and locally formed in highly doped regions implanted on a lightly doped wafer. Taking advantage of the preliminary study of PS formation (chapters 1 and 2) and its well-controlled oxidation procedure, we have also given some helpful recommendations which are useful for the fabrication process of local OPS with a relatively planar and uniform structure. As example, it has been suggested that n-type silicon is more preferred than p-type as far as it first exhibits higher selectivity for PS formation and second it manifests less variation of the porosity with the current density which allows a homogenous in-depth porous structure and more reproducible results. Moreover, besides adjusting anodization parameters in order to obtain 56% porosity, a potentiostatic regime should be employed with a sufficiently low applied bias to avoid breakdown of the silicon surface.

Finally, we have also performed capacitance-voltage C-V measurements on OPS layers allowing the determination of their dielectric constant. Measured dielectric constants are sufficiently close to those calculated from FTIR data. Therefore, one can conclude that the C-V technique could also be used to characterize OPS by determining its structural

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf

© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

composition. I-V characterization has also shown that OPS can be considered as a good dielectric insulator, exhibiting high resistivity and reasonable leakage current. At the same time, we have been interested in the electrical transport of pre-oxidized PS samples. It has been demonstrated that at relatively high forward bias, the conductivity follows a non linear regime and is limited by Poole-Frenkel conduction between charge states confined at the interface between Si crystallites and the thin grown oxide layer.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

General conclusion

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Porous silicon is a very interesting material which offers promising properties leading to a large variety of applications. In this work, we have pointed out the property of PS formation dependence with silicon doping concentration. Through the investigation of I-V characteristics during electrochemical anodization, it has been found that this dependence is attributed for p-type silicon to an increase in the potential drop across the Helmholtz layer which is present at the direct-biased Schottky silicon/electrolyte interface. While, it is probably due to the variation of the threshold breakdown voltage of the reverse-biased interface in the case of n-type Si.

This result was at the origin of developing a very simple and quite sensitive method for impurity profiling using electrochemical anodization. In fact, it has been shown that during anodization of a p-type doping staircase sample at constant current density, recorded potential variations can be converted to silicon doping variations according to the "Helmoltz + Schottky" model, and the electrolysis time scale to a depth scale knowing the PS formation rate. The depth resolution of the technique is found to be dependent on the doping level and approaches that of SIMS analysis for high doping concentrations with an estimated value of 60 nm/decade. However, the PS profiling method still presents two major limitations; it is restricted to p-type doping impurities and it cannot provide an accurate doping profile when the impurity concentration level to analyze is lower than that of the underlying layer.

In addition, we have exploited the above mentioned property of PS to locally form oxidized PS. Actually, it has been shown that when a silicon wafer of different doping concentration regions is anodized at a well chosen constant potential, the dissolution current only flows through regions of higher doping levels and hence PS (and subsequent OPS) is only formed there. We have also established well controlled anodization and oxidation procedures leading to an oxide of a more or less good quality. In conclusion, the PS approach seems to be interesting to be used for electrical isolation in CMOS circuits. It can be a good candidate to replace the shallow trench isolation (STI) process which begins to show limitations for the most advanced technologies (voiding and dishing). On the other hand, the fabrication of oxidized PS has been shown to be dependent on many factors during its three principal processing steps: ion implantation, electrochemical anodization and oxidation. Therefore, our main concern remains, at first, to optimize even better each step in order to obtain a resulting oxide of reliable dielectric properties comparable to the CVD oxide used in STI. Secondly, to confirm the feasibility of the PS technique for sub-65 nm CMOS

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

technologies, MOS transistors have to be successfully fabricated and then electrically characterized and compared to those fabricated with STI.

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Appendices

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Appendix A: Measuring of metal-semiconductor junction contact resistance using the transmission line method (TLM)

The first step in measuring the contact resistance of a metal-semiconductor junction is to deposit the metal on the semiconductor and pattern it so that identical pads which are spaced with variable distances are obtained (Figure . A rapid thermal annealing at 700 °C under nitrogen atmosphere is then performed.

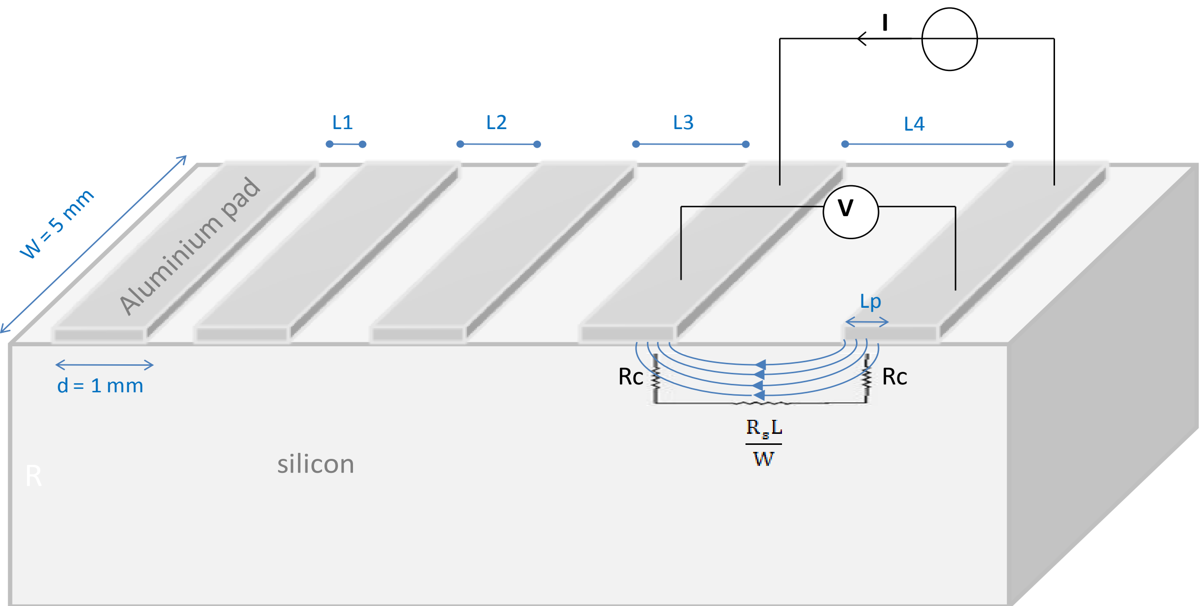


Figure A.1 The TLM structure used with the four point probe electrical connection

Current-voltage measurements are done using a four point probe station by applying a voltage between pairs of adjacent pads, and measuring the current flow. From that, one can calculate the total resistance R_T between two pads which is the series combination of three resistors: metal to semiconductor, through the semiconductor, and back into metal:

$$R_T = \frac{V}{I} = 2\,R_c + \frac{R_s L}{W} = 2\frac{R_s\,L_p}{W}\coth\left(\frac{d}{L_p}\right) + \frac{R_s L}{W} = 2\frac{\sqrt{R_s \rho_c}}{W}\coth\left(\frac{d}{L_p}\right) + \frac{R_s L}{W}$$

where R_s is the sheet resistance of the semiconductor layer with units of Ω/□, R_c the contact resistance, W the width of the pad, d the length, L is the variable distance between two adjacent pads, ρ_c the contact resistance per unit area with units of Ωcm^2 and L_p the

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

characteristic distance over which the current lines change under the metal contact. It is also referred to as the penetration length.

Assuming an infinitely long contact (i.e. d >> L_p), the total resistance will be given by:

$$R_T = 2\frac{\sqrt{R_s\rho_c}}{W} + \frac{R_sL}{W}$$

Therefore, a measurement of the resistance between a set of contacts with variable distance L can be fitted to a straight line as shown in Figure . The sheet resistance R_s can be obtained from the slope while the contact resistivity ρ_c can be determined from the intersection with the y-axis.

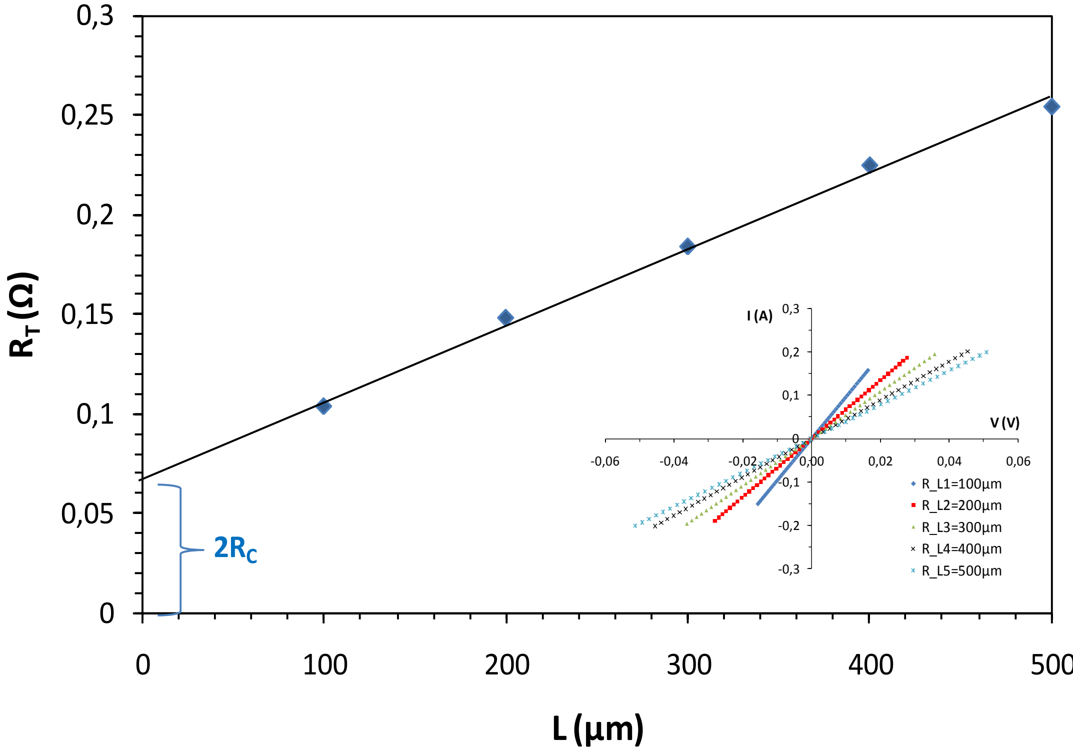


Figure A.2 Total resistance vs. contact spacing of a TLM structure. Inset shows the I-V curves measured between pairs of adjacent pads (silicon doping concentration is 2.10^{17}cm^{-3})

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés

Appendix B: Helmholtz layer

When a solid electrode put in contact with an electrolyte dissolves continuously, its surface may become charged. So, attracted ions are assumed to approach this surface and form a layer balancing the electrode charge (Figure B.a). The result is a potential drop and two layers of charge, that is analogous to an electrical capacitor which has two plates of charge. The distance of approach defining the thickness of the layer (few angstroms) is assumed to be limited to the radius of the ion and a single sphere of solvation round each ion.

In a somewhat more complex model, there are two planes forming the Helmholtz layer (Figure B.b). An inner layer (inner Helmholtz layer) in which the potential changes linearly with the distance. It comprises the absorbed water molecules (attracted toward the electrode due to its dipole nature) and sometimes the specifically adsorbed anions. An outer Helmholtz layer (OHP) which comprises hydrated (solvated) cations and where the potential varies linearly with the distance too. The cations which are hydrated and attracted toward the electrode surface are limited in their approach to the electrode surface because of the presence of water molecules. Finally, the diffuse layer, also called the Guoy-Chapman layer, contains excess cations or anions and the potential varies exponentially with the distance.

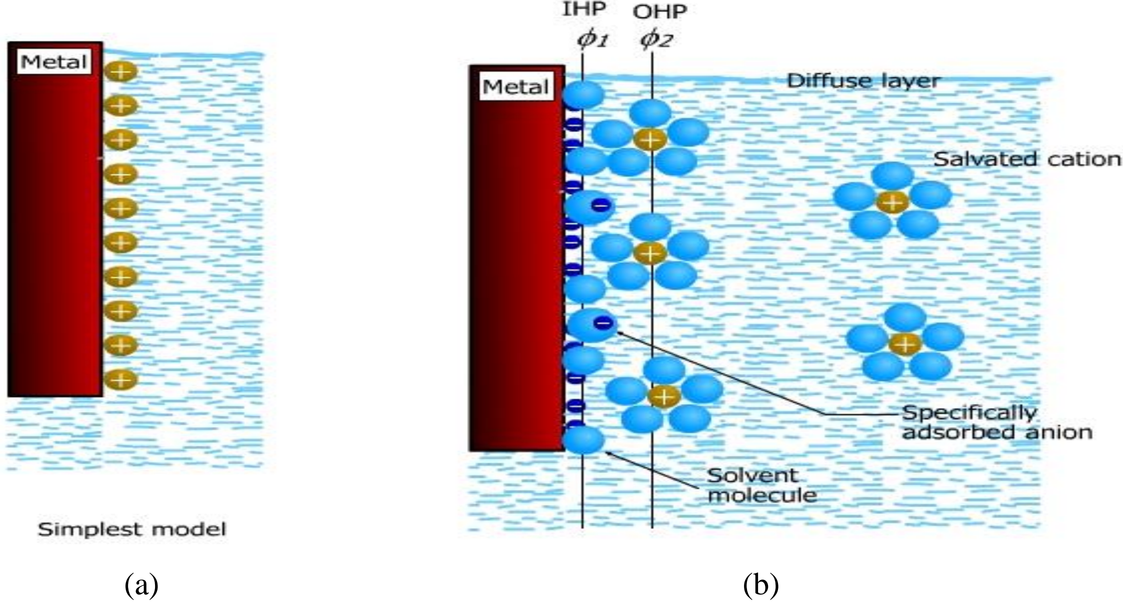


Figure B The Helmoltz layer (a) a simplest model, (b) a model showing inner and outer Helmoltz layers and the diffuse layer

Cette thèse est accessible à l'adresse : http://theses.insa-lyon.fr/publication/2011ISAL0072/these.pdf
© [A. Gharbi], [2011], INSA de Lyon, tous droits réservés