Modèle compact paramétrable du SCR pour applications ESD et RF

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To cite this version:

Sorin Romanescu. Modèle compact paramétrable du SCR pour applications ESD et RF. Autre. Université de Grenoble, 2011. Français. NNT : 2011GRENT055 . tel-00648390

HAL Id: tel-00648390
https://theses.hal.science/tel-00648390

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UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Optique et Radiofréquence**

Arrêté ministériel : 7 août 2006

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préparée au sein du **Laboratoire IMEP-LAHC**
dans **l'École Doctorale de l'Electronique, de l'Electrotechnique, de l'Automatique et du Traitement du Signal**

Modèle compact paramétrable du SCR pour applications ESD & RF

Thèse soutenue publiquement le **27 octobre 2011,**
devant le jury composé de :

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UNIVERSITÉ DE GRENOBLE

THESIS

Submitted for the degree of

Doctor of Philosophy of the UNIVERSITY OF GRENOBLE

Speciality : **Optics and Radiofrequency**

Presented by

Alexandru ROMANESCU

Thesis directed by **Philippe FERRARI**
and **Jean-Daniel ARNOULD**

Prepared at the **IMEP-LAHC**
In the **Doctoral School of Electronics, Electrotechnics, Automatisation and Signal Processing**

Scalable SCR Model for ESD and RF Applications

Defended on the **27th of October 2011,**
in front of the following committee :

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"There are more things in heaven and earth, Horatio, than are dreamt of in your philosophy."

Shakespeare

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Acknowledgments

Contrary to some believes, a PhD is far from being a solitary work. Let aside finishing this thesis, I might not have even started it, had it been on me. Thus, I would first like to thank Professor Paul Svasta from the Politehnica University of Bucharest, for showing me what research means and having me pursue this path, and Florence Podevin from Grenoble INP for enticing me in doing it in France.

I would like to thank all the ESD team at STMicroelectronics for making the "algeco" feel worm, especially Helene Beckrich-Ros for teaching me so much and Jean-Robert Manouvrier, who, through both his advices and personal example, made me try to raise the bar higher. I would also like to acknowledge Jean-François Larchanche for all the help in starting the RF-ESD work. From the Institute of Microelectronics, Electromagnetism and Photonics I would like to thank Professor Jean-Michel Fournier for his great RF design course and all his advices and Nicolas Corraro for the help and discussions about RF characterization.

I had the rare opportunity of having four advisers, whom honest collaboration and involvement drew the importance of the final scientific results. Jean-Daniel and Charles-Alex, this thesis would have been a lot more difficult without your continuous encouragement. Thank you for all your time spent in helping me solve my technical as well as my administrative problems. Pascal and Philippe, you offered me all the freedom, trust and guidance I needed. It has been both a pleasure and honour having you as my supervisors.

Thank you Andy, Andrei, Qianru, Xue, Niccolo, Tony, Maciej K., Alina R., Alexandra, Alina U., Dragos, Leonce, Yan, Bogdan, Ana, Ana-Maria, Teo, Geta, Tingting, Christoph, Tobias, Greg, Petr, Slava and Vladimir for being such wonderful friends across these years. Thank you Luis, Zuzanna, Anna, Maciej and Kalle for all the trips, parties and skiing we've done during your too short staying in Grenoble. And, finally, thank you Kavita, Alin, Natasa, Alain and Livia for supporting me during the most difficult period of my thesis: when it all seemed without an end.

In the end, I would like to thank my family that, although being so far, I always felt so close.

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Introduction

The electrostatic discharge (ESD) has always been one of the biggest reliability concerns in the integrated circuits (IC) manufacturing industry.

The scientific community handling this subject is grouped in the Electrostatic Discharge Association (ESDA), counting more than 2000 members across the globe. Since its creation in 1982, ESDA is chartered to expand ESD awareness through standards development, educational programs, local chapters, publications, tutorials, certification, and symposia.

With the continuous miniaturization process, the integrated circuits become more and more vulnerable to ESD. The usual failure mechanisms include metal lines or silicon over-heating and oxide breakdown. Protection against it is a must in every IC. With few exceptions, special devices that protect against the electrostatic discharge are deployed on-chip, alongside the functional elements. They are grouped in complex circuits, in order to assure the protection between each pin of the IC, regardless of its type (high frequency input/output, high voltage, power supply etc.). These auxiliary circuits need to be simulated in order to validate their functioning and achieve first silicon success from an ESD point of view. More, the protection network is electrically connected to the functional circuit, influencing its behaviour. Thus, they need to be taken into account when evaluating the overall performance of an IC through what is called a full-chip simulation. In consequence, a world-wide effort to build compact models of ESD protection devices to be used in SPICE-type simulations has been carried out. This effort is lead by the continuously evolving complexity of the protection designs and the increased sensitivity of the protected circuit to the parasitic introduced by the protection devices.

The parasitic is proportional with the size of the device, giving yet another reason to minimize the surface occupied by the protection. The SCR (silicon controlled rectifier, also called thyristor) is a very efficient device from this point of view. It eliminates the ESD energy in its whole volume, rather than at the surface, as other devices, most notably MOS-based. Thus, it needs a smaller surface for a given ESD protection level. Its drawback stands in the fact that it does not trigger instantly, leading to a very short period of over-voltage in the case of an ESD event, fact not tolerable by some circuits.

The first chapter of the thesis treats the general ESD problematic, ESD protection strategies, as well as an overview of the devices commonly used as protection.

In the context of increased demand from the industry of more accurate, scalable and easier to maintain ESD protection devices models, many studies regarding the SCR

have been carried out throughout the world. All of them are based on the bipolar transistor (BJT) device, the SCR – a pnpn device – being similar to a pair of npn and pnp interconnected BJTs. We can identify two main approaches. The first uses only BJTs – with an advanced electrical model (ST-BJT or vbic) – in order to model the behaviour of the SCR. The most important drawbacks are that (i) a number of unneeded phenomena are modelled, unnecessarily burdening and complicating the model and (ii) the plethora of available parameters allows us to fit the main characteristics at both low and high current, but we tend to model certain aspects with equations that do not have any physical support (the phenomenon modelled in the BJT differs from the one in the SCR). The later has a very high impact on the scalability of the model and over the parameter extraction procedure. The second approach pays a greater respect to the SCR particularities. It divides it into two functioning states: one before the triggering, modelled with 2 BJTs, and a second one, at high injection, usually modelled with a pin diode. This separation comes with two concerns: (i) the model is less consistent and might lead to divergence related problems due to its discontinuity and (ii) the switching point, being strongly related to the triggering, should be an output of the model, given by the other effects, and not an empirical input.

Model support and parameter extraction are important resource-consuming tasks. A good model should not only take into account the complexity-accuracy trade-off, but also the efficiency of the related parameter extraction strategy and maintainability.

The second chapter follows the development of a new model for the SCR. It aims to solve problems like divergence, versatility (as the ability to be used in various configurations or ESD protection designs) and scalability domain (limited by too empirical laws). This is obtained by the use of a more physical approach, and can be considered as a real improvement upon the existing state of the art. The core is still based on bipolar transistor equations, but these were modified in order to describe the phenomena happening in an SCR, especially at high injection levels.

Scalability is an important aspect of an ESD protection device model. Different level of protection can be required across different designs in a given technology. Thus, devices of different dimensions have to be employed. Moreover, important functional parameters, as the triggering voltage or the over-shoot, depend directly on the geometry of the structure.

A scalable model is presented in the third chapter. It is based on general scaling laws in semiconductors, adapted to the specific layout of an ESD protection SCR.

Protecting high frequency circuits against electrostatic discharge has always been a difficult task. The parasitic introduced by the protection devices at the I/O of an RF circuit can strongly degrade its performance. Until now, these parasitic were usually reduced to a capacitance. As the frequencies got higher and the demand for precision increases, these approximations become incomplete.

In order to model complex devices, as the SCR, a network of resistances and capacitances that is closer to the physics of the device has to be considered. The

backend (metal layers) plays an important role in the ESD performance. Thus, not all the routing should be left under layout-efficiency laws; bottom metal levels should be considered part of the device and, in consequence, part of the model. The ESD protection may often be found under a bias voltage. Being made out of pn junctions (like the SCR or the diodes are), some of their inner capacitances change; thus the need of distinguishing between metal (non voltage dependent) and junction (voltage dependent) capacitances.

High frequency models of the ESD protection diode and the SCR are proposed in the forth (and last) chapter. Their purpose is to help the RF designers make better input stages and evaluate the overall performance of their circuit, after the inclusion of the indispensable ESD protection. Finally, the models were tested on a complete protection structure - DTSCR (diode triggered SCR) - made of an SCR, three diodes that make the triggering circuit for the SCR and a diode for reverse protection.

Introduction (français)

Les décharges électrostatiques (ESD pour « Electrostatic Discharge ») ont toujours constitué un aspect important de la fiabilité des circuits intégrés pour les fabricants et utilisateurs de circuits électroniques.

La communauté scientifique s'intéressant à ce sujet s'est regroupée au sein de l'« Electrostatic Discharge Association », qui compte plus de 2000 membres à travers le monde. Depuis sa création en 1982, ESDA est mandatée pour étendre les connaissances concernant l'ESD à travers le développement de standards, programmes éducatifs, associations locales, formations, certifications, et conférences.

Avec la miniaturisation incessante des circuits, les circuits intégrés deviennent de plus en plus vulnérables à l'ESD. Les mécanismes de panne les plus fréquents sont liés à l'échauffement excessif des conducteurs ou du silicium, et au claquage au niveau des oxydes. La protection vis-à-vis de ces causes de pannes est quasi-indispensable pour tout circuit intégré. A part quelques rares exceptions, les circuits spéciaux de protection contre les événements ESD sont réalisés au sein de la puce (« on-chip ») dans chaque circuit intégré concerné, en même temps que les éléments fonctionnels. Ils sont regroupés en circuits complexes, afin d'assurer la protection sur chaque « pin » du circuit intégré, indépendamment de son type (entrée/sortie haute fréquence, forte tension, alimentation, …). Ces circuits auxiliaires doivent être simulés afin de valider leur fonctionnement et atteindre un fonctionnement sans erreur dès la première réalisation sur puce. En outre, les circuits de protection sont connectés électriquement aux circuits fonctionnels, influençant leur fonctionnement. Ainsi, ils doivent être pris en compte lors de l'évaluation des performances globales d'un circuit intégré à travers une simulation complète des circuits implémentés (« full-chip simulation »). En conséquence, un effort de l'ensemble des équipes concernées à travers le monde a été concentré pour l'implémentation de modèles ESD au sein de simulateurs de type SPICE. Ces efforts sont continuellement nécessaires du fait de l'évolution croissante d'une part de la complexité des circuits de protection contre les décharges électrostatiques et d'autre part de la sensibilité des circuits protégés vis-à-vis des parasites introduits par les circuits de protection.

Les effets parasites engendrés par les circuits de protection sont proportionnels à leur taille physique, fournissant ainsi une raison supplémentaire dans le sens de la diminution de la surface des circuits de protection, venant s'ajouter à la problématique du coût du silicium. Le SCR (pour « Silicon Controlled Rectifier ») ou thyristor constitue un circuit très efficace de ce point de vue. Il permet d'absorber l'énergie ESD dans l'ensemble de son volume, et non seulement à sa surface comme

c'est le cas pour d'autres circuits utilisés pour la protection, notamment les circuits basés sur des transistors de type MOS. Ainsi, son implémentation nécessite une moindre surface pour un niveau de protection donné. Son principal défaut est lié à son temps de déclenchement non instantané par rapport à la vitesse de propagation d'un événement ESD, conduisant à une brève surtension transitoire lors d'un événement, non tolérable pour certains types de circuits.

Le chapitre 1 de cette thèse traite de la problématique des circuits de protection ESD en général, des stratégies de protection, et donne une vision globale des circuits les plus largement utilisés pour la protection ESD.

Dans le contexte d'une demande accrue de la part de l'industrie de modèles à la fois plus précis, pouvant être adaptés à différentes dimensions géométriques (« scalable models »), et plus simples à faire évoluer face à l'évolution des technologies, plusieurs études sur le SCR ont été menées à travers le monde, et continuent à être menées. Toutes les études sont basées sur l'utilisation de transistors bipolaires (BJT) pour décrire le SCR, le SCR étant un circuit de type pnpn, pouvant être considéré comme similaire à une paire de deux transistors bipolaires pnp et npn interconnectés. Deux principales approches de modélisation peuvent être identifiées. La première utilise uniquement des transistors bipolaires, avec un modèle électrique évolué, de type ST-BJT ou vbic, afin de modéliser le comportement du SCR. Les principaux écueils de cette approche sont (i) la prise en compte par les modèles d'un grand nombre de phénomènes inutiles dans le cas du SCR, compliquant inutilement le modèle, et (ii) l'utilisation d'un grand nombre de paramètres non physiques nécessaires pour obtenir un modèle fiable et prédictif. Ce dernier aspect a un impact négatif direct sur la « scalabilité » du modèle et sur la procédure d'extraction des paramètres constitutifs du modèle. Ainsi la seconde approche s'avère plus proche des particularités de fonctionnement du composant SCR. Le fonctionnement du SCR est divisé en deux états : l'un correspond au SCR avant déclenchement, il est modélisé par deux BJT, le second correspond au fonctionnement à forte injection de courant, après déclenchement, il est modélisé par une diode pin. Cette approche permet d'obtenir des modèles mieux basés sur la physique du SCR. Cependant elle souffre également d'inconvénients majeurs : (i) le modèle est moins robuste et peut conduire à des problèmes de divergence du fait de la discontinuité avant et après déclenchement, et (ii) le point de changement de modèle, intimement lié au point de déclenchement, est une donnée empirique d'entrée, alors qu'il devrait être une sortie du modèle, sans que l'utilisateur n'ait à intervenir de manière très empirique.

L'extraction de paramètres est un aspect important et une tâche consommatrice de ressources. Un bon modèle ne doit pas seulement tenir compte du compromis entre précision et complexité, mais également de l'efficacité de la stratégie d'extraction des paramètres.

Le deuxième chapitre concerne le développement d'un nouveau modèle pour le SCR. Ce modèle vise à résoudre des problèmes tels que la divergence, la polyvalence (comme la capacité devant être utilisé dans différentes configurations de protection

ESD) et le domaine de paramétrisation géométrique (limitée par des lois trop empiriques). Ceci est obtenu par l'utilisation d'une approche plus physique, et peut être considéré comme une réelle amélioration de l'état de l'art. Le noyau est toujours basé sur des équations de transistor bipolaire, mais celles-ci ont été modifiées afin de décrire les phénomènes propres au SCR, en particulier aux niveaux de forte injection.

La paramétrisation géométrique est un aspect important d'un modèle de dispositif de protection l'ESD. Différents niveaux de protection peuvent être nécessaires pour différents circuits dans une technologie donnée. Ainsi, des dispositifs de dimensions différentes doivent être employés. Par ailleurs, d'importants paramètres fonctionnels, comme la tension de déclenchement ou la surtension, dépendent directement de la géométrie de la structure.

Un modèle paramétrique d'un point de vue géométrique est présenté dans le troisième chapitre. Il est basé sur des lois d'échelle classiques dans les semi-conducteurs, adaptées à la configuration spécifique d'un SCR de protection.

Protéger les circuits à haute fréquence contre les décharges électrostatiques a toujours été une tâche difficile. Le parasite introduit par les dispositifs de protection à l'entrée ou à la sortie d'un circuit RF peut fortement dégrader ses performances. Jusqu'à présent, ces parasites ont été généralement réduits à une simple capacité. Comme les fréquences augmentent en même temps que la demande de précision, ces approximations deviennent trop limitées.

Afin de modéliser des dispositifs complexes comme le SCR, un réseau de résistances et de capacités plus proche de la physique de fonctionnement du SCR doit être envisagé. Le « back-end-of-line » (couches métalliques) joue un rôle important dans la performance des circuits de protection ESD. Ainsi, les premiers niveaux de métaux doivent être considérés comme faisant partie du dispositif et, en conséquence, du modèle. La protection ESD peut souvent être soumise à une tension de polarisation superposée de manière normale au signal RF. Le circuit de protection ESD comportant des jonctions pn (comme le SCR ou les diodes), certaines capacités internes changent, d'où la nécessité de distinguer entre les capacités de métallisation (non dépendantes de la polarisation) et les capacités de jonction (dépendantes de la polarisation). Des modèles petit signal haute fréquence de la diode et du SCR de protection contre l'ESD sont proposés dans le quatrième et dernier chapitre. Leur but est d'aider les concepteurs RF à concevoir des étages d'entrée mieux adaptés et bien sûr d'être capable de prendre en compte dès la conception l'impact des circuits de protection sur le signal RF. Afin de valider les modèles proposés, ceux-ci ont été testés sur une structure de protection complète - DTSCR (SCR déclenché par diode) - constitué d'un SCR, de trois diodes formant le circuit de déclenchement pour le SCR, et d'une diode de protection montée en inverse afin d'obtenir une protection bidirectionnelle.

1 Context and state of the art

1.1 General ESD protection aspects

1.1.1 The ESD problem

Charges accumulated in semiconductor devices are able to create potential differences up to thousands of volts. There are two steps in protecting a device against the electrostatic discharge that may appear: (1) preventing the charge to accumulate in the first place and (2) providing a way to evacuate the discharge energy.

Preventing the charge accumulation

The first step is effective during the manufacturing process (from the chip manufacturing to the final electronic product assembly), where the chip is the most exposed to the external environment and most of the ESD events may appear.

The unwanted charge accumulates through triboelectriciy (friction with another material) or through induction (by an electromagnetic field). This accumulation can be limited by controlling the IC's environment. All the facilities and equipment have to be adapted. A list of common measures includes:

- grounding facilities for humans (conducting shoes and wrist straps)
- antistatic clothing
- conducting and dissipative floors
- air ionizers
- antistatic coating of materials

On chip protection - evacuating the ESD energy

The second step is to increase the ESD robustness of the integrated circuit. A controlled environment cannot totally stop the accumulation of charge and, after the final product is delivered, this control is lost. Also, the rapid downscaling in nowadays technologies comes with a decrease in the circuit's resistance to ESD (ex. the gate oxides are thinner and easier to break by even a less intense over-voltage).

Thus, despite the increase in cost, given by the extra surface occupied by the protection devices, on-chip ESD protection is of extreme importance.

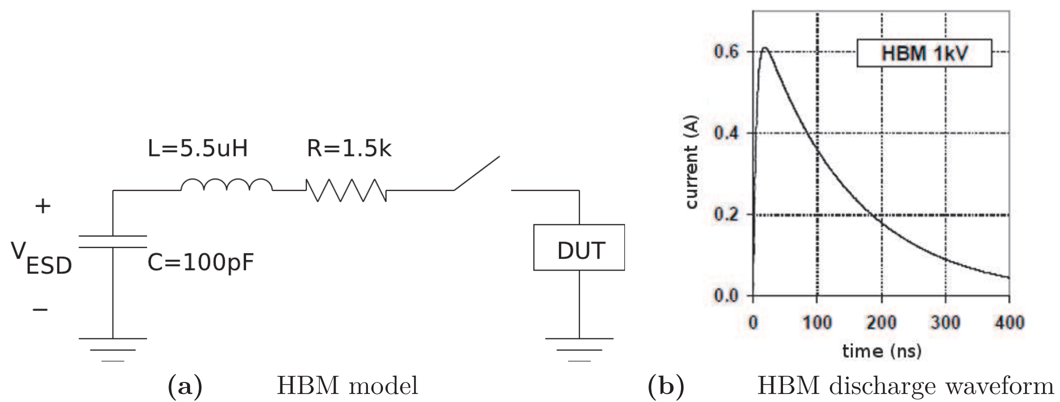
The strategy is selected having as target a certain level of protection under certain ESD conditions. These conditions are described by ESD models.

1.1.2 ESD models

There are three mainstream models of the electrostatic discharge process. They are all described by standards, one of their purposes being to offer an objective measure of how robust a certain circuit is under a specific ESD event. The models are used for reproducing a close-to-real electrostatic discharge in order to test and qualify the integrated circuits.

Human Body Model

The Human Body Model (HBM) represents the discharge between a person and an integrated circuit [ESD-STM 5.1]. The human body is modelled by a $100\,pF$ capacitance connected through a $1.5\,k\Omega$ (Figure 1.2a). An additional parasitic inductance between $5.5\,\mu H$ and $11.8\,\mu H$ may be added in order to better reproduce the testing environment.



(a) HBM model **(b)** HBM discharge waveform

Figure 1.1: HBM model and discharge waveform

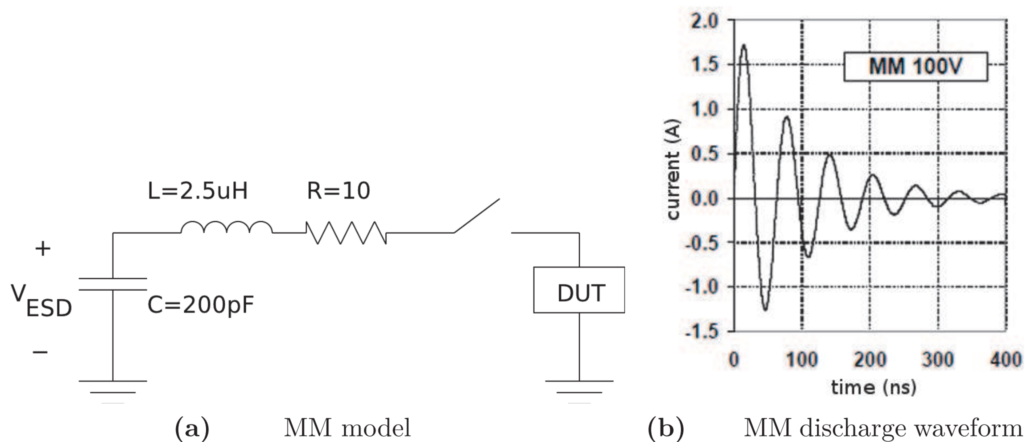
The current expression is approximated in 1.1 [Rooz'90] and the typical waveform is shown in Figure 1.1b.

$$I_{HBM}(t) = \frac{V_{ESD}}{R} \cdot \left(1 - exp\left(-\frac{R}{L} \cdot t\right)\right) \cdot exp\left(-\frac{t}{R \cdot C}\right) \tag{1.1}$$

Machine Model

The Machine Model (MM) represents the discharge between manufacturing equipment and the integrated circuit [ESD-STM 5.2]. It was introduced in Japan in the '70s but it is less used nowadays as a test reference.

It is similar to the HBM model, only that the machine is modelled by a $200\,pF$ capacitance connected through a insignificant (0 to $20\,\Omega$) resistance to the integrated circuit (Figure 1.2a). An additional parasitic inductance between $1.5\,\mu H$ and $2.5\,\mu H$ may be added in order to better reproduce the testing environment.



(a) MM model **(b)** MM discharge waveform

Figure 1.2: MM model and discharge waveform

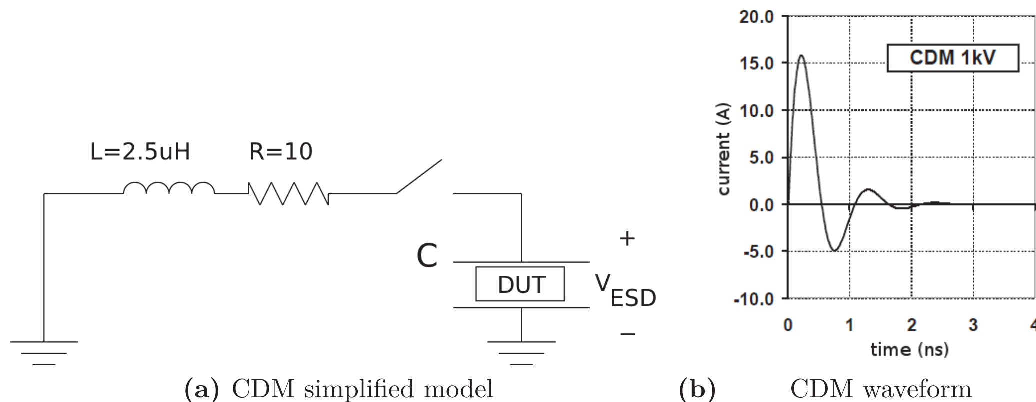
The current expression is approximated in 1.2 [Rooz'90] and the typical waveform is shown in Figure 1.2b.

$$I_{HBM}(t) = V_{ESD} \cdot \sqrt{\frac{C}{L}} \cdot exp\left(-\frac{R}{2L} \cdot t\right) \cdot sin\left(\frac{1}{\sqrt{LC}}\right) \tag{1.2}$$

Charged Device Model

The Charged Device Model (CDM) represents the discharge of a previously self-charged integrated circuit (Figure 1.3a) [ESD-STM 5.3.1]. Originally, this type of events appeared when a chip, charged while sliding out of its package, entered in contact with a ground plane. Nowadays, effects like induction charging are also taking into account in the description of the model.

During a CDM discharge, high currents (up to $10\,A$) with a duration of only a few nanoseconds can occur, making the protection against this type of discharge a difficult task.



(a) CDM simplified model **(b)** CDM waveform

Figure 1.3: CDM simplified model and discharge waveform

The current expression is approximated in 1.3 [Rooz'90] and the typical waveform is shown in Figure 1.3b.

$$I_{CDM}(t) = \frac{V_{ESD}}{\omega L} \cdot exp\left(-\frac{R}{2L} \cdot t\right) \cdot sin\left(\omega t\right) \tag{1.3}$$

$$\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \tag{1.4}$$

The discharged capacitance, being the capacitance of the tested device, is highly dependent on the package [Aver'87]. In order to simulate the CDM discharge process, package models were developed [Rich'02, Goea'05].

CDM events mostly appear during the automatic manufacturing and handling processes. The most common failure they cause is at oxide level, when the CDM voltage surpasses the oxide breakdown voltage. They are one of the biggest threats in the continuous downscaled, with thinner oxide, technologies [Dabr'98].

1.1.3 ESD protection design

In order to assure the robustness (resistance to electrostatic discharge) of an integrated circuit, one has to make sure that an ESD event between each two input/output pins don't damage the core circuit.

This is obtained using ESD protection devices arranged in such a way that, under an ESD event, they form a current path between the affected pins, taking on themselves all the destructive energy. These devices have the role of a switch passing into a low impedance mode (lower than any other path that can be formed in the protected circuit) when an ESD event is detected, yet having a high impedance (be transparent to the protected circuit) in normal conditions (outside an ESD event).

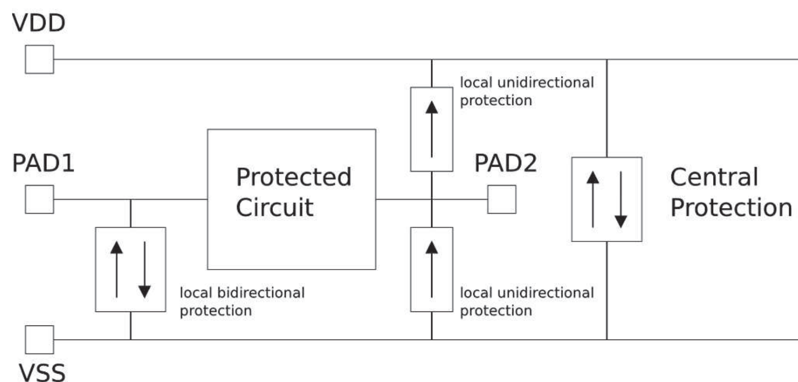


Figure 1.4: General ESD protection strategy using local unidirectional and bidirectional devices and a central protection

Protections can be unidirectional or bidirectional. Different current path examples are shown in Fig. 1.5.

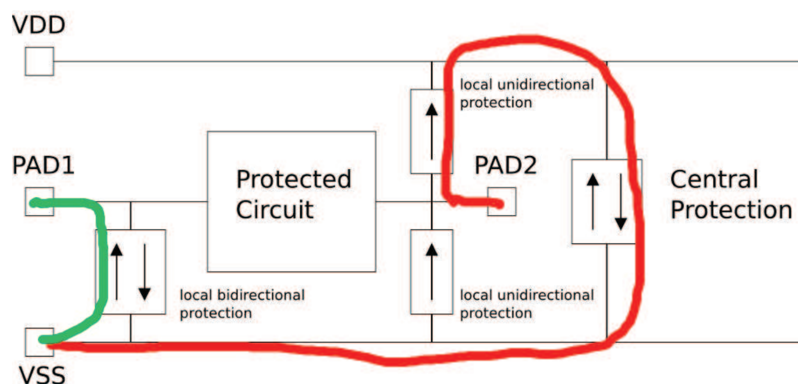


Figure 1.5: Current path for a positive ESD event at PAD1 (green) and PAD2 (red)

A positive or negative ESD event on PAD1 will discharge (Fig. 1.5: green) directly through the bidirectional element. A positive ESD event on PAD2 will have to pass through the power rail and the central protection (Fig. 1.5: red).

There are too main distinct positions (and functions) a protection device can occupy in the protection scheme:

- between an I/O pad and a power rail (ex. PAD1 and VDD) - also called "local protection"; the common devices used in this case are: diodes, SCRs, ggNMOS.
- between the power rails (ex. VDD and VSS) - also called "power clamps" or "central protection"; the common devices used here are the classic MOSFET transistor, the gcNMOS and the SCR.

Their requirements differ accordingly and can be resumed in what is called a "design window" (Fig. 1.6).

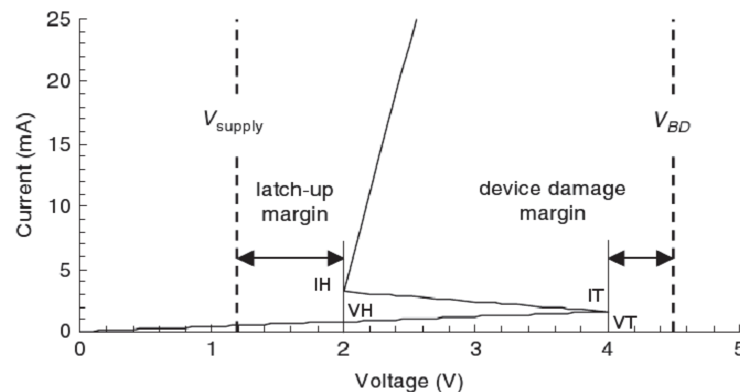


Figure 1.6: ESD device design window

The important voltage and current points are:

- V_{supply}: the voltage of the power source (VDD in Fig. 1.4)
- V_{BD}: the breakdown voltage - maximum voltage supported by the protected circuit
- V_T and I_T: the trigger voltage and current
- V_H: the holding voltage - below which the ESD protection device is always off

Choosing a device inside the design window ensures that:

- it will be transparent (off = high impedance) for the circuit outside an ESD event ($VT > V_{supply}$)
- it will turn on before the failure voltage level ($V_T < V_{BD}$)
- it will turn off after the ESD event ($V_H > V_{supply}$)

Diodes and the SCR are unidirectional devices while the ggNMOS is bidirectional. In Fig. 1.7 we reproduce Fig. 1.4, exemplifying the use of different types of devices. Diodes are used as unidirectional devices. A positive ESD event on Pad2 will, thus,

need to discharge through the VDD rail and the central protection. On the other hand, a positive ESD stress on Pad1 will discharge directly to VSS, the ggNMOS being a bidirectional protection. This is an important aspect, as using the power rail in the discharge path needs a careful design. For long distances, the resistance of the rail becomes important, being able to favour the triggering of different, undesired, current paths through the protected circuit.

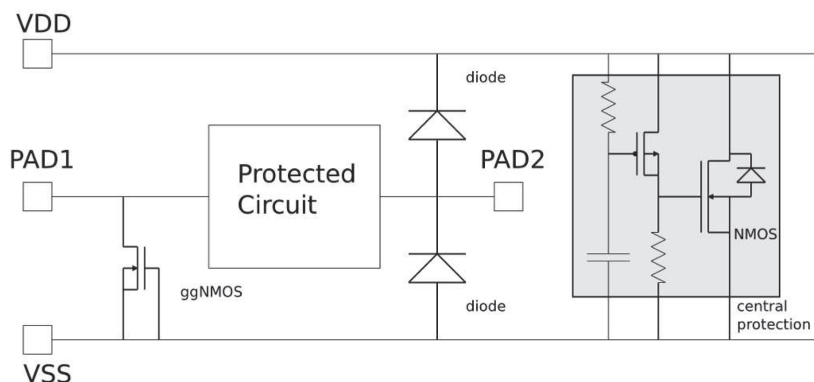


Figure 1.7: General ESD protection strategy using a ggNMOS, diodes and a NMOS based power clamp

Some devices need an auxiliary circuit in order to turn on. In this example, the power clamp is composed by an n-type MOSFET device (NMOS), an ESD event detection circuit and a sub-circuit, used to bias and trigger the NMOS. The detection circuit is a RF filter built in such a way that only lets the high rise-time ESD-specific signal to pass, turning on the PMOS. This positively biases the gate of the NMOS, activating the protection.

1.1.4 ESD vs. RF constraints

Protecting high frequency circuits against electrostatic discharge (Fig. 1.8) has always been a difficult task [Wang'02]. The parasitic introduced by the protection devices at the I/O of an RF circuit can strongly degrade its performance. Until now, these parasitic were usually reduced to a capacitance [Vass'02]. As the frequencies get higher and the demand for precision increases, these approximations become incomplete.

In order to design ESD protections for high frequency circuits, small capacitance devices must be used. This implies smaller and, thus less robust protections. In order

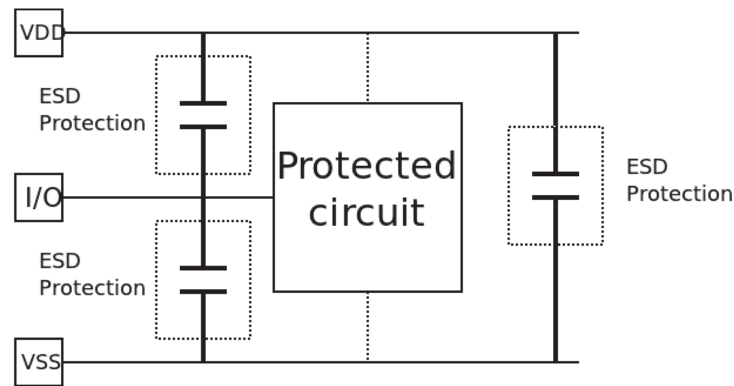


Figure 1.8: Parasitic capacitance introduced by the protection devices

to achieve a high ESD protection level, bigger devices are divided into equal-sized smaller ones and coupled through CPW (co-planar waveguides) that are meant to adapt the sub-parts (Fig. 1.9). This technique is called distributed protection [Ito'02, Klev'00]. Because of the CPW resistance, the sub-device situated the closest to the I/O pin takes the most of the ESD. A decreasing-size technique was presented in [Ming'05]; the sub-device near the I/O pin being the biggest, and the one next to the protected circuit, the smallest.

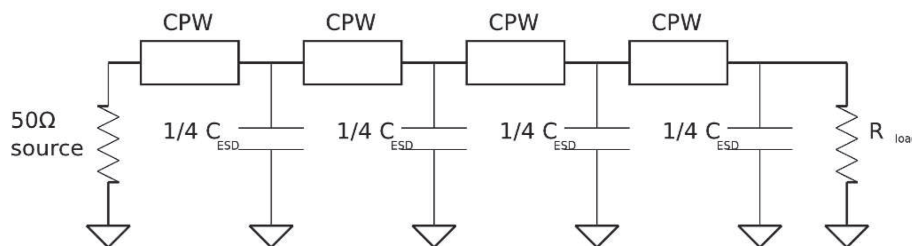


Figure 1.9: Distributed ESD protection

For a robust and well functioning circuit, RF-ESD co-design has to be done. This means, for example, tailoring the CPW transmission lines in order to match the ESD protection sub-devices they feed or, more generally, by matching the input stage of an amplifier and evaluating the overall performance of the circuit after the inclusion of the indispensable ESD protection. In order to be able to do that, advanced RF models of the ESD protection devices should be available. Very few studies have been carried out in this direction, mostly concerning the diodes [Ming'10, Wang'05]. An SCR-type device was analyzed by Lin and Ker in [Chun'10]. However, a more comprehensive approach and a more general methodology is, nevertheless, needed and will be treated in Chapter 4.

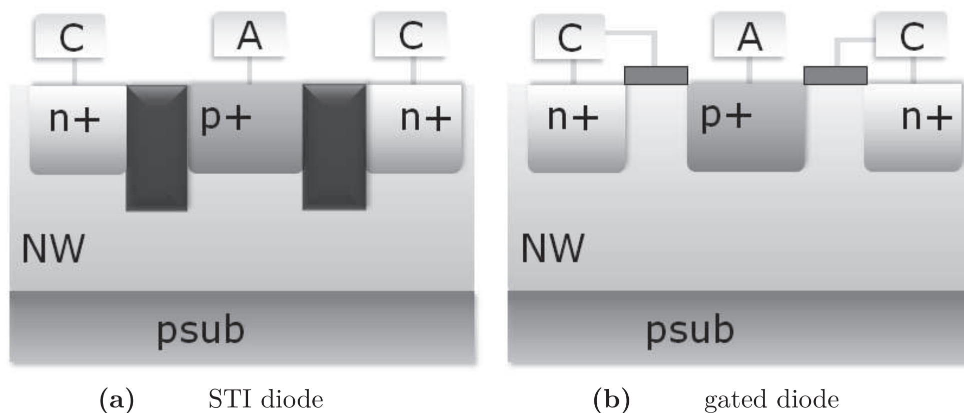
1.2 ESD protection devices

1.2.1 Diodes

Diodes are the most common ESD protection devices. They usually assure unidirectional protection between an I/O and the power supply rails (Vdd or Vss). They are placed in the circuit in such a way that under normal conditions (no ESD event) they are reverse biased, protecting in the opposite direction (Fig. 1.7).

There are two basic types of ESD protection diodes:

- *STI diodes* (Figure 1.10a), having a shallow trench isolation oxide between the electrodes
- *Gated diodes* (Figure 1.10b), having a polysilicon gate between the electrodes; the shorter distance between p+ and n+ makes them turn on faster [Mano'08]



(a) STI diode **(b)** gated diode

Figure 1.10: ESD protection diodes: STI and gated

The turn-on voltage of a diode is around $0.7\,V$. Bigger turn-on voltages can be achieved only through stacking multiple diodes. For example, in order to obtain a V_T of $2.1\,V$, it will be necessary to stack three diodes (Fig. 1.11).

In reality, because of parasitic bipolar effects, the resulting triggering voltage is smaller than expected [Dabr'98] (Fig. 1.12).

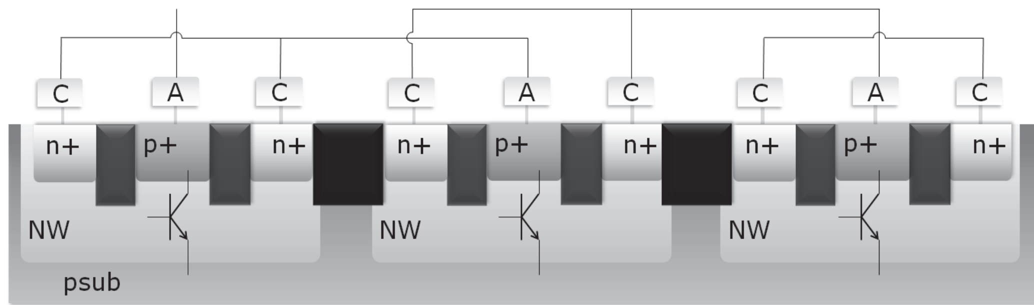


Figure 1.11: Stacked diodes

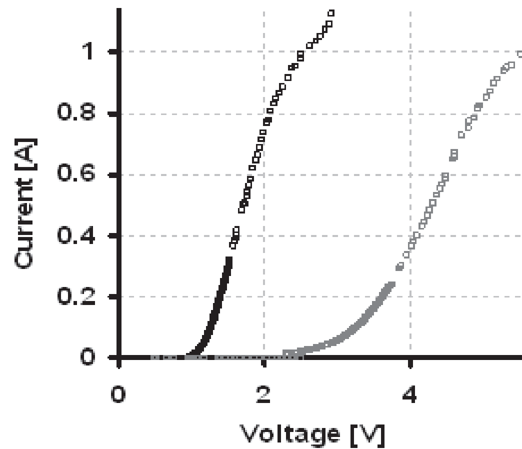


Figure 1.12: Triggering voltage for a diode and three stacked diodes

1.2.2 MOS-type devices

The MOSFET is a classic MOS device, operated in a non-breakdown mode. Its functioning is simple: once a voltage is applied on its gate, it turns on, evacuating the ESD energy. In order to operate it in non-breakdown, the MOS has to be large, with low "on" resistance and be fast (turn on before the drain voltage reaches the snapback voltage). Although it takes a large surface on silicon, it is one of the most used solutions in power clamps, being easy to predict and with fewer changes from a technology node to another. On the other side, breakdown-based MOS devices (like the ggNMOS) are harder to simulate and model, the triggering point being highly technology-dependent [Dabr'98].

The ggNMOS (gate grounded NMOS) is a bidirectional snapback device. The well, gate and source are all connected to the ground, thus, in normal conditions, the transistor is always off.

Although being realized as a MOS device, the main conduction and turn-on mechanism between the drain and the source is through its parasitic npn bipolar

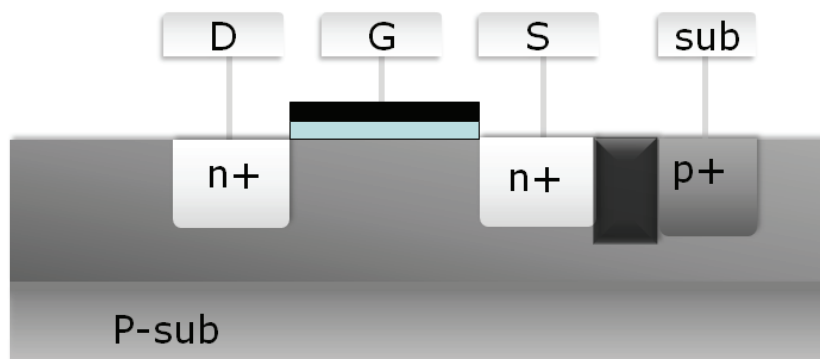


Figure 1.13: n-type MOSFET layout

transistor (Fig. 1.14). When the substrate voltage (which acts as a base) is high enough, it forward-biases the substrate-source (base-emitter) junction. This activates the parasitic npn, lowering the voltage drop across the NMOS. In the opposite sense (from the source to the drain), the device protects through its substrate-drain pn junction.

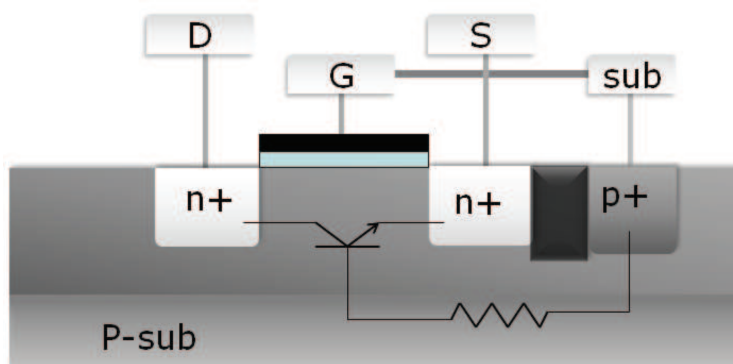


Figure 1.14: ggNMOS layout

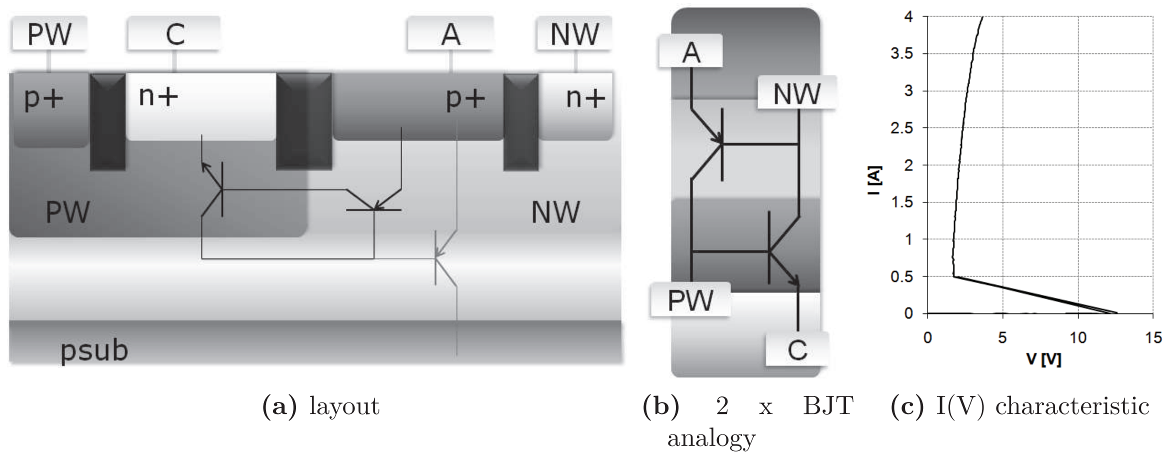
The main advantages of the ggNMOS are its bidirectional capability, snapback behaviour and its fast response (almost instantaneous turn-on time); compared to the classic MOSFET it is harder to simulate and predict, due to the breakdown nature of triggering.

The biggest disadvantage of MOS devices is their high surface (and the related capacitance) required to reach an acceptable level of robustness.

1.2.3 Silicon Controlled Rectifier (SCR)

The Silicon Controlled Rectifier, or thyristor, is one of the most effective protection devices - low surface required to attain a certain level of robustness. It is a pnpn

device (Fig. 1.15a), usually represented through two bipolar junction transistors (Fig. 1.15b).



(a) layout (b) 2 x BJT analogy (c) I(V) characteristic

Figure 1.15: The SCR: layout, analogy with two bipolar transistors and I(V) characteristic

There are two ways of triggering an SCR.

The first one is by breaking up the central pn junction. In nowadays technologies, this is achieved at around 13 V, a far too high level for ESD protection needs. A way of lowering this voltage is by creating an ggNMOS between the cathode and the n-well through a n+ diffusion (Fig. 1.16) This sub-device will trigger faster (as described in sec. 1.2.2) and inject enough current in the pnp base so that it turn on the whole structure.

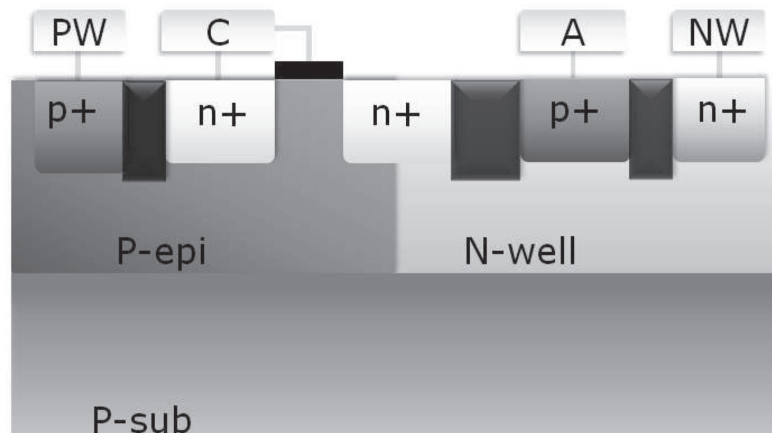


Figure 1.16: Low voltage triggered SCR (LVTSCR)

The second one is through what is called a “latch-up”. As being composed of two interconnected transistors, turning on one of them (by positively biasing the base-emitter junction) will cause its collector current to be injected in the other transistor’s base. Thus, both transistors will be in a conductive state, creating a low-impedance path between the anode and the cathode. This phenomenon is presented with more details in 1.3. Depending on the triggering circuit, there are two common ways of creating a latch-up SCR based protection: the DTSCR - Diode Triggered SCR [Merg’03] and the STMSCR - Smart Triggered Multifinger SCR [Cail’05], both analyzed in sec. 1.3.2.

The biggest advantage of the SCR is the small silicon surface needed to evacuate a large ESD energy, compared especially with the ggNMOS. This is achieved through the fact that the energy is evacuated in the body volume of the device, not only in the surface.

Its drawback is the necessary time to turn on (to latch up), leading to a short (but not negligible) period of over-voltage.

1.3 The SCR

1.3.1 Turn-on mechanism

The SCRs carried out along this thesis have been designed to turn on through latch-up. The following section describes the physical phenomena happening if the structure is latched up by turning on the npn side first (Fig. 1.17).

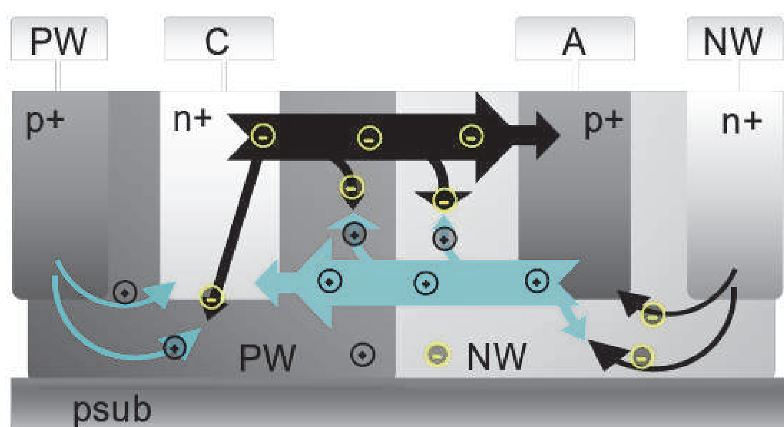


Figure 1.17: The triggering mechanism in an SCR

A voltage drop between the anode (A) and the p-well (PW) will cause electrons from the n+ dropped A region (the npn's emitter) to diffuse in the PW region (the npn's base). Some of these electrons will be carried to the n-well (NW) by the electric field between the PW (npn's base) and NW (npn's collector) through what is called a bipolar transistor effect (and we say that the npn transistor is turned on). This will increase the NW's electric potential which will help the electrons pass to the cathode (C) and, in the same time, pull holes from C (the pnp's emitter) to the NW (the pnp's base). Some of these holes will be carried to the PW (pnp's collector) by the same electric field of the central pn junction, also through a bipolar transistor effect. At their place, these will cause the npn to open even more, starting a cycle that will end by completely "locking" the device in an on state (with a low impedance path between the A and the C).

The PW and NW share both the role of a base and of a collector. In these regions, at high injection levels, the majority carriers of one transistor will meet the majority carriers of the other one, leading to high recombination rates [Cail'05].

1.3.2 Auxiliary circuit

In order to produce a latch-up in the protection device when an ESD event occurs, a turn-on circuit has to be connected to the SCR. Its purpose is to detect an ESD event and use its voltage drop to turn on one of the transistors.

DTSCR

The easiest way is to connect a stack of diodes to the n-well (NW) - that is, to the base of the pnp transistor (Fig. 1.18) [Merg'03]. Together with its emitter-base junction, we have a total of four junctions in series that will trigger between $2.4\,V$ and $2.8\,V$, depending on the technology. The current flowing at that point through the NW (the base of the pnp) will cause the pnp transistor to turn on and inject current into the base of the npn, latching up the whole SCR.

STMSCR

The diode chain can be replaced by a resistor. Its value is chosen so that the desired triggering voltage be the sum of the voltage drop on it and the triggering voltage of the pnp's base-collector junction. The problem here is that even at lower voltages, there will still be a significant current flowing through the resistance. In order to overcome this and take the protection closer to the ideal (transparent for the protected circuit - an almost infinite impedance between A and C outside an ESD event), a detection / triggering circuit has to be added (Fig. 1.19). Its role will be to have the resistance connected to the PAD in normal conditions and to switch it to the ground when an ESD event is detected. This can be done using an RC filter

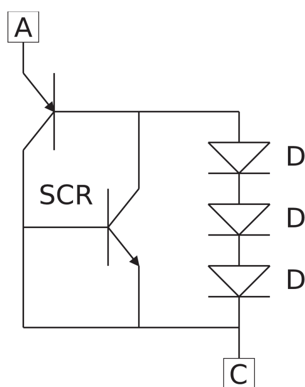


Figure 1.18: The Diode Triggered SCR (DTSCR)

for detection and a MOS inverter for the switch, similar to the circuit described in Fig. 1.7 for the central protection [Cail'05].

Outside an ESD event, the gates of the inverter's transistor are connected to the ground, making the PMOS open and the NMOS closed - thus, RNwell is connected to the PAD (and the SCR is only able to turn on through central junction breakdown). Once an ESD event is detected (its rise time will "pass" the capacitor and polarize the gates), the PMOS will turn off and the NMOS will turn on, connecting RNwell to the ground.

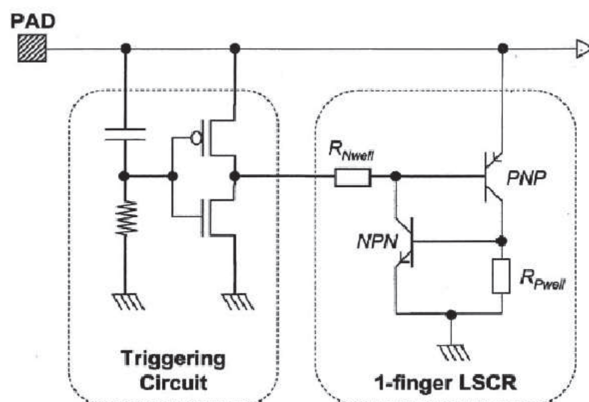


Figure 1.19: The Smart Triggered Multifinger SCR (STMSCR)

1.3.3 Overshoot

The SCR does not turn on instantly. The over-voltage that occurs during the first instants of a pulse is called overshoot (Fig. 1.20) and can be fatal for some circuits. Usually this problem is solved by using a small ggNMOS in parallel, which will turn on fast and lead the first part of the ESD current, while the SCR fully turns on.

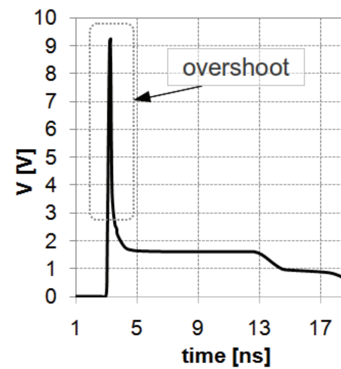


Figure 1.20: A typical SCR overshoot

1.4 State of the art in SCR compact modelling

There are three approaches of building SCR models to be used in SPICE simulators.

1.4.1 Based on advanced BJT models

The elementary approach is to use bipolar transistor models, given that the SCR can be theoretically approximated with 2 BJTs. Unfortunately, at high injection levels, the coupling of the two bipolars that make the SCR (the collector of one is the base of the other and vice-versa) becomes important. The bipolar models, even from the basic (Gummel - Poon) predict a big current gain (“beta”) degradation caused by the majority charge present in the base (electrons in the case of the npn). In the case of an SCR, as the base of one is the collector of the other, at high injection it will be flooded with the opposite type of carriers from the other transistor, leading to a larger recombination rate. The lack of modelling this phenomenon is overcome by using advanced BJT models. These models take into account a large number of effects and have a large number of parameters that can be “tuned” in order to fit the main I(V) characteristic.

Zhou proposed a macro-model composed of industry-standard compact models as VBIC and Gummel-Poon [Zhou’07]. Furthermore, Liou extended this model by taking into account substrate effects and making it usable for different types of SCR [Lou’08]. The special high injection impact on the I(V) characteristic was solved using the base push-out and collector conductivity modulation effects present already in the VBIC model.

Nevertheless, the effects modelled for the advanced BJT are not the same as those actually happening in an SCR, thus making it hard to extrapolate the model to different topologies and configurations. The geometrical scalability is also problematic: no scalable models were reported using this technique.

1.4.2 Using 4 BJT sub-devices

Another way of modelling an SCR was proposed in [Font'08]. The model is made of 2 pairs of bipolar transistors. One has the parameters adjusted for low and the other for high injection levels. If connected as in Fig. 1.21, once the low current transistors start conducting, the second pair turns on and becomes the main current driver.

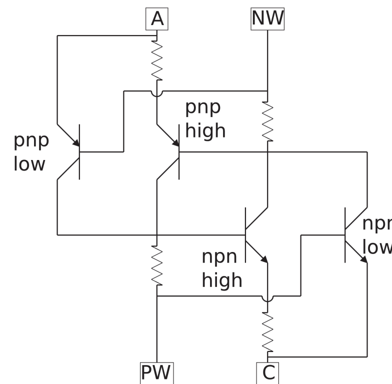


Figure 1.21: SCR model using 4 bipolar transistors

The "switch" between the two pairs is made in a continuous, consistent way. Nevertheless, the modelled phenomena are, as before, different from the physical ones, with parameters often outside the normal range, making their extraction and geometrical scalability difficult.

1.4.3 Using two models for different current levels

At high injection levels, when BJT models are not able to describe the real physics inside an SCR, the high recombination levels in the base/collector regions make them resemble a large intrinsic volume.

The approach here (first in [Cail'03]) is to divide the SCR model into two states, modelled separately:

- a low-injection state, modelled by 2 BJTs;
- a high injection state, modelled through a p-i-n diode.

Di Sarro and Rosembaum built a scalable model using this technique [Sarr'08].

The main problem here is the switching between the two models, both from the simulator point of view (given the discontinuity introduced) and the physical phenomenon (modelling the switching point).

An advanced study on this path was recently reported by Di Sarro [Sarr'10]. Many of its weak points – like continuity problems in the models switching point, high current recombination model and charge storage and transit time – were analyzed and improved. Yet, the highly empirical nature of the scaling laws makes this model difficult to handle for a full scalability.

1.5 Conclusion

Electrostatic discharge is a continuous and growing threat to the constantly down-scaled integrated circuits. To protect the latter, auxiliary circuits are made in order to detect an ESD event and to evacuate its energy.

The main devices used as protection are the diode, the classic MOSFET, the ggNMOS and the SCR. As protection circuits become more complex and tailored on specific demands, a full chip simulation, including the ESD protection, is necessary. This leads to the need of compact models for the protection devices. As these devices work in different, uncommon conditions: short high voltage pulses, modelling becomes a challenging task. Even for the common ones, like the MOS-type or the diodes, existing models have to be completed or adjusted for ESD functioning.

Each protection device introduces unwanted parasitic effects in the protected circuit. At high frequency, these become of extreme importance, possibly leading to malfunctioning. In order to avoid it, the designer has to take into account the devices used to protect his circuit. Thus, high frequency models, that be able to describe the impact a protection device has over the protected circuit, are needed.

The SCR is the most efficient ESD protection device in terms of consumed silicon area for a certain level of robustness. It is built around parasitic bipolar effects in CMOS technologies. As it is a pnpn structure, it can be seen as a pair of pnp and npn bipolar junction transistors (BJTs). Thus, first attempts to model it were based on the BJT devices. The high current behaviour in an SCR differs from the one that is modelled in BJTs. As a result, modelling the SCR with BJTs did not give the best results. Even if advanced models were able to compel, the phenomena that were modelled – and used to fit its characteristics – were not identical to the ones in a SCR, making scalability almost impossible (some parameters lose their physical sense and their normal geometrical evolution). One solution was to divide the functioning in two: one for low current, modelled with a pair of bipolar transistors, and one for high current, modelled with a p-i-n diode. The resulting model was able to follow a set of basic scalability laws, though the latter being highly empirical and difficult to modify and adapt.

The need to generalize even more these laws and extend them to other geometrical variations lead towards the development of a new model, that describe the SCR as it is and model its particularities with the right equations.

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2 The SCR Compact Model

A compact model for an SCR is required to be precise in anticipating the functioning of the device, convergent, able to be rendered scalable and to have an easy and consistent parameter extraction strategy. The work presented in this chapter was aimed at the triggering and post-triggering behaviour, the core elements of the device, where the current state of the art did not meet the above requirements. Another important aspect of each ESD protection device is the high current self-heating. Models that handle this phenomenon were reported in [Mano'08a] and specifically for an SCR in [Sarr'10]. Thus, this aspect was not further studied.

The newly developed model is built against the physics of the device. It was built so that the important functioning parameters, as the triggering and holding voltages and currents, are not a behavioural input, but an output of the model, consequence of elementary physical phenomena. These phenomena include bipolar effect, high injection beta degradation, Early effect, resistance distribution and modulation, high current recombination etc. and will be treated in this chapter. Many of them are inherited from bipolar transistors models [Gumm'70], adapted to the electrical behaviour of an SCR.

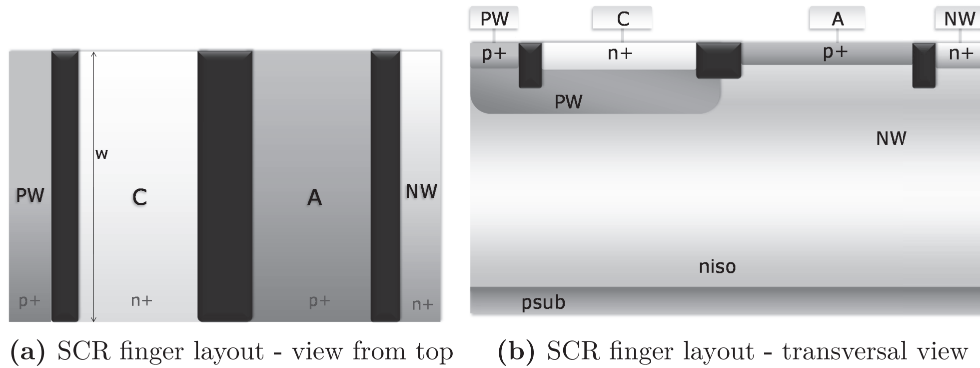
2.1 Devices description

The devices analysed in this thesis are classic multifinger silicon controlled rectifiers [Cail'03]. The level of protection assured by an SCR depends on its size: the bigger the size, the higher the ESD energy it is able to evacuate. Theoretically, the area of an electrode can be manipulated using two dimensions: its length, l , and its width, w, (Figure 2.1a).

However by increasing the length (l), the performances don't follow proportionally. This will be shown in sec. 3.2.2 and it is caused mainly by inhomogeneous current flow.

Thus, the main parameter to adjust is the SCR's width (w). This can lead to very "wide" devices, compared to their "length". In order to circumvent layout-related problem that are caused by this form factor, the devices are divided into multiple identical "fingers" connected in parallel.

Each finger is made using classic CMOS procedures (Figure 2.1b). An n-well (NW) and a p-well (PW) are created. On the NW, a p+ diffusion is done, having the role



(a) SCR finger layout - view from top **(b)** SCR finger layout - transversal view

Figure 2.1: The layout of the SCR type analysed in this thesis

of an Anode (A). On the PW, an n+ diffusion is done, having the role of a Cathode (C). The devices studied in this thesis were done using a triple well technology (the p-well is isolated from the substrate using an n layer - NISO).

2.2 DC modelling

2.2.1 Gummel-Poon model adaptation to the SCR topology

Being a pnpn structure, the main phenomenon at the base of an SCR is the bipolar effect described in Fig. 2.2 and sec. 1.3.1. The base of each transistor shares, however, the same physical volume as the collector of the complementary one. Thus, the charge balance differs in this case from what normally happens - and is modelled - in a single bipolar junction transistor (BJT).

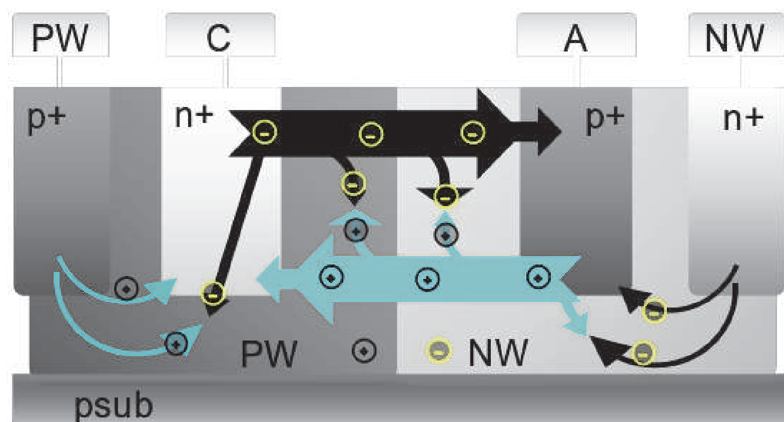


Figure 2.2: The triggering mechanism in an SCR

The developed model (Fig. 2.3), is based on classical transistor equations. However it is seen from an SCR point of view and the interactions between the different parts are taken into account.

For the BJT-type parts basis, a simple model – like the basic Ebers-Moll [Eber'54] – does not suit our requirements. It lacks important effects like high injection beta degradation, base width and resistance modulation, and so on. In order to fit the measurements, the extracted parameters would need to be optimized to compensate the non-modelled effects and, consequently, they get farther away from their physical meaning. This raises serious problems when dealing with the scalability of the model, leading to the necessity of highly empirical laws.

A step forward, the Gummel-Poon model [Gumm'70] has the base charge - a very important quantity in the behaviour of an SCR - in the centre of its equations. Therefore, modified Gummel-Poon equations, that reflect the particularities of our device, are considered for the proposed model.

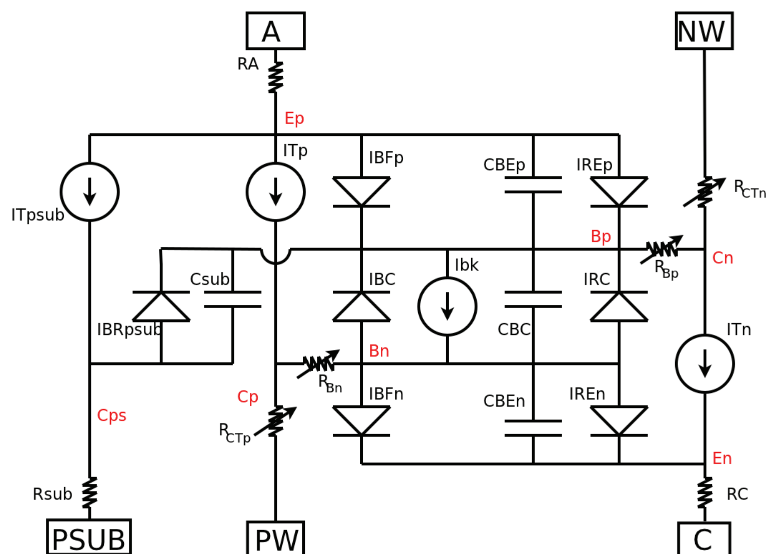


Figure 2.3: SCR model schematic

These particularities are:

- redistribution of collector and base resistance;
- modulation of the base/collector resistance;
- high injection beta degradation correction (due to physical coupling effects between the two BJTs that compose the SCR);
- transit time dependence of the currents flowing through each transistor.

More complex phenomena like Kirk effect [Kirk'62] and Early potential variation present in other advanced bipolar models [Xiao'00] were tested and found unnecessary. Quasi-saturation is, up to a certain level, taken into account through the base/collector resistance variation.

ESD-specific effects like avalanche breakdown were taken into account and modelled.

2.2.2 Basic current flow in an SCR

The basic current flow is based on common Gummel-Poon equations. In the model developed here, they represent the fundamental part of each of the two BJTs composing the SCR.

The three important terminals for the npn part are:

- the cathode (C) - acting as the emitter
- the p-well (PW) - acting as the base
- the n-well (NW) - acting as the collector

For the pnp part, these are:

- the anode (A) - acting as the emitter
- the n-well (NW) - acting as the base
- the p-well (PW) - acting as the collector

The bipolar transistor effect

The bipolar transistor effect (the collector - emitter current) is described by the I_{Tn} and I_{Tp} current sources, for the npn part and the pnp part, respectively.

$$I_{Tn} = \frac{I_{Fn} - I_{Rn}}{q_{Bn}} \tag{2.1}$$

$$I_{Tp} = \frac{I_{Fp} - I_{Rp}}{q_{Bp}} \tag{2.2}$$

with

$$I_{Fn} = I_{Sn} \cdot \left(\exp\left(\frac{V_{BEn}}{V_T} \right) - 1 \right) \tag{2.3}$$

$$I_{Rn} = I_{SRn} \left(\exp\left(\frac{V_{BC}}{V_T} \right) - 1 \right) \tag{2.4}$$

$$I_{Fp} = I_{Sp} \cdot \left(\exp\left(\frac{V_{BEp}}{V_T} \right) - 1 \right) \tag{2.5}$$

$$I_{Rp} = I_{SRp} \left(\exp\left(\frac{V_{BC}}{V_T} \right) - 1 \right) \tag{2.6}$$

V_{BEn} is the voltage drop between PW and C, thus, the base-emitter voltage of the npn transistor.

V_{BEp} is the voltage drop between NW and A, thus, the base-emitter voltage of the pnp transistor.

V_{BC} is the voltage drop between NW and PW, thus, the base-collector voltage for both the npn and pnp transistors.

V_T is the thermal voltage, defined as $V_T = \frac{k \cdot T}{q}$, where k is the Boltzmann constant ($k = 1.380 \cdot 10^{-23}\,\mathrm{J/K}$), T is the junction's temperature and q is the electron charge ($q = 1.6 \cdot 10^{-19}\,C$).

The model parameters for the equations above are:

- I_{Sn} - the forward saturation current of the npn transistor
- I_{Sp} - the forward saturation current of the pnp transistor
- I_{SRn} - the reverse saturation current of the npn transistor
- I_{SRp} - the reverse saturation current of the pnp transistor

Although the base-collector junction is controlled by the same voltage drop for both the transistors - V_{BC}, it behaves differently when it is the base-collector junction of the npn, than when being the base-collector junction of the pnp. This is caused by the fact that the conduction is assured by different types of carrier for each of the transistors: electrons for the npn and holes for the pnp. Thus, two parameters are needed to model the reverse current: I_{SRn} for the npn transistor and I_{SRp} for the pnp.

q_{Bn} and q_{Bp} are the normalized base charges and will be discussed in sec. 2.2.3.

Current gain

The base-emitter current is described by I_{BFn} and I_{BFp} for the npn part and the pnp part, respectively.

$$I_{BFn} = I_{SFn} \cdot \left(\exp\left(\frac{V_{BEn}}{V_T}\right) - 1 \right) \tag{2.7}$$

$$I_{BFp} = I_{SFp} \cdot \left(\exp\left(\frac{V_{BEp}}{V_T}\right) - 1 \right) \tag{2.8}$$

The base-collector current is described by I_R for both the npn and pnp transistors, as the junction is shared by the two.

$$I_{BC} = I_{SR} \cdot \left(\exp\left(\frac{V_{BC}}{V_T}\right) - 1 \right) \tag{2.9}$$

The model parameters for the equations above are:

- I_{SFn} - the saturation current of the base-emitter junction for the npn transistor
- I_{SFp} - the saturation current of the base-emitter junction for the pnp transistor
- I_{SR} - the saturation current for the base-collector junction

The current gain is defined as the ratio between the collector and the base current.

In forward polarisation ($V_{BE} > 0$ and $V_{BC} < 0$), the base current is only given by the base-emitter current (the base-collector current being negligible). Thus, the forward current beta is:

$$\beta_{Fn} = \frac{I_{Tn}}{I_{BFn}} = \frac{I_{Sn}\left(\exp(\frac{V_{BEn}}{V_T}) - 1\right)}{I_{SFn}\left(\exp\frac{V_{BEn}}{V_T} - 1\right)} = \frac{I_{Sn}}{I_{SFn}} \tag{2.10}$$

$$\beta_{Fpn} = \frac{I_{Tp}}{I_{BFp}} = \frac{I_{Sp}\left(\exp(\frac{V_{BEp}}{V_T}) - 1\right)}{I_{SFp}\left(\exp\frac{V_{BEp}}{V_T} - 1\right)} = \frac{I_{Sp}}{I_{SFp}} \tag{2.11}$$

In reverse polarisation ($V_{BE} < 0$ and $V_{BC} > 0$), the base current is given by the base-collector current. Thus, the reverse current gain is:

$$\beta_{Rn} = \frac{I_{Tn}}{I_{BR}} = \frac{I_{SRn}\left(\exp(\frac{V_{BEn}}{V_T}) - 1\right)}{I_{SR}\left(\exp\frac{V_{BEn}}{V_T} - 1\right)} = \frac{I_{SRn}}{I_{SR}} \tag{2.12}$$

$$\beta_{Rp} = \frac{I_{Tp}}{I_{BR}} = \frac{I_{SRp}\left(\exp(\frac{V_{BEp}}{V_T}) - 1\right)}{I_{SR}\left(\exp\frac{V_{BEp}}{V_T} - 1\right)} = \frac{I_{SRp}}{I_{SR}} \tag{2.13}$$

In the model developed here, the parameters controlling the current gain are I_{SFn}, I_{SFp} and I_{SR}, instead of the more common β. Note that for the reverse current gain only one parameter (I_{SR}) is used, the junction being shared by both transistors. Had β parameters been used, we would have been forced to have two parameters modelling the reverse current gain (β_{Rn} and β_{Rp}) that are, in fact, physically bound together (2.12, 2.13).

Low current recombination

I_{REn}, I_{REp} and I_{RC} represent the low current recombination:

$$I_{REn} = I_{SEn} \cdot \left(\exp\left(\frac{V_{BEn}}{N_{En} \cdot V_T}\right) - 1\right) \tag{2.14}$$

$$I_{REp} = I_{SEp} \cdot \left(\exp\left(\frac{V_{BEp}}{N_{Ep} \cdot V_T}\right) - 1\right) \tag{2.15}$$

$$I_{RC} = I_{SC} \cdot \left(\exp\left(\frac{V_{BC}}{N_C \cdot V_T}\right) - 1\right) \tag{2.16}$$

The model parameters for the equations above are:

- I_{SEn} - the saturation current of the npn forward low current recombination diode
- N_{En} - non-linearity factor of the forward low current recombination diode
- I_{SEp} - the saturation current of the pnp forward low current recombination diode
- N_{Ep} - non-linearity factor of the pnp forward low current recombination diode
- I_{SR} - the saturation current of the reverse low current recombination diode
- N_C - non-linearity factor of the reverse low current recombination diode

2.2.3 Base charge behaviour in an SCR

The base charge is one of the most important quantities, influencing both the DC behaviour (high injection beta degradation) and the transient one (transit time dependence of the current level).

Base charge in the Gummel-Poon model

According to the Gummel-Poon model, the base charges for the npn and pnp parts are:

$$q_{Bn} = \frac{q_{1n}}{2} \cdot \left(1 + \sqrt{1 + 4 \cdot q_{2n}}\right) \tag{2.17}$$

$$q_{Bp} = \frac{q_{1p}}{2} \cdot \left(1 + \sqrt{1 + 4 \cdot q_{2p}}\right) \tag{2.18}$$

with

$$q_{1n} = 1 + \frac{V_{BEn}}{V_{ARn}} + \frac{V_{BC}}{V_{AFn}} \tag{2.19}$$

$$q_{2n} = \frac{I_{Fn}}{I_{KFn}} + \frac{I_{Rn}}{I_{KRn}} \tag{2.20}$$

$$q_{1p} = 1 + \frac{V_{BEp}}{V_{ARp}} + \frac{V_{BC}}{V_{AFp}} \tag{2.21}$$

$$q_{2p} = \frac{I_{Fp}}{I_{KFp}} + \frac{I_{Rp}}{I_{KRp}} \tag{2.22}$$

q_{1n} and q_{1p} model the Early effect and q_{2n} and q_{2p} model the high injection beta degradation.

The model parameters for the equations above are:

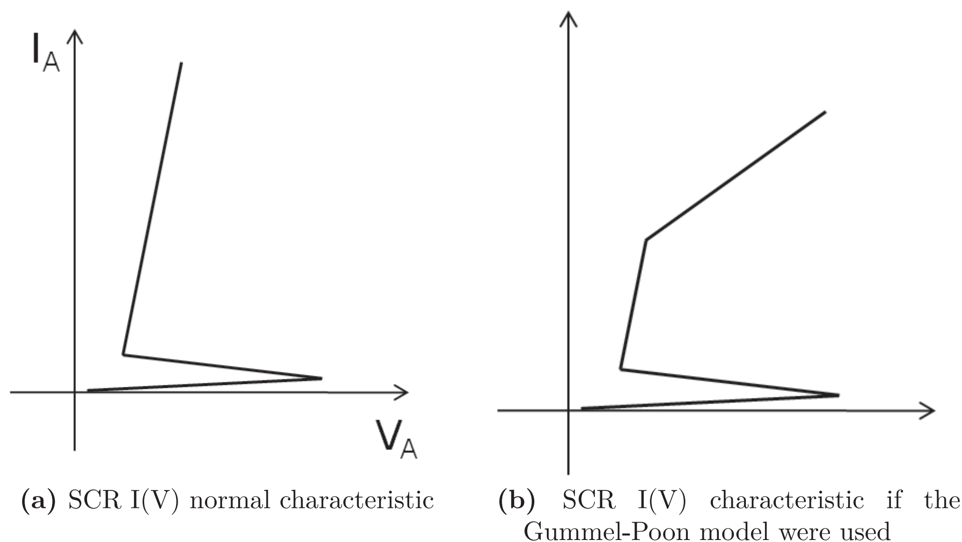
- V_{ARn} and V_{AFp} - the forward Early voltages for the npn transistor and the pnp transistor, respectively

- V_{ARp} and V_{AFn} - the reverse Early voltages for the npn transistor and the pnp transistor, respectively
- I_{KFn} and I_{KFp} - the forward knee currents for the npn transistor and the pnp transistor, respectively
- I_{KRn} and I_{KRp} - the reverse knee currents for the npn transistor and the pnp transistor, respectively

The Early parameters model the charge quantity caused by the variation of the space charge region, formed around each junction, with the voltage applied on it. The knee currents represent the current from which the collector current and, thus, the current gain, start to degrade.

High current beta degradation in an SCR

The high current beta degradation is caused by the big number of carriers in the base. They slow down the accelerated charges, reducing the collector current in respect to the base one. In the case of an SCR, the phenomenon is different (as described in sec. 1.3.1). The base charge of each of the transistors depends on the complementary one, being evacuated by its collector current. For instance, the base charge of the npn (electrons) is neutralized by the collector current coming from the pnp (holes). At high injection levels, the base/collector areas become strong recombination regions, stabilizing the current. The limitation of using bipolar transistor models are shown in Fig. 2.4.



(a) SCR I(V) normal characteristic

(b) SCR I(V) characteristic if the Gummel-Poon model were used

Figure 2.4: Modelling error introduced by using pure Gummel-Poon models for the transistors

The Gummel-Poon model predicts a too high beta degradation (Figure 2.4b), leading to a diminishing of the current after a certain level of injection. In reality (Figure 2.4a), the post-triggering current depends linearly on the voltage drop (before self-heating related phenomena appear).

Thus, a new model for q_{2n} and q_{2p} from 2.17 and 2.18 is required, so that the npn base charge depend on the pnp collector current and vice-versa. In order to maintain the consistency between the SCR and the Gummel-Poon equations, mostly for parameter extraction simplicity, the new model is required to fall-back to the one in 2.20 and 2.22 in the particular case of only one transistor being active. This was achieved by not considering the knee current as constant, but modulated by a *high current correction* factor (HCC):

$$q_{2n} = \frac{I_{Fn}}{I_{KFn} \cdot HCC_{Fn}} + \frac{I_{Rn}}{I_{KRn} \cdot HCC_{Rn}} \tag{2.23}$$

$$q_{2p} = \frac{I_{Fp}}{I_{KFp} \cdot HCC_{Fp}} + \frac{I_{Rp}}{I_{KRp} \cdot HCC_{Rp}} \tag{2.24}$$

HCC_{Fn} and HCC_{Fp} are the correction factors for the forward knee currents (I_{KFn} and I_{KFp}).

$$HCC_{Fn} = \frac{I_{rTn} + \frac{IHC_{KFn}}{I_{KFn}} \cdot \sqrt{I_{Fp}}}{I_{rTn} + \sqrt{I_{Fp}}} \tag{2.25}$$

$$HCC_{Fn} = \frac{I_{rTp} + \frac{IHC_{KFp}}{I_{KFp}} \cdot \sqrt{I_{Fn}}}{I_{rTp} + \sqrt{I_{Fn}}} \tag{2.26}$$

The model parameters for the equations above are:

- I_{rTn} - the current passing through the npn transistor from which the pnp starts to inject holes into the PW;
- IHC_{KFn} - the knee current of the npn transistor while the pnp is fully active (both transistors are simultaneous in high injection mode);
- I_{rTp} - the current passing through the pnp transistor from which the npn starts to inject electrons into the NW;
- IHC_{KFp} - the knee current of the pnp transistor while the npn is fully active (both transistors are simultaneous in high injection mode);

HCC_{Rn} and HCC_{Rp} are the correction factors for the reverse knee currents (I_{KRn} and I_{KRp}).

As at high injection (where these correction factors are needed), the transistors are forward biased, HCC_{Rn} and HCC_{Rp} are less important parts of the model and their associated parameters need not to be extracted with precision.

2.2.4 Resistances

Base-collector resistances

The base and the collector share the same regions. The npn's base and the pnp's collector resistances share the PW, while the npn's collector and the pnp's base resistances share the NW. Thus an adapted model must take the place of the classical base and collector resistances from the classical BJT one.

The PW, for example, as a base, has its main current flow made by electrons coming from the cathode. At the same time, it acts as a collector for the pnp transistor. As a collector, the main current flow is made by holes passing from the anode through a bipolar effect (Fig. 2.5).

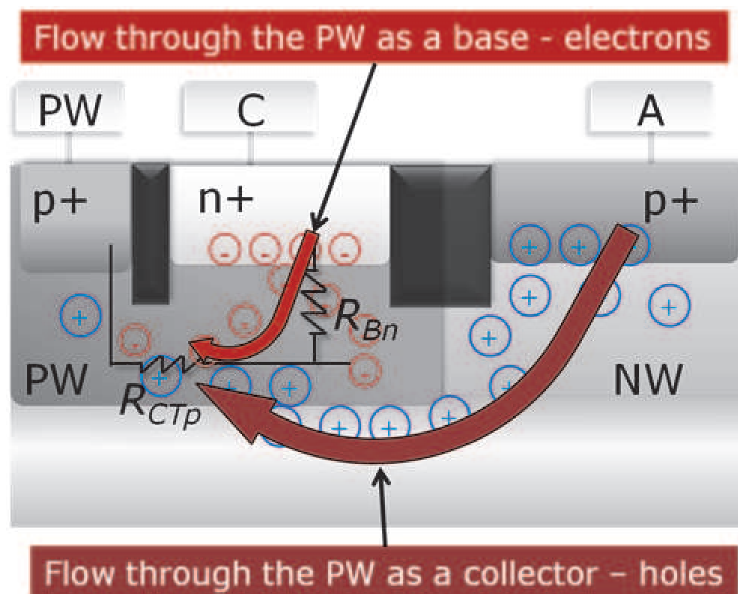


Figure 2.5: Current flow in the PW area

The difference in current flows leads to the need for a more complex model of the NW and PW resistances. The proposed solution is to divide these resistances in two parts: R_{Cp} and R_{Bn} for the PW, and R_{Cn} and R_{Bp} for the NW (Fig. 2.3). R_{Bn} and R_{Bp} are modulated by the base charge:

$$R_{Bn} = \frac{R_{Bxn}}{q_{Bn}} \tag{2.27}$$

$$R_{Bp} = \frac{R_{Bxp}}{q_{Bp}} \tag{2.28}$$

As in the Gummel-Poon model, R_{CTn} and R_{CTp} are divided into well contact resistance (R_{CMn} and R_{CMp}, respectively) and the the well-part resistance ($R_{CTn} - R_{CMn}$ and $R_{CTp} - R_{CMp}$, respectively). The latter is also modulated by the base charge, having its resistivity dependent on the carriers in its region (q_{Bn} and q_{Bp}):

$$R_{Cn} = \frac{R_{CTn} - R_{CMn}}{q_{Bp}} + R_{CMn} \tag{2.29}$$

$$R_{Cp} = \frac{R_{CTp} - R_{CMp}}{q_{Bn}} + R_{CMp} \tag{2.30}$$

The new model parameters are:

- R_{CMn} and R_{CMp} - the collector resistances at high injection (physically, the well contact resistance)
- R_{CTn} and R_{CTp} - the total collector resistance
- R_{Bxn} and R_{Bxp} - the base resistance at low injection

Emitter resistances

The model has two parameters modelling the emitter resistances:

- R_C - used to model the cathode resistance - the emitter of the npn part
- R_A - used to model the anode resistance - the emitter of the pnp part

2.2.5 Substrate modelling

The substrate effect is modelled by a parasitic pnp transistor (Fig. 2.6)

Its terminals are:

- the anode (A) - acting as the emitter
- the n-well (NW) - acting as the base
- the substrate (PSUB) - acting as the collector

Its bipolar transistor effect (collector - emitter current) is described by I_{Tpsub}:

$$I_{Tpsub} = \frac{I_{Fpsub} - I_{Rpsub}}{q_{Bpsub}} \tag{2.31}$$

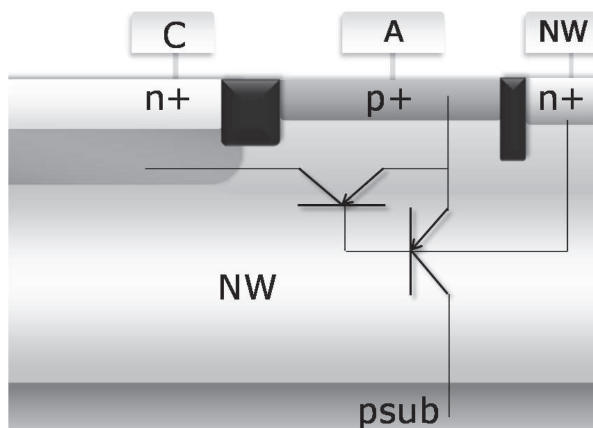


Figure 2.6: The pnp and the parasitic substrate transistors

I_{Fpsub} and I_{Rpsub} are modelled in the same way as 2.5 and 2.6.

$$I_{Fpsub} = I_{Spsub} \left(\exp\left(\frac{V_{BE}}{V_T}\right) - 1 \right) \tag{2.32}$$

$$I_{Rpsub} = I_{Rpsub} \left(\exp\left(\frac{V_{BCpsub}}{V_T}\right) - 1 \right) \tag{2.33}$$

There is no need to specially model the forward current gain for this transistor. This phenomenon is already modelled through I_{Fpsub} (with I_{Spsub} as a parameter - 2.32) and I_{BFp} (with I_{SFp} as parameter - 2.8).

$$\beta_{Fpsub} = \frac{I_{Fpsub}}{I_{BFp}} = \frac{I_{Spsub}}{I_{SFp}} \tag{2.34}$$

The reverse current gain is modelled through the substrate/nwell junction:

$$I_{BRpsub} = I_{SRpsub} \cdot \left(\exp\left(\frac{V_{BCpsub}}{V_T}\right) - 1 \right) \tag{2.35}$$

$$\beta_{Rpsub} = \frac{I_{Rpsub}}{I_{BRpsub}} = \frac{I_{Rpsub}}{I_{SRpsub}} \tag{2.36}$$

2.2.6 Breakdown modelling

Unlike the case of a BJT, where a weak base-collector avalanche model is used, the particularities of an SCR's breakdown lead to the need of a strong avalanche model:

$$I_{bk} = (MM - 1) \cdot I_{BC} \tag{2.37}$$

$$MM = \frac{1}{1 - \left(\frac{V_{BC}}{V_{BCbk}}\right)^{m_c}} \tag{2.38}$$

MM is the multiplication factor.

The model parameters are

- V_{BCbk} - the junction breakdown voltage;
- m_c - the breakdown factor, typically equal to 2.

The expression (2.37) is linearised in order to avoid the divergence at the breakdown voltage, by replacing 2.38 after the voltage reaches a certain value V_{BClin} with its tangent in that point.

$$MM = \begin{cases} 1, & V_{BC} < 0 \\ \frac{1}{1-\left(\frac{V_{BC}}{V_{BCbk}}\right)^{m_c}}, & 0 \leq V_{BC} < V_{BClin} \\ \frac{1}{1-\left(\frac{V_{BClin}}{V_{BCbk}}\right)^{m_c}} + \frac{m_c}{V_{BCbk}} \cdot \frac{\left(\frac{V_{BClin}}{V_{BCbk}}\right)^{m_c-1}}{1-\left(\frac{V_{BClin}}{V_{BCbk}}\right)^{m_c}} \cdot (V_{BC} - V_{BClin}), & V_{BC} \geq V_{BClin} \end{cases} \tag{2.39}$$

2.2.7 DC modelling summary

The base of the DC modelling is the classical Gummel-Poon model. It has been modified in order to account for the particularities of an SCR.

The biggest contributions of this thesis for the SCR model is the reformulation of the base charge, making it dependant on the simultaneous npn and pnp conduction. The dual base and collector conduction was also reconfigured, using a complex well-resistance model. The current gain was not modelled using the β parameters, as with classical BJTs, but by using the junctions saturation currents.

The substrate was found to have a significant impact on the functioning of an SCR and, thus modelled. A strong avalanche model was used for the breakdown of the central junction (NW-PW), unlike the weak avalanche model used with typical BJTs.

The choice of other specific phenomena needed to be modelled in order to well describe an SCR (like base resistance modulation, high injection beta degradation or Early effect) was also important.

2.3 Transient modelling

The model has to predict SCR behaviour under short pulses. These pulses have a duration on the order of nano-seconds, leading to a bandwidth of a couple of GHz. The capacitances constitute the main dynamic elements (Fig. 2.7). Given the dimensions of an ESD protection integrated SCR and the frequencies at which the model should be valid, the impact of the parasitic inductances can be neglected.

Each capacitance is divided in two parts: one given by the transition charges (caused by the space charge region at the p/n contact) and the second given by the diffusion charges (given by the carriers transported during the current flow)

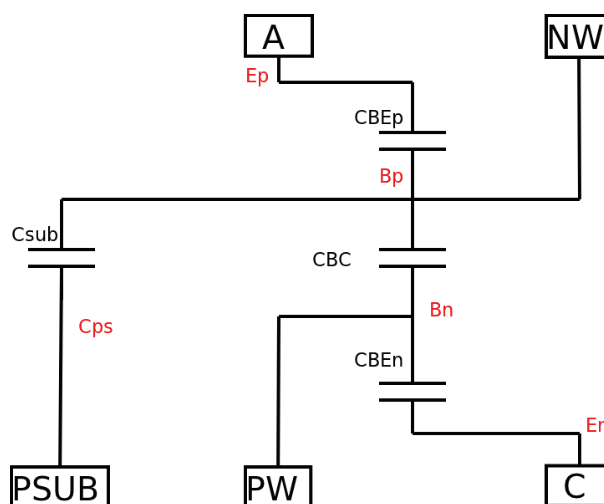


Figure 2.7: SCR's capacitances schema

$$C_{BEn} = \frac{\partial Q_{BEn}}{\partial V_{BEn}} \tag{2.40}$$

$$C_{BEp} = \frac{\partial Q_{BEp}}{\partial Q_{VEp}} \tag{2.41}$$

$$C_{BC} = \frac{\partial Q_{BC}}{\partial V_{BC}} \tag{2.42}$$

where

$$Q_{BEn} = Q_{BEn_{diffusion}} + Q_{BEn_{transistion}} \tag{2.43}$$

$$Q_{BEp} = Q_{BEp_{diffusion}} + Q_{BEp_{transistion}} \tag{2.44}$$

$$Q_{BC} = Q_{BC_{diffusion}} + Q_{BC_{transistion}} \tag{2.45}$$

The substrate being always reverse biased, a transition capacitance its enough to model its transient behaviour.

$$C_{sub} = \frac{\partial Q_{BCsub}}{\partial V_{BCsub}} \tag{2.46}$$

2.3.1 Transition charges

The transition charges are modelled using the classic Q(V) equations for a pn junction:

$$Q_{BEn_{transition}} = C_{JEn} \cdot \frac{V_{JEn} \cdot \left[1 - \left(1 - \frac{V_{BEn}}{V_{JEn}}\right)^{1-mje_n}\right]}{1 - mje_n} \tag{2.47}$$

$$Q_{BEp_{transition}} = C_{JEp} \cdot \frac{V_{JEp} \cdot \left[1 - \left(1 - \frac{V_{BEp}}{V_{JEp}}\right)^{1-mje_p}\right]}{1 - mje_p} \tag{2.48}$$

$$Q_{BC_{transition}} = C_{JC} \cdot \frac{V_{JC} \cdot \left[1 - \left(1 - \frac{V_{BC}}{V_{JC}}\right)^{1-mjc}\right]}{1 - mjc} \tag{2.49}$$

$$Q_{BCsub_{transition}} = C_{JCsub} \cdot \frac{V_{JCsub} \cdot \left[1 - \left(1 - \frac{V_{BCsub}}{V_{JC}}\right)^{1-mjc_{sub}}\right]}{1 - mjc_{sub}} \tag{2.50}$$

The model parameters are:

- C_{JEn}, C_{JEp}, C_{JC} and C_{JCsub} - the junctions' zero bias depletion capacitances;
- V_{JEn}, V_{JEp}, V_{JC} and V_{JCsub} - the built-in potentials;
- mje_n, mje_p, mjc and mjc_{sub} - the junctions' exponential factor.

2.3.2 Diffusion charges and the transit time

In the bipolar transistor theory [Getr'79], the diffusion charges are defined as the product between the current given by the charges flowing through the base and the time these charges stay in the base. The latter is called "transit time".

$$Q_{BEn_{diffusion}} = T_{FFn} \cdot \frac{I_{Fn}}{q_{Bn}} \tag{2.51}$$

$$Q_{BEp_{diffusion}} = T_{FFp} \cdot \frac{I_{Fp}}{q_{Bp}} \tag{2.52}$$

$$Q_{BC_{diffusion}} = T_R \cdot \left(\frac{I_{Rn}}{q_{Bn}} + \frac{I_{Rp}}{q_{Bp}} \right) \tag{2.53}$$

The base charge influences both the current flow and the transit time. The modification made in 2.2.3 is kept in order to reflect the SCR particularities.

T_{FFn} and T_{FFp} represent the forward transit time of the npn and pnp transistor, respectively. They are also depending on the bias and the current flow:

$$T_{FFn} = T_{Fn} \cdot \left[1 + X_{TFn} \cdot \left(\frac{I_{Fn}}{I_{Fn} + I_{TFn}} \right)^2 \cdot \exp\left(\frac{V_{BC}}{1.44 \cdot V_{TFn}} \right) \right] \tag{2.54}$$

$$T_{FFp} = T_{Fp} \cdot \left[1 + X_{TFp} \cdot \left(\frac{I_{Fp}}{I_{Fp} + I_{TFp}} \right)^2 \cdot \exp\left(\frac{V_{BC}}{1.44 \cdot V_{TFp}} \right) \right] \tag{2.55}$$

The parameters are:

- T_{Fn} and T_{Fp} - the transit times when no currents are flowing through the SCR;
- X_{TFn}, I_{TFn}, X_{TFp} and I_{TFp} - controlling the increase of T_{FFn} and T_{FFp}, respectively, at high currents;
- V_{TFn} and V_{TFp} - controlling the variation of T_{FFn} and T_{FFp}, respectively, with V_{BC} (equivalent of Early effect in DC).

2.3.3 Transient modelling summary

The transient behaviour was modelled using capacitive elements. Classical models used in BJTs, dividing the charges into depletion and transition, were employed. The high current variation of the transit time was found to be an important phenomenon, needing to be modelled.

2.4 Characterization and parameter extraction

This chapter presents the parameter extraction strategy along with the different measurements carried out in order to support it. SCR devices were realized in CMOS 40 nm and BiCMOS 130 nm technologies.

The parameters can be divided in three categories, along the different necessary kinds of measurements: DC, transient and high current (ESD). The transient and high current parameters are extracted using ESD-specific equipment and techniques. These are the Transmission Line Pulse (TLP) and the Very Fast Characterisation System (VF-TCS) [Mano'07]. The TLP is generally used to investigate very high current behaviour, most notably the self-heating, as it is able to produce very high voltage pulses. The VF-TCS is more precise than the TLP, but limited in voltage.

An exception is made by the transition capacitance. Their model parameters can be extracted from capacitance vs. voltage - C(V) - measurements of the junctions. As these are standard measurements and don't depend on a particular device (the SCR in our case) they won't be presented here. However, an extraction method using small signal measurements for the SCR's transition capacitances is presented in Chapter 4.

As the self-heating, the only effect not in the reach of the VF-TCS, is not treated in this thesis (validated models having already been reported), the TLP will not be used in the parameter extraction and model validation.

All the measures were carried out on-chip.

Measurement pads that connect to each of the 5 terminals were realized (Fig. 2.8). This allows the characterisation of each sub-transistor independently, as well as the characterisation of the SCR as a whole.

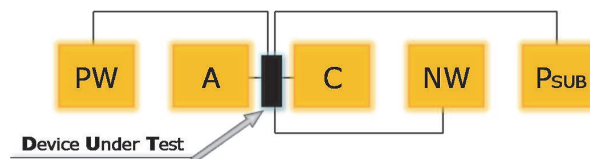


Figure 2.8: PAD structure used for the characterisation SCR devices

2.4.1 DC measurements

A high degree of similarity was kept between this model's parameter extraction strategy and BJT techniques [Sisc'01]. Classical set-ups were used for each "transistor". The parameters for the substrate pnp transistor were extracted together with the lateral pnp.

The parameters extracted using DC measurements are:

- basic current flow: I_{Sn}, I_{Sp}, I_{SRn}, I_{SRp}, I_{SFn}, I_{SFp}, I_{SR}, I_{Spsub}, I_{Rpsub}, I_{SRpsub}
- low current recombination: I_{SEn}, I_{SEp}, I_{SC}, N_{En}, N_{Ep}, N_C
- early voltages: V_{AFn}, V_{AFp}, V_{ARn}, V_{ARp}

For the following parameters sets, a first approximation is made using DC measurements, but their final values are obtained using TLP and VF-TCS measurements:

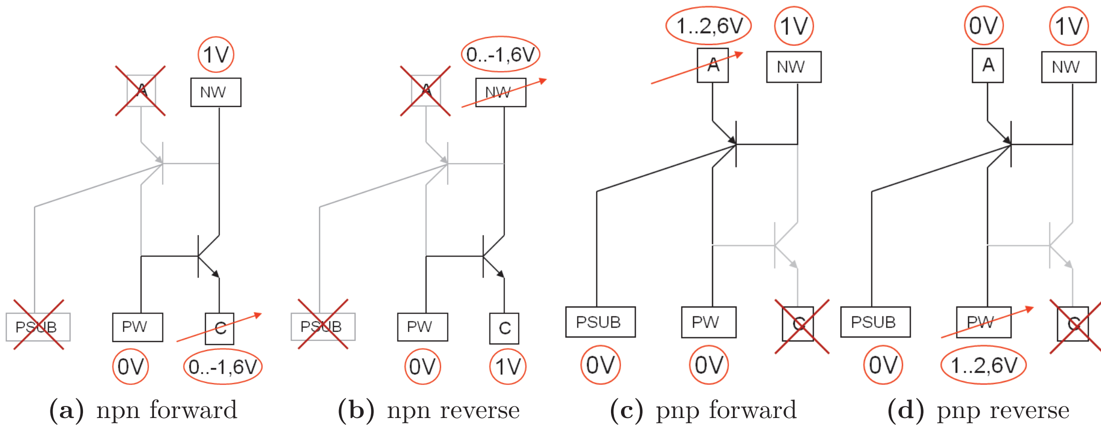
- high injection beta degradation: I_{KFn}, I_{KFp}, I_{KRn}, I_{KRp}, IHC_{KFn}, I_{rTn}, IHC_{KFp}, I_{rTp}
- resistances: R_{En}, R_{Ep}, R_{Bn}, R_{Cp}, R_{Bp}, R_{Cn}

Basic current flow extraction

In order to extract the forward basic current flow parameters, the base-emitter junction was forward biased by varying its voltage. The base-collector junction was kept under reverse bias. The collector-emitter voltage was kept at 1V (Fig. 2.9). This ensures a better consistency with the extraction of the Early effect parameters, assuring that the characterization is done in the constant part of the output plot (see Fig. 2.15).

For the reverse parameters, the same measurements were repeated, interchanging the role of the collector and the emitter. Thus, the base-collector junction was forward biased by varying its voltage, and the base-emitter voltage was kept constant (Fig. 2.13).

The measurements were done for both the npn and the pnp parts of the transistor, in both forward and reverse mode.



(a) npn forward **(b)** npn reverse **(c)** pnp forward **(d)** pnp reverse

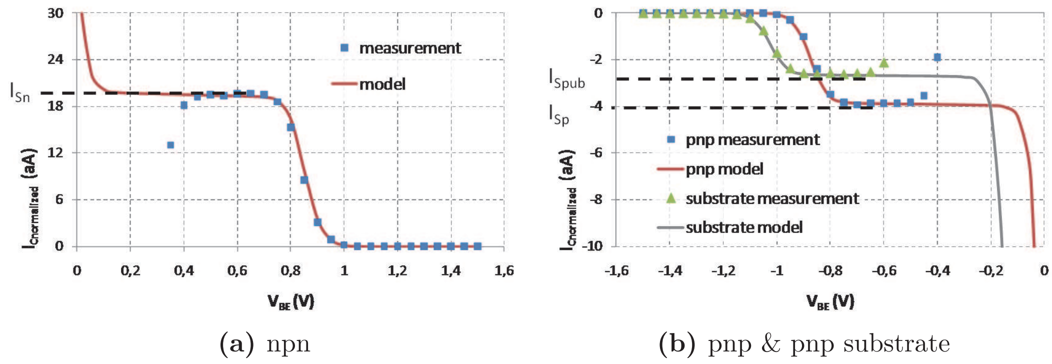
Figure 2.9: "Gummel" characterization setups for the npn and pnp transistors

I_{Sn}, I_{Sp}, and I_{SRn} were extracted from normalized collector current versus the base-emitter voltage plots ($I_{Cnormalized}$ vs. V_{BE}), while I_{SRp}, I_{Spsub} and I_{Rpsub} were

extracted from normalized emitter current versus the base-collector voltage plots ($I_{Enormalized}$ vs. V_{BC}) [Pour'07].

Fig. 2.10 shows how the forward saturation currents were extracted for the npn, pnp and substrate pnp transistors. The normalized currents used in these plots are defined by 2.56.

$$I_{Cnormalized} = \frac{I_C}{\exp \frac{V_{BE}}{V_T}} \tag{2.56}$$



(a) npn **(b)** pnp & pnp substrate

Figure 2.10: Forward saturation current extraction

In a similar way, I_{SFn} and I_{SFp}, were extracted from the normalized base current versus the base-emitter plots, while I_{SR} and I_{SRpsub} were extracted from the normalized collector current versus the base-collector voltage plots.

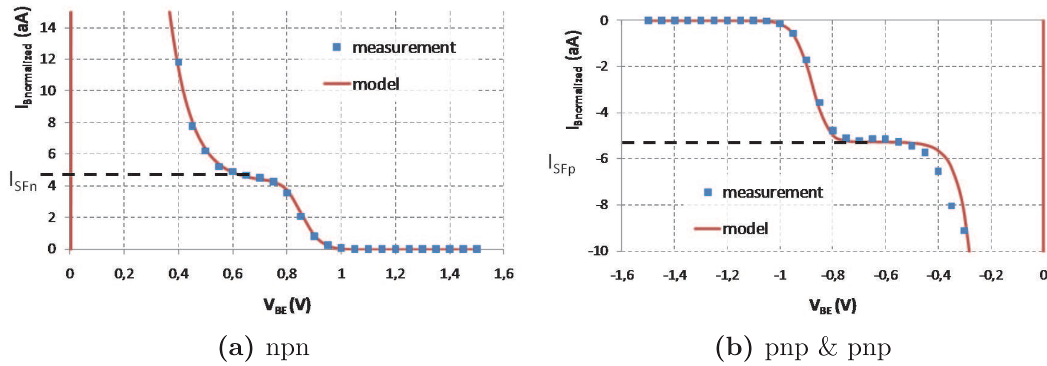
Note that I_{SR} can be extracted from both the npn and the pnp characterizations. If the values are not identical, an average can be considered.

Given the way the SCR is used as an ESD protection device, the reverse parameters, including I_{SR}, are less important.

Fig. 2.11 shows how the gain parameters were extracted. The normalized currents used in these plots is defined by (2.57).

$$I_{Bnormalized} = \frac{I_C}{\exp \frac{V_{BE}}{V_T}} \tag{2.57}$$

Note that no forward current gain parameter for the substrate transistor is extracted. The phenomenon is already taken into account by the other parameters, proved by Fig. 2.12.



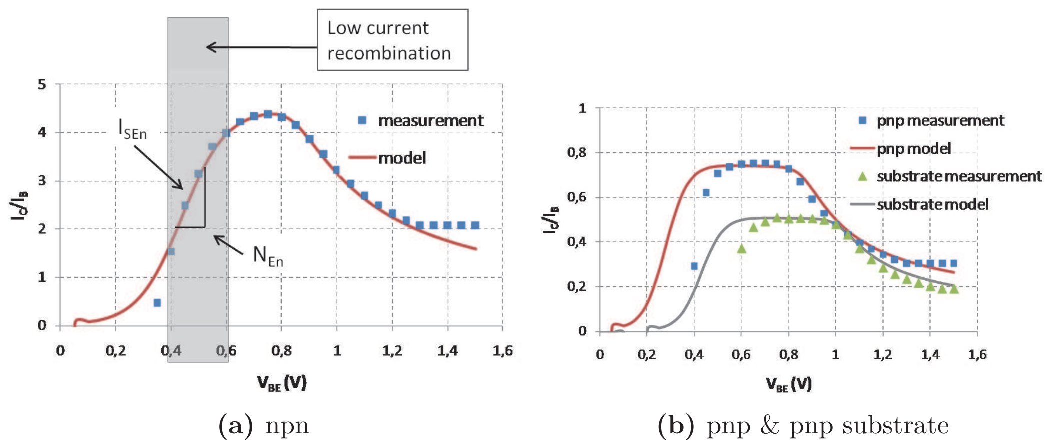
(a) npn **(b)** pnp & pnp

Figure 2.11: Forward current gain parameters extraction

Low current recombination

The low current recombination parameters were extracted and optimized using the data from the same measurements as above. I_{SEn}, I_{SEp}, N_{En} and N_{Ep} are obtained by plotting:

- the ratio between the collector and the base currents versus the base-emitter voltage - "beta plot"
- the base current versus the base-emitter voltage - "Gummel plot"



(a) npn **(b)** pnp & pnp substrate

Figure 2.12: "Beta" plots

I_{SC} and N_C were obtained by plotting:

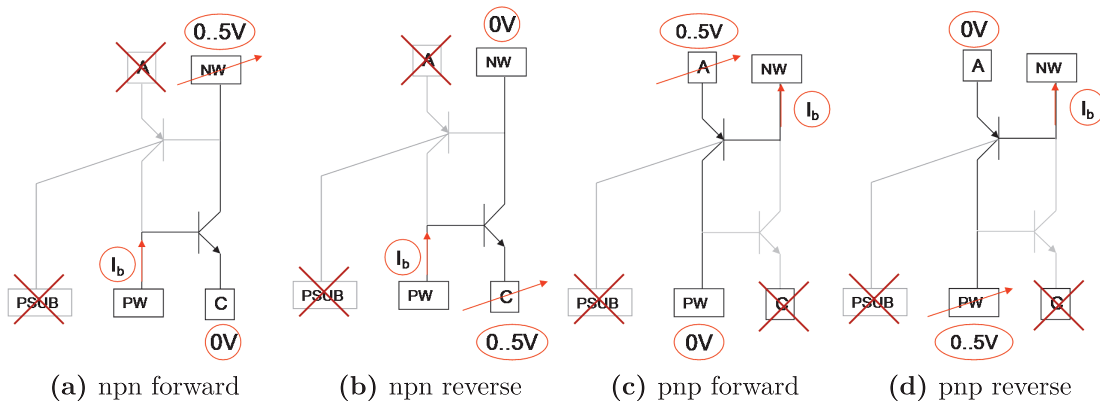
- the ratio between the base and the collector currents versus the base-emitter voltage - "reverse beta plot"
- the collector current versus the base-collector voltage - "reverse Gummel plot"

The low current recombination parameters influence the current gain at low voltages. Thus, they can be obtained by fitting the beta-plots between the voltage at which

the currents are high enough to be measured (around 0.4 V) and the voltage at which the current gain becomes constant (around 0.6 V) - Fig. 2.12.

Early voltages

The Early effect parameters were extracted from the forward and reverse output plots. The measurements made in order to obtain the output plots were made by varying the collector-emitter voltage while keeping the base current constant (Fig. 2.13).



(a) npn forward **(b)** npn reverse **(c)** pnp forward **(d)** pnp reverse

Figure 2.13: "Output" characterization setups for the npn and pnp transistors

The measurements were done for multiple base current values.

V_{ARn} and V_{ARp} are obtained from the forward output plot, while V_{AFn} and V_{AFp} are obtained from the reverse output plot.

Fig. 2.14 shows the extraction principle and Fig. 2.15 shows the actual extraction results for the V_{AFn} parameter.

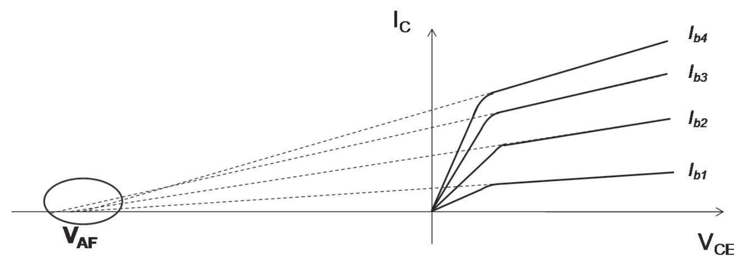


Figure 2.14: Early potential extraction principle

High injection beta degradation

The knee currents are defined as the current from which the current gain starts to degrade (Fig. 2.12). Thus, it should be natural that the extraction be done on the

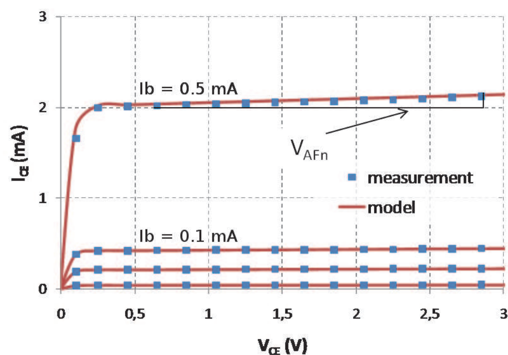


Figure 2.15: Early potential extraction for the npn transistor

beta plots. In reality, for the type of bipolar sub-structures that compose the SCR, the high current region of the plot is affected by both the knee current value and the collector and emitter resistances in an indiscernible way. In consequence, another classic method of extracting the knee current was employed, using the output characteristic (Fig. 2.16), obtained from the measurements shown in (Fig. 2.13). This approach was used for the forward knee currents, I_{KFn} and I_{KFp}.

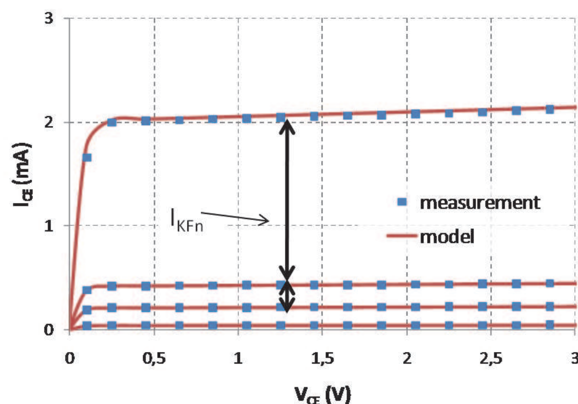
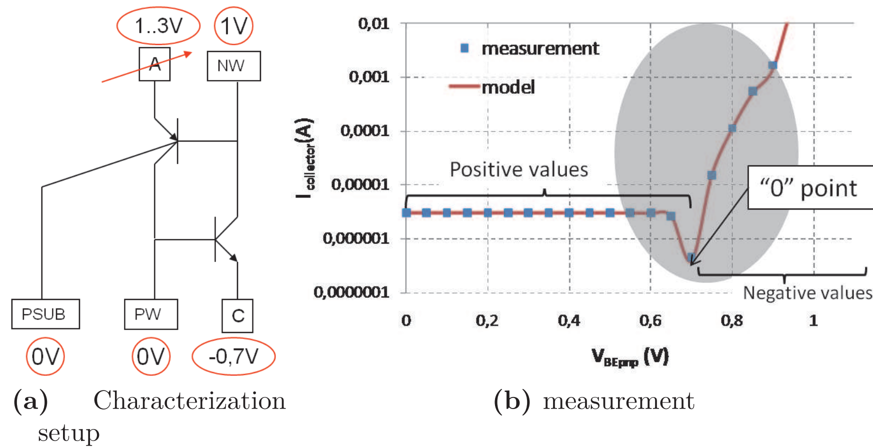


Figure 2.16: Forward knee current extraction for the npn transistor

The reverse knee current, I_{KRn} and I_{KRp}, being less important for the functioning of an SCR, can be approximated by tuning the reverse-beta plots.

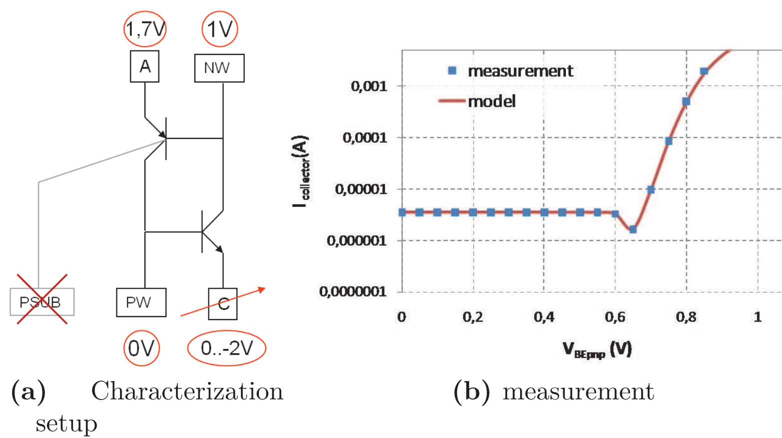
In order to obtain the information necessary to approximate the value of the SCR's specific parameters, I_{rTn}, I_{rTp}, IHC_{KFn} and IHC_{KFp}, two other measurement configurations were used (Fig. 2.17 and Fig. 2.18). The principle is to turn on one transistor, similar to what was presented in (Fig. 2.9). This time, however, the complementary transistor (the pnp when turning on the npn and vice-versa) is not deactivated, but slightly turned on using a 0.6 V bias on their base-emitter junction.

Further optimization of these values was achieved using the quasi-static turn-on I(V) characteristic of the SCR, presented in 2.4.2 (Fig. 2.26).



(a) Characterization setup **(b)** measurement

Figure 2.17: pnp controlled triggering of the SCR



(a) Characterization setup **(b)** measurement

Figure 2.18: npn controlled triggering of the SCR

Resistances

The values of the resistances are particularly hard to extract for bipolar transistors, in general. From classical measurements, only the collector resistance R_{TCn} and R_{TCp} are extracted. This was achieved on the beta-plots (Fig. 2.19), after the knee currents had been extracted. The emitter resistances also influence this plot. As their extraction can be accurately made using VF-TCS measurements (see sec. 2.4.2), it is recommended that this step be done before the extraction of the collector resistances.

The other resistance-related parameters are obtained from SCR ESD-specific measurements presented in sec. 2.4.2.

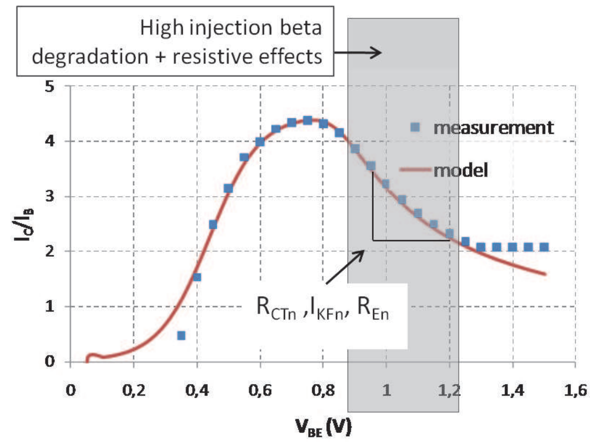
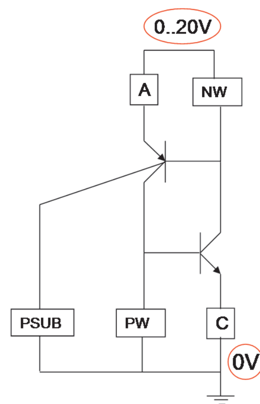


Figure 2.19: Collector resistance extraction for the npn transistor

Breakdown

V_{BCbk} and m_c were extracted by fitting the breakdown I(V) characteristic. This was obtained by applying a voltage between 0 V and 20 V on the SCR configured as a dipole device (the NW connected to the A and the PW and PSUB connected to the C - Fig. 2.20). In this configuration, the SCR turns on through the breakdown of its central (NW-PW) junction. On modern technologies, this happens between 10 V and 15 V.



(a) setup

Figure 2.20: Breakdown characterization setup

2.4.2 VF-TCS measurements

Characterisation system description

The system used to perform ESD measurements is a TLP (Transmission Line Pulse) based VF-TCS (Very Fast Transient Characterization System [Mano'08b]). Its main components are a pulse generator and an oscilloscope, leading to a TDT (Time Domain Transmission) approach, as presented in Fig. 2.21.

Figure 2.21: TDT characterization technique

The analysed device receives the ESD pulse from the generator through a 50 Ω transmission line. Its time domain response is further transmitted, also through a 50 Ω transmission line, to the oscilloscope. This is equivalent to a generator with a double amplitude and a 50 Ω internal resistance. The transmitted signal discharges to the ground through the 50 Ω input resistance of the oscilloscope. The TDT method uses the incident (V_i) and the transmitted (V_t) voltages in order to determine the current and the voltage drop on the device:

$$V = V_t \tag{2.58}$$

$$I = \frac{2 \cdot V_i - V_t}{Z_0} \tag{2.59}$$

The pulses are obtained using a pico-second generator. They are required to have a short rise-time in order to resemble the real ESD stress, according to the CDM discharge standard.

A sequential sampling oscillator is used. It offers an increased bandwidth for a repetitive signal. This allows us to obtain a better time domain resolution by constructing the device's response point by point, from a repeated set of identical pulses (Fig. 2.22).

A triggering signal is sent by the oscilloscope to the generator, indicating that the latter is ready to make the acquisition and synchronizing the acquisition. The pulses sent by the generator are divided by a T-junction device. One part is dropped on the analysed device; V_t is obtained at the oscillator level. The other part is sent directly to the oscillator, as V_i.

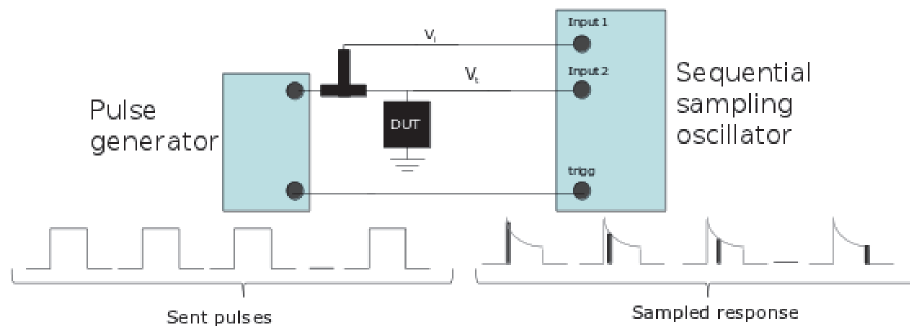


Figure 2.22: VF-TCS system

Pulse - temporal measurements

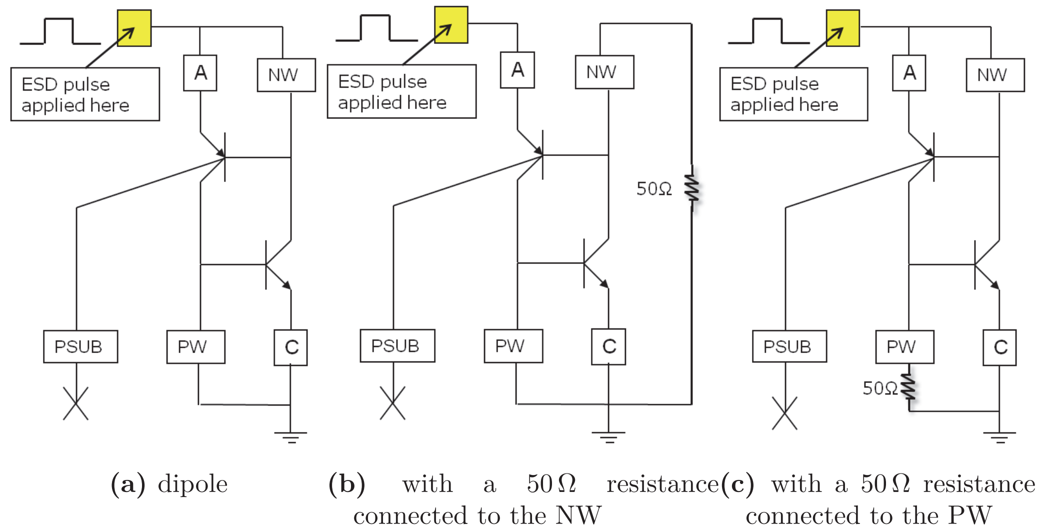
Capacitances parameters (C_J, V_J and m_j parameters) were extracted using classical C-V measurements. On the other hand, for the transient time related parameters, the extraction methods were adapted to ESD specific transient measurements. The information gathered in the time domain characteristics of a VF-TCS pulse measurement was used. Even though the procedure is not very rigorous, it offers a sufficient level of accuracy, saving characterization and extraction time.

Three measurement configurations were used (Fig. 2.23):

- dipole configuration - the NW is connected to the A and the PW and PSUB to the C; the device turns on through the breakdown of its central NW-PW junction
- 50 Ω NW - the NW is connected to the ground through a 50 Ω resistance and the PW is connected to the C; the device turns on through latch-up: the pnp transistor turns on first, triggering the npn after it.
- 50 Ω PW - the NW is connected to the A, the PW is connected to the ground through a 50 Ω resistance; the device turns on through latch-up: the npn transistor turns on first, triggering the pnp after it.

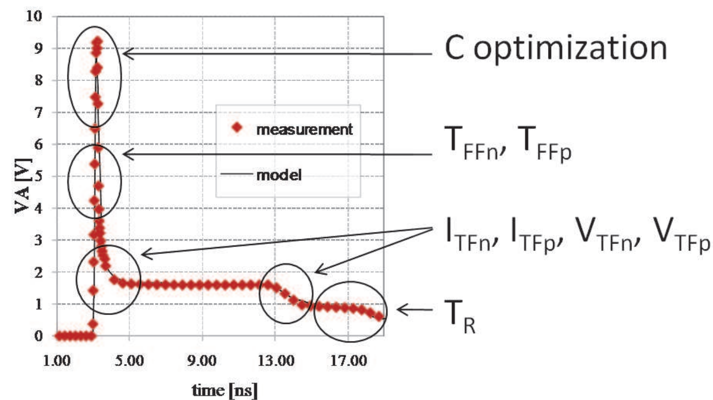
Multiple transient measurements, taken at different voltage amplitudes, are required. All the VF-TCS pulses used have a length of 9 ns. For the transit time extraction, a plot taken just after the trigger is used. Forward transit time parameters, T_{FFn} and T_{FFp} are given by the width of the overshoot. The reverse transit time, T_R is given by the post-pulse decay (Fig. 2.24).

For the high-current behaviour, I_{TFn}, I_{TFp}, V_{TFn} and V_{TFp} are tuned. X_{TF} can be considered equal to 10. This is the default value in classic BJT models. Also, as both transistors are turned on, it is impossible to differentiate between the npn and pnp effects; a factor of 2 between them was observed that can be used with good results. For instance, T_{FFp} can be considered as double than T_{FFn}.



(a) dipole **(b)** with a 50 Ω resistance connected to the NW **(c)** with a 50 Ω resistance connected to the PW

Figure 2.23: Characterization setups used to analyse the SCR



(a) measurement

Figure 2.24: Dipole VF-TCS characterization - temporal plot

Quasi-static characteristic

Quasi-static I-V characteristics are an excellent way of analysing the overall SCR behaviour under close-to-reality ESD events. Each point of the characteristic is obtained by averaging a VF-TCS pulse transient measurement (and simulation) during its stable period (Fig. 2.25).

Two ways were used for turning the device on: by turning on the pnp bipolar using a 50 Ω resistance connected to the NW and by turning on the npn bipolar by using a 50 Ω resistance connected to the PW (Fig. 2.23). The role of the 50 Ω resistances is to simulate the usual trigger environment for an SCR.

The emitter resistance are given by the high-current, post-triggering slope. A

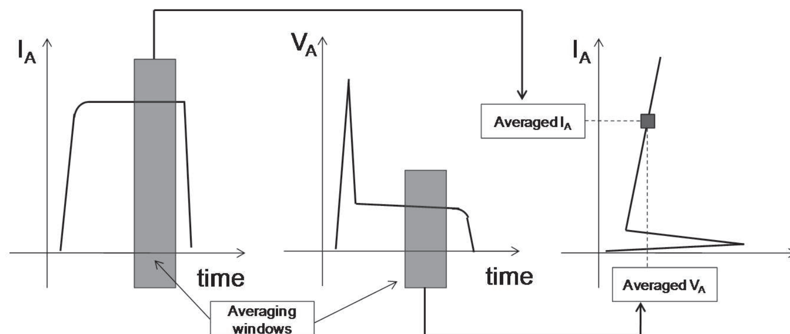


Figure 2.25: Quasi-static plot construction principle

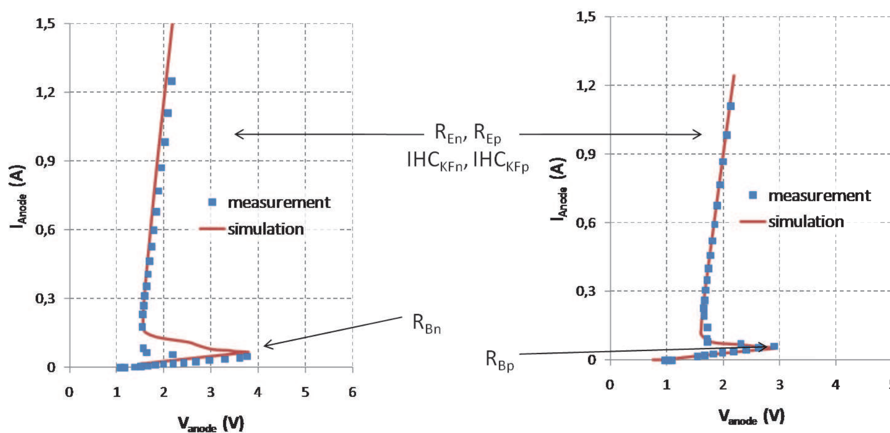


Figure 2.26: Quasi-static plots for an SCR

differentiation between R_{En} and R_{Ep} cannot be done here, nor is it necessary.

R_{Bn} influences the triggering point of the SCR turned on with a 50 Ω on the NW and the pre-triggering slope of the SCR turned on with a 50 Ω on the PW. R_{Bp} behaves in the opposite way.

A fine tuning of the triggering point can be done by optimizing the I_{rTn} and I_{rTp} parameters.

The quasi-static measurements show the real behaviour of the whole SCR. Thus, they are used for both parameter extraction and fine tuning of the DC and transient parameters, as well as for the overall validation of the model.

Overshoot characteristic

The over-shoot is an effect of extreme importance, limiting the efficiency and use of the SCR. Thus, the capability of the model to predict it, is capital.

The over-shoot plot is obtained from multiple VF-TCS transient measurements,

similar to Fig. 2.25. Instead of taking an average value of the voltage in its stable part, we plot its peak value Fig. 2.27.

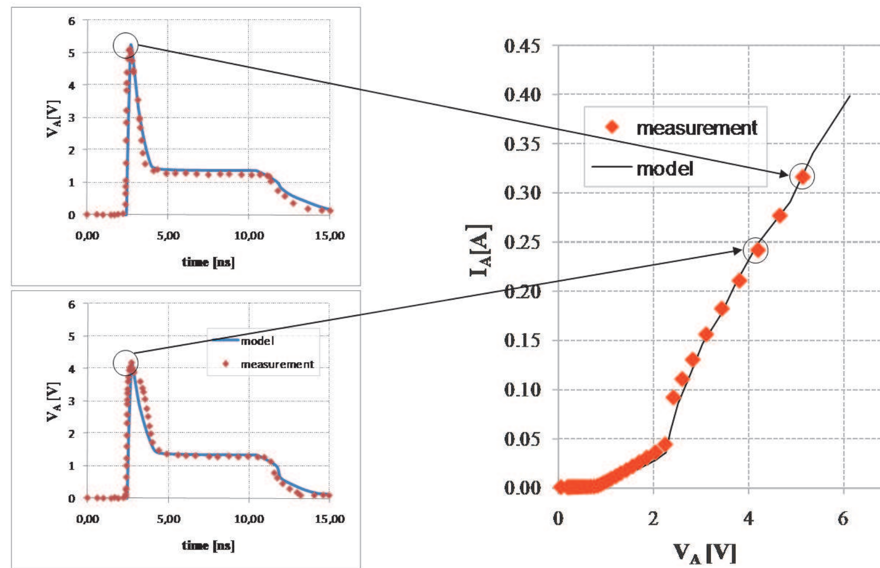


Figure 2.27: Over-shoot plot construction for an SCR

The optimized parameters are C_{JC}, V_{JC} and I_{TF}.

Fig. 2.27 shows that the model can predict with enough accuracy the peak voltage of every pulse response.

2.5 Conclusion

A novel compact model for the ESD protection SCR device has been developed. It is based on the Gummel-Poon equations with emphasis on the physics of the device. It has been validated on ST CMOS 40 nm and CMOS 130 nm technologies. The parameter extraction strategy is simple, highly based on BJT extraction techniques combined with ESD-specific characterization methods. It improves over the existent work by adapting its equations to the SCR particularities, most notably in the case of the base charge. The latter's further influence over the transit time leads to a good overall prediction of the SCR's temporal, overshoot and quasi-static behaviour. Also, being closer to the physical phenomena, the model becomes very promising for scalability, this being the next focus of our research.

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3 Scalable model

One of the reasons that lead to the development of a more complex and physical model than the state of the art [Cail'05, Font'08, Lou'08] was its ability to become scalable. Had a simpler model been considered [Sarr'10], the scaling laws would have become strongly empirical, the parameters getting farther away from their physical meaning. The SCR is a complex structure, with many effects modelling its current flow. Thus, a controlled accuracy of its behaviour would have been almost impossible to obtain if natural geometrical variation of the basic effects in semiconductors wouldn't have been preserved.

From a geometrical point of view, the bipolar parts of the ESD protection SCR are radically different than in usual bipolar junction transistors. These particularities, mostly given by the direction and homogeneity of the current flow through the base, are being analysed in this chapter. The newly proposed scaling equations, although conceptually based on known electrical/semiconductor/bipolar laws, are tailored on the reality of an SCR.

3.1 Geometry and parameters

3.1.1 Geometrical variations taken into account

The size of an SCR is important, as it defines, in the first place, the amount of current that can flow through it. This provides the ESD level that has to be assured in order to protect a certain circuit. The dimension that covers this aspect is the area of the electrodes (the anode - A and the cathode - C). The area of the electrodes is given by their width (w) and length (l). In reality, as the width would be too big for the usual SCRs in CMOS technologies, the devices are divided into multiple "fingers" connected in parallel. The total equivalent width is:

$$w = w_{finger} \cdot N_{fingers} \tag{3.1}$$

where $N_{fingers}$ is the number of fingers.

The amount of current being able to flow through the SCR varies linearly with w, but non-linearly with l, as it will be shown in sec. 3.2.2.

Thus, taking into account the two types of variations, our model can be used for:

- simulating structures for different protection levels;
- optimizing the structure at a certain protection level.

Other two requirements of a device are its triggering and holding levels. The SCR can be adjusted from this point of view by modifying the distance between its electrodes, $d2nw$.

Thus, the important geometrical dimensions taken into account for building a scalable model are:

- electrode width, w;
- electrode length, l;
- distance between the electrodes, $d2nw$;

Fig. 3.1 shows the layout of one finger, with its main dimensions.

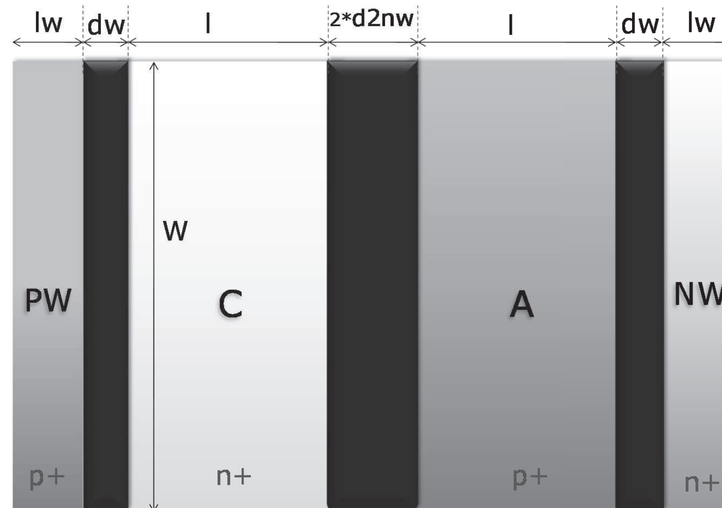


Figure 3.1: Top view of one SCR finger

3.1.2 Scalable parameters

The scaling laws are applied to the input parameters of the model presented in Chapter 2. Building a scalable model means defining their geometrical variation.

From a scaling point of view, the model's parameters can be divided into five categories:

- currents;
- resistances;
- capacitances;
- transit times;

- other (voltages, coefficients etc...).

Each category shares scaling similarities between its members. The parameters are grouped as following:

Currents

- Current flow control: I_{Sn}, I_{SRn}, I_{Sp}, I_{SRp}, I_{Spsub}, I_{SRpsub}
- Gain control: I_{SFn}, I_{SFp}, I_{SR}
- Low current recombination: I_{SEn}, I_{SEp}, I_{SC}
- Knee currents: I_{KFn}, I_{KRn}, I_{KFp}, I_{KRp}, IHC_{KFn}, IHC_{KFp}
- High injection recombination: I_{rTn}, I_{rTp}

Resistances

- Emitter resistances: R_A, R_C
- Base/collector resistances: R_{Bn}, R_{CMn}, R_{CTn}, R_{Bp}, R_{CMp}, R_{CTp}, R_{Cpsub}

Capacitances

- junction (transition) capacitances: C_{JEn}, C_{JEp}, C_{JC}, C_{JS}

Transit time

- diffusion effect: T_{FFn}, T_{FFp}, T_R

Others

Some of the model's parameters can be considered constant:

- low current recombination non-linearity factors: N_{En}, N_{Ep}, N_C
- early voltages: V_{AFn}, V_{ARn}, V_{AFp}, V_{ARp}
- breakdown effect: V_{BCbk}, m_c
- junctions built-in potentials: V_{JEn}, V_{JEp}, V_{JC}, V_{JCsub}
- junctions exponential factors: mje_n, mje_p, mjc, mjc_{sub}

Their variation was unobservable or small enough to have little to no impact on the behaviour of the SCR.

3.1.3 The test plan

In order to conceive, test and extract the parameters for the scaling laws, a number of devices were manufactured.

One device was considered as reference. At least two other devices were realized for each geometrical variation taken into account. The size of the reference device was chosen to be able to protect at an usual level - see Tab. 3.1.

device	$w\,(\mu m)$	$l\,(\mu m)$	$d2nw\,(\mu m)$
SCR1	80	1.38	0.31
SCR2	120	1.38	0.31
SCR3	160	1.38	0.31
SCR4	80	0.66	0.31
SCR5	80	2.1	0.31
SCR6	80	1.38	0.62
SCR7	80	1.38	0.93

Table 3.1: DOE - Design of Experiment for SCR scalability

For the variation of the length l, two sizes, one smaller and one bigger, were chosen. The smaller is set at half of the length of the reference, the bigger at twice. Very small sizes of l are not efficient, as the "auxiliary" parts of one finger (the NW and PW) would become comparable to the actual useful surface (the electrodes). Big lengths are also not efficient, as the current flow does not increase linearly with l (as it will be shown below).

$d2nw$ was increased, from its minimum size - the usual for an SCR, up to its tripple, in order to test the ability to tune the triggering and holding points, as well as its drawback on the turn-on time.

SCR1 is the reference device. For the other devices, except for the dimensions whom variation is studied, all the others are inherited from SCR1:

- SCR2 and SCR3 represent w variations
- SCR4 and SCR5 represent l variations
- SCR6 and SCR7 represent $d2nw$ variations

3.2 Scaling laws

3.2.1 The base width concept in an SCR

The base width is an important element of many bipolar transistor's parameters. As it will be shown below, for an ESD protection SCR, this element plays an important

role in the parameter's variation with the length of the electrodes (l) and the distance between them ($d2nw$).

In bipolar transistors, the base is considered thin, having its width constant, only dependant on the technological process. In the case of an SCR, the base region is the entire PW, for the npn part, or NW, for the pnp part. The current distribution is more complex in such a structure, being a mixture between a lateral and a vertical flow. TCAD studies [Bour'10] showed that the current density resembles the one in Fig. 3.2. This is easily explainable by considering a distributed model for the base. Because of its resistance, the voltage drop will be higher near the centre of the SCR and lower near its extremities.

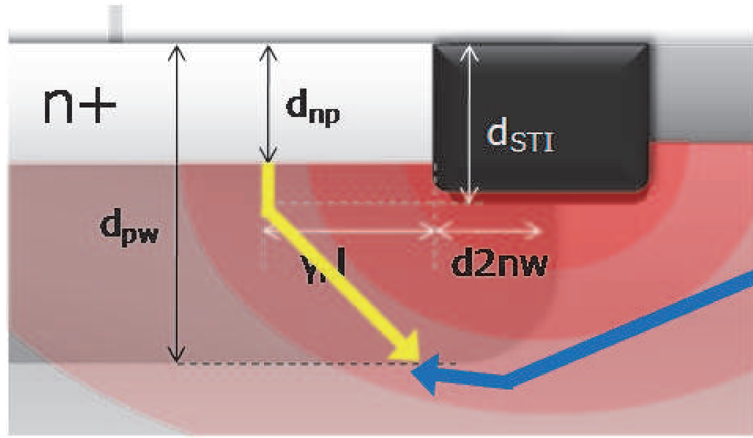


Figure 3.2: Current density distribution in a turned-on ESD protection SCR

Thus, the current density will be higher near the centre. This current crowding leads to a diagonal equivalent flow of the current. We shall generalize the concept of base width, defining it as the average distance covered by the carriers through the base. This distance, being the measure of a diagonal, will also depend on the horizontal dimensions of the SCR, as l.

The dimensions involved in computing the effective base width are shown in Fig. 3.3.

where:

- d_{np} is the depth of the emitter diffusion
- d_{STI} is depth of the STI (Silicon Trench Isolation) wall
- d_{pw} is the depth of the PW diffusion
- γ is the verticality factor of the current flow.

γ indicates how much the length of the electrodes (l) influences the verticality of the current flow and, thus, the effective base width. It is a measure of the current crowding effect.

There are three big differences between the npn and the pnp from the effective base width computation point of view:

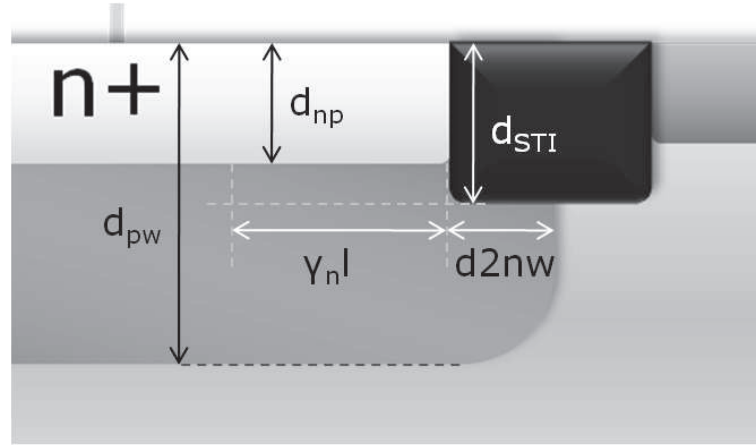


Figure 3.3: SCR's transversal view: details of the technological geometric dimensions

- the verticality factor, γ, is different, the pnp being more horizontal;
- the pnp part has a more complex current flow; a supplementary parameter, N_{γ_p} is meant to cover this aspect; it represents the form factor of the pnp's current flow and was found to typically be between 2 and 3; it is a scaling fitting parameter.
- $d2nw$ only influences the behaviour of the pnp base width;

The latter was observed by extracting parameters of structures having different $d2nw$ values. The effective base width of the pnp part, W_{Bp}, was found to vary with the double of $d2nw$. This is schematically represented in Fig. 3.2.

Thus, the effective base widths can be writthen as:

$$W_{Bn} = \sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d \tag{3.2}$$

$$W_{Bp} = \sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma_p}} + \Delta d_w^2} + \Delta d_d \tag{3.3}$$

where

$$\Delta d_w = d_{pw} - d_{STI} \tag{3.4}$$

$$\Delta d_d = d_{STI} - d_{np} \tag{3.5}$$

3.2.2 Currents scalability

Bipolar effect saturation currents

Considering a simplified approach, with no recombination, the saturation current of a bipolar transistor [Getr'79] is :

$$I_S = \frac{q \cdot A_E \cdot D_{nB} \cdot n_{iB}^2}{N_{AB} \cdot W_B} \tag{3.6}$$

where:

- q is the electron charge,
- N_{AB} is the number of acceptors in the base,
- D_{nB} is the electrons diffusion coefficient in the base,
- n_{iB} is the intrinsic concentration in the base,
- A_E the emitter area,
- W_B the base width;

The parameter is, thus, proportional to the emitter area and to the reverse of the base width. If we note $J_S^w = \frac{q \cdot D_{nB} \cdot n_{iB}^2}{N_{AB}}$, then:

$$I_S = \frac{J_S^w \cdot A_E}{W_B} \tag{3.7}$$

The scaling equations for the transistor effect saturation currents can, thus, be written as:

$$I_{Sn} = \frac{J_{Sn}^w \cdot l \cdot w}{\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d} \tag{3.8}$$

$$I_{Sp} = \frac{J_{Sp}^w \cdot l \cdot w}{\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma_p}} + \Delta d_w^2} + \Delta d_d} \tag{3.9}$$

$$I_{Spsub} = \frac{J_{Spsub}^w \cdot (l + \gamma_{snw} \cdot d2nw) \cdot w}{W_{Bpsub}} \tag{3.10}$$

W_{Bpsub} is the distance between the p+ diffusion that makes the Anode and the substrate. As it is a constant technological parameter, we can include it in J_{Spsub}, defined as:

$$J_{Spsub} = \frac{J^w_{Spsub}}{W_{Bpsub}} \tag{3.11}$$

Thus:

$$I_{Spsub} = J_{Spsub} \cdot (l + \gamma_{snw} \cdot d2nw) \cdot w \tag{3.12}$$

It was observed that the value of I_{Spsub} increases with $d2nw$. This can be explained by the fact that the pnp part of the SCR and the pnp substrate share their base and emitter, only having a different collector, the PW and the PSUB region, respectively. As $d2nw$ increases, the PW gets farther away from the emitter, decreasing the probability that the holes be collected by it and increasing the probability that they be collected by the PSUB. γ_{snw} is a measure of this effect. It is, by default, equal to 1.

Note that I_{Sn} and I_{Sp} depend on l both proportionally, at the nominator, in a linear way, and inversely proportionally, at the denominator, in a non-linear way. This makes the dependency of the overall behaviour of the SCR on l non-trivial.

The knee currents and the ones modelling the transit time dependence on the current level follow the same pattern:

Knee currents

$$I_{KFn} = \frac{J^w_{KFn} \cdot l \cdot w}{\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d} \tag{3.13}$$

$$I_{KFp} = \frac{J^w_{KFp} \cdot l \cdot w}{\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma p}} + \Delta d_w^2} + \Delta d_d} \tag{3.14}$$

$$I_{KRn} = \frac{J^w_{KRn} \cdot l \cdot w}{\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d} \tag{3.15}$$

$$I_{KRp} = \frac{J^w_{KRp} \cdot l \cdot w}{\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma p}} + \Delta d_w^2} + \Delta d_d} \tag{3.16}$$

$$IHC_{KFn} = \frac{JHC_{KFn}^{w} \cdot l \cdot w}{\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d} \tag{3.17}$$

$$IHC_{KFp} = \frac{JHC_{KFp}^{w} \cdot l \cdot w}{\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma_p}} + \Delta d_w^2} + \Delta d_d} \tag{3.18}$$

Transit time dependence on the current level

$$I_{TFFn} = \frac{J_{TFFn}^{w} \cdot l \cdot w}{\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d} \tag{3.19}$$

$$I_{TFFp} = \frac{J_{TFFp}^{w} \cdot l \cdot w}{\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma_p}} + \Delta d_w^2} + \Delta d_d} \tag{3.20}$$

Junctions saturation currents

The saturation currents of the base-emitter junctions, responsible with the base current and, thus, the current gain, do not depend on the base width, but on the emitter "thickness" (it will not be called emitter width so that it don't be confused with w):

$$I_{SF} = \frac{q \cdot A_E \cdot D_{pE} \cdot n_{iB}^2}{N_{DE} \cdot W_E} \tag{3.21}$$

The emitter thickness is a technological constant, given by the thickness of the anode and cathode implants. Thus, the scaling parameter J_{SF} will only be normalized to the emitter area.

$$I_{SF} = J_{SF} \cdot A_E \tag{3.22}$$

The scaling equations for the saturation currents of the base-emitter junctions have been set as:

$$I_{SFn} = J_{SFn} \cdot l \cdot w \tag{3.23}$$

$$I_{SFp} = J_{SFp} \cdot l \cdot w \tag{3.24}$$

Using an equivalent approach, the saturation current of the central junction will be:

$$I_{SR} = \frac{J_{SR}^{w} \cdot lw \cdot w}{l + d2nw + d_{pw} + \Delta d_d} \tag{3.25}$$

In this case, the equivalent emitter area is the one of the well contact, $lw \cdot w$.

Note that the well width, lw, has been considered a constant. This model does not cover the scalability with lw; in practice, when designing an ESD protection SCR, the lw is kept at its minimum dimension allowed by the technology. Moreover, being a reverse parameter, I_{SR}'s impact on the overall behaviour of the device is smaller. Thus, the level of accuracy targeted for its scaling law was lower. The denominator's expression in 3.25 is considered to be a good enough approximation of the equivalent emitter thickness.

Recombination currents

On the contrary, the parameters representing recombination currents are proportional to the entire volume (the bigger the volume, the higher the recombination probability). However, the dependence of the low current recombination on the base width was found to have too little significance to be taken into account.

$$I_{SEn} = J_{SEn} \cdot l \cdot w \tag{3.26}$$

$$I_{SEp} = J_{SEp} \cdot l \cdot w \tag{3.27}$$

$$I_{SC} = J_{SC} \cdot lw \cdot w \tag{3.28}$$

$$I_{rTn} = J_{rTn}^{w} \cdot l \cdot w \cdot \left(\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d \right) \tag{3.29}$$

$$I_{rTp} = J_{rTp}^{w} \cdot l \cdot w \cdot \left(\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma_p}} + \Delta d_w^2} + \Delta d_d \right) \tag{3.30}$$

3.2.3 Resistance scalability

As a general rule, the resistances are proportional with their length and inversely proportional to their section.

Applied to the geometry of an SCR, this leads to the following laws:

$$R_A = \frac{R_{A_A}}{l \cdot w} \tag{3.31}$$

$$R_C = \frac{R_{C_A}}{l \cdot w} \tag{3.32}$$

The npn's emitter is the cathode and the pnp's is the anode. The two resistances only depend on the area of the two electrodes. The "length" of the resistor is the electrodes thickness, a technological constant included in the normalized parameters R_{En_A} and R_{Ep_A}.

$$R_{CMn} = \frac{R_{CMn_A}}{w} \tag{3.33}$$

$$R_{CMp} = \frac{R_{CMp_A}}{w} \tag{3.34}$$

R_{CMn} and R_{CMp} are the minimum resistances of the collector, that is, the resistances that are below the well contacts. Thus, they only vary with the contact's area. As the contact's length, lw in Fig. 3.1, is not a geometric variation taken into account, it is introduced in the value of the normalized parameters R_{CMn_A} and R_{CMp_A}.

$$R_{CTn} = \frac{R_{CMn_A}}{w} + \frac{R_{CTn_l} \cdot l + R_{CTn_{d2nw}} \cdot d2nw}{w \cdot l} \tag{3.35}$$

$$R_{CTp} = \frac{R_{CMp_A}}{w} + \frac{R_{CTp_l} \cdot l + R_{CTp_{d2nw}} \cdot d2nw}{w \cdot l} \tag{3.36}$$

R_{CTn} and R_{CTp} comprise, through the way they were defined in Chapter 2, both the non high-injection modulated parts, R_{CMn} and R_{CMp}, and the modulated ones. Their variation with the geometry differs. Thus, the scaling law has two terms.

$$R_{Bn} = \frac{R_{Bn_l} \cdot l + R_{Bn_{d2nw}} \cdot d2nw}{w \cdot l} \tag{3.37}$$

$$R_{Bp} = \frac{R_{Bp_l} \cdot l + R_{Bp_{d2nw}} \cdot d2nw}{w \cdot l} \tag{3.38}$$

The semiconductor resistivity differs near the boundary between the NW and the PW, under the STI (isolation) between the anode and the cathode. Thus, for the four resistance parameters defining the base, R_{CTn}, R_{CTp}, R_{Bn} and R_{Bp}, a separate dependence on l and $d2nw$ has to be taken into account. This results in the need of having two normalized parameters for each of them.

$$R_{Cpsub} = \frac{R_{Cpsub}}{(l + d2nw) \cdot w} \tag{3.39}$$

The substrate resistance was found to vary after the law in 3.39. This is not a very precise law, but it is accurate enough to catch the influence R_{Cpsub} has on the overall behaviour of the SCR.

3.2.4 Capacitances scalability

The capacitances are divided into a surface dependent component (C_{bottom}) and a perimeter dependent one (C_{STI}). This is a standard in junctions modelling [Wu'04]. As the junction capacitance model is not dependent on a particular device, the canonical approach was kept, as its extraction can be done independently.

$$C_{JEn} = C_{JEn_{bottom}} \cdot l \cdot w + C_{JEn_{STI}} \cdot 2 \cdot (l + w) \tag{3.40}$$

$$C_{JEp} = C_{JEp_{bottom}} \cdot l \cdot w + C_{JEp_{STI}} \cdot 2 \cdot (l + w) \tag{3.41}$$

$$C_{JC} = C_{JC_{bottm}} \cdot (l + d2nw + dwell + \frac{lw}{2}) \cdot w + C_{JC_{STI}} \cdot 2 \cdot (l + d2nw + dwell + \frac{lw}{2} + w) \tag{3.42}$$

$$C_{JCsub} = C_{JCsub_{bottom}} \cdot 2 \cdot (l + d2nw + dwell + lw) \cdot w + C_{JCsub_{STI}} \cdot 4 \cdot (l + d2nw + dwell + lw + w) \tag{3.43}$$

3.2.5 Transient parameters scalability

The transit time is proportional to the length the carriers have to cover:

$$T_{Fn} = T_{Fn0} \cdot \left[\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d\right] \tag{3.44}$$

$$T_{Fp} = T_{Fp0} \cdot \left[\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma_p}} + \Delta d_w^2} + \Delta d_d\right] \tag{3.45}$$

$$T_R = T_{R0} \cdot \left(\frac{lw}{l} \cdot l + d2nw + d_{pwell} + \Delta d_d\right) \tag{3.46}$$

3.3 Characterization and validation

Each of the devices was characterized and had its parameters extracted as described in Chapter 2. One device, SCR 1 in Tab. 3.1, was used as a reference. The normalized parameters are mainly (see the final note in sec. 3.3.1) obtained from it.

There are two categories of scaling parameters:

- normalized parameters, such as: J_{Sn}^w, J_{Sp}^w, R_{A_A}, R_{C_A} etc.
- scaling fit parameters: γ_n, γ_p, N_{γ_p}, γ_{snw}

3.3.1 Scaling parameters extraction and individual parameter scaling validation

Currents

For SCR1, I_{Sn} from 3.8 is defined as:

$$I_{Sn1} = \frac{J_{Sn}^w \cdot l_1 \cdot w_1}{\sqrt{(\gamma_n \cdot l_1)^2 + \Delta d_w^2} + \Delta d_d} \tag{3.47}$$

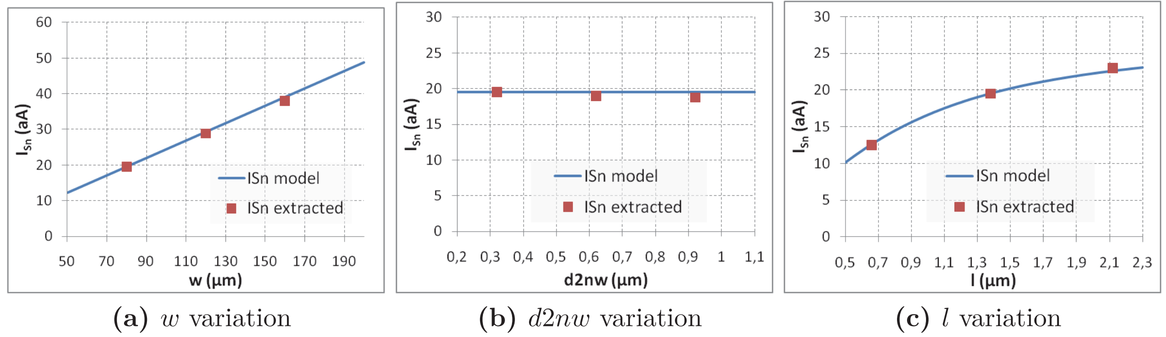
- I_{Sn1} is the value of I_{Sn} extracted for the SCR1 device Fig. 2.10
- l_1, w_1 are obtained from Tab. 3.1
- Δd_w and Δd_d are technological constants, defined in 3.4 and 3.5

The scaling parameters needing to be extracted are J_{Sn}^{w} and γ_n. The γ_n parameter will first be considered as known, with a default value of 0.3. It will be later optimized by using the data obtained from the other devices (Fig. 3.4).

Thus, the normalized scaling parameter is:

$$J_{Sn}^{w} = \frac{I_{Sn1} \cdot \sqrt{(\gamma_n \cdot l_1)^2 + \Delta d_w^2} + \Delta d_d}{l_1 \cdot w_1} \tag{3.48}$$

Introducing J_{Sn}^{w} in 3.8, we vary each of the scaling parameters, w (Figure 3.4a), $d2nw$ (Figure 3.4b) and l (Figure 3.4c), while keeping the other two at the constant value of the reference device. We compare the parameters given by the scaling law with the ones obtained through individual extraction (Fig. 3.4).



(a) w variation **(b)** $d2nw$ variation **(c)** l variation

Figure 3.4: I_{Sn} scaling law validation

γ_n is obtained by fitting 3.4b. This is done by consequently changing its value and recalculating J_{Sn}^{w}, until the error for the points at $l = 0.66\,\mu m$ and $l = 2.1\,\mu m$ (in 3.4c) is minimum. In the case presented here, γ_n was found to be equal to 0.4.

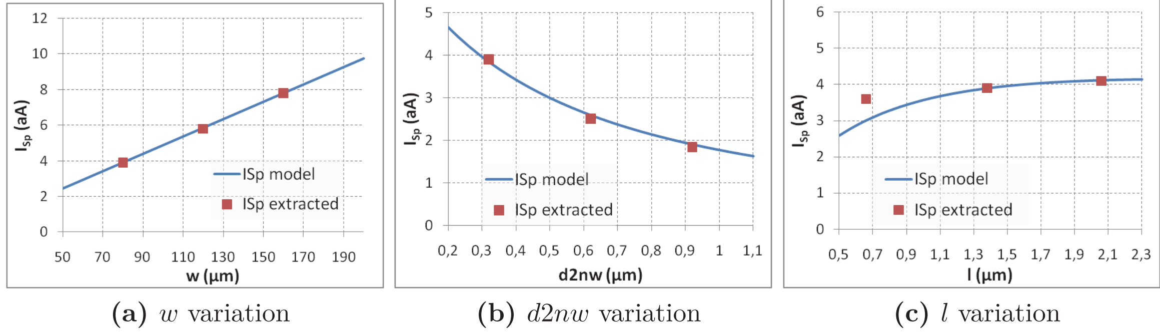
J_{Sp}^{w} is obtained by using the same approach and considering $\gamma_p = 0.7$ and $N_{\gamma_p} = 2$:

$$J_{Sp}^{w} = \frac{I_{Sp1} \cdot \sqrt{(\gamma_p \cdot l_1 + 2 \cdot d2nw)^{N_{\gamma_p}} + \Delta d_w^2} + \Delta d_d}{l_1 \cdot w_1} \tag{3.49}$$

After fitting the curves (Fig. 3.5), γ_p was found to be equal to 0.75 and N_{γ_p} to 2.75.

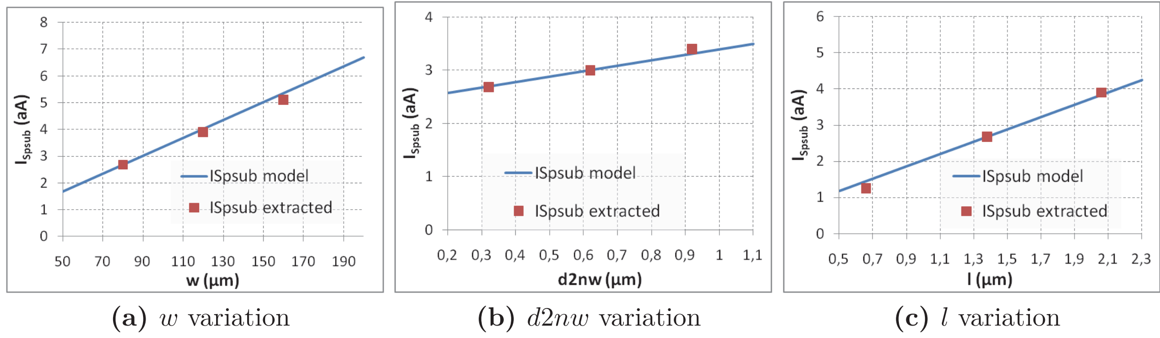
The normalized saturation current of the substrate parasitic bipolar saturation current is:

$$J_{Spsub} = \frac{I_{Spsub1}}{(l + \gamma_s \cdot d2nw) \cdot w} \tag{3.50}$$



(a) w variation (b) $d2nw$ variation (c) l variation

Figure 3.5: I_{Sp} scaling law validation



(a) w variation (b) $d2nw$ variation (c) l variation

Figure 3.6: I_{Spsub} scaling law validation

γ_S is considered by default as equal to 1. It is optimized in order to better fit the curves in Fig. 3.6. Its value after the optimization in the case presented here is 0.6.

The normalized parameters for I_{SFn} and I_{SFp} are obtained from 3.23 and 3.24, with the parameters extracted from SCR1:

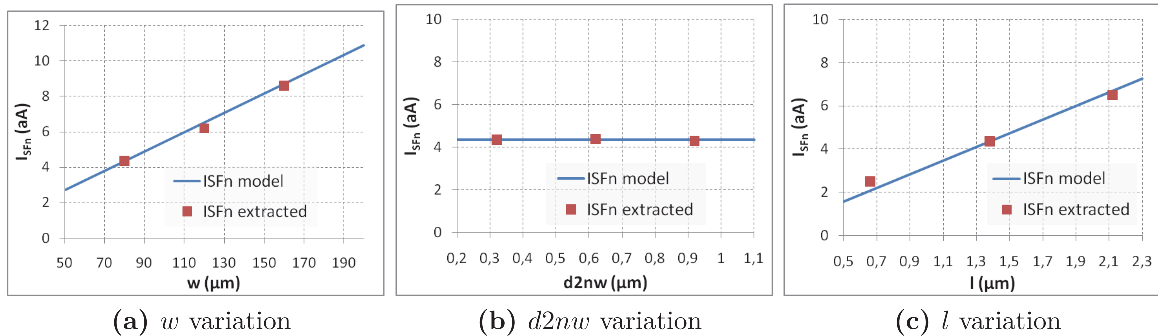
$$J_{SFn} = \frac{I_{SFn1}}{l_1 \cdot w_1} \tag{3.51}$$

$$J_{SFp} = \frac{I_{SFp1}}{l_1 \cdot w_1} \tag{3.52}$$

The prediction accuracy of the scaling law with respect to the three variation is shown in Fig. 3.7 for I_{SFn} and in Fig. 3.8 for I_{SFp}.

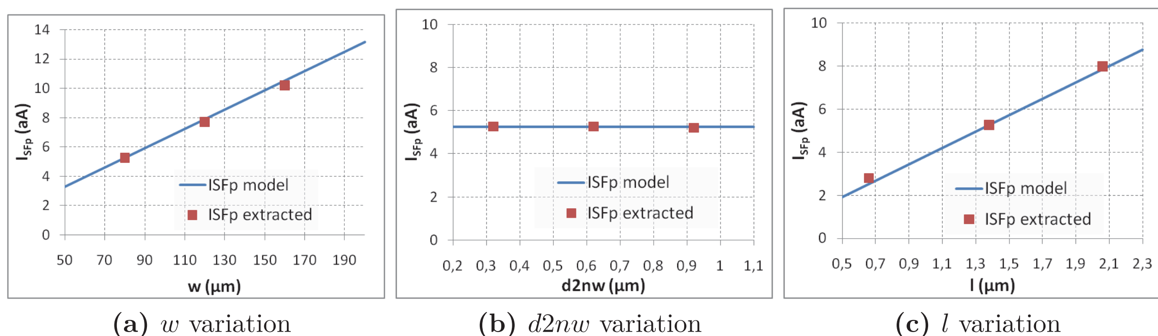
The exact values of the extracted parameters are given in Tab. 3.2 and Tab. 3.3.

Note that for the reference dimensions $w = 80\,\mu m$, $d2nw = 0.31\,\mu m$ and $l = 1.38\,\mu m$, the values are identical. This is normal, as they correspond to the device used for extracting the scaling parameters.



(a) w variation **(b)** $d2nw$ variation **(c)** l variation

Figure 3.7: I_{SFn} scaling law validation



(a) w variation **(b)** $d2nw$ variation **(c)** l variation

Figure 3.8: I_{SFp} scaling law validation

These four parameters, I_{Sn}, I_{Sp}, I_{SFn}, I_{SFp}, are important for two reasons. First, they stand at the core of the current flow, making them extremely important for the capability of the model to predict the SCR's behaviour. On the other hand, they can be accurately extracted, without the help of a linear regression or optimization. Thus, they are used to extract the scalability parameters γ_n, γ_p and N_{γ_p} and validate the proposed scaling paradigm. The accuracy of the prediction of I_{Sn} and I_{Sp} is a proof that the equivalent base width approximation is consistent with the actual physical phenomena.

The other parameters cannot be individually extracted as accurately as the formers. The steps carried out in order to obtain them are:

- full extraction and optimization of all the parameters for SCR1
- first approximation of the parameters for different structures using the scaling laws and the normalized parameters obtained from SCR1 (the scaling parameters γ were previously obtained from I_{Sn}, I_{Sp} and I_{Spsub})
- inspection of the characteristic containing the influence of a certain parameter; the respective characteristic should fit the measurement for each of the devices
- if the characteristic does not fit, the normalized parameter should be adjusted in order to obtain the best result across the devices

device	variation	I_{Sn} (aA) extraction	I_{Sn} (aA) model	I_{Sp} (aA) extraction	I_{Sp} (aA) model
SCR1	reference	19.5	19.5	3.9	3.9
SCR2	w	28.8	29.25	5.8	5.85
SCR3	w	38	39	7.8	7.8
SCR4	d2nw	19	19.5	2.5	2.58
SCR5	d2nw	18.75	19.5	1.85	1.88
SCR6	l	12.5	12.58	3.6	3
SCR7	l	23	22.51	4.3	4.1

Table 3.2: I_{Sn} and I_{Sp} scalable model vs. extracted parameters

device	variation	I_{SFn} (aA) extraction	I_{SFn} (aA) model	I_{SFp} (aA) extraction	I_{SFp} (aA) model
SCR1	reference	4.36	4.36	5.26	5.26
SCR2	w	6.2	6.54	7.7	7.89
SCR3	w	8.6	7.82	10.2	10.52
SCR4	d2nw	4.4	4.36	5.26	5.26
SCR5	d2nw	4.3	4.36	5.2	5.26
SCR6	l	2.5	2.08	2.8	2.51
SCR7	l	6.5	6.63	8	8

Table 3.3: I_{SFn} and I_{SFp} scalable model vs. extracted parameters

One first consequence of this approach is the reduced time in extracting and optimizing the parameters of each individual device

A full validation can only be done by inspecting the overall capability of the model to predict the SCR behaviour. This will be done in sec. 3.3.2, by comparing I-V triggering characteristics of each SCR with the scalable model's prediction.

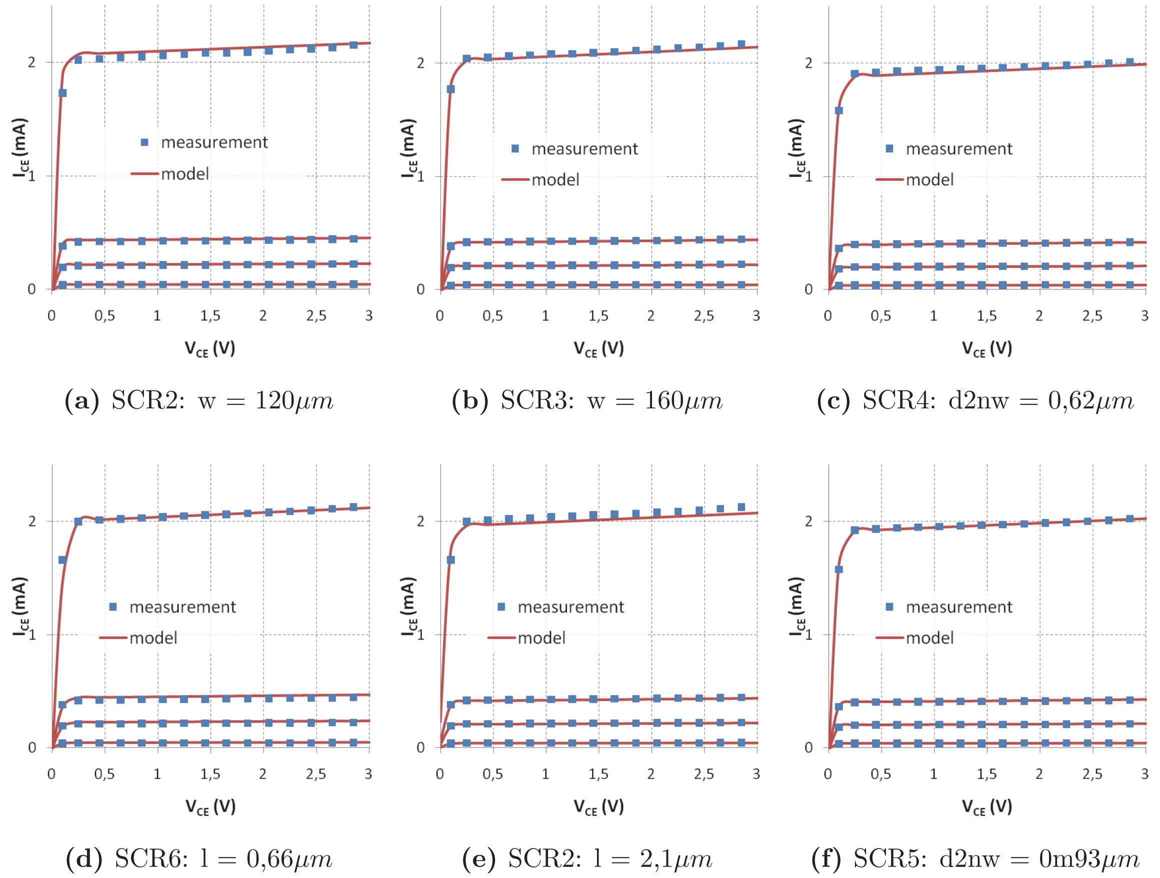
An important parameter obtained in such a way is the knee current. The normalized parameters, obtained from the reference SCR, are:

$$J^w_{KFp} = \frac{I_{KFn} \cdot \left(\sqrt{(\gamma_n \cdot l)^2 + \Delta d_w^2} + \Delta d_d\right)}{l \cdot w} \tag{3.53}$$

$$J^w_{KFp} = \frac{I_{KFp} \cdot \left(\sqrt{(\gamma_p \cdot l + 2 \cdot d2nw)^{N_{\gamma p}} + \Delta d_w^2} + \Delta d_d\right)}{l \cdot w} \tag{3.54}$$

The knee current, as presented in Chapter 2 is fitted on the output plot. Fig. 3.9 shows how the values obtained by using 3.13 fit the respective curves of all the SCRs

analysed, validating the proposed scaling law. Note that the scaling parameter γ_n was already extracted from the geometric variation of I_{Sn}.



(a) SCR2: w = 120μm **(b)** SCR3: w = 160μm **(c)** SCR4: d2nw = 0,62μm

(d) SCR6: l = 0,66μm **(e)** SCR2: l = 2,1μm **(f)** SCR5: d2nw = 0m93μm

Figure 3.9: Scalable fit of the npn's knee current, I_{KFn}

All the remaining current-related parameters are treated in the same manner.

Resistances

The normalized parameters for R_A, R_C, R_{CMn}, R_{CMp} and R_{Cpsub} are extracted using the technique described above. A final optimization among the values of different geometries can be done in order to minimize the effect of the extraction errors.

The normalized parameters for R_{CTn}, R_{CTp}, R_{Bn} and R_{Bp} need multiple geometries in order to be extracted. After all their nominal values for each geometry are being extracted, an optimization is done across all the geometries, targeting the minimum error between the extracted nominal value and the one obtained with 3.35, 3.36, 3.37 and 3.38, respectively.

Capacitances

The capacitances formed in an SCR structure are classic junction capacitances, characteristic to a considered CMOS process. In a general way, they are divided into a perimeter-dependent part and a surface-dependent one. They are extracted in a device-independent manner, by designing junctions of different areas and perimeters.

This model is made to be integrated in the development kit associated with a certain technology/process. The capacitance extraction part was not covered during the research, as no SCR-specific measurements were needed. For the devices presented here, the scaling parameters were already available.

Transit times

The transit time related normalized parameters, T_{Fn0}, T_{Fp0} and T_{R0}, are extracted from the reference geometry. Then, they are used in 3.44, 3.45 and 3.46, respectively, in order to obtain the nominal values for the other geometries. These values are used in order to simulate the device in a time domain way, as shown in Fig. 3.13, Fig. 3.14 and Fig. 3.15. A further optimization of each individual nominal value can be done on these curves, followed by an optimization of the scaling parameter in order to minimize the scaling law's error.

Note

Two approaches on the scalable parameters extraction were presented.

First approach implied the individual extraction of the nominal parameters for all the geometries. Using these values, the normalized and other scaling parameters were obtained by minimizing the error on the scaling law. This approach is used when (a) the nominal parameters can be individually extracted with good precision and (b) the scaling law has other fit parameters that needed to be extracted and a single geometry can't provide enough information; this kind of laws were used especially when they had to provide accurate values, as the parameters described by them are important for the whole behaviour of the SCR. A strong point of the developed model is that the parameters having the (b) requirement also fulfil the (a) condition.

The second approach implied the extraction of the nominal parameter for the reference geometry. The parameters for the other geometries were obtained using the scaling law and then verified on the curves that they affect on each of the devices. An optimization across their values was finally done in order to harmonize them. This approach is used when the nominal parameters can't be extracted with sufficient accuracy.

3.3.2 Overall scaling validation

VF-TCS measurements [Mano'07] were performed for each device, using a 50Ω resistance connected to the NW in order to simulate the triggering, as described in Chapter 2.

Simulations using the scalable model were then compared with the measurements in order to check the accuracy of the model and do a global parameter optimization.

Quasi-static characteristic

The quasi-static characteristic offers some of the most important information on the SCR, like the triggering voltage and current, holding voltage and post-triggering resistance slope. Fig. 3.10, Fig. 3.11 and Fig. 3.12 show it for "w", "d2nw" and, "l" variations, respectively.

In each case, the scalable model describes well the behaviour of different SCRs, being able to predict with sufficient accuracy the value of important parameters like the triggering and the holding voltage.

Time domain characteristic

Temporal characteristics were obtained under a 50 V pulse. This is a post triggering voltage, when most of the model's components are active. Fig. 3.13, Fig. 3.14 and Fig. 3.15 show it for "w", "d2nw" and, "l" variations, respectively.

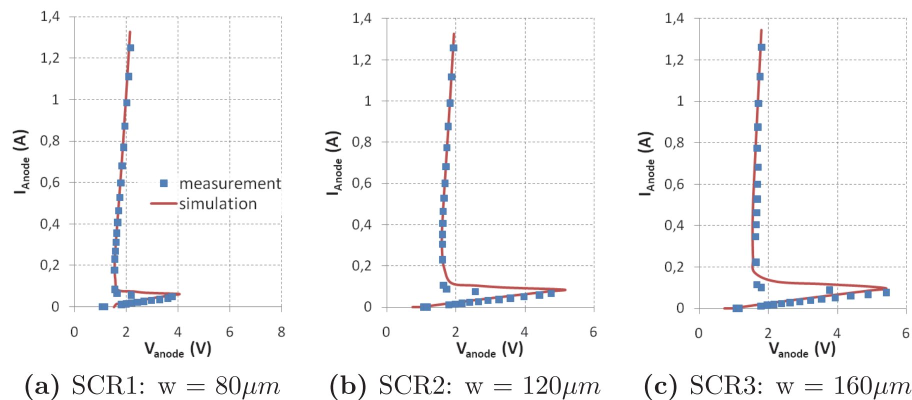
Over-shoot characteristic

The overshoot prediction also relies highly on the transient model. The peak values in transient characteristics taken at different pulse voltages are plotted. Fig. 3.16, Fig. 3.17 and Fig. 3.18 show it for "w", "d2nw" and, "l" variations, respectively.

The imprecision seen for the highest $d2nw$ value in Fig. 3.14 also translates in the inability of the model to predict the overshoot a high voltages in Fig. 3.17.

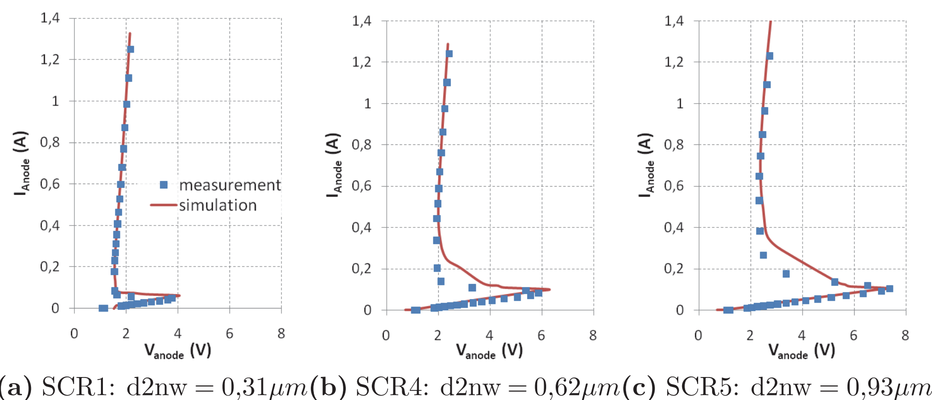
However, the results are good enough to validate the scalable model.

The w variation is almost perfect, the scaling laws here being simple and trivial. On the other hand, for high values of $d2nw$ and l, the model is less precise, showing its limits. Nevertheless, the geometries tested here as upper boundaries of these values are very unlikely to be used in protecting environments. A high l is inefficient, as the the SCRs level of protection does not increase linearly with it (explained by the inhomogeneity in the current density - see Fig. 3.2). A high $d2nw$ leads to considerably higher transit times and, thus, a much larger overshoot (the SCR turns on slower in time), being dangerous for the protected devices.



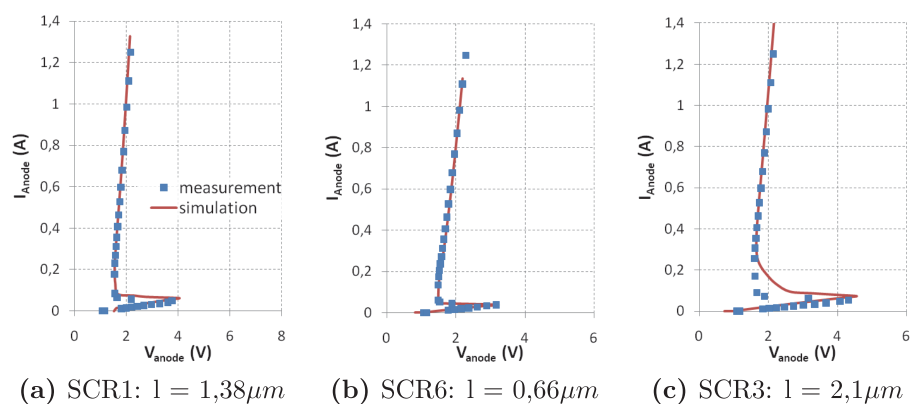
(a) SCR1: w = 80μm **(b)** SCR2: w = 120μm **(c)** SCR3: w = 160μm

Figure 3.10: Quasi-static characteristic for the w variation (vfTCS, 9 ns pulse width, 50 Ω on the NW)



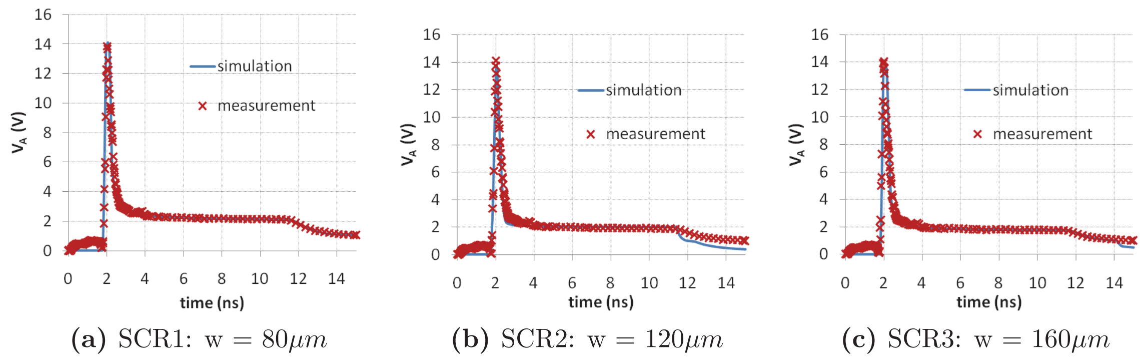
(a) SCR1: d2nw = 0,31μm **(b)** SCR4: d2nw = 0,62μm **(c)** SCR5: d2nw = 0,93μm

Figure 3.11: Quasi-static characteristic for the $d2nw$ variation (vfTCS, 9 ns pulse width, 50 Ω on the NW)



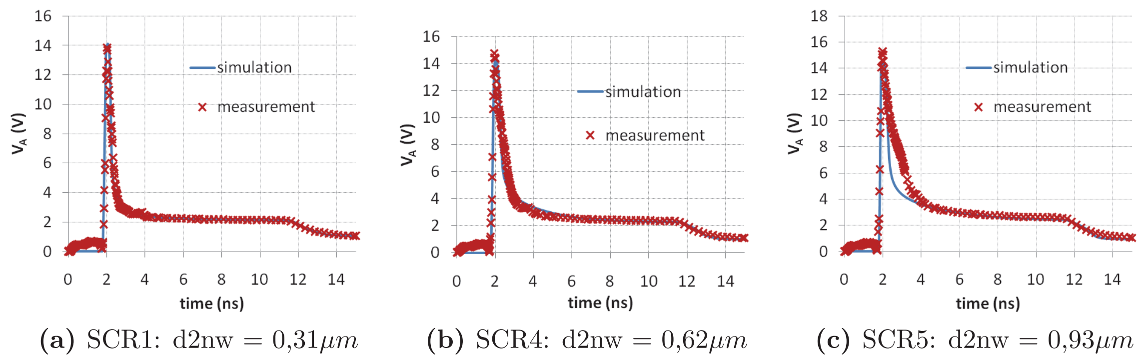
(a) SCR1: l = 1,38μm **(b)** SCR6: l = 0,66μm **(c)** SCR3: l = 2,1μm

Figure 3.12: Quasi-static characteristic for the l variation (vfTCS, 9 ns pulse width, 50 Ω on the NW)



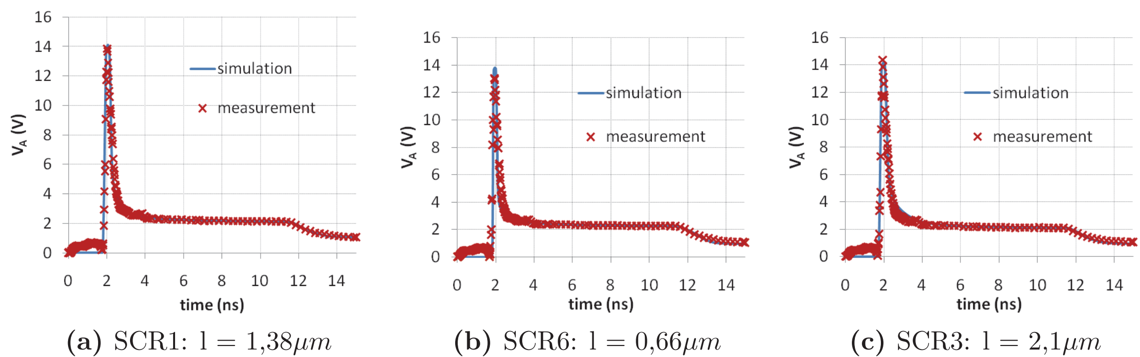
(a) SCR1: w = 80μm **(b)** SCR2: w = 120μm **(c)** SCR3: w = 160μm

Figure 3.13: Temporal characteristic for the w variation (vfTCS, 9 ns pulse width, 50 Ω on the NW, 50V)



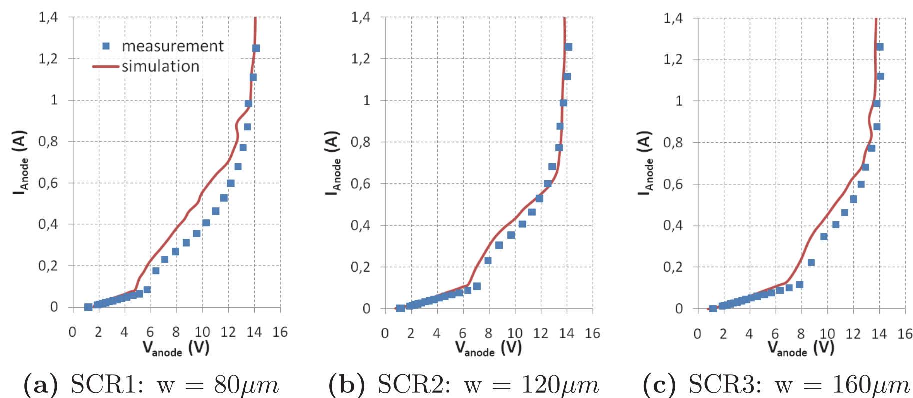
(a) SCR1: d2nw = 0,31μm **(b)** SCR4: d2nw = 0,62μm **(c)** SCR5: d2nw = 0,93μm

Figure 3.14: Temporal characteristic for the $d2nw$ variation (vfTCS, 9 ns pulse width, 50 Ω on the NW, 50V)



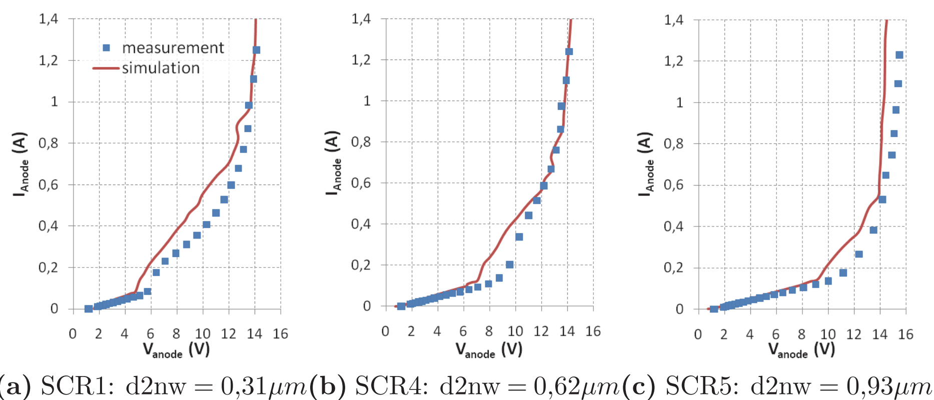
(a) SCR1: l = 1,38μm **(b)** SCR6: l = 0,66μm **(c)** SCR3: l = 2,1μm

Figure 3.15: Temporal characteristic for the l variation (vfTCS, 9 ns pulse width)



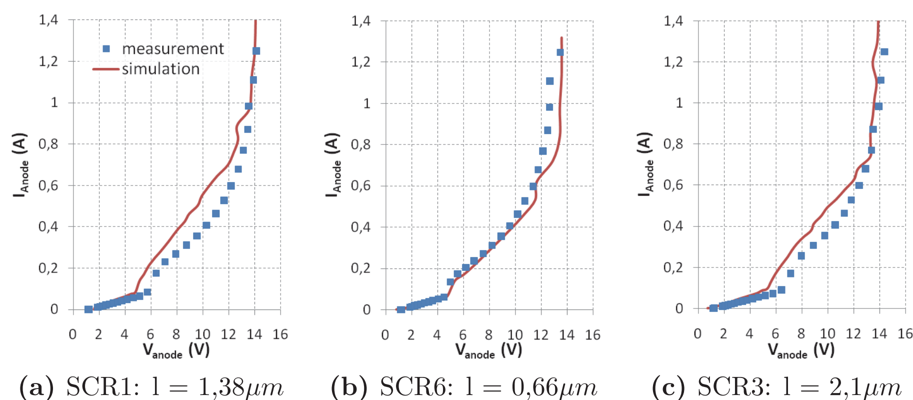
(a) SCR1: w = 80μm **(b)** SCR2: w = 120μm **(c)** SCR3: w = 160μm

Figure 3.16: Over-shoot characteristic for the w variation (vfTCS, 9 ns pulse width, 50 Ω on the NW)



(a) SCR1: d2nw = 0,31μm **(b)** SCR4: d2nw = 0,62μm **(c)** SCR5: d2nw = 0,93μm

Figure 3.17: Overshoot characteristic for the $d2nw$ variation (vfTCS, 9 ns pulse width, 50 Ω on the NW)



(a) SCR1: l = 1,38μm **(b)** SCR6: l = 0,66μm **(c)** SCR3: l = 2,1μm

Figure 3.18: Over-shoot characteristic for the l variation (vfTCS, 9 ns pulse width, 50 Ω on the NW)

3.4 Conclusion

A scalable model for the SCR ESD protection device was presented in this chapter. It describes the behaviour of an SCR as function of three variable dimensions: the width (“w”) and the length (“l”) of the anode and cathode, and the distance between them (“$d2nw$”). These are the most useful parameters from an ESD-protection SCR point of view

The scaling laws are based on the bipolar junction transistor ones, adapted to the geometrical particularities of the SCR. As the model keeps a close link with the physical phenomena, being as less empirical as possible, the scaling laws are very close to physically-based geometrical behaviour of currents and resistances. A new equivalent base width model was proposed, tailored on the ESD-protection SCR’s layout.

A sufficient number of devices were designed in order to develop the scaling laws and validate the model.

The equivalent base model was validated through accurate measurements of some of the parameters it affects: the transport model’s saturation currents of the SCR’s bipolar parts.

The good fit of the plots shows that the time domain, quasi-static and over-shoot characteristics of the SCR can be well predicted versus the proposed geometrical variations.

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4 RF Model

4.1 ESD RF co design problematic

Apart from the direct cost of using ESD protection devices, given by the extra surface they occupy on the silicon, there is also a functional cost: their influence on the protected circuit [Gong'02]. At microwave frequencies, this influence can significantly impact the functioning of the latter. Until now, the parasitic introduced was usually reduced to a capacitance [Chen'04, Yuan'05, Lin'10]. As the frequencies get higher and the demand for precision increases, these approximations become incomplete.

This chapter will investigate the influence the SCR ESD protection device has on the protected circuit at high frequencies. As the SCR is never used as it is, but in conjunction with other devices, most notably diodes, these were also analysed. The purpose of this investigation is the creation of complete models for both the diode and the SCR. The proposed models are meant to help the RF designers build better input stages and evaluate the overall performance of their circuit, after the inclusion of the indispensable ESD protection.

In order to model complex devices, a network of resistance and capacitance that is closer to their physics has to be considered.

The backend (metal layers) plays an important role in the ESD performance. Thus, not all the routing should be left under layout-efficiency laws; bottom metal levels should be considered part of the device and, in consequence, part of the model.

The ESD protection may often be found under a voltage bias - Fig. 4.1. Being made out of pn junctions (like the SCR or the diodes are), some of their inner capacitances change depending on the bias these devices might be under; thus the need of distinguishing between metal (non voltage dependent) and junction (voltage dependent) capacitances.

A voltage dependent model for the SCR and the diode was first developed, covering the behaviour of the two devices up to 65GHz. Then, in order to prove their consistency, the models were tested on a complete protection structure made of an SCR, three diodes that make the triggering circuit for the SCR and a diode for reverse protection. Experimental results that confirm their validity and the voltage dependent variation of different parameters are shown in sec. 4.5.

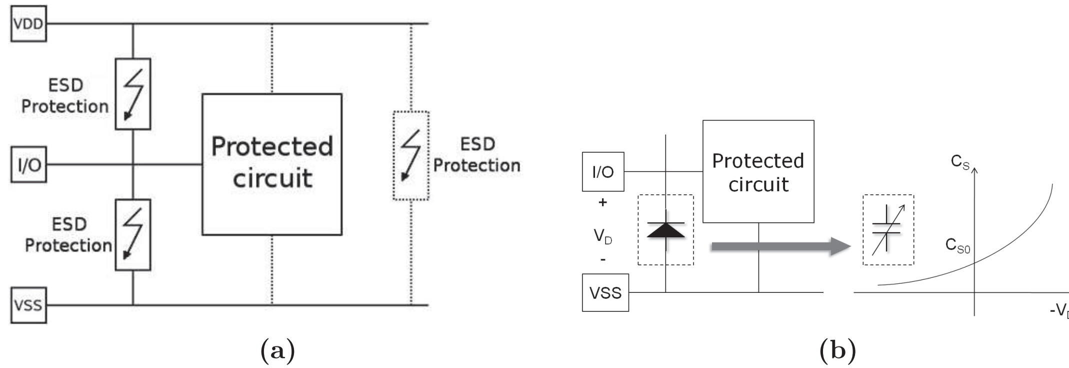


Figure 4.1: ESD protection devices in a circuit; bias dependent influence on the protected circuit

4.2 Devices description

The target of our study is the DTSCR (Diode Triggered SCR), an SCR-based complete protection structure. It is made out of an SCR having a chain of three diodes connected on its NW, acting as a triggering circuit (sec. 1.3.2). This is a unidirectional protection. In order to make it a bidirectional one, it is completed with an ESD protection diode (Fig. 4.2).

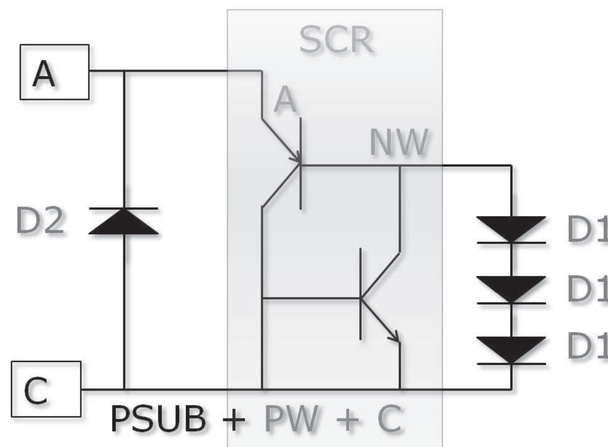


Figure 4.2: DTSCR schematic

Four structures were analysed:

- a protection diode
- a triggering diode
- an SCR
- a DTSCR

4.2.1 Protection diode

The protection diode, D2 in Fig. 4.2, is a N+PW device, with its anode made of the p-well and its cathode made of an n+ diffusion (Fig. 4.3).

It is a large device, its surface being tailored to resist a certain ESD event.

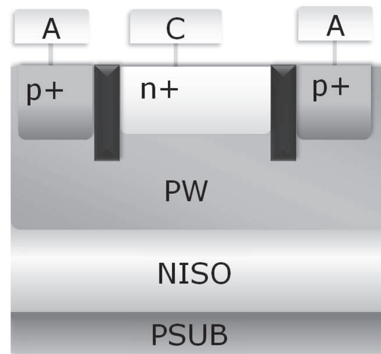


Figure 4.3: Protection diode layout

4.2.2 Triggering diode

The triggering diode, D1 in Fig. 4.2 is a P+NW device, with its anode made of a p+ diffusion and its cathode made of the n-well (Fig. 4.4).

It is part of the triggering circuit, made out of three identical D1 diodes. It is a small device, needing to drive ESD energy only before the SCR turns on.

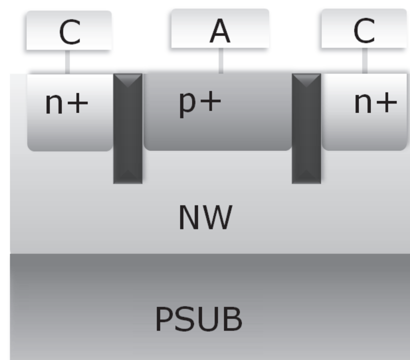


Figure 4.4: Triggering diode layout

4.2.3 SCR

The SCR considered for this investigation is the classic multi-finger device described and analysed from an ESD point of view in Chapter 2 and Chapter 3. It is the

reference device (SCR1) from Chapter 3.

4.2.4 DTSCR

A DTSCR [Merg'03] structure, as shown in Fig. 4.2 was also realized, with the purpose of seeing if the models built and extracted for the individual devices are able to predict its behaviour.

4.3 Devices modelling

In normal circuit operating conditions, the ESD protection devices can be seen as passive components. They are designed in such a way that they be transparent for the protected circuit. The voltage drops across them is always small enough so that they remain in a high impedance state. The probability that these devices answer to an ESD event and turn on is very small during the lifetime of a product. This usually happens during the manufacturing process. Thus, it is of no interest of modelling their high-frequency impact as active devices.

The proposed models are built by taking into account the:

- junction capacitances and dynamic resistances
- well resistances
- backend resistances, inductances and capacitances
- substrate capacitance and resistance

4.3.1 Diodes

The electrical model proposed for a p+nw diode is presented in Fig. 4.5, alongside its physical basis.

Its elements are:

- Junction related:

- C_S - diode's central junction capacitance
- R_{ON} - dynamic ON resistance

- well resistances

- R_S - the NW resistance

- substrate related

- C_{sub} - the NW-PSUB capacitance
- R_{sub} - substrate resistance

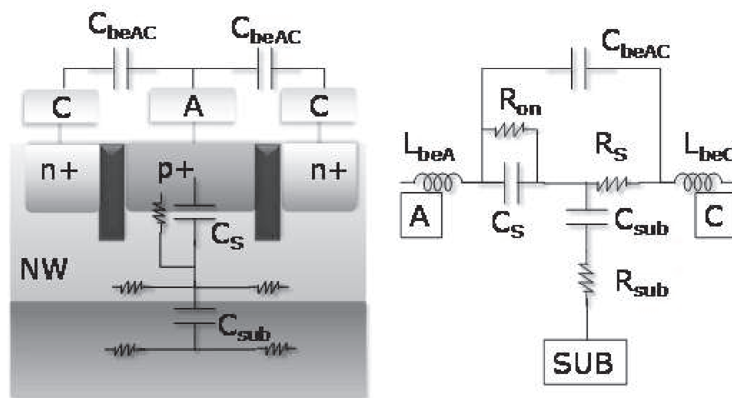


Figure 4.5: RF model for the ESD protection diode

- backend related

- C_{beAC} - the capacitance between the metal lines of the anode and the cathode
- L_{beA} - inductance of the metal line used to access the anode
- L_{beC} - inductance of the metal line used to access the cathode

C_S and C_{sub} are modelled through their depletion capacitance:

$$C_S = \frac{C_{S0}}{\left(1 - \frac{V_D}{V_{JS}}\right)^{m_{js}}} \tag{4.1}$$

$$C_{sub} = \frac{C_{sub0}}{\left(1 - \frac{V_{sub}}{V_{Jsub}}\right)^{m_{jsub}}} \tag{4.2}$$

Where:

- C_{S0} and C_{sub0} are the junctions capacitance at 0 V (no bias);
- V_{JS} and V_{Jsub} are the junctions built-in voltages;
- m_{js} and m_{jsub} are the junctions coefficients;
- V_D and V_{sub} are the voltage drops on the central junction and the substrate junction, respectively.

The purpose not being to model the ESD conduction, but the device impact over the circuit, we can assume that the current flowing through the diode is insignificant outside an ESD event. Thus, the diffusion capacitance, given by the charges transiting the junction, becomes negligible.

Although when used as stand-alone protections the diodes are reverse-biased, they can get forward-biased when part of a more complex structure, as the DTSCR. In this case, the junction allows a certain current to pass through it. This is modelled through a bias-dependent (dynamic) resistance:

$$R_{ON} = R_{ON_{hc}} + \frac{V_D}{I_S \exp \frac{V_D}{V_T}} \tag{4.3}$$

Where:

- $R_{ON_{hc}}$ is the value of R_{ON} at high bias levels - when the diode is in passing state
- I_S is the junction saturation current
- V_T is the thermal voltage, $26\,mV$ at a temperature of $300\,K$
- V_D is the voltage drop on the central junction

The model for the n+pw diode (Fig. 4.3) is identical. C_{sub} will take the role of the p-well - n-iso junction.

4.3.2 SCR

The electrical model proposed for an ESD protection SCR is presented in Fig. 4.6, alongside its physical basis.

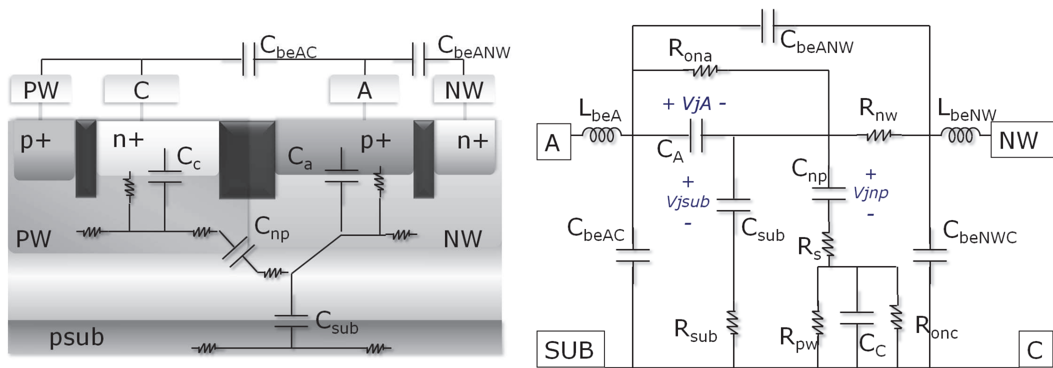


Figure 4.6: RF model for the ESD protection SCR

Its elements are:

- Junction related:

- C_A - the anode to n-well (A-NW) junction capacitance
- R_{onA} - dynamic ON resistance of the A-NW junction
- C_C - the cathode to p-well (C-PW) junction capacitance

- R_{onC} - dynamic ON resistance of the C-PW junction
- C_{np} - the n-well - p-well (NW-PW), central junction capacitance
- R_S - the distribution of the well resistances towards the substrate

- well resistances

- R_{nw} - the NW resistance
- R_{pw} - the PW resistance

- substrate related

- C_{sub} - NW-PSUB capacitance
- R_{sub} - substrate resistance

- backend related

- C_{beAC} - The capacitance between the metal lines of the anode (A) and the cathode (C)
- C_{beANW} - The capacitance between the metal lines of the anode (A) and the n-well (NW)
- C_{beNWC} - The capacitance between the metal lines of the n-well (NW) and the cathode (C)
- L_{beA} - inductance of the metal line used to access the anode
- L_{beNW} - inductance of the metal line used to access the n-well

The central junction, between the NW and the PW, whose capacitance is modelled by C_{np}, is always reverse-biased. Thus, there is no need for a dynamic resistance to model the conduction through it.

For the junction capacitances, a depletion model, similar to 4.1, was used:

$$C_A = \frac{C_{A0}}{\left(1 - \frac{V_A}{V_{JSA}}\right)^{m_{jA}}} \tag{4.4}$$

$$C_C = \frac{C_{C0}}{\left(1 - \frac{V_C}{V_{JSC}}\right)^{m_{jC}}} \tag{4.5}$$

$$C_{np} = \frac{C_{np0}}{\left(1 - \frac{V_{np}}{V_{JSnp}}\right)^{m_{jnp}}} \tag{4.6}$$

and for the R_{ON} resistances, one similar to 4.3:

$$R_{ON_A} = R_{ON_{Ahc}} + \frac{V_A}{I_{S_A} \exp \frac{V_A}{V_T}} \tag{4.7}$$

$$R_{ON_C} = R_{ON_{Chc}} + \frac{V_C}{I_{S_C} \exp \frac{V_C}{V_T}} \tag{4.8}$$

4.4 S-parameters characterization

The devices were realized in a 130 nm BiCMOS MW (Microwave) technology. S-parameter measurements were carried out directly on the wafer using a Cascade characterization bank and a VNA (Vector Network Analyser) up to 65 GHz. DC bias was applied in order to build the voltage dependent model.

No special procedures were involved. A classic Cascade-specific LRRM calibration [Davi'90] was used.

All the devices were prepared in RF measurement pad frames (Fig. 4.7), in the configurations presented next.

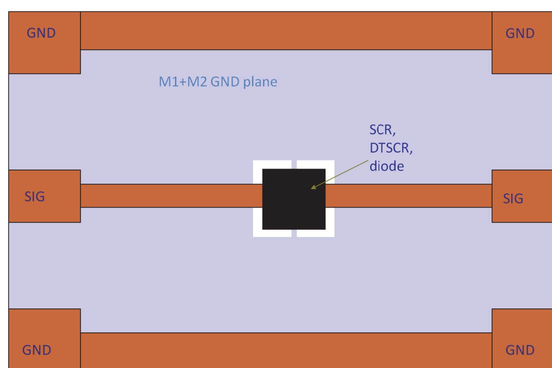


Figure 4.7: Measurement structure

The choice of measurement configurations was given by:

- The need of sufficient information in order to build and extract a model for a certain device
- The limited silicon surface available for this study

4.4.1 Diodes characterization

For the diodes, two configurations were used: "parallel" and "cascade". In the parallel configuration (Fig. 4.8) the diode has its anode connected to the signal (S) and the cathode connected to the ground (GND), together with the substrate (PSUB). This will offer an overall image of the diode and of the non de-embedded parasitic. Different voltages were applied to the S pads in order to bias the device.

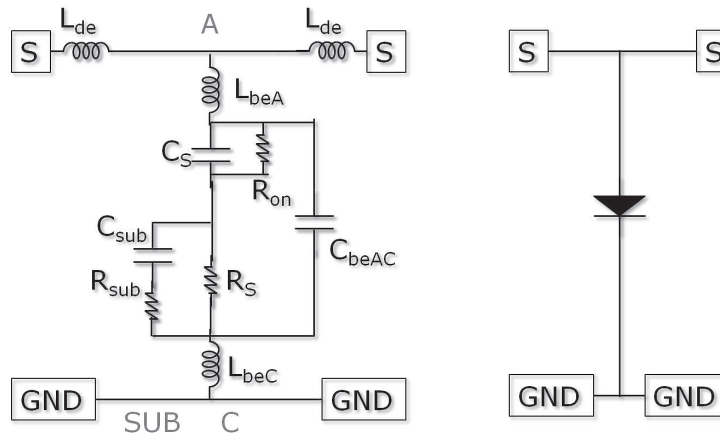


Figure 4.8: Diode parallel characterization configuration

In the cascade configuration (Fig. 4.9), the anode is connected to one signal (S1) and the cathode to another one (S2). This configuration will offer, besides a supplemental information on the diode's junction, a detailed look on the substrate parasitic effects. Different voltages were applied between the S1 and the S2 pads in order to bias the device.

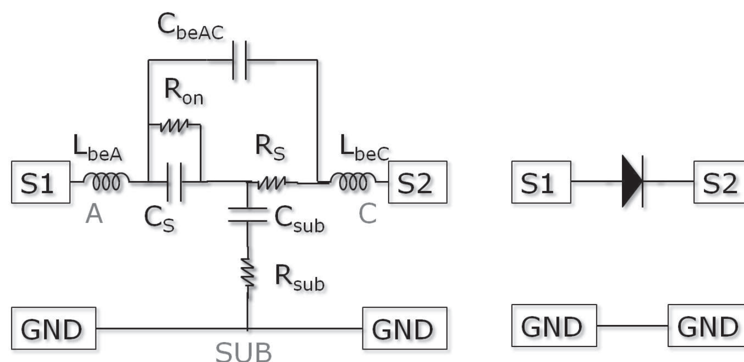


Figure 4.9: Diode cascade characterization configuration

4.4.2 SCR characterization

The SCR was measured in only one configuration (Fig. 4.10). It was chosen in such a way that the information at the important spots be maximal. It is the case of the NW pad, where a triggering circuit is going to be connected (Fig. 4.2).

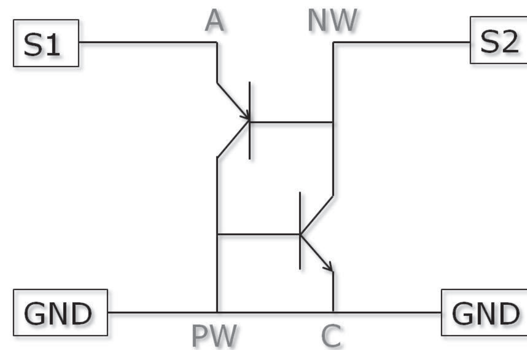


Figure 4.10: SCR characterization configuration

The related parameters of the further developed model, between the anode (A) and NW (which will be continued with a chain of diodes in a complete protection structure), have to be extracted with a good precision. Thus, A is connected to one signal (S1), NW to another one (S2) and the cathode (C), PW and the substrate are connected to the ground (GND). This configuration offers a detailed look on the anode - NW part, as well as an overall look on the "body" of the device.

Different voltages were applied to the S1 pad in order to bias the device.

4.4.3 DTSCR characterization

The DTSCR was measured in the configuration shown in Fig. 4.11. The bias was applied to S1.

4.4.4 De-embedding structures

The measurement results have to be de-embedded in order to eliminate the parasitic introduced by the auxiliary measurement structure present on the silicon. That is, the reference planes have to be "moved" through a data processing at the boundary of the actual analysed device. In order to obtain the information necessary to de-embed, several special structures, containing only the measurement pad frames in different configurations, were designed.

An important aspect is how much should be de-embedded. Where does the useful information about the structure end?

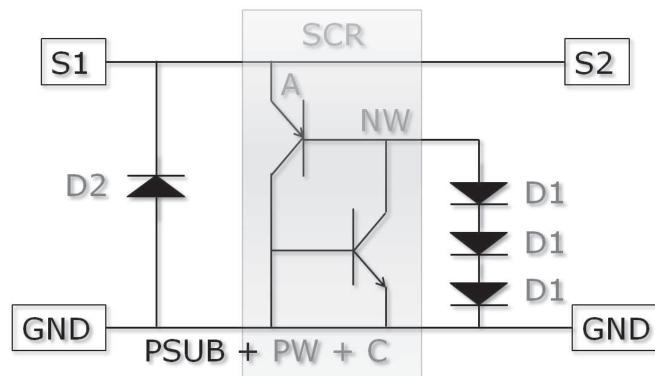


Figure 4.11: DTSCR characterization configuration

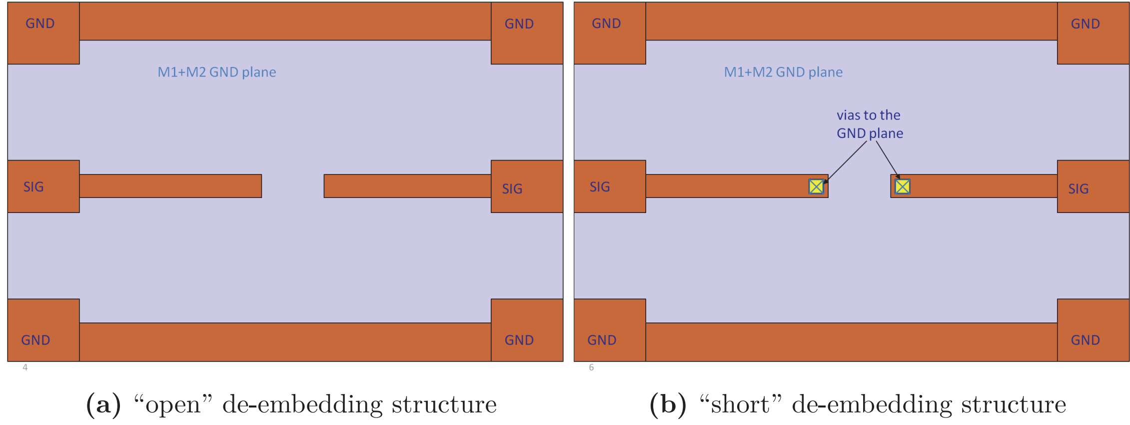
From a modelling point of view, the easiest way to extract the parameters would have been to de-embed all the way down to the silicon level (the frontend), excluding all the metal layers (the backend). However, this work was intended as an overall study on the RF behaviour of the ESD protection devices.

Moreover, the related scientific literature is very limited in experiments and information in this area. One of the purposes of this study was also the analysis of the particularities present in the high frequency characterization of ESD protection devices. These particularities are mostly due to their size, bigger than usual functional devices in a certain technology, and the special layout of the backend.

The metal layers play a significant role in the ESD performance of a certain structure. Up to a certain level they have to be considered as part of the device. Thus, although it makes the parameter extraction more difficult, the de-embedding was done above these metal layers. As consequence, the characterisation offers a better image on the overall high frequency behaviour. Another consequence of this choice was the fact that a single set of de-embedding structures can be used with multiple devices and configurations.

The set was made out of two structures, an open (Figure 4.12a) and a short (Figure 4.12b), according to the needs of the chosen de-embedding method [Torr'05]. The algorithm in [Torr'05] was implemented in MATLAB using the RF Toolbox [MAT'11].

The “open” structure has an open circuit between the two signal pads and also between each signal pad and the ground plane. The “short” structure has each pad short-circuited to the ground plane through a chain of vias. In some measurement configurations, the diode parallel (Fig. 4.8) and the DTSCR (Fig. 4.11), the two signal pads are interconnected. It will be shown in sec. 4.5 how the error introduced by the strip connecting the two pads in this case can be estimated and isolated.



(a) "open" de-embedding structure **(b)** "short" de-embedding structure

Figure 4.12: De-embedding structures

4.5 Parameter extraction and model validation

Advanced Design System [ADS'08] design automation software from Agilent was used for data analysis and parameter extraction.

The measured S parameters are first transformed into Z parameters. This is done in order to give them a physical sense, related to the proposed model, made out of passive elements. Thus, the [S] matrix is transformed in a [Z] matrix.

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{12} & S_{21} \end{bmatrix} \longrightarrow \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{21} \end{bmatrix} \tag{4.9}$$

where:

$$Z_{11} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{\Delta S} \cdot Z_0 \tag{4.10}$$

$$Z_{12} = \frac{2S_{12}}{\Delta S} \cdot Z_0 \tag{4.11}$$

$$Z_{21} = \frac{2S_{21}}{\Delta S} \cdot Z_0 \tag{4.12}$$

$$Z_{22} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{\Delta S} \cdot Z_0 \tag{4.13}$$

$$\Delta S = (1 - S_{11})(1 - S_{22}) - S_{12}S_{21} \tag{4.14}$$

Given the arrangement of the different branches in all of the three cases (Fig. 4.8, Fig. 4.9 and Fig. 4.10) used for the parameter extraction, the information obtained from the measurements was grouped in a T-configuration (Fig. 4.13).

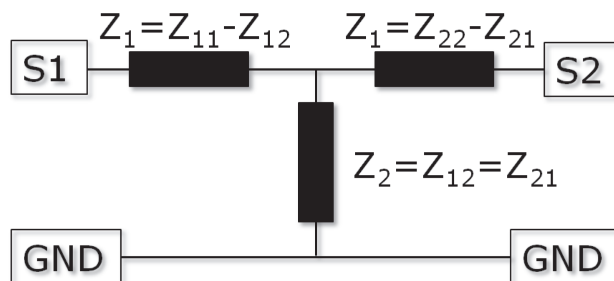


Figure 4.13: T-model used to compare the impedance distribution of the models with the measurements

The following methodology was used for obtaining the parameters of the models:

- whenever needed, converting the model schematic to a T-configuration; this is particularly the case with the diode in cascade, Fig. 4.9; the anode-cathode backend capacitance, C_{beAC}, has to be introduced in the other branches through a delta-star transformation;
- obtaining the equivalent impedance for each of the branches of a model and simplifying whenever possible by taking into account the usual magnitudes of the parameters involved;
- comparing the frequency-dependent model equation of each equivalent impedance with the one obtained from the measurements.

Various ways of obtaining the parameters from the measured curves is shown next for each of the devices and configurations.

4.5.1 Diode parameter extraction

As stated above, two configurations were available for extracting the diode's model parameters. The parallel one is mostly used, as it better represents the diode in its usual position as a protection or triggering device. Nevertheless, the substrate is hard to be separated from the other parameters. The cascade configuration (Fig. 4.9) is used to accomplish this task.

Cascade configuration

The model has to be brought to a T-configuration by a delta-star transformation around C_{beAC}. Thus, the model in Fig. 4.9 becomes as in Fig. 4.14.

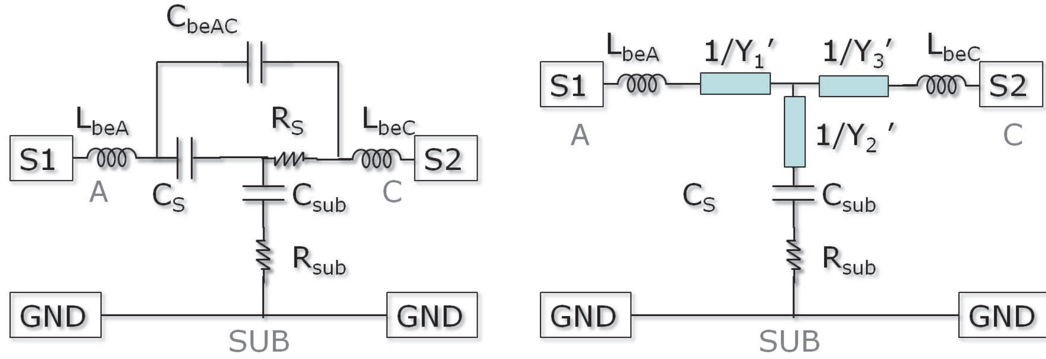


Figure 4.14: Diode model after being converted to a T-configuration

Where:

$$Y_1' = j\omega\left(C_{met} + C_s\right) - R_s\omega^2 C_s C_{met} \tag{4.15}$$

$$Y_2' = j\omega C_s + \frac{1}{R_s} + \frac{C_s}{R_s C_{met}} \tag{4.16}$$

$$Y_3' = j\omega C_{met} + \frac{1}{R_s} + \frac{C_{met}}{R_s C_s} \tag{4.17}$$

The substrate configuration is contained by the middle branch, Z_2 from Fig. 4.14:

$$Z_2 = \frac{1}{Y_2'} + R_{sub} + \frac{1}{j\omega C_{sub}} \tag{4.18}$$

$$\frac{1}{Y_2'} = \frac{1}{\frac{C_{met}+C_s}{R_s C_{met}} + j\omega C_s} = \frac{\frac{C_{met}+C_s}{R_s C_{met}} + j\omega C_s}{\frac{(C_{met}+C_s)^2}{R_s^2 C_{met}^2} + \omega^2 C_s^2} \tag{4.19}$$

Given the expected magnitudes of the parameters: $C_{met} \approx 10^{-14}\,F$, $C_s \approx 10^{-14}\,F$, $R_s \approx 10\,\Omega$, $\omega \approx 10^{10}\,Hz$, it can be concluded that

$$\underbrace{\frac{\left(\overbrace{C_{met}}^{10^{-14}} + \overbrace{C_s}^{10^{-14}}\right)^2}{\underbrace{R_s^2}_{10^2}\,\underbrace{C_{met}^2}_{10^{-28}}}}_{10^{-2}} \gg \underbrace{\underbrace{\omega^2}_{10^{20}}\,\underbrace{C_s^2}_{10^{-28}}}_{10^{-8}} \tag{4.20}$$

4.19 is introduced in 4.18 by using 4.20 and the real and imaginary parts are grouped together:

$$Z_2 = \frac{R_s C_{met}}{C_s + C_{met}} + R_{sub} + j\left(\omega C_s \cdot \frac{R_S^2 C_{met}^2}{(C_{met} + C_s)^2} - \frac{1}{\omega C_{sub}}\right) \tag{4.21}$$

Using the same approach as in 4.20, 4.21 can be further simplified by considering:

$$\underbrace{\underbrace{\omega C_s}_{10^{-4}} \cdot \underbrace{\frac{R_S^2 C_{met}^2}{(C_{met} + C_s)^2}}_{10^{2}}}_{10^{-2}} \ll \underbrace{\frac{1}{\omega C_{sub}}}_{10^{4}} \tag{4.22}$$

A simpler form of the real and imaginary parts is then obtained and can be exploited.

$$Re(Z_2) \simeq \frac{R_s C_{met}}{C_s + C_{met}} + R_{sub} \tag{4.23}$$

$$Im(Z_2) \simeq -\frac{1}{\omega C_{sub}} \tag{4.24}$$

4.23 contains in a inseparable way the effect of R_s, C_{met}, C_s and R_{sub}. Thus, no parameter can be directly extracted from it. On the other hand, 4.24 contains approximately only the effect of C_{sub}.

$$C_{sub} = -\frac{1}{\omega \cdot Im(Z_2)} \tag{4.25}$$

By plotting 4.25 from the measured data, C_{sub} can be easily obtained (Fig. 4.15).

For the device analysed in Fig. 4.15, $C_{sub} = 61\,fF$.

4.23 can be used after the extraction of R_s, C_{met}, C_s when R_{sub} can be obtained by fitting the $Re(Z_2)$ curve.

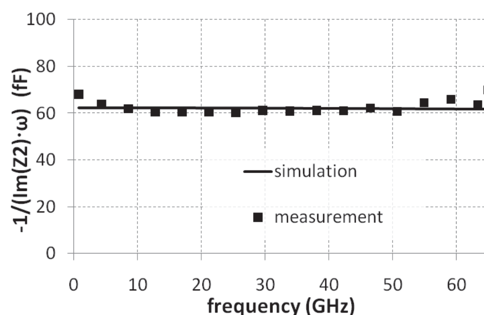


Figure 4.15: Substrate capacitance extraction for an ESD diode

Parallel configuration

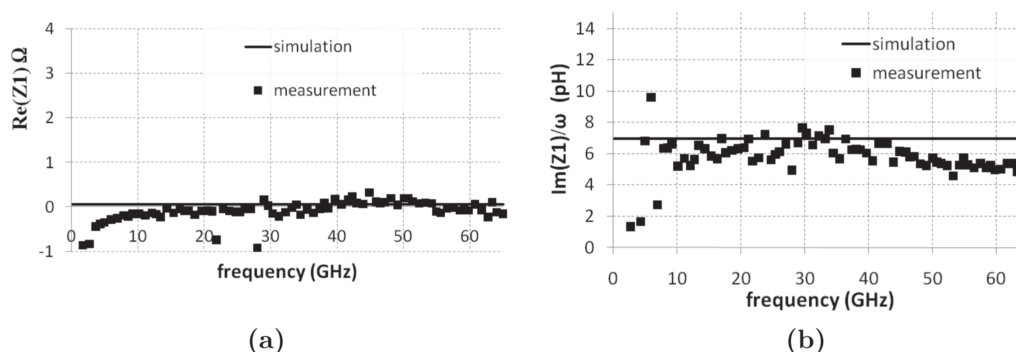
The other parameters (C_s, C_{beAC}, R_s, L_{beA}) are extracted directly or through optimization, using the parallel characterization setup (Fig. 4.8).

L_{de}, modelling the non de-embedded part of the feed line to the diode (part of the strip connecting the two signal pads), is extracted from Z_1:

$$Z_1 = j\omega L_{de} \tag{4.26}$$

$$L_{de} = \frac{Im(Z_1)}{\omega} \tag{4.27}$$

The real part of Z_1 represents the residual non de-embedded resistance. Fig. 4.16 shows in a quantitative way the elements that weren't able to be de-embedded using the de-embedding structures presented in sec. 4.4.4.



(a) (b)

Figure 4.16: Information contained in the Z_1 branch of the diode in a parallel measurement configuration

Z_2 contains the whole model. As with the previous configuration, a complete analysis of this impedance is done in order to see the impact each parameter has on the measured characteristics. Given the model composition, $Y_2 = \frac{1}{Z_2}$ was found to be easier to compute.

$$Y_2 = j\omega C_{met} + \left(j\omega C_s \parallel \left(\frac{1}{R_s} + \frac{1}{R_{sub}} \parallel j\omega C_{sub}\right)\right) \tag{4.28}$$

$$= j\omega C_{met} + \left(j\omega C_s \parallel \frac{1 + \omega^2 C_{sub}^2 R_{sub}\left(R_s + R_{sub}\right) + j\omega C_{sub} R_s}{R_s\left(1 + \omega^2 R_{sub}^2 C_{sub}^2\right)}\right) \tag{4.29}$$

Given the usual magnitude of the parameters, we can suppose that:

$$\underbrace{\underbrace{\omega^2}_{10^{20}} \underbrace{C_{sub}^2}_{10^{-28}} \underbrace{R_{sub}}_{10^{2}} \left(\underbrace{R_s + R_{sub}}_{10^{2}}\right)}_{10^{-4}} \ll 1 \tag{4.30}$$

$$\underbrace{\underbrace{\omega^2}_{10^{20}} \underbrace{R_{sub}^2}_{10^{4}} \underbrace{C_{sub}^2}_{10^{-28}}}_{10^{-4}} \ll 1 \tag{4.31}$$

Note that the previous simplification, valid at lower frequencies (ω was considered to be around $10\,GHz$), completely eliminates the dependency of Y_2 with R_{sub}.

$$Y_2 \simeq j\omega C_{met} + \left(j\omega C_s \parallel \frac{1 + j\omega C_{sub} R_s}{R_s}\right) \tag{4.32}$$

$$= \frac{\omega^2 R_s C_s^2 + j\omega\left(C_{met} + C_s\right) + j\omega^3 R_s C_s C_{sub}\left(C_s + C_{sub}\right)}{1 + \omega^2 R_s^2\left(C_s + C_{sub}\right)^2} \tag{4.33}$$

$$\underbrace{\underbrace{\omega^2}_{10^{20}} \underbrace{R_s^2}_{10^{4}} \underbrace{\left(C_s + C_{sub}\right)^2}_{10^{-28}}}_{10^{-4}} \ll 1 \tag{4.34}$$

$$Y_2 \simeq \omega^2 R_s C_s^2 + j\omega\left(C_{met} + C_s\right) + j\omega^3 R_s C_s C_{sub}\left(C_s + C_{sub}\right) \tag{4.35}$$

Finally, we obtained an approximation of the real and imaginary parts:

$$Re(Y_2) = \omega^2 R_s C_s^2 \tag{4.36}$$

$$Im(Y_2) = \omega \left(C_{met} + C_s\right) + \omega^3 R_s C_s C_{sub} \left(C_s + C_{sub}\right) \tag{4.37}$$

We can observe that at low frequencies, $Re(Y_2)$ gathers the influence of R_s and C_s:

$$R_s C_s^2 = \frac{Re(Y_2)}{\omega^2} \tag{4.38}$$

The characteristic associated with 4.38 is shown in Figure 4.17a. R_{sub} impacts it at high frequency, where the approximations in 4.30 and 4.31 do not stand.

From $Im(Y_2)$ we can obtain the sum of C_s and C_{met}. The latter has a more pronounced impact at high frequencies, given by the second term of 4.37. At lower frequencies, only the first term is visible:

$$\underbrace{\underbrace{\omega}_{10^{10}}\underbrace{(C_{met} + C_s)}_{10^{-14}}}_{10^{-4}} \gg \underbrace{\underbrace{\omega^3}_{10^{30}}\underbrace{R_s^2}_{10^4}\underbrace{C_s}_{10^{-14}}\underbrace{C_{sub}}_{10^{-14}}\underbrace{(C_s + C_{sub})}_{10^{-14}}}_{10^{-8}} \tag{4.39}$$

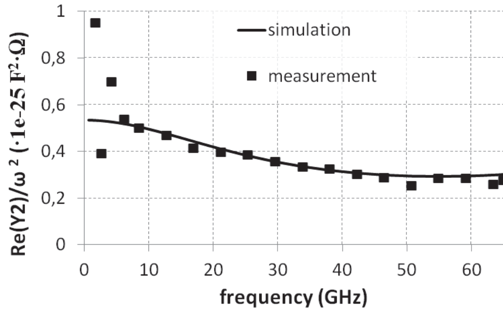
Thus, by using 4.39 in 4.37:

$$C_{met} + C_s = \frac{Im(Y_2)}{\omega} \tag{4.40}$$

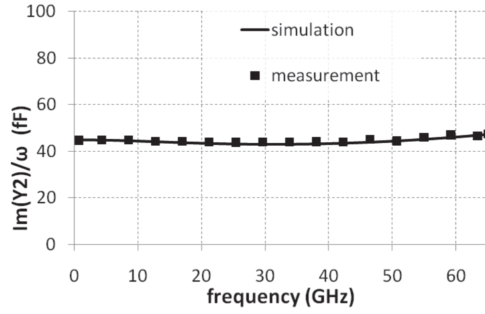
The characteristic associated with 4.40 is shown in Figure 4.17b. The backend impedance, L_{be} also impacts it at very high frequencies.

The following steps were used to obtain the parameters using the curves in Fig. 4.17:

- R_s and C_s are estimated from Figure 4.17a at low frequencies; as their impact differs slightly with the frequency, it is possible to separate them by targeting a good fit on the curve between 0 and $20\,GHz$.
- C_{met} is then calculated from 4.40 and the plot in Figure 4.17b.
- Having C_{sub} already extracted using the cascade configuration, R_{sub} is extracted by fitting Figure 4.17a at high frequencies or by using 4.23.

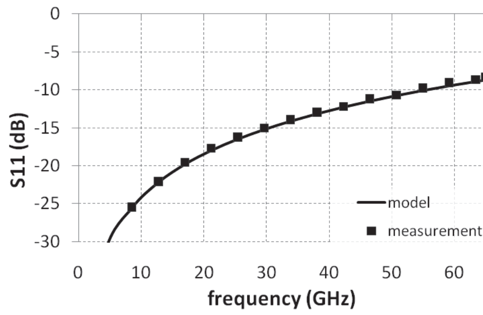


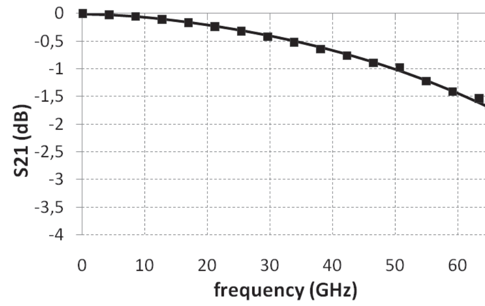
(a) Information obtained from $Re(Y_2)$

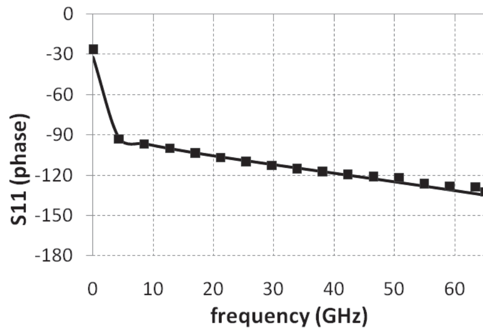


(b) Information obtained from $Im(Y_2)$

Figure 4.17: Plots used for extracting and optimizing the diode's parameters in the parallel configuration







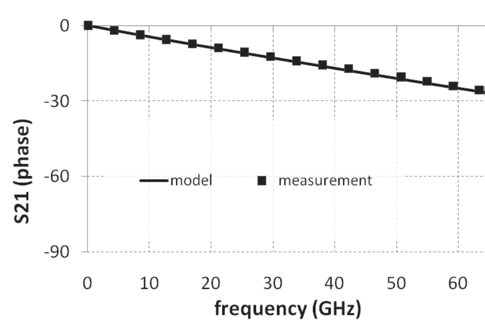


Figure 4.18: S-parameter (amplitude and phase) measurements vs. simulation for a diode device

- L_{be} is estimated by fitting Figure 4.17b at high frequencies

Finally, we shall compare the measured S-parameters with the ones obtained through simulations using the extracted model (Fig. 4.18):

The agreement between simulations and measurements is very good, validating the electrical models proposed for the diodes.

All the extractions above were done at $0\,V$. In this case, R_{on} is considered infinite.

Voltage dependent model

By modifying the bias, only C_s and R_{on} are affected. The change in voltage drop on the substrate can be neglected. Thus, in order to build the voltage dependent model, C_s and R_{on} are extracted at different biases.

C_s is extracted from the normalized imaginary part of Y_2, Figure 4.17b. This contains information about both C_{beAC}, the backend capacitance, and C_s, but only the latter varies with the voltage, being sensitive only at high-low frequencies (0-15 GHz). Thus, an optimization run in this range of the curve will lead to a very accurate value.

Fig. 4.19 shows the plots used to extract the junction capacitance for a diode made to be used in a triggering circuit of a DTSCR. Thus, it is important that the model describe it well under forward bias.

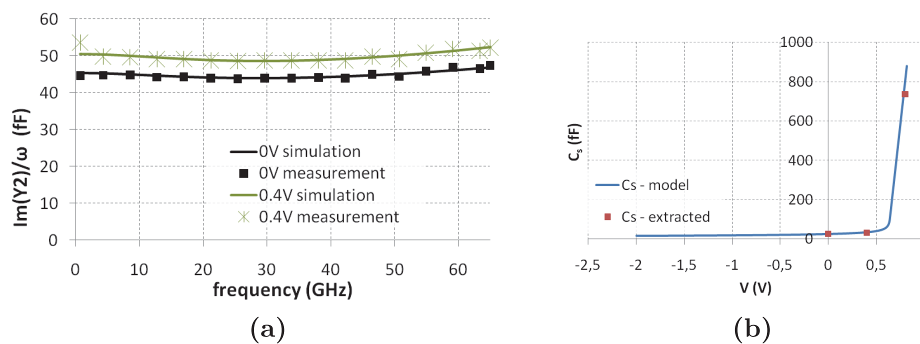


Figure 4.19: Normalized imaginary part of Y2, used for extracting or optimizing a triggering diode's junction capacitance at different voltages.

Fig. 4.20 shows the plots used to extract the junction capacitance for a diode made to be used as a protection device. Thus, it is important that the model describe it well under reverse bias. Nevertheless, in order to evaluate 4.1 and to more accurately estimate its parameters, V_{JS} and m_{jS}, measurements were also carried out under positive bias.

In both cases, V_{JS} and m_{jS} are extracted using a regression on the plots in Figure 4.19b and Figure 4.20b. C_{S0} is the capacitance extracted at 0 V.

I_S is extracted using classical I(V) DC measurements. R_{ONhc} is the R_{ON} extracted at 0.8 V. As the ESD protection devices are inactive during the normal functioning of the circuit they protect, the model proposed has its boundaries set at 0.8 V.

An overall evaluation is done by comparing S parameter measurements and simulations for different biases. Fig. 4.21 shows it for the triggering diode analysed above.

The agreement between simulations and measurement is very good, validating the electrical model proposed for the diode.

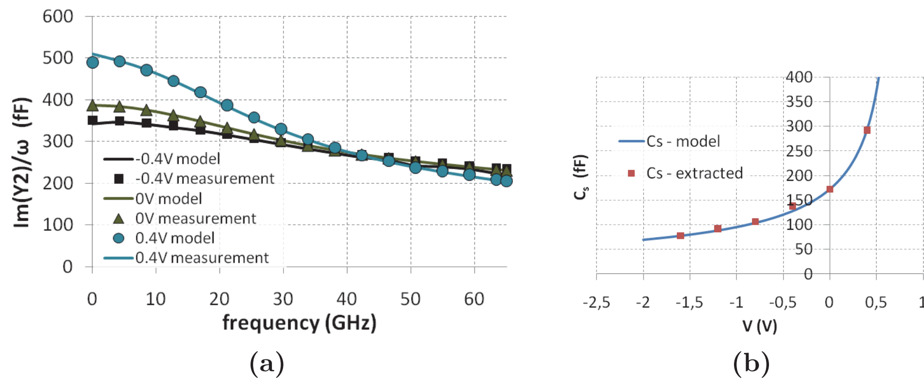


Figure 4.20: Normalized imaginary part of Y2, used for extracting or optimizing a protection diode's junction capacitance at different voltages.

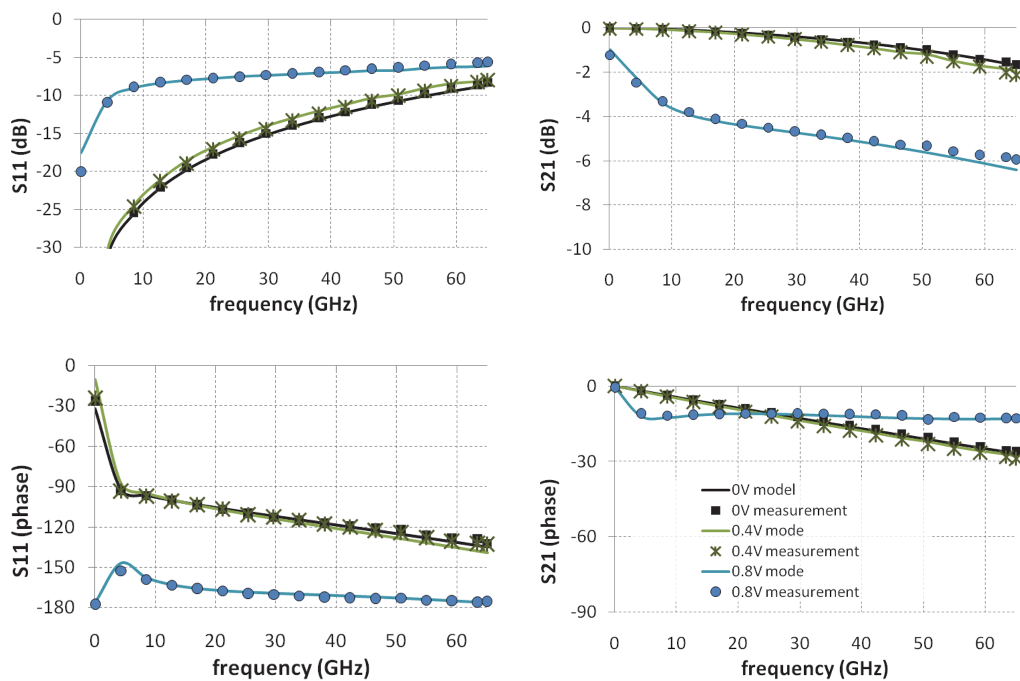


Figure 4.21: S-parameter (amplitude and phase) measurements vs. simulation for a diode device at different voltages

4.5.2 SCR parameter extraction

In a similar way, using a T configuration, the parameters for the SCR have been extracted and optimized.

Given the increased complexity compared to the diodes, a similar mathematically rigorous approach is not possible. A methodology consisting in tuning the parameters based on their impact on certain characteristics and at certain

frequencies will be presented. In order to facilitate the estimation of the parameters, the metal (backend) capacitances (C_{beAC}, C_{beANW} and C_{beNWC}) should first be extracted from Post-Layout-Simulations (PLS).

The reverse imaginary part of Z_1 multiplied by the frequency represents the sum of C_A and C_{beANW}. L_{beAC} can be optimized on the same plots, at high frequency. R_{ON_A} is extracted from the real part (Fig. 4.22).

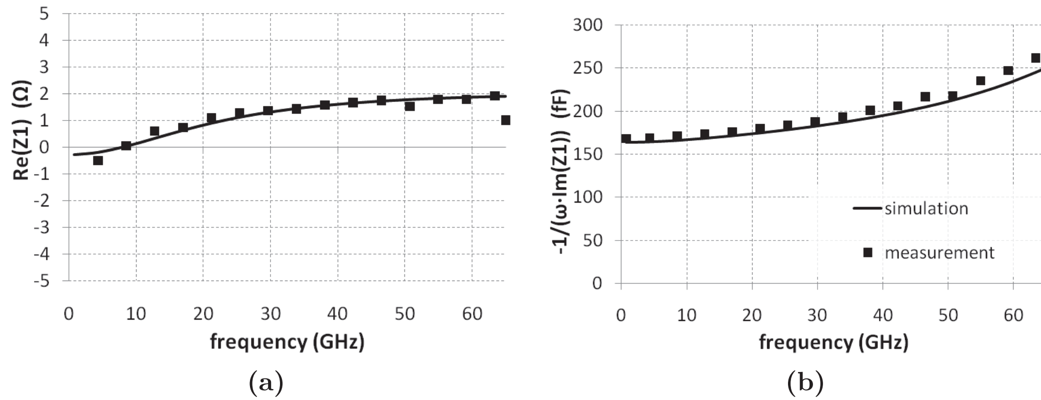


Figure 4.22: Information contained in the Z_1 branch of the SCR model

In the same manner, C_{np} and C_{beNWC} are extracted from the imaginary part of Z_2. C_{sub} is sensible at "high low" frequencies (up to $20\,GHz$) and R_{np} at high frequencies on the same plot. R_{np} can also be estimated from the real part of Z_2, also at high frequencies, while R_{sub} can be estimated from the information at low frequencies (Fig. 4.23).

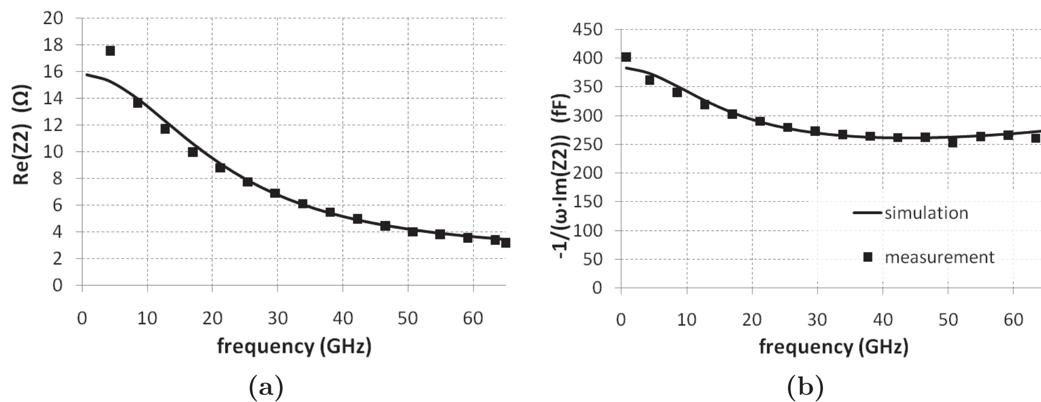


Figure 4.23: Information contained in the Z_2 branch of the SCR model

In the real part of Z_3 we have the influence of R_{nw} and C_{beNWC} (the latter's influence also being present in $Im(Z_2)$). From its imaginary part we can extract L_{beNW} (Fig. 4.24).

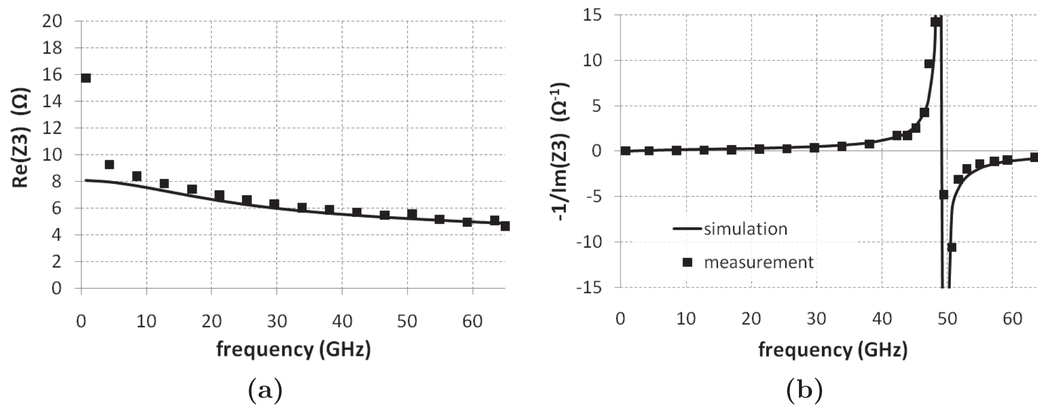


Figure 4.24: Information contained in the Z_3 branch of the SCR model

Finally, we shall compare the measured S-parameters with the ones obtained through simulations using the extracted model (Fig. 4.25).

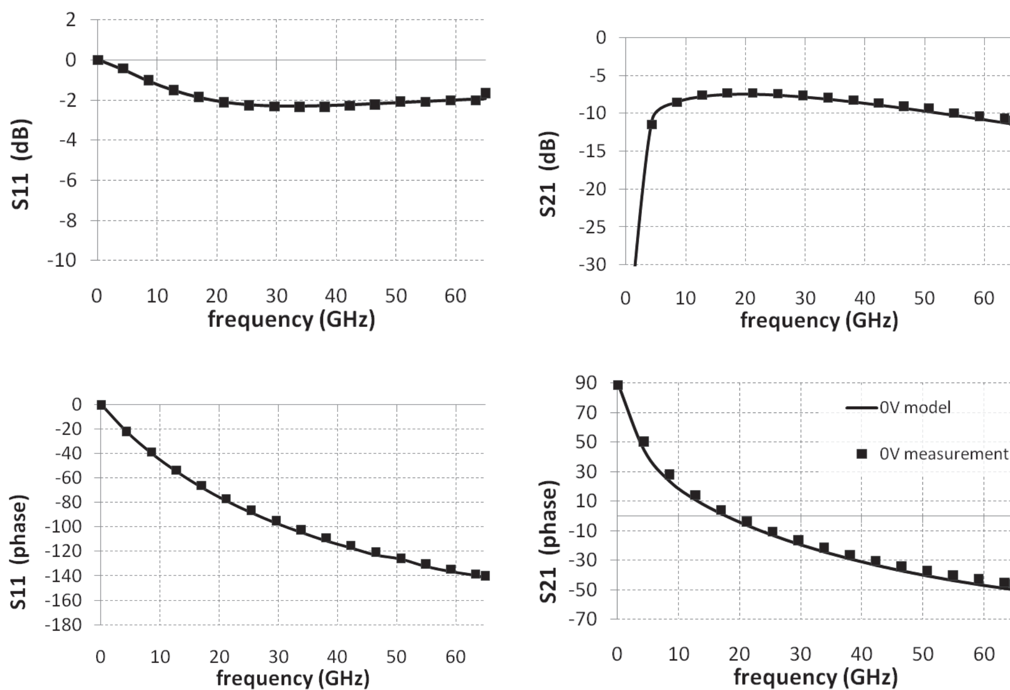


Figure 4.25: S-parameter (amplitude and phase) measurements vs. simulation for an SCR device

The agreement between simulations and measurement is very good, validating the electrical models proposed for the SCR.

Voltage dependent model

The parameters whose variation with the bias is important are C_A, C_{np} and C_{sub}. The bias is applied at the A; the NW is connected to the ground through the 50 Ω impedance of the network analyzer.

In order to determine the voltage distribution (as the part of the total voltage that falls over each internal junction - Fig. 4.26) in these conditions, an electrical DC model of the SCR was used (sec. 2.2).

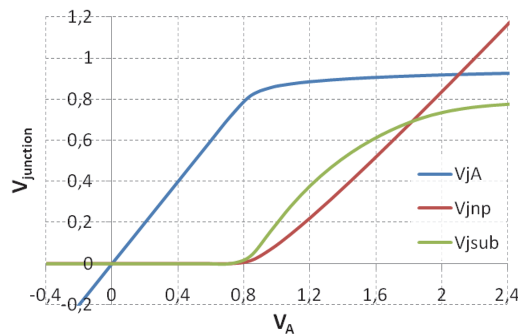


Figure 4.26: Internal voltage distribution in an SCR as function of the bias

Note that although Fig. 4.26 represents all the voltages as positive, C_{np} and C_{sub} are under reverse bias.

C_A is extracted from the imaginary part of Z_1. Compared to the measurement at $0\,V$, only C_A varies with the bias voltage. All the other capacitive elements are given by the backend. Fig. 4.27 shows the extraction of C_A for an SCR at 0 V and 0.4 V. At these voltages, almost all the voltage drop is on the anode junction.

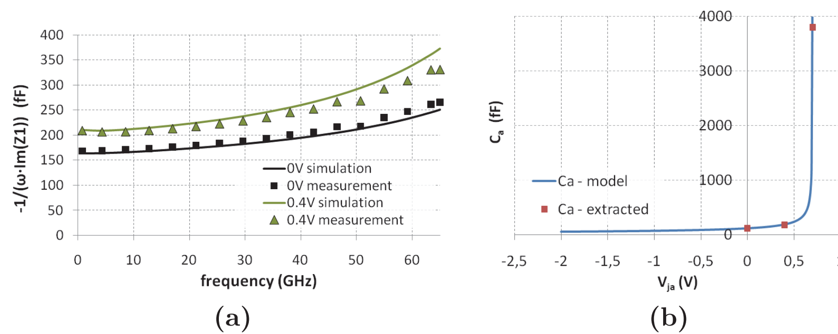


Figure 4.27: Plot derived from the imaginary part of Z1, used to extract C_A.

The capacitance varies with the voltage according to 4.4, as shown in Fig. 4.27.

C_{np} and C_{sub} are extracted from the imaginary part of Z_2. Fig. 4.28 is used for extracting them at 0 V, 0.8 V and 1.6 V. The actual voltage drops on the junctions are obtained using Fig. 4.26.

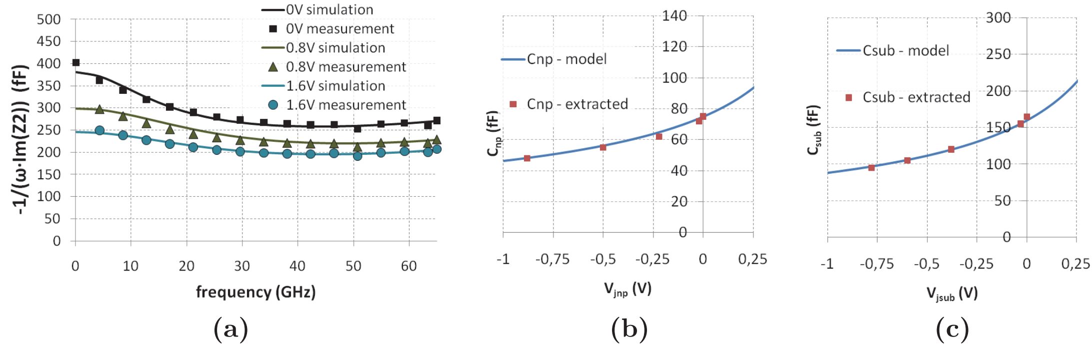


Figure 4.28: Plot derived from the imaginary part of Z_2, used to extract C_{np} and C_{sub}.

The depletion capacitance model parameters, V_J and m_j are extracted through a linear regression on the $C(V)$ curves.

An overall evaluation is done by comparing S parameter measurements and simulations for different biases (Fig. 4.29).

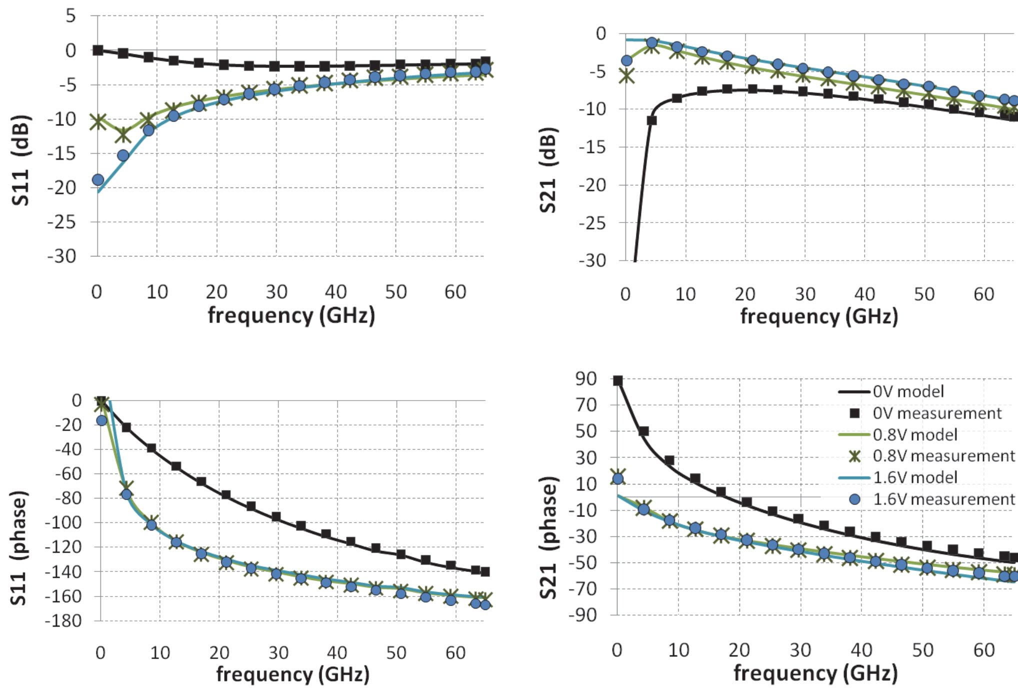


Figure 4.29: S-parameter (amplitude and phase) measurements vs. simulation for an SCR device at different voltages

Here again, the agreement between simulations and measurement is very good, validating the electrical models proposed for the SCR.

4.5.3 DTSCR validation

The DTSCR was measured with the setup shown in Fig. 4.11, and simulated using the diode and SCR models developed in the sections above.

The measurement configuration is similar to the one used for the diode in parallel, as shown in Fig. 4.8. As for the latter, the information regarding the device is contained in Z_2.

The quasi-linearity of Fig. 4.30 allows us to define it as the total, overall capacitance of the DTSCR (4.41). This is an important information needed by the ESD protection designer and the proposed model is shown to accurately present it.

$$C_{total} = -\frac{1}{\omega \cdot Im(Z_2)} \tag{4.41}$$

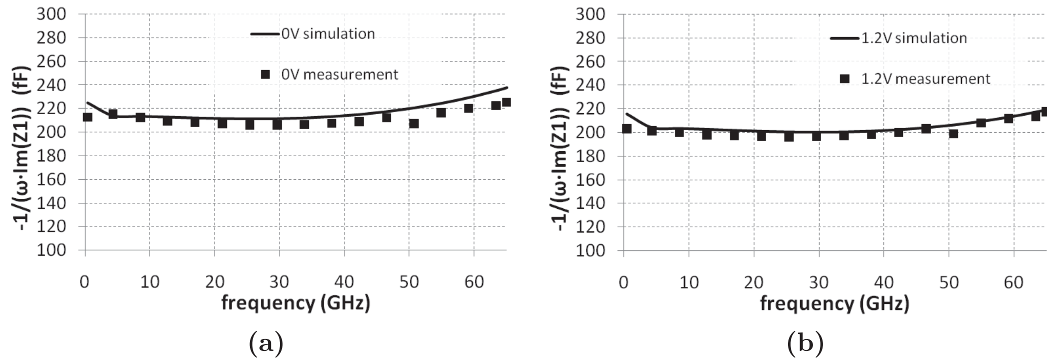


Figure 4.30: Total equivalent capacitance of a DTSCR

It was observed that the backend capacitances have a high impact on C_{total}, as well as the substrate capacitance of D2, thus the need of accurately modelling it with a separate measurement setup (Fig. 4.9).

It can be observed from Fig. 4.30 that the difference between the behaviour at 0 V is not very different of the one at 1.2 V, the capacitance levels being almost identical. This is due to the fact that different junction capacitance components vary in different senses with the applied voltage bias:

- the junction capacitance of D2 (C_s^{D2}) and the central junction capacitance of the SCR (C_{np}^{SCR}) decrease with the bias, being reverse-biased;
- the junction capacitance of D1 (C_s^{D1}) and the anode capacitance of the SCR (C_A^{SCR}) increase with the bias, being forward-biased.

The overall behaviour (measurement vs. simulation) is shown as S-parameters fit in Fig. 4.31. Two cases are presented: at no bias and for a 1.2 V voltage drop between

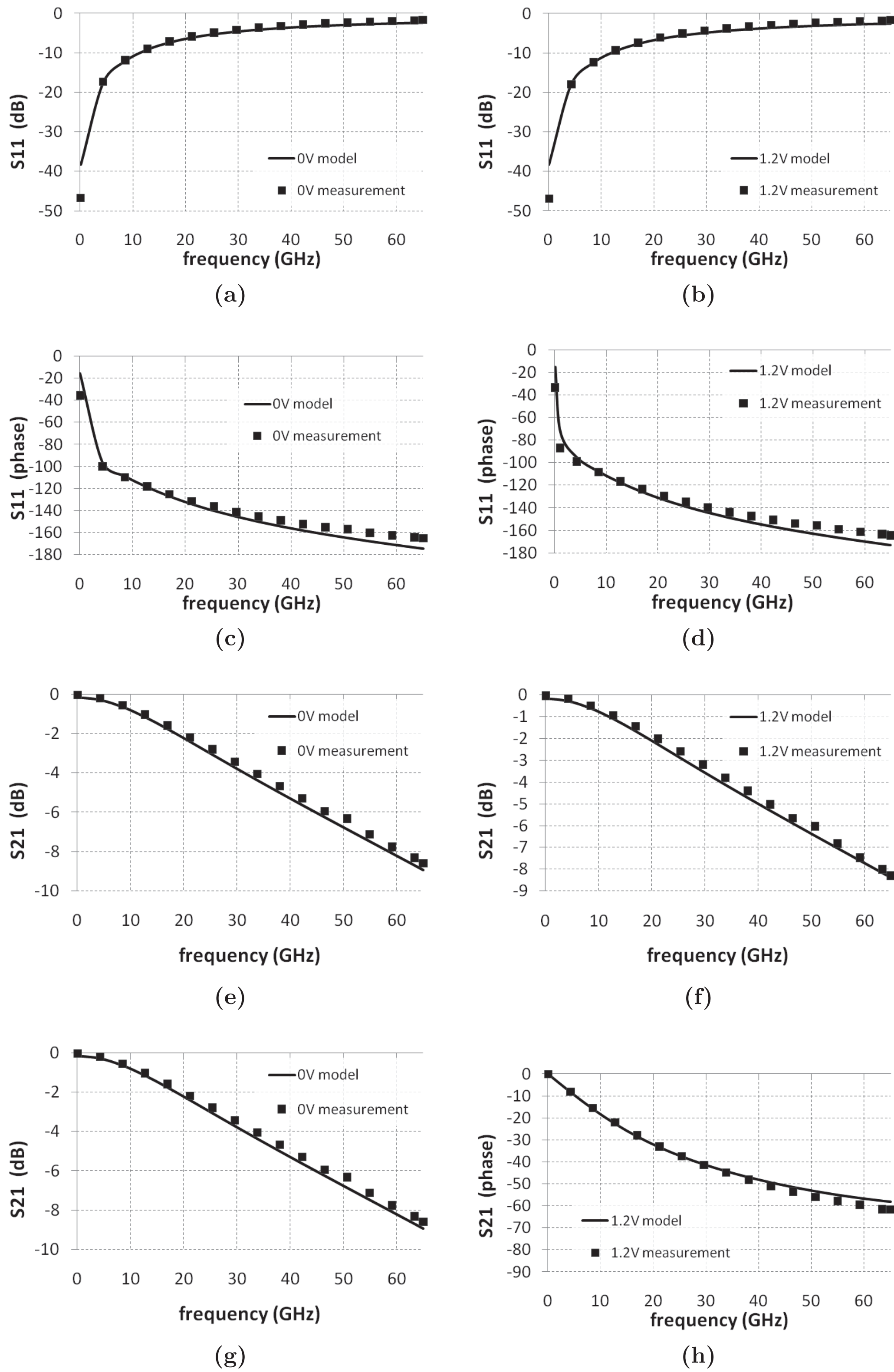


Figure 4.31: S-parameter (amplitude and phase) measurements vs. simulation for a DTSCR device at different voltages

the anode and the cathode of the DTSCR. The voltage distribution on each junction was obtained using the model presented in Fig. 4.26 for the SCR and a basic DC model for the diodes. The backend differences between the final DTSCR and the sum of its components taken separately were taken into account.

The results show that the models are able to predict the high frequency behaviour of a complete DTSCR ESD protection structure.

4.6 Conclusion

A microwave frequency electrical model was developed for the diode and the SCR ESD protection devices. In order to validate it, devices were realized and measured in a 130 nm technology. RF characterization plots were used (Fig. 4.17) and de-embedded using the Torres-Torres method [Torr'05]. The de-embedding was done so that the analysed devices include a part of the backend, the one that is considered part of the protection.

The parameters were rigorously extracted for the diode, by mathematically comparing the model and the measurement data. A similar approach was not possible with the more complex SCR. There, the parameters were estimated using their sensitivity on certain characteristics and at certain frequencies.

These models can accurately offer a detailed view on the influence the ESD protection devices have over the circuit they protect.

Furthermore, a complete, SCR based, ESD protection structure, a DTSCR (Fig. 4.2), was carried out. It has been shown that its microwave frequency behaviour can be predicted using the herein developed models, allowing the designers to adapt their circuit to the ESD protected input, from DC to 65 GHz. The models were shown valid under the usual biases an ESD protection device might be used.

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Conclusion

The primary target of this work was building a new model for the SCR ESD protection device, according to present and future industrial requirements. The detailed study was carried out from ESD functioning point of view to high frequency behaviour.

The ESD model was required to be accurate, scalable and have a relatively easy and consistent parameter extraction procedure. Different modelling strategies employed for ESD protection devices, as well as their capability in offering a robust model, were analysed. It was decided that the best approach would be to start a new model, coding directly its equations according to the physical phenomena. The core equations were inspired by the Gummel-Poon BJT model, as the bipolar effect is at the base of the SCR's functioning. However, they were modified and adapted, by taking into account the high injection recombination present in an SCR.

The model was written in Verilog-A and can be used by the industrial SPICE simulation programs.

A series of devices were designed in order to build the model, test it and develop a parameter extraction strategy. This part was done using the ST Microelectronics BiCMOS 130 nm technology.

The results were presented at the major annual ESD event, EOS/ESD Symposium, in 2010.

A strong point of this model is the fact that the important points of its I(V) characteristic are predicted by the model; they are not an empirical input, as model parameters, but an output, their value being a consequence of the multitude of phenomena controlling the current flow. This was mandatory for the further accomplished scalability work. The physical phenomena that lead to a certain triggering voltage, for example, vary in different directions and with different laws when the dimensions of the device change. An empirical approach would have been impossible given the scaling requirements and dimensions analysed.

The model was rendered scalable by making the value of its parameters dependent on the geometry. Three geometrical dimensions were taken into account: the width and length of the electrodes and the distance between them. The first two have an impact on the overall ESD performance, as in the maximum current that they are able to pass. The length of the electrodes was found to have a non-linear impact, giving the opportunity to use the model as a way to optimize the protection device. A scaling law was developed accordingly, making it the first model of the

ESD protection SCR that takes this important variation into account. The distance between the electrodes influences some of the functioning parameters, such as the triggering and the holding voltage, as well as the overshoot. All these influences are quantitatively predicted by the scalable model. The study was presented at the EOS/ESD Symposium in 2011.

The influence ESD protection devices have on the circuits they protect, a critical effect in high frequency designs, was also analysed in this thesis. Very few studies including high frequency characterization and modelling of ESD protection devices exist, although this problematic is a continuously increasing concern in the semiconductor manufacturing industry. Defining the problem and the methods needed to be used in order to solve it were among the most difficult tasks.

Building an SCR model that predict its high-frequency small-signal behaviour was the main target. Nevertheless, the SCR is never used alone in a protection circuit. Diodes that are usually used in conjunction with it were also analysed and tested together in a complete protection structure. A second reason to also analyse diodes was linked to their simplicity, making it easier to validate the RF analysis methodology developed for ESD protections.

The results were very good and presented during the International Microwave Symposium 2011.

One of the most important properties of the developed model is the ability to be easily upgradeable, following the advancements and new requirements of future technologies. This is a direct consequence of physical approach in the model building process. Different physical phenomena, such as low or high current recombination, Early effect, differentiated role as base or collector for the wells in current conduction etc., are independently modelled. The different nodes of the model correspond to specific regions in the physical structure of an SCR, making the model easily expandable to future improvements on the device.

One of the most important point not treated in this thesis is the thermal behaviour. A thermal model has two aspects: (i) the behaviour of the device at different environment temperatures and (ii) the self-heating happening during a high voltage ESD pulse. For the first aspect, the equations proposed in this thesis can be upgraded with the thermal aspect according to the classical thermal models present in semiconductor models, as in the BJT ones. For the second aspects, as it is a very important one in ESD protection, models that treat the self-heating in both the backend and the silicon bulk were already reported, just needing to be plugged in.

Another improvement, that will simplify the packaging of the model and, thus, its inclusion in the industrial development kits, is the merging between the ESD and the RF models. This is a non-trivial task. As the ESD pulses a device has to respond to are very short, the ESD model has to accurately predict the functioning of the device up to a couple of GHz. On the other hand, the RF model has to predict the influence of the device at higher frequencies. The values of the parameters the two models

have in common may differ, being extracted from different kinds of measurements and in different conditions. A separate study has to be done in order to put these two aspects of the model together.

Overall, this thesis offers a detailed study of the SCR ESD protection device, concluded with a ready to be industrialized model, and a high frequency analysis methodology for the ESD protection devices in general.

Conclusion (français)

L'objectif principal de ce travail a été la construction d'un nouveau modèle pour les dispositifs de protection contre l'ESD de type SCR, répondant aux besoins présents et futurs des industriels. L'étude détaillée a été réalisée à la fois d'un point de vue ESD, c'est-à-dire lorsque la protection est active, ainsi qu'en prenant en compte le comportement à haute fréquence, lorsque le circuit fonctionne correctement avec une protection non active.

Le modèle ESD développé se devait d'être précis, paramétrable en fonction de la géométrie des dispositifs, et de disposer d'une procédure relativement simple et cohérente pour l'extraction des paramètres constitutifs. Différentes stratégies de modélisation utilisées pour les dispositifs de protection contre l'ESD, ainsi que leur capacité à fournir un modèle robuste, ont été analysées. Il a été décidé que la meilleure approche serait de développer un nouveau modèle, en codant directement ses équations en fonction des phénomènes physiques. Comme l'effet bipolaire est à la base du fonctionnement du SCR, les équations de base ont été inspirées par le modèle de BJT Gummel-Poon. Cependant, il a été modifié et adapté, afin de prendre en compte le phénomène de recombinaison à forte injection, présent dans un SCR.

Le modèle a été écrit en Verilog-A et peut être utilisé par les programmes industriels de simulation SPICE.

Une série de dispositifs ont été conçus afin de construire le modèle, le tester et développer une stratégie d'extraction de paramètres. Cette partie a été réalisée en utilisant la technologie STMicroelectronics BiCMOS9 130 nm.

Les résultats ont été présentés à l'événement majeur ESD annuel, « EOS / ESD Symposium », en septembre 2010.

Un point fort de ce modèle réside dans sa capacité à prédire de manière très précise les points importants de la caractéristique I(V) du SCR, et en particulier le point de déclenchement. Celui-ci n'est plus une donnée d'entrée empirique, comme dans les précédents modèles, mais bien une valeur de sortie. Ainsi chaque caractéristique prédite par le modèle est une conséquence de la multitude de phénomènes physiques contrôlant le flux de courant. Cette démarche était nécessaire pour le travail de paramétrisation géométrique réalisé par la suite. Les phénomènes physiques qui conduisent à une certaine tension de déclenchement varient, par exemple, dans des directions différentes et avec des lois différentes lorsque les dimensions du dispositif changent. Une approche empirique n'aurait pu aboutir à une modèle paramétrable.

La notion de modèle paramétrable géométriquement implique que ses paramètres dépendent de la géométrie. Trois dimensions ont été prises en compte : la largeur et la longueur des électrodes ; ainsi que la distance entre les électrodes. Les deux premières dimensions ont un impact sur la performance ESD, comme le courant maximum que le dispositif est capable d'absorber. La longueur des électrodes a un impact non linéaire, donnant la possibilité d'utiliser le modèle comme un moyen d'optimiser le dispositif de protection. Une loi d'échelle a été développée en conséquence, menant au premier modèle de SCR de protection prenant cette variation importante en compte. La distance entre les électrodes influence certains paramètres de fonctionnement, tels que le déclenchement et la tension de maintien, ainsi que l' « overshoot ». Toutes ces influences sont quantitativement prédites par le modèle. L'étude a été présentée lors du « EOS / ESD Symposium » en septembre 2011.

Les dispositifs de protection contre l'ESD ont une influence sur les circuits qu'ils protègent. Cet effet, critique pour la conception à haute fréquence, a également été analysé dans cette thèse. Très peu d'études sur la caractérisation et la modélisation à haute fréquence des dispositifs de protection contre l'ESD existent, bien que cette problématique soit devenue une réelle préoccupation dans l'industrie de fabrication des semiconducteurs. Définir le problème et les méthodes nécessaires pour le résoudre ont été parmi les tâches les plus difficiles de ce travail de thèse. La construction d'un modèle du SCR permettant de prédire le comportement à haute fréquence et petit signal a été le but principal. Néanmoins, le SCR n'est jamais utilisé seul dans un circuit de protection. Des diodes, qui sont habituellement utilisées en conjonction avec le SCR, ont également été analysées et testées, dans un premier temps de manière indépendante, puis au sein d'une structure de protection complète. Une seconde raison d'analyser également les diodes est lié à leur simplicité, ce qui a permis de valider dans un premier temps la méthodologie d'analyse RF développée pour les dispositifs de protection contre l'ESD. Les résultats ont été très bons et ont donné lieu à une présentation orale lors du « International Microwave Symposium » en juin 2011.

Une des propriétés les plus importantes du modèle développé réside dans sa capacité à être facilement mis à jour, suivant les progrès et les nouvelles exigences des technologies du futur. Ceci est une conséquence directe de l'approche physique dans le processus de construction du modèle. Différents phénomènes physiques, tels que la recombinaison à faible ou à fort courant, l'effet Early, le rôle différencié entre base ou collecteur pour les caissons dans la conduction du courant, etc..., sont modélisés de manière indépendante. Les différents nœuds du modèle correspondent à des régions spécifiques de la structure physique d'un SCR, ce qui rend le modèle facilement extensible pour les futures améliorations du dispositif.

Un des points les plus importants n'a pas pu être abordé dans cette thèse : le comportement thermique. Un modèle thermique recouvre deux aspects : (i) le comportement du circuit à différentes températures de l'environnement et (ii) la survenance d'auto-échauffement pendant une impulsion ESD à haute tension. Pour le premier aspect, les équations proposées dans cette thèse peuvent être

améliorées pour prendre en compte l'aspect thermique selon les modèles classiques de semi-conducteurs, comme dans les BJT. Pour le second aspect, très important dans la protection ESD, les modèles qui traitent de l'auto-échauffement dans les backend et le silicium bulk ont été déjà identifiés, il reste seulement à les implémenter au sein du modèle développé dans la thèse.

Une autre amélioration, qui permettra de simplifier le packaging du modèle et, par conséquent son inclusion dans les kits de développement industriel, est la fusion entre les modèles ESD et RF. C'est une tâche non triviale. Le temps de montée des impulsions ESD impose au modèle ESD de prédire avec précision le fonctionnement de l'appareil à quelques GHz seulement. Afin de répondre aux besoins des concepteurs RF pour les systèmes fonctionnant aux fréquences millimétriques (plusieurs dizaines de GHz), le modèle RF doit prédire l'influence de l'appareil à des fréquences nettement plus élevées. La valeur des paramètres que les deux modèles ont en commun peuvent différer du fait du très large spectre à couvrir. En outre ils sont extraits à partir de mesures différentes réalisées avec des systèmes de mesures différents. Une étude approfondie doit être menée avant de regrouper les modèles, cette étude devra permettre d'identifier les paramètres communs, d'évaluer leur impact à l'ensemble des fréquences concernées, puis à rechercher le modèle optimal commun.

Globalement, cette thèse propose une étude détaillée du dispositif de protection contre l'ESD de type SCR, conclu avec un modèle prêt à être industrialisé, et d'une méthodologie d'analyse à haute fréquence pour les dispositifs de protection contre l'ESD en général.

List of publications

"A Novel Physical Model for the SCR ESD Protection Device", A. ROMANESCU, P. FONTENEAU, C. LEGRAND, P. FERRARI, J. ARNOULD, J.MANOUVRIER, H.BECKRICH-ROS, *32nd Electrical Overstress/ Electrostatic Discharge Symposium* (EOS/ESD 2010, Reno, NV, USA)

"Modeling a SCR-based protection structure for RF-ESD co-design simulations", A. ROMANESCU, P. FERRARI, J. ARNOULD, P. FONTENEAU, C. LEGRAND, *International Microwave Symposium 2011* (IMS 2011, Baltimore, MD, USA), paper in the final for the Student Paper Competition (25 out of 199 papers selected)

"Scalable Modeling Studies on the SCR ESD Protection Device", A. ROMANESCU, H.BECKRICH-ROS, P. FONTENEAU, C. LEGRAND, P. FERRARI, J. ARNOULD, *33nd Electrical Overstress/ Electrostatic Discharge Symposium* (EOS/ESD 2011, Anaheim, CA, USA)

"Modélisation à Haute Fréquence de Dispositifs de Protection Contre la Décharge Electrostatique", A. ROMANESCU, P. FERRARI, J. ARNOULD, P. FONTENEAU, C. LEGRAND, H.BECKRICH-ROS, J.MANOUVRIER, 17eme Journées Nationales Microondes, (JNM 2011, Brest, France)

"Voltage Dependent High Frequency Modeling of ESD Protection Devices", A. ROMANESCU, J. ARNOULD, P. FONTENEAU, C. LEGRAND, P. FERRARI - *in progress*

// Abstract

Electrostatic discharge (ESD) protection is a must in every integrated circuit. It is done by deploying a network of special devices on-chip, alongside the functional elements. The demand for continuously improvements in ESD design and simulations brings the need of new and more accurate scalable models.

The SCR (silicon controlled rectifier) is one of the most efficient ESD protection devices. A new electrical model, that can be used to evaluate the complex protection structures of which it is part of, was developed during this thesis. Built with a strong relation between the physical phenomena and its equations, it was rendered scalable, offering the possibility of tailoring and optimizing the device according to the needed protection level. Moreover, a high-frequency study on the SCR and the ESD protection diode was carried out, leading to a model able to predict the impact these devices have on the protected circuit.

Keywords: Electrostatic Discharge, modeling, compact model, scalable, silicon, over-voltage protection, microwave measurements, thyristors.

// Résumé

La protection contre les décharges électrostatiques (ESD) est un fait necessaire dans chaque circuit intégré. Elle se fait par le déploiement sur la puce d'un réseau de dispositifs spéciaux, à côtés des éléments fonctionnels. La demande pour des améliorations en continu dans la conception et la simulation de l'ESD apporte le besoin de modèles nouveaux et plus précises.

La SCR (« Silicon Controlled Rectifier ») est l'un des dispositifs les plus efficaces de protection contre l'ESD. Un nouveau modèle électrique, qui peut être utilisé pour évaluer les structures de protection complexe dont il fait partie, a été développé au cours de cette thèse. Construit avec une forte relation entre les phénomènes physiques et ses équations, il a été parametrisé geometriquement, offrant la possibilité d'adapter et d'optimiser le dispositif selon le niveau de protection nécessaire. Par ailleurs, une étude à haute fréquence sur le SCR et la diode de protection ESD a été réalisé, conduisant à un modèle capable de prédire l'impact de ces dispositifs ont sur le circuit protégé.

Mots-clés : Décharge électrostatique, modélisation, modèle compact, paramétrisation, silicium, caractérisation micro-ondes.