Ultra-capacitor based regenerative energy storage and power factor correction device for controlled electric drives

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Ultra-capacitor based regenerative energy storage and power factor correction device for controlled electric drives

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PhD Dissertation

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PART ONE: INTRODUCTION AND GENERAL CONSIDERATIONS OF THE DISSERTATION

1. GENERAL INTRODUCTION

1.1. Background

1.1.1. Short History of Electric Drives

Through the centuries, “the production power” was the power of animals and slaves, hydro power and wind power. In the 1800s, after the invention of James Watt, it was the power of the steam machine. With the invention of electricity, electrical energy gradually came into focus. The first motors were direct current (DC) motors. At the end of 1800s, Nikola Tesla invented the three-phasevoltage system and the most famous motor; the induction motor was born. Because of many advantages over DC motors, the induction motors became dominant in most constant speed electric drive applications. However, difficulty with speed regulation was the basic disadvantage of the induction motor, and the main limiting factor for application in variable speed applications.

At the beginning of 20th century, a few configurations of variable speed drives were used.

1) Ward-Leonard motor-generator group. Since power conversion in such a system is done three times and a dc machine is included in the loop, this concept had not been broadly accepted in high power applications.

2) Wound rotor induction motor. The motor speed were adjusted and “regulated” by a circuit connected to the rotor via set of brushes, while the stator is connected to the fixed frequency supply. 1) The rotor resistor control and 2) “constant power” Kramer or “constant torque” Scherbious configurations [1].

All these drive configuration were fairly inefficient and faced a problem of reliability.

1.1.1.1. The Early “Power Electronics” Driven ac Drives

The first period in development of “power electronics” controlled electric drives was the period between 1910 and 1940. Early “power electronics” drives were based on triggered-arc power switches, such as controlled mercury-arc rectifiers, thyratrons and ignitrons. The drive configurations were the electronic Kramer configuration using uncontrolled rectifier bridge, electronic Scherbius using rectifier-inverter configuration, Brown Boveri commutator-less drive, thyratron motor configuration and early version of load commuted synchronous motor drive [1]. In 1930s, the first cycloconvertor was used. All those topologies did not have broad success in industrial applications, simply because of complexity and reliability issues of the “power electronics” switches.

In early 1960s, the first silicon controlled rectifier (SCR) was invented. This invention brought a large step in development of power electronics controlled electric drives. Kramer and Scherbius drive configuration, load commuted synchronous motor drives and cycloconvertor drives become dominant in most of high power applications. Later on, current sourced inverter with variable output frequency became a very competitive scheme for induction motor applications. Voltage source drive topologies became competitive with the

invention of the gate turn-off thyristors (GTO) in 1970s and insulated gate bipolar transistors (IGBT) in the 1980s.

1.1.2. Present

Today, 70 % of the world electricity production is consumed by some kind of controlled electric drives; traction and transportation drives, industrial drives, home appliance drives and so on. This indicates the importance of controlled electric drives in everyday life.

Modern low voltage controlled electric drives are exclusively based on three-phase motors, either induction or permanent magnet synchronous motors [2]-[3]. The motor is powered from a power converter, so-called the drive converter, having variable output voltage and frequency. The drive converter is supplied from low voltage industrial or distributive three-phase mains 230 V to 690V, 50 Hz to 60Hz. The most common converter topology is a cascade-connected diode front-end rectifier and voltage source pulse width modulated (PWM) inverter. A simplified circuit diagram is depicted in Fig. 1.1. The drive converter consists of an input three-phase diode rectifier (D_1-D_6), dc bus link with passive filter ($L_{BUS}C_{BUS}$) and pulse width modulated (PWM) output inverter (S_1-S_6). The rectifier generates dc bus voltage v_{BUS}, which is further inverted in the output variable ac voltage via PWM inverter. The input rectifier is based on Si diodes, while the output inverter is exclusively based on IGBT devices [4]. Switching frequency falls in range of few kHz up to 20kHz. The PWM inverter is controlled from the upper level controller using some of advanced digital control techniques. The control objective is the control of the motor torque and speed in closed or open loop control mode [3].

An additional switch S_B, diode D_B and resistors R_B, so-called brake chopper and resistor are used in applications with a demand for braking of the drive load (hoisting and large inertia applications). The braking energy is dissipated in the brake resistor R_B via the brake chopper S_B D_B. This is, in fact, one of the most limiting factors for advanced high efficient drive applications.

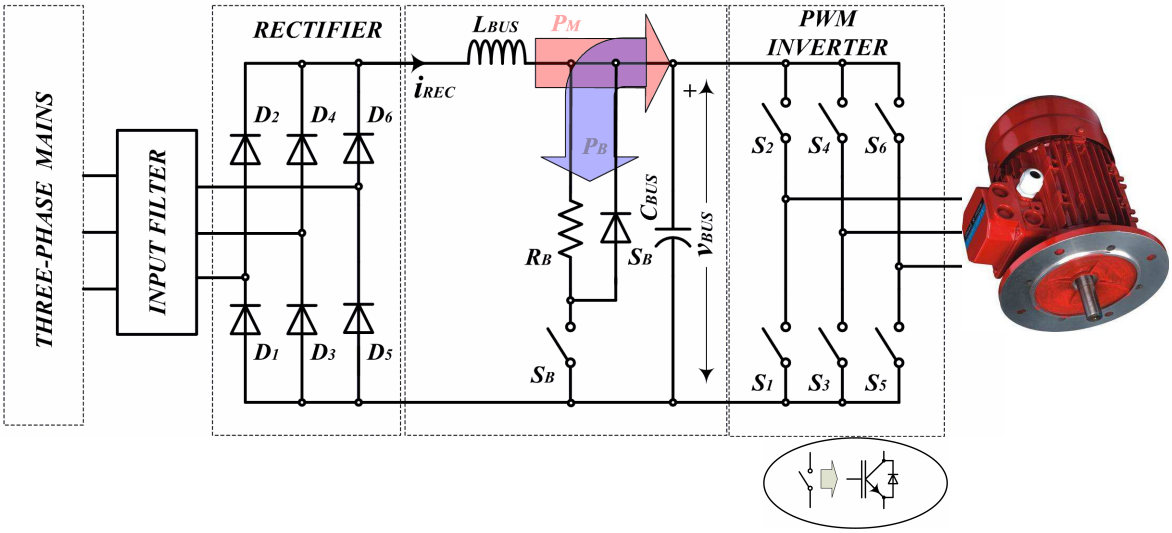
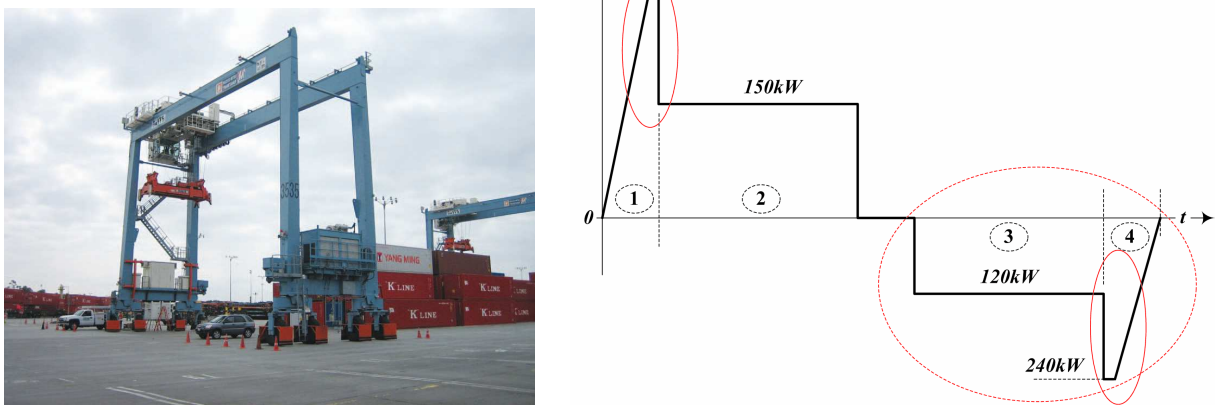


Fig. 1.1 State of the art low voltage drive converter based on voltage source indirect AC-DC-AC conversion. The output voltage is pulse width modulated (PWM) having fundamental voltage that is adjustable in amplitude, frequency and phase.

1.1.3. Typical Applications of Controlled Electric Drives

1.1.3.1. Hoisting and Lift Applications

The first type of applications that are in the scope of this project are hoisting type applications. Fig. 1.2 (a) shows photography of one typical on-port rubber tyred gantry (RTG) crane [5]. The hoisting drive time-power profile is sketched in Fig. 1.2 (b). When lifting the load, the hosting drive takes energy from the primary supply, in this case a diesel engine generator. When lowering the load, the drive operates in braking mode. As a diesel engine generator is not reversible, the braking energy cannot be pumped back into the primary power source. Instead, it is dissipated as heat in the brake resistor.



(a) (b)

Fig. 1.2 a) Rubber tyred gantry crane. b) Typical power profile of a hoisting application: lifting the load and acceleration (1), lifting the load at constant speed (2), lowering the load at constant speed (3) and lowering the load and deceleration (4).

Lift applications are similar to the RTG crane applications, except for two differences. The mains as the primary power supply source in lift applications is reversible. This means that the drive braking energy can be pumped back to the mains. The lift load (cabin) is balanced with a counterweight. Thus, the drive operating mode depends on the load direction (up or down) and ratio of the load to the counterweight.

1.1.3.2. Machines with Intermittent Load

The second type of application to consider is industrial machines with intermittent load. Such applications are characterised by low ratio of average to peak power. The input power is highly positive when the drive accelerates, and the power is highly negative when the drive decelerates. During constant speed operation, the input power is normally low. Fig. 1.3 illustrates the time-power profile of such a drive application. Typical application is tools carriers in automatic milling machines [3].

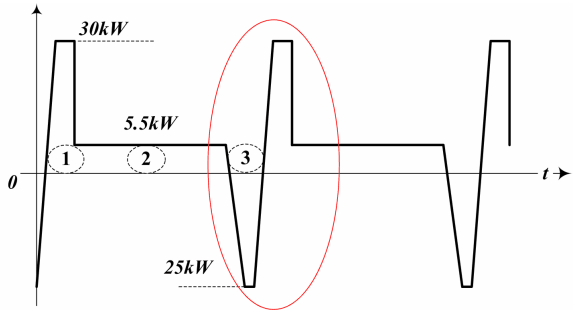


Fig. 1.3 Typical power profile of a controlled electric drive applied in a machine with cycling load: acceleration (1), constant speed (2), and deceleration (3).

1.1.3.3. Blowers and Pumps Applications

These applications are normally the simplest controlled electric drive applications. Blowers and pumps do not require specific control scheme and do not require braking (at lest do not require fast braking). In some cases, those applications can be sensitive to the mains power interruptions if applied in critical process industry.

Low power irrigation pump systems are specific application because the mains supply is often single-phase network. The motor is a three-phase induction motor powered from a three-phase PWM inverter.

1.1.4. Remaining Technical Issues in Application of Controlled Electric Drives

Six technical issues in application and design of modern variable speed drives can be identified. Those issues are still a great challenge for power electronics researchers and drive designers [6].

1.1.4.1. Saving and Recovery of the Drive Braking Energy

A lot of industrial and other applications, such as lifts, cranes and tooling machines are characterized by low balance between the input average power and peak power. Moreover, such applications have a demand for braking at full power. In ordinary variable speed drives, the mechanical energy stored in rotating mass of the motor load and the motor shaft is usually realized and wasted in a braking resistor. The energy losses in such applications go up 20 to 50% of the consumed energy. In today's energy crisis, energy efficiency has become the issue that needs an urgent solution [6].

1.1.4.2. The Drive Ride-Through Capability

Modern controlled electric drives are sensitive to the mains supply disturbances. The most frequent disturbances are voltage dips/sags. A voltage sag is defined as instantaneous decrease in the RMS voltage, where the decrease is in range of 10 to 90% of the nominal voltage, while the sag duration is in order of a half cycle up to a minute [7]-[11]. Such a power interruption causes the dc bus voltage to drop below its lower limit, and then the entire drive system trips. The system interruptions are very costly and unacceptable when the drive is applied in critical process industry, oil pump systems, semiconductor and glass industry.

Such kind of industries have reported losses ranging from 10k$ to 1M$ per disrupting event [10].

1.1.4.3. Quality of the Drive Input Current

Another power quality issue, which is introduced by the drive itself, is quality of the drive input current. Harmonic spectra of the drive input current depends on the drive rectifier topology. Ordinary diode front-end rectifiers equipped with passive LC filter draws the input current that is distorted and rich with higher harmonics. An example set of waveforms is depicted in Fig. 1.4 (a). Total harmonic distortion (THD) factor can be as high as 150%, or even higher [12].

The mains current harmonics cause additional heating and stress of the distribution transformers, power factor correction capacitors and neutral line in low voltage distribution network. Electromagnetic interference (EMI) with communication network and sensitive equipment is a critical issue too. To avoid or at least minimize those problems, advanced controlled electric drive converters have to comply with the input current harmonics limitations defined by international standards [13].

1.1.4.4. Quality of the Drive Converter DC Bus Voltage

The dc bus voltage is the intermediate voltage in the conversion path from the mains supply to the motor terminal. To achieve full motor voltage without distortion, it is important to provide sufficient dc bus voltage without significant fluctuation and ripple. Moreover, the higher dc bus voltage the better performance of the motor current and torque control [3].

The ordinary diode rectifier provides the dc bus voltage that is lower than the mains phase-to-phase peak voltage. The voltage ripple at 6^{th} harmonic of the mains frequency is significant too. An example set of waveforms is depicted in Fig. 1.4 (a). The motor voltage, therefore, is not well controlled in case that the drive operates in full speed mode. This causes distortion of the motor flux and ripple in the motor torque. Negative effects of that are well known: oscillations and mechanical stress of the load machine, noise and vibrations.

1.1.4.5. Single Phase Supply with or without the Drive De-rating

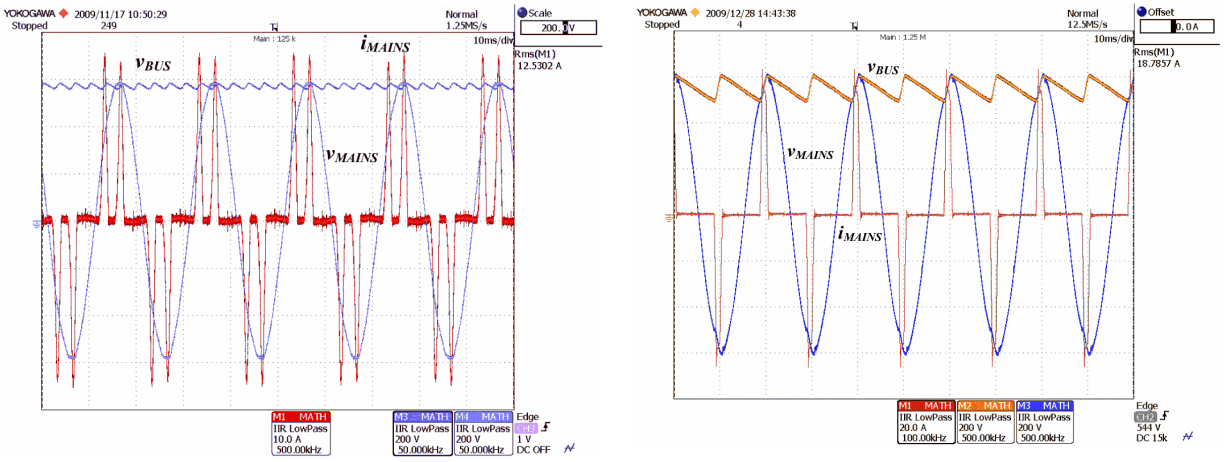
Operation of three-phase variable speed drives on single-phase supply is an application issue to be considered too. Single-phase supply could be due to the mains degradation when one of three phases is disconnected. In that case the drive rectifier is supplied with one phase-to-phase voltage. From the rectifier side it is nothing other than a single-phase supply. Another application example is rural single-phase supply network or specific drive applications, such as irrigation and small water supply systems.

Ordinary single-phase supplied diode front-end rectifiers draw an input current that is distorted and rich with higher harmonics. An example set of waveforms is depicted in Fig. 1.4 (b). The current peak is 5 to 10 times greater than the first harmonic current. This causes significant losses in the dc bus capacitor and input rectifier bridge. To be able to continuously operate under such conditions, the drive power has to be reduced to less than 40% of the drive rated power.

1.1.4.6. Smoothing of the Drive Peak Power

Some controlled drive applications are characterized by low ratio of the average to peak power. Typical examples are lifts and hosting applications, and industrial tolling

machines having intermittent load. Fig. 1.5 shows waveforms of the mains current i_{MAINS} and dc bus voltage v_{BUS} of an example controlled electric drive application. Peak power is 5500W for 0.8s, while minimum power is 500W for 1.6 s. It gives the ratio of average to peak power of 0.31. Thus, the drive cabling, fuses and contactors have to be over-sized by factor of 3. This type of load may also cause fluctuation and flicker in weak supply networks [14]. In lift applications the peak to average power ratio could be greater than 10, as reported in [15].



(a) (b)

Fig. 1.4 Waveforms of the mains current, voltage and the dc bus voltage. a) Three-phase supply, P_{LOAD}=5500W, the current scale [10A/div]. b) Single phase supply, P_{LOAD}=4000W, the current scale [20A/div].

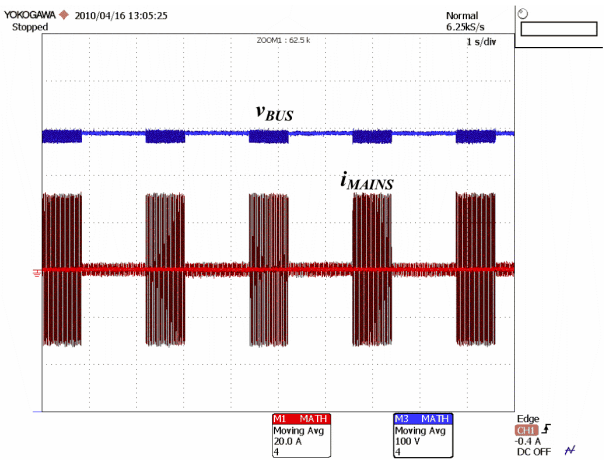


Fig. 1.5 Waveforms of the mains current i_{MAINS} [20A/div] and the dc bus voltage v_{BUS} [100V/div]. The drive load is cycling between 500W and 5500W at period of 2.2s with duty cycle of 30%. The average power is approximately 31% of the peak power.

1.2. Literature Overview

1.2.1. Regenerative Drives Based on Back to Back and Matrix Converter

Most of the existing regenerative controlled electric drive solutions belong to two groups; back to back PWM rectifiers [16], and so-called direct (matrix) converters, [17], [18].

Fig. 1.6 shows simplified circuit diagram of voltage source back-to-back and matrix drive converters. The drive takes energy from the mains whenever operates in motoring mode, and pumps the energy back to the mains whenever operates in breaking mode. The main disadvantage of such solutions is the fact that functionality and reliability of the drive is strongly linked to the mains reliability. Simple speaking, any power interruption of the mains is reflected on the drive. The drive is disabled whenever the mains is interrupted for longer than the mains cycle (20ms). Moreover, these drives have a high power demand during acceleration and deceleration (low ratio of average to peak power). This modulated input power produces additional losses and disturbances (flicker) in the weak supply mains.

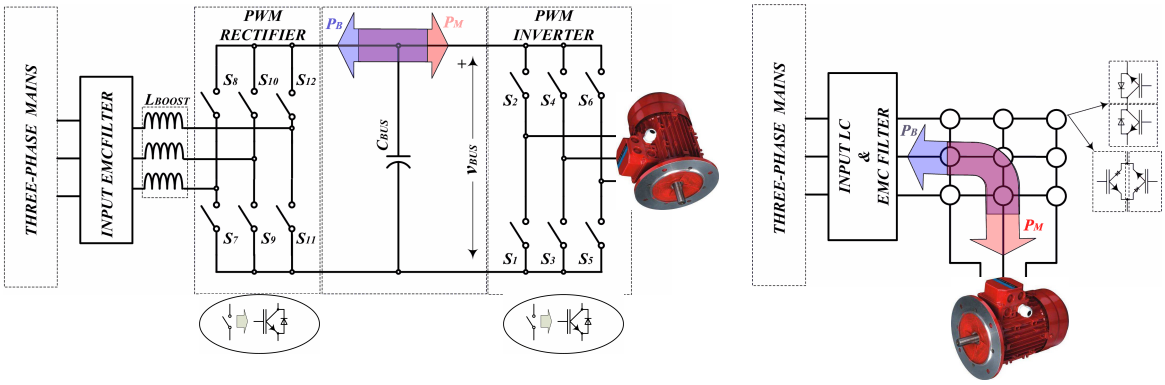


Fig. 1.6 a) Voltage source back to back regenerative controlled electric drive. b) Voltage source matrix drive converter.

1.2.2. Regenerative Drives Based on the Energy Storage Concept

A block diagram of a regenerative drive based on energy storage concept is given in Fig. 1.7. The drive system consists on an ordinary diode front-end converter equipped with an energy storage device [19]-[24]. This concept has come into focus recently with broad application of new electro-chemical double layer capacitors (EDLC), so-called ultra-capacitors [26]. An ultra-capacitor is electro-chemical capacitor having two porous electrodes made of activated carbon that are separated by a separator and impregnated with electrolyte [26]. Thanks to large specific surface ($2000m^2/g$) of activated carbon electrodes, the specific capacitance and energy are much higher than for standard electrolytic capacitors. In addition, the specific peak power of the ultra-capacitors is much higher than peak power of the existing electro-chemical batteries. Flywheel energy storage is usefully used in such a drive concept too [24].

The kinetic energy of the drive rotating masse, so-called braking energy is stored into the ultra-capacitor during the drive braking sequence. During the next motoring sequence, the energy is restored from the ultra-capacitor and realized on the drive. The first commercial applications of the ultra-capacitor based regenerative drives were traction and hybrid car drives [27]-[29]. General purpose variable speed drive with such an energy saving concept could be used in lift and hoisting applications, tooling machines having high demand for frequent and fast start/stop sequence, and many other application having a demand for braking. In [5], such a drive concept is analyzed and successfully applied on the rubber tyred gantry (RTG) crane. As reported in [5], the fuel saving is 30% to 40%. Moreover, the diesel

gen-set can be re-sized and smaller unit could be used. The same drive concept has been proposed for building lift applications [20], [15]. The ultra-capacitor as the energy storage for short term UPS function or extension of the drive ride-through capability is applied in critical industrial applications [21], [22].

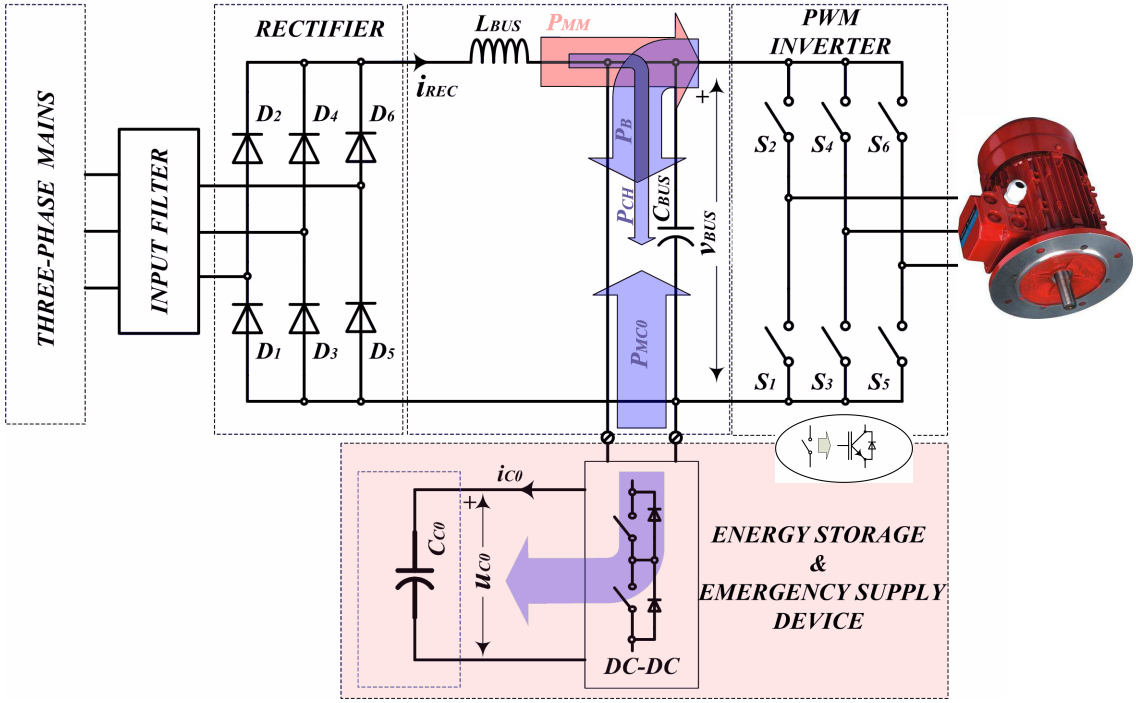


Fig. 1.7 Controlled electric drive based on an ordinary drive converter with parallel connected energy storage and emergency power supply device.

Unlike electrochemical battery, the ultra-capacitor state of charge strongly depends on the capacitor terminal voltage. The capacitor voltage varies a lot when the capacitor is charged/discharged. That means the ultra-capacitor cannot be connected directly to the drive dc bus, because the voltage adaptation and matching between the ultra-capacitor and dc bus. To achieve flexibility and high efficiency, a dc-dc power converter is used as a link between the ultra-capacitor and the drive [30]-[42].

Most of dc-dc converter topologies are based on the ordinary two-level single-phase or multiphase interleaved topologies [5], [30]-[35]. The main drawback of these topologies is the switches voltage rating. The switches are rated on the full dc bus voltage. As the dc bus voltage may go up to 800V, even more, the switches are rated on 1200V. This becomes an issue if the converter switching frequency is quite high; let us say above 20kHz. Switching losses become quite significant. It causes degradation in the conversion efficiency and additional difficulties in the converter thermal design. Two-level dc-dc converter with soft switching has been presented in [36]. This solution offers lower switching losses. However, since the converter operates in discontinuous conduction mode (DCM), the peak current and ripple current are significantely greater than one that operates in continuous conduction mode (CCM). This causes a problem of the inductor losses, particularly the core losses. Moreover, additional losses on the ultra-capacitor internal resistance cannot be neglected if the output current is not well filtered. Isolated dc-dc converter topologies with soft switching have been analyzed in [37], [38]. These topologies are attractive solutions when ratio of the dc bus voltage to the ultra-capacitor voltage is high, greater than 2. If the ratio is lower than 2, the

efficiency is lower than that of a non-isolated ordinary topology. Three-level converters are well adopted solution in applications with high input voltage and relatively high switching frequency [39]- [40]. The switches are stressed on half of the total dc bus voltage. This allow us to use lower voltage rated switches having better switching and conduction performance compared to the switches rated on the full blocking voltage. Therefore, the converter overall performances, including cost and efficiency, can be significantly improved compared to two-level converters, especially when the switching frequency is above 20kHz or MOSFETs are used [41].

Most of the control methods presented in the literature are focused on hybrid electric vehicle and power sources [14], [27]-[29], [32]-[35], [43]-[47]. Only a few publications are focused on control of the ultra-capacitor based electric drives [5], [21]-[22].

1.2.3. The Mains Current Harmonics and Related Issues

The energy storage based electric drives provide a more efficient way to save braking energy and improve global efficiency and reliability of the controlled electric drive systems [48]. The input current quality, however, remains an unsolved challenging issue. In the last decade, numerous different solutions for this problem have been proposed and discussed in literature.

Single-switch three-phase continuous conduction mode (CCM) boost rectifier is a solution that offers numerous advantages compared to the ordinary diode front-end rectifier [49]-[51]. The rectifier output current is constant and therefore the mains current is $2\pi/3$ square waveform with THD of approximately 30%. The dc bus voltage is actively controlled and boosted above the mains phase to phase peak voltage. The low frequency voltage ripple is small and it could be neglected compared to that of the diode rectifier. A variant of the CCM boost rectifier is discontinuous conduction mode (DCM) boost rectifier [52]-[55]. This topology offers lower THD of the input current than CCM boost rectifier (10-15% in comparison to 30%).

A common disadvantage of the single-switch boost topologies is power rating of the semiconductor switches. The switches are rated for the full dc bus voltage and full rectifier current. Generally speaking, a semiconductor switches' performance; conduction and switching strongly depend on the switch voltage rating and the switch technology. Lower voltage rating means lower conduction losses, better switching performance, higher efficiency and lower cost. For example, let us consider a 400V three-phase rectifier. The dc bus voltage is 700 to 800V. For the ordinary single-switch boost converter, the switch and boost diode voltage rating is 1000V to 1200V. For this voltage rating, 1200V IGBT and 1200V fast diode are used. In this case, maximum switching frequency is limited by the switching performance of the IGBT and the diode. To reduce switching losses, soft switching techniques can be used [56]-[58]. However, the soft switching techniques require additional active switches, diodes and passive resonant circuits, which make the circuit more complex and expensive.

Double-boost rectifiers employ two interleaved active switches and boost diodes. The switches and diodes are rated for half dc bus voltage and full rectifier current. As a result, the conversion losses are slightly lower in comparison to the single-switch boost rectifier [59]. The boost inductor is approximately 25% that of the single-switch topology.

A dc side shunt active filter, applied on a single-phase diode rectifier has been analysed in [60]. The filter circuit is connected on the rectifier dc side, and as such it is simple and cost effective in comparison to the state of the art ac side connected active filters. This approach could be extended to three-phase rectifiers, wherein the input current THD can be

reduced to approximately 30%. The main disadvantage of such a filtering concept is high current stress and low efficiency. The first reason for this is an additional diode in the main current path. The current that circulates between the dc filter and dc bus capacitor is a few time greater than the mains current. Hence, losses of the filter and dc bus capacitor are significant.

The electronic smoothing inductor (ESI) has been proposed and analysed in [61]-[63]. An auxiliary low voltage dc-dc converter is serially connected between the rectifier and the dc bus capacitor. The rectifier current is actively controlled to be constant or pseudo-constant. The input current THD is approximately 30%, the same as that of the CCM single-switch boost rectifier. A key advantage of the ESI concepts is that the auxiliary dc-dc converter is rated on full current and a fraction (normally 20%) of the dc bus voltage. Hence, the auxiliary converter losses are quite small. The entire rectifier efficiency can go above 98% [63]. The main disadvantage of the ESI is that the dc bus average voltage is not controlled and it is slightly lower than the rectifier average voltage.

The concept of a third harmonic injection method for three-phase diode rectifiers is well presented in monograph [64]. Although the harmonic injection method is simple, it does not have broad application in conventional industrial rectifiers. The main reason for this lays in the need for bulky passive elements, mainly coupling transformers. The overall efficiency is not sufficiently high as required by the applications.

Single-phase supplied three-phase controlled electric drives and related application issues are not often treated in the literature. Single-phase supplied rectifier with passive LC dc bus filter and three-phase pulse width modulated (PWM) inverter is the most common solution in low power low cost applications. The dc bus capacitor is a large electrolytic capacitor, while the inductor is small or even absent. Such a rectifier works as peak detecting circuit; the dc bus voltage is charged to the peak mains voltage and the mains current is a train of narrow pulses. Apart the fact that such a rectifier is simple, cost effective and robust, the drive manufactures do not recommended it because of a few serious limitations:

-The input current is distorted, with peaks that are 5 to 10 times of the fundamental RMS current. The total harmonic distortion factor is as high as 150%, or even higher. The power factor is low.

-A bulky dc bus capacitor is necessary to keep the dc bus voltage ripple acceptably low.

-A filter inductor must be used to limit peak of the input current. The inductance value is however limited because the dc bus voltage quickly decays with the inductance.

-The dc bus voltage is reduced in comparison to three-phase supplied drive. Hence, available motor voltage is reduced too.

-The drive life time is limited by the dc bus capacitor life time (the capacitor is the most stressed component).

-The drive may be de-rated by 50% when single-phase supplied, which means higher installation cost per kW.

Single-phase single-switch and double-boost rectifier is the most popular solution in applications that require boosted dc bus voltage and sinusoidal or pseudo-sinusoidal input current, [65], [66]. This topology is often used in low power supplies such as PC and small telecom supplies. In variable speed drives, however, this is rarely used topology because cost, size and efficiency.

Split-capacitor three-leg rectifier/inverter is used in low cost low power variable speed drive applications, such as air-conditioning and home appliance applications [67], [68]. This topology offers the lowest count of the active and passive components in comparison to the other solutions. However, two drawbacks make this topology inappropriate in high power industrial applications; 1) The dc bus capacitor current stress at low frequency, and 2) the output current ripple.

1.2.4. Smoothing of the Input Peak Power

The problem of the peak power filtering and voltage fluctuation in weak distribution supply in public transportation is briefly analysed in [14]. The peak power and braking issue in lift application has been analysed [15]. Ultra-capacitor based energy storage has been proposed as a solution. Control aspects have been briefly presented in [14].

1.3. The Dissertation Objective

The objective of this dissertation is to identify and discuss some of the remaining technical issues in application of advanced controlled electric drives. Then, a solution or set of solutions for the problems that are identified have to be proposed, analysed, discussed and validated by simulation and set of experiments. Three sub-objectives can be summarized as follows.

1.3.1. Parallel Connection of Energy Storage Device and Controlled Electric Drive

The first objective is to analyse the existing solutions of parallel connected energy storage device and controlled electric drive. The system operating modes have to be analysed in details and critical points clearly identified. Important properties of the ultra-capacitor as energy storage device for power conversion application have to be discussed too. Then, an appropriate topology of the interface dc-dc converter has to be proposed. Finally, the entire conversion system should be modelled and a new control scheme proposed. The proposed solution(s) has to be competitive with state of the art solutions regarding efficiency, cost, size of active and passive components and heat sink, and dynamic performances of the dc bus voltage control, the ultra-capacitor state of the charge control and the ultra-capacitor current control.

1.3.2. The Mains Current Harmonics, DC Bus Voltage Control and Single Phase Supply

State of the art solutions of three-phase diode boost rectifiers have to be analysed and disadvantages clearly identified. A new topology for three-phase diode boost rectifier has to be proposed, analysed, discussed and verified by simulations and set of experiments. The proposed solution(s) has to be competitive with state of the art solutions regarding efficiency, size of passive components including heat sink, cost and dynamic performances of the voltage and rectifier current control.

1.3.3. Energy Storage and Power Factor Correction Device for Electric Drive Applications

Last but not least is to merge the solutions of 1.3.1 and 1.3.2 into one generic solution that intents to solve all the six technical issues mentioned in section 1.1.4. Analyses, discussion and verification by simulations and experiments have to be done. The solution has to be competitive with state of the art solutions regarding efficiency, size, cost and dynamic performances of the overall system.

1.4. The Dissertation Organization

The dissertation is organised in five parts. Each part presents one or set of similar technical problems as well as a new solution for those problems. Each part consists of one or more logically organised chapters.

1.4.1. Part One: General Introduction

In the first part, a general introduction is given. Background of controlled electric drives is given, typical applications of controlled electric drives are discussed and remaining applications issues are identified. An overview of the literature is given, and objectives of the dissertation are also given.

1.4.2. Part Two: Parallel Connected Energy Storage Device for Controlled Electric Drives

In the second part of the dissertation, the ultra-capacitor as an energy storage device for advanced power conversion application is discussed. Then, the concept of parallel-connected energy storage device for controlled electric drives is presented and discussed. The presented solution solves the first two technical issues mentioned in the introduction; 1) saving of the drive braking energy and 2) Extension of the drive ride-through time.

The ultra-capacitor as an energy storage device is discussed in chapter 2. The basic operating principle of the ultra-capacitors is described. As an electric device, the ultra-capacitor can be modeled for two purposes; analysis of the electric circuit dynamic behavior (analysis and synthesis of the control) and thermal behavior of the ultra-capacitor. Those two modeling aspects are discussed in the second part of chapter 2. Finally, the ultra-capacitor losses versus frequency of the excitation current are discussed and losses model is proposed.

In chapter 3, a controlled regenerative electric drive using the ultra-capacitor as energy storage device is discussed. The basic operating modes are described. Then, the ultra-capacitor design and selection guidelines are given. The conversion losses and efficiency versus size of the ultra-capacitor are discussed. The system cost versus the conversion efficiency is also briefly discussed.

Chapter 4 presents a three-level dc-dc converter that is employed as a link between the variable speed drive and the ultra-capacitor. The converter operating principle is discussed and advantages of such a topology are clearly identified. Design guidelines are given. Finally, a design example is presented at the end of the chapter.

Modelling and control aspects are discussed in chapter 5. Firstly, some modelling technique theory is presented. Thereafter a non-linear and linearzed model of the dc-dc converter is developed. The dc bus circuit model is discussed too. Finally, a non-linear and

small signal linear model of the entire conversion system is developed. The model is verified by Matlab/Simulink simulations. In the second party of chapter 5, a new control scheme is presented and discussed. Control of the ultra-capacitor current and the voltage balancing error is presented. The presented control is experimentally validated. The results are discussed. Then, control of the ultra-capacitor voltage and the dc bus voltage is presented and analysed. The controllers' synthesis procedure is given in details. The designed control system is validated by simulations and set of experiments.

In chapter 6, the solution presented is compared with state of the art solutions. At first, concept of the ultra-capacitor based regenerative electric drive is compared to back-to-back and matrix converters. Then, the three-level dc-dc converter is compared with state of the art topologies. Three parameters are compared: 1) properties of the active switches (IGBTs and diodes), 2) properties of the passive components (the output filter inductor and input filter capacitor) and 3) the conversion losses. Control aspects are also discussed and compared.

1.4.3. Part Three: Three-terminal Power Factor Correction and Voltage Control Device

In the third part, the three-terminal power factor and the dc bus voltage control device is presented is discussed. The presented solution solves the following three technical issues: 1) the mains current harmonics, 2) the dc bus voltage control and 3) single-phase supply.

Background and state of the art of active rectifier topologies is given in chapter 7. A novel half-dc-bus-voltage rated boost rectifier is briefly presented.

The new half-dc-bus-voltage rated boost rectifier is presented in chapter 8. Structure of the topology is analysed in detail. A design example is given and the new topology is experimentally validated. The results are discussed.

Modelling and control aspects of the new topology are discussed in chapter 9. Nonlinear and small signal models are developed. Those models are verified by Matlab/Simulink simulations. The control scheme is given and the controllers' synthesis procedure discussed.

Single phase operation of the presented boost rectifier is analysed in chapter 10. Critical design points are discussed.

Chapter 11 is gives a comparison of the presented boost rectifier versus state of the art solutions.

1.4.4. Part Four: Three-terminal Energy Storage and PFC Device for Controlled Electric Drives

In the fourth part, a three-terminal energy storage and PFC device for controlled electric drives is presented and discussed. The presented solution intents to solve all six technical issues mentioned in the introduction: 1) Saving and recovery of the drive braking energy, 2) Extension of the drive ride-through time, 3) The mains current harmonics, 4) The dc bus voltage control, 5) Single-phase supply and 6) The mains peak power shaving function.

In chapter 12, the concept of the three-terminal energy storage and PFC device for controlled electric drives is discussed and necessary theoretical analysis is given. Some aspects of the system design are given.

Modelling aspects and control scheme are discussed in chapter 13. The entire power conversion system consisting of the input boost rectifier, dc link, the ultra-capacitor interface dc-dc converter and the PWM inverter is modelled. Then, a new control scheme is proposed. The control scheme is validated by Matlab/Simulink simulation and set of experiments performed on a laboratory industrial prototype. The results are presented and discussed in chapter 14.

1.4.5. Part Five: Concluding Remarks and Conclusions

The dissertation work and contribution are discussed in chapter 15. Final concluding remarks and perspectives are given in chapter 16.

PART TWO: PARALLEL CONNECTED ENERGY STORAGE DEVICE FOR CONTROLLED ELECTRIC DRIVES

2. AN ULTRA-CAPACITOR AS ENERGY STORAGE DEVICE FOR POWER CONVERSION APPLICATIONS

2.1. The Ultra-Capacitors

An electric capacitor is a passive dynamic one-terminal electric device. In this context, dynamic means the device terminal voltage to current ratio is not a constant and linear. The voltage and current are linked via a differential equation which is in the general case a nonlinear equation. As that, the electric capacitor has capability to store energy as electric charge, more precisely as electric field between the capacitor plates. There are three different types of capacitors, namely electrostatic, electrolytic and electrochemical capacitors. In this dissertation, the electrochemical capacitors, so-called the ultra-capacitors are considered only.

Ultra-capacitors are different from the other type of capacitors mainly because their specific capacitance, [F/dm^3] and energy density, [kJ/dm^3] are several orders of magnitudes larger than that of electrolytic capacitors. In comparison to electrochemical batteries, the energy density is lower while the power density is larger than that of conventional batteries. Cycling capability is also significantely better compared to batteries. TABLE 2-1 compares the most important properties of the ultra-capacitor versus batteries and other type of capacitors.

TABLE 2-1: Properties of the existing energy storage devices.

	Capacitors	Ultra-capacitors	Electro-chemical batteries
Energy density [Wh/kg]	~0.1	1-6 (*)	~100
Peak power density [kW/kg]	10^4	2-20	0.1-0.5
Number of cycle	10^{10}	10^6	~10^3
Life time [years]	~10	~15	~5

* Based on technological trends, the energy density will in near future be increased by a factor of 10 or more.

2.1.1. Short History of the Ultra-capacitors

The double-layer capacitor effect was discovered and described by Helmholtz in 1879 [69]-[73]. Almost a century after that, a first ultra-capacitor was patented by Standard Oil Company in 1966. A decade after NEC developed and commercialized this device in 1978 [69]-[73]. The first high power ultra-capacitor was developed for military applications by the Pinnacle Research Institute in 1982 [69]-[73]. Ten years after, in 1992, the Maxwell Laboratory had started development of DoE ultra-capacitors for hybrid electric vehicles. Today, the ultra-capacitors are commercially available from a number of manufacturers [74].

Today, the ultra-capacitors are composed of two electrodes separated by a porous membrane, the so-called a separator. The separator and the electrodes are impregnated by a solvent electrolyte. The electrodes are made of porous material such as activated carbon or

carbon nano-tubes [69]-[73]. Typical specific surface area of the electrode is about 2000m^2/g. Such a large surface area and very thin layer of the charges, in order of *nm* gives specific capacitance of up to 250F/g [69]-[73]. Rated voltage of the ultra-capacitor cell is determined by the decomposition voltage of the electrolyte. Typical cell voltage is 1 to 2.8V, depending on the electrolyte technology [69]-[73]. To obtain higher working voltage, which is determined by the application, a number of cells must be series-connected into one capacitor module.

Ultra-capacitors as energy storage devices have found very wide application in power conversion due to their advantages over the conventional capacitors and electro-chemical batteries; high energy and power density, high efficiency, high cycling capability and long life.

2.1.2. Overview of Different Technologies

Fig. 2.1 shows taxonomy of the existing types of electrochemical capacitors. Whole family of the ultra-capacitors can be divided into two groups: electric double layer capacitors (EDLC) and pseudo-capacitors. A combination between the EDLC and pseudo-capacitors is group of hybrid capacitors. The EDLC group consists of three-subgroups; activated carbon, carbon nano-tubes and carbon aero gels. In this dissertation, application of activated carbon EDLC is discussed.

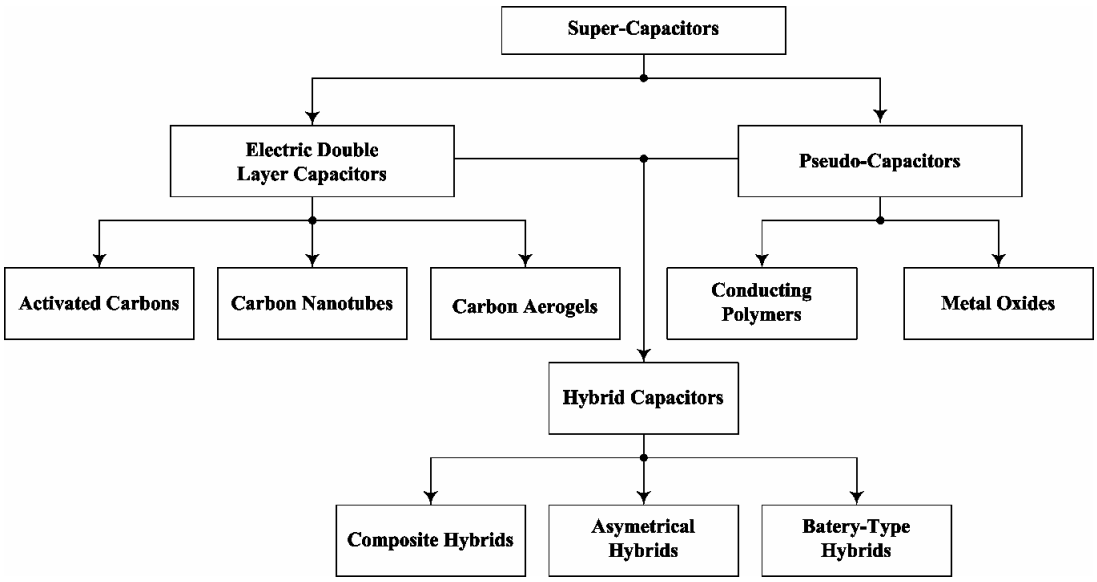


Fig. 2.1 Taxonomy of the ultra-capacitors.

2.1.3. Electric Double Layer Capacitors -EDLC

2.1.3.1. The Ultra-capacitor Structure

In order to increase the capacitance of anultra-capacitor, it is necessary to maximize contact surface are. To achieve this without increaseing in the capacitor volume, one must use a special material for the electrode. This material must have a porous structure and consequently a very high specific surface. The most frequently used material is activated carbon or carbon nano-tubes. In both cases, the specific surface may be as high as 1000m^2/g

to 3000m^2/g. The simplified structure of super-capacitor cell is depicted in Fig. 2.2. The elementary capacitor cell consists of positive and negative current collectors, positive and negative porous electrodes made of activated carbon which are attached on the current collectors, and a separator between the porous electrodes. The separator is material transparent to ions but an insulator for direct contact between the porous electrodes.

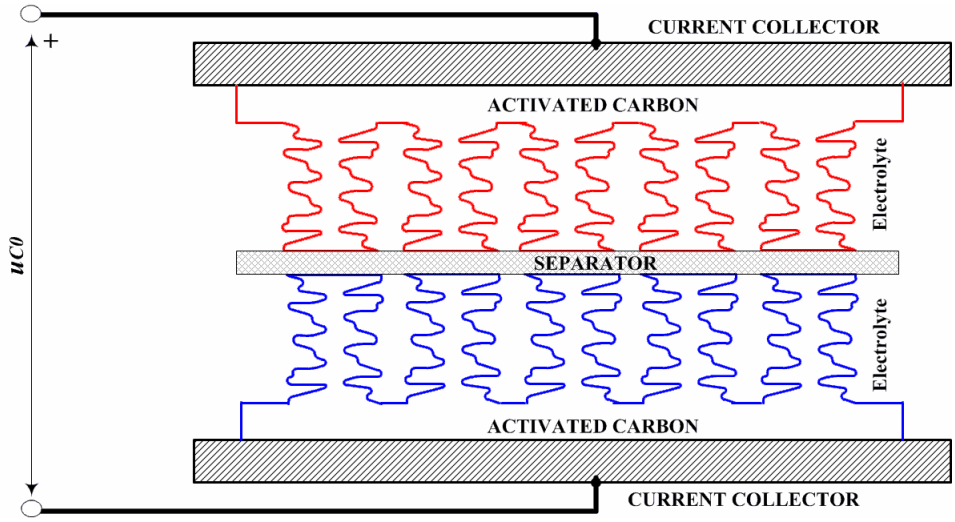


Fig. 2.2 Construction of an electrochemical double layer capacitor with porous electrodes (activated carbon).

Since the first development of double layer capacitors, there have been several iterations and models of the basic structure.

The very first work on double layer capacitors was carried out by Helmholtz in 1853. He supposed that the layer in an electrolyte is a single layer of the electrolyte molecules attached to the solid electrode, Fig. 2.3 (a).

The specific capacitance of such a structure is

$$c' = \frac{\varepsilon}{d}, \tag{2.1}$$

where ε is the solvent electrolyte permittivity and d is thickness of the layer, which equals to the molecule diameter.

The specific capacitance is overestimated compared to the experimentally obtained value. For aqueous electrolyte with ε_R=78 and d=0.2nm, equations (2.1) gives 340μF/cm^2, what is much greater than the measured value 10μF/cm^2 to 30μF/cm^2. Also, the model does not take in account that the capacitance is voltage dependent.

In order to describe voltage dependence of the capacitance, Gouy introduced a theory of random thermal motion in 1910, and considered a space distribution of the charge in the electrolyte in proximity of theboundary between the electrolyte and electrode, Fig. 2.3 (b). A few years later, Chapman defined the charge distribution in the electrolyte as a function of linear distance and properties of the electrolyte. The specific capacitance is estimated as

$$c' = z\sqrt{\frac{2q^2 n_0 \varepsilon}{kT}} ch\left(\frac{z\Psi_M q}{2kT}\right), \tag{2.2}$$

where q is elementary charge, n_0 is the concentration of anions and cations, z is the valence electrolyte ions, ε is the electrolyte permittivity, k is Bolzman' constant, and T is the temperature.

In the model, the charge is considered as point charge (charge density is Dirac function of space). Thus, the specific capacitance is over-evaluated.

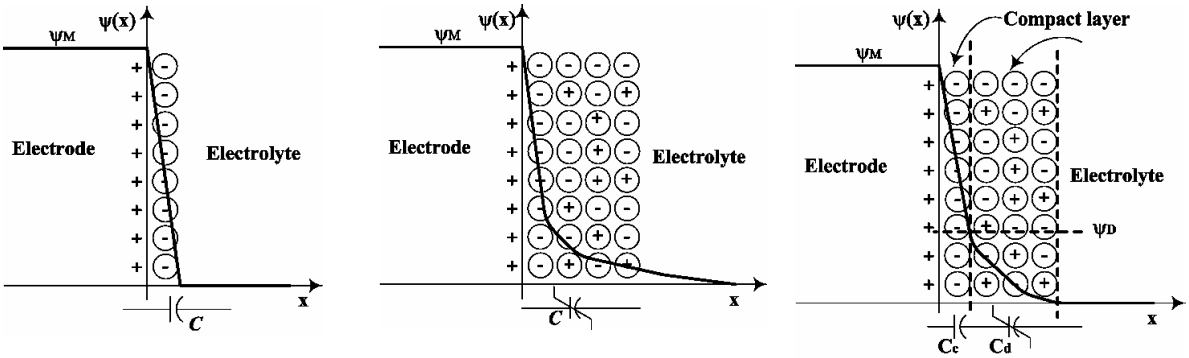


Fig. 2.3 a) Helmholtz's model of a DLEC (1857). b) Gouy and Chapman's model (1910 and 1913). C) Stern's model (1924).

In 1924 Stern proposed new model which improved Gouy and Chapmen's models. He introduced the real dimension of solvent molecules and then divided the space charge into two layers; compact layer and diffused layer, Fig. 2.3 (c).

Total specific capacitance is estimated as

$$c' = \frac{c'_C c'_D}{c'_C + c'_D}, \tag{2.3}$$

where c'_C is the compact layer capacitance, and c'_D is the diffused layer capacitance defined as

$$c'_D = z\sqrt{\frac{2q^2 n_0 \varepsilon}{kT}} ch\left(\frac{z\Psi_D q}{2kT}\right). \tag{2.4}$$

2.2. The Ultra-capacitors Macro (Electric Circuit) Model

In this section, the ultra-capacitor macro model is analysed and discussed. The ultra-capacitor macro model is used for the conversion system control analysis and design, as well as evaluation of the ultra-capacitor losses and temperature in different operating modes.

2.2.1. Full Theoretical Model

The traditional model consists of an ideal linear capacitor and equivalent series resistance (ESR). This simple model cannot be used in a super-capacitor model because two

phenomena: (1) the capacitance is voltage dependent, and (2) the time/space redistribution of the charge due to porosity of the activated carbon electrodes. The porous electrode structure behaves as a nonlinear transmission line, [75]-[77]. It is known from theory of electric circuit that an electrically short transmission line can be approximated with N^{th} order *RLCG* ladder network. At low frequency, below 100 Hz, distributed serial inductance L can be neglected [77]. Distributed conductance G can be neglected too, except if long term steady state analysis is needed. Thus, an approximated model of an ultra-capacitor having porous electrodes is serial connection of two *RC* leader networks of N^{th} order, the separator resistance R_{SP} and the current collector resistances R_{CP} and R_{CN}. A schematic diagram of the approximated model is given in Fig. 2.4.

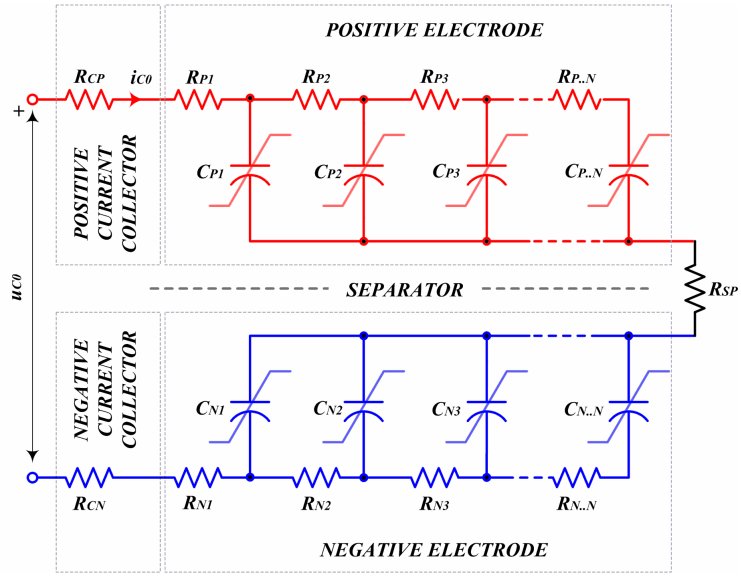


Fig. 2.4 An approximated model of the electrochemical double layer capacitor taking in the account porosity of the electrodes.

The resistors R_{P1}…..$R_{P..N}$ and R_{N1}…..$R_{N..N}$ are the resistances of positive and negative porous electrode respectively. For more accurate modeling of the ultra-capacitor, the fact that these resistances are nonlinear and depend on the capacitor voltage must be taken into account. Nonlinear capacitances C_{P1}…..$C_{P..N}$ and C_{N1}…..$C_{N..N}$ are the positive and negative porous electrode capacitances.

The voltage dependent capacitances C_{P1}…..$C_{P..N}$ and C_{N1}…..$C_{N..N}$ can be approximated by first order functions of the voltage across each cell,

$$\begin{bmatrix} C_{P1} \\ C_{P2} \\ \\ C_{P..N} \end{bmatrix} = \begin{bmatrix} C_{0P1} \\ C_{0P2} \\ \\ C_{0P..N} \end{bmatrix} + \begin{bmatrix} K_{CP1} & 0 & 0 & 0 \\ 0 & K_{CP2} & 0 & 0 \\ 0 & 0 & & 0 \\ 0 & 0 & 0 & K_{CP..N} \end{bmatrix} \begin{bmatrix} u_{CP1} \\ u_{CP2} \\ \\ u_{CP..N} \end{bmatrix}, \tag{2.5}$$

$$\begin{bmatrix} C_{N1} \\ C_{N2} \\ \\ C_{N..N} \end{bmatrix} = \begin{bmatrix} C_{0N1} \\ C_{0N2} \\ \\ C_{0N..N} \end{bmatrix} + \begin{bmatrix} K_{CN1} & 0 & 0 & 0 \\ 0 & K_{CN2} & 0 & 0 \\ 0 & 0 & & 0 \\ 0 & 0 & 0 & K_{CN..N} \end{bmatrix} \begin{bmatrix} u_{CN1} \\ u_{CN2} \\ \\ u_{CN..N} \end{bmatrix}. \tag{2.6}$$

The coefficients $K_{CN1}….K_{CP..N}$ models the voltage dependency of the capacitance due to the diffused layer. Voltages $u_{CN1}….u_{CP..N}$ are the voltage across each elementary capacitor cell.

Considering that the positive and negative electrodes are symmetric, the circuit in Fig. 2.4 can be reduced to a simple N^{th} order RC ladder network, depicted in Fig. 2.5.

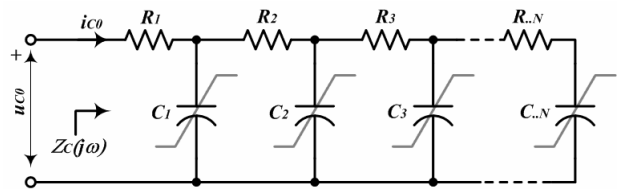


Fig. 2.5 N^{th} order equivalent model of an electrochemical double layer capacitor.

Resistances of the equivalent circuit in Fig. 2.5 are

$$\begin{bmatrix} R_1 \\ R_2 \\ \vdots \\ R_{..N} \end{bmatrix} = \begin{bmatrix} R_{CP} + R_{SP} + R_{CN} \\ 0 \\ \vdots \\ 0 \end{bmatrix} + \begin{bmatrix} R_{P1} \\ R_{P2} \\ \vdots \\ R_{.P.N} \end{bmatrix} + \begin{bmatrix} R_{N1} \\ R_{N2} \\ \vdots \\ R_{.N.N} \end{bmatrix}. \tag{2.7}$$

For simplicity of notation, we will use electrical elastance as inverse variable of capacitance to define the capacitances of the equivalent model,

$$\begin{bmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \vdots \\ \frac{1}{C_{..N}} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_{P1}} \\ \frac{1}{C_{P2}} \\ \vdots \\ \frac{1}{C_{P..N}} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{N1}} \\ \frac{1}{C_{N2}} \\ \vdots \\ \frac{1}{C_{.N.N}} \end{bmatrix}. \tag{2.8}$$

2.2.1.1. Ultra-capacitor Model in Frequency Domain

The circuit of Fig. 2.5 is a nonlinear circuit because the capacitances depend on the voltage. To develop a model in the frequency domain we have to linearize the nonlinear circuit. Expanding (2.5) and (2.6) into a Taylor series, taking just the zero order members and substituting them into (2.8) yields

$$\begin{bmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \vdots \\ \frac{1}{C_{..N}} \end{bmatrix} \cong \begin{bmatrix} \frac{1}{C_{0P1} + K_{CP1} \cdot U_{C01}} \\ \frac{1}{C_{0P2} + K_{CP2} \cdot U_{C02}} \\ \vdots \\ \frac{1}{C_{0P..N} + K_{CP..N} \cdot U_{C0..N}} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{0N1} + K_{CN1} \cdot U_{C01}} \\ \frac{1}{C_{0N2} + K_{CN2} \cdot U_{C02}} \\ \vdots \\ \frac{1}{C_{0N..N} + K_{CN..N} \cdot U_{C0..N}} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_{01} + K_{C1} \cdot U_{C01}} \\ \frac{1}{C_{02} + K_{C2} \cdot U_{C02}} \\ \vdots \\ \frac{1}{C_{0..N} + K_{C..N} \cdot U_{C0..N}} \end{bmatrix}. \tag{2.9}$$

Now, having a linearizerd mode of the super capacitor ladder network and using the N Extra Element theorem [76] one can develop the ultra-capacitor input impedance $Z_{C0}\omega)$. Since the capacitances are voltage dependent, the developed impedance is a small signal impedance, which is valid just in proximity of the capacitor voltage operating point U_{C0}.

$$Z_{C0}(j\omega)\Big|_{u_C=U_{C0}} = R_{C0}(\omega)\Big|_{u_C=U_{C0}} + \frac{1}{j\omega C_C(\omega)\Big|_{u_C=U_{C0}}} \tag{2.10}$$

As one can see from equation (2.10), the super-capacitor equivalent series resistance R_{C0} and equivalent capacitance C_C are frequency dependent properties. The resistance and capacitance are defined for zero frequency (DC operational mode) and high frequency as

$$\begin{aligned} \lim_{\omega\to 0} C_C(\omega)\Big|_{u_C=U_{C0}} &= \sum_{i=1}^{N} C_i\,, \\ \lim_{\omega\to \infty} C_C(\omega)\Big|_{u_C=U_{C0}} &= C_1\,, \end{aligned} \tag{2.11}$$

$$\begin{aligned} \lim_{\omega\to 0} R_{C0}(\omega)\Big|_{u_C=U_{C0}} &= \sum_{i=1}^{N} R_i\,, \\ \lim_{\omega\to \infty} R_{ESR}(\omega)\Big|_{u_C=U_{C0}} &= R_1\,. \end{aligned} \tag{2.12}$$

To illustrate these properties, a 2500F/2.5V ultra-capacitor cell has been modelled as a 5^{th} order *RC* ladder network . The super-capacitor parameters are given in TABLE 2-2.

TABLE 2-2: Simulated parameters of a 2500F/2.5V ultra-capacitor at U_{C0}=1V. The capacitance C in [F] and the resistance R in [Ω].

R_1	C_1	R_2	C_2	R_3	C_3	R_4	C_4	R_5	C_5
0,324E-04	23,2	0,0324E-06	211	55,4E-06	235	88,4E-06	699	0,389E-04	1172

The magnitude and phase of the capacitor input impedance are plotted in Fig. 2.6 (a) and Fig. 2.6 (b). From this plot one can see that the ultra-capacitor behaves as a pure capacitor in the very low frequency range, up to 20mHz. In the high frequency range, let say above 10Hz, the ultra-capacitor bank behaves as a pure resistor. In the mid-frequency range, it behaves as a RC element.

The equivalent serial resistance and capacitance versus frequency were calculated and plotted in Fig. 2.6 (c) and Fig. 2.6 (d). Both resistance and capacitance decrease with frequency. The resistance is high and constant at low frequency up to 200mHz, and then decreases to a minimum value at frequencies above 10Hz. Ratio max/min resistance is approximately 1.6. The equivalent capacitance varies in the same frequency range as the resistance. The ratio max/min capacitance is approximately 10. In the following section we will discuss these properties in more detail.

2.2.1.2. The ESR versus Frequency

As already mentioned, the ultra-capacitor is not an ideal loss-free device. Whenever current flows through the capacitor, regardless on the conversion process and power flow

direction, an amount of energy is wasted as the Jule's energy. This is due to the resistance of the ultra-capacitor collectors, porous electrodes, separator and electrolyte. The quantity of energy wasted generally depends on the resistance and current. In power applications, the capacitor current is a varying quantity, depending on charge/discharge cycle. In addition, the capacitor current containes a high frequency component due to switch mode operation of the power conversion unit which charges/discharges the ultra-capacitor. The capacitor current spectra falls in range from, let say mHz up to kHz or tens of kHz. As the equivalent resistance is frequency dependent, the contribution of each spectral component on the losses is different. This is discussed in section 2.4.

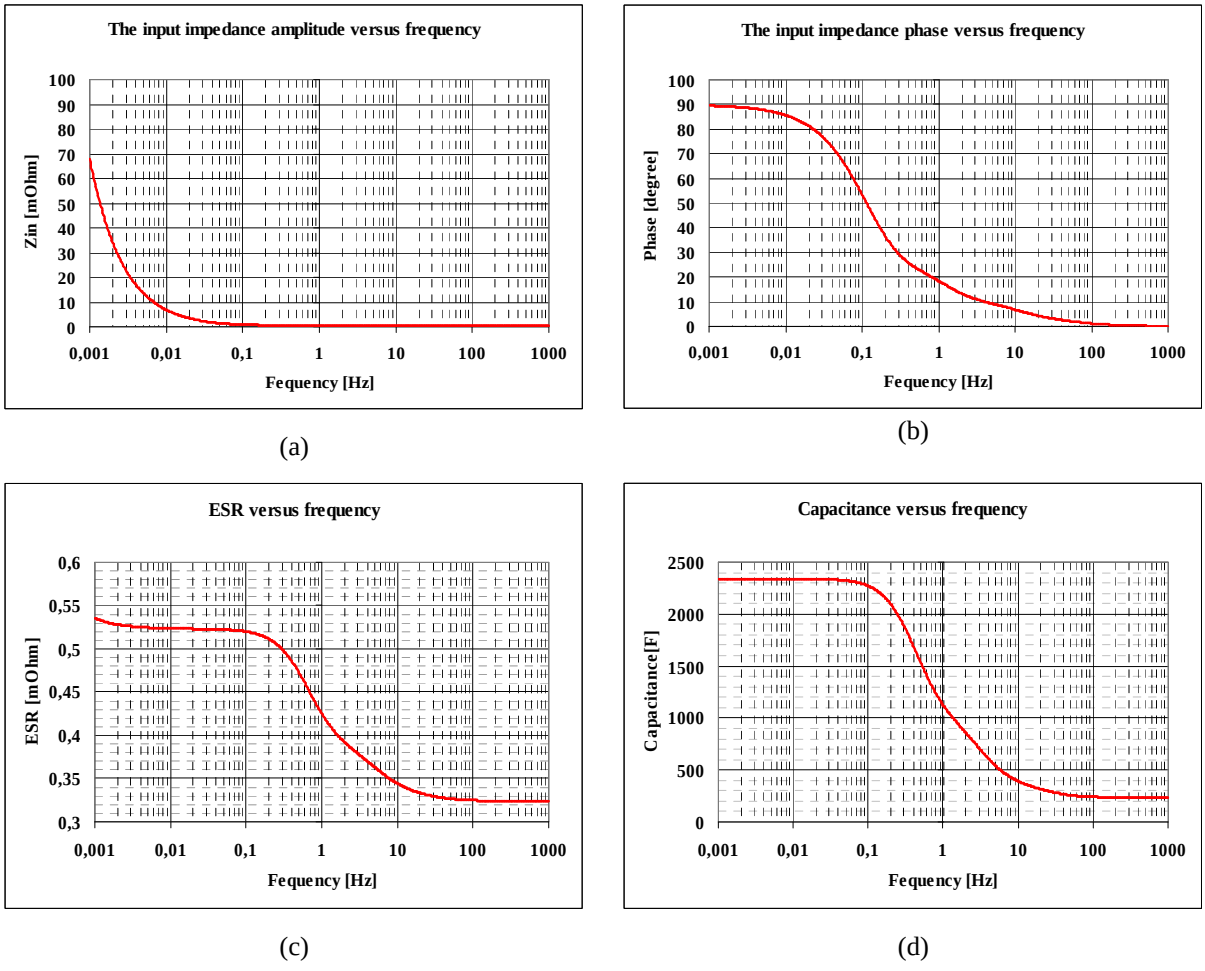


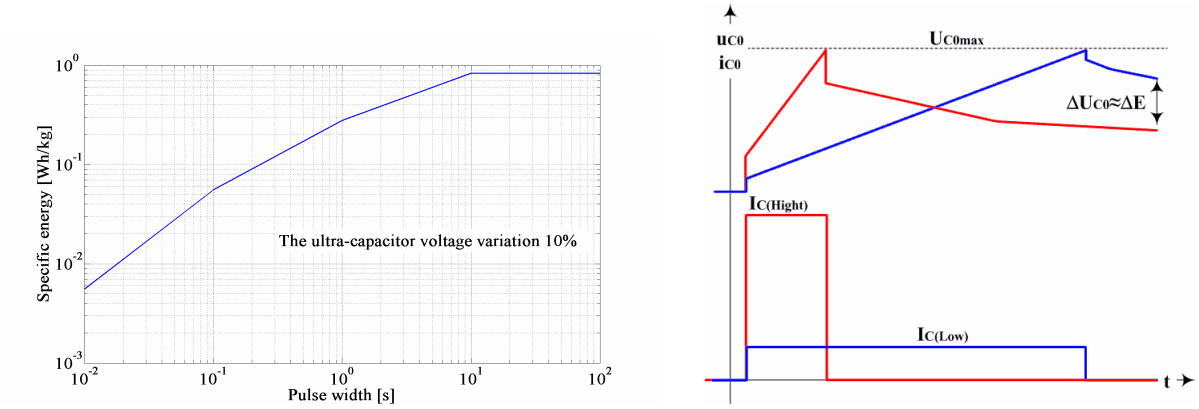
Fig. 2.6 The ultra-capacitor input impedance versus frequency. a) Amplitude, b) phase, c) the equivalent series resistance and d) the capacitance. The ultra-capacitor is 2500F/2.5V cell.

2.2.1.3. The Capacitance versus Frequency

The capacitance varies more significantly with frequency than the resistance. The factor C_{MAX}/C_{MIN} could be up to 10 or more. What are typical implications of this in real power application application? The capacitance variation with frequency means that one needs certain time to store the required energy in the capacitor. If one charges the capacitor with high power, close to maximum, the capacitor voltage will increase fast, and reach the maximum voltage before the capacitor is fully charged. Thus, the full energy capability of the capacitor is not used. In contrast to this, if one charges the capacitor with low power, the voltage increases slowly and the charge is distributed over the entire capacitor. Once the

voltage reaches maximum voltage, the capacitor is fully charged, and the energy capability is maximized. From this short discussion one can conclude that the total capacitance is available only at very low frequency, and consequently light load.

Fig. 2.7 (a) shows the dynamic specific energy versus pulse width. The ultra-capacitor voltage charge/discharge variation is 10% of the rated voltage. Notice that the specific energy (energy capability) decreases as the pulse width decreases. Variation of the energy capability is due to the frequency dependent capacitance which is caused by the relaxation phenomenon in the porous electrodes [69], [76]. There is another factor that limits the ultra-capacitor energy capability. That is voltage drop of the electrode and separator resistance, and porous electrode resistance close to the input. Fig. 2.7 (b) illustrates two different cases. The red plot illustrates the charging process with relatively high charging current, while the blue waveforms illustrate charging process with current, 10% of the previous. This issue could be solved by the control of charge/discharge process, wherein the real capacitor voltage is estimated from the capacitor model and measured input voltage and current.



(a) (b)

Fig. 2.7 Illustration of the effect of the ultra-capacitor frequency dependent capacitance on energy storage capability. a) Effective specific energy versus charging/discharging pulse width, and b) time diagrams for two different cases, short pulse and long pulse.

The charge criterion is the voltage across the capacitor terminals, which should not be higher than U_{C0max}. The difference between the steady state voltages U_{C01}, U_{C02} represents the difference in the stored energy in the ultra-capacitor for different charging speeds. Considering a linear capacitor with frequency dependent capacitance, one can estimate the difference in energy stored as ΔE.

$$\Delta E = \frac{1}{2} C_0 \Delta U_{C0}^2 \left(1 + \frac{2U_{C01}}{\Delta U_{C0}} \right), \tag{2.13}$$

where ΔU_{C0} strongly depends on the time profile of the charging current.

2.2.2. Simplified Model

For simplicity of the following analysis, a first order nonlinear model of an ultra-capacitor is used. The model takes in account the linear (voltage independent) internal resistance R_{C0} and total capacitance as a function of the capacitor voltage. Effects of the

transmission line are neglected. The internal equivalent resistance R_{C0} is modelled as a constant and frequency independent resistance. Fig. 2.8 depicts a simplified model of ultra-capacitor used in the analysis. The equivalent capacitor consists of a linear capacitor C_0 and parallel connected voltage dependent capacitor $C(u_C)$.

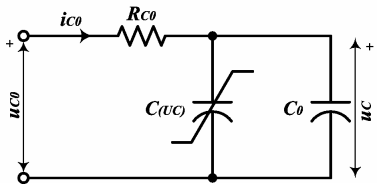


Fig. 2.8 Simple RC model of the ultra-capacitor.

The total capacitance of an ultra-capacitor is voltage controlled capacitance defined as

$$C(u_C) = C_0 + k_C \cdot u_C , \tag{2.14}$$

where C_0 is initial linear capacitance which represents electrostatic capacitance of the capacitor, and k_C is a coefficient which represent the effects of the diffused layer of the super-capacitor. In case of a hybrid super-capacitor, the coefficient models the Faradic effect and electrochemical processes on one side of the capacitor [69].

The capacitor current defined is

$$i_C = \frac{\partial Q}{\partial t} = \left(C(u_C) + u_C \frac{dC(u_C)}{du_C} \right) \frac{du_C}{dt} = C_I(u_C) \frac{du_C}{dt} . \tag{2.15}$$

The capacitance denoted as $C_I(u_C)$ is a virtual capacitance, the so-called current capacitance. Substituting (2.14) in (2.15) yields

$$C_I(u_C) = C_0 + 2k_C \cdot u_C \text{ and } i_C = (C_0 + 2k_C \cdot u_C) \frac{du_C}{dt} . \tag{2.16}$$

2.2.3. The Ultra-capacitor Energy Capacity

Energy stored in the ultra-capacitor charged to a voltage u_C is

$$E_C(u_C) = \frac{1}{2} \left(C_0 + \frac{4}{3} k_C u_C \right) u_C^2 = \frac{1}{2} C_E(u_C) u_C^2 . \tag{2.17}$$

The capacitance denoted as $C_E(u_C)$ is the so-called energetic capacitance.

The energy available from the ultra-capacitor discharged from the initial voltage U_{C0max} to the final voltage U_{C0min} is

$$\Delta E_C = \frac{C_0}{2} \left(U_{C0\max}^2 - U_{C0\min}^2 \right) + \frac{2}{3} K_C \left(U_{C0\max}^3 - U_{C0\min}^3 \right) . \tag{2.18}$$

This equation will be used to compute the energy that can be stored and restored from the ultra-capacitor in real applications. For example, it could be braking energy or ride-

through energy in variable speed drive systems. This will be discussed in more detail in chapter 3.

2.3. The Ultra-capacitor Charge/Discharge Methods

Theoretically, four different power conversion modes are possible; constant voltage, constant resistance, constant current and constant power conversion mode. The first one is not applicable because the ultra-capacitor is some kind of voltage source with an internal resistance. The most important characteristics of the other three conversion methods are briefly discussed in the following section.

2.3.1. Constant Resistive Load

Constant resistive load is the simplest charge/discharge method. The capacitor is charged from voltage source V_{BUS} via a charge resistor R_0 and discharged in the load resistor R_0. However, because low conversion efficiency this method is rarely used in power applications, and therefore will not be discussed.

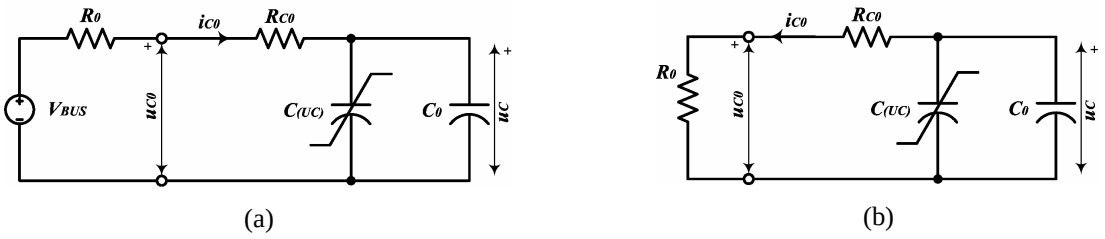


Fig. 2.9 The ultra-capacitor resistive power conversion. a) Charging, and b) discharging.

2.3.2. Constant Current

The ultra-capacitor can be charged/discharged with a constant current load/source. Constant current load/source is often found in regulated power converters, such as regulated chargers and constant torque driven electric motors.

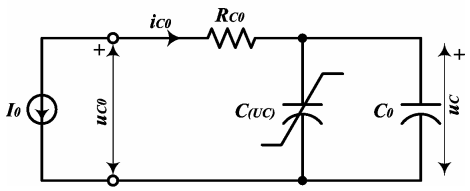


Fig. 2.10 Charging/discharging the ultra-capacitor with a constant current source.

2.3.2.1. Discharging

Let the ultra-capacitor initial voltage be U_{C0} and the ultra-capacitor, and assume the ultra-capacitor is being discharged by constant current I_0. The capacitor internal voltage declines as

$$u_C(t)=\sqrt{\frac{C_0^2}{4k_C^2}+\frac{1}{k_C}\left(U_{C0}C_0+U_{C0}^2k_C-I_0t\right)}-\frac{C_0}{2k_C}\text{.....}0<t<T_{DIS}\,, \tag{2.19}$$

where the discharge time is

$$T_{DIS}=\frac{1}{I_0}\left(C_0U_{C0}+k_CU_{C0}^2\right). \tag{2.20}$$

2.3.2.2. Maximum Discharge Power

Maximum power delivered to the load is limited and defined by the capacitor internal resistance R_{C0},

$$P_{0MAX}=\frac{u_C^2}{4R_{C0}}\,. \tag{2.21}$$

The current I_0 is limited and depends on the capacitor voltage u_C and the internal resistance R_{C0}.

$$0\le I_0\le I_{0MAX}\quad\text{where}\quad I_{0MAX}=\frac{u_C}{R_{C0}} \tag{2.22}$$

If the current exceeds the limit, the capacitor terminal voltage u_{C0} becomes negative and the load changes in the nature and turns to be a source. However, the capacitor is still being discharged. All energy recovered from the capacitor and energy delivered from the current source is dissipated in the capacitors internal series resistance R_{C0}.

2.3.3. Charging

The ultra-capacitor voltage during the charging process is

$$u_C(t)=\sqrt{\frac{C_0^2}{4k_C^2}+\frac{1}{k_C}\left(U_{C0}C_0+U_{C0}^2k_C+I_0t\right)}-\frac{C_0}{2k_C}\text{.....}0<t<T_{CH}\,. \tag{2.23}$$

The charge time is

$$T_{CH}=\frac{1}{I_0}\left(\frac{C_0^2}{4}-k_C\left(U_{0\max}-R_{C0}I_0+\frac{C_0}{2k_C}\right)^2-C_0U_{C0}-k_CU_{C0}^2\right), \tag{2.24}$$

where U_{0MAX} is the capacitor terminal voltage.

2.3.3.1. Maximum Charging Power

In charging mode the current I_0 is negative. Maximum current that can be injected into the ultra-capacitor is limitated by the capacitor terminal voltage U_{0MAX},

$$I_{0MAX} = \frac{U_{0MAX} - u_C}{R_{C0}}. \tag{2.25}$$

From (2.25) one can define maximum charging power as a function of the capacitor resistance and the capacitor voltage,

$$P_{0MAX} = \frac{U_{0\max}\left(U_{0\max} - u_C\right)}{R_{C0}}. \tag{2.26}$$

2.3.4. Constant Power

In power conversion applications, most of load and sources behave as constant power, either positive or negative. Typical examples of such constant power loads are power converters having regulated output voltage, such as pulse width modulated (PWM) variable speed drives and dc-dc converters. According to the convention on Fig. 2.11, power of the load is defined as $P_{C0} = -u_{C0}i_{C0}$, where power is positive in sink (load) mode and negative in source mode.

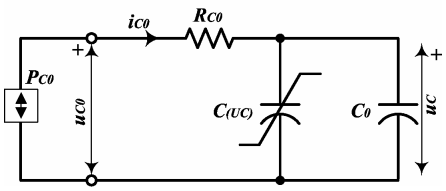


Fig. 2.11 Charging/discharging the ultra-capacitor with a constant power source.

2.3.4.1. Discharging

The circuit in Fig. 2.11 is described by the following differential equation,

$$P_{C0} = -C_0 \frac{P_{C0}^2}{i_{C0}^3}\frac{di_{C0}}{dt} + R_{C0}C_0^2\frac{P_{C0}^2}{i_{C0}^4}\left(\frac{di_{C0}}{dt}\right)^2, \tag{2.27}$$

where the ultra-capacitor is taken as a linear capacitor (k_C=0). If the ultra-capacitor is properly selected, the power P_{C0} is much lower than the matched maximum power, $P_{C0} << P_{\max} = u_C^2 / 4R_{C0}$, and therefore the ultra-capacitor resistance R_{C0} can be neglected in the analysis. From those two approximations one obtains the ultra-capacitor discharging current

$$i_{C0} \cong -\frac{|P_{C0}|}{U_C}\sqrt{\frac{C_0U_C^2}{C_0U_C^2 - 2P_{C0}t}}, \tag{2.28}$$

where the voltage U_{C0} is the ultra-capacitor initial voltage. The maximum discharge time is

$$t \le \frac{C_0U_{C0}^2}{2|P_{C0}|}. \tag{2.29}$$

2.3.4.2. Maximum Discharge Power

Just as in the case of current or resistive discharge, the capacitor maximum power is limited due to internal series resistance R_{C0}. The maximum power that can be delivered to the load having constant power characteristic is

$$P_{0MAX} = \frac{u_C^2}{4R_{C0}}. \tag{2.30}$$

Please note that the maximum power is defined by the capacitor voltage and R_{C0}, exactly as in the two previous two cases (constant resistance and constant current load). There is however an essential difference. If the load is higher than the maximum power at given the ultra-capacitor voltage, the system becomes unstable and the voltage collapses.

2.3.4.3. Charging

In the charging mode of an ultra-capacitor, the power of the power source P_{C0} is negative according to the notation in Fig. 2.11. Using the same method as we used before, but simply applying negative power, we obtain the ultra-capacitor charging current

$$i_{C0} \cong \frac{P_{C0}}{U_{C\min}} \sqrt{\frac{C_0 U_{C\min}^2}{C_0 U_{C\min}^2 + 2P_{C0}t}}, \tag{2.31}$$

where the initial ultra-capacitor voltage is $U_{C\min}$.

2.3.4.4. Maximum Charging Power

In charging mode the power P_{C0} is negative. Thus, the maximum power stability criteria is not applicable in this case. In other words, the system described by Fig. 2.11 is stable in charging mode regardless on the power P_{C0}. In a real application, however, there is another limitation that defines maximum power that can be transfered into the ultra-capacitor bank. It is the limitation of the power source maximum voltage U_{0MAX},

$$P_{0MAX} = \frac{U_{0MAX}\left(U_{0MAX} - u_C\right)}{R_{ESR}}. \tag{2.32}$$

2.4. Frequency Related Losses

As mentioned in section 2.2.1, the ultra-capacitor is a non-linear device, with voltage and frequency dependent properties. In this section, the effect of the frequency dependent resistance on the conversion losses is discussed.

One can distinguish two different frequency ranges in spectrum of the capacitor current. The first one is low frequency, which is related to the capacitor operational mode and cycle. The second one is high frequency current due to the nature of the power converter used to charge/discharge the ultra-capacitor. Low frequency current is normally aperiodic, while high frequency current is periodic, where the basic period is multiple or fraction of the switching period T_S.

2.4.1. How to Calculate Total Losses in Case that the ESR is a Function of Frequency?

The serial equivalent series resistance is the frequency dependent resistance. Based on the time to frequency transformations, one can conclude that the resistance is alos time dependent.

$$R_{C0} = R_{C0}(\omega) \Rightarrow R_{C0} = R_{C0}(t) \tag{2.33}$$

Due to the frequency dependent resistance, instantaneous voltage and current are not linked by a simple coefficient R_{C0},

$$u_{ESR}(t) \neq R_{C0} \cdot i_{C0}(t). \tag{2.34}$$

Considering the excitation current i_{C0} is sinusoidal function $i_{C0}(t) = I_{C0}\sin(\omega_0 t)$, one can write that instantaneous voltage and current are linked by a simple coefficient R_{C0}, where R_{C0} is the resistance at a specified frequency,

$$u_{ESR}(t) = U_{ESR}\sin(\omega_0 t) = R_{C0}(\omega)\big|_{\omega=\omega_0} I_{C0}\sin(\omega_0 t) = R_{C0}(\omega)\big|_{\omega=\omega_0} i_{C0}(t). \tag{2.35}$$

Instantaneous power of the resistor R_{C0} carrying a current i_0 is

$$p(t) = u_{ESR}(t)\cdot i_0(t) = f\left(i_0(t)\right)\cdot i_0(t), \tag{2.36}$$

where $u_{ESR} = f\left(i_{C0}(t)\right)$ is the voltage across the equivalent series resistance of the capacitor as a function of the current. This nonlinearity is some kind of hidden nonlinearity, which exists due to the frequency dependent resistance of the capacitor.

Average power calculated over a period T is

$$P_{AV}(T) = \frac{1}{T}\int_{t}^{t+T} f\left(i_{C0}(\tau)\right) i_{C0}(\tau)\, d\tau. \tag{2.37}$$

where the period T represents the fundamental period in case of periodic function. If the current is non-periodic, T represents the period of observation.

2.4.2. The Current is Periodic Function

Consider the current i_{C0} is periodic function with a period T_0, and angular frequency ω_0. This current can be expanded in a Fourier series:

$$i_{C0}(t) = \sum_{k=0}^{+\infty} I_{C0(k)}\sin\left(k\omega_0 t + \varphi_k\right). \tag{2.38}$$

The voltage across equivalent series resistance con also be expanded in a Fourier series

$$u_{ESR}(t) = \sum_{k=0}^{+\infty} R_{C0}(k\omega_0)\cdot I_{C0(k)}\sin\left(k\omega_0 t + \psi_k\right), \tag{2.39}$$

where $R_{C0}(k\omega_0) = R_{C0}(\omega)$ is the frequency dependent R_{C0} of the capacitor. Since the resistor is quasi-linear (2.35), the phase displacement for each harmonic is zero, and $\psi_k = \varphi_k$

as a consequence. Inserting (2.38) and (2.39) into (2.36) yields instantaneous power dissipated on the resistor $R_{C0,}$

$$p(t)=\sum_{k=0}^{+\infty} I_{C0(k)}\sin\left(k\omega_0 t+\varphi_k\right)\cdot\sum_{k=0}^{+\infty} R_{C0}\left(k\omega_0\right)I_{C0(k)}\sin\left(k\omega_0 t+\varphi_k\right). \tag{2.40}$$

Using the Lagrange identity [82],

$$f_1\cdot f_2=\sum_{k=0}^{+\infty}F_{1(k)}\cdot\sum_{k=0}^{+\infty}F_{2(k)}=\sum_{k=0}^{+\infty}F_{1(k)}F_{2(k)}+\sum_{n=0}^{+\infty}\sum_{\substack{m=0\\ n\neq m}}^{+\infty}F_{1(n)}F_{1(m)}, \tag{2.41}$$

where f_1 and f_2 are regular functions which could be expanded in potential series, yields

$$\begin{aligned}p(t)=&\frac{1}{2}\sum_{k=0}^{+\infty}R_{C0}\left(k\omega_0\right)I_{0(k)}^2\left(1-\cos\left(2k\omega_0 t+2\varphi_k\right)\right)\\&+\sum_{n=0}^{+\infty}\sum_{\substack{m=0\\ n\neq m}}^{+\infty}I_{0(n)}\cdot R_{C0}\left(m\omega_0\right)I_{0(m)}\sin\left(n\omega_0 t+\varphi_n\right)\cdot\sin\left(m\omega_0 t+\varphi_m\right)\end{aligned}. \tag{2.42}$$

The average power dissipated over a period T is

$$P_{AV}(T)=\frac{1}{T}\int_t^{t+T}\left(\begin{aligned}&\frac{1}{2}\sum_{k=0}^{+\infty}R_{C0}\left(k\omega_0\right)I_{C0(k)}^2\left(1-\cos\left(2k\omega_0\tau+2\varphi_k\right)\right)+\\&+\sum_{n=0}^{+\infty}\sum_{\substack{m=0\\ n\neq m}}^{+\infty}I_{C0(n)}\cdot R_{C0}\left(m\omega_0\right)I_{C0(m)}\sin\left(n\omega_0\tau+\varphi_n\right)\sin\left(m\omega_0\tau+\varphi_m\right)\end{aligned}\right)d\tau. \tag{2.43}$$

Using orthogonal property of the *sin* and *cos* functions,

$$\begin{aligned}&\int_t^{t+T}\sin\left(\omega_0\tau\right)\cos\left(\omega_0\tau\right)d\tau=0,\ \int_t^{t+T}\sin\left(n\omega_0\tau\right)\sin\left(m\omega_0\tau\right)d\tau\Big|_{n\neq m}=0\\&\int_t^{t+T}\cos\left(n\omega_0\tau\right)\cos\left(m\omega_0\tau\right)d\tau\Big|_{n\neq m}=0,\end{aligned} \tag{2.44}$$

yields an average power

$$P_{AV}(T)=\frac{1}{2}\sum_{k=0}^{+\infty}R_{C0}\left(k\omega_0\right)\cdot I_{0(k)}^2. \tag{2.45}$$

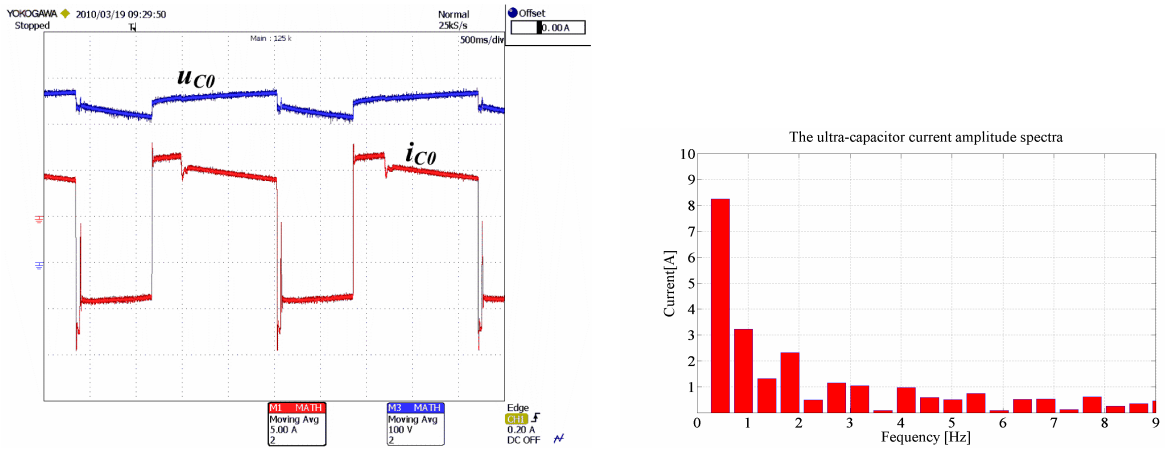
Please note from (2.45), that the total average power depends strongly on the frequency spectrum of the capacitor current. Thus, to estimate total losses one has to take account of the real time profile of the capacitor current.

2.4.2.1. Low Frequency Current

In the general case, the low frequency current would be either pseudo-periodic or periodic, depending on the application. The dominant time constant and fundamental frequency depends on the charge/discharge cycle and power/current level. This can be expressed as

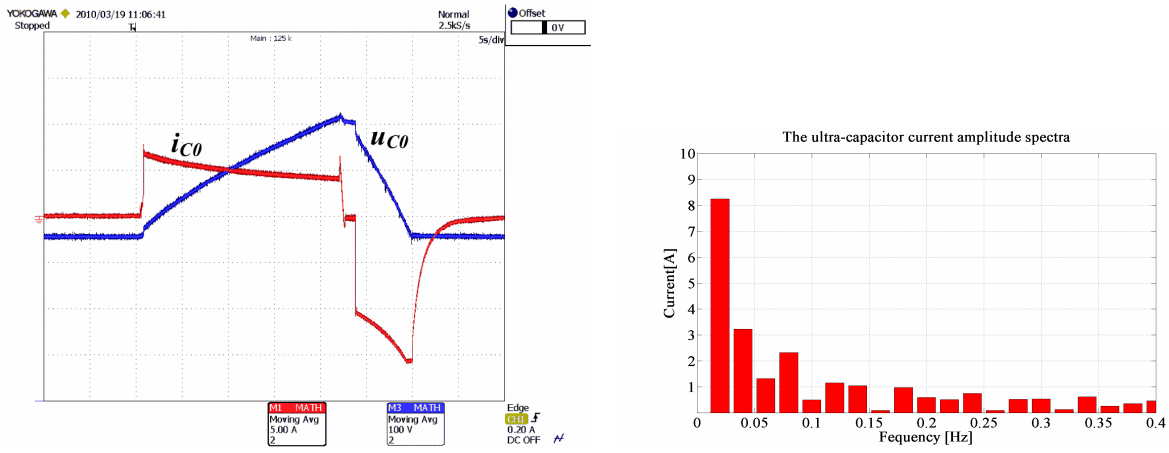
$$i_{C0\_LF}(t)=i_{C0\_LF}\left(P_0,U_{C0},R_{C0},C\right). \tag{2.46}$$

Two application examples are illustrated in Fig. 2.12 and Fig. 2.13. The first one is a tooling machine application with intermittent load. The ultra-capacitor is used as an energy storage device to filter peak power from the mains supply. Fig. 2.12 (a) shows an experimental waveform of the ultra-capacitor current and voltage. The current amplitude spectrum is shown in Fig. 2.12 (b). Note that the dominant frequency (first harmonic) is 0.48 Hz and the higher harmonics fall in the mid-frequency range (see example in Fig. 2.6). Hence, the losses have to be computed taking all spectral components of the current and the frequency dependent resistance into account, as given in (2.45).



(a) (b)

Fig. 2.12 Variable speed drive with the ultra-capacitor as energy storage device used to filter the drive input peak power. a) Experimental waveform of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div]. b) The current amplitude spectra.



(a) (b)

Fig. 2.13 Braking and energy recovery cycle of a variable speed drive with the ultra-capacitor as energy storage device. A) Experimental waveform of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div]. b) The current amplitude spectrum.

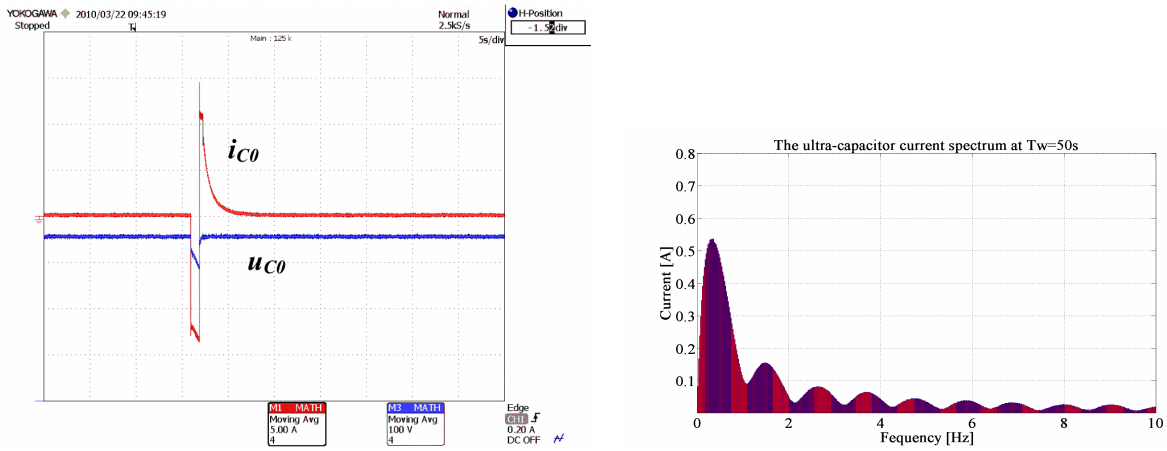
Another typical application is a lift or hoisting application with a requirement for braking. The waveforms over one entire cycle are shown in Fig. 2.13 (a), while the amplitude spectrum is shown in Fig. 2.13 (b). In this example, the current fundamental frequency is below the ultra-capacitor mid-frequency range. Therefore the losses can be computed using the total RMS current and that the resistance is constant (frequency independent).

2.4.2.2. High Frequency Current

The ultra-capacitor high frequency current is the current ripple caused by the power converter used to charge/discharge the ultra-capacitor. The current ripple depends on the power converter topology. This will be discussed in more details in chapter 4. For the moment, we can assume that the power converter is designed in such a way to have the current ripple significantly smaller than the average current (selecting an appropriate topology or adding a low pass filter between the converter and the ultra-capacitor). Also, it is assumed that fundamental frequency of the current ripple is far above the ultra-capacitor cut-off frequency (the capacitance and resistance can be assumed as constant properties).

2.4.3. The Current is Non-periodic Function

Let's consider that the capacitor current is non-periodic function. Typical example is variable speed drive with extended ride-through capability. The ultra-capacitor is employed as the energy storage to supply the drive system in case of short power interruption. An example is illustrated in Fig. 2.14. The waveforms of the ultra-capacitor current and voltage are shown in Fig. 2.14 (a). Fig. 2.14 (b) shows the current amplitude spectrum computed within a window T=50s.



(a) (b)

Fig. 2.14 Variable speed drive with emergency supply based on the ultra-capacitor as an energy storage device. a) Experimental waveform of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div]. b) The current amplitude spectra.

The ultra-capacitor current and voltage drop on the equivalent resistor R_{C0} could be represented by Fourier's integrals

$$i_0(t)=\frac{1}{2\pi}\int_{-\infty}^{+\infty} I(j\omega)e^{j\omega t}d\omega,\ u_{ESR}(t)=\frac{1}{2\pi}\int_{-\infty}^{+\infty} R_{C0}(j\omega)I(j\omega)e^{j\omega t}d\omega. \tag{2.47}$$

Then, instantaneous power dissipated on the R_{C0} is

$$p(t)=\frac{1}{4\pi^2}\int_{-\infty}^{+\infty} I(j\omega)e^{j\omega t}d\omega\cdot\int_{-\infty}^{+\infty} R_{C0}(j\omega)I(j\omega)e^{j\omega t}d\omega. \tag{2.48}$$

From the conditions $\int_{-\infty}^{+\infty} i_0(t)dt < \infty$ and $\int_{-\infty}^{+\infty} u_{ESR}(t)dt < \infty$ it follows that average power is zero

$$P_{AV} = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} p(t)dt = 0 . \tag{2.49}$$

Please, note that average power (2.49) is zero, and as that it has no practical value. However, the question is how to evaluate the ultra-capacitor losses? Is it sufficient to compute the losses or is some other quantity as important? The quantities are important, namely: 1) the energy dissipated on the internal resistor and 2) the module temperature increase.

2.4.3.1. The Energy Losses

The energy dissipated on the ultra-capacitor resistance is

$$E_{RESR} = \int_{-\infty}^{\infty} p(t)dt = \frac{1}{4\pi^2} \int_{-\infty}^{\infty} \left(\int_{-\infty}^{+\infty} I(j\omega)e^{j\omega t}d\omega \cdot \int_{-\infty}^{+\infty} R_{C0}(j\omega)I(j\omega)e^{j\omega t}d\omega \right) dt . \tag{2.50}$$

2.4.3.2. The Ultra-capacitor Temperature Increase

The power losses can be computed in the frequency domain from (2.47) and using convolution in the frequency domain.

$$p(j\omega) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} (R_{C0}(j\upsilon)I(j\upsilon)I(j(\omega-\upsilon)))d\upsilon \tag{2.51}$$

$R_{C0}(j\upsilon)$ is the ultra-capacitor resistance as a function on the frequency (2.10), $I(j\upsilon)$ is a spectrum of the ultra-capacitor current and υ is angular frequency.

The ultra-capacitor temperature rise can be computed as

$$\Delta\theta(t) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} p(j\omega)Z(j\omega)e^{j\omega t}d\omega , \tag{2.52}$$

where $Z(j\omega)$ is the ultra-capacitor thermal impedance.

2.5. Trends in the Ultra-capacitors Development

Two key features are relevant for the development of new generation of the ultra-capacitors: 1) energy density and 2) the internal equivalent series resistance that basically determines the power density. Presently, most commercially available ultra-capacitors have the energy density around 5Wh/kg and a power density up to 20kW/kg [70]-[73], [84]. Existing ultra-capacitors energy density is approximately 5% of the energy density of the broadly used lithium-ion batteries. For most of applications this is not sufficient. There is need for energy densities of 20Wh/kg or more.

Currently, there are four different mainstreams in the ultra-capacitors development: 1) Carbon nano-tube technology, 2) Nano-gate technology, 3) so-called EeStore technology, and 4) Mega farad super-capacitor technology. A summary of all four ongoing ultra-capacitor technologies is given in TABLE 2-3.

A team at Massachusetts Institute of Technology (MIT) led by Professor Joel Schindall has started development of new ultra-capacitor based on carbon nano-tube technology [86], [87]. An ultra-capacitor based on such an approach could have energy density as high as 25% or even 50% of the energy density of the existing chemical batteries.

Okamura Laboratory and Power Systems have announced first significant development results of new generation of ultra-capacitor based on very promising Nano-gate technology in September 2007 [88]. The expected energy density is 50 to 80Wh/kg, which is the same order as the existing electrochemical batteries.

The third, quiet different ultra-capacitor technology is so-called EeStore technology, which promises to increase the energy density up to 280Wh/kg, and the operating voltage up to 3000V, [89]. These ultra-capacitors are based on high voltage multilayer ceramic technology, and therefore the internal series resistance is expected to be very low compared to the existing technologies.

A recently announced technology is the double layer capacitor with a thin layer of high permittivity material on top of the activated carbon electrode [90]. Expected energy density is two order of magnitude greater than existing technology, ~500[Wh/kg].

TABLE 2-3: Existing ultra-capacitor technology versus technology under development.

	The existing technology	Nano-tube	Nano-gate	EesE	Mega Farad super-capacitor
Energy density [Wh/kg]	~5	20-40	50-80	~280	~500
Operating voltage [V]	<2.8	~3	~3.9	3000	<2.8
Internal resistance [mΩ]	0.66+1000/C*	As the existing	As the existing	Lower than the existing	As the existing

* This is an approximation where C is the cell capacitance [F].

The ultra-capacitor cost is driven by the market, mainly the automotive industry. As the application fields of ultra-capacitors increase so the cost of ultra-capacitors decrease. The cost prediction for 2010 is 1.28US$ per kJ of the stored energy [84], [85].

2.6. Short Conclusion

In this chapter, the ultra-capacitor as an energy storage device dedicated for power conversion applications has been discussed. In comparison to state of the art electrochemical batteries, the ultra-capacitors have higher power density, higher efficiency, longer lifetime and greater cycling capability. In comparison to the state of the art electrolytic capacitors, the ultra-capacitors have higher energy density. All these advantages make the ultra-capacitors good candidate for many power conversion applications with a need for short term, 0.1 to 15s,

energy storage. The applications could be industrial applications, power transmission/distribution network, building and IT centre.

The ultra-capacitor macro model has been discussed. Depending on the application need, a simplified first order or higher order RC model is proposed. The model can be used to estimate the ultra-capacitor losses and temperature. The first order model is sufficient if the ultra-capacitor current frequency is well below or above the transition frequency. Otherwise, a second or even third order model is necessary. The first order model is sufficiently accurate for the interface power converter controllers' analysis and synthesis.

State of the art ultra-capacitor technology is activated carbon double layer capacitor [70]-[73], [84]. Among this, there are four different technologies under development: 1) Nano tube capacitor [86], 2) Nano-gate capacitor [88], 3) EeStore high voltage multilayer capacitor [89], and 4) Mega Farad ultra-capacitor [90]. All technologies under development promise order of magnitude higher energy density in comparison to the state of the art technology. Some of them, for example technology 3) and 4), promise energy density even greater than state of the art electrochemical batteries.

3. ULTRA-CAPACITOR BASED REGENERATIVE ELECTRIC DRIVES

3.1. Background

In general introduction of the dissertation, application of controlled electric drives and some associated technical issues have been discussed. For the sake of clarity and simplicity, a part of that discussion has been repeated in this chapter.

Modern controlled electric drives are exclusively based on three phase motors, either the induction or permanent magnet (PM) synchronous motors. The motor is powered from a pulse width modulated (PWM) converter, and the converter is supplied from the industrial or distributive mains 230 V to 690V and 50 to 60Hz. Several technical issues in application of such drives are still a big challenge. Two of these issues, namely 1) recovery of the braking energy and 2) the drive ride-through capability, are discussed and a solution is proposed in this chapter.

Most of drive applications, such as lifts, cranes, tooling machines, and so on, are characterized by low balance between average and peak power. Moreover, such applications have a demand for braking at rated power. In ordinary variable speed drives, the mechanical energy of rotating mass of the motor load and the motor shaft is usually dissipated in a brake resistor. The energy losses in such applications can be 20 to 50% of the consumed energy. Nowadays, having in mind energy crisis, this has become an issue that needs a very urgent solution [6].

Modern variable speed drives are sensitive to the mains supply disturbances. The most frequent disturbance is voltage dip/sag [10]. Power interruptions cause drop in the dc bus voltage below the limit, and then the entire drive system trips. The system interruptions are very costly and unacceptable when the drive is applied in critical process industry, oil pump systems or glass industry. Such kind of industry have reported losses ranging from 10k$ to 1M$ per a disrupting event [10].

State of the art solutions can be split into two different groups: 1) back to back PWM rectifiers and 2) direct (matrix) converters [16]-[18]. These regenerative drives draw the energy from the mains when operates in motoring mode, and pump the energy in the mains while the drive is in breaking mode. The main disadvantage of such solutions is the fact that functionality of the drive is strongly linked to the mains. In other words, any power interruption of the mains is reflected to the drive, and the drive is disabled whenever the mains is interrupted for longer than one the mains cycle (20ms). Moreover, such kind of drives has a high power demand during acceleration and deceleration. This modulated power produces additional disturbances and losses in weak supply mains.

A basic idea of the regenerative controlled electric drive system using an ultra-capacitor as an energy storage device is illustrated in Fig. 3.1. The drive system consists of an ordinary variable speed drive converter (the input diode rectifier, voltage dc link and output inverter) and a parallel connected energy storage device. The rectifier is connected to the three-phase distribution network, while the inverter feeds a three-phase motor (the induction or synchronies PM motor). The energy storage device is composed of an ultra-capacitor C_{C0} and a bi-directional dc-dc power converter. The energy storage could be another type of storage device, such as flywheel or battery. However, the battery is not an appropriate

solution because limited power density, while the flywheel is a system that is more complex in comparison to the ultra-capacitor system.

For generality of the analysis, in the first part of this section the dc-dc power converter will be considered as a controllable bi-directional dc-dc power converter with one input (the dc bus voltage v_{BUS}) and one output (the ultra-capacitor voltage u_{C0}). The dc-dc converter could be, for example, non-isolated two-level or three-level converter, multiphase interleaved converter or an isolated dc-dc converter. The dc-dc converter is controlled by the control variable m that could be duty cycle, phase shift or switching frequency, depending on the converter topology. More details of the dc-dc power converter will be given in chapter 4.

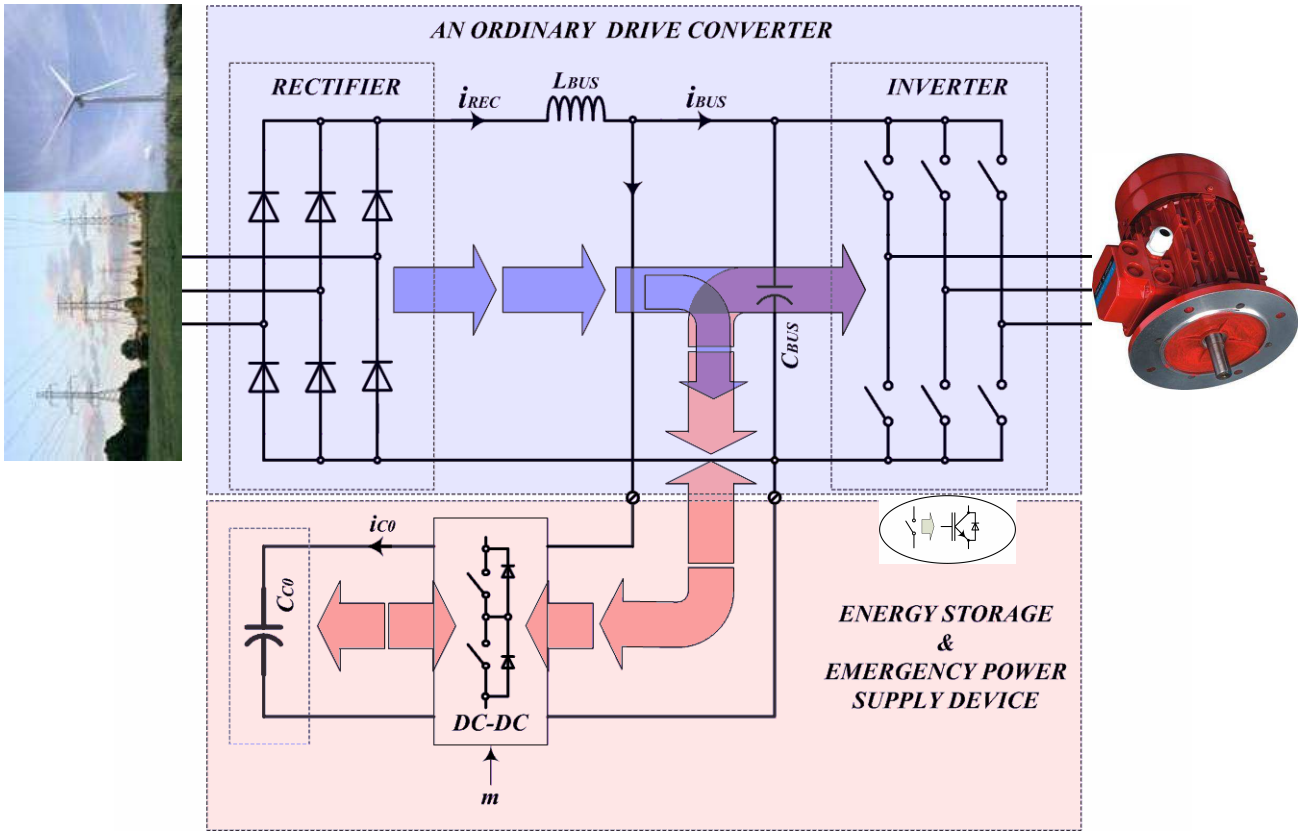


Fig. 3.1 Concept of regenerative controlled electric drive based on an auxiliary energy storage device and an interface dc-dc converter.

3.2. Operational Modes

The drive system whose block circuit diagram is depicted in Fig. 3.1 may operate in six different modes. The modes are illustrated in Fig. 3.2 and Fig. 3.3. The drive system is represented by the rectifier, inverter, dc bus capacitor C_{BUS}, dc-dc converter and the ultra-capacitor. The dc bus inductor L_{BUS} is not relevant for this analysis and therefore it is just indicated in the circuit as an inductance between the rectifier and inverter. Fig. 3.4 illustrates relevant waveforms for different operating conditions. The signification of voltages V_{BUSmax}, V_{BUSmin}, U_{C0max}, U_{C0inM} and U_{C0min} that appear in Fig. 3.4 will be discussed shortly after.

MM) Motoring from the mains is illustrated in Fig. 3.2 (a). The drive operates in motoring mode, being powered from the mains. The dc bus voltage v_{BUS} is slightly lower than the input phase to phase peak voltage. The dc-dc converter controls the ultra-capacitor voltage

to U_{C0inM}, in order to prevent energy flow between the ultra-capacitor and the drive dc bus. In this mode, the rectifier voltage v_{REC} is determined by the mains voltage and conduction state of the rectifier diodes, where the diodes state is determined by dc bus filter capacitor, inductor and load [48].

B) Braking and energy storing mode is illustrated in Fig. 3.2 (b). The drive operates in braking mode. As the dc bus load is negative (the motor turns to be a generator), the dc bus capacitor is charged and therefore the dc bus voltage v_{BUS} increases. Once it reaches V_{BUSmax}, the dc-dc converter starts to regulate the ultra-capacitor current i_{C0} in order to regulate the dc bus voltage to V_{BUSmax}. The ultra-capacitor current is positive and the ultra-capacitor voltage increases. The braking energy is stored into the ultra-capacitor. Since the dc-dc converter controller is designed to maintain the dc bus voltage V_{BUSmax} greater than the input phase to phase peak voltage, the drive rectifier is blocked. Thus the drive input current is zero and the rectifier voltage v_{REC} is equal to the dc bus voltage v_{BUS}. The ultra-capacitor is sized to store certain energy during a braking phase. Thus, at the end of a braking phase the ultra-capacitor voltage has to be lower than the maximum rated voltage U_{C0max}.

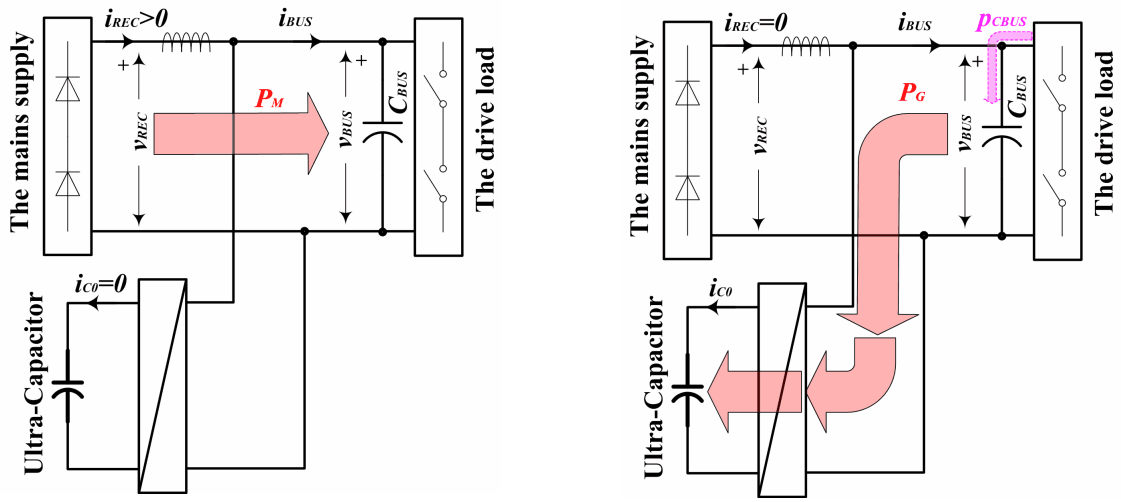


Fig. 3.2 The power flow for different operating modes a) the mains motoring mode (**MM**), b) braking mode (**B**).

STB) Standby mode: There is not energy flow between the drive, mains and ultra-capacitor. The ultra-capacitor voltage is constant, taking any value between U_{C0max} and U_{C0inM}. The control system is designed in such a way to maintain the dc bus voltage to V_{BUSmax} whenever the ultra-capacitor voltage is greater than U_{C0inM}. Therefore, if this is case in stand-by mode, the dc bus voltage will stay constant at V_{BUSmax}.

MC$_0$) Motoring and energy recovery mode is illustrated in Fig. 3.3 (a). The drive operates in motoring mode, being powered from the ultra-capacitor. The ultra-capacitor voltage is greater than U_{C0inM}. The dc bus voltage controller acts on the dc-dc converter, in order to maintain the dc bus voltage constant (V_{BUSmax}). The ultra-capacitor is discharged and its voltage decreases towards the intermediate level U_{C0inM}. The energy is restored from the ultra-capacitor. Once the ultra-capacitor has been discharged to the intermediate level U_{C0inM}, the dc bus voltage falls to the nominal voltage and the drive rectifier diodes start to conduct. The drive is again powered from the mains.

RT) Ride-through mode is illustrated in Fig. 3.3 (b). The mains supply is interrupted and the dc bus voltage starts to decrease quickly. Once it has reached the minimum voltage V_{BUSmin}, the dc-dc converter starts to discharge the ultra-capacitor and maintain the dc bus voltage to V_{BUSmin}. The drive is powered from the ultra-capacitor. The ultra-capacitor is discharged deeper below the intermediate level U_{C0inM} towards the minimum level U_{C0min}.

MM-CH) The ultra-capacitor charging mode is illustrated in Fig. 3.3 (b). The mains supply is recovered and then the ultra-capacitor is recharged to the intermediate level U_{C0inM}.

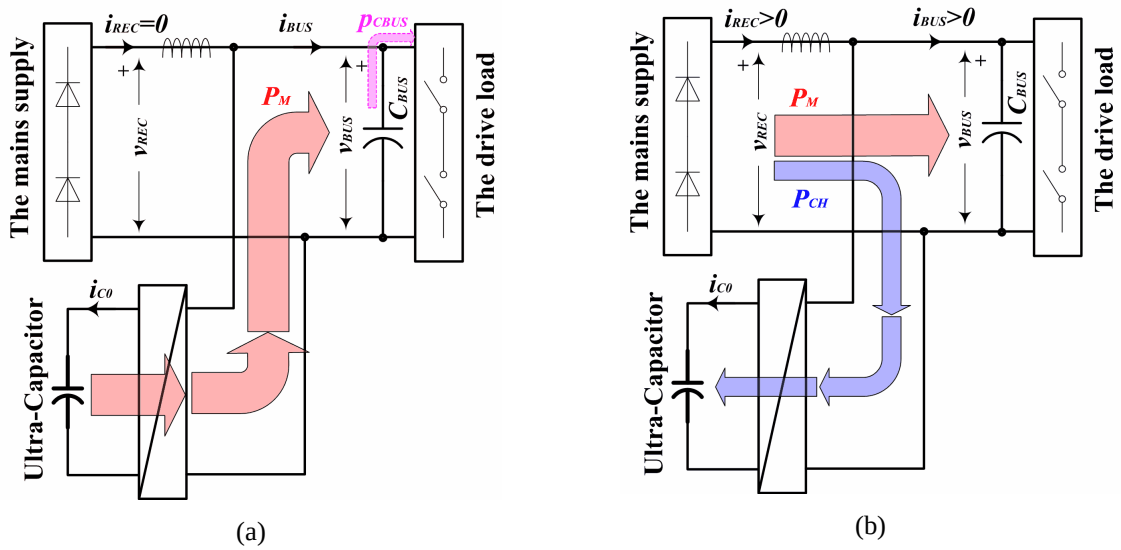


Fig. 3.3 The power flow for different operating modes: a) energy recovery mode (**MC$_0$**) and ride-through mode (**RT**), b) the ultra-capacitor charging mode (**MM-CH**).

3.2.1. Definition of the Reference Voltages

Let us now explain the signification of the reference voltages V_{BUSmax}, V_{BUSmin}, U_{C0max}, U_{C0inM} and U_{C0min}. Fig. 3.5 (a) illustrates the signification of the reference voltages V_{BUSmax} and V_{BUSmin}. OBF signifies Over-Braking Fault, while USF signifies the Under Supply Fault. When the system operates in the mains motoring mode, the dc bus voltage takes a value between minimum and maximum input voltage. In order to avoid unnecessary charge and discharge of the ultra-capacitor, the dc bus voltage references V_{BUSmin} and V_{BUSmax} must stay outside of the normal operation range, as shown in Fig. 3.5 (a). On other side, to prevent the system fault, either OBF or USF, the dc bus voltage references must not be in the forbidden regions. Therefore, the reference V_{BUSmin} is located within an interval [USF, Min Input Voltage] while the reference V_{BUSmax} is located within an interval [Max Input Voltage, OBF].

The ultra-capacitor voltage takes value within an interval [U_{C0max}, U_{C0min}], as shown in Fig. 3.5 (b). The maximum voltage U_{C0max} is determined by the ultra-capacitor rated voltage. This limit must not be exceeded in any case; otherwise the ultra-capacitor will be damaged or even totally destroyed. The minimum voltage U_{C0min} is determined by the current capability of the power converter and the ultra-capacitor; the lower voltage the higher current capability and vice versa. The intermediate voltage U_{C0inM} can take any value between the maximum and minimum, depending on the design criteria (ratio of the braking energy capability to the ride-through energy availability).

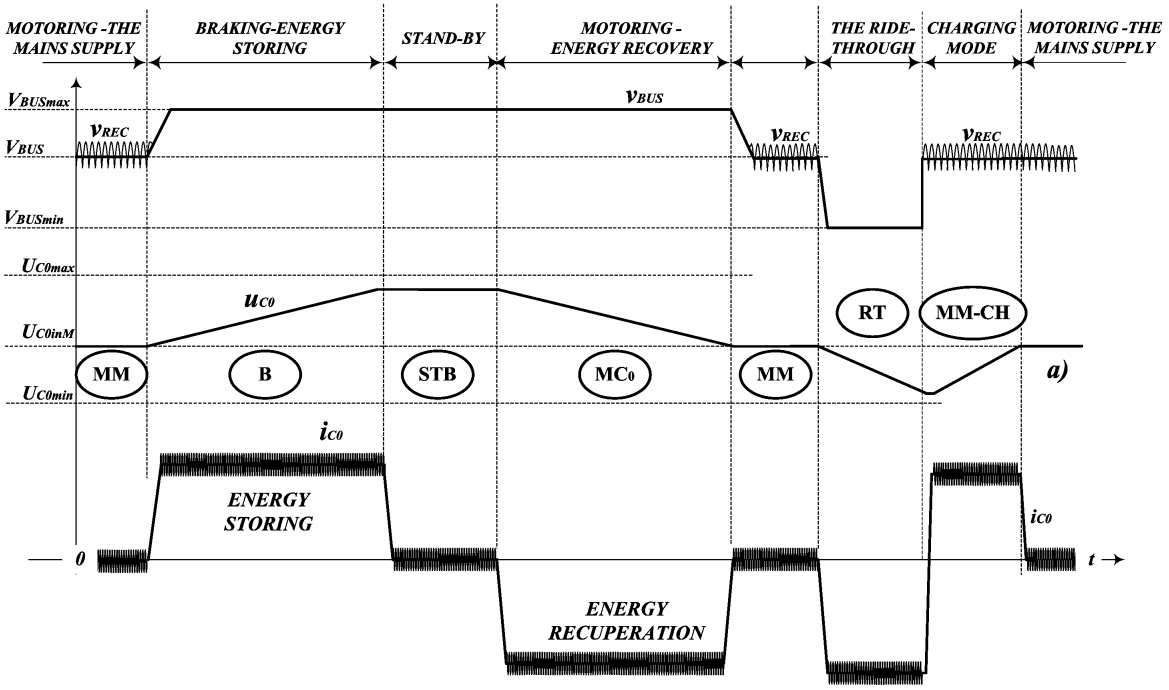


Fig. 3.4 The waveforms for different operating modes: the mains motoring mode (**MM**), braking mode (**B**), stand-by mode (**STB**), energy recovery mode (**MC$_0$**), ride-through mode (**RT**), the ultra-capacitor charging mode (**MM-CH**) and the mains peak power filtering mode (**MPFM**).

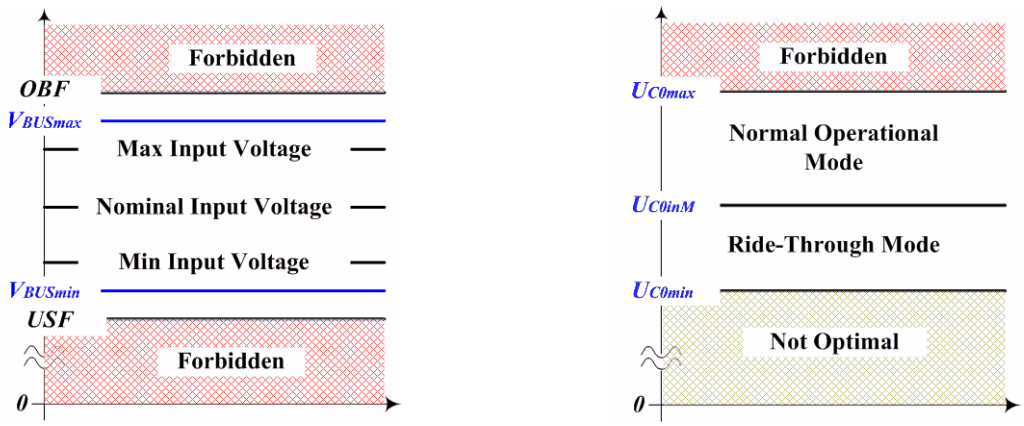


Fig. 3.5 Definition of the reference voltages, (a) V_{BUSmax}, V_{BUSmin}, and, b) U_{C0min}, U_{C0inM} and U_{C0max}.

3.2.2. Some Experimental Waveforms

Block diagram of an experimental set-up is depicted in Fig. 3.6. A general purpose variable speed drive *ATV71* (5.5kW 400V) was used in the test set up. An ultra-capacitor module of 0.4F rated capacitance and 800V rated voltage was connected to the drive via the custom designed bi-directional dc-dc converter. The converter was controlled by a digital signal processor (DSP) TMS 320F2808 and interfacing analog/digital electronic circuitry (measurement, gate driving and protection). Different operation modes were analysed and some waveforms recorded. The waveforms are depicted and discussed hereafter.

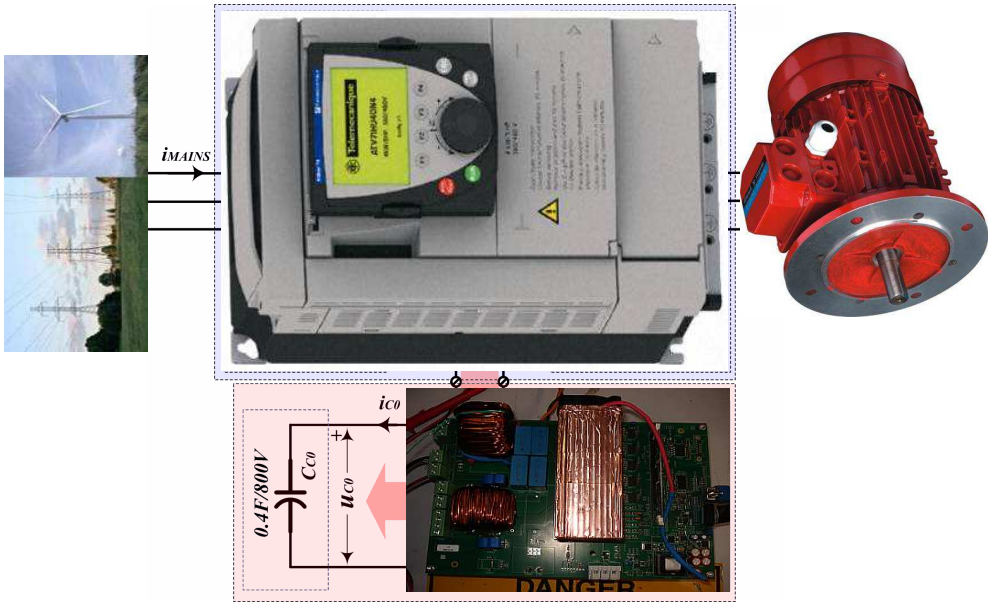


Fig. 3.6 Experimental set-up. An ultra-capacitor is connected to a general purpose variable speed drive ATV71 5.5kw via the dc-dc converter.

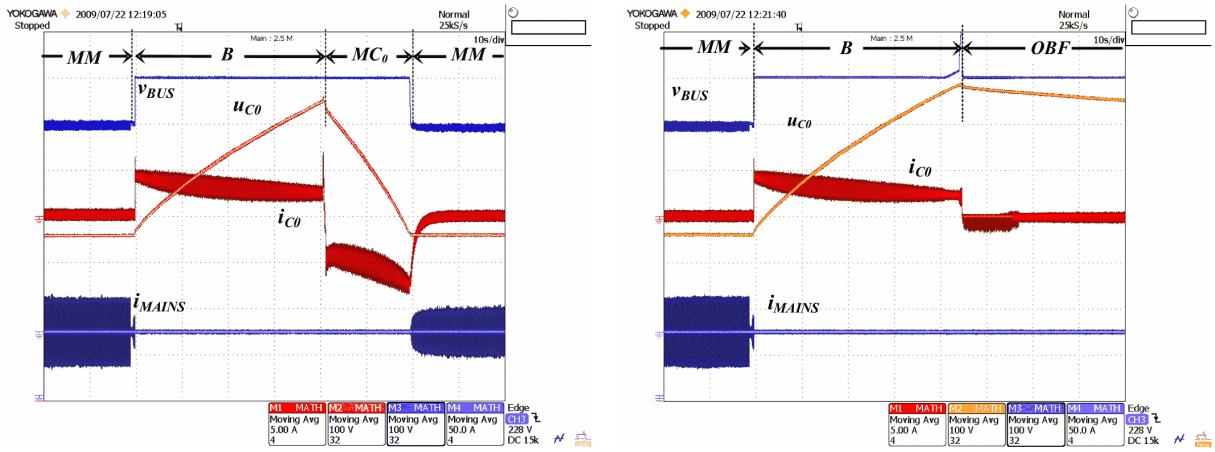
Fig. 3.7 (a) shows waveforms of the dc bus voltage v_{BUS}, the drive input current i_{MAINS}, the ultra-capacitor current i_{C0} and voltage u_{C0} when the drive operates in motoring/braking/motoring cycle. The drive system runs in motoring mode (**MM**) being supplied from the mains. The ultra-capacitor voltage is U_{C0inM}, while the dc bus voltage is determined by the mains phase to phase voltage ($\approx 1.41 V_{MAINS}$). Once the drive load is inverted, the drive enters in the braking phase (**B**) and the energy being transferred from the load to the drive dc bus. The dc bus voltage v_{BUS} elevates up to the upper reference V_{BUSmax} and then stayes regulated to that level. At the same time, the input current i_{MAINS} falls to zero. The ultra-capacitor voltage increases and the current decreases (charging/discharging power is roughly constant). When the braking phase is finished, the drive load becomes again positive and the drive enters in motoring mode (**MC$_0$**), being supplied from the ultra-capacitor. The current i_{C0} turns negative and the voltage u_{C0} starts to decrease towards the reference U_{C0inM}. When the ultra-capacitor voltage reaches the reference U_{C0inM} the current droppes to zero and the dc bus voltage falls to the nominal value. The ultra-capacitor discharging is finished and the drive is again supplied from the mains (**MM**).

Fig. 3.7 (b) illustrates the system behaviour when the braking energy is greater than the ultra-capacitor storage capability. In this case the ultra-capacitor is charged to the maximum voltage U_{C0max} before the braking is finished. As the voltage reaches the maximum, charging is stopped to prevent break-down of the ultra-capacitor. The dc bus voltage v_{BUS} starts to increase until reached over-braking protection level and drive system falls into over-braking fault (**OBF**). Shortly before the ultra-capacitor voltage has reached the maximum, the dc bus voltage started to increase and follow the increase in the ultra-capacitor voltage. This is caused by the dc-dc converter duty cycle saturation ($dmax$=97.5%).

Fig. 3.8 (a) shows the waveforms in case of the mains short interruption. The drive runs in the mains motoring mode (**MM**). Once the mains is interrupted, the dc bus voltage falls to the minimum reference V_{BUSmin}, and stays at that level regulated by the dc bus voltage controller. The drive operates in the ride-through mode (**RT**), being supplied from the ultra-capacitor. The ultra-capacitor voltage decreases below U_{C0inM} towards U_{Cimin}. Once the mains

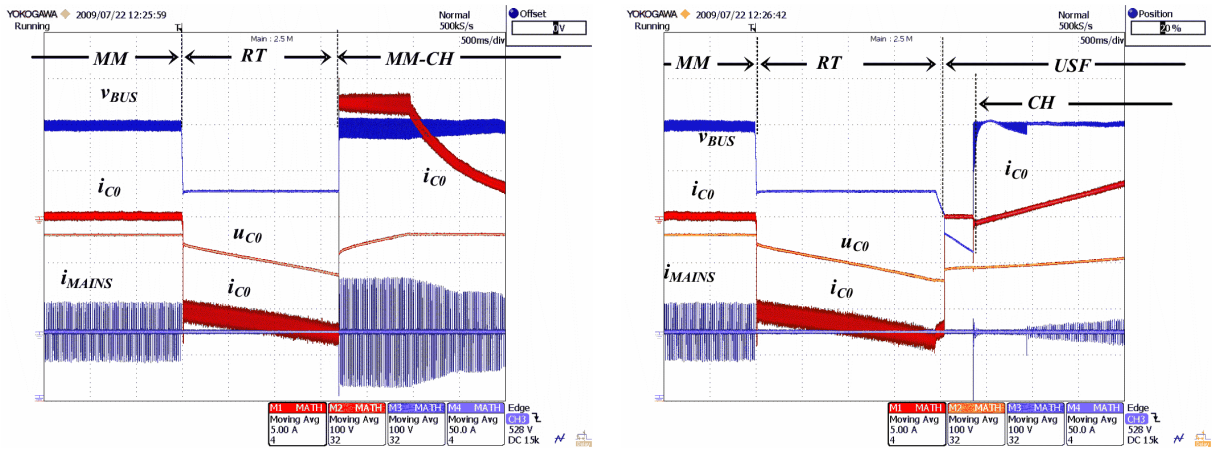
is recovered after 1.5s, the ultra-capacitor is re-charged to U_{C0inM} (the mains motoring and charging mode (**MM-CH**)).

Fig. 3.8 (b) illustrates a case when the power interruption is longer than the specified. The ultra-capacitor is discharged to the minimum voltage U_{C0min}, and then the ultra-capacitor discharge current i_{C0} falls to zero. Since the dc bus voltage is not controlled any more, it falls below the limit, and the drive falls into under-supply fault (**USF**).



(a) (b)

Fig. 3.7 Experimental waveforms of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div], the dc bus voltage v_{BUS} [100V/div] and the mains current i_{MAINS} [50A/div] during an entire braking-motoring cycle. a) The ultra-capacitor is properly sized, and b) the ultra-capacitor is under-sized.



(a) (b)

Fig. 3.8 Experimental waveforms of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div], the dc bus voltage v_{BUS} [100V/div] and the mains current i_{MAINS} [50A/div] when the mains is interrupted. a) Short power interruption, and b) long power interruption.

3.3. Ultra-capacitor Selection and Design

The ultra-capacitor design and selection criterion is based on the three parameters. 1) Rated voltage of the ultra-capacitor module, 2) the ultra-capacitor rated capacitance, and 3) the ultra-capacitor losses and conversion efficiency.

3.3.1. Voltage Rating

The ultra-capacitor module rated voltage depends on the interface dc-dc converter topology. In this analysis we have assumed that the dc-dc converter is a non-isolated direct dc-dc converter with voltage gain not greater than unity $u_{C0}/v_{BUS}\leq 1$. Therefore, the ultra-capacitor voltage cannot be greater than the dc bus voltage. As the ultra-capacitor is charged when the drive dc bus voltage is maximum (the drive is braking), the ultra-capacitor rated voltage U_{C0max} is

$$U_{C0\max} \leq V_{BUS\max}. \tag{3.1}$$

The ultra-capacitor minimum operating voltage is determined by the dc-dc converter current capability I_{C0max} and conversion power P_0,

$$U_{C0\min} \geq \frac{P_0}{I_{C0\max}}. \tag{3.2}$$

Very often, the minimum voltage is limited to 40 to 50% of the rated voltage ($U_{C0min} = 0.4 \div 0.5\ U_{C0max}$).

3.3.2. The Capacitance

Most of the ultra-capacitor models presented in the literature consider a non-linear (the voltage dependent) transmission line or a finite ladder RC network [76]. For simplicity of the analysis, the transmission line effect is neglected, and a first order nonlinear model depicted in Fig. 3.9 is used [75]. The equivalent series resistance R_{C0} is the frequency-independent resistance. The ultra-capacitor total capacitance is the voltage-controlled capacitance defined as

$$C_{C0}(u_C) = C_0 + k_C \cdot u_C, \tag{3.3}$$

where C_0 is the initial capacitance that represents the electrostatic capacitance of the capacitor, and k_C is a coefficient that represents effects of the diffused layer of the super-capacitor [69].

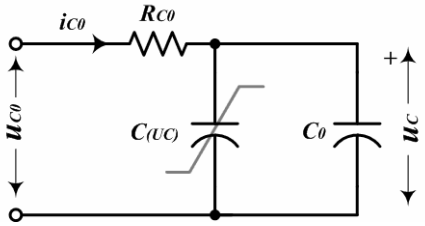


Fig. 3.9 First order RC model of the ultra-capacitor.

Energy storage capacity of the ultra-capacitor (3.3) is

$$E_C = \frac{C_0}{2}\left(U_{C0\max}^2 - U_{C0}^2\right) + \frac{2}{3}k_C\left(U_{C0\max}^3 - U_{C0}^3\right), \tag{3.4}$$

where U_{C0max} is the ultra-capacitor maximum voltage, which has been defined in (3.1) and U_{C0} is the ultra-capacitor initial voltage. The initial capacitance C_0 for the given braking energy E_B and coefficient k_C can be computed from (3.4) as

$$C_0 = \left(E_B - \frac{2}{3} k_C \left(U_{C0\max}^3 - U_{C0inM}^3 \right) \right) \frac{2}{\left(U_{C0\max}^2 - U_{C0inM}^2 \right)}, \tag{3.5}$$

where the ultra-capacitor voltage U_{C0inM} is the intermediate voltage that has been defined in Fig. 3.5 (b). The braking energy E_B is

$$E_B = \eta_B \int_0^{t_B} P_0(t) dt, \tag{3.6}$$

where η_B is efficiency of the entire conversion system, including the motor, drive converter, dc-dc converter and the ultra-capacitor efficiency. Power $P_0(t)$ is the motor shaft power and t_B is braking time.

The ultra-capacitor energy that is available for ride-through cycle is

$$E_{RT} = \frac{C_0}{2} \left(U_{C0inM}^2 - U_{C0\min}^2 \right) + \frac{2}{3} k_C \left(U_{C0inM}^3 - U_{C0\min}^3 \right), \tag{3.7}$$

where U_{C0min} is the ultra-capacitor minimum voltage that has been defined in Fig. 3.5 (b).

The ride-through energy E_{RT}, which the ultra-capacitor has to provide to the drive during a power interruption, is

$$E_{RT} = \frac{1}{\eta_M} \int_0^{t_{RT}} P_0(t) dt, \tag{3.8}$$

where t_{RT} is the ride-through time. η_M is efficiency of the entire conversion system, which depends on the motor shaft power $P_0(t)$ and internal resistance of the ultra-capacitor.

The ultra-capacitor intermediate voltage U_{C0inM} is selected according to the application requirement, for the braking energy capability E_B (3.6) and the ride-through energy availability E_{RT} (3.8). The intermediate voltage U_{C0inM} can be computed from (3.5) and (3.7) as

$$U_{C0inM} \cong \sqrt{\frac{E_{RT} U_{C0\max}^2 + E_B U_{C0\min}^2}{E_C + E_{RT}}}, \tag{3.9}$$

where $k_C \cong 0$.

Fig. 3.10 illustrates the ultra-capacitor intermediate voltage U_{C0inM} versus braking energy E_{BR} and minimum discharge voltage u_{C0min}. The ultra-capacitor voltages are normalized on the rated voltage U_{C0max}, while the braking energy is normalized on the ride-through energy E_{RT}. For example, if the ride through energy is 25% of the braking energy (*Ebr/Ert*=4 on the *x* axis) and minimum discharge voltage is 50% (the blue trace), the intermediate voltage is approximately 63%.

3.3.3. Current Stress and Losses

The ultra-capacitor current, in general case has two essentially different frequency components: 1) Very low frequency, and 2) high switching frequency current.

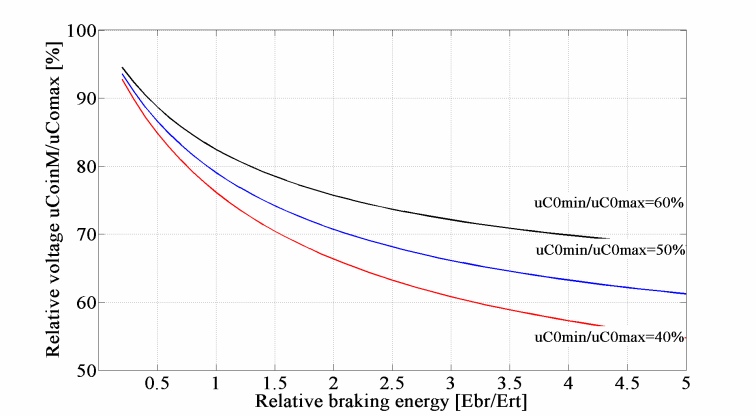


Fig. 3.10 The ultra-capacitor intermediate voltage u_{C0inM} versus relative braking energy (determined as ration between the braking energy E_B and ride-through energy E_{RT}) and relative minimum ultra-capacitor voltage (determined as ratio of minimum to maximum ultra-capacitor voltage).

Very low frequency current corresponds to the energy transfer between the drive dc bus and the ultra-capacitor (braking and motoring from the ultra-capacitor). Considering that the ultra-capacitor is a linear capacitor ($k_C \cong 0.$) and neglecting the internal resistance R_{C0} one can find the ultra-capacitor charging current as

$$i_{C0} \cong P_{C0}\sqrt{\frac{C_0}{C_0 U_{C0\min}^2 + 2P_{C0}t}}\,, \tag{3.10}$$

where the initial ultra-capacitor voltage is $U_{C0\min}$.

Discharging current has similar form

$$i_{C0} \cong -\left|P_{C0}\right|\sqrt{\frac{C_0}{C_0 U_{C0}^2 - 2P_{C0}t}}\,, \tag{3.11}$$

where the voltage U_{C0} is the ultra-capacitor initial voltage. The ultra-capacitor charging/discharging power P_{C0} is constant.

The ultra-capacitor losses are computed from (3.10) and (3.11) as

$$P_C(t) \cong R_{C0}P_{C0}^2\begin{cases}\dfrac{C_0}{C_0 U_{C0\min}^2 + 2P_{C0}t} & \textit{CHARGING}\\[2ex] \dfrac{C_0}{C_0 U_{C0}^2 - 2P_{C0}t} & \textit{DISCHARGING}\end{cases}. \tag{3.12}$$

The losses model (3.12) is correct only if the frequency of the charging/discharging current is lower that the ultra-capacitor cut-off frequency. Otherwise the losses have to be computed using the method described in section 2.4.2.

High frequency ripple Δi_{C0} could be neglected because the ripple is normally quite smaller than the average current. If this is not a case, the additional high frequency losses have to be taken into account.

$$P_{C(HF)} \cong R_{C0(HF)}\Delta i_{C0(RMS)}^2\,, \tag{3.13}$$

where $R_{C0(HF)}$ is the ultra-capacitor resistance at high frequency.

3.3.4. Conversion Efficiency

As given in (3.12), the ultra-capacitor losses depend on a few parameters: the series resistance, capacitance and the ultra-capacitor initial voltage. Is it possible to select the ultra-capacitor for the losses given as a design parameter? To find answer on this question, let us consider that the ultra-capacitor is charged (braking mode of the drive system) from U_{C0inM} toward U_{C0max} with a constant power P_{C0}. The losses-time profile and the energy lost during entire charge time can be defined as

$$P_C(t) \cong R_{C0} P_{C0}^2 \frac{C_0}{C_0 U_{C0\max}^2 - 2E_{BR} + 2P_{C0} t}, \tag{3.14}$$

$$E_{LOSSES} \cong R_{C0} P_{C0}^2 \int_0^{T_{CH}} \frac{C_0}{C_0 U_{C0\max}^2 - 2E_{BR} + 2P_{C0} t} dt = \frac{R_{C0} P_{C0} C_0}{2} \ln \frac{C_0 U_{C0\max}^2}{C_0 U_{C0\max}^2 - 2E_{BR}}, \tag{3.15}$$

where T_{CH} is the ultra-capacitor charge time, in this case the braking time.

The ultra-capacitor resistance depends also on the capacitance. The greater capacitance the smaller resistance

$$\begin{aligned} R_{C0} &= f_1(C_0), \\ \frac{\partial f_1(C_0)}{\partial C_0} &< 0. \end{aligned} \tag{3.16}$$

Fig. 3.11 shows an example. The ultra-capacitor series resistance R_{C0} versus the capacitance C_0 is plotted for an 800V ultra-capacitor module. The module is composed of series/parallel connected ultra-capacitor cells rated on 2.8V [91].

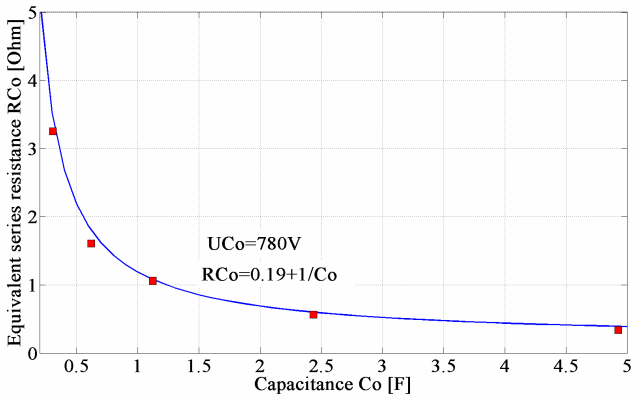


Fig. 3.11 The ultra-capacitor resistance R_{C0} versus the capacitance C_0. The red squares are value from datasheet and blue line is interpolation. The module is arranged as series/parallel connection of 2.8V rated ultra-capacitor cells. The module rated voltage is U_{C0max}=800V.

Substituting (3.16) in (3.15) yields the conversion energy losses as a function on the capacitance C_0,

$$E_{LOSSES} \cong \frac{P_{C0}}{2}(0.19C_0 + 1)\ln \frac{C_0 U_{C0\max}^2}{C_0 U_{C0\max}^2 - 2E_{BR}}. \tag{3.17}$$

Charge/discharge (round trip) energy efficiency is

$$\eta = 100\left(1-2\frac{E_{LOSSES}}{E_{BR}}\right) = 100\left(1-\frac{P_{C0}}{E_{BR}}(0.19C_0+1)\ln\frac{C_0U_{C0\max}^2}{C_0U_{C0\max}^2-2E_{BR}}\right). \quad (3.18)$$

Fig. 3.12 and Fig. 3.13 illustrate the conversion efficiency versus the capacitance C_0, the intermediate voltage U_{C0inM} and cost of the ultra-capacitor module.

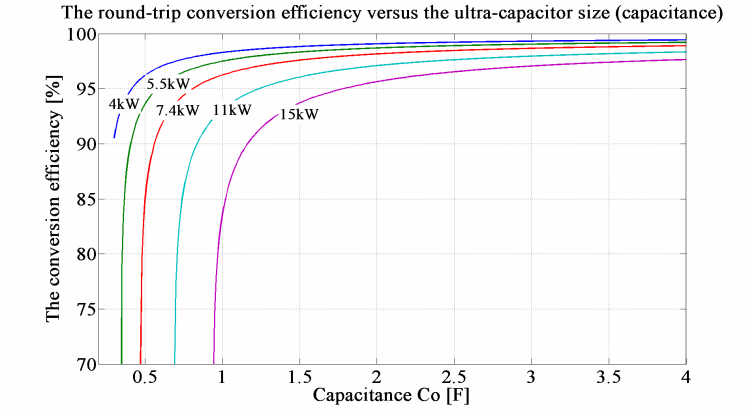
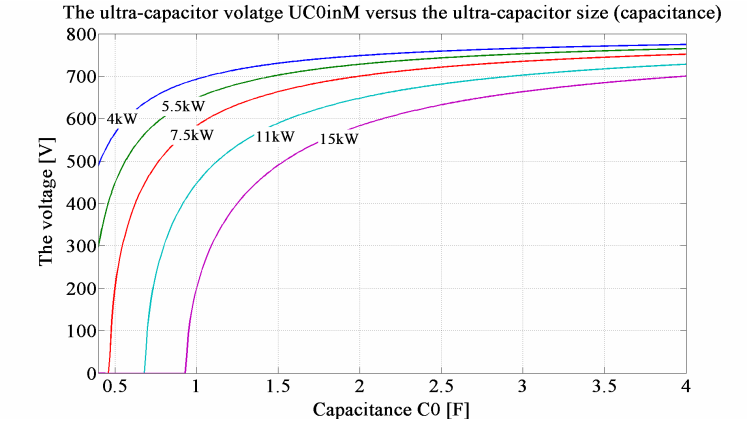
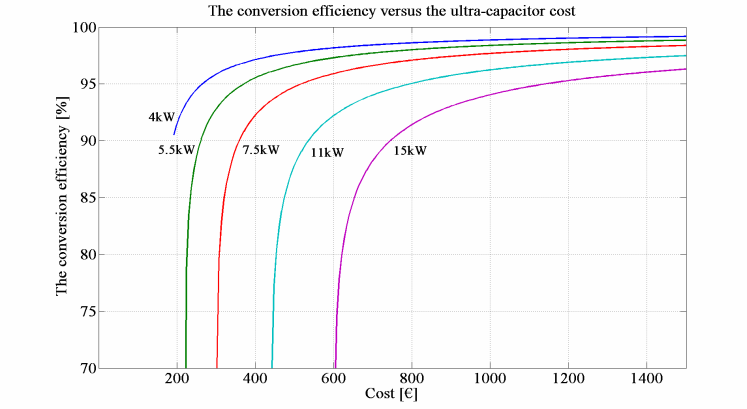


Fig. 3.12 The conversion efficiency and intermediate voltage U_{C0inM} versus the ultra-capacitor rated capacitance C_0 and the ultra-capacitor module cost. The ultra-capacitor module rated voltage U_{C0max}=800V, braking time T_{BR}=20s, the conversion power P_{C0}=4kW, 5.5kW, 7.5kW and 11kW.



(a)



(b)

Fig. 3.13 a) The intermediate voltage U_{C0inM} versus the ultra-capacitor rated capacitance C_0. b) The conversion efficiency versus the ultra-capacitor module cost. The ultra-capacitor module rated voltage U_{C0max}=800V, braking time T_{BR}=20s, the conversion power P_{C0}=4kW, 5.5kW, 7.5kW and 11kW.

The conversion efficiency versus capacitance and voltage is computed from (3.5) and (3.18).The module cost is computed using prediction of 1.28 $/kJ for an ultra-capacitor cell. Taking into account that the module cost is approximately twice of the cell cost, we have 2 €/kJ of total stored energy capacity.

4. THREE-LEVEL INTERFACE DC-DC CONVERTER

4.1. Background and State of the Art

For the sake of better flexibility and higher efficiency of the controlled electric drive with the ultra-capacitor energy storage, the ultra-capacitor cannot be directly connected to the drive dc bus. An interface power converter is necessary. The converter is controlled in the way depending on the system control objectives: control of the dc bus voltage, the ultra-capacitor state of charge, active sharing of the energy between the drive and ultra-capacitor and so on.

Typical dc-dc converter and variable speed drive system is specified as follows:

- The drive is supplied from a three-phase 400V 50Hz industrial network,
- The converter input is the dc bus: V_{BUSmin}=450V, V_{BUSmax}=800V,
- The converter output is the ultra-capacitor: U_{C0min}>250V, U_{C0max}=780V,
- The converter output current ripple: Δi_{C0}≤20%,
- Effective switching frequency: f_{SW_E}≥50kHz,
- Passive components: minimized,
- Efficiency: >95%.

Most of dc-dc converter topologies are based on ordinary two-level single-phase or multiphase interleaved topologies [30]-[35], Fig. 4.1 (a) and (b). The main drawback of these topologies is the fact that the switches are rated for the full dc bus voltage. As the dc bus voltage may go up to 800V, or more, the switches are rated on 1200V. This becomes an issue if the converter switching frequency is high, let us say above 20kHz. Two-level dc-dc converter with soft switching is an alternative [36]. This solution offers lower switching losses. However, since the converter operates in discontinuous conduction mode (DCM), the peak current and ripple current are quite greater than of that one operates in continuous conduction mode (CCM). This causes problem of the inductor losses, particularly the core losses. Fig. 4.1 (c) and (d) shows circuit diagrams of single-phase boost-back and buck-boost topology. Those topologies are used in applications that require large variation of the ultra-capacitor voltage around the dc bus voltage. Isolated dc-dc converter topologies with soft switching have been analyzed in [37], [38]. These topologies are attractive solution when ratio of the dc bus voltage to the ultra-capacitor voltage is high, greater than 2. If the ratio is lower than 2, the efficiency is lower than efficiency of a non-isolated topology.

4.2. Three-Level DC-DC Converter

Three-level converter is well adopted solution in applications with high input voltage and high switching frequency. The switches are stressed on half of the total dc bus voltage. This allow us to use lower voltage rated switches with better switching and conduction performance compared to the switches rated for the full dc bus voltage. Therefore, the converter overall performances, including cost and efficiency, can be significantly better

compared to two-level converters, especially when switching frequency is above 20kHz or MOSFETs are used as the switches.

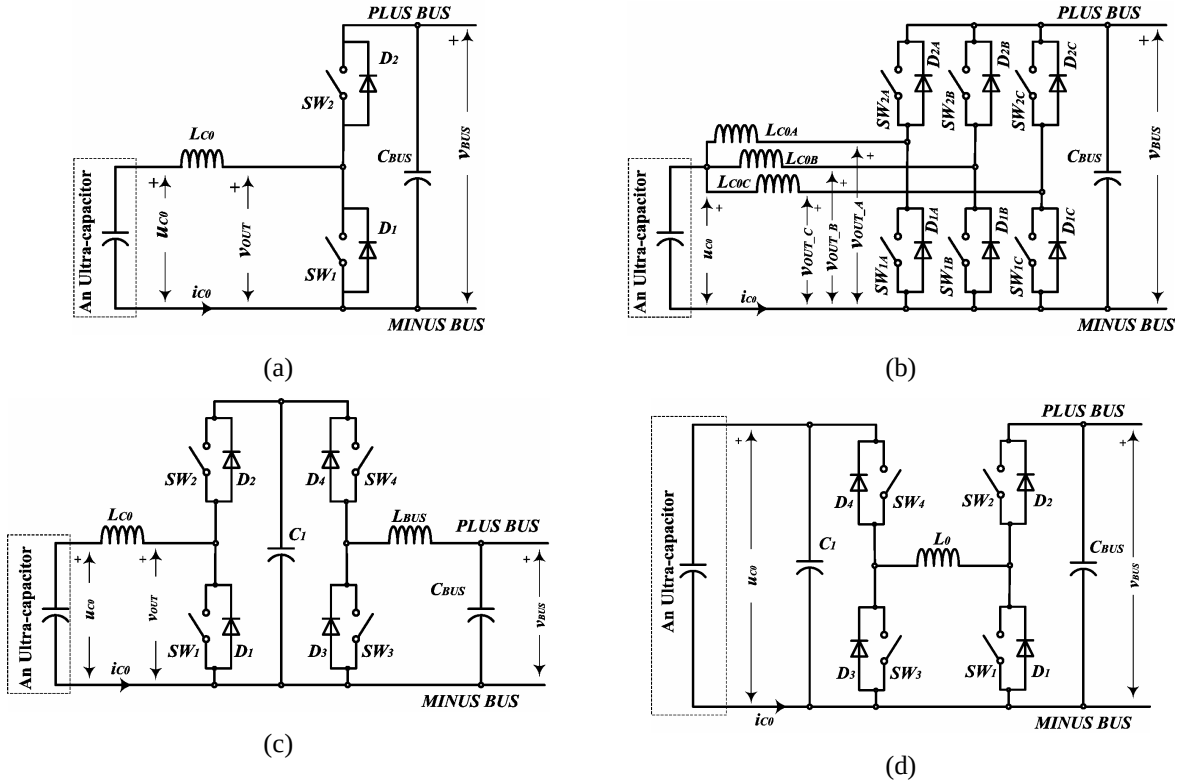


Fig. 4.1 State of the art topologies of the inter-connection dc-dc converters. a) single phase two level , b) three phase two level, c) boost-buck, d) buck-boost.

Fig. 4.2 shows a circuit diagram of a three-level bi-directional dc-dc converter. The converter is composed of four switches SW_{1A}, SW_{1B}, SW_{2A} and SW_{2B} and four freewheeling diodes D_{1A}, D_{1B}, D_{2A} and D_{2B}, an output filter inductor L_{C0} and two input filter capacitors C_{B1} and C_{B2}.

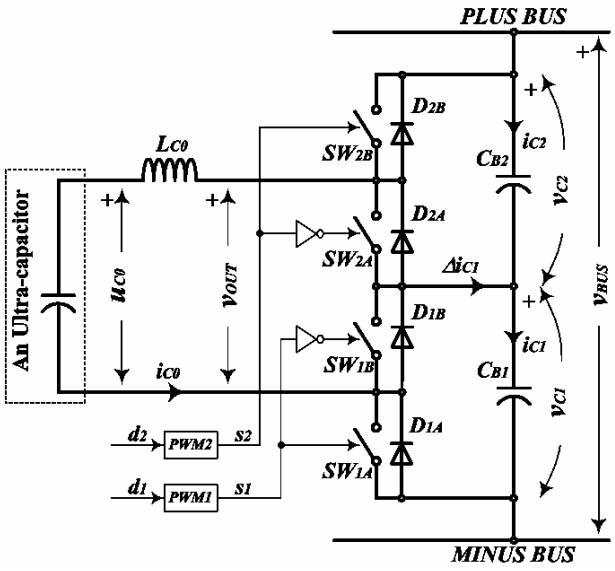


Fig. 4.2 Circuit diagram of the interface bidirectional dc-dc converter based on three-level topology.

The input filter capacitors are series connected and serve as a capacitive voltage divider to split the dc bus voltage v_{BUS} into two equal voltages v_{C1} and v_{C2}. The capacitors mid-point is connected to the switching cell mid-point.

4.2.1. Analysis

The switches SW_{1A} and SW_{1B} states are determined by a switching function s_1 and the complementary function, while the switches SW_{2B} and SW_{2A} states are determined by a switching function s_2 and the complementary function. The switching functions s_1 and s_2 are generated by the pulse width modulators *PWM1* and *PWM2*. The switching functions s_1 and s_2 are

$$s_1(t)=\begin{cases}1, & kT_{SW}<t\le T_{SW}\left(k+\frac{d_1}{2}\right) \quad \& \; T_{SW}\left(k+1-\frac{d_1}{2}\right)<t\le (k+1)T_{SW}\\ 0, & T_{SW}\left(k+\frac{d_1}{2}\right)<t\le T_{SW}\left(k+1-\frac{d_1}{2}\right)\end{cases}$$

$$s_2(t)=\begin{cases}1, & kT_{SW}<t-\frac{T_{SW}}{2}\le T_{SW}\left(k+\frac{d_2}{2}\right) \quad \& \; T_{SW}\left(k+1-\frac{d_2}{2}\right)<t-\frac{T_{SW}}{2}\le (k+1)T_{SW}\\ 0, & T_{SW}\left(k+\frac{d_2}{2}\right)<t-\frac{T_{SW}}{2}\le T_{SW}\left(k+1-\frac{d_2}{2}\right)\end{cases}, \tag{4.1}$$

where k is an integer $k\in[,+\infty)$ and T_{SW} is the switching period. The modulation signals d_1 and d_2 are duty cycles generated by the control circuit. The control circuit controls the ultra-capacitor current i_{C0} and balances the voltages v_{C1} and v_{C2}. The modulation carriers are triangular signals v_{T1} and v_{T2} shifted for π radians and running at the same frequency f_{SW} (see Fig. 4.3). Fig. 4.3 (a) shows the converter waveforms when $d_1=d_2<1/2$, while Fig. 4.3 (b) shows the waveforms when $d_1=d_2>1/2$. Depending on the switches state, four different topological stages can be distinguished, namely A, B, C and D. Equivalent circuit diagrams for these stages are illustrated in Fig. 4.3 (c). The input filter capacitors are modeled as ideal voltage sources v_{C1} and v_{C2}.

The stage A): The converter can be in this stage only if the duty cycles are lower than 1/2. The switches SW_{1B} and SW_{2A} are closed, while the switches SW_{1A} and SW_{2B} are opened. As the current i_{C0} is assumed as positive according to the circuit diagram, the currents i_{1B} and i_{2A} are negative; the freewheeling diodes D_{1B} and D_{2A} are conducting. The output voltage is $v_{OUT}=0$, and therefore the current i_{C0} decreases.

$$\frac{di_{C0}}{dt}=\left(-\frac{u_{C0}}{L_{C0}}\right)<0 \tag{4.2}$$

The stage B): The switches SW_{1A} and SW_{2A} are closed, while the switches SW_{1B} and SW_{2B} are opened. The current i_{1A} is positive and the current i_{2A} is negative; the freewheeling diode D_{2A} is conducting. The filter capacitor C_{B1} is discharged by the current i_{1A}. The output voltage is $v_{OUT}=v_{C1}$. The current i_{C0} decreases or increases. It depends on the ultra-capacitor voltage (duty cycle consequently).

$$\frac{di_{C0}}{dt}=\frac{1}{L_{C0}}(v_{C1}-u_{C0})\begin{cases}>0 & u_{C0}<v_{C1}\\ <0 & u_{C0}>v_{C1}\end{cases} \tag{4.3}$$

The stage C): The switches SW_{1B} and SW_{2B} are closed, while the switches SW_{1A} and SW_{1B} are opened. The current i_{2B} is positive and the current i_{1B} is negative; the freewheeling diode D_{1B} is conducting. The filter capacitor C_{B2} is discharged by the current i_{2B}. The output voltage is $v_{OUT}=v_{C2}$. The current i_{C0} decreases or increases, depending on the duty cycle,

$$\frac{di_{C0}}{dt}=\frac{1}{L_{C0}}\left(v_{C2}-u_{C0}\right)\begin{cases}>0, & u_{C0}<v_{C2}\\ <0, & u_{C0}>v_{C2}\end{cases}. \tag{4.4}$$

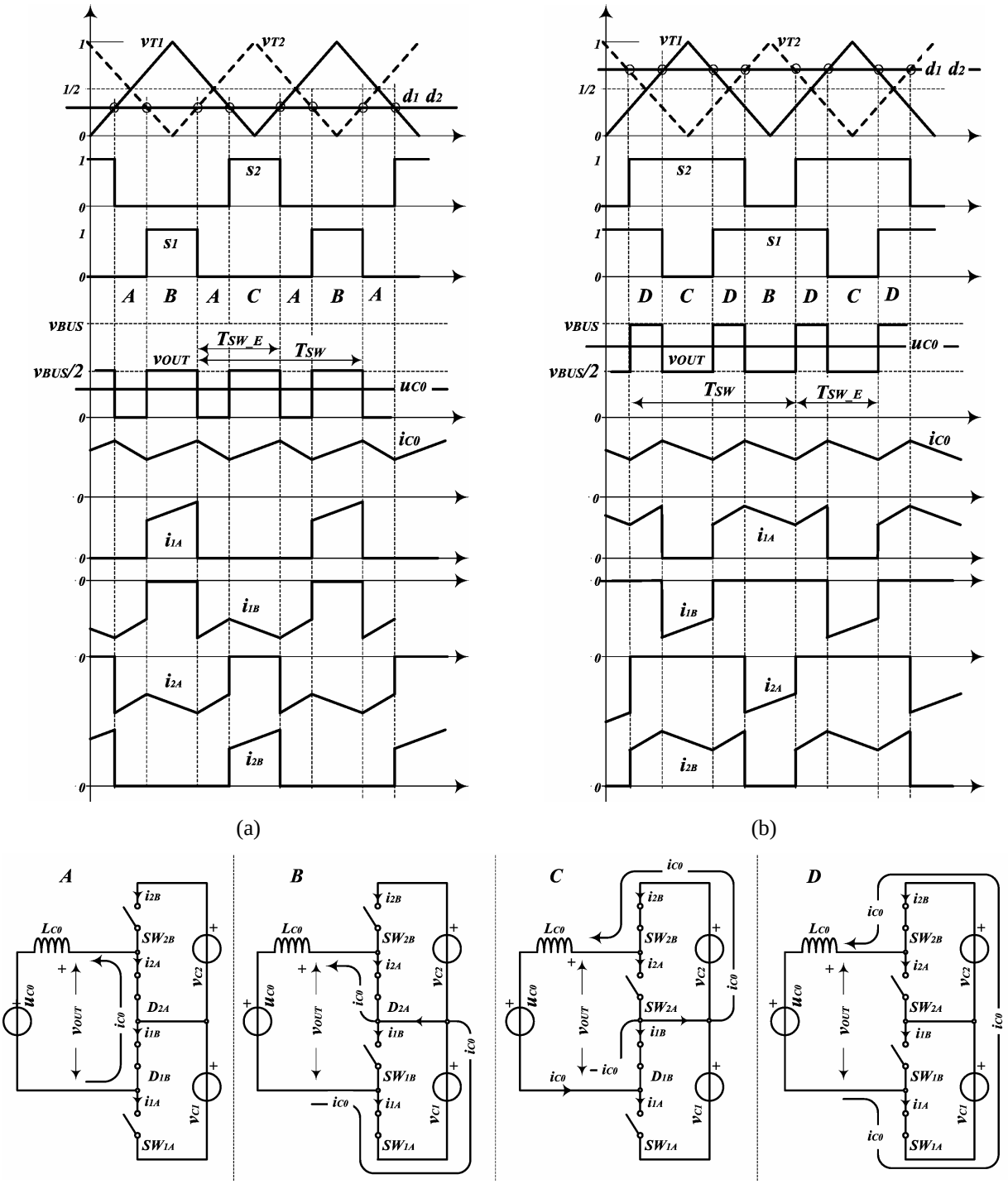


Fig. 4.3 Different topological stages of the three-level dc-dc converter: a) ideal waveforms for d<1/2, b) ideal waveforms for d>1/2, c) equivalent circuits for the stages A, B, C and D.

The stage D): The converter can be in this stage only if the duty cycles are greater than 1/2. The switches SW_{1A} and SW_{2B} are closed, while the switches SW_{1B} and SW_{2A} are opened. The switches currents i_{1A} and i_{2B} are positive. The output voltage is $v_{OUT}=v_{BUS}$, and therefore the current i_{C0} increases.

$$\frac{di_{C0}}{dt}=\frac{1}{L_{C0}}\left(v_{BUS}-u_{C0}\right)>0 \tag{4.5}$$

Instantaneous output voltage v_{OUT} can be expressed as

$$v_{OUT}(t)=v_{BUS}s_1(t)+v_{C1}\left(s_1(t)-s_2(t)\right), \tag{4.6}$$

where $s_1(t)$ and $s_2(t)$ are the switching functions (4.1).

Assuming that $d_1=d_2=d$ and $v_{C1}=v_{C2}=v_{BUS}/2$ (this is a case when the converter is well designed and controlled), from (4.1)-(4.5) and Fig. 4.3 follows that

$$\begin{aligned} v_{OUT}\left(t+\frac{T_{SW}}{2}\right)&=v_{OUT}(t),\\ u_{C0}&=\frac{1}{T_{SW}}\int_0^{T_{SW}}v_{OUT}(t)dt=v_{BUS}d\ . \end{aligned} \tag{4.7}$$

As (4.7) shows, the output voltage is periodic function with period $T_{SW}/2$. That means the effective fundamental frequency of the output voltage v_{OUT} and therefore the output current i_{C0} is twice switching frequency, $f_{SW\text{-}E}=2f_{SW}$. This has a significant influence on design of the inductor L_{C0}, as it will be shown in the following section.

4.2.2. Filter Inductor L_{C0}

Two main parameters are relevant for the inductor design: 1) the inductance L_{C0} and 2) losses P_{LC0}.

4.2.2.1. Inductance L_{C0}

To compute the inductance L_{C0}, peak to peak current ripple Δi_{C0max} has to be defined. From (4.2)-(4.5) and the assumptions $d_1=d_2=d$ and $v_{C1}=v_{C2}=v_{BUS}/2$ one finds the current ripple as a function of the duty cycle d,

$$\Delta i_{C0}(d)=\begin{cases}\dfrac{v_{BUS}}{L_{C0}2f_{SW}}(1-2d)d, & d\le 1/2\\[2ex] \dfrac{v_{BUS}}{L_{C0}2f_{SW}}(2d-1)(1-d), & d\ge 1/2\end{cases}. \tag{4.8}$$

Maximum of the current ripple is

$$\Delta i_{C0\max}=\Delta i_{C0}(d)\Big|_{\substack{d=1/4\\ d=3/4}}=\frac{v_{BUS}}{L_{C0}f_{SW}16}. \tag{4.9}$$

From (4.9) one finds the inductance L_{C0}

$$L_{C0} \geq \frac{V_{BUS\max}}{\Delta i_{C0\max} f_{SW} 16}, \tag{4.10}$$

where the dc bus voltage (input voltage) is maximum voltage $v_{BUS}=V_{BUSmax}$. The current ripple Δi_{C0max} is given as a design criterion.

Please note that the inductance (4.10) is 25% of the inductance of two-level dc-dc converter for the same current ripple Δi_{C0max} and the same switching frequency f_{SW}. That means the inductor volume is 25% of that of the conventional converter. Fig. 4.4 shows the current ripple versus duty cycle for the ordinary two-level converter and the three-level converter.

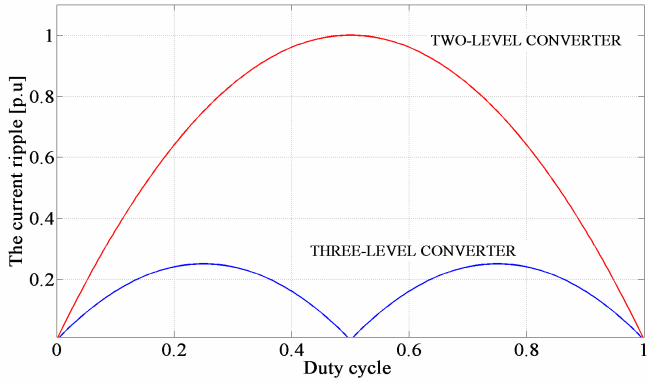


Fig. 4.4 The inductor current ripple Δi_{C0} versus duty cycle d (the duty cycle corresponds to the ultra-capacitor voltage u_{C0}). The ripple is normalized on the maximum current ripple when two-level dc-dc converter is used.

4.2.2.2. The Inductor Losses

The inductor losses consist of the copper (winding) losses and the core losses. Both of them depends on the inductor instantaneous current. The inductor current can be expressed as

$$i_{C0}(t) = I_{C0(DC)} + \sum_{n=1}^{\infty} I_{C0(2nf_{SW})} \sin\left(2n\omega_{SW}t + \varphi_{(2n\omega_{SW})}\right), \tag{4.11}$$

where $\omega_{SW} = 2\pi f_{SW}$. The converter switching frequency is f_{SW} and n is the harmonic order.

The copper losses can be found in a general form

$$P_{CU} = \sum_{n=0}^{n} I_{C0RMS(n)}^2 R_{Cu(n2\,f_{SW})}, \tag{4.12}$$

where $R_{Cu(n)}$ is the inductor winding resistance that depends on the frequency.

The core losses can be defined in similar way,

$$P_C \cong \sum_{n=0}^{n} I_{C0RMS(n)}^2 R_{C(n2\,f_{SW})}, \tag{4.13}$$

where $R_{C(2nfsw)}$ is the core equivalent resistance that models the core losses as a function of the frequency [92]-[98]. Here we have to highlight that the core losses model

(4.13) is an approximation of the real core losses [99]. The core losses model (4.13) was extensively discussed in [92]. Experimental verification of (4.13) was also given.

The inductor losses model (4.12) and (4.13) takes into account harmonics of the inductor current. To simplify analysis, one can substitute the current ripple by an equivalent sinusoidal current with the RMS value and frequency same as the total current ripple. Such an approach is not completely correct, but it is sufficient for simplified calculation.

RMS value of the equivalent sinusoidal current ripple is

$$I_{C0RMS(2f_{SW})} \cong \Delta i_{C0\max}\frac{4}{\sqrt{3}}\begin{cases}(1-2d)d, & 0\le d\le 1/2\\ (2d-1)(1-d), & 1/2\le d\le 1\end{cases}, \tag{4.14}$$

where Δi_{C0max} is the current ripple (4.9).

The inductor average current (dc component) is computed from output power P_{C0} and the ultra-capacitor voltage u_{C0} as

$$I_{C0}=\frac{P_{C0}}{u_{C0}}=\frac{P_{C0}}{v_{BUS}d}. \tag{4.15}$$

Substituting (4.14) and (4.15) into (4.12) and (4.13) yields the inductor total losses,

$$\begin{aligned}P_{LC0}(P_{C0},d)\cong & R_{DC}\left(\frac{P_{C0}}{v_{BUS}d}\right)^2\\ &+\left(R_{Cu(2f_{SW})}+R_{C(2f_{SW})}\right)\Delta i_{C0\max}^2\frac{16}{3}\begin{cases}(1-2d)^2d^2, & 0\le d\le 1/2\\ (2d-1)^2(1-d)^2, & 1/2\le d\le 1\end{cases}\end{aligned}, \tag{4.16}$$

where R_{DC} is the inductor resistance at low frequency, while $R_{Cu(2fsw)}$ and $R_{C(2fsw)}$ are the inductor winding resistance and the core equivalent resistance at twice switching frequency.

4.2.3. Filter Capacitors C_{B1}, C_{B2}

The filter capacitors are designed for two main criteria: 1) the capacitors peak and RMS current, and 2) the input voltage ripple. For simplicity of the analysis one can neglected the current ripple ($\Delta i_{C0}\cong 0$), and assume that $d_1=d_2=d$ and $v_{C1}=v_{C2}=v_{BUS}/2$.

Fig. 4.5(a) illustrates waveforms of the currents i_{C1}, i_{C2} and the voltages v_{C1}, v_{C2}, when $d<1/2$. Fig. 4.5 (b) illustrates the case when $d>1/2$. The capacitors current and the voltage ripple are periodic functions with a period $T_{SW}=1/f_{SW}$.

4.2.3.1. Peak and RMS Current

From Fig. 4.5 one can define the capacitors instantaneous current as follows

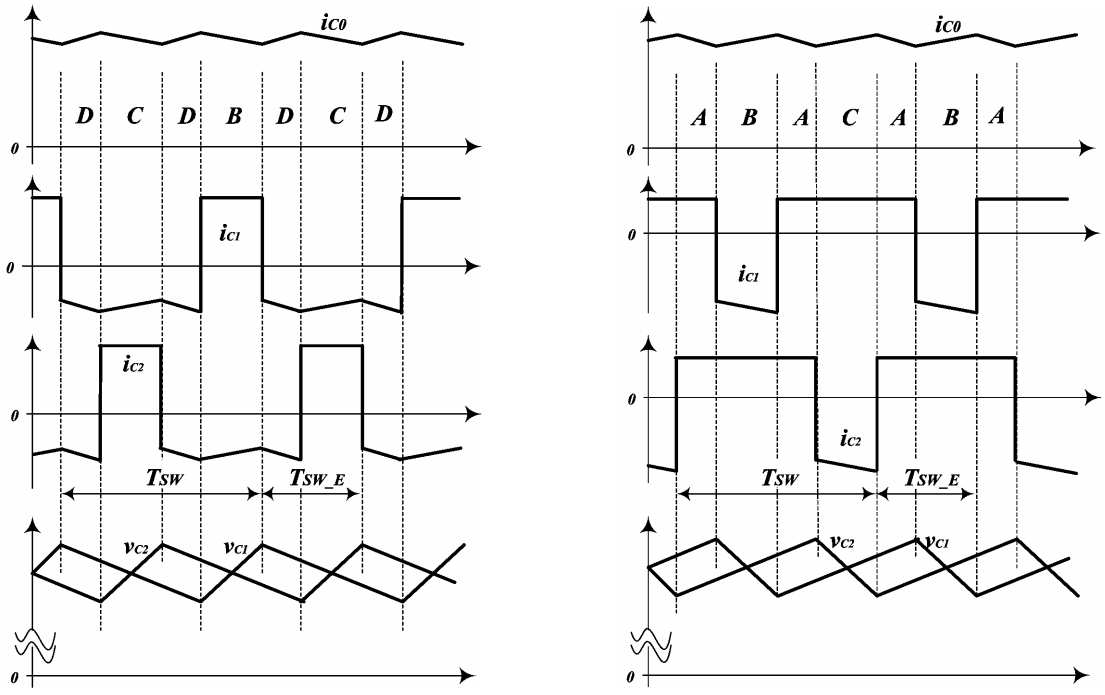
$$\begin{aligned}i_{C1}(t)&=i_{C0}(d-s_1(t))\\ i_{C2}(t)&=i_{C0}(d-s_2(t))\end{aligned}. \tag{4.17}$$

As the dc-dc converter is loaded by constant power P_{C0}, the capacitors current has to be defined as a function of the power P_{C0} and the ultra-capacitor voltage u_{C0}. Using the assumption $\Delta i_{C0}\cong 0$ and substituting (4.7) and (4.15) into (4.17) yields the peak current

$$i_{C1peak\max} = i_{C2peak\max} = \frac{P_{C0}}{v_{BUS}} \max\left(1, \frac{(1-d_{\min})}{d_{\min}}\right), \tag{4.18}$$

and RMS current

$$I_{C1RMS} = I_{C2RMS} = \frac{P_{C0}}{v_{BUS}} \sqrt{\frac{(1-d)}{d}}\,. \tag{4.19}$$



(a) (b)

Fig. 4.5 The filter capacitors currents i_{C1} and i_{C2} and the voltages v_{C1} and v_{C2} at different duty cycle: a) d<1/2 and b) d>1/2.

Maximum of the capacitors RMS current is

$$I_{C1RMS\max} = I_{C2RMS\max} = \frac{P_{C0}}{v_{BUS}} \sqrt{\frac{1-d_{\min}}{d_{\min}}}\,. \tag{4.20}$$

The capacitors losses are

$$P_{C1} = P_{C1} = \left(\frac{P_{C0}}{v_{BUS}}\right)^2 \frac{(1-d_{\min})}{d_{\min}} R_{ESR}\,, \tag{4.21}$$

where R_{ESR} is the capacitors equivalent series resistance.

4.2.3.2. Input Voltage (DC Bus Voltage) Ripple

For this analysis, the filter capacitors are taken as identical, $C_{B1}=C_{B2}=C$. The input voltage peak to peak ripple is

$$\Delta v_{BUS}(d)=\frac{P_{C0}}{C v_{BUS} 2 f_{SW}}\begin{cases}(1-2d), & d\le 1/2\\ (2d-1)\dfrac{(1-d)}{d}, & d\ge 1/2\end{cases}. \tag{4.22}$$

Comparison of the input voltage ripple of an ordinary two-level and the proposed three-level dc-dc converter is given in Fig. 4.6 The voltage ripple is computed for the same conditions: the capacitance C, output power P_{C0} and switching frequency f_{SW}. As seen from the graph, the three-level converter ripple is quite lower than that of two-level converter. The ripple ratio depends on the duty cycle range. If the duty cycle is in a range 1/2 to 1, the voltage ripple of the three-level converter is roughly 20% of that of two-level converter. That means the filter capacitor can be five times smaller than that of two-level converter for the same voltage ripple Δv_{BUS}.

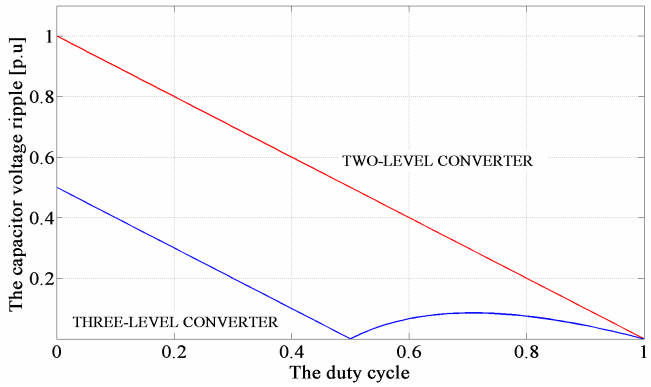


Fig. 4.6 The capacitors voltage ripple Δv_{BUS} versus duty cycle d (duty cycle corresponds to the ultra-capacitor voltage u_{C0}). The conversion power P_{C0} and the dc bus voltage V_{BUS} are considered as constant. The ripple is normalized on the maximum voltage ripple when two-level dc-dc converter is used.

Maximum of the input voltage ripple is

$$\Delta v_{BUS\max}=\frac{P_{C0}}{C v_{BUS} 2 f_{SW}}\begin{cases}(1-2d_{\min}) & d\le 1/2\\ \left(3-2\sqrt{2}\right)_{d=\sqrt{2}/2} & d\ge 1/2\end{cases}. \tag{4.23}$$

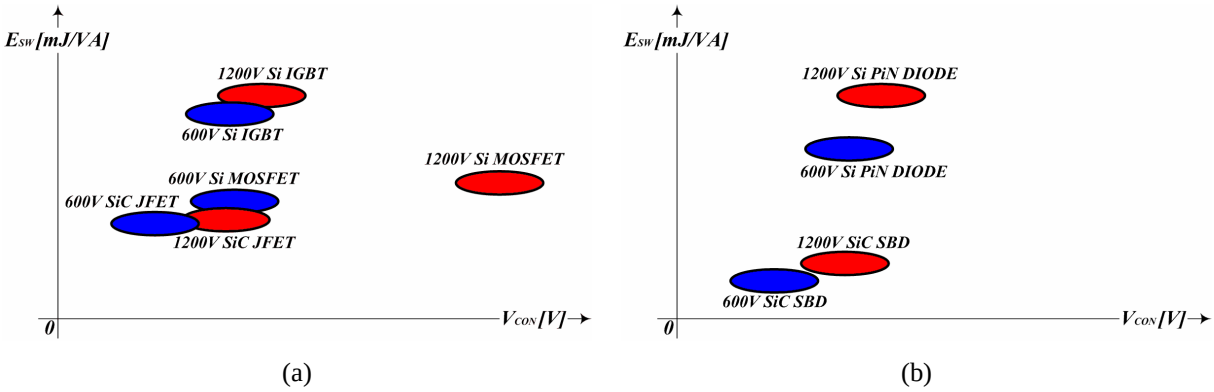
The capacitance C is computed from (4.23) as

$$C\ge \max\left(\frac{P_{C0}(1-d_{\min})}{v_{BUS}\Delta v_{BUS\max} 2 f_{SW}}, \frac{P_{C0}\left(3-2\sqrt{2}\right)}{v_{BUS}\Delta v_{BUS\max} 2 f_{SW}}\right). \tag{4.24}$$

4.3. Design and Selection of the Active Components

4.3.1. Advanced Semiconductor Switches

The most common power semiconductor switches used in switch mode power converters are Si based insulated gate bipolar transistor (IGBT), metal oxide semiconductor field effect transistors (MOSFET) and PiN diodes [104]. In last decade, we have seen intensive development of SiC based power semiconductor switches, such as Schottky barrier diode (SBD) and junction filed effect transistor (JFET) [105]. Fig. 4.7 illustrates comparison of performance of the most used semiconductor switches. The conduction losses (on-state voltage V_{CON}) and switching losses of three types of active switches, Si IGBT, Si MOSFET and SiC JFET are compared at two different voltage rating, 600V and 1200V. Comparison is illustrated in Fig. 4.7 (a). Regarding overall performance, switching and conduction, in both voltage ranges the SiC JFET is superior. 600V rated MOSFET and IGBT have similar conduction performances, while the MOSFET is superior regarding switching performance. In 1200V range, the MOSFET has superior switching performance in comparison to the IGBT. The situation for conduction performance is opposite; the IGBT is superior. Here, we have to highlight that technology of 600V and 1200V MOSFET is different. In 600V range, super-junction technology is dominant [101]. This technology offers significant improvement of the switch conduction performance. However, there is not possibility to implement the super-junction technology in 1200V range.



(a) (b)

Fig. 4.7 Advanced power semiconductor switches performances versus rated voltage. a) Active switches and b) diodes.

600V and 1200V rated Si PiN and SiC SBD switching diodes are compared. Note that switching losses of SiC SBD are quite lower than that of Si PiN diode. The difference in on-state voltage is less significant. SiC PiN diode is not considered because such type of diode is applicable in very high voltage rather than in low voltage applications.

4.3.2. Voltage Rating

The switches and diodes voltage rating is defined by the switch transient blocking voltage

$$V_{SW(\max)} = V_{D(\max)} = \frac{V_{BUS(\max)}}{2} + \Delta V \,, \tag{4.25}$$

where ΔV is the commutation over-voltage [100].

Since the switch voltage rating is a half of the dc bus voltage, a device rated for 500 to 600V can be used. It could be either 550V CoolMOSFET or 600V IGBT. The first one offers better switching and similar conduction performance compared to the IGBT [101]. However, the intrinsic FWD of the CollMOSFET has inferior characteristics in comparison to the PiN diode used in the IGBT module. This issue could be solved by the use of some complex topology, but it cause additional expenses and losses. Thus, 600V IGBT with an integrated FWD is used as the switch.

4.3.3. Conduction and Switching Losses

The switches and diodes output characteristics are approximated by the first order functions

$$\begin{aligned} v_{SW} &= v_{SW}(i_{SW}) \cong V_{SW0} + \frac{\partial F(i_{SW})}{\partial i_{SW}} i_{SW} = V_{SW0} + r_{SW} i_{SW}, \\ v_D &= v_D(i_D) \cong V_{D0} + \frac{\partial v_D(i_D)}{\partial i_D} i_D = V_{D0} + r_D i_D, \end{aligned} \tag{4.26}$$

were V_{SW0} and r_{SW} are the IGBT threshold conduction voltage and dynamic resistance. V_{D0} and r_D are the freewheeling diode (FWD) threshold conduction voltage and dynamic resistance.

The switch and FWD conduction losses can be computed from (4.26) as

$$\begin{aligned} P_{SW(CON)} &= \frac{1}{T_{SW}} \int_0^{T_{SW}} v_{SW} i_{SW} dt \cong V_{SW0} I_{SW(AV)} + r_{SW} I^2_{SW(RMS)}, \\ P_{D(CON)} &= \frac{1}{T_{SW}} \int_0^{T_{SW}} v_D i_D dt \cong V_{D0} I_{D(AV)} + r_D I^2_{D(RMS)}. \end{aligned} \tag{4.27}$$

Commutation losses are

$$\begin{aligned} P_{SW(SW)} &= \frac{1}{T_{SW}} \left(E_{ON}\left(v_{SW(ON)}, i_{SW(ON)}\right) + E_{ON}\left(v_{SW(OFF)}, i_{SW(OFF)}\right) \right) \cong f_{SW} \frac{(E_{ON} + E_{ON})}{V_N I_N} v_{SW} i_{SW}, \\ P_{D(SW)} &\cong f_{SW} \frac{E_Q}{V_N I_N} v_D i_D, \end{aligned} \tag{4.28}$$

where E_{ON}, E_{OFF} and E_Q denotes turn on, turn off and reverse recovery commutation energy, which are given at the rated voltage V_N, current I_N and 125°C junction temperature.

Let us consider that the current i_{C0} is positive (the ultra-capacitor is charged). The switches and freewheeling diodes current is determined by the current i_{C0} and the switching functions s_1 and s_2 as follows,

$$\begin{aligned} i_{SW1A} &= i_{C0}s_1(t) & i_{SW1B} &= 0 \\ i_{SW2A} &= 0 & i_{SW2B} &= i_{C0}s_2(t) \\ i_{D1A} &= 0 & i_{D1B} &= i_{C0}(1-s_1(t)) \\ i_{D2A} &= i_{C0}(1-s_2(t)) & i_{D2B} &= 0 \end{aligned}. \tag{4.29}$$

The losses are computed from (4.15), (4.27), (4.28) and (4.29) as

$$P_{SW1A} = P_{SW2B} = \underbrace{\left(V_{SW0}\frac{P_{C0}}{v_{BUS}} + r_{SW}\frac{P_{C0}^2}{v_{BUS}^2 d}\right)}_{CONDUCTION} + \underbrace{\frac{1}{2}\frac{P_{C0}}{V_N I_N d}(E_{ON}+E_{OFF})f_{SW}}_{SWITCHING}, \tag{4.30}$$

$$P_{SW1B} = P_{SW2A} = 0$$

$$P_{D2A} = P_{D1B} = \underbrace{\left(V_{D0}\frac{P_{C0}}{v_{BUS}} + r_D\frac{P_{C0}^2}{v_{BUS}^2 d}\right)\frac{(1-d)}{d}}_{CONDUCTION} + \underbrace{\frac{1}{2}\frac{P_{C0}}{V_N I_N d}E_Q f_{SW}}_{SWITCHING}. \tag{4.31}$$

$$P_{D1A} = P_{D2B} = 0$$

Remark: The losses equations (4.30) and (4.31) have been derived assuming that the ultra-capacitor current is ripple-free ($\Delta i_{C0} \cong 0$) and duty cycles are balanced ($d_1=d_2=d$).

If the current is negative (the ultra-capacitor is discharged), the losses have the same form as (4.30) and (4.31) but redistributed to the complementary devices. When the duty cycle is varying in time, as it is a case when the ultra-capacitor is charged/discharged, the total loses profile can easily be computed from (4.30) and (4.31) substituting the ultra-capacitor current profile (3.10) and (3.11).

4.4. The DC-DC Converter Design Example

A 5.5 kW prototype was designed (see Fig. 4.8) and the proposed bi-directional dc-dc converter experimentally verified. The converter specification and parameters of the selected main components are given in TABLE 4-1. Active power components (IGBTs and FWDs) were selected for the target switching frequency, dc bus voltage and ultra-capacitor current. The filter inductor L_{C0} and input filter capacitors C_{B1} and C_{B2} were designed and selected according to the specification in TABLE 4-1 and the criteria (4.10) and (4.24). R_{DC} is the winding resistance at low frequency and R_{AC} is the winding resistance at switching frequency, which was computed taking the high frequency resistance factor of 20 [102]. The resistance R_C is the core equivalent resistance as a model of the core losses (4.16). The core resistance was computed at the inductor rated current, using the manufacture datasheet [103].

The inductor losses were computed from (4.16) and the parameters in TABLE 4-1. Fig. 4.9 (a) shows 3-D graph of the total inductor loses versus output power and duty cycle. As seen, the core losses are dominant in most of the operating region. The core losses and the total losses reach a peak at duty cycle of $d=3/4$ and $d=1/2$ and full load. The first peak corresponds to the maximum current ripple (4.9) (and core losses), while the second one corresponds to the maximum conversion power (and low frequency copper losses).

The IGBTs and FWDs losses were computed from (4.30), (4.31) and data given in TABLE 4-1. Fig. 4.10 shows 3-D graph of the total losses (switching and conduction) versus conversion power and duty cycle, where the duty cycle corresponds to the ultra-capacitor

voltage. As seen from the graph, the losses reach maximum of roughly *125W* at the maximum output power P_{OUT}=5500W and minimum duty cycle d=1/2.

TABLE 4-1. The converter specification

Nominal power				P_{C0}=5500W	
DC bus nominal voltage				V_{BUS}=570V	
DC bus braking voltage				V_{BUSmax}=700V	
DC bus ride-through voltage				V_{BUSmin}=450V	
Switching frequency				f_{SW}=25kHz	
The current ripple				Δi_{C0}=3A	
IGBT/FWD 600V 30A					
V_{CE}	R_{CE}	*E_{ON}+E_{OFF}	V_{DF}	r_{DF}	*E_{QF}
0.8V	27mΩ	80µJ/A	0.9 V	20 mΩ	10µJ/A
*Switching losses at V_N=300V T_J=150˚C					
FILTER INDUCTOR L_{C0}				CAPACITOR C_{B1}, C_{B2}	
High Flux Powder Core (2x) 58192-A2				MKP EPCOS B32774D4106	
L	R_{DC}	R_{AC}	R_C	C	ESR
580µH	38mΩ	0.8Ω	3Ω	2x10µF	3.75mΩ

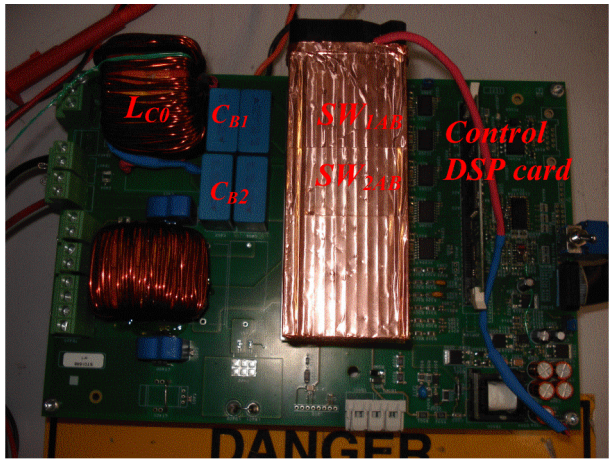


Fig. 4.8 Prototype of 5.5kW three-level dc-dc converter.

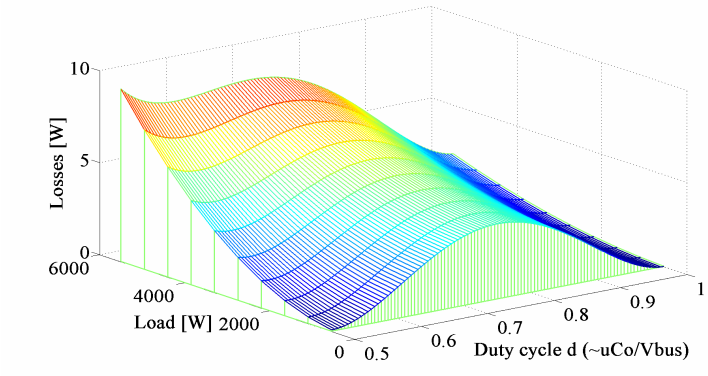


Fig. 4.9 The inductor losses versus the load power P_{C0} and duty cycle (that is proportional to the ultra-capacitor voltage $d \approx u_{C0}/v_{BUS}$). v_{BUS}=700V and the inductor core temperature T_C=100°C.

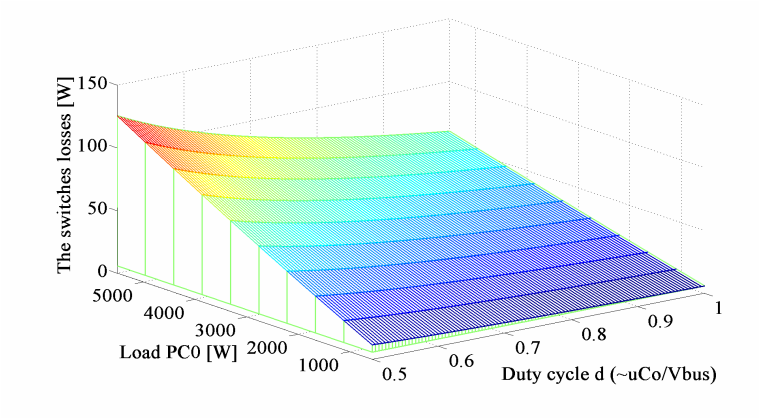
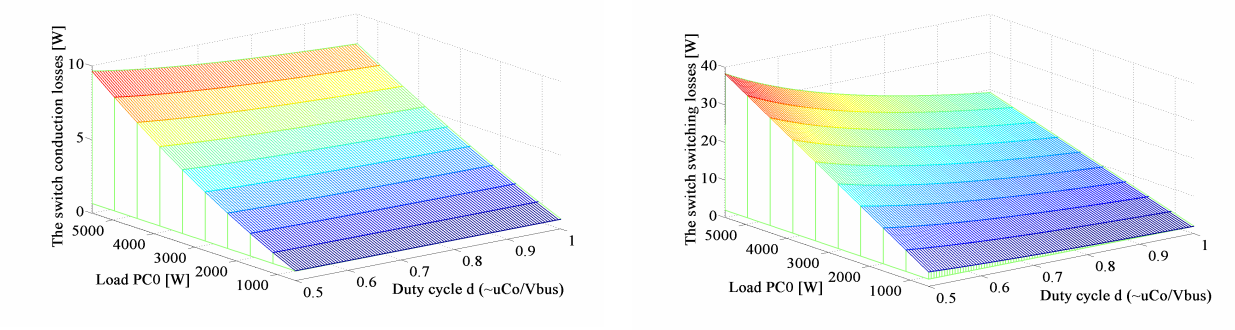


Fig. 4.10 The switches total losses versus the load power P_{C0} and duty cycle (that is proportional to the ultra-capacitor voltage $d \approx u_{C0}/v_{BUS}$). The dc bus voltage v_{BUS}=700V, the switch junction temperature T_J=150°C.

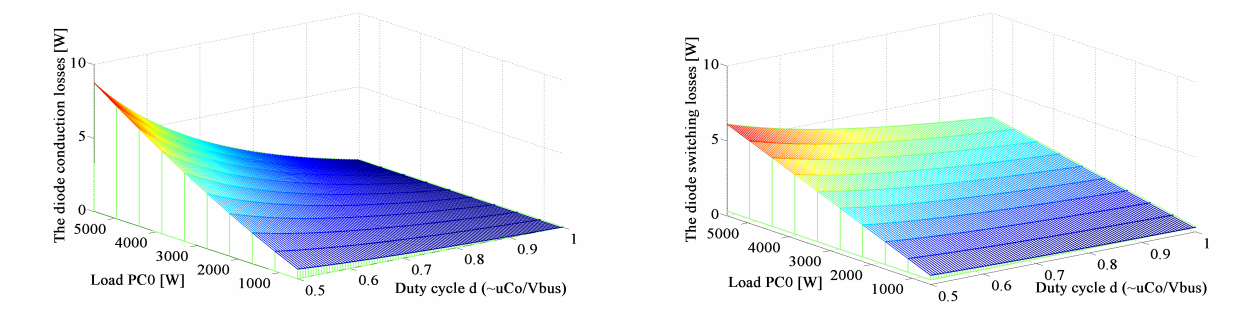


(a) (b)

Fig. 4.11 The IGBT losses versus the load power P_{C0} and duty cycle (that is proportional to the ultra-capacitor voltage $d \approx u_{C0}/v_{BUS}$). a) Conduction losses, b) switching losses. The dc bus voltage v_{BUS}=700V, the switch junction temperature T_J=150°C.

Fig. 4.11 and Fig. 4.12 show graph of the IGBT and FWD losses versus conversion power and duty cycle. The IGBT switching losses are dominant and quite dependent on the duty cycle. In contrast to this, the IGBT conduction losses are almost constant overall whole range of the duty cycle. The FWD losses, particularly conduction losses vary significantly with the duty cycle.

Fig. 4.13 shows the converter efficiency versus output power and duty cycle. This calculation shows that the converter efficiency is quite high, from 95% (at minimum output power of 550W and duty cycle of 3/4) up to 99% at minimum output power and maximum duty cycle (d=1). In this calculation, the filter capacitors C_{B1} and C_{B2} losses and the control circuit and gate drivers' losses were neglected. The filter capacitors losses are quite small, below 1W in the worst case (d=1/2 and maximum power). The control circuit and the gate drivers' losses were not calculated.



(a) (b)

Fig. 4.12 The FWD losses versus the load power P_{C0} and duty cycle (that is proportional to the ultra-capacitor voltage $d \approx u_{C0}/v_{BUS}$). a) Conduction losses, b) switching losses. The dc bus voltage v_{BUS}=700V, the switch junction temperature T_J=150°C.

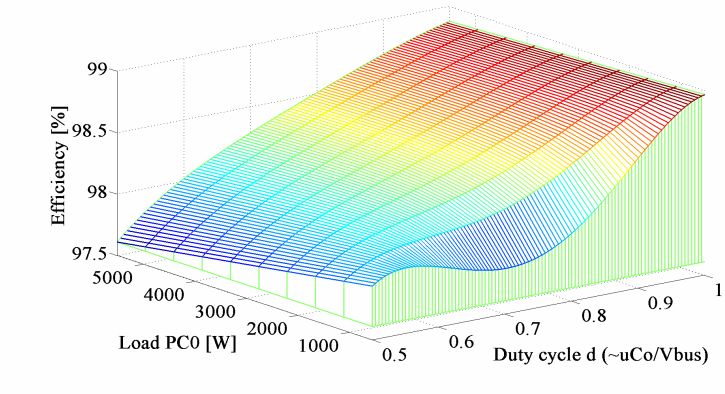
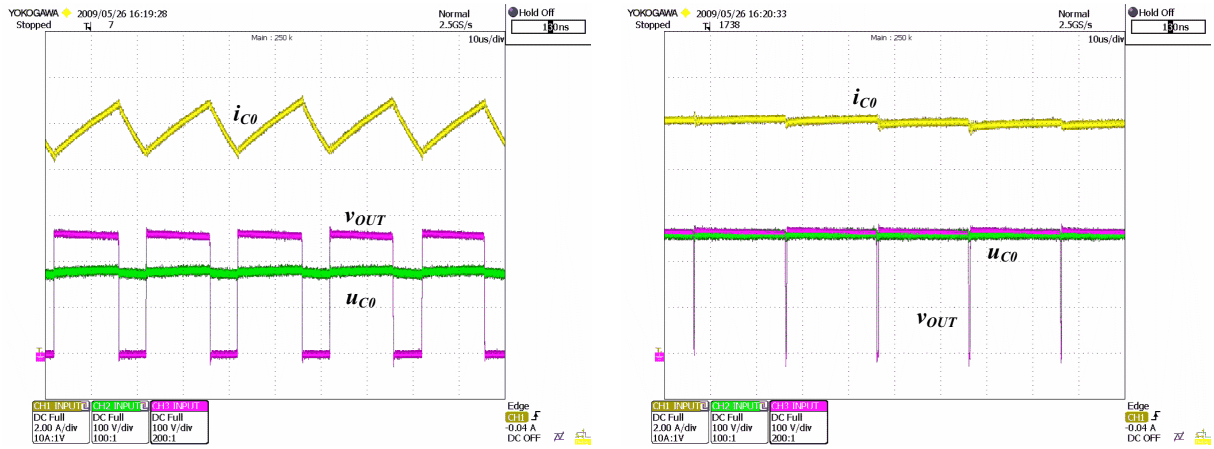


Fig. 4.13 The switches losses versus the load power P_{C0} and duty cycle (that is proportional to the ultra-capacitor voltage $d \approx u_{C0}/v_{BUS}$). The dc bus voltage v_{BUS}=700V, the switch junction temperature T_J=150°C, the inductor core temperature T_C=100°C.

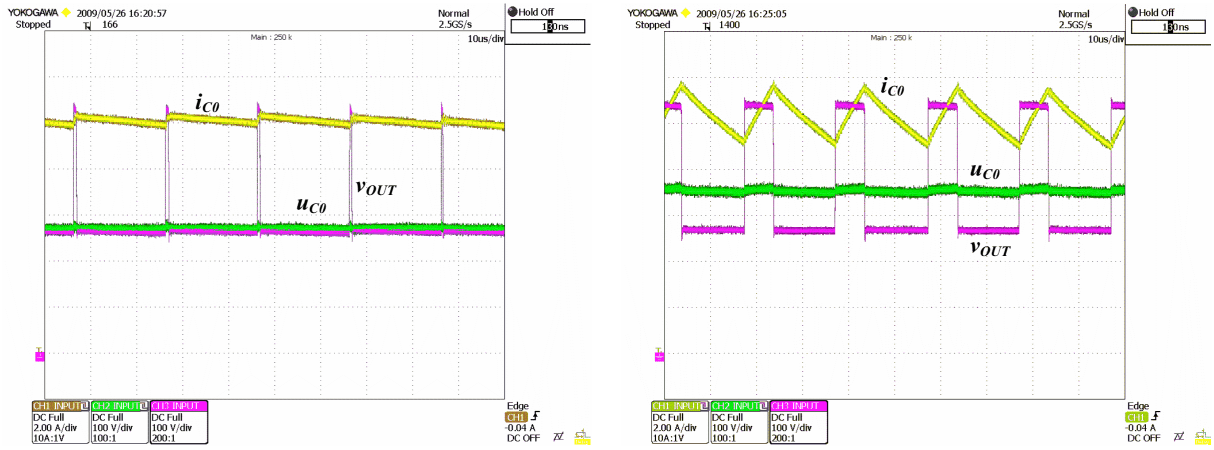
Fig. 4.14 and Fig. 4.15 show waveforms of the converter output voltage v_{OUT}, the ultra-capacitor voltage u_{C0} and the current i_{C0} when the ultra-capacitor voltage u_{C0} takes different value. Fig. 4.14 (a) and Fig. 4.14 (b) show the waveforms when $u_{C0}<v_{BUS}/2$ ($d<1/2$). The output voltage takes discreet value of zero and $v_{BUS}/2$, which corresponds to the topological stages A, B and C (Fig. 4.3).

Fig. 4.15 (a) and Fig. 4.15 (b) show the waveforms when $u_{C0}>v_{BUS}/2$ ($d>1/2$). The output voltage v_{OUT} takes discreet value of $v_{BUS}/2$ or v_{BUS}, which corresponds to the topological stages B, C and D (Fig. 4.3). Fig. 4.14 (b) and Fig. 4.15 (b) show the waveforms when the ultra-capacitor voltage is slightly lower or greater than $v_{BUS}/2$. In the both cases the current ripple almost disappeared, as given in (4.8).



(a) (b)

Fig. 4.14 Experimental waveforms of the output voltage v_{OUT} [100V/div] the ultra-capacitor current i_{C0} [2A/div] and the ultra-capacitor voltage u_{C0} [100V/div] for different duty cycle d. a) d<1/2, b) d=1/2- ε, where ε≈0. v_{BUS}=500V, $i_{C0(AV)}$=10A, L_{C0}=600μH, f_{SW}=25kHz.



(a) (b)

Fig. 4.15 Experimental waveforms of the output voltage v_{OUT} [100V/div] the ultra-capacitor current i_{C0} [2A/div] and the ultra-capacitor voltage u_{C0} [100V/div] for different duty cycle d. a) d=1/2+ ε where ε≈0, b) d >1/2. v_{BUS}=500V, $i_{C0(AV)}$=10A, L_{C0}=600μH, f_{SW}=25kHz.

Fig. 4.16 (a-c) shows waveforms of the output current and ac component of the voltages v_{C1}, v_{C2} and v_{BUS} when the duty cycle takes different values; a) $d\cong1/4$, b) $d\cong1/2$, c) $d\cong3/4$. Noise in the voltage waveforms is the commutation noise picked up by the active voltage probes that were used to measure the capacitor voltages. The output current ripple and dc bus voltage ripple are practically disappeared as the duty cycle approaches 1/2.

Fig. 4.16 (d-f) shows the output current, the ac component of the voltages v_{C1} and v_{C2}, and the capacitors mid-point current Δi_C when the duty cycle takes different values, d) $d\cong1/4$, e) $d\cong1/2$, f) $d\cong3/4$. The capacitors mid-point current Δi_C is alternative current having symmetrical positive and negative segments. Spikes that are seen in the current waveforms (the red ellipses) are the FWD reverse recovery current.

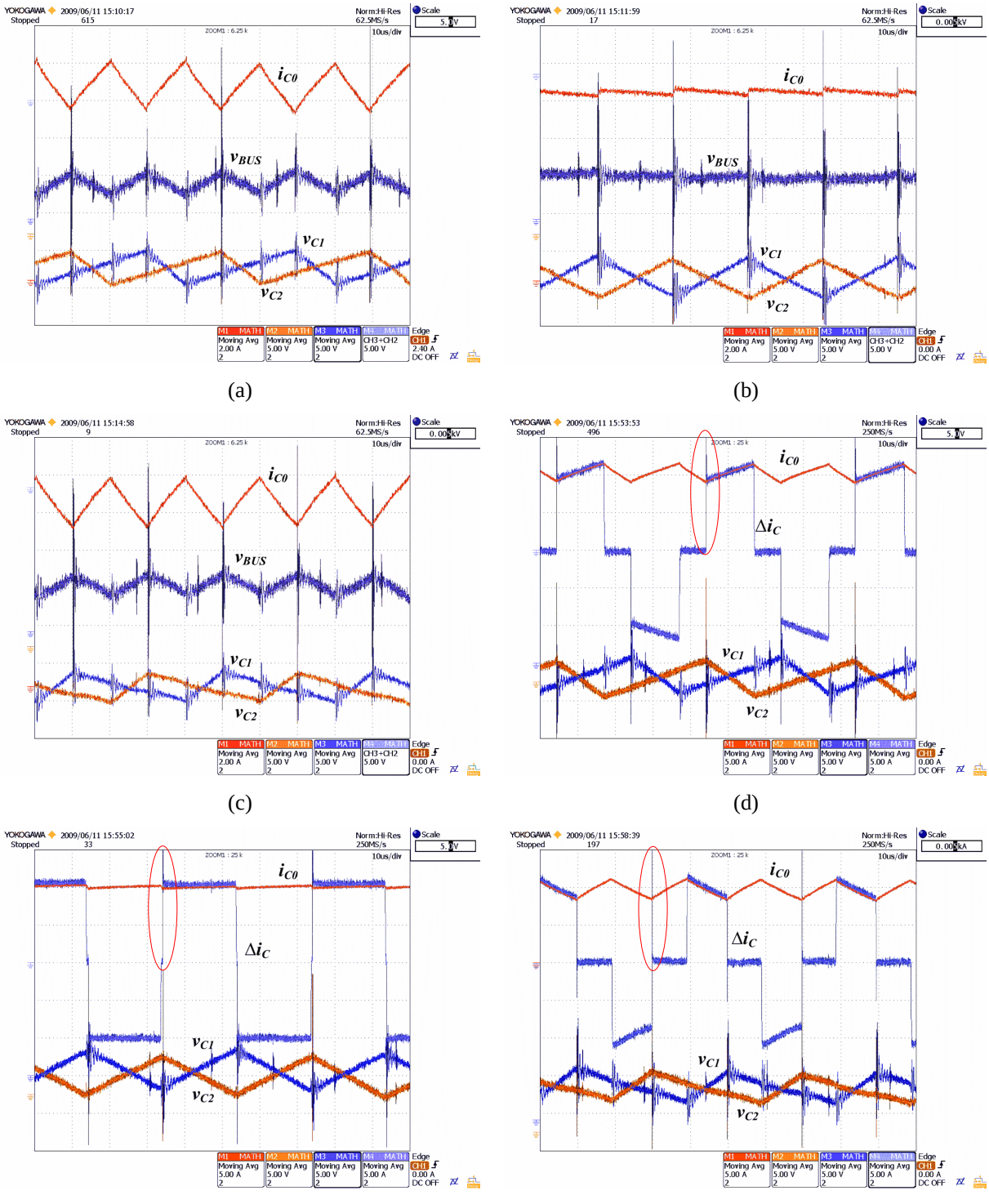
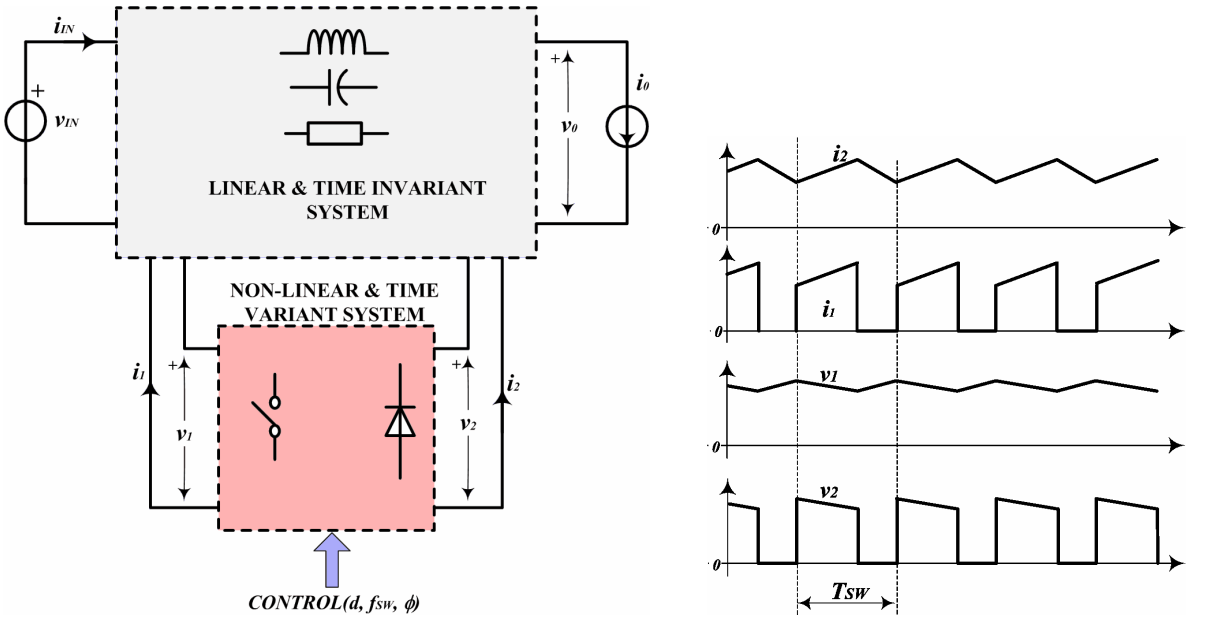


Fig. 4.16 Experimental waveforms of the capacitor voltages v_{C1}, v_{C2}, [5V/div], the dc bus voltage v_{BUS} [5V/div] and the ultra-capacitor current i_{C0} [5A/div] at different the duty cycle. a) $d \cong 0.25$, b) $d \cong 0.5$ and c) $d \cong 0.75$.The waveforms of the capacitor voltages v_{C1}, v_{C2}, the mid point capacitor current Δi_C and the ultra-capacitor current i_{C0} at different duty cycle. d) $d \cong 0.25$, e) $d \cong 0.5$ and f) $d \cong 0.75$. v_{BUS}=500V, $i_{C0(AV)}$=10A, L_{C0}=600µH, f_{SW}=25kHz.

5. MODELING ASPECTS AND CONTROL SCHEME

5.1. Modelling Techniques

In last two decades we have seen much research activities in field of modeling of switching mode power converters [106]-[107]. To give background of these modeling techniques, let us consider a power converter whose circuit diagram is depicted in Fig. 5.1. The converter consists of an input voltage source v_{IN}, a linear and time invariant passive network, a switching network, a vector of control variables and an output load given as constant current i_0. The switching network terminal variables are v_1, v_2, i_1 and i_2 .The input variables are v_{IN} and i_0, and output variables are v_0 and i_{IN}. The control variables can be duty cycle as wewll as switching frequency. In case of more complex converters, such as full-bridge phase shifted converters, the control variable can be phase shift of the bridge driving signals.



(a) (b)

Fig. 5.1 An example of switching mode power converter that consists of a linear passive network and a non-linear switching network. a) Circuit diagram and b) waveforms of the switching cell voltages and currents.

The terminal variables (v_1, v_2, i_1 and i_2) are periodic signals with the period equal to the control signal period (as given in Fig. 5.1 (b)). Therefore, the terminal variables can be expanded in Fourier series.

$$v_1(t) = \sum_{k=0}^{+\infty} V_1(k)\sin\left(k2\pi f_{sw} + \varphi_1(k)\right)$$
$$v_2(t) = \sum_{k=0}^{+\infty} V_2(k)\sin\left(k2\pi f_{sw} + \varphi_2(k)\right) \quad (5.1)$$

$$i_1(t) = \sum_{k=0}^{+\infty} I_1(k)\sin\left(k2\pi f_{sw} + \psi_1(k)\right)$$
$$i_2(t) = \sum_{k=0}^{+\infty} I_2(k)\sin\left(k2\pi f_{sw} + \psi_2(k)\right) \quad (5.2)$$

The analysis could be simplified if the following assumptions are made:

- The linear & time invariant passive network is essentially a low pass filter, and
- Dominant time constant of the linear passive network is much greater than the switching period, $T_{SW} << T_0$.

The terminal variables now can be approximated by first element of the Fourier series. The first elements of the Fourier series are average value computed over a switching period, so-called local or moving average variables [108].

$$\langle v_1 \rangle(t) = \frac{1}{T_{SW}} \int_t^{t+T_{SW}} v_1(\tau) d\tau$$
$$\langle v_2 \rangle(t) = \frac{1}{T_{SW}} \int_t^{t+T_{SW}} v_2(\tau) d\tau \quad (5.3)$$

$$\langle i_1 \rangle(t) = \frac{1}{T_{SW}} \int_t^{t+T_{SW}} i_1(t)(\tau) d\tau$$
$$\langle i_2 \rangle(t) = \frac{1}{T_{SW}} \int_t^{t+T_{SW}} i_2(\tau) d\tau \quad (5.4)$$

Note: The switching period T_{SW} is not necessarily constant.

The switching network variables are generally multi-frequency variables. In such a case, multi-dimensional Fourier series can be applied to obtain multi-frequency moving average value [109]. Typical power converters that show such behavior are power factor correctors.

The voltage $\langle v_1 \rangle$ and current $\langle i_2 \rangle$ are commonly treated as dependent variables, which are nonlinear functions of voltages $\langle v_2 \rangle$, $\langle v_{IN} \rangle$, $\langle v_0 \rangle$, the currents $\langle i_1 \rangle$, $\langle i_{IN} \rangle$, $\langle i_0 \rangle$ and the control variables $d(t)$ and $f_{SW}(t)$.

$$\begin{aligned}\langle v_1\rangle(t) &= F_1\big(\langle v_2\rangle,\langle v_{IN}\rangle,\langle v_0\rangle,\langle i_1\rangle,\langle i_{IN}\rangle,\langle i_0\rangle,\, d(t),\, f_{SW}(t),t\big),\\ \langle i_2\rangle(t) &= F_2\big(\langle v_2\rangle,\langle v_{IN}\rangle,\langle v_0\rangle,\langle i_1\rangle,\langle i_{IN}\rangle,\langle i_0\rangle,\, d(t),\, f_{SW}(t),t\big),\end{aligned} \tag{5.5}$$

where nonlinear function F_1 and F_2 (5.5) depends strongly on the converter topology and operation mode, continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

To perform transient analysis, nonlinear equations (5.5) are linearized around the steady state. The nonlinear equations (5.5) can be expanded in multidimensional Taylor series. Neglecting higher order elements yields a linarized equation that describes the switching network.

$$\begin{aligned}\hat{v}_1(t) \cong{}& \frac{\partial F_1}{\partial\langle v_2\rangle}\hat{v}_2(t)+\frac{\partial F_1}{\partial\langle v_{IN}\rangle}\hat{v}_{IN}(t)+\frac{\partial F_1}{\partial\langle v_0\rangle}\hat{v}_0(t)+\frac{\partial F_1}{\partial\langle i_1\rangle}\hat{i}_1(t)\\ &+\frac{\partial F_1}{\partial\langle i_{IN}\rangle}\hat{i}_{IN}(t)+\frac{\partial F_1}{\partial\langle i_0\rangle}\hat{i}_0(t)+\frac{\partial F_1}{\partial d(t)}\hat{d}(t)+\frac{\partial F_1}{\partial f_{SW}(t)}\hat{f}_{SW}(t)\\ \hat{i}_2(t) \cong{}& \frac{\partial F_2}{\partial\langle v_2\rangle}\hat{v}_2(t)+\frac{\partial F_2}{\partial\langle v_{IN}\rangle}\hat{v}_{IN}(t)+\frac{\partial F_2}{\partial\langle v_0\rangle}\hat{v}_0(t)+\frac{\partial F_2}{\partial\langle i_1\rangle}\hat{i}_1(t)\\ &+\frac{\partial F_2}{\partial\langle i_{IN}\rangle}\hat{i}_{IN}(t)+\frac{\partial F_2}{\partial\langle i_0\rangle}\hat{i}_0(t)+\frac{\partial F_2}{\partial d(t)}\hat{d}(t)+\frac{\partial F_2}{\partial f_{SW}(t)}\hat{f}_{SW}(t)\end{aligned} \tag{5.6}$$

The circuit given in Fig. 5.1 can be now analyzed as a standard linear circuit. Linear differential equations in time domain or unilateral Laplace transformation in complex domain are used. The output variables, in this case ac components of the output voltage v_0 and the input current i_{IN} are determined as a function of ac components of the input voltage, output current, duty cycle and switching frequency, as expressed in matrix form

$$\begin{bmatrix} v_0(s)\\ i_{in}(s)\end{bmatrix} = \underbrace{\begin{bmatrix} G_{d0}(s) & G_{f0}(s)\\ G_{din}(s) & G_{fin}(s)\end{bmatrix}\begin{bmatrix} d(s)\\ f_{SW}(s)\end{bmatrix}}_{CONTROL} + \underbrace{\begin{bmatrix} G_{in0}(s) & G_{00}(s)\\ G_{in}(s) & G_{0in}(s)\end{bmatrix}\begin{bmatrix} v_{in}(s)\\ i_0(s)\end{bmatrix}}_{DISTURBANCE}, \tag{5.7}$$

where a transfer function $G_{xy}(s)$ is defined by the definition as

$$G_{xy}(s) = \left.\frac{x(s)}{y(s)}\right|_{\substack{OTHER\ CONTROL\\ AND\ DISTURBANCE\\ VARIABLES=0}}. \tag{5.8}$$

Remark: This approach is not completely correct. The small signal model is developed assuming that an instantaneous variable could be de-composed in one variable that is constant over time (steady state or equilibrium point) and one superimposed ac variable. Frequency of that ac variable must be lower than the Nyquist frequency, in this case half of the switching frequency. Applying the Laplace transformation, however, does not give any limitation of the signal spectra. It means that the signal could be any regular signal having the Laplace transformation, including the step function and even the Dirac function. This is in contradiction with the first assumption of using small signal model; limited spectra of the superimposed small signal.

5.2. The DC-DC Converter Model

Fig. 5.2 shows the converter equivalent circuit diagram. The input filter capacitors are modeled by ideal capacitors C_{B1}, C_{B2}. The capacitors leakage current is modeled by the current sources i_{B1} and i_{B2}. Resistance R_{LC0} is the inductor resistance that is a constant (frequency independent) resistance.

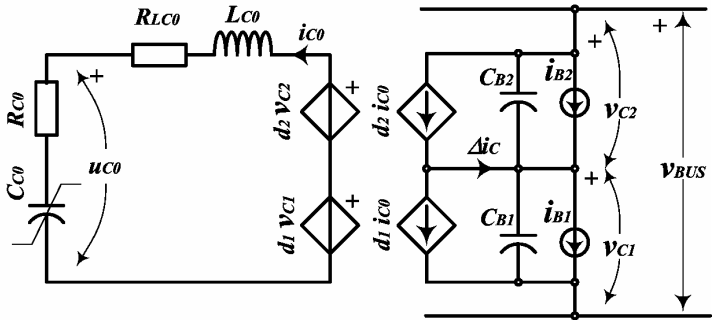


Fig. 5.2 The dc-dc converter large signal (average) model.

5.2.1. Large Signal Model

Assuming that v_{BUS}=*const*, the circuit in Fig. 5.2 can be described by the following set of equations,

$$\begin{aligned}
L_{C0}\frac{d\langle i_{C0}\rangle}{dt} &= \langle v_{C1}\rangle d_1 + \langle v_{C2}\rangle d_2 - u_{C0} - R_{LC0}\langle i_{C0}\rangle \\
\frac{d\Delta\langle v_C\rangle}{dt} &= \frac{2}{C_{B1}+C_{B2}}\left(\langle i_{C0}\rangle(d_2-d_1)+(i_{B2}-i_{B1})\right) \\
&= \frac{1}{C}\left(\langle i_{C0}\rangle(d_2-d_1)+(i_{B2}-i_{B1})\right)\Big|_{C_{B1}=C_{B2}=C} \\
\langle v_{C1}\rangle &= \frac{1}{2}\left(\langle \Delta v_C\rangle + \langle v_{BUS}\rangle\right)
\end{aligned}, \tag{5.9}$$

where $\Delta\langle v_C\rangle = \langle v_{C1}\rangle - \langle v_{C2}\rangle$, and i_{B1} and i_{B2} are the filter capacitors leakage current.

Duty cycles d_1 and d_2 are modulation signals (PWM_1 and PWM_2), which are generated by a non-linear controller, where the control law is

$$\begin{aligned}
d_1 &= \frac{u_0 + u_{C0}}{v_{BUS}} + \Delta d \\
d_2 &= \frac{u_0 + u_{C0}}{v_{BUS}} - \Delta d
\end{aligned}. \tag{5.10}$$

u_0 is the main control variable, while Δd is the balancing duty cycle as an auxiliary control variable. u_{C0} is the ultra-capacitor voltage and v_{BUS} is the dc bus voltage. The control

variable u_0 is generated by the current controller, while Δd is generated by the voltage error controller (Δv_C). This is discussed shortly after in section 5.5.2.

Substituting (5.10) into (5.9) yields

$$\begin{aligned} L_{C0}\frac{d\langle i_{C0}\rangle}{dt} &= u_0 + \Delta\langle v_C\rangle\Delta d - R_{LC0}\langle i_{C0}\rangle \\ \frac{d\langle \Delta v_C\rangle}{dt} &= -\frac{2}{C}\langle i_{C0}\rangle\Delta d - \frac{1}{C}\Delta i_B \end{aligned} \quad . \tag{5.11}$$

where $\Delta i_B = i_{B1} - i_{B2}$.

5.2.2. Linearization and Small Signal Model

The state and control variables of the system (5.11) are approximated by the first order perturbation model

$$\begin{aligned} &\langle i_{C0}\rangle = I_{C0} + \hat{i}_{C0} \quad \langle \Delta v_C\rangle = \Delta V_C + \Delta\hat{v}_C \\ &\Delta d = \Delta D + \Delta\hat{d} \quad \Delta i_B = \Delta I_B + \underbrace{\Delta\hat{i}_B}_{\cong 0} \qquad u_0 = U_0 + \hat{u}_0 \end{aligned} \quad . \tag{5.12}$$

Substituting (5.12) into (5.11) yields small signal model

$$\begin{aligned} L_{C0}\frac{d\hat{i}_{C0}}{dt} &= \hat{u}_0 + \Delta V_C\Delta\hat{d} + \Delta D\Delta\hat{v}_C - R_{LC0}\hat{i}_{C0} \\ \frac{d\Delta\hat{v}_C}{dt} &= -\frac{2}{C}I_{C0}\Delta\hat{d} - \frac{2}{C}\Delta D\hat{i}_{C0} - \frac{1}{C}\underbrace{\Delta\hat{i}_B}_{\cong 0} \end{aligned} \quad . \tag{5.13}$$

Circuit diagram of the small signal model is depicted in Fig. 5.3.

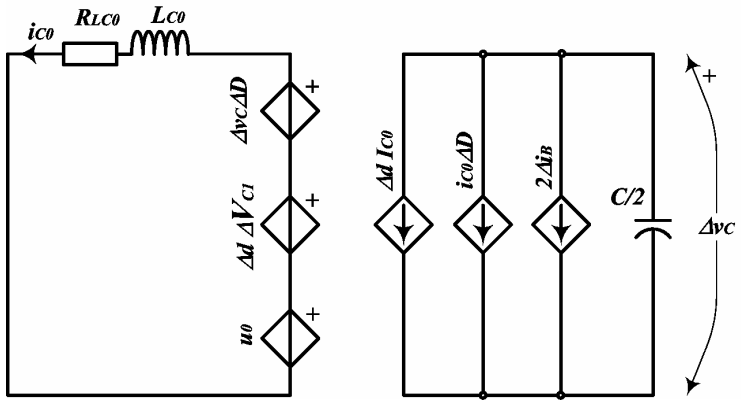


Fig. 5.3 The dc-dc converter small signal model.

Appling Laplace transformation on (5.13) yields the system transfer functions in a matrix form

$$\underbrace{\begin{bmatrix} i_{C0}(s) \\ \Delta v_C(s) \end{bmatrix}}_{OUT} = \begin{bmatrix} G_{iC0u0}(s) & G_{iC0\Delta d}(s) \\ G_{vCu0}(s) & G_{vC\Delta d}(s) \end{bmatrix} \underbrace{\begin{bmatrix} u_0(s) \\ \Delta d(s) \end{bmatrix}}_{CONTROL} + \begin{bmatrix} G_{iC0B} \\ G_{vCB} \end{bmatrix}\Delta i_B(s), \tag{5.14}$$

where the transfer functions are

$$\begin{aligned} G_{iC0u0} &= \left.\frac{i_{C0}(s)}{u_0(s)}\right|_{\Delta d(s)=0} = \frac{sC}{s^2 L_{C0}C + sCR_{LC0} + 2\Delta D^2} \\ G_{iC0\Delta d} &= \left.\frac{i_{C0}(s)}{\Delta d(s)}\right|_{u_0(s)=0} = \frac{sC\Delta V_C - 2\Delta D I_{C0}}{s^2 L_{C0}C + sCR_{LC0} + 2\Delta D^2} \\ G_{vCu0} &= \left.\frac{\Delta v_C(s)}{u_0(s)}\right|_{\Delta d(s)=0} - 2\frac{\Delta D}{s^2 L_{C0}C + sCR_{LC0} + 2\Delta D^2} \\ G_{vC\Delta d} &= \left.\frac{\Delta v_C(s)}{\Delta d(s)}\right|_{u_0(s)=0} = -2\frac{sL_{C0}I_{C0} + (R_{LC0}I_{C0} + \Delta D\Delta V_C)}{s^2 L_{C0}C + sCR_{LC0} + 2\Delta D^2} \end{aligned} \quad . \tag{5.15}$$

The capacitors leakage current Δi_B is not included in transfer function (5.15) because this current is not dynamic variable (the capacitors leakage current is constant $\Delta\hat{i}_B \cong 0$). However, the leakage current has to be taken into account when computing steady state balancing duty cycle *ΔD*.

$$\Delta D = -\frac{\Delta I_B}{2I_{C0}} = \frac{I_{B2} - I_{B1}}{2I_{C0}} \tag{5.16}$$

Fig. 5.4 (a) illustrates a block diagram of the small signal model (5.15). This model will be further used for synthesis of the current controller (i_{C0}) and the input voltage error controller (Δv_C). The transfer functions (5.15) are second order functions, wherein the nominators and denominator coefficients depend on the steady state variables: ΔV_C, ΔD, U_0 and I_{C0}. If the system is well designed and controlled, the steady state voltage balancing error is $\Delta V_C = 0$. Furthermore, from (5.11) follows that the duty cycles d_1 and d_2 in steady state must be equal, and therefore $\Delta D = 0$. This is a case only if the filter capacitors leakage current can be neglected ($\Delta i_B = i_{B1} - i_{B2} = 0$), for example when high quality film capacitors are used. If electrolytic capacitors are used, leakage current has to be taken into account. In that case, steady state balancing duty cycle is given by (5.16).

Substituting conditions $\Delta V_C = 0$ and $\Delta D = 0$ into (5.15) yields simplified transfer functions,

$$\begin{aligned} G_{iC0u0} &= \frac{1}{sL_{C0} + R_{LC0}}, \\ G_{iC0\Delta d} &= 0 \\ G_{vCu0} &= 0 \\ G_{vC\Delta d} &= -2\frac{I_{C0}}{sC}. \end{aligned} \tag{5.17}$$

The transfer functions G_{iCu0} and $G_{vC\Delta d}$ have become first order functions. The cross-coupling terms $G_{iC\Delta d}$ and $G_{iC0\Delta d}$ are zero; u_0 has no influence on the voltage balancing error Δv_C and Δd has no influence on the output current i_{C0}. Bode diagrams of the transfer functions (5.15) have been computed for different conditions and depicted in Fig. 5.4 (b), (c) and (d). To prove small signal model (5.15), the dc-dc converter frequency response was simulated under different conditions. The results are included in the Bode diagram of Fig. 5.4 at different frequencies; 1Hz, 10Hz, 100Hz and 1kHz.

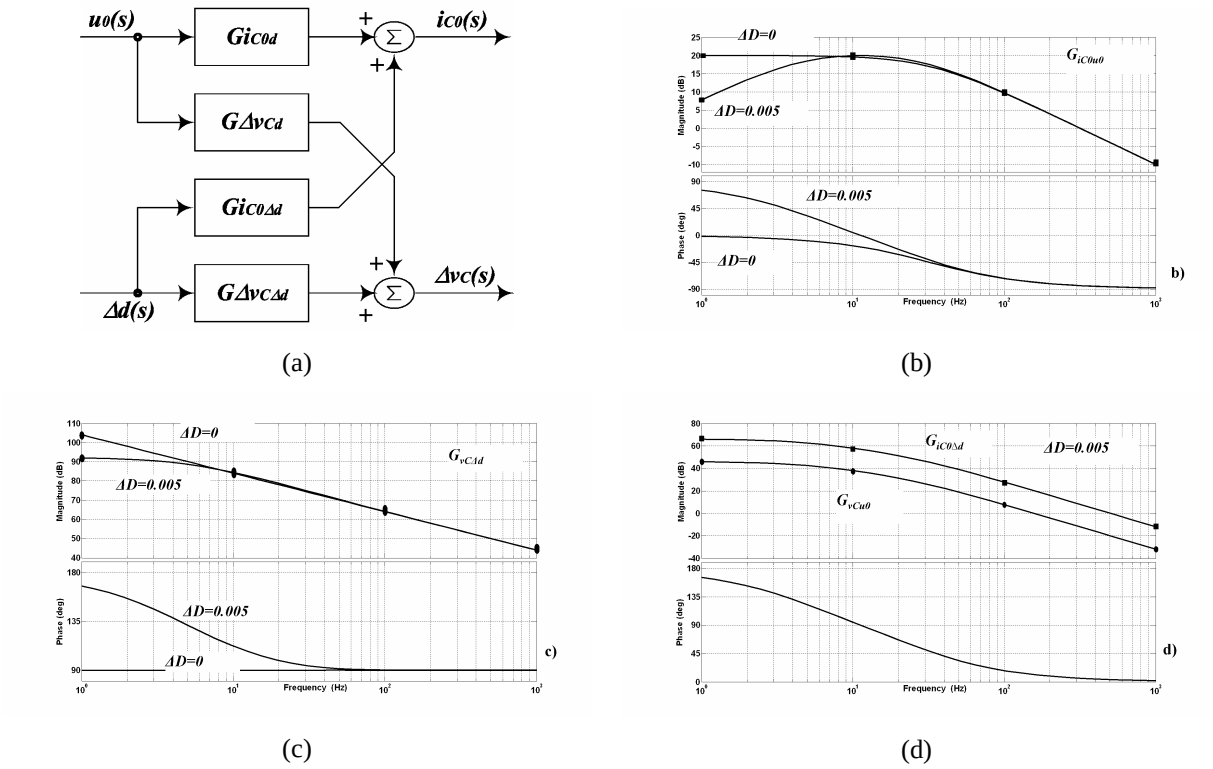


Fig. 5.4 a) The dc-dc converter small signal model. Bode diagram of the system transfer functions: b) the control to the ultra-capacitor current system transfer function $G_{iC0u0}=\dfrac{i_{C0}(s)}{u_0(s)}$, c) $G_{vC\Delta d}=\dfrac{\Delta v_C(s)}{\Delta d(s)}$, and d) $G_{iC0\Delta d}=\dfrac{i_{C0}(s)}{\Delta d(s)}$, $G_{vCu0}=\dfrac{\Delta v_C(s)}{u_0(s)}$.

5.3. The DC Bus Circuit Model

In this section, general case of the dc bus load model is discussed. Then, PWM fed variable speed drive is analysed as an application example.

5.3.1. A General Case

In real applications, such as lose-less power conversion, the dc bus load is more complex than a simple current source. It could be also constant resistance and constant power as well as a combination of all the three loads. This could be an essential issue for the system control, particularly the dc bus voltage and overall system stability. To cover all these cases, we shall consider a generic load composed of constant power P_{LOAD}, constant current I_{LOAD} and a passive resistive load R_{LOAD}, as given in Fig. 5.5, [110]-[111]. The dc bus filter is modelled by an ideal capacitor C_{BUS} and equivalent series resistance R_{ESR}. The dc bus supply is indicated by a current i_{BUS}.

From Fig. 5.5 we have the load equivalent current i_{L_E}

$$i_{L\_E}=i_{LOAD}+\frac{1}{R_{LOAD}}v_{BUS}+\frac{p_{LOAD}}{v_{BUS}}. \tag{5.18}$$

Linearization around an equilibrium point yields steady state (DC component) variables

$$I_{L\_E} = I_{LOAD} + \frac{V_{BUS}}{R_{LOAD}} + \frac{P_{LOAD}}{V_{BUS}}, \tag{5.19}$$

and small signal variation (ac component) around the steady state

$$\hat{i}_{L\_E} = \hat{i}_{LOAD} + \left(\frac{1}{R_{LOAD}} - \frac{P_{LOAD}}{V_{BUS}^2} \right) \hat{v}_{BUS} + \frac{1}{V_{BUS}} \hat{p}_{LOAD}. \tag{5.20}$$

P_{LOAD}-R_{L_E} graph for different type of load, active constant power load and passive resistive load is given in Fig. 5.6. As seen from Fig. 5.6, the load incremental resistance (small signal resistance) is negative if the load is positive constant power, while the resistance is positive when the load is either passive resistive load or negative constant power load.

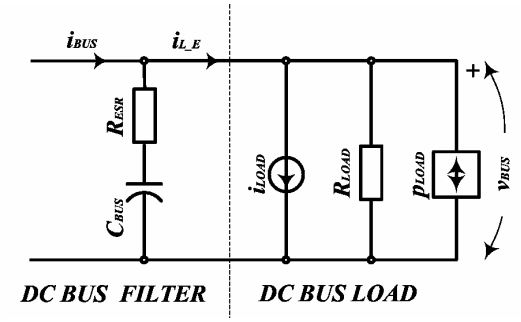


Fig. 5.5 Model of the dc bus filter and load.

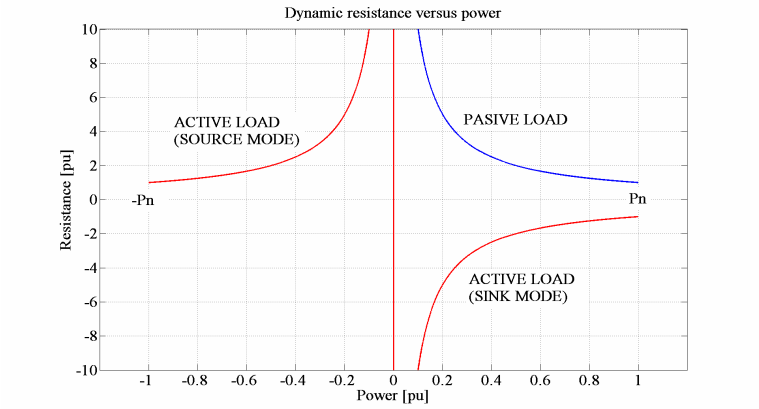


Fig. 5.6 Incremental (small signal) resistance versus the dc bus load.

5.3.2. PWM Inverter fed Variable Speed Drives as DC bus load

Basically, two different operational modes of a variable speed drive can be distinguished, namely constant power and constant torque mode. Most of today's drives work in constant power mode thanks to accurate control of the speed. Typical examples are lifts in constant speed mode, conveyers, pumps fans, and so on. There are, however, some applications with constant torque control. Typical examples are high performance servo

positioning drives, such as robot applications, tooling machines and so on. In such applications the shaft speed is varying while to torque is controlled by an inner control loop. However, even in this case, the inverter behaves as a constant power load. The inverter output voltage is controlled to be constant, controlling the inverter duty cycle. Therefore, on short term scale in order of several 100ms, the inverter output power is constant too. If the inverter losses can be neglected, as it is case when the inverter is well designed, the inverter input power (dc bus power) is constant too, regardless on the input voltage (dc bus voltage) variation.

5.4. The Entire Conversion System Model

5.4.1. Large Signal Model

The large signal (nonlinear) model of the entire power conversion system is depicted in Fig. 5.7. The input rectifier is modeled by a voltage source v_{REC}, diode D_R and filter inductor L_{BUS}. Here, we consider that the drive operates in braking or motoring mode from the ultra-capacitor. In that case the dc bus voltage is boosted, being greater that the input voltage, and therefore the input rectifier diodes are blocked. Thus, the input voltage v_{REC}, diode D_R and inductor L_{BUS} can be dropped from the model. This is indicated by the dashed lines in Fig. 5.7 (a). The dc bus capacitor is modeled by an ideal capacitor C_{BUS} and its equivalent series resistance R_{ESR}. The dc bus load, in this case a controlled electric drive, is modeled by a constant power load p_{LOAD}.

The bi-directional dc-dc converter is modeled by a loss-free power converter with an input (v_{BUS}) and an output (u_{C0}). The input is modeled by a power source p_{C0} that is connected on the dc bus side. The output is modeled by a current source i_{C0} that is connected on the ultra-capacitor side. Details are shown in Fig. 5.7 (a). Block diagram of the converter model is depicted in Fig. 5.7 (b).

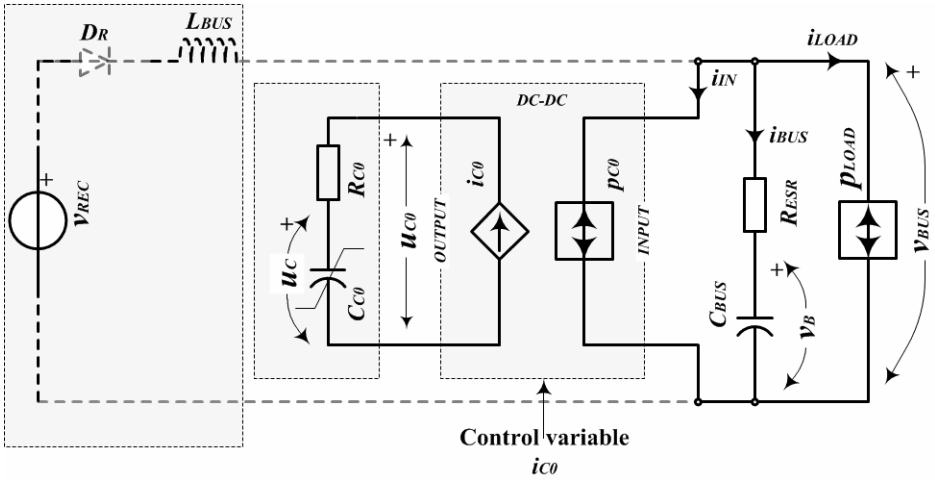
The dc-dc converter contains an inductor L_{C0} that is carrying the current i_{C0}. The input to output instantaneous power balance is

$$p_{C0} = u_{C0} i_{C0} + i_{C0} L_{C0} \frac{di_{C0}}{dt}. \tag{5.21}$$

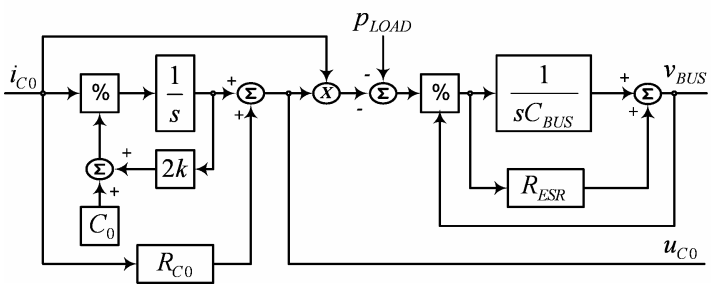
However, if the dc-dc converter is designed in such a way to have switching frequency quite greater than bandwidth of the dc bus voltage control loop, the effect of the inductance L_{C0} can be neglected, and therefore it can be assumed that $\left(L_{C0} \frac{di_{C0}}{dt} \right) \to 0$ .Thus, the input instantaneous power is equal to the output instantaneous power,

$$p_{C0} = u_{C0} i_{C0}. \tag{5.22}$$

Without losing generality of the analysis, one may consider that the current i_{C0} is well controlled by an inner current controller and as that the current i_{C0} will be taken as the system control variable.



(a)



(b)

Fig. 5.7 Model of entire power conversion system. a) Circuit diagram and b) bloc diagram.

The system of Fig. 5.7 can be described by following set of nonlinear equations

$$(C_0 + 2k_C u_C)\frac{du_C}{dt} = i_{C0}, \tag{5.23}$$

$$C_{BUS}\frac{dv_B}{dt} = -\frac{p_{C0}}{v_{BUS}} - \frac{p_{LOAD}}{v_{BUS}}, \tag{5.24}$$

$$\begin{aligned} u_{C0} &= u_C + R_{C0} i_{C0}, \\ v_{BUS} &= v_B - R_{ESR}\left(\frac{p_{C0}}{v_{BUS}} + \frac{p_{LOAD}}{v_{BUS}}\right). \end{aligned} \tag{5.25}$$

5.4.2. Linearization and Small Signal Model

Applying Taylor series expansion (5.6) or the first order perturbation model (5.12) on (5.23), (5.24) and (5.25) yields a linear model,

$$\frac{d\hat{u}_C}{dt} = \frac{1}{(C_0 + 2k_C U_C)}\hat{i}_{C0} - \frac{2k_C I_{C0}}{(C_0 + 2k_C U_C)^2}\hat{u}_C, \tag{5.26}$$

$$C_{BUS}\frac{d\hat{v}_B}{dt} = -\frac{I_{C0}}{V_{BUS}}\hat{u}_{C0} - \frac{U_{C0}}{V_{BUS}}\hat{i}_{C0} + \frac{U_{C0}I_{C0} + P_{LOAD}}{V_{BUS}^2}\hat{v}_{BUS} - \frac{1}{V_{BUS}}\hat{p}, \tag{5.27}$$

$$\hat{u}_{C0} = \hat{u}_C + R_{C0}\hat{i}_{C0},$$
$$\hat{v}_{BUS} = \hat{v}_B - R_{ESR}\left(\frac{I_{C0}}{V_{BUS}}\hat{u}_{C0} + \frac{U_{C0}}{V_{BUS}}\hat{i}_{C0} - \frac{U_{C0}I_{C0} + P_{LOAD}}{V_{BUS}^2}\hat{v}_{BUS} + \frac{1}{V_{BUS}}\hat{p}\right). \tag{5.28}$$

where a variable $x = X_0 + \hat{x}$ is represented by the steady state X_0 and a small variation $\hat{x}$ around the steady state.

Applying Laplace transformation on (5.26)-(5.28) yields the transfer functions in a matrix form,

$$\begin{bmatrix} u_{C0}(s) \\ v_{BUS}(s) \end{bmatrix} = \underbrace{\begin{bmatrix} G_{C0}(s) \\ G_{BUS}(s) \end{bmatrix} i_{C0}(s)}_{CONTROL} + \underbrace{\begin{bmatrix} 0 \\ G_P(s) \end{bmatrix} p_{LOAD}(s)}_{DISTURBANCE}. \tag{5.29}$$

Block diagram of the small signal model (5.29) is depicted in Fig. 5.8.

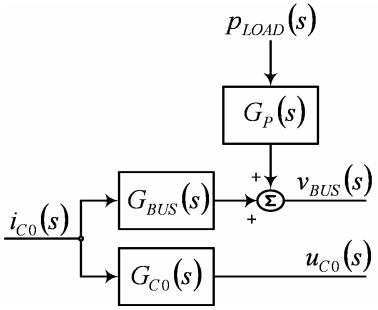


Fig. 5.8 Block diagram of small signal model of the conversion system of Fig. 5.7.

The ultra-capacitor current to voltage transfer functions is

$$G_{C0}(s) = R_{C0}\frac{s + \dfrac{C_0 - 2kI_{C0}R_{C0} + 2k(U_{C0} + I_{C0}R_{C0})}{R_{C0}(C_0 + 2k(U_{C0} - I_{C0}R_{C0}))^2}}{s + \dfrac{2kI_{C0}}{(C_0 + 2k(U_{C0} - I_{C0}R_{C0}))^2}} = R_{C0}\frac{s + \omega_Z}{s + \omega_P}, \tag{5.30}$$

where ω_Z and ω_P are a zero and pole that depend on steady state variables U_{C0}, I_{C0} and the ultra-capacitor parameters.

The control and disturbance to the dc bus voltage transfer functions are

$$G_{BUS}(s) = \frac{-(I_{C0}G_{C0}(s) + U_{C0})(1 + sC_{BUS}R_{ESR})V_{BUS}}{sC_{BUS}(V_{BUS}^2 - R_{ESR}(U_{C0}I_{C0} + P_{LOAD})) - (U_{C0}I_{C0} + P_{LOAD})},$$
$$G_P(s) = \frac{-V_{BUS}(1 + sC_{BUS}R_{ESR})}{sC_{BUS}(V_{BUS}^2 - R_{ESR}(U_{C0}I_{C0} + P_{LOAD})) - (U_{C0}I_{C0} + P_{LOAD})}, \tag{5.31}$$

where V_{BUS} and P_{LOAD} are the dc bus voltage and load power in steady state and G_{C0} is the ultra-capacitor voltage transfer function (5.30). When the electric drive operates in steady state, being supplied from the ultra-capacitor, the ultra-capacitor power and load are balanced, $U_{C0}I_{C0} + P_{LOAD} = 0$. Substituting this condition into (5.31) yields

$$G_{BUS}(s) = -\frac{(I_{C0}G_{C0}(s)+U_{C0})(1+sC_{BUS}R_{ESR})}{sC_{BUS}V_{BUS}},$$
$$G_P(s) = -\frac{(1+sC_{BUS}R_{ESR})}{sC_{BUS}V_{BUS}}. \quad (5.32)$$

If the ultra-capacitor is large enough to be considered as an infinite capacitance compared to the dc bus capacitor C_{BUS}, as it is case in most of the applications, the transfer function G_{BUS} becomes

$$\lim_{C_{C0}\to\infty} G_{BUS} = -\frac{(1+sC_{BUS}R_{ESR})(U_{C0}+I_{C0}R_{C0})}{sC_{BUS}V_{BUS}}. \quad (5.33)$$

Transfer function could be further simplified. The ultra-capacitor voltage is high enough and therefore the voltage droop on the series resistance can be neglected, $U_{C0} >> I_{C0}R_{C0}$. The dc bus voltage transfer function is

$$G_{BUS} \cong -\frac{(1+sC_{BUS}R_{ESR})U_{C0}}{sC_{BUS}V_{BUS}}. \quad (5.34)$$

5.4.3. Discussion on the Model

As well known from the literature, a dc-dc converter may have right half plane zero (RHPZ) in the control to the dc bus voltage transfer function [106], [112]-[114]. The control variable can be either duty cycle d in voltage control mode or output current i_{C0} in the current control mode. Location of the zero depends on the output current i_{C0}. The positive current the negative zero and negative current the positive zero. This causes an issue when the dc bus voltage control loop has to be fast, in the same order as the output current control loop.

Please note from (5.34) that the zero of the transfer function is independent on the output current. In fact, when linear model of the conversion system has being developed, it has been assumed that the dc-dc converter is a device that satisfies the instantaneous power balance (5.22). That means the dc-dc converter does not content any energy storage element, neither an inductor nor a capacitor. This is just an approximation. If the dc-dc converter contents an inductor L_{C0} which cannot be neglected, the instantaneous power balance (5.21) has to be used. Substituting (5.21) into (5.24) and (5.25), yields a transfer function that has a zero, whose position in complex plane depends on the steady state current I_{C0}; the positive current the negative zero and the negative current the positive zero. If the dc-dc converter is designed in such a way to have switching frequency quite greater than bandwidth of the dc bus voltage control loop, the RHPZ can be neglected in the transfer function G_{BUS}. Also, in this case, the current controller response time can be neglected.

5.5. Control Scheme

5.5.1. The Control Objectives

The primary control objective is to control the ultra-capacitor current i_{C0} and the voltage balancing error Δv_C [92]. The secondary control objective is to asymptotically regulate the dc bus voltage v_{BUS} to desired reference, where the reference depends on the

system operation mode [114]. Last but not least control objective is to regulate the ultra-capacitor state of the charge, where the state of charge reference depends on the operating mode [114]. The system operating modes and corresponding references have been discussed in chapter 3, section 3.2.

5.5.2. Control of the Ultra-capacitor Current and Voltage Balancing Error

Fig. 5.9 illustrates small signal block diagram of the converter, including control scheme for the ultra-capacitor current and the voltage balancing error. The converter model and two controllers can be distinguished. The controller Gi_{C0} controls the ultra-capacitor current i_{C0}, while the controller $G\Delta v_C$ controls the voltage balancing error Δv_C. The current reference is i_{C0REF}, while the reference for the voltage balancing controller is zero.

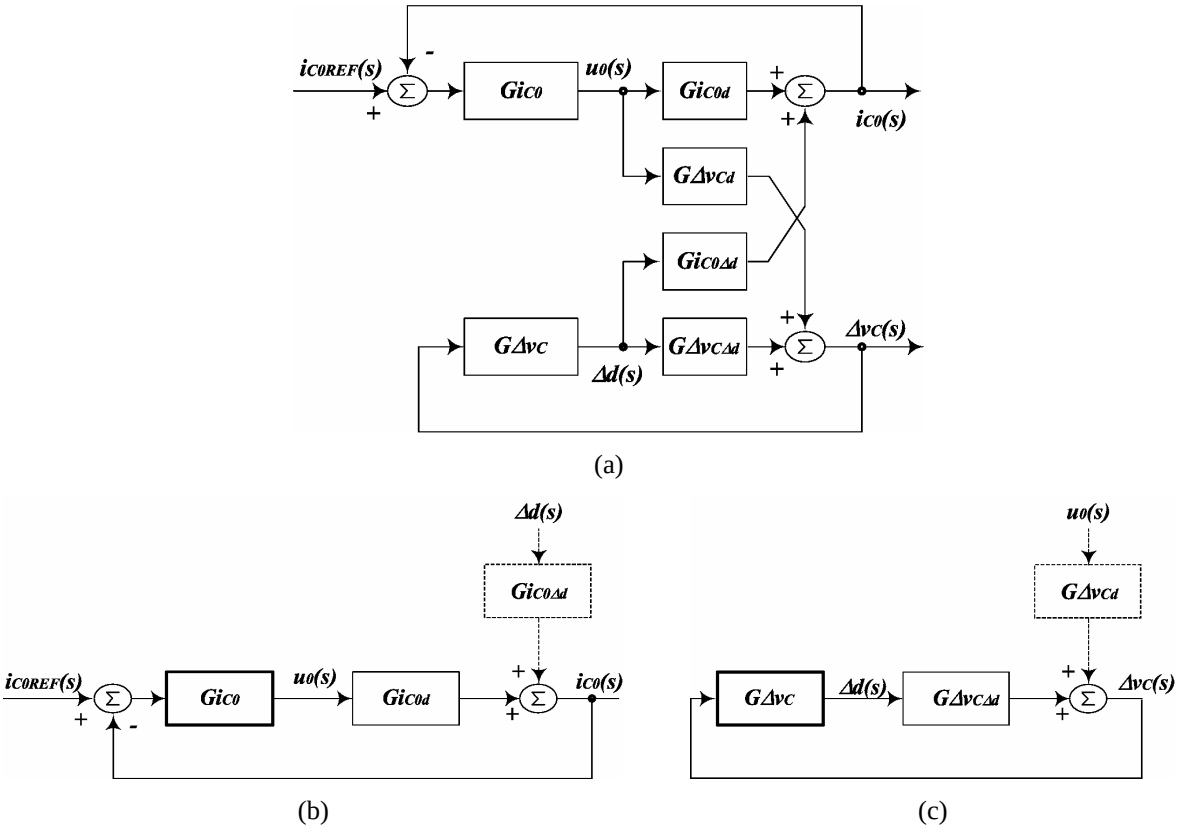


Fig. 5.9 Control algorithm for the ultra-capacitor current and the voltage balancing error. a) Small signal model, b) the ultra-capacitor current control loop, and c) the voltage balancing control loop.

5.5.2.1. The Control Scheme Realization

Design and realization of the current controller is state of the art, and therefore it is not discussed. The voltage balancing controller design and realization is discussed in some more detail. As seen from (5.17), gain of the transfer function $G_{vC\Delta d}$ depends on the output current; the positive current the negative gain and opposite; the controller parameters depend on the current i_{C0}. To avoid the use of complex adaptive controller, the controller $G_{vC\Delta d}$ can be designed considering positive output current. Then, the output of the controller is multiplied by function $sgn(i_{C0})$. Simple realization is illustrated in Fig. 5.10. If the current i_{C0} is positive,

the control signal Δd is the controller output signal. If the current i_{C0} is negative, the control signal Δd is switched to the inverted output signal of the controller $G\Delta v_C$.

Fig. 5.11 illustrates the functionality and performance of the ultra-capacitor current controller and the voltage balancing controller. The current i_{C0} is cycling between -9A and 10A, and the voltages v_{C1} and v_{C2} were recorded. Please note that the voltages v_{C1} and v_{C2} are quite well matched. When the load current is positive the voltages are decreasing and when the current is negative the voltages are increasing. This is caused by the power supply current limitation. Fig. 5.11 (b) shows details when the output current i_{C0} rises from -9A to 10A, while Fig. 5.11 (c) illustrates the details when the current falls from 10A to -9A. High frequency oscillations (when the current rises/falls) are caused by the input filter inductance (not included in the analysis and the circuit diagram).

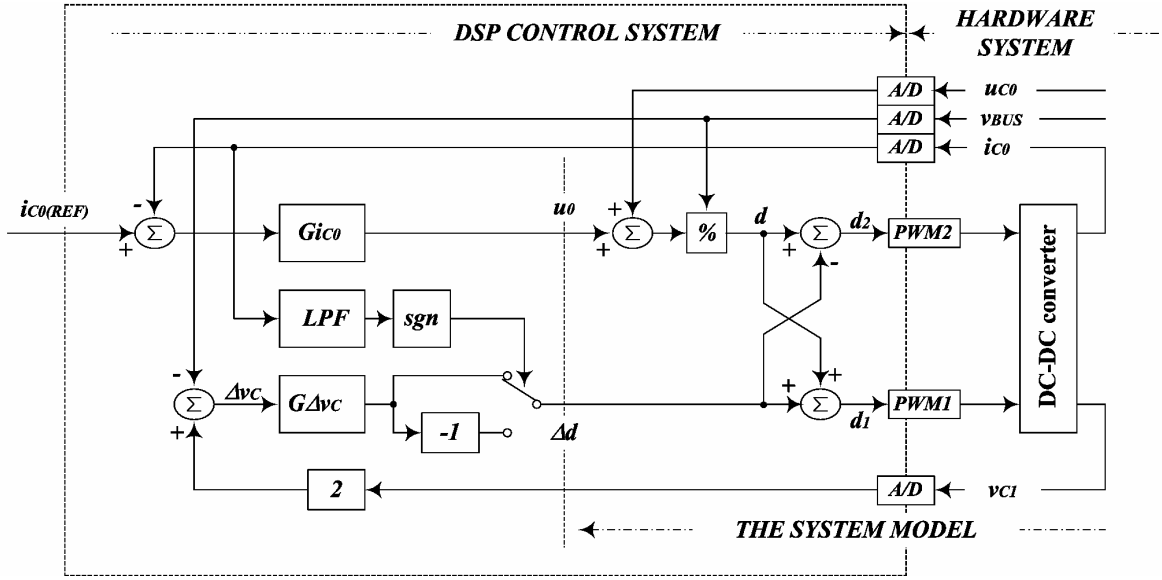


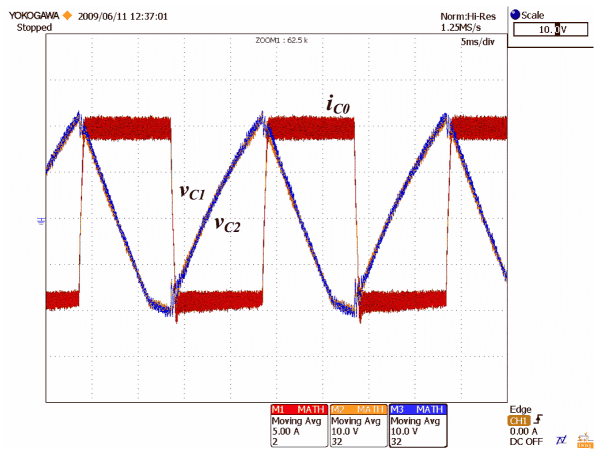
Fig. 5.10 Realization of the ultra-capacitor current and the voltage balancing error control.

5.5.3. The Ultra-capacitor and the DC Bus Voltage Control

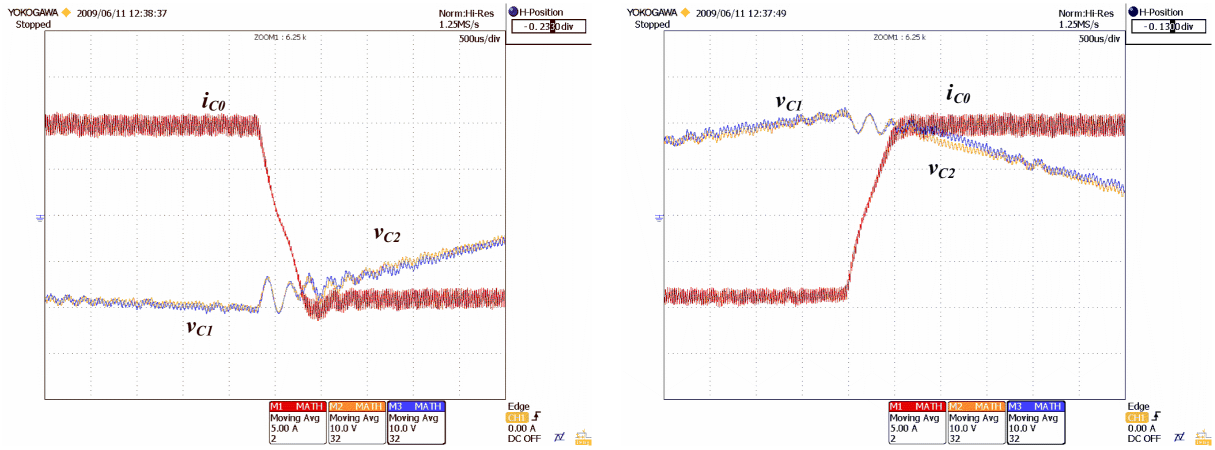
To describe the control scheme, three operational modes that are important from the control point of view are considered: 1) The mains motoring mode, 2) the braking and motoring from the ultra-capacitor, and 3) ride-through mode [114].

Fig. 5.12 illustrates the proposed control scheme. One can distinguish an inner current controller G_{iC0} and three outer controllers. The inner controller G_{iC0} regulates the ultra-capacitor current i_{C0}. This was discussed in the previous section. Here in this section, it will be assumed that the current i_{C0} is well controlled and it follows the reference without significant error.

The outer controller G_{uC0} regulates the ultra-capacitor voltage u_{C0}. This controller generates reference $i_{C0(REF)}$ for the ultra-capacitor current controller. The dc bus voltage v_{BUS} is controlled by two outer voltage controllers $G_{vBUSmax}$ and $G_{vBUSmin}$. The controller $G_{vBUSmax}$ regulates the dc bus voltage when the drive operates in braking and motoring mode from the ultra-capacitor (modes ***B*** and ***MC$_0$***, Fig. 3.4), while the controller $G_{vBUSmin}$ regulates the dc bus voltage when the system operates in the ride-through mode (mode ***RT***, Fig. 3.4). The ultra-capacitor voltage reference $u_{C0(REF)}$ is sum of the output signals of the dc bus voltage controllers $G_{vBUSmax}$ and $G_{vBUSmin}$.



(a)



(b) (c)

Fig. 5.11 Experimental waveforms of the capacitor voltages v_{C1}, v_{C2} [10V/div] and the ultra-capacitor current i_{C0} [5A/div]. The ultra-capacitor current commutes from -9A to +10A.

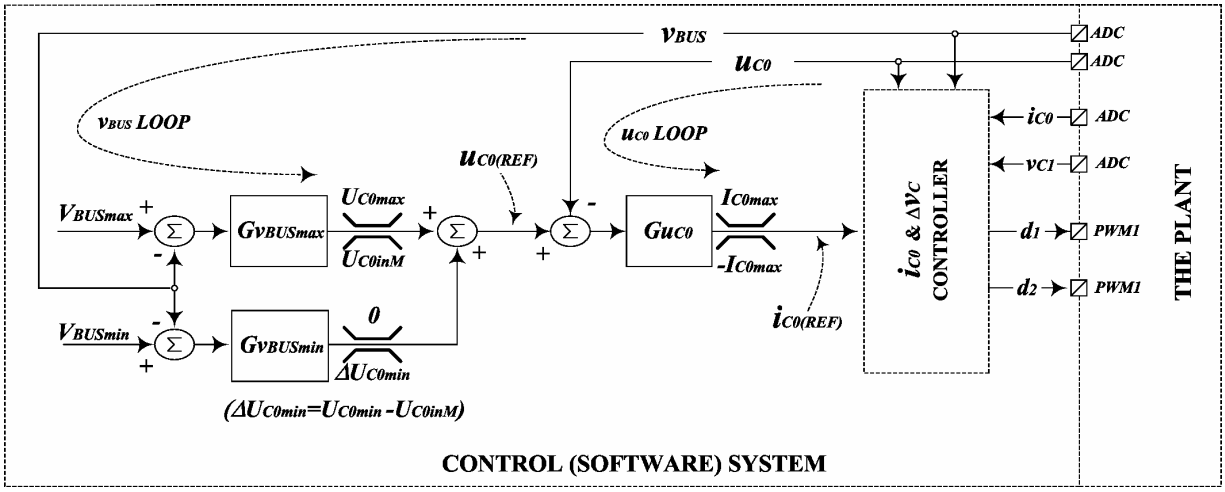


Fig. 5.12 Control block diagram of the converter, excluding control of the ultra-capacitor current and voltage balancing error.

5.5.3.1. The Mains Motoring Mode

The dc bus voltage is determined by the mains voltage, $v_{BUS} \cong 1.41 V_{MAINS}$, where V_{MAINS} is the mains phase-to-phase RMS voltage. As defined in Fig. 3.5 (a), the dc bus voltage is lower than the reference V_{BUSmax} and greater than the reference V_{BUSmin}. Hence, the dc bus voltage controller $G_{vBUSmax}$ is saturated to U_{C0inM}, while the controller $G_{vBUSmin}$ is saturated to zero. The ultra-capacitor voltage reference is therefore

$$u_{C0ref} = U_{C0inM} + 0 = U_{C0inM} \,. \tag{5.35}$$

The controller G_{uC0} maintains the ultra-capacitor voltage constant to the intermediate level U_{C0inM} in order to prevent energy flow between the ultra-capacitor and the drive.

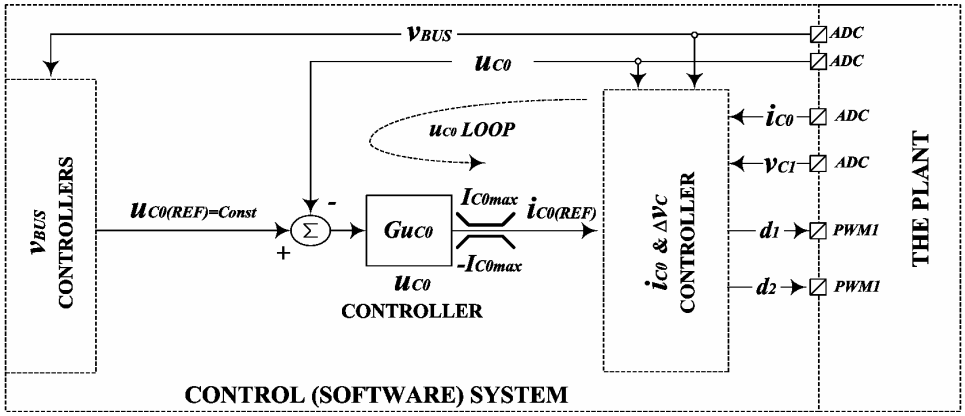


Fig. 5.13 The ultra-capacitor voltage closed loop.

5.5.3.2. The Drive Braking Mode and Motoring Mode from the Ultra-capacitor

The drive load is inverted (the motor operates as a generator) and therefore the dc bus capacitor C_{BUS} is charged. The dc bus voltage v_{BUS} increases until it reaches the reference V_{BUSmax}. The dc bus voltage controller $G_{vBUSmax}$ goes out of saturation while the controller $G_{vBUSmin}$ stays saturated to zero. The ultra-capacitor reference voltage starts to increase from U_{C0inM} towards U_{C0max} and therefore the ultra-capacitor current increases. The magnitude of the current is adjusted by the cascaded controllers $G_{vBUSmax}$ and G_{uC0} to such level to maintain the dc bus voltage constant. If the braking energy is greater than the ultra-capacitor capability the voltage u_{C0} will reach the maximum U_{C0max}. Then the dc bus voltage controller $G_{vBUSmax}$ will be saturated at U_{C0max}. The ultra-capacitor voltage is regulated to U_{C0max} and the current i_{C0} falls to zero. Charging of the ultra-capacitor is stopped. The dc bus voltage starts to increase until activation of the braking resistor or the drive over-voltage (over-braking) protection.

When the drive operates in motoring mode, the ultra-capacitor has to be discharged to the intermediate value U_{C0inM} in order to be ready for the next braking phase. The dc bus voltage controller $G_{vBUSmax}$ maintains the dc bus voltage to V_{BUSmax}. The controller $G_{vBUSmax}$ output decreases, and therefore the ultra-capacitor voltage reference decreases towards U_{C0inM}.

$$U_{C0\max} \geq u_{C0ref} \downarrow \geq U_{C0inM} \,. \tag{5.36}$$

The ultra-capacitor is being discharged, supplying the drive. Once the ultra-capacitor voltage reaches the intermediate value U_{C0inM}, the dc bus voltage controller $G_{vBUSmax}$ will be saturated at the reference U_{C0inM}. The ultra-capacitor voltage is regulated to U_{C0inM}, and therefore the ultra-capacitor current falls to zero. Discharging of the ultra-capacitor is finished. The dc bus capacitor is being discharged, and therefore the dc bus voltage decreases until the drive input rectifier starts to conduct. The drive is being supplied again from the mains.

5.5.3.3. The Ride-Through Mode

When the mains is interrupted the dc bus voltage starts to decrease until it reaches the lower reference V_{BUSmin}. The controller $G_{vBUSmin}$ goes out of saturation and its output starts to decrease below zero towards $\Delta U_{C0min}=U_{C0min}-U_{C0inM}$. Since the controller $G_{vBUSmax}$ is saturated to U_{C0inM}, the ultra-capacitor reference voltage starts to decrease below U_{C0inM} towards U_{C0min}.

$$U_{C0inM} \geq u_{C0ref} \downarrow \geq \left(U_{C0inM} + U_{C0\min} - U_{C0inM} = U_{C0\min}\right). \tag{5.37}$$

It allows deeper discharge of the ultra-capacitor, and regulation of the dc bus voltage to the minimum level V_{BUSmin}. If the power interruption is longer than specified, the ultra-capacitor will be discharged to the minimum level U_{C0min}. The ultra-capacitor current will fall to zero and then the dc bus voltage will start to decrease until it reaches the under-voltage supply fault (USF) level.

5.5.4. The Controller(s) Synthesis

5.5.4.1. The Ultra-capacitor Voltage Controller

Fig. 5.14 shows the ultra-capacitor voltage control loop, where G_{C0} is the ultra-capacitor current to voltage transfer function (5.30), G_{uC0} is the voltage controller and G_F is the feedback filter.

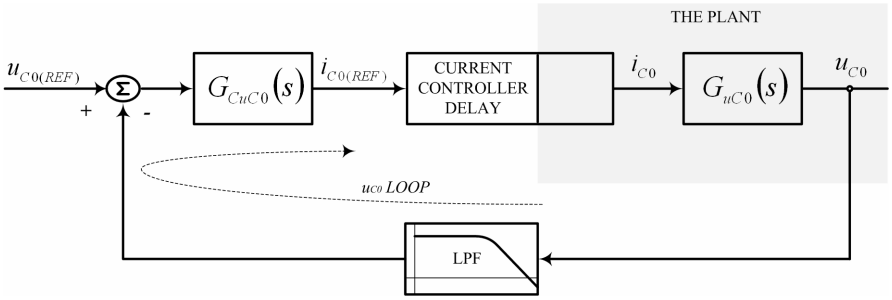


Fig. 5.14 The ultra-capacitor voltage closed loop.

The ultra-capacitor voltage closed loop transfer function is

$$\begin{aligned}\frac{u_{C0}(s)}{u_{C0}^{REF}(s)} &= \frac{G_{C0}(s)G_{uC0}(s)}{1+G_{C0}(s)G_{uC0}(s)G_F(s)} \\ &= \frac{R_{C0}k_{PC0}(s+\omega_Z)}{s^2T_F + s\left(1+T_F\omega_P + k_{PC0}R_{C0}\right)+\left(\omega_P + \omega_Z k_{PC0}R_{C0}\right)}\end{aligned}, \tag{5.38}$$

where ω_Z and ω_P are the zero and pole of the ultra-capacitor voltage transfer function (5.30). The ultra-capacitor voltage controller is a classical proportional (P) controller and the filter G_F is a low-pass filter

$$G_{uC0}(s) = k_{PC0}, \tag{5.39}$$

$$G_F(s) = \frac{1}{sT_F + 1}. \tag{5.40}$$

Characteristic equation of (5.38) is

$$\begin{aligned} D_{uC0}(s) &= s^2 + s\frac{(1 + T_F\omega_P + k_{PC0}R_{C0})}{T_F} + \frac{(\omega_P + \omega_Z k_{PC0}R_{C0})}{T_F} \\ &= s^2 + s2\zeta_{C0}\omega_{C0} + \omega_{C0}^2 \end{aligned}, \tag{5.41}$$

where ζ_{C0} is damping factor and ω_{C0} is the closed loop natural frequency. Proportional gain of the controller and time constant of the filter can be computed from (5.30) and (5.41) using the binomial criterion ($\zeta_{C0}=1$).

However, the question is how to define the natural frequency, or simply speaking how to define the close loop band-width? To answer on this question one has to keep in mind some system limitations. In fact, the controller bandwidth is determined by the ultra-capacitor voltage tracking error. In section IV it has been explained how the control system works when the ultra-capacitor is charged (the drive braking mode) and discharged (the drive motoring from the ultra-capacitor). In both modes, the ultra-capacitor voltage reference slowly increases/decreases. The ultra-capacitor voltage has to follow the reference. If the tracking error is too big, the ultra-capacitor current reference will be too small, and therefore the dc bus voltage can not be maintained constant.

Maximum bandwidth is limited by the converter current capability. If the bandwidth is high, the ultra-capacitor voltage controller will generate the current reference greater than maximum current of the dc-dc converter. Therefore, the current controller G_{iC0} will be saturated, and as consequence the ultra-capacitor voltage controller will not be able to regulate the voltage; the control loop is saturated.

From (5.41) follows relation between proportional and integral gain

$$\frac{(1 + \omega_P T_F + k_{PC0}R_{C0})^2}{4\zeta_{C0}^2 T_F} - \omega_P - \omega_Z R_{C0}k_{PC0} = 0. \tag{5.42}$$

From Fig. 5.14 and (5.39) one can determine the ultra-capacitor voltage error as

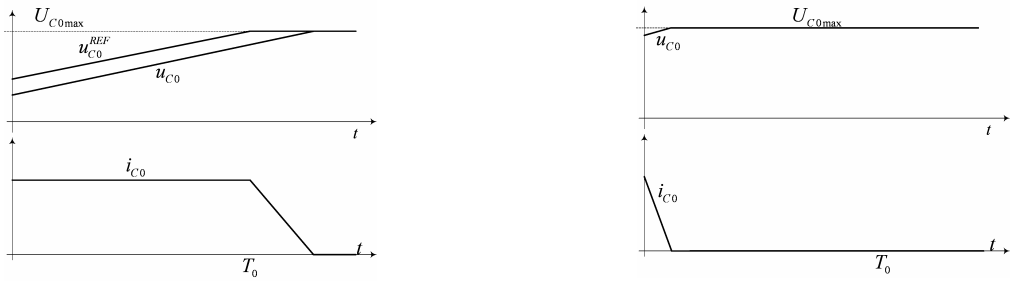
$$\Delta u_{C0}(s) = u_{C0}^{REF}(s) - u_{C0}(s) = i_{C0}(s)\frac{1}{k_{PC0}}. \tag{5.43}$$

Let the ultra-capacitor is charged/discharged with constant current i_{C0max} and the ultra-capacitor charge/discharge time is T_0. One can compute the ultra-capacitor voltage error as

$$\Delta u_{C0} = \frac{i_{C0\max}}{k_{PC0}}. \tag{5.44}$$

Fig. 5.15 illustrates (5.44) in two different cases: the ultra-capacitor voltage is lower than the maximum U_{C0max}, and the ultra-capacitor voltage is high, slightly lower than the

maximum U_{C0max}. The ultra-capacitor is charged by constant current i_{C0}. The current is determined by the dc bus voltage controller via the ultra-capacitor voltage reference in such a way to maintain the dc bus voltage constant. At the end of charging, at the moment T_0, the voltage reference $u_{C0(REF)}$ is limited on U_{C0max}, while the ultra-capacitor voltage is still increasing. Therefore, the error starts rapidly decreasing, causing decrease in the ultra-capacitor current. The decrease in the current will cause lost of the dc bus voltage control. If the charge/discharge time is long, the ultra-capacitor voltage error is low at the end of charging, at T_0, Fig. 5.15 (a). The most critical case is when the ultra-capacitor initial voltage is close to the maximum U_{C0max}. In this case that is not possible even to start controlling the dc bus voltage. This case is illustrated in Fig. 5.15 (b).



(a) (b)

Fig. 5.15 Relation between the ultra-capacitor controller gain and control performance. a) The ultra-capacitor voltage is lower than the maximum U_{C0max}. b) the ultra-capacitor voltage is high, slightly lower than the maximum U_{C0max}.

The controller proportional gain k_{PC0} is computed from (5.44) as

$$k_{PC0} \geq \frac{i_{C0\max}}{\Delta u_{C0\max}}. \tag{5.45}$$

Finally, substituting (5.45) into (5.42) yields the filter time constant as a function on the ultra-capacitor parameters and the closed loop damping factor

$$T_F = \frac{1}{2\omega_P^2}\left(\begin{array}{l} +\left(\omega_P + \omega_Z k_{PC0} R_{C0}\right)4\zeta_{C0}^2 - 2\left(1 + k_{PC0} R_{C0}\right) \\ \pm\sqrt{\left(\left(\omega_P + \omega_Z k_{PC0} R_{C0}\right)4\zeta_{C0}^2 - 2\left(1 + k_{PC0} R_{C0}\right)\right)^2 - 4\left(1 + k_{PC0} R_{C0}\right)^2 \omega_P^2} \end{array}\right). \tag{5.46}$$

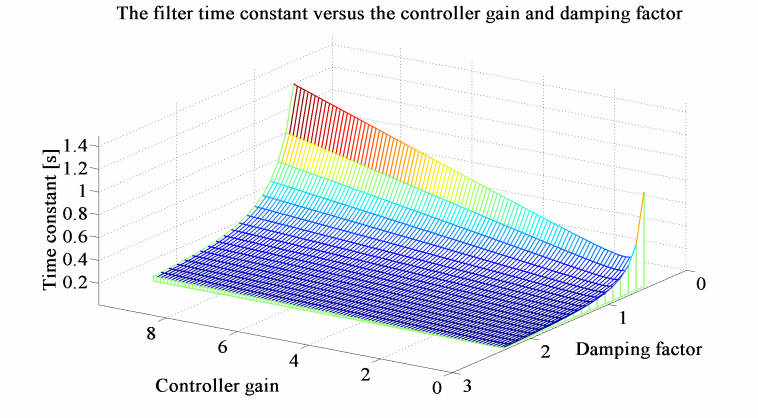
Fig. 5.16 shows the filter time constant versus the damping factor and the ultra-capacitor voltage controller gain.

5.5.4.2. The DC Bus Voltage Controller(s) Synthesis

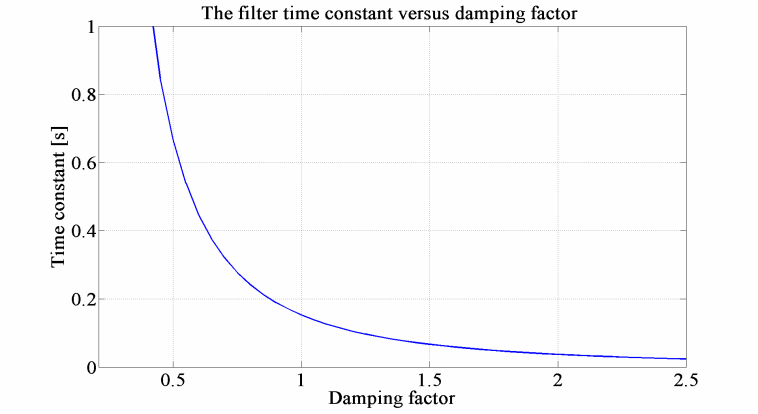
The dc bus voltage closed loop is illustrated in Fig. 5.17. The ultra-capacitor voltage control is cascaded with the dc bus voltage control. This may cause a problem in the controller synthesis because the ultra-capacitor voltage control loop is in order of magnitude slower than the dc bus voltage control loop. Let us see how the analysis can be simplified and the dc bus voltage controller designed.

The ultra-capacitor voltage control loop appears in the dc bus voltage control loop as transfer function

$$\frac{i_{C0}(s)}{u_{C0}^{REF}(s)} = \frac{G_{uC0}(s)}{1 + G_{uC0}(s)G_{C0}(s)G_F(s)} = \frac{k_{PC0}\left(T_F s + 1\right)\left(s + \omega_P\right)}{s^2 T_F + s\left(1 + \omega_P T_F + k_{PC0} R_{C0}\right) + \omega_P + \omega_Z R_{C0} k_{PC0}}. \tag{5.47}$$



(a)



(b)

Fig. 5.16 a) The filter time constant T_F versus damping factor and the controller gain. R_{C0} =2Ω, C_{C0}=0.3F, k_C=0.1/700 F/V. b) T_F versus damping factor at fixed controller gain k_{PC0} =5.

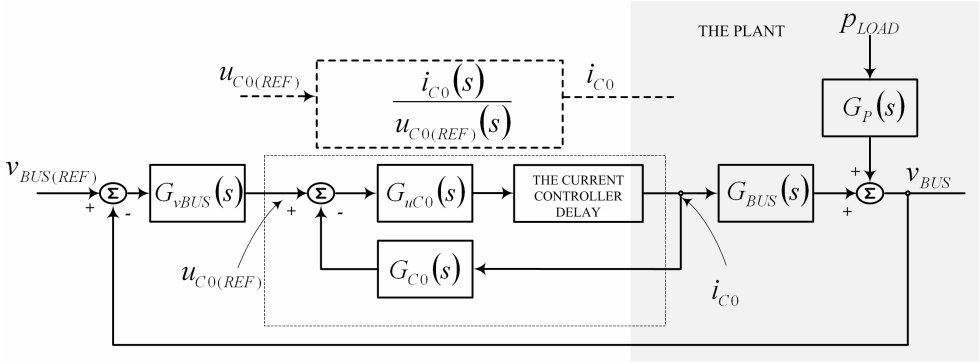


Fig. 5.17 Block diagram of the dc bus voltage closed loop control.

Assuming that the ultra-capacitor is large enough, (5.47) can be simplified as

$$\lim_{C_{C0}\to\infty}\left(\frac{G_{uC0}(s)}{1+G_{uC0}(s)G_{C0}(s)G_F(s)}\right)=\frac{k_{PC0}(sT_F+1)}{sT_F+(1+k_{PC0}R_{C0})}. \tag{5.48}$$

Because current capability of the dc-dc converter is limited, the bandwidth of the ultra-capacitor voltage controller is much lower than bandwidth of the dc bus voltage controller. Therefore, the filter time constant T_F can be assumed as infinite in comparison to the dc bus voltage response time. (5.48) is therefore simplified as

$$\lim_{T_F\to\infty}\left(\frac{k_{PC0}(sT_F+1)}{sT_F+(1+k_{PC0}R_{C0})}\right)=k_{PC0}\,. \tag{5.49}$$

This simplification can be done straightforward from (5.47) if taken into account that the dc bus voltage controller is much faster than the ultra-capacitor voltage controller. Therefore, one can assume that the ultra-capacitor voltage reference $u_{C0(REF)}$ is a unity step function and then apply the initial value theorem into (5.47).

$$\lim_{s\to\infty}\left(s\underbrace{\left(\frac{1}{s}\right)}_{\substack{UNITY\ STEP\\ FUNCTION}}\left(\frac{G_{uC0}(s)}{1+G_{uC0}(s)G_{C0}(s)G_F(s)}\right)\right)=k_{PC0} \tag{5.50}$$

Frequency response of the transfer function (5.47) and the approximation (5.50) have been compared. The comparison is illustrated in Fig. 5.18 Note that the approximated model and the original one are quite well matched at frequencies above 20Hz. In low frequency range, there is deviation in amplitude and phase characteristic.

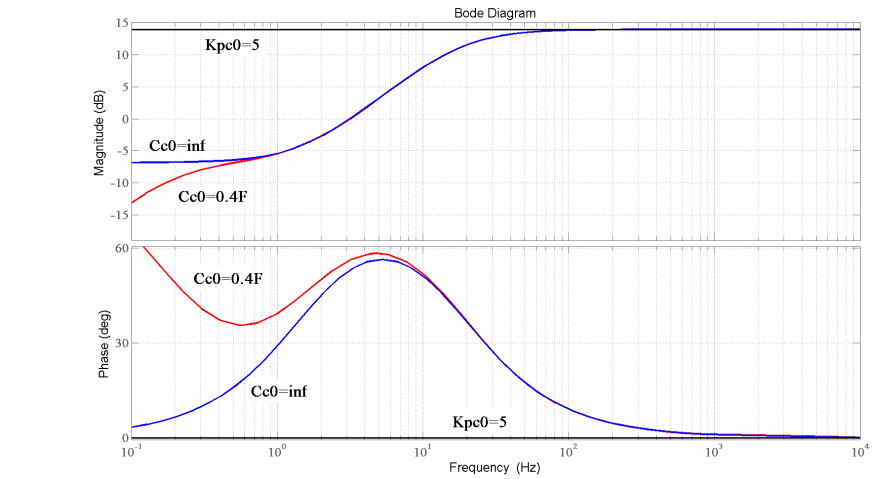


Fig. 5.18 Bode diagram of the transfer function (5.47). The ultra-capacitor feedback filter time constant is T_F=100ms. The ultra-capacitor C_{C0}=0.4F (the red trace) and an infinite capacitance (the blue trace).

Now, the dc bus voltage close loop transfer function is define as

$$\frac{v_{BUS}(s)}{v_{BUS}^{REF}(s)}=\frac{G_{vBUS}(s)G_{BUS}(s)k_{PC0}}{1+G_{vBUS}(s)G_{BUS}(s)k_{PC0}}= -\frac{k_{PC0}U_{C0}(1+sR_{ESR0}C_{BUS})}{s^2C_{BUS}(V_{BUS}-k_PR_{ESR}k_{PC0}U_{C0})-s(k_P+k_IR_{ESR}C_{BUS})k_{PC0}U_{C0}-k_Ik_{PC0}U_{C0}}\,. \tag{5.51}$$

The dc bus voltage controller is the classical PI controller

$$G_{CvBUS}(s)=\frac{k_P s+k_I}{s}. \tag{5.52}$$

The characteristic equation of the closed loop transfer function (5.51) is given by (5.53), where ζ_{BUS} is damping factor and ω_{BUS} is the closed loop natural frequency.

$$\begin{aligned} D_{vBUS}(s) &= s^2 - s\frac{(k_P+k_I R_{ESR}C_{BUS})k_{PC0}U_{C0}}{C_{BUS}(V_{BUS}-k_P R_{ESR}k_{PC0}U_{C0})} - \frac{k_I k_{PC0}U_{C0}}{C_{BUS}(V_{BUS}-k_P R_{ESR}k_{PC0}U_{C0})} \\ &= s^2 + s2\zeta_{BUS}\omega_{BUS} + \omega_{BUS}^2 \end{aligned} \tag{5.53}$$

Proportional and integral gains are computed using the Butterworth criteria ($\zeta_{BUS}=0.7$)

$$\begin{aligned} k_P &= -\frac{\omega_{BUS}C_{BUS}V_{BUS}(1.4-\omega_{BUS}R_{ESR}C_{BUS})}{k_{PC0}U_{C0}(1-\omega_{BUS}R_{ESR}C_{BUS}(1.4-\omega_{BUS}R_{ESR}C_{BUS}))} \\ k_I &= -\frac{\omega_{BUS}^2 C_{BUS}V_{BUS}}{k_{PC0}U_{C0}(1-\omega_{BUS}R_{ESR}C_{BUS}(1.4-\omega_{BUS}R_{ESR}C_{BUS}))} \end{aligned}. \tag{5.54}$$

If the dc bus capacitor series resistance can be neglected, $1>>\omega_{BUS}R_{ESR}C_{BUS}$, (5.54) is simplified and the controller gains computed as

$$\begin{aligned} k_P &= -\frac{\omega_{BUS}C_{BUS}V_{BUS}1.4}{k_{PC0}U_{C0}} \\ k_I &= -\frac{\omega_{BUS}^2 C_{BUS}V_{BUS}}{k_{PC0}U_{C0}} \end{aligned}. \tag{5.55}$$

The controllers' gains depend on the ultra-capacitor voltage, which is in general case not constant over time, taking value from the minimum U_{C0min} to the maximum U_{C0max}. The dc bus voltage controller has to be designed in such a way to provide sufficient damping in the worst case of the ultra-capacitor voltage U_{C0}. To determine the worst case, one can draw the close loop root locus versus the ultra-capacitor voltage. The root locus is depicted in Fig. 5.19.

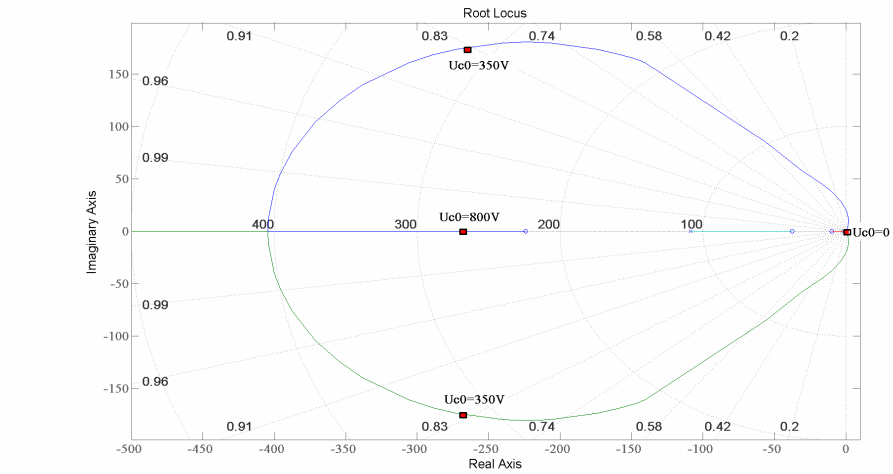


Fig. 5.19 The dc bus voltage closed loop root locus versus the ultra-capacitor voltage U_{C0}. V_{BUS}=700V, f_{BUS}=25Hz, k_{PBUS}=0.08, k_{IBUS}=16.

As seen, the damping factor increases as the ultra-capacitor voltage increases. Therefore, the controllers have to be designed for the minimum ultra-capacitor voltage U_{C0min}.

In that case, the damping factor will not be lower than the desired for any value of the ultra-capacitor voltage.

The gains of the dc bus voltage controllers can now be computed from (5.54), taking the dc bus voltage and the ultra-capacitor voltage reference from Fig. 3.5.

$$\begin{aligned} k_{P\max} &= k_P\left(V_{BUS\max}, U_{C0inM}\right) \\ k_{I\max} &= k_I\left(V_{BUS\max}, U_{C0inM}\right) \\ k_{P\min} &= k_P\left(V_{BUS\min}, U_{C0\min}\right) \\ k_{I\min} &= k_I\left(V_{BUS\min}, U_{C0\min}\right) \end{aligned} \tag{5.56}$$

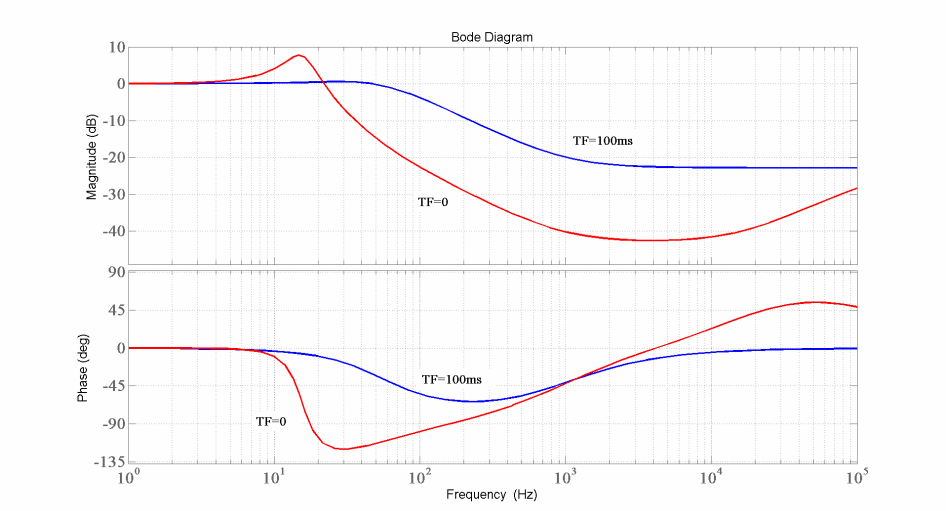


Fig. 5.20 Bode diagram of the dc bus voltage transfer function $v_{BUS}(s)/v_{BUS(REF)}(s)$ for different time constant of the ultra-capacitor voltage feedback filter.

5.5.5. Simulation and Experimental Results

The model and control scheme presented in this chapter were simulated by Matlab/Simulink. For simulation purpose, non-linear model (Fig. 5.7) was used. The model and control scheme were also experimentally verified. Some of the simulation and experimental results are presented and discussed hereafter. The control algorithm, PWM and protection functions were implemented in a fixed-point 32 bit digital signal processor (DSP). The complete control algorithm is executed at 50 kHz. The controllers were implemented as ordinary proportional-integral (PI) controllers. The controller parameters were computed in continuous time domain (s), and then translated into discrete time domain, (z), using the approximation $s = \frac{1-z^{-1}}{T_S}$, where $T_S = 200\mu s$ is the sampling period. The control system specification is given in TABLE 5-1 on the next page.

5.5.5.1. Simulation Results

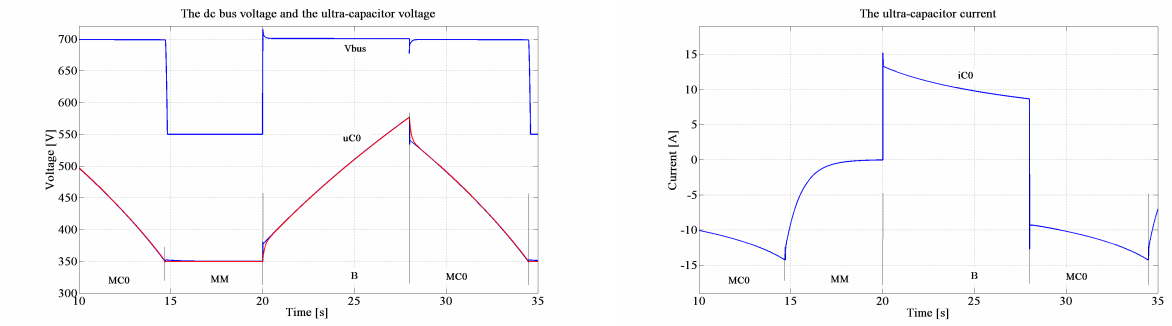
Fig. 5.21 shows the waveforms during an entire operating cycle: the mains motoring (**MM**), braking (**B**), the ultra-capacitor motoring (**MC$_0$**) and the mains motoring mode (**MM**).

Fig. 5.22 (a) shows the dc bus voltage and the ultra-capacitor current and voltage waveforms during transition from the mains motoring mode to braking mode. Fig. 5.22 (b)

shows the same waveforms during transition from braking to the ultra-capacitor motoring mode.

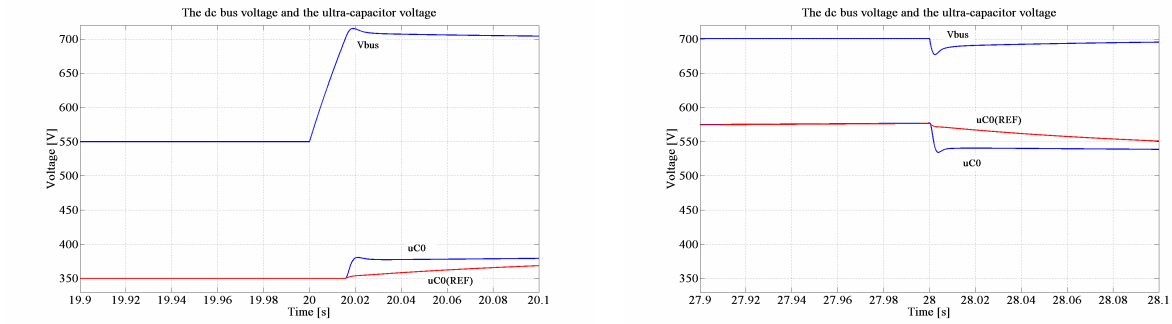
TABLE 5-1. Specification of the control system.

ULTRA-CAPACITOR		DC BUS	
U_{C0max}	780V	V_{BUSmax}	*700V*
U_{C0inM}	350V	V_{BUSmin}	*450V*
U_{C0min}	250V	C_{BUS}	*820μF*
C_{C0}	0.4F	R_{ESR}	*190mΩ*
R_{C0}	2Ω	Bandwidth	*50Hz*
Controller U_{C0}	$G_{uC0}(z)=5$	Controller V_{BUSmax}	$G_{vBUS\max}(z)=-0.145-\frac{0.0065}{1-z^{-1}}$
Feedback filter	$G_F(z)=\frac{1}{500(1-z^{-1})+1}$	Controller V_{BUSmin}	$G_{vBUS\min}(z)=-0.2-\frac{0.009}{1-z^{-1}}$



(a) (b)

Fig. 5.21 Simulation waveforms of the dc bus voltage v_{BUS}, the ultra-capacitor voltage u_{C0} and current i_{C0} during the mains motoring- braking-the ultra-capacitor motoring mode. v_{BUSmax}=700V, f_B=50Hz, P_{LOAD}=+/- 5000W, C_{BUS}=820μF, C_{C0}=0.4F.

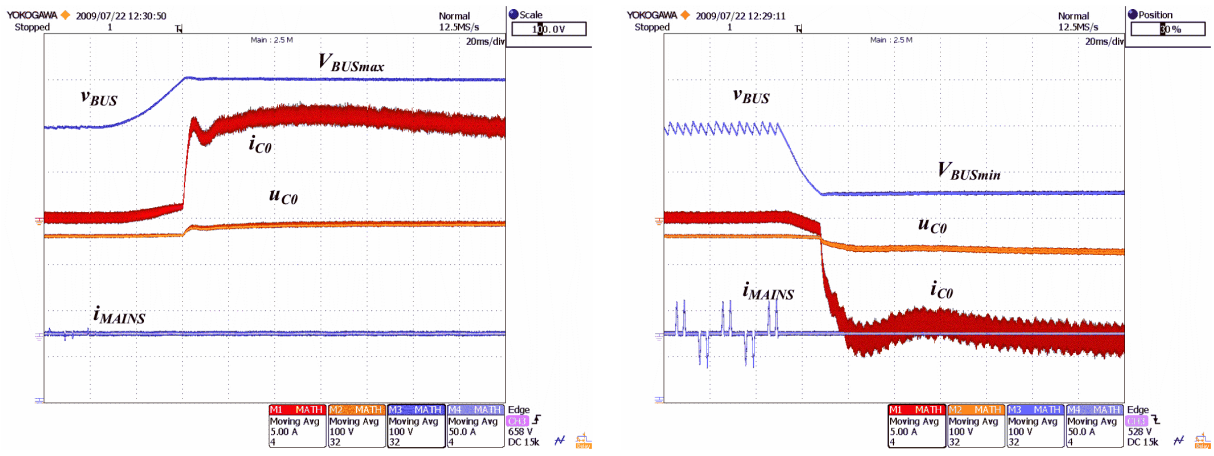


(a) (b)

Fig. 5.22 Simulation waveforms of the dc bus voltage v_{BUS}, the ultra-capacitor voltage u_{C0} and current i_{C0}. a) transition from **MM** to **B**, and b) transition from **B** to **MC0** mode v_{BUSmax}=700V, f_B=50Hz, P_{LOAD}=+/- 5000W, C_{BUS}=820μF, C_{C0}=0.4F.

5.5.5.2. Experimental Results

The control system was experimentally tested under different conditions. Fig. 5.23 (a) shows the waveforms when the drive runs on the full speed and then is stopped suddenly. The dc bus voltage rapidly increases within 30ms until reaches reference V_{BUSmax}=700V. At that instant dc bus voltage controller starts to regulate dc bus voltage with slight overshoot of approximately 12V. The ultra-capacitor current is approximately 13A. Similar test was done in case of power interruption. The drive is loaded and then the mains is interrupted. The dc bus voltage falls to minimum V_{BUSmin}=450V within 10ms, and then stays well regulate to that level. As seen from Fig. 5.23 (b) the dc bus voltage has an under-shoot of approximately 12V during settling time of about 30ms. The ultra-capacitor discharge current is approximately -13A. The initial step in the ultra-capacitor voltage seen in the both experiments is caused by the voltage drop across the capacitor internal resistance R_{C0}. The ultra-capacitor charging/discharging power computed from the ultra-capacitor voltage and current is roughly 4500W.



(a) (b)

Fig. 5.23 Experimental waveforms of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div], the dc bus voltage v_{BUS} [100V/div] and the mains current i_{MAINS} [50A/div]. a) Transition from the mains motoring mode to the braking mode. b) Transition from the mains motoring to ride-through mode.

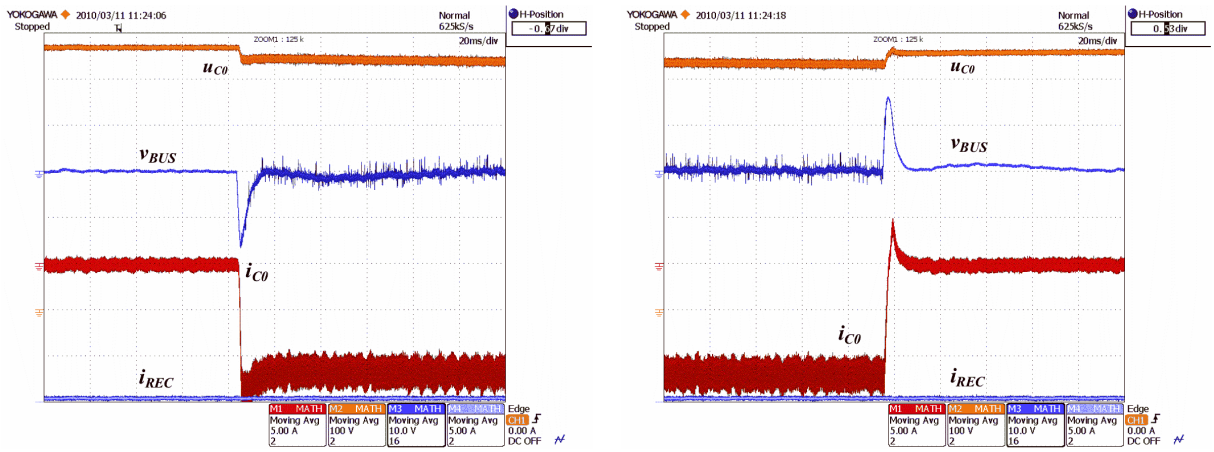
Fig. 5.24 illustrates the functionality of the dc bus voltage braking controller, $G_{VBUSmax}$. The ultra-capacitor is charged on 550V. Fig. 5.24 (a) shows the ultra-capacitor voltage and current, ac component of the dc bus voltage and rectifier current when the drive switches from stand-by mode to the ultra-capacitor mode. The controller response time is approximately 8 ms, while the voltage undershoot is approximately -15V. Fig. 5.24 (b) shows the waveforms when the drive switches from the ultra-capacitor mode to stand-by mode. The voltage overshoot is approximately 14V. The controller response time is similar to the previous one.

5.5.6. Discussion on the Current Controller Response Time and the DC Bus Voltage Control

In the above analysis, response time of the current controller has been neglected and the current i_{C0} has been taken as an independent control variable. This is sufficiently accurate approximation if the dc bus control is slow compared to the current controller. In most of the applications that is the case. The current controller response time is $T_{iC0} \leq 500\mu s$, while

response time of the dc bus voltage controller is $T_{vBUS} \geq 5$ms. Therefore, the current controller can be considered as a pure gain without delay, and the dc bus voltage controller can be designed as it has been described.

However, in certain applications the dc bus voltage controller has to be fast, having response time in order of 1ms. Typical application is variable speed drive converter equipped with a small dc bus capacitor. In such an application, the dc bus voltage controller has to be able to regulate the voltage regardless on the dc bus load variation. Thus, the current controller response time has to be taken into account when designing the dc bus voltage controllers.



(a) (b)

Fig. 5.24 Experimental waveforms of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div], the dc bus voltage v_{BUS} [100V/div] and the rectifier current i_{REC} [5A/div]. The dc bus voltage controller response on a step load. a) Transition from stand by mode to the ultra-capacitor motoring mode, b) transition from the ultra-capacitor motoring mode to stand by mode. V_{BUSmax}=700V, u_{C0}=550V and f_B=50Hz.

6. DISCUSSION AND CONCLUSIONS

6.1. Concept of the Ultra-capacitor Based Controlled Electric Drive

To compare the ultra-capacitor based regenerative electric drive with state of the art solutions, the following two features are considered:

1. The drive immunity on the mains interruption, and
2. The drive system cost versus braking and ride-through time.

6.1.1. The Drive Immunity on the Mains Power Interruption

Comparison of the ultra-capacitor based regenerative drive with back-to-back and matrix drive is summarized in TABLE 6-1. The ride-through time in braking and motoring mode are compared. The back-to-back drives have short-term ride-through capability, in order of 20ms, while the matrix converter drives do not have ride-through capability at all. In contrast to this, the ultra-capacitor based drives have the ride-through capability, wherein the ride-through time is the system design parameter.

TABLE 6-1: Comparison of different drive concepts regarding ride-through capability.

	Back-to-back drive converter	Matrix drive converter	The ultra-capacitor based drive
Ride-through time in motoring mode	Depends on the load. At full load and 100% interruption, the ride-through time is less than 100ms	No ride-through capability	From 100ms up to several seconds or minutes, depending on the design criteria
Ride-through time in braking mode	Normally less the mains period (20ms)	No ride-through capability	From few seconds up to minutes, depending on the design criteria

6.1.2. The Drive Cost Comparison

The cost of the ultra-capacitor based controlled electric drive depends on the braking and ride-through capability. Longer braking and ride-through time the bigger the ultra-capacitor is. In contrast to this, cost of back-to-back and matrix converters is practically independent on the braking time. If the braking time is shorter than the critical time T_{CR}, the ultra-capacitor based solution is more cost effective than back-to-back and matrix solution. The critical braking time T_{CR} is currently between 10 and 15s. This limit will go up in the near future with development of new technology of the ultra-capacitors. Regarding extended ride-through capability the ultra-capacitor solution is the most cost effective solution regardless on the ride-through time. Reason for this lays in the fact that an additional energy storage device and dc-dc or dc-ac converter are required for back-to-back and matrix solution. Fig. 6.1 illustrates the drive cost versus braking and ride-through time for different drive technology.

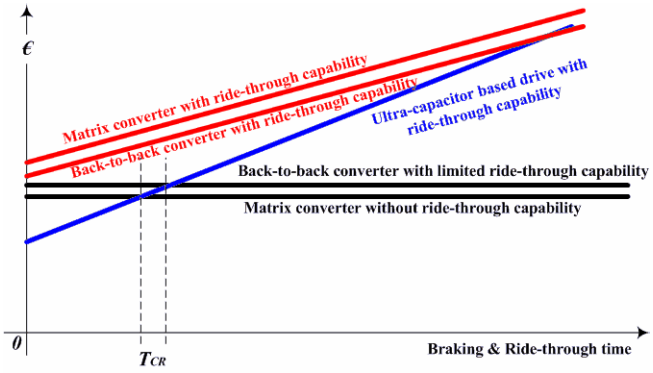
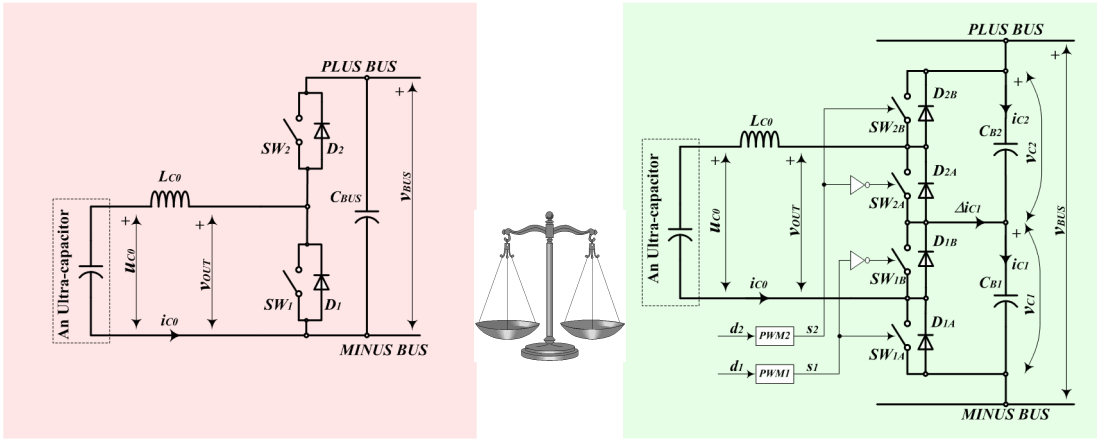


Fig. 6.1 Cost comparison of the ultra-capacitor based regenerative drive versus back-to-back and matrix converter regarding braking time and ride-through time.

6.2. Interface DC-DC Converter

When comparing different power converter topologies, a few parameters are important. The first one is power rating of the active switches. The second one is size of the passive components, particularly inductors. Finally, the conversion losses and efficiency are parameters to be also considered.



(a) (b)

Fig. 6.2 Two-level versus three-level dc-dc converter.

6.2.1. Semiconductors Switches

Power rating and surface of chip of the semiconductor switch are defined by two parameters: the switch utilization factor [92], [115] and the switch voltage rating.

6.2.1.1. The Switch Utilization Factor SUF

The switch utilization factor of a power converter that consists of N switches (including diodes) is defined as

$$SUF = \frac{P_{C0}}{S_{SW}} = \frac{P_{C0}}{\sum_{j=1}^{N} V_{S\max(j)} I_{S\max(j)}}, \tag{6.1}$$

where I_{Smax} and V_{Smax} are the switches peak current and peak voltage and P_{C0} is the conversion power.

The switch utilization factor of two-level and three-level topology is computed from (4.15) and (6.1) as

$$SUF_{(2L)} = \frac{P_{C0}}{S_{SW}} = \frac{P_{C0}}{\underbrace{2v_{BUS}i_{C0}}_{SWITCHES} + \underbrace{2v_{BUS}i_{C0}}_{FWD}} = \frac{d}{4}, \tag{6.2}$$

$$SUF_{(3L)} = \frac{P_{C0}}{S_{SW}} = \frac{P_{C0}}{\underbrace{4\frac{v_{BUS}}{2}i_{C0}}_{SWITCHES} + \underbrace{4\frac{v_{BUS}}{2}i_{C0}}_{FWD}} = \frac{d}{4}, \tag{6.3}$$

where subscript (*3L*) and (*2L*) denote three-level and two-level. Please, note that the SUF of the two-level and three-level converter is the same. From (6.2) and (6.3) it seems that the two topologies are equivalent.

6.2.1.2. The Switches Voltage Rating

The switches voltage rating has been taken into account as a parameter in the switch utilization factor (6.1). However, this is not sufficient to compare two topologies with different voltage rating of the switches. Semiconductor switch conduction and switching performance depend strongly on the switch voltage rating and the switch technology. Generally, lower voltage rating means lower conduction losses, better switching performance, higher efficiency and lower cost. For example, let us consider a 400V supplied variable speed drive. The dc bus voltage varies from 500V up to 850V. For two-level dc-dc converter (Fig. 4.1 (a), (b)), the switches and diodes voltage rating is the full dc bus voltage. For this voltage rating, 1200V IGBT and 1200V fast diode are used. In this case, maximum switching frequency is limited by the switching performance of the IGBT and the diode. To reduce switching losses, soft switching techniques can be employed [36].

In contrast to this, for the three-level converter, the switches and diodes voltage rating is a half of dc bus voltage. In this case, 600V rated IGBT or 500V super junction MOSFET and ultra-fast diodes can be used. Switching losses of 600V rated IGBT and diode are three to four times lower than the switching losses of a 1200V rated IGBT and diode. Conduction losses are lower too in comparison to a 1200V device. If compare two MOSFETs, one 1200V and one 600V rated, the difference in conduction losses is significant, because the drain source on-state resistance depends strongly on the voltage rating [41].

6.2.2. Passive Components

6.2.2.1. Filter Inductor L_{C0}

Comparison of the filter inductor is based on the comparison of the inductance L_{C0} at the same conditions: the current ripple, switching frequency and the dc bus voltage. The inductance of the three-level topology is computed from (4.8), while the inductance for two-level topology is computed from following equation

$$\Delta i_{C0}(d) = \frac{v_{BUS}}{L_{C0} f_{SW}}(1-d)d\,. \tag{6.4}$$

The inductors size is compared from (4.8) and (6.4) as

$$\frac{size_{(3L)}}{size_{(2L)}} \approx \frac{L_{0(3L)} I_{PEAK(3L)} I_{RMS(3L)}}{L_{0(2L)} I_{PEAK(2L)} I_{RMS(2L)}} = \frac{L_{0(3L)}}{L_{0(2L)}}, \tag{6.5}$$

where subscript *(3L)* and *(2L)* denote three-level and two-level.

Fig. 6.3 shows the inductor relative size versus minimum duty cycle d_{min}, where the minimum duty cycle corresponds to the ultra-capacitor minimum voltage U_{C0min} (3.2). Note that the inductor for the three-level topology is 25% of the inductor for two-level topology when the minimum duty cycle is inferior to 1/2. The inductor size increases from 25% up to 50% as the minimum duty cycle increases from 1/2 towards 1. Comparison of the inductor size computed by (6.5) is not sufficient to compare the inductor volume. For that, the inductor losses have to be alos considered and compared. That comparison is given in section 6.2.3.

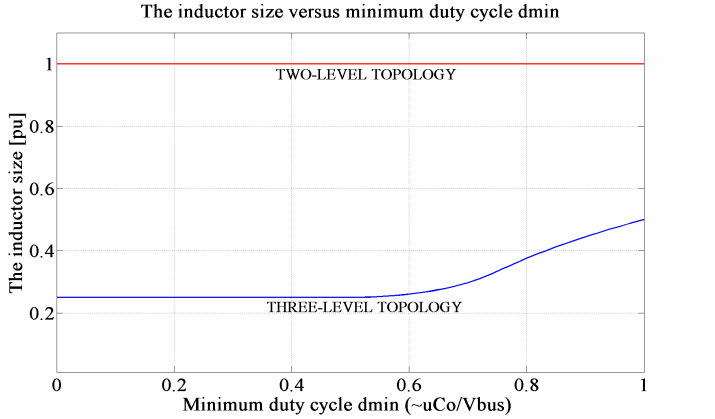


Fig. 6.3 Comparison of the filter inductor size versus minimum duty cycle (corresponds to the minimum ultra-capacitor voltage).

6.2.2.2. The DC Bus Filter Capacitors C_{B1}, C_{B2}

The filter capacitors are compared at the same conditions: the voltage ripple, switching frequency, dc bus voltage and conversion power. The filter capacitor of the three-level topology is computed from (4.22), while the capacitor of the two-level topology is computed from equation

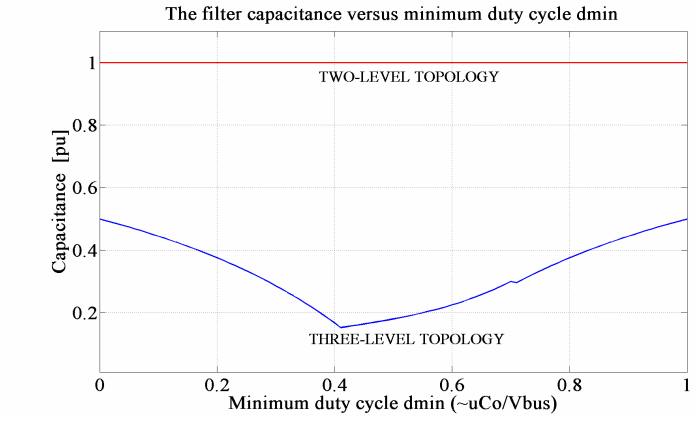
$$\Delta v_{BUS}(d) = \frac{P_{C0}}{C v_{BUS} f_{SW}}(1-d). \tag{6.6}$$

The capacitors size (volume) is compared from the capacitor(s) total energy, taking into account that the voltage rating of capacitor(s) is different. One filter capacitor rated for the full dc bus voltage is used in two-level topology, and two capacitors rated for half dc bus voltage are used in three-level topology. From (4.22) and (6.6) follows

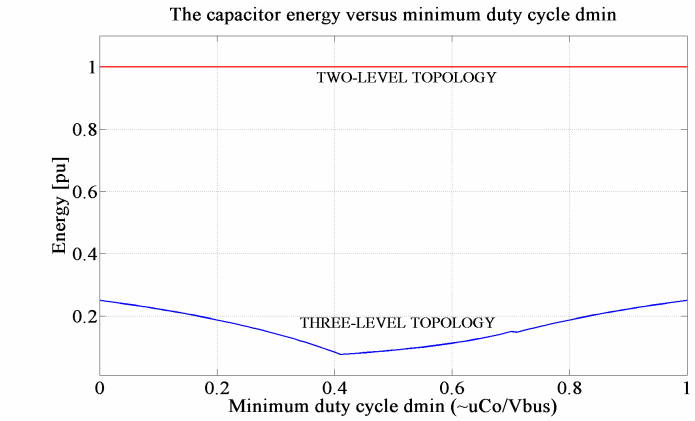
$$\frac{size_{(3L)}}{size_{(2L)}} \approx \frac{2\left(\frac{1}{2}C_{(3L)}V_{C(3L)}^2\right)}{\frac{1}{2}C_{(2L)}V_{C(2L)}^2} = \frac{C_{(3L)}}{2C_{(2L)}}, \tag{6.7}$$

where subscript *(3L)* and *(2L)* denote three-level and two-level.

Fig. 6.4 shows the capacitor relative capacitance and energy (which corresponds to size) versus minimum duty cycle d_{min}. Note that the capacitance of the three-level topology is below 20% of that of two-level topology when the minimum duty cycle is inferior to 1/2. The capacitance increases from 20% up to 50% as the minimum duty cycle increases from 1/2 towards 1. The capacitors total energy (size) varies from 10% at minimum duty cycle of 1/2 up to 25% at duty cycle of 1. The capacitor losses are not compared because high quality film capacitors are used and therefore the losses can be neglected.



(a)



(b)

Fig. 6.4 Comparison of the filter capacitance (a) and the filter capacitor total energy (b) versus minimum duty cycle (corresponds to the minimum ultra-capacitor voltage). The capacitance and energy are computed as ratio of the capacitance and energy of the filter capacitor of two-level to three-level topology.

6.2.3. Conversion Losses

The switches losses are computed from the models (4.30) and (4.31), and data in TABLE 4-1. Fig. 6.5 shows 3-D graph of relative losses versus the conversion power and

duty cycle, where duty cycle corresponds to the ultra-capacitor voltage. The relative losses are computed as ratio of the three-level converter losses to the two-level converter losses. The losses vary from 85% at maximum duty cycle up to 89% at minimum duty cycle. That means heat sink of the three-level converter is 10% to 15% smaller than that of the two-level converter.

The inductor losses are computed from the losses model (4.16) and data in TABLE 4-1. Fig. 6.6 shows the inductor relative losses versus the conversion power and the ultra-capacitor voltage. The relative losses are computed as ratio of the three-level converter losses to the two-level converter losses. Please note that the relative losses vary between 25% and 45% at full load, while at light load the losses vary from approximately 5% up to 50%.

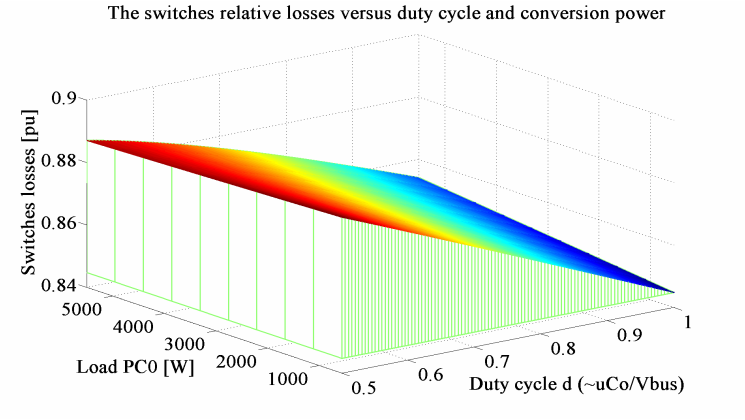


Fig. 6.5 The switches (IGBT+FWD) relative losses versus duty cycle and conversion power. The relative losses are computed as ratio of total losses of two-level dc-dc converter to the three-level dc-dc converter.

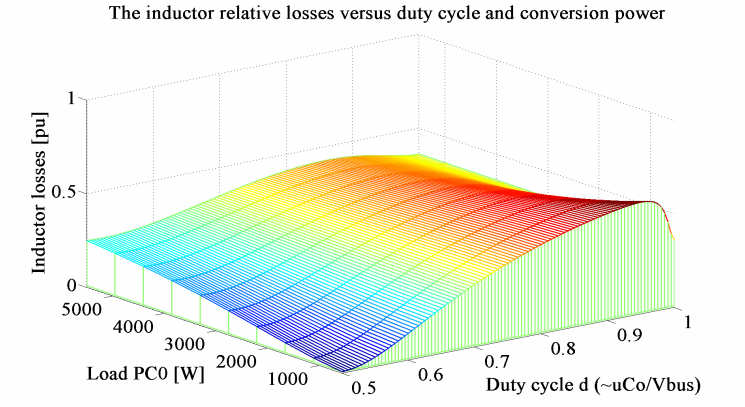


Fig. 6.6 The filter inductor relative losses versus duty cycle and conversion power. The relative losses are computed as ratio of total losses of two-level dc-dc converter to the three-level dc-dc converter.

6.2.4. Model and Control Scheme

Most of the control method presented in the literature are focused on hybrid electric vehicle and power sources [14], [27]-[29], [32], [33]-[35], [43]-[47]. Only a few publications are focused on control of the ultra-capacitor based electric drives [5], [21], [22]. In

comparison to state of the art, the model and control scheme proposed in this part of the dissertation has the following features:

- The entire conversion system is modeled, considering all parasitic effects, such as the voltage-dependent capacitance of the ultra-capacitor. This is particularly important for the ultra-capacitor voltage controller design and synthesis.
- The dc bus voltage is asymptotically regulated to a pre-defined reference, where the reference depends on operating mode of the drive.
- The ultra-capacitor voltage is asymptotically regulated to a desired reference, where the reference is determined depending on the application requirement. Doing this, the drive system is kept ready for the next braking and ride-through sequence.

6.3. Conclusions

Application of ultra-capacitor based energy storage devices in controlled electric drives has been discussed in this part of this dissertation. The ultra-capacitor is used to store the drive braking energy and restore the energy whenever it is possible. Moreover, the ultra-capacitor can be utilized as emergency energy storage in case of the mains power interruption.

Because it is not convenient to connect the ultra-capacitor directly to the controlled electric drive, an interface dc-dc converter is necessary. State of the art topologies of interface dc-dc converters are discussed and a new three-level dc-dc converter is proposed. The proposed topology is analysed and design guidelines are given. The model of the entire conversion system is developed and a new control scheme is proposed. The control objective of the proposed control scheme is to control the ultra-capacitor current and the dc bus mid-point voltage. The second control objective is to asymptotically regulate the dc bus voltage to desired reference, depending on the operating mode. The ultra-capacitor state of charge (SOC) control is third control objective.

In comparison to state of the art solutions, such as back-to-back and matrix drive converters, the proposed ultra-capacitor based controlled electric drive has the following advantages:

- The system ride-through capability is extended. The drive time autonomy is a design parameter. Depending on the application, the ride-through time could be extended up to 15s. Above this limit, it is not cost effective to use the ultra-capacitors. Electrochemical batteries are more suitable solution. This limit will move up with development of new generation of ultra-capacitors.
- The system functionality, including braking capability is not linked to the mains reliability.
- Regarding the system installation cost, the proposed ultra-capacitor based regenerative electric drive is cost effective in applications that require braking time up to 10 to 15s. Above this limit, back-to-back and matrix converter based drive is better solutions.

The three-level dc-dc converter has the following features in comparison to state of the art topologies:

- The semiconductors losses are smaller than that of the state of the art topologies, such as two-level topology and isolated topologies.

- The output inductor is smaller than that of the two-level topology. The inductor size depends on the ultra-capacitor minimum voltage, and it varies from 25% to 50% of that of the two-level converter.
- The input filter capacitor is also smaller. The capacitor volume varies between 10% and 25% of that of the two-level converter.

PART THREE: THREE-TERMINAL POWER FACTOR CORRECTION DEVICE

7. BACKGROUND AND STATE OF THE ART

7.1. Background

Three-phase ac-dc power converters (rectifiers) are widely used in many applications, such as variable speed drives, UPS, data centers and telecom power supplies and many other applications. The rectifier main design objectives are efficiency, size, reliability and cost. Recently, the input current harmonics have become a more and more important design criterion. In some applications, the dc bus voltage has to be constant and greater than the mains voltage regardless on the mains voltage variations and disturbances. A further issue in the application of three-phase rectifiers is single-phase supply operation. Single-phase supply could be the mains degradation when one phase is lost. In such a case, the rectifier is supplied with one phase-to-phase voltage and from the rectifier sideequvalent to a single-phase supply. Another application example is rural single-phase network or some specific application of variable speed drives, such as irrigation systems.

7.2. State of the Art

Numerous different rectifier topologies have been presented in literature and used in applications. The most important topologies are briefly presented in this section as state of the art solutions.

Three-phase diode front-end rectifier with passive LC filter is the most common rectifier topology. The circuit diagram is depicted in Fig. 7.1 (a). This is the simplest and the most robust solution. However, it has numerous disadvantages, which make it undesirable in many applications. The input current total harmonic distortion (THD) is relatively high and the power factor (PF) is low. THD depends on the inductor and capacitor size, and it could be as high as 100%, or higher. The dc bus voltage is uncontrolled and slightly lower than the mains phase-to-phase peak voltage. In addition, low frequency voltage ripple is significant too. The dc bus filter capacitor C_{BUS} and inductor L_{BUS} are bulky, lossy and expensive.

The single-switch three-phase continuous conduction mode (CCM) boost rectifier is a solution that offers some advantages compared to the diode front-end rectifier [49]-[51]. The circuit diagram is shown in Fig. 7.1 (b). The rectifier output current i_{REC} is constant and therefore the mains current is a square waveform of $2\pi/3$ radians with a THD of approximately 30%. The dc bus voltage is controlled and boosted above the mains phase-to-phase peak voltage. Low frequency voltage ripple is negligible compared to the diode rectifier. A variant of this topology is discontinuous conduction mode (DCM) boost rectifier [52]-[55] (Fig. 7.1 (c)). This topology offers lower THD of the input current than CCM boost rectifier. The common disadvantage of those two topologies is power rating of the switch and the boost diode. Both of them are rated at full dc bus voltage v_{BUS} and full rectifier current i_{REC}. The double-boost rectifier, Fig. 7.1 (d), is a solution that offers better efficiency and smaller filter inductor in comparison to the single-switch boost topology.

An electronic smoothing inductor (ELSI) has been proposed in [61]-[63] (see Fig. 7.1 (e)). A low voltage H bridge with a low voltage capacitor and a small filtering inductor is connected between the rectifier and the dc bus plus rail. This emulates an infinity inductance

and maintains the rectifier current constant. The active components are rated on a fraction of the dc bus voltage. The main disadvantage of this topology is the fact that the dc bus voltage is equal to the average value of the rectifier voltage. This means the dc bus voltage is even lower than that of the ordinary diode rectifier with capacitive filter. In some applications, this is a serious limiting factor.

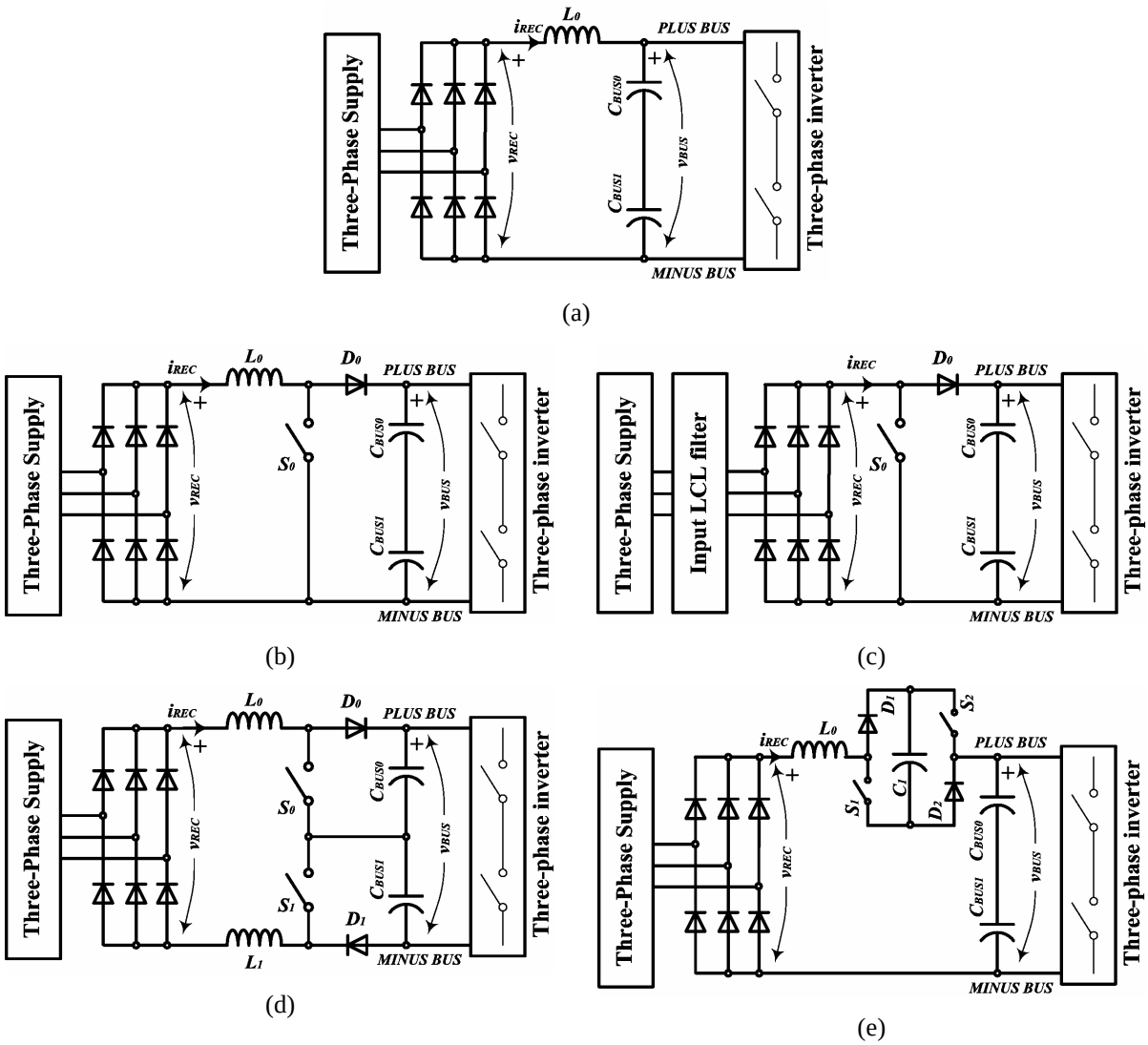


Fig. 7.1 State of the art rectifier topologies a) diode front end rectifier, b) continuous conduction mode (CCM) single switch boost rectifier, c) discontinuous conduction mode (DCM) single switch boost rectifier, d) double boost, and e) an electronic smoothing inductor (ESI) rectifier.

7.3. A Novel Half-DC-Bus-Voltage Rated Boost Rectifier

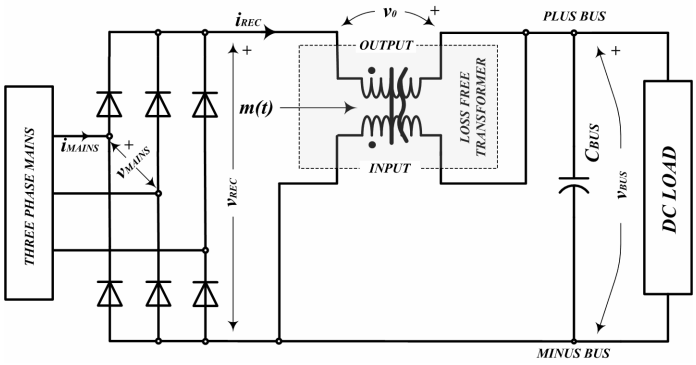
In this part of the dissertation, chapters 8 to 11, a novel hybrid half-dc-bus-voltage rated boost rectifier is presented [116]. The core of the presented solution is a unidirectional power conversion device, so-called the loss-free transformer (LFT), see. The LFT has two output and input terminals. The output is series connected between the rectifier plus rail and the dc bus plus rail. The input is parallel connected with the dc bus. Because of such a

connection, it is possible to control the rectifier current and to boost the dc bus voltage above the mains phase-to-phase peak voltage. The LFT is composed of two uni-directional dc-dc converters. The first converter is rated on half of the dc bus voltage and full rectifier current, while the second one is rated on half dc bus voltage and a fraction of the input rectifier current. The first converter regulates the rectifier current and the dc bus voltage, while second one assists to the first one. Power rating, size and efficiency of the entire conversion system depend strongly on the ratio of the dc bus voltage to the rectifier voltage (boosting factor). For example, if the boosting factor is low, below 1.5, the efficiency is around 98 to 99%

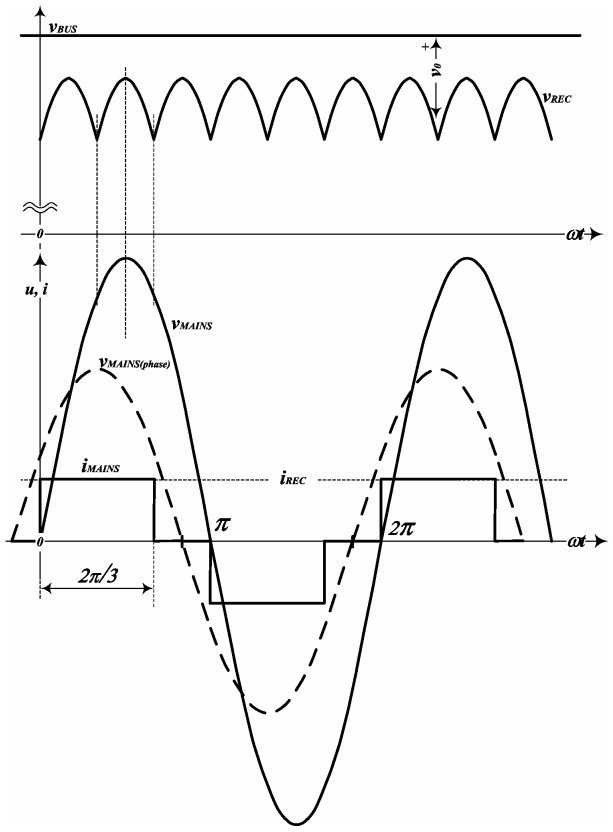
8. HYBRID HALF-DC-BUS-VOLTAGE RATED BOOST RECTIFIER

8.1. The Basic Principle

The basic principle of the proposed boost rectifier is illustrated in Fig. 8.1. One can distinguish a three-phase diode rectifier, a dc bus filter capacitor C_{BUS}, the dc bus load and a two-terminal device designated as loss free-transformer (LFT).



(a)



(b)

Fig. 8.1 a) Basic principle of the proposed boost rectifier, b) the rectifier voltage v_{REC}, the dc bus voltage v_{BUS} and the compensation voltage v_0, the mains phase-to-phase voltage v_{MAINS}, the mains phase-to-neutral voltage $v_{MAINS(phase)}$ and the mains phase current i_{MAINS}.

The output terminal of the LFT is connected between the rectifier plus rail and the dc bus plus rail, while the input is connected in parallel with the dc bus. The LFT is controlled by a control variable *m(t)*.

Let the mains be symmetrical three phase mains with phase to phase voltages given as

$$v_{MAINS}(t) = V_{PEAK} \sin\left(\omega_m t - p\frac{2\pi}{3}\right), \tag{8.1}$$

where *p=0,1,2* is the phase order.

Let the rectifier current i_{REC} be constant or pseudo constant (being controlled by the LFT). Since the rectifier operates in continuous conduction mode (CCM), the rectifier output voltage is

$$v_{REC}(t) = V_{PEAK} \cdot \sin \omega_m t\big|_{60° < \omega t \le 120°}, \tag{8.2}$$

with the period $T=T_m/6$, where T_m is the mains period. The rectifier voltage, the dc bus voltage, the mains phase voltage and phase-to-phase voltage, and the mains current are illustrated in Fig. 8.1 (b).

The rectifier average voltage and average current are

$$v_{REC(AV)} = \frac{6}{T_m}\int_{T_m/6}^{T_m/3} v_{REC}(t)dt = V_{PEAK}\frac{3}{\pi}, \tag{8.3}$$

$$i_{REC(AV)} = \frac{P_{LOAD}}{v_{REC(AV)}} = \frac{P_{LOAD}}{V_{PEAK}}\frac{\pi}{3}. \tag{8.4}$$

As it can be seen from Fig. 8.1, the dc bus voltage v_{BUS} is sum of the rectifier voltage v_{REC} and the auxiliary boost voltage $v_0(t)$, where $v_0(t)$ is generated and controlled by the LFT. Hence, the dc bus voltage can be directly controlled by the boost voltage $v_0(t)$ via the LFT, regardless on variation of the mains voltage and the dc bus load. The instantaneous and average boost voltage is

$$v_0(t) = v_{BUS} - v_{REC}(t), \tag{8.5}$$

$$v_{0(AV)} = v_{BUS} - V_{PEAK}\frac{3}{\pi} \ge V_{PEAK}\frac{\pi - 3}{\pi}. \tag{8.6}$$

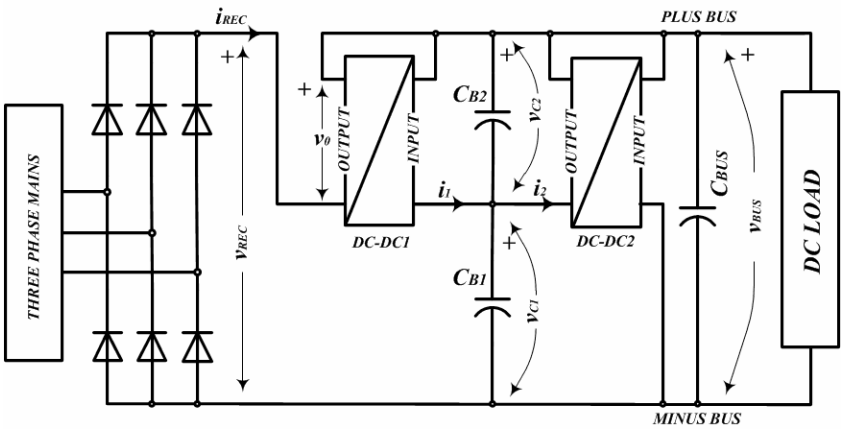
8.1.1. The LFT Realization

Some possible realizations of the LFT are illustrated in Fig. 8.2. The LFT consists of two uni-directional dc-dc converters, namely DC-DC1 and DC-DC2, and two series connected capacitors C_{B1} and C_{B2}. Output of the converter DC-DC1 is connected between the rectifier and dc bus plus rail, while the input is connected in parallel with the capacitor C_{B2}. The average power of the converter DC-DC1 is not zero ($v_{0(AV)}i_{REC} \neq 0$). Therefore, the current i_1, which flows into the capacitors mid point, is not zero. Since the capacitors average current must be zero in steady state, one additional converter must be connected on the capacitors mid point in order to compensate the current i_1. The converter DC-DC2 could be connected in three different ways.

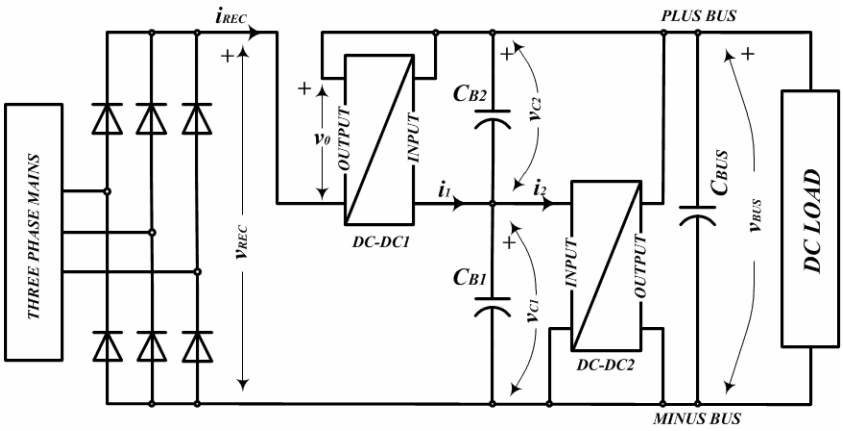
The case A: The DC-DC2 output is parallel connected with the capacitor C_{B2}, while the input is connected in parallel with the dc bus (Fig. 8.2 (a)).

The case B: The DC-DC2 output is connected on the dc bus, while the input is connected in parallel with the capacitor C_{B1} (Fig. 8.2 (b)).

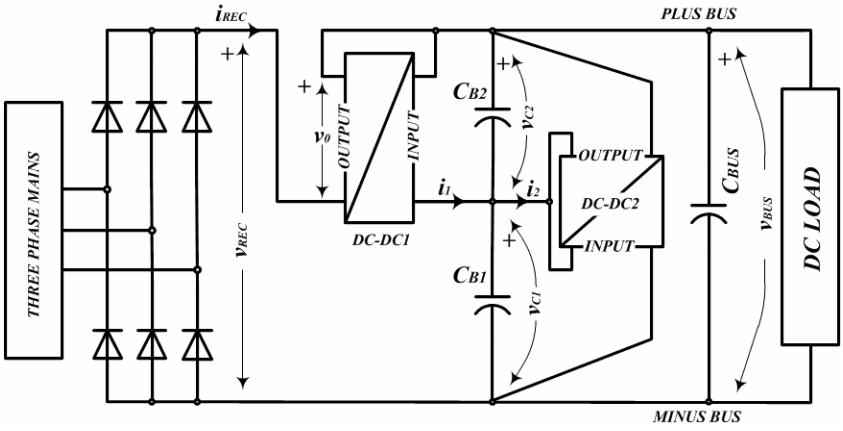
The case C: The DC-DC2 output is connected in parallel with C_{B2}, while the input is connected in parallel with C_{B1} (Fig. 8.2 (c)).



(a)



(b)



(c)

Fig. 8.2 Realization of the LFT with two dc-dc converters. a) DC-DC2 is connected on top capacitor C_{B2} and the dc bus, b) DC-DC2 is connected on bottom capacitor C_{B1} and the dc bus, and c) DC-DC2 is connected on C_{B1} and C_{B2}.

8. HYBRID HALF DC BUS VOLTAGE RATED BOOST RECTIFIER

The best of the three possible topologies depends on the power rating of the DC-DC2 converter. To examine this, let us compute power rating of DC-DC2 converter for all the three cases.

The average currents i_1 and i_2 are computed from the power balance as

$$i_{1(AV)} = i_{2(AV)} = \frac{P_{LOAD}}{k_{C2} v_{BUS}} \left(k_{BOOST} \frac{\pi}{3} - 1 \right), \tag{8.7}$$

where the top capacitor voltage is $v_{C2} = k_{C2} v_{BUS}$. The dc bus voltage boosting factor k_{BOOST} is defined as

$$k_{BOOST} = \frac{v_{BUS}}{V_{PEAK}} \geq 1. \tag{8.8}$$

From (8.7) and Fig. 8.2 one can find power rating of the DC-DC2 converter.

The case *A*:

$$P_{2A} = i_{2(AV)} v_{C2} = P_{LOAD} \left(k_{BOOST} \frac{\pi}{3} - 1 \right). \tag{8.9}$$

The case *B*:

$$P_{2B} = i_{2(AV)} v_{C1} = \frac{1 - k_{C2}}{k_{C2}} P_{LOAD} \left(k_{BOOST} \frac{\pi}{3} - 1 \right). \tag{8.10}$$

The case *C*:

$$P_{2C} = i_{2(AV)} (1 - k_{C2}) v_{C2} = (1 - k_{C2}) P_{LOAD} \left(k_{BOOST} \frac{\pi}{3} - 1 \right). \tag{8.11}$$

The converter relative power rating versus the voltage v_{C2} is plotted in Fig. 8.3.

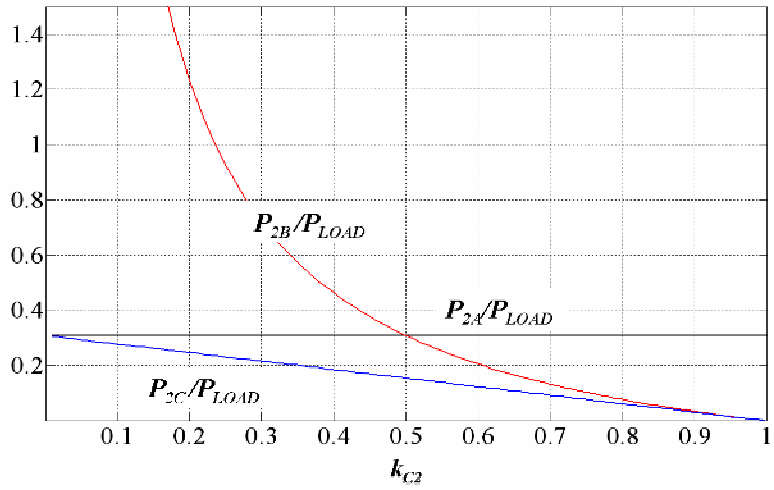
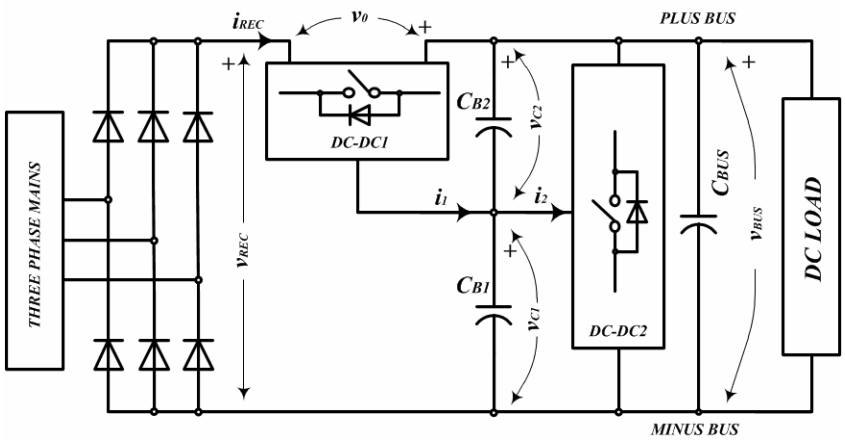


Fig. 8.3 Relative power of the converter DC-DC2 versus voltage v_{C2}. P_{2A} if case A, P_{2B} if case B, and P_{2C} if case C. The coefficient $k_{C2} = \frac{v_{C2}}{v_{BUS}}$ is the voltage v_{C2} normalized on the dc bus voltage v_{BUS}.

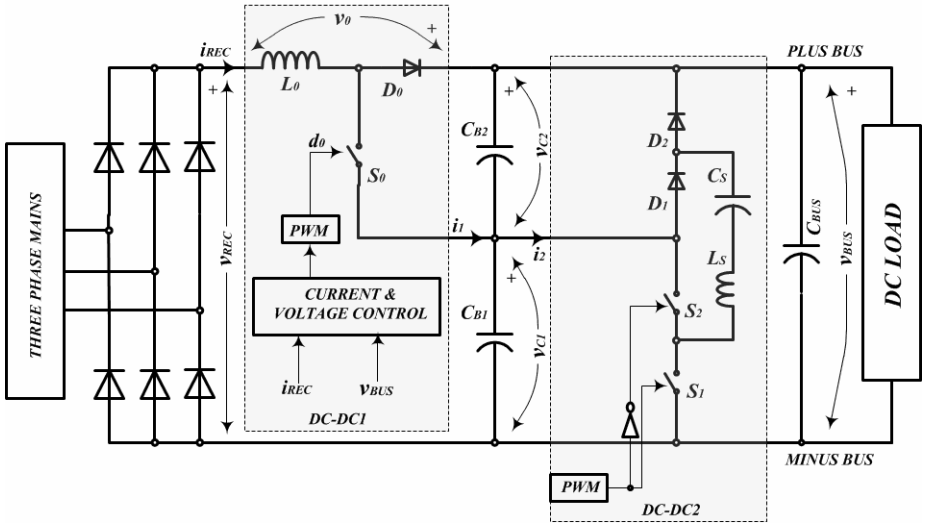
One can see from the graph, Fig. 8.3, that the power rating of the converter of case A (Fig. 8.2 (a)) is constant. In contrast to this, the power rating of the converter in case B and C (Fig. 8.2 (b) and (c)) strongly depends on the voltage v_{C2}. From the graph, one can conclude that the topology C requires minimum power rating of the DC-DC2 converter.

A particular case that is considered in the dissertation is $v_{C2}=v_{C1}=v_{BUS}/2$ (the DC-DC2 is connected as in case C). Because some of the terminals of the DC-DC1 and DC-DC2 converters are connected together, the circuit of Fig. 8.2 (c) could be further simplified as given in Fig. 8.4 (a).

Detailed circuit diagram is depicted in Fig. 8.4 (b). The DC-DC1 converter is a converter connected in three points; plus rail of the input rectifier, plus rail of the dc bus and mid point of the capacitors C_{B1} and C_{B2}. The DC-DC2 converter is a switched capacitor converter that is connected between mid point of the capacitors C_{B1} and C_{B2} and plus/minus dc bus. Detailed analysis of these two converters is given in sections 8.2 and 8.3.



(a)



(b)

Fig. 8.4 Realization of the LFT using two three-points connected dc-dc converters, and b) some details of a possible realization.

8.1.2. The Mains Current Quality

The mains current quality has become an important issue recently with broad application of nonlinear loads such as diode bridge passive rectifiers. Such loads generate higher harmonics in the mains current, which cause additional heating of the distribution transformers, capacitor banks and neutral line of the low voltage distribution network. Moreover, the higher harmonics generates electromagnetic interference (EMI) with analog communication equipment.

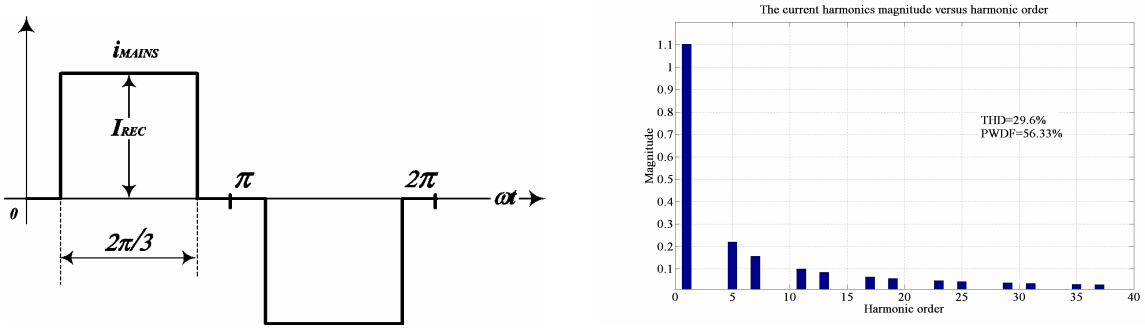
Based on the international IEC standard [13], total harmonic distortion factor (THD) and partially weighed harmonic distortion factor (PWHD) are defined as

$$THD = \frac{\sqrt{\sum_{k=2}^{40} I_k^2}}{I_1}, \tag{8.12}$$

$$PWHD = \frac{\sqrt{\sum_{k=14}^{40} kI_k^2}}{I_1}. \tag{8.13}$$

Please notice that harmonics up to 40th order are taken into account in the THD and PWHD definition [13]. In the near future, it is expected that the standards will be modified and higher order harmonics (above 40th) will be taken into account.

In this dissertation, an intermediate solution is discussed. The mains current is square-waveform with certain level of higher harmonics. An ideal waveform is depicted in Fig. 8.5 (a), while the current spectrum is depicted in Fig. 8.5 (b). The THD and PWHD factors are indicated in Fig. 8.5 (b).



(a) (b)

Fig. 8.5 a) Ideal waveform of the mains current, and b) amplitude spectra up to 40th harmonic. The THD and PWHD factor are computed from definitions (8.12) and (8.13).

TABLE 8-1 shows the current emission limits applicable on three-phase variable speed drives. In most industrial applications, the short circuit coefficient I_{SC}/I_N is greater than 300. In this case, the square waveform current satisfies THD limit but not PWHD limit. Further improvement of the current shape regarding the PWHD factor is possible.

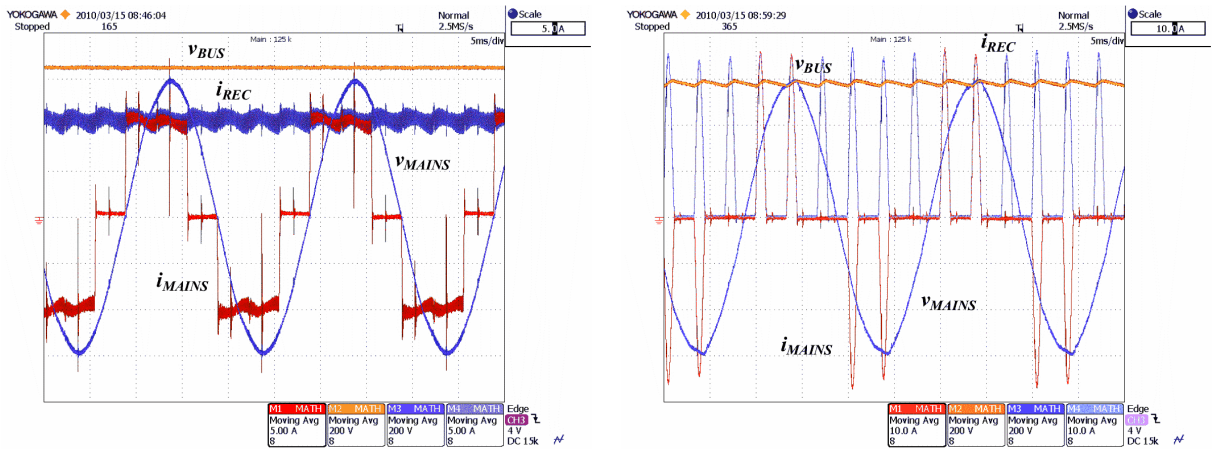
Fig. 8.6 (a) shows some experimental waveforms that illustrate the functionality of the proposed boost rectifier. Waveform of the mains phase-to-phase voltage v_{MAINS}, current i_{MAINS} and the dc bus voltage v_{BUS} are given. The current is a square-waveform, as expected from theoretical analysis. The dc bus voltage is constant, ripple-free and boosted above the mains

phase-to-phase peak voltage. The same waveforms of an ordinary diode rectifier are depicted in Fig. 8.6 (b). The waveforms were recorded at the same conditions: the load and the mains voltage. The mains current peak and RMS value are 35A and 12.5A respectively in comparison to 10A and 8A in case of the proposed boost rectifier. Fig. 8.7 shows the mains current amplitude spectra. Fig. 8.7 (a) shows spectra in full frequency range, from 2 kHz up to 150 kHz, while Fig. 8.7 (b) shows spectra up to 40th harmonic.

TABLE 8-1: Current emission limits for balanced three-phase equipment, based on the IEC 61000-3-12 standard [13].

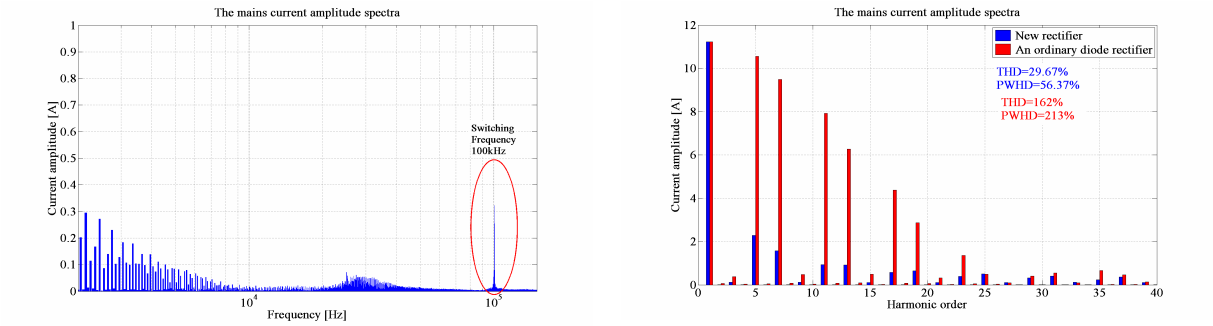
Short circuit ratio $\frac{I_{SC}}{I_N}$	Admissible individual current harmonics I_n/I_1 [%]				Admissible harmonic distortion factors	
	I_5	I_7	I_{11}	I_{13}	THD	PWHD
33	10.7	7.2	3.1	2	13	22
66	14	9	5	3	16	25
120	19	12	7	4	22	28
250	31	20	12	7	37	38
≥350	40	25	15	10	48	46
The relative values of even harmonics up to 12 shall not exceed 16/n %. Even harmonics above order 12 are taken into account in THD and PWHD in the same way as odd order harmonics.						

I_{SC} and I_N are the network short circuit current and the equipment nominal phase current.



(a) (b)

Fig. 8.6 Experimental waveforms the mains current i_{MAINS} [5A/div] and voltage v_{MAINS} [200V/div] and the dc bus voltage v_{BUS} [200V/div]. a) Rectifier with proposed half-dc-bus-voltage rated topology. b) An ordinary diode rectifier with capacitive filter. V_{MAINS}=400V, V_{BUS}=650V, P_{LOAD}=5.5kW.



(a) (b)

Fig. 8.7 The mains current amplitude spectra. a) From 2kHz up to 150kHz, and b) up to 40th harmonic. The THD and PWHD factor are computed from definitions (8.12) and (8.13). The bars in red: spectra of a standard diode rectifier current, and bars in blue: spectra of the boost rectifier current.

8.2. The DC-DC1 Converter

In this section, the DC-DC1 converter is analyzed and some design guidelines are given.

A circuit diagram of the DC-DC1 converter is depicted in Fig. 8.8. The input rectifier, DC-DC2 converter and the dc bus load are not detailed, just indicated as gray shaded boxes. Equivalent circuit diagram and waveforms (the inductor current i_{REC} and voltage v_{L0}) are given in Fig. 8.9. The input rectifier is represented by a voltage source v_{REC}. The capacitors C_{B1} and C_{B2} are modeled as a voltage sources v_{C1} and v_{C2} that are assumed to be constant. Let Since the capacitors could be large enough to behave as constant voltage sources over a short period (order of switching period). However, on long term, the voltage v_{C1} has tendency to increase and v_{C2} has tendency to decrease because the mid point current i_1 is non-zero positive current. To keep those voltages in a constant ratio, an auxiliary converter DC-DC2 is used. Selecting a proper topology, it would be possible to maintain the voltages v_{C1} and v_{C2} in constant ratio regardless on the current i_1. In this analysis, a particular case, $v_{C1}=v_{BUS}/2$ is considered.

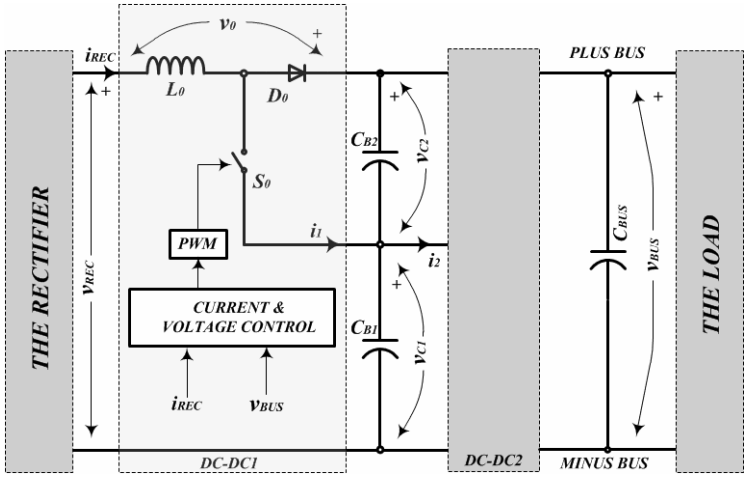
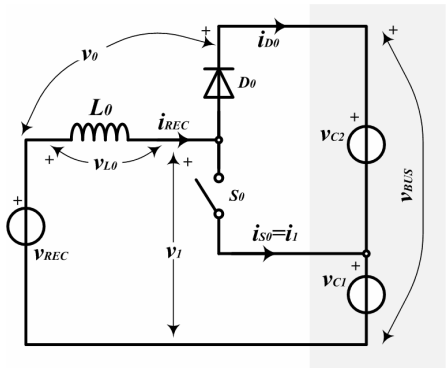


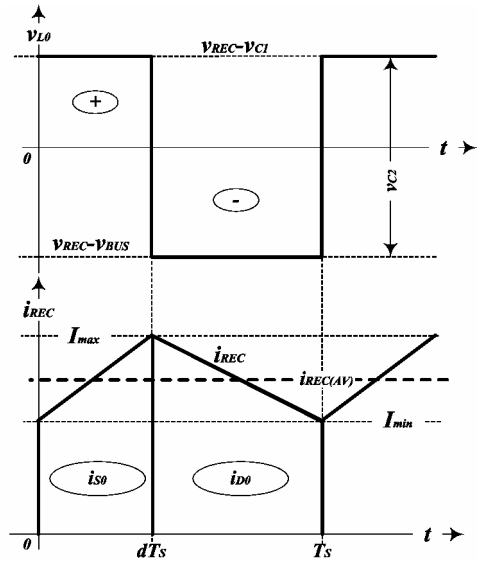
Fig. 8.8 Circuit diagram of the DC-DC1 converter.

8.2.1. Analysis

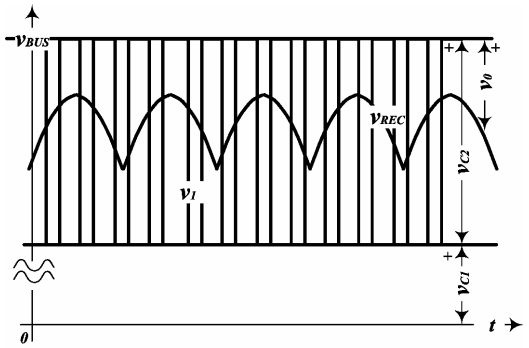
The converter basically operates in the same way as the ordinary boost converter: the switch S_0 conducts during period dT_S and the inductor current i_{REC} increases. The boost diode D_0 conducts during the complementary period $(1\text{-}d)T_S$ and the inductor current decreases and charges the dc bus capacitor C_{BUS}. The difference between the ordinary boost converter and the proposed one is that the switch S_0 is connected to the mid point of the capacitors C_{B1} and C_{B2}. That means the inductor voltage swing is the voltage $v_{C2}=v_{BUS}/2$.



(a)



(b)



(c)

Fig. 8.9 a) The equivalent circuit of the DC-DC1 converter. b) Waveforms of the inductor voltage v_{L0}, and the current i_{L0}, and c) the voltages v_{REC}, v_1, v_{BUS}, v_0, v_{C1} and v_{C2}.

8. HYBRID HALF DC BUS VOLTAGE RATED BOOST RECTIFIER

In the standard single-switch boost topology, the switch is connected to the minus dc bus and therefore the inductor voltage swing is the full dc bus voltage v_{BUS}. This has direct influence on the inductor size, losses and electromagnetic interference (EMI) [117]-[118].

The circuit of Fig. 8.9 (a) is described by equation

$$L_0 \frac{di_{REC}}{dt} = \begin{cases} v_{REC} - v_{C1} & 0 < t \le dT_S \\ v_{REC} - v_{BUS} & dT_S < t \le T_S \end{cases}, \tag{8.14}$$

where T_S is the switching period and d is the duty cycle. From (8.14) and the volt-second balance it follows that duty cycle d is

$$d = \frac{v_{BUS} - v_{REC}}{v_{BUS} - v_{C1}} = 2\frac{v_{BUS} - v_{REC}}{v_{BUS}}, \tag{8.15}$$

where $v_{C1}=v_{BUS}/2$. Substituting (8.2) into (8.15) yields duty cycle

$$d(t) = 2\left(1 - \frac{\sin \omega_m t}{k_{BOOST}}\right)\Bigg|_{60° < \omega_m t \le 120°}. \tag{8.16}$$

Fig. 8.10 shows 3-D graph of the duty cycle (8.16) versus the boost factor and angle ωt.

Maximum boost factor and the dc bus voltage are computed from (8.16) and the condition that the duty cycle is maximum ($d_{max}=1$) at minimum of the rectifier voltage.

$$\begin{aligned} k_{BOOST(\max)} &= \frac{2\sin \omega_m t}{2-d}\Bigg|_{\substack{d=1 \\ \omega_m t = n\pi/3}} = \sqrt{3} \\ V_{BUS(\max)} &= \sqrt{3} V_{PEAK} \end{aligned} \tag{8.17}$$

The boost factor (and therefore the dc bus voltage) of the proposed hybrid boost converter is limited, in contrast to the ordinary boost converter that has theoretically unlimited boost factor (in reality limited by the circuit parasitic resistance). In most of the applications, the boost factor is often lower than 1.5, and therefore the limitation (8.17) is not relevant.

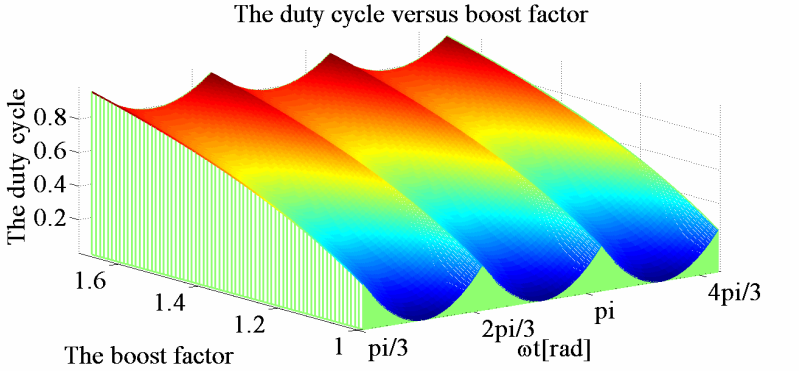
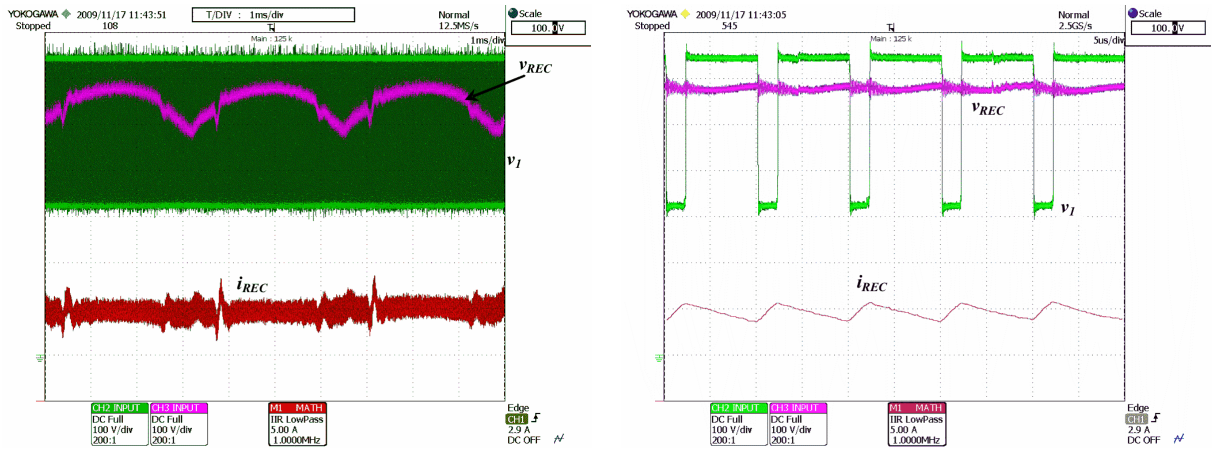


Fig. 8.10 Duty cycle d versus the boost factor k_{BOOST} and angle ω is the mains angular frequency.

Fig. 8.11 (a) illustrates the functionality of the DC-DC1 converter. Experimental waveforms of the rectifier voltage v_{REC}, rectifier current i_{REC} and the voltage v_1 are shown. The voltage v_1 is the voltage between the inductor and minus dc bus (see Fig. 8.11 (a)). Fig.

8.11 (b) shows a zoom of the waveforms. Please notice notches in the rectifier voltage waveform and corresponding distortion in the rectifier current waveform, which are caused by the mains background voltage distortion.



(a) (b)

Fig. 8.11 a) Experimental waveforms the rectifier current i_{REC} [5A/div] and voltage v_{REC} [100V/div] and the switching voltage v_1 [100/div]. b) Zoom at maximum rectifier voltage. V_{MAINS}=400V, V_{BUS}=650V, P_{LOAD}=5500W.

8.2.2. Design Aspects

In this section, some aspects of design of the boost inductor L_0, the dc bus capacitor C_{BUS} and boost switch S_0 and diode D_0 are discussed and design guidelines are given.

8.2.2.1. Boost Inductor L_0

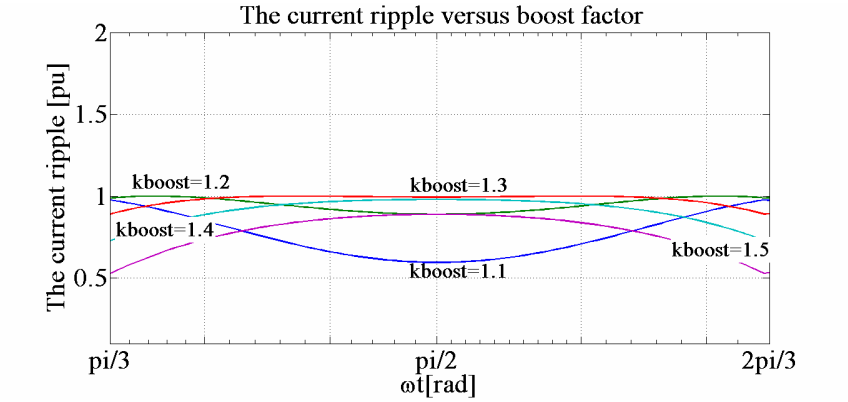
Design of the boost inductor is one of the most important design steps in a boost converter design. The design is based on two criteria: the inductance (for allowed current ripple Δi_{REC}) and the inductor losses. The current ripple has significant influence on the total losses and the inductor thermal design. For generality of the analysis, it is assumed that the maximum current ripple is given as a design parameter. The boost inductor losses are computed, however the thermal design is not discussed in detail.

- **The Inductance and Current Ripple**

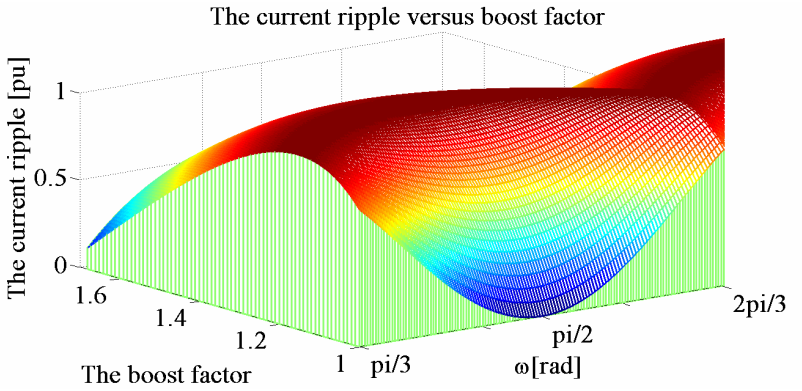
The inductor current ripple is computed from (8.14) and volt-second balance as

$$\Delta i_{REC} = \frac{v_{BUS}}{2L_0 f_{SW}}\left(d - d^2\right), \tag{8.18}$$

where f_{SW} is the switching frequency. Fig. 8.12 shows the current ripple versus boost factor and angle ωt.



(a)



(b)

Fig. 8.12 The rectifier current ripple versus the boost factor k_{BOOST} and angle ωt, where ω is the mains angular frequency. The ripple is normalized on the maximum current ripple achieved at d=0.5.

Substituting (8.16) into (8.18) one can find the maximum current ripple

$$\Delta i_{\max} = \begin{cases} \dfrac{v_{BUS}}{2L_0 f_{SW}} \left(-2 + 3\dfrac{\sqrt{3}}{k_{BOOST}} - \dfrac{3}{k_{BOOST}^2} \right) \Bigg|_{k_{BOOST} \le \frac{2}{\sqrt{3}}} \\ \dfrac{v_{BUS}}{8L_0 f_{SW}} \Bigg|_{k_{BOOST} > \frac{2}{\sqrt{3}}} \end{cases}. \tag{8.19}$$

The boost inductance is computed for the worst case of (8.19) and the maximum current ripple Δi_{max}

$$L_0 \ge \frac{v_{BUS\max}}{8\Delta i_{\max} f_{SW}}. \tag{8.20}$$

o The Inductor Losses

The inductor losses consist of the winding losses and the core losses.

$$P_{L0} = \sum_{n=0}^{n} I_{L0RMS(n)}^2 \left(R_{L0(nf_{SW})} + R_{C(nf_{SW})} \right), \tag{8.21}$$

where $R_{L0(fsw)}$ is the inductor winding resistance that dependents on the frequency. The resistance $R_{C(fsw)}$ is the core equivalent resistance that models the core losses [92]. The losses model (8.21) takes into account harmonics of the inductor current. To simplify computation, the current ripple can be substituted by an equivalent sinusoidal current having the same RMS value and frequency as the total current ripple. As can be seen from (8.18), the ripple current is time varying because duty cycle varies with the instantaneous rectifier voltage (8.2). Hence, the ripple RMS current varies too. It could be considered as local RMS current.

$$\Delta i_{REC(RMS)}(t) = \frac{\Delta i_{REC}(t)}{2\sqrt{3}} \tag{8.22}$$

Substituting (8.22) into (8.21) yields local average losses of the inductor

$$P_{L0}(t) = \underbrace{R_{L0(DC)}\left(\frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \frac{\pi}{3}\right)^2}_{LOW\ \ FREQUENCY\ LOSSES} + \underbrace{\left(R_{L0}(_{fSW}) + R_{C}(_{fSW})\right)\frac{\Delta i_{REC}^2(t)}{12}}_{HIGH\ \ FREQUENCY\ LOSSES}, \tag{8.23}$$

where $R_{L0(DC)}$ is the inductor winding resistance at low frequency.

Substituting (8.18) into (8.23) one can compute the inductor average losses, (8.24). Here, we have to highlight that the losses model (8.24) is not very accurate, but sufficient as an initial step in the inductor design procedure.

$$\begin{aligned} P_{L0(AV)} &= \frac{6}{T_m}\int_0^{6/T_m} P_{L0}(t)dt = \underbrace{R_{L0(DC)}\left(\frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \frac{\pi}{3}\right)^2}_{LOW\ \ FREQUENCY\ LOSSES} \\ &+ \underbrace{\left\{\begin{array}{l} \left(R_{L0}(_{fSW}) + R_{C}(_{fSW})\right)\Delta i_{\max}^2 \dfrac{16}{\pi} \\ \times \dfrac{\left(4\pi k_{BOOST}^4 - 72k_{BOOST}^3 + \left(39\sqrt{3}+26\pi\right)k_{BOOST}^2 - 132k_{BOOST} + 6\pi + 27\dfrac{\sqrt{3}}{2}\right)}{k_{BOOST}^4} \end{array}\right\}}_{HIGH\ \ FREQUENCY\ LOSSES} \end{aligned} \tag{8.24}$$

8.2.2.2. The DC Bus Circuit

The dc bus capacitor is designed with the dc bus voltage ripple as the design criterion. The dc bus voltage ripple at low frequency is computed from the instantaneous power balance equation

$$v_{REC} i_{REC} = P_{LOAD} + v_{BUS} i_{CBUS}, \tag{8.25}$$

where i_{CBUS} is the dc bus capacitor current. In (8.25), it has been assumed that instantaneous power of the capacitors C_{B1}, C_{B2} and C_S, and inductors L_0 and L_S could be neglected in comparison to the dc bus capacitor. The rectifier current is assumed as constant (actively controlled by the DC-DC1 converter).

The rectifier voltage (8.2) can be expanded in Fourier series

$$v_{REC}(t) = V_{PEAK}\frac{3}{\pi} + V_{PEAK}\frac{3}{\pi}\sum_{n=1}^{\infty}\frac{2}{(6n)^2 - 1}\sin\left(6n\omega_m t + \varphi_{(n)}\right). \tag{8.26}$$

From (8.25) and (8.26) it follows that

$$i_{CBUS}(t)=\frac{P_{LOAD}}{v_{BUS(AV)}}\sum_{n=1}^{\infty}\frac{2}{(6n)^2-1}\sin\left(6n\omega_m t+\varphi_{(n)}\right)\cong\frac{P_{LOAD}}{v_{BUS(AV)}}\frac{2}{35}\sin 6\omega_m t\,. \tag{8.27}$$

Here, it has been assumed that 6th harmonic of the instantaneous power (8.25) is dominant, and the dc bus voltage ripple is significantly lower than the average dc bus voltage, $\Delta v_{BUS} << v_{BUS(AV)}$. Thus, the peak-to-peak voltage ripple can be computed as

$$\Delta v_{BUS}\cong\frac{2}{35}\frac{2P_{LOAD}}{v_{BUS(AV)}(6\omega_m C_{BUS})}\,. \tag{8.28}$$

From (8.28) it follows that the dc bus capacitance is

$$C_{BUS}\geq\frac{2}{35}\frac{2P_{LOAD}}{v_{BUS(AV)}\Delta v_{BUS\max}6\omega_m}\,, \tag{8.29}$$

where $\Delta v_{BUS\max}$ is maximum dc bus voltage ripple given as a design parameter.

8.2.2.3. The Switch and Boost Diode

Three parameters are important for design and selection of the boost switch and diode:

1. The device voltage stress,
2. The device current stress, and
3. The device losses and associated thermal stress.

The device voltage rating, current stress and losses will be analyzed. Thermal aspects however will not be discussed because that is an issue well known and presented in literature, [119].

- **The Device Voltage Rating**

The device transient voltage defines the switch and diode voltage rating

$$V_{S0(\max)}=V_{D0(\max)}=\frac{v_{BUS(\max)}}{2}+\Delta V\,, \tag{8.30}$$

where ΔV is commutation over-voltage

$$\Delta V=L_c\frac{di_{S0}}{dt}\cong L_c\frac{0.8I_{S0}}{t_F}\,. \tag{8.31}$$

L_c is the commutation inductance [100], I_{S0} is the switch peak current and t_F is the current fall time. Notice that the voltage rating is one half of the dc bus voltage in contrast to the ordinary boost converter.

- **Current Stress and Losses**

The switch average and RMS current are

$$I_{S0(AV)} = \frac{3}{\pi}\int_{\pi/3}^{2\pi/3} i_{S0}\, d(\omega t) = \frac{P_{LOAD}}{v_{BUS}} 2\left(\frac{\pi}{3} k_{BOOST} - 1\right),$$
$$I_{S0(RMS)} = \sqrt{\frac{3}{\pi}\int_{\pi/3}^{2\pi/3} i_{S0}^2\, d(\omega t)} = \frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \frac{\pi}{3}\sqrt{2\left(1 - \frac{3}{\pi k_{BOOST}}\right)}. \quad (8.32)$$

The switch losses are computed from the switch model (chapter 5) and (8.32)

$$P_{S0} = \underbrace{V_{S0} I_{S0(AV)} + r_{S0} I_{S0(RMS)}^2}_{CONDUCTION\ LOSSES} + \underbrace{\frac{P_{LOAD} k_{BOOST}}{2 V_N I_N}\left(E_{ON} + E_{OFF}\right) f_{SW}}_{SWITCHING\ LOSSES}, \quad (8.33)$$

where f_{SW} is switching frequency. The switch S_0 is approximated by threshold voltage V_{S0} and dynamic resistance r_{S0}. E_{ON} and E_{OFF} are switching energy at the given conditions; rated voltage V_N and current I_N.

Similar calculation is applied on the boost diode D_0. Average and RMS currents and losses are

$$I_{D0(AV)} = \frac{P_{LOAD}}{v_{BUS}}\left(2 - \frac{\pi}{3} k_{BOOST}\right),$$
$$I_{D0(RMS)} = \frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \frac{\pi}{3}\sqrt{\frac{6}{\pi k_{BOOST}} - 1}, \quad (8.34)$$

$$P_{D0} = \underbrace{V_{DF0} I_{D0(AV)} + r_{D0} I_{D0(RMS)}^2}_{CONDUCTION} + \underbrace{\frac{P_{LOAD} k_{BOOST}}{2 V_N I_N} E_Q f_{SW}}_{SWITCHING}, \quad (8.35)$$

where the diode is approximated by threshold voltage V_{DF0} and dynamic resistance r_{D0}. E_Q is reverse recovery energy at given the conditions; rated voltage V_N and current I_N.

8.3. The DC-DC2 Converter

As already mentioned in section 8.1, the role of the DC-DC2 converter is to balance the voltages v_{C1} and v_{C2}. The circuit diagram of the proposed converter is given in Fig. 8.13. Basically, the converter is a variant of a switched capacitor converter [118]. A switch leg S_1 S_2 is connected across the bottom capacitor C_{B1}, and a diode leg D_1 D_2 is connected across the top capacitor C_{B2}. The capacitor C_S is the main switched capacitor that transfers the energy, while inductor L_S is an auxiliary inductor used to reduce conduction losses and achieve zero current switching (ZCS) [118]. The switches S_1 S_2 are driven with complementary control signals at period T_{S2}. The duty cycle d_2 is constant, around 50%.

8.3.1. Analysis

For simplicity of the analysis, one can assume that the capacitors C_{B1} and C_{B2} are large enough to maintain the voltages v_{C1} and v_{C2} constant over one switching cycle T_{S2}. Also, the switches and diodes are modeled by constant voltage sources V_{S0} and V_{DF0}. One complete

cycle T_{S2} can be divided into four stages, namely stage A to stage D. Fig. 8.14 illustrates topological stages and waveform of the resonant current i_{R2}.

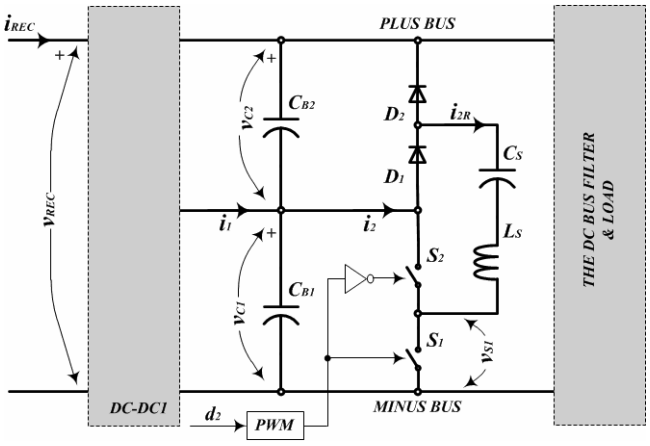


Fig. 8.13 DC-DC2 converter circuit diagram.

Stage A: Switch S_1 is closed at the instant $t=0$. The capacitor C_S is charged from v_{C1} via the switch S_1 diode D_1 and the inductor L_S. The current i_{2R} and voltage v_{CS} increase. Once reaches the maximum, the current starts decreasing towards zero (L_SC_S resonant circuit).

Stage B: The current i_{2R} reaches zero and diode D_1 is blocked at the instant $t=T_0/2$. The current remains zero until commutation of the switch S_2.

Stage C: The switch S_2 is closed at the instant $t=T_{S2}/2$. The capacitor C_S is discharged (into v_{C2}) via the switch S_2, diode D_2 and the inductor L_S. The current i_{2R} increases in negative direction with respect to the direction in Fig. 7 The voltage v_{CS} decreases. After reaching the maximum, the current starts decreasing towards zero (L_SC_S resonant circuit).

Stage D: The current i_{2R} reaches zero and diode D_2 is blocked at the instant $t=T_{S2}/2+T_0/2$. The current remains zero until the commutation of the switch S_1 at the moment $t=T_{S2}$. One switching cycle is finished.

Neglecting the circuit resistance, the current i_{2R} can be described by fractions of sinusoidal function,

$$i_{2R}(t)=\begin{cases}(-1)^k i_2 \dfrac{\pi}{2}\dfrac{T_{S2}}{T_0}\sin\omega_0\left(t-k\dfrac{T_{S2}}{2}\right) & k\dfrac{T_{S2}}{2}<t\le k\dfrac{T_{S2}}{2}+\dfrac{T_0}{2} \\ 0 & k\dfrac{T_{S2}}{2}+\dfrac{T_0}{2}<t\le (k+1)\dfrac{T_{S2}}{2}\end{cases}, \tag{8.36}$$

where the circuit natural frequency is

$$\omega_0=\frac{2\pi}{T_0}=\frac{1}{\sqrt{L_SC_S}}, \tag{8.37}$$

and k is a floor integer defined as $k=INT(\dfrac{2t}{T_S})$.

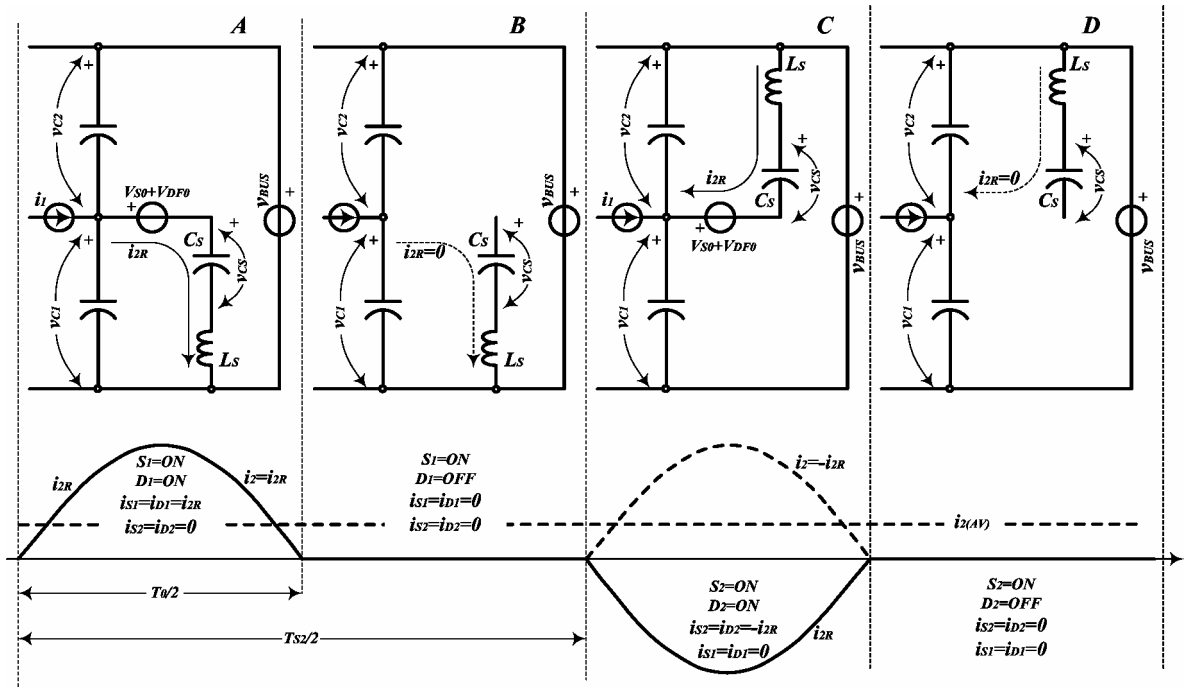


Fig. 8.14 Different topological stages of the converter. A) S1, D1 are conducting, B) S1 is conducting D1 is blocking, C) S2, D2 are conducting, and D) S2 is conducting D2 is blocking.

The current i_1 is the current of the switch S_0 (the converter DC-DC1), and is a purely discontinuous current. However, because of presence of the capacitors C_{B1} and C_{B2} that are assumed sufficiently large, the current i_1 can be considered as a constant current $i_{1(AV)}$. In steady state, the capacitors voltages are constant. As the capacitors are large, but not infinite capacitance, it follows that the capacitors current over a certain period must be zero. Hence, $i_{2(AV)}=i_{1(AV)}$. From (8.4) and (8.16) it follows that

$$i_{2(AV)}(t)=i_{REC}d(t)=\frac{P_{LOAD}}{v_{BUS}}\frac{\pi}{3}2\left(k_{BOOST}-\sin\omega_m t\right)\Big|_{\pi/3<\omega_m t\le 2\pi/3}. \tag{8.38}$$

Please, note that $i_{2(AV)}(t)$ is the current averaged over a switching period T_{S2}. So, it can be considered as the local average current [108]. Also, note from (8.36) and (8.38) that peak of the resonant current i_{2R} changes with the rectifier voltage; the lower rectifier voltage the greater peak current.

8.3.1.1. The Voltage Transfer Ratio

The converter DC-DC2 can be considered as series resonant converter that operates in discontinuous conduction mode (DCM), mode 1 [121]. The input is voltage v_{C1} and output is voltage v_{C2}. The voltage gain of the series resonant converter operating in this mode is unity, regardless on the load and switching frequency.

$$M=\frac{v_{C2}}{v_{C1}-\left(V_{S0}+V_{DF0}\right)}=1, \tag{8.39}$$

where V_{S0} and V_{DF0} are the switch and diode voltage droop.

The bottom and top capacitor voltages are computed from (8.39) as

$$v_{C1} = \frac{v_{BUS} + V_{S0} + V_{DF0}}{2}, \quad v_{C2} = \frac{v_{BUS} - V_{S0} - V_{DF0}}{2}. \tag{8.40}$$

As is it can be seen from (8.40), the ratio of v_{C1} to v_{C2} is constant. That means there is no need for direct measurement and control of the mid point voltage.

Fig. 8.15 illustrates the functionality of the DC-DC2 converter. Waveforms of the rectifier voltage v_{REC} and current i_{REC} and the resonant current i_{2R} are shown. Note that the peak of the current i_{2R} changes as the rectifier voltage changes, as predicted in (8.36) and (8.38). Fig. 8.16 shows a zoomed in disply of these waveforms and voltage v_{S1} of the bottom switch S_1 (circuit in Fig. 8.13); Fig. 8.16 (a) is zoomed at the peak of the rectifier voltage and Fig. 8.16 (b) is zoomed at the minimum rectifier voltage. Note that the switches commutate at the zero current condition.

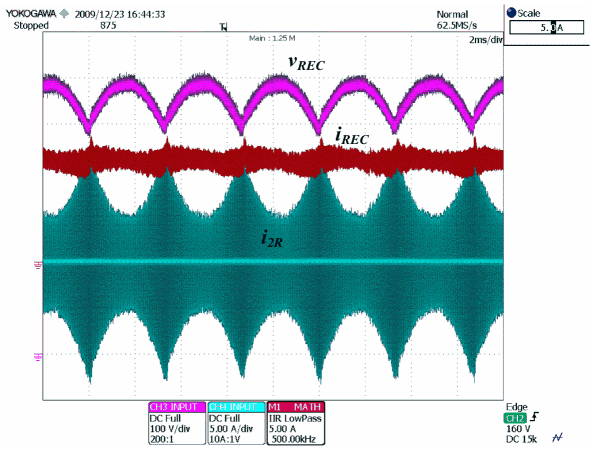
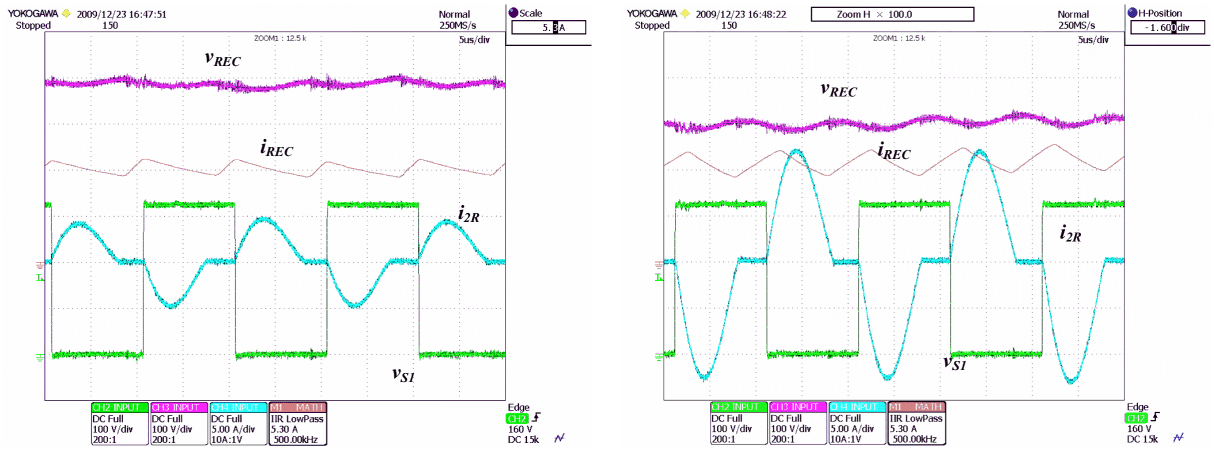


Fig. 8.15 Experimental waveforms of the rectifier current i_{REC} [5A/div], the rectifier voltage v_{REC} [100/div] and resonant circuit current i_{R2} [5A/div]. V_{MAINS}=400V, V_{BUS}=650V, P_{LOAD}=5.5kW.



(a) (b)

Fig. 8.16 Experimental waveforms of the rectifier current i_{REC} [5A/div], the rectifier voltage v_{REC} [100/div] and resonant circuit current i_{R2} [5A/div]. a) Zoom at peak of the rectifier voltage, and b) zoom at minimum rectifier voltage. V_{MAINS}=400V, V_{BUS}=650V, P_{LOAD}=5.5kW.

8.3.2. Design Aspects

8.3.2.1. The Switches and Diodes

The switches and diodes average and RMS current computed over a switching cycle (local averaging [108]) are

$$i_{S(AV)} = \frac{i_{2(AV)}}{2}, \qquad i_{S(RMS)} = i_{2(AV)} \frac{\pi}{2\sqrt{2}} \sqrt{\frac{T_{S2}}{T_0}}. \tag{8.41}$$

The average and RMS current computed over a fundamental period $\frac{\pi}{3}$ are

$$i_{S(AV)} = \frac{P_{LOAD}}{v_{BUS}} \left(\frac{\pi}{3} k_{BOOST} - 1 \right), \qquad i_{S(RMS)} = \frac{P_{LOAD}}{v_{BUS}} \frac{\pi^2}{3} \sqrt{\frac{T_{S2}}{2T_0} \left(k_{BOOST}^{\ 2} + \frac{1}{2} - \frac{12 k_{BOOST} - 3\sqrt{3}}{2\pi} \right)}. \tag{8.42}$$

Now, having average and RMS current, one can compute conduction losses of the switch and diode as

$$P_S = V_S I_{S(AV)} + r_S I_{S(RMS)}^2, \qquad P_D = V_{DF} I_{S(AV)} + r_D I_{S(RMS)}^2. \tag{8.43}$$

The switches and diodes are approximated by constant threshold voltage V_S and V_{DF} and dynamic resistance r_S and r_D. Switching losses are neglected since the switches commute at zero current conditions. If necessary, the losses due to the switch parasitic capacitance can be taken into account.

8.3.2.2. LC Circuit

The resonant circuit RMS current and losses depend on the load power P_{LOAD}, the boosting factor k_{BOOST} and ratio between the switching and resonant frequency,

$$i_{2RMS} = \frac{P_{LOAD}}{v_{BUS}} \frac{\pi^2}{3} \sqrt{\frac{T_{S2}}{T_0} \left(k_{BOOST}^{\ 2} + \frac{1}{2} - \frac{12 k_{BOOST} - 3\sqrt{3}}{2\pi} \right)}. \tag{8.44}$$

The role of the inductor L_S is to minimize the conduction losses and ensure the zero current switching condition. It follows from (8.37), (8.42) and (8.44) that the greater inductance the lower conduction losses. The zero current switching condition is defined as $T_0 \le T_{S2}$. From this condition and (8.37) it follows that

$$L_S C_S \le \left(\frac{T_{S2}}{2\pi} \right)^2. \tag{8.45}$$

The capacitor and inductor have to be selected for minimum size, cost and losses of the *LC* circuit. Total volume of the capacitor and inductor can be expressed in general form

$$W = F_1(C_S) + F_2\left(\frac{\left(\frac{T_{S2}}{2\pi}\right)^2}{C_S}\right), \tag{8.46}$$

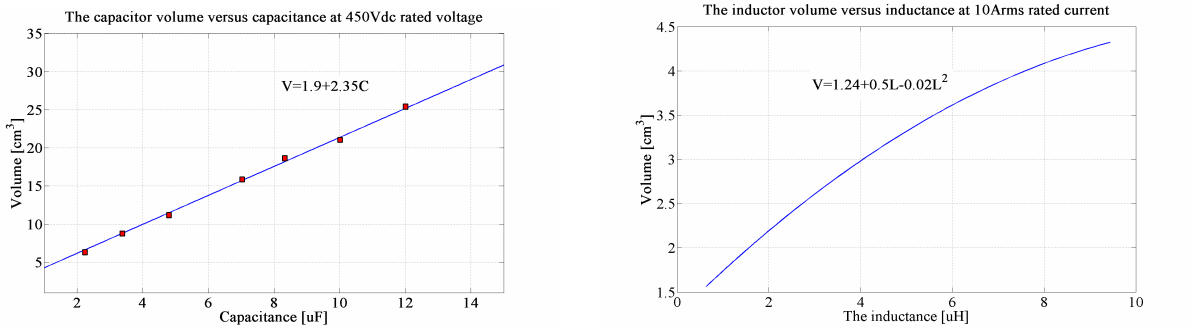
where functions F_1 and F_2 depends on the capacitor and the inductor technology.

The function F_1 has been interpolated for EPCOS film capacitors B32674 at 450Vdc rated voltage [122]. Fig. 8.17 shows the capacitor volume versus capacitance. Red squares are the data sheet values and blue line is first order interpolation,

$$F_1(C_S) = 1.9 + 2.35 \cdot C_S\,[cm^3]. \tag{8.47}$$

Volume of the air-core short inductor [123] can be approximated by a second order function

$$F_2(L_S) = 1.24 + 0.5L_S - 0.02L_S^2\,. \tag{8.48}$$



(a) (b)

Fig. 8.17 a) Volume of MKP Epcos film capacitors B32674 versus capacitances at 450Vdc rated voltage. b) Volume of an air-core inductor versus the inductance at 10Arms rated current.

From (8.47) and (8.48) and the condition

$$\frac{\partial W}{\partial C_S} = \frac{\partial F_1(C_S)}{\partial C_S} + \frac{\partial F_2\left(\frac{\left(\frac{T_{S2}}{2\pi}\right)^2}{C_S}\right)}{\partial C_S} = 0\,, \tag{8.49}$$

the capacitance C_S and inductance L_S can be found that gives minimum volume of the converter. Another parameter that has to be verified is the capacitor RMS current. This is a trivial problem of optimisation and as that it will not be further discussed.

8.4. A Design Example

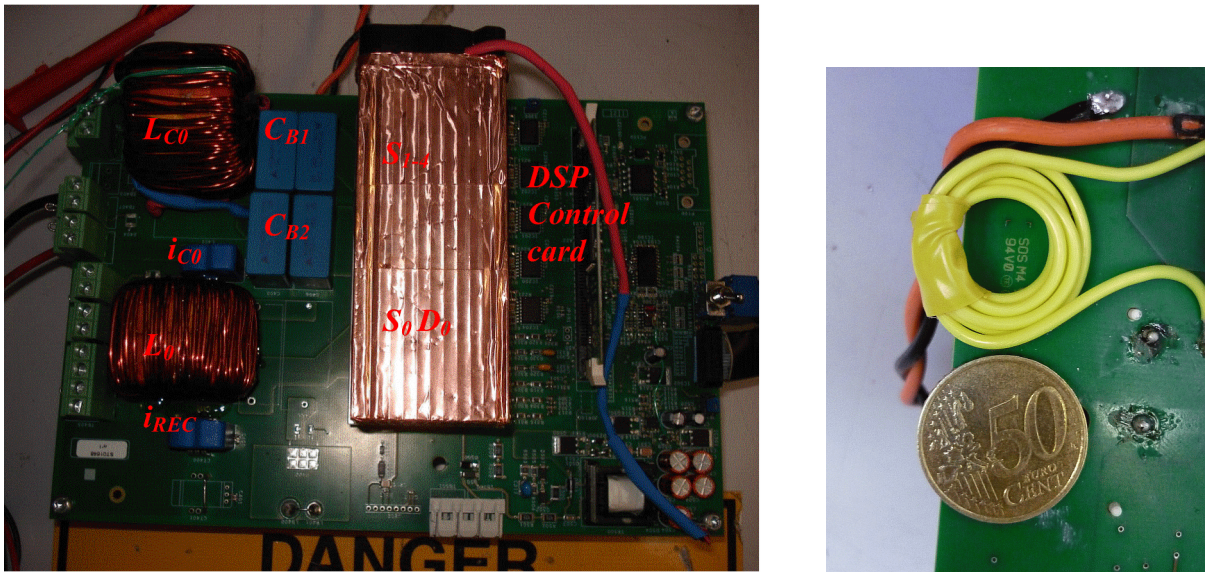
A 5.5 kW prototype was designed and the proposed half-dc-bus-voltage-rated boost rectifier experimentally verified. A picture of the prototype is shown in Fig. 8.18. The converter specification and parameters of the selected main components are given in TABLE 8-2 Active power components (MOSFETs, IGBTs and FWDs) were selected for the target switching frequencies, dc bus voltage, boost factor and rated power. R_{DC} is the winding resistance at low frequency and R_{AC} is the winding resistance at switching frequency [102]. The resistance R_C is the core equivalent resistance as a model of the core losses (8.21). The core resistance was computed at the inductor rated current, using the manufacture datasheet and design software tool [103].

The inductor losses were computed from (8.21) and the parameters in TABLE 8-2. Fig. 8.19 shows 3-D graph of the total inductor loses versus output power and boost factor.

The switch S_0 and diode D_0 losses were computed from (8.33), (8.35) and data given in TABLE 8-2. Fig. 8.20 and Fig. 8.21 show 3-D graph of switching and conduction losses versus conversion power and boost factor. The switch conduction losses strongly depend on the boost factor. They are dominant at full power and high boost factor. In contrast to this, the switch commutation losses are less dependent on the boost factor. The boost diode losses, particularly conduction losses vary significantly with the boost factor.

TABLE 8-2: Specification of the half-dc-bus-voltage rated boost rectifier.

Nominal power			P_{C0}=5500W		
DC bus voltage			V_{BUS}=650V		
Minimum input (line RMS) voltage			V_{mains}=350V		
Switching frequency DC-DC1			f_{SW1}=100kHz		
Switching frequency DC-DC2			f_{SW2}=50kHz		
The current ripple			Δi_{REC}=2.5A		
S_0: MOSFET 500V 20A			D_0: FAST DIODE 500V 20A		
V_{S0}	r_{S0}	$*E_{ON}+E_O$	V_{DF0}	r_{D0}	$*E_Q$
0	200mΩ	10µJ/A	1.13 V	11 mΩ	5µJ/A
*Switching losses at V_N=300V T_J=150˚C					
BOOST INDUCTOR L_0				DC BUS CAPACITOR C_{BUS}	
High Flux Powder Core 58439-A2					
L_0	R_{DC}	R_{AC}	R_C	C	ESR
325µ	40mΩ	0.8Ω	4.4Ω	820µF	0.19 Ω
S_1/S_2 IGBT 600V 10A		D_1/D_2 FAST DIODE 600V 10A		L_S	C_S
				Air core inductor	MKP
V_S	r_S	V_D	r_D		
0.8V	80 mΩ	0.9V	100 mΩ	0.6µH	10µF



(a) (b)

Fig. 8.18 a) Prototype of the boost converter. b) The resonant air-core inductor 0.6µH 10Arms.

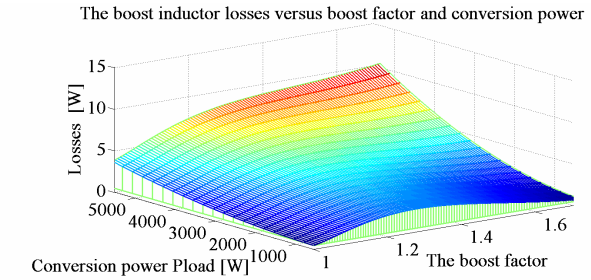
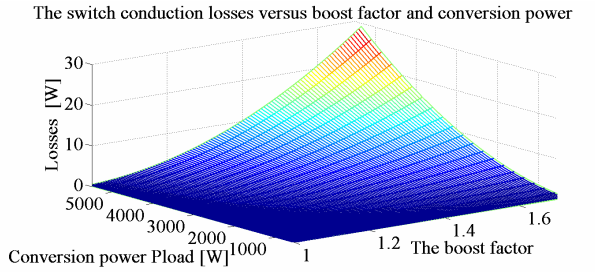
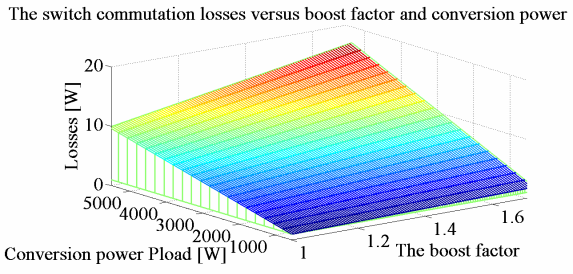


Fig. 8.19 The boost inductor L_0 losses versus the boost factor and conversion power.

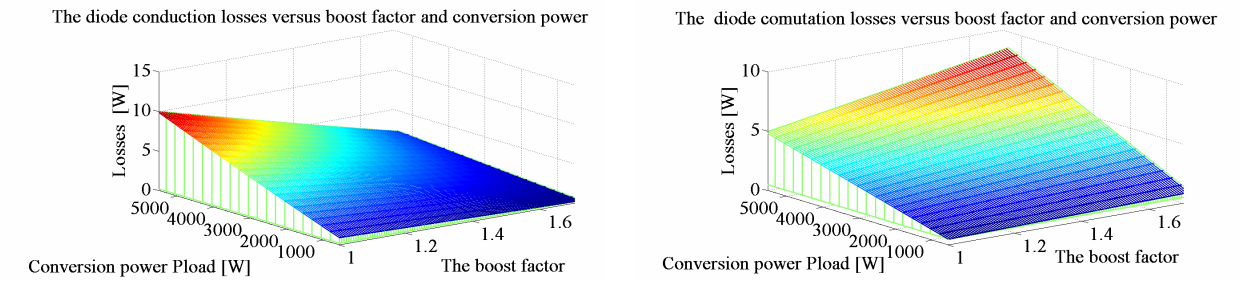


(a)



(b)

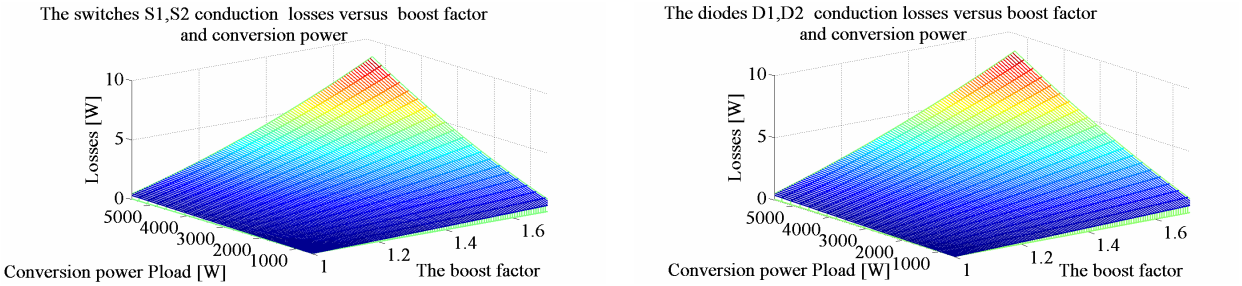
Fig. 8.20 The switch S_0 losses versus the boost factor and conversion power.



(a) (b)

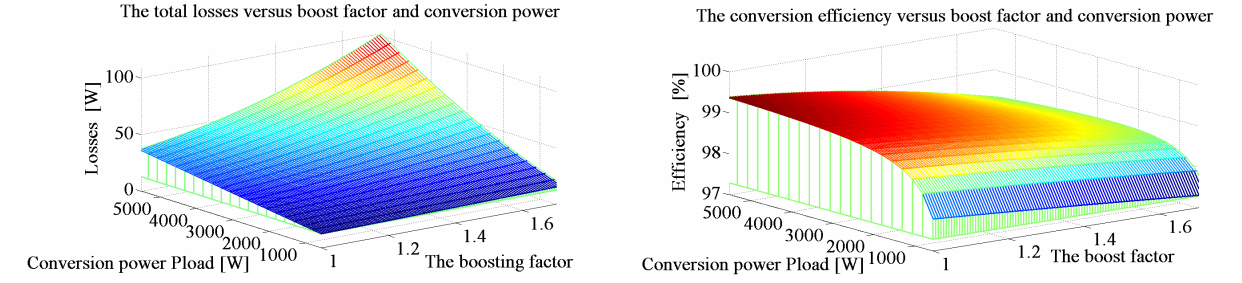
Fig. 8.21 The diode D_0 losses versus the boost factor and conversion power.

The switch $S_{1/2}$ and diode $D_{1/2}$ losses were computed from losses model (8.43) and data in TABLE 8-2. The computed losses versus conversion power and boost factor are illustrated in Fig. 8.22. Fig. 8.23 shows the converter total losses and conversion efficiency versus conversion power and boost factor. The calculation shows that the converter efficiency is quite high, from 97% at minimum output power of 550W and boost factor k_{BOOST}=1.7 up to 99% at maximum output power and minimum boost factor k_{BOOST}=1. In this calculation, losses of the filter capacitors C_{B1} and C_{B2} and resonant capacitor C_S and inductor L_S were neglected. The control circuit and gate drivers' losses were also neglected.



(a) (b)

Fig. 8.22 The switch $S_{1/2}$ and diode $D_{1/2}$ losses versus the boost factor and conversion power. The losses are computed per one device (total losses are twice).



(a) (b)

Fig. 8.23 The conversion total losses and efficiency versus the boost factor and conversion power.

9. MODELING ASPECTS AND CONTROL SCHEME

The model of the half-dc-bus-voltage rated boost rectifier is developed and discussed in this chapter. As mentioned in chapter 8, the half-dc-bus-voltage rated boost rectifier consists of two converters (DC-DC1 and DC-DC2). Model for each converter and then model of the entire rectifier system have to be developed. The model of the DC-DC1 converter is more or less state of the art [106] and therefore it is not discussed in details in this chapter. The model of the DC-DC2 converter is less known in the literature, and is developed and discussed. Finally, a large signal and small signal model of the entire boost rectifier is developed. The model is verified by the Matlab simulations and a set of experiments.

In second part of this chapter, the control scheme is discussed and the controllers' synthesis procedure is given. The proposed control scheme is verified by Matlab/Simulink simulation and a set of experiments. The results are presented and discussed.

9.1. Model of Series Resonant Converter

As discussed in chapter 8, section 8.3, the DC-DC2 converter is the series resonant converter that operates in type 1 discontinuous conduction mode (DCM) [121]. The series resonant converter topology is well-know topology since the age of vacuum tube high frequency generators and SCRs power converters [124]. In the 1980s and 1990s this topology was in focus for high-density dc-dc conversion applications [124]. Two of the most often used methods to model series resonant converter (SRC) are sinusoidal approximation [124]-[127], and discrete time modelling [128], [129]. However, those modelling techniques are not appropriate if the resonant converter operates in continuous conduction mode (CCM) at resonant frequency or in type 1 discontinuous conduction mode (DCM) [121]. The concept of the quantum modelling and control technique introduced in [130] can be used in analysis of type 1 DCM resonant converter.

The circuit diagram is given in Fig. 9.1 (a). The capacitors C_{B1} and C_{B2} are modelled by the ideal voltage sources v_{C1} and v_{C2}. The equivalent circuit diagram is depicted in Fig. 9.1 (b). The model consists of two voltage-controlled voltage sources (v_{C1} and v_{C2}), two current-controlled current sources (i_S and i_D) and an equivalent inductance L_E. The controlled voltage sources are known (v_{C1} and v_{C2}). The controlled current sources and the equivalent inductance L_E have to be determined.

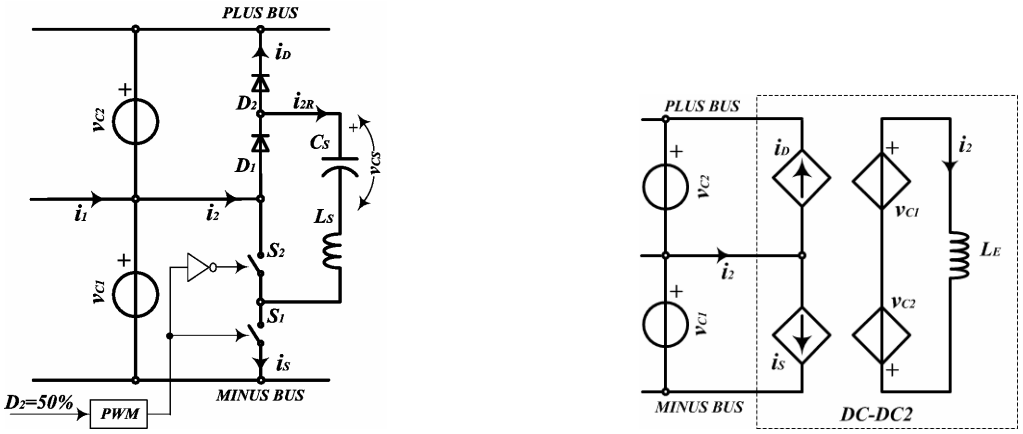
To determine the equivalent inductance L_E, the following virtual experiment is performed. Let us consider steady state and no load condition, meaning that $i_{2(AV)}=0$, and $v_{C1}=v_{C2}=V_{C0}$. The switch and diode conduction voltages are neglected, $V_S=V_{DF}\cong 0$. Hence, the resonant circuit current i_{2R} is zero, and the capacitor C_S initial voltage is $v_{CS}=V_{C0}$. Then, at the instant $t=0$, a step ΔV_C is applied on the input voltage v_{C1}, while the voltage v_{C2} remains constant. Then, the average currents, i_S, i_D and i_2 will be computed. Finally, the inductance L_E will be computed from variation of the average current i_2.

The switch S_1 (Fig. 9.1 (a).) is closed and a step voltage ΔV_C is applied on the voltage source v_{C1} at the instant $t=0$, while the voltage v_{C2} remains constant.

$$\begin{aligned} v_{C1} &= V_{C0}h(t+\infty) + \Delta V_C h(t) \\ v_{C2} &= V_{C0}h(t+\infty) \end{aligned}, \tag{9.1}$$

where *h(t)* is the step function defined as

$$h(t) = \begin{cases} 0 & t \le 0 \\ 1 & t > 0 \end{cases}. \tag{9.2}$$



(a) (b)

Fig. 9.1 a) Simplified circuit diagram of the DC-DC2 converter, and b) the equivalent circuit diagram.

Neglecting the circuit resistance, the instantaneous currents i_{2R}, i_2, i_S and i_D can be described by a train of half-sinusoidal pulses with cycle by cycle increasing magnitude. The waveforms are illustrated in Fig. 9.2 (a). The phase portrait of the resonant circuit is shown in Fig. 9.2 (b).

The equations describing the currents i_{2R}, i_2, i_S and i_D are

$$i_{2R}(t) = \begin{cases} (-1)^k \dfrac{(k+1)\Delta V_C}{\omega_0 L_S} \sin\omega_0\left(t - k\dfrac{T_{S2}}{2}\right) & k\dfrac{T_{S2}}{2} < t \le k\dfrac{T_{S2}}{2} + \dfrac{T_0}{2} \\ 0 & k\dfrac{T_{S2}}{2} + \dfrac{T_0}{2} < t \le (k+1)\dfrac{T_{S2}}{2} \end{cases}, \tag{9.3}$$

$$i_2(t) = \begin{cases} \dfrac{(k+1)\Delta V_C}{\omega_0 L_S} \sin\omega_0\left(t - k\dfrac{T_{S2}}{2}\right) & k\dfrac{T_{S2}}{2} < t \le k\dfrac{T_{S2}}{2} + \dfrac{T_0}{2} \\ 0 & k\dfrac{T_{S2}}{2} + \dfrac{T_0}{2} < t \le (k+1)\dfrac{T_{S2}}{2} \end{cases}, \tag{9.4}$$

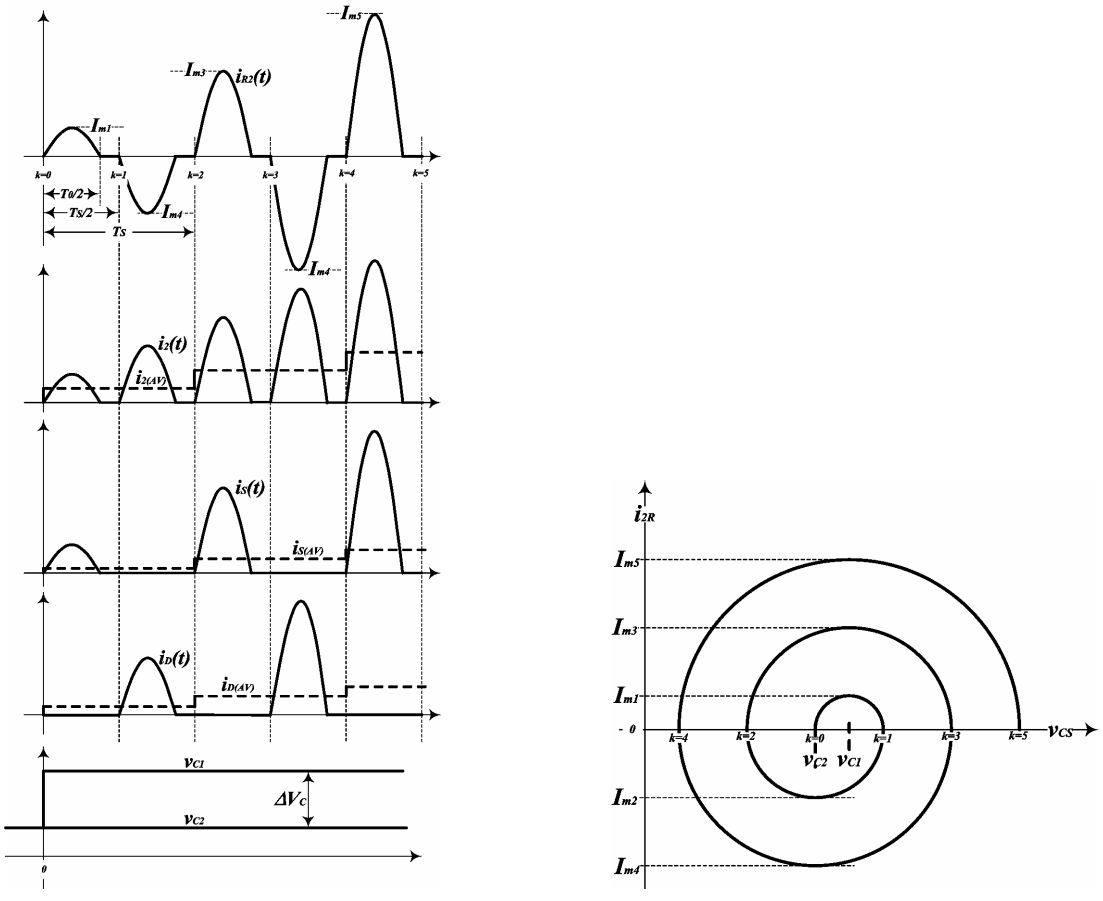
$$i_S(t) = \begin{cases} \dfrac{(k+1)\Delta V_C}{\omega_0 L_S} \sin\omega_0\left(t - k\dfrac{T_{S2}}{2}\right) & k\dfrac{T_{S2}}{2} < t \le k\dfrac{T_{S2}}{2} + \dfrac{T_0}{2} \\ 0 & k\dfrac{T_{S2}}{2} + \dfrac{T_0}{2} < t \le (k+2)\dfrac{T_{S2}}{2} \end{cases}, \tag{9.5}$$

$$i_D(t)=\begin{cases}0 & k\dfrac{T_{S2}}{2}<t\le(k+1)\dfrac{T_{S2}}{2}\\ \dfrac{(k+2)\Delta V_C}{\omega_0 L_S}\sin\omega_0\left(t-(k+1)\dfrac{T_{S2}}{2}\right) & (k+1)\dfrac{T_{S2}}{2}<t\le(k+1)\dfrac{T_{S2}}{2}+\dfrac{T_0}{2}\\ 0 & (k+1)\dfrac{T_{S2}}{2}+\dfrac{T_0}{2}<t\le(k+2)\dfrac{T_{S2}}{2}\end{cases}. \tag{9.6}$$

Average values of the currents (9.3)-(9.6) are

$$\begin{aligned} i_{2(AV)}(k)&=\frac{1}{T_S}\int_t^{t+T_S} i_{2R}(t)dt=(2k+3)\frac{\Delta V_C}{2\pi^2 L_S}\frac{T_0^2}{T_{S2}},\\ i_{S(AV)}(k)&=\frac{1}{T_S}\int_t^{t+T_S} i_S(t)dt=(k+1)\frac{\Delta V_C}{2\pi^2 L_S}\frac{T_0^2}{T_{S2}},\\ i_{D(AV)}(k)&=\frac{1}{T_S}\int_t^{t+T_S} i_D(t)dt=(k+2)\frac{\Delta V_C}{2\pi^2 L_S}\frac{T_0^2}{T_{S2}}, \end{aligned} \tag{9.7}$$

where k is a floor integer defined as $k = INT(\dfrac{2t}{T_{S2}})$.



(a) (b)

Fig. 9.2 The resonant current i_{R2}. a) Time diagram, and b) the phase portrait.

Variation of the average current i_2 between two successive cycles is

$$\Delta i_{2(AV)}(k) = i_{2(AV)}(k+2) - i_{2(AV)}(k) = 2\frac{\Delta V_C}{\pi^2 L_S}\frac{T_0^2}{T_{S2}}. \tag{9.8}$$

The equivalent circuit of Fig. 9.1 (b) can be described by difference equation

$$\frac{\Delta i_{2(AV)}(k)}{\Delta T} L_E = v_{C1}(k) - v_{C2}(k) = \Delta V_C(k), \tag{9.9}$$

where the time step is $\Delta T = T_{S2}$. Finally, from (9.8) and (9.9) one computes the equivalent inductance L_E as

$$L_E = L_S \frac{\pi^2}{2}\left(\frac{T_{S2}}{T_0}\right)^2. \tag{9.10}$$

From (9.7) one can also define i_S and i_D as

$$\begin{aligned} i_{S(AV)}(k) &= \frac{k+1}{2k+3} i_{2(AV)}(k), \\ i_{D(AV)}(k) &= \frac{k+2}{2k+3} i_{2(AV)}(k). \end{aligned} \tag{9.11}$$

Fig. 9.3 illustrates interpolated equations (9.11). Notice that the difference between the currents i_S and i_D is initially 20% and it drops below 10% for $k>3$ (after three half-periods).

In this virtual experiment, we have assumed that the switch S_1 is closed at the same time as the variation ΔV_C is applied on v_{C1}. As the average currents are computed over an interval (0, T_{S2}), the diode average current is greater than the switch average current, as given in (9.7) and (9.11). However, if we assume that the switch S_2 is closed at the same time as the variation ΔV_C is applied on v_{C1}, the switch average current $i_{S(AV)}$ will be greater than the diode average current $i_{D(AV)}$. In reality, the step voltage could be applied at any instant in the interval (0, T_{S2}). Thus, the diode to switch average currents ratio could be any between the two extreme cases mentioned before. However, the switching frequency f_{SW2} is greater that the frequency of our interest. Therefore, it could be assumed that the transition period is much shorter than the observation period. In that case the switch and diode currents can be assumed as the same $i_{S(AV)} \cong i_{D(AV)}$.

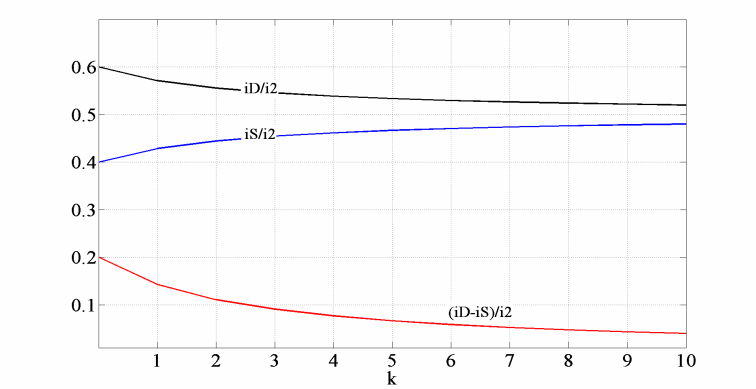


Fig. 9.3 Average current of the switch and diode versus number of cycles k.

9.2. The Entire Rectifier Model

9.2.1. Large Signal Model

Now, having model of the DC-DC1 and DC-DC2 converters, one can construct a model of the entire rectifier. The model is depicted in Fig. 9.4. The dc bus load is a constant power p_{LOAD} (this is typical load in controlled power converter applications). The inductance L_0 is the boost inductor, while the resistance R_0 is an equivalent input resistance

$$R_0 = R_{L0} + \frac{3}{\pi}\omega_m L_m . \tag{9.12}$$

The resistance R_{L0} is the boost inductor parasitic resistance, which includes the winding resistance and the core losses resistance [92]. The second part of (9.12) is model of the rectifier commutation voltage losses [115]. The frequency $\omega_m = 2\pi f_m$ is the mains angular frequency and L_m is the mains inductance.

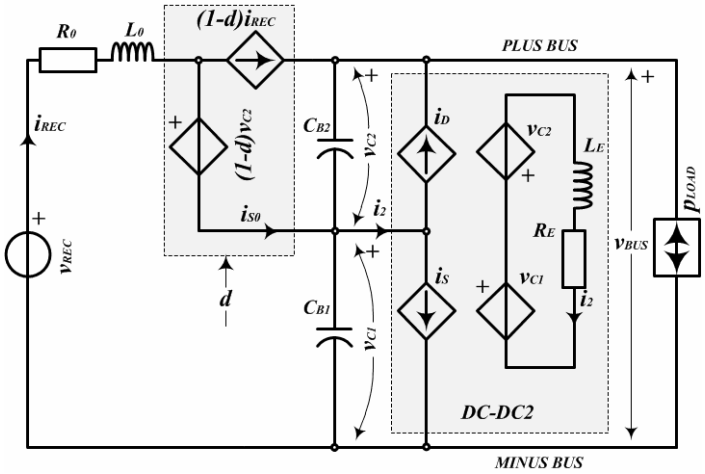


Fig. 9.4 Large signal model of the entire boost rectifier.

The large signal model of circuit in Fig. 9.4 is described by set of nonlinear differential equations,

$$L_0 \frac{di_{REC}}{dt} = -R_0 i_{REC} + v_{REC} - v_{BUS} + d \cdot v_{C2} , \tag{9.13}$$

$$\left.\begin{aligned} L_E \frac{di_2}{dt} &= -R_E i_2 + v_{C1} - v_{C2} \\ C_{B1} \frac{dv_{C1}}{dt} &= i_{REC} - i_S - \frac{p_{LOAD}}{v_{BUS}} \\ C_{B2} \frac{dv_{C2}}{dt} &= (1-d) i_{REC} + i_D - \frac{p_{LOAD}}{v_{BUS}} \\ v_{BUS} &= v_{C1} + v_{C2} \end{aligned}\right\} . \tag{9.14}$$

Variable d is duty cycle as the modulation signal of the DC-DC1 converter. The duty cycle is generated by a non-linear controller, where the control law is

$$d = \frac{u - v_{REC} + v_{BUS}}{v_{C2}}. \tag{9.15}$$

The variable u is the main control variable that is generated by the upper level controller (the rectifier current controller for example). Substituting (9.15) into (9.13) yields linear differential equation

$$L_0 \frac{di_{REC}}{dt} = u - R_0 i_{REC}. \tag{9.16}$$

The dc bus circuit is described by (9.14). However, notice that duty cycle d appears as an intermediate variable in (9.14). To find an equation that describes the dc bus circuit (the dc bus voltage v_{BUS}) as a function of the rectifier current i_{REC} as the control variable, one can use the power balance

$$p_{IN} = p_{OUT} + \sum_{k=1}^{N} i_k^2 R_k + \sum_{j=1}^{M} i_j L_j \frac{di_j}{dt} + \sum_{i=1}^{Q} v_i C_i \frac{dv_i}{dt}. \tag{9.17}$$

p_{IN} and p_{OUT} are the system input and output power, N is number of the resistors (including parasitic resistances), M is number of the inductors and Q is number of the capacitors in the circuit. Applying (9.17) on the circuit of Fig. 9.4 yields

$$\begin{aligned} v_{REC} i_{REC} = p_{LOAD} &+ L_0 i_{REC} \frac{di_{REC}}{dt} + R_0 i_{REC}^2 + L_E i_2 \frac{di_2}{dt} + R_E i_2^2 \\ &+ C_{B1} v_{C1} \frac{dv_{C1}}{dt} + C_{B2} v_{C2} \frac{dv_{C2}}{dt} \end{aligned}. \tag{9.18}$$

Assuming that the filter capacitors are the same $C_{B1} = C_{B2} = 2C_B$, (9.18) can be rearranged as

$$\begin{aligned} v_{REC} i_{REC} = p_{LOAD} &+ L_0 i_{REC} \frac{di_{REC}}{dt} + R_0 i_{REC}^2 + C_B v_{BUS} \frac{dv_{BUS}}{dt} \\ &+ R_E i_2^2 + L_E \frac{di_2}{dt} \left(i_2 + C_B L_E \frac{d^2 i_2}{dt^2} \right) \end{aligned}. \tag{9.19}$$

From (9.14) we have the following set of equations that describes the balancing current i_2 and balancing voltage error Δv_C (the DC-DC2 converter)

$$\begin{aligned} L_E \frac{di_2}{dt} &= -R_E i_2 + \Delta v_C \\ C_B \frac{d\Delta v_C}{dt} &= d \cdot i_{REC} - i_2 \\ \Delta v_C &= v_{C1} - v_{C2} \end{aligned}. \tag{9.20}$$

Here, product of duty cycle and rectifier current, $d \cdot i_{REC}$, is the disturbance for the DC-DC2 converter.

9.2.2. Linearization and Small Signal Model

The small signal model is obtained by the use of the first order perturbation model or Taylor series expansion. Then, Laplace transformation is applied to obtain the rectifier current (9.21) and the dc bus voltage (9.22) transfer functions.

$$i_{REC}(s)=u(s)\frac{1}{R_0+sL_0} \tag{9.21}$$

$$\begin{aligned} v_{BUS}(s)=i_{REC}(s)&\frac{\left(V_{REC}V_{BUS}-2R_0k_{BOOST}\frac{\pi}{3}P_{LOAD}\right)-sL_0k_{BOOST}\frac{\pi}{3}P_{LOAD}}{sC_BV_{BUS}^2} \\ &+v_{REC}(s)\frac{k_{BOOST}\frac{\pi}{3}P_{LOAD}}{sC_BV_{BUS}^2}-\hat{p}_{LOAD}\frac{V_{BUS}}{sC_BV_{BUS}^2}\underbrace{-i_2(s)\frac{D_0\frac{P_{LOAD}}{V_{BUS}}k_{BOOST}\frac{\pi}{3}(2R_E+sL_E)}{sC_BV_{BUS}^2}}_{\cong 0} \end{aligned} \tag{9.22}$$

Transfer functions of the voltage balancing error Δv_C and balancing current i_2 are,

$$\begin{aligned} i_2(s)=i_{REC}(s)&\frac{\frac{D_0V_{C2}+R_0\frac{P_{LOAD}}{V_{BUS}}k_{BOOST}\frac{\pi}{3}}{V_{C2}}+s\frac{L_0\frac{P_{LOAD}}{V_{BUS}}k_{BOOST}\frac{\pi}{3}}{V_{C2}}}{D(s)} \\ &+v_{REC}(s)\frac{\frac{P_{LOAD}}{V_{C2}V_{BUS}}k_{BOOST}\frac{\pi}{3}}{D(s)}\underbrace{-v_{BUS}(s)\frac{\frac{(2-D_0)}{2}\frac{P_{LOAD}}{V_{C2}V_{BUS}}k_{BOOST}\frac{\pi}{3}}{D(s)}}_{\cong 0}, \end{aligned} \tag{9.23}$$

$$\Delta v_C(s)=i_2(s)(sL_E+R_E), \tag{9.24}$$

where the denominator *D(s)* is

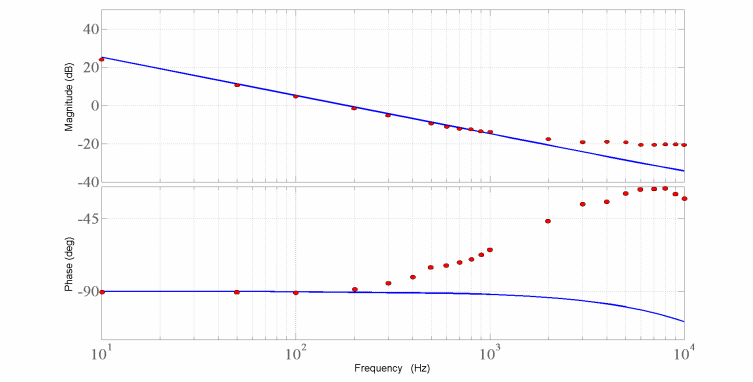
$$D(s)=s^2L_EC_B+s\left(R_EC_B+\frac{D_0L_E}{2}\frac{P_{LOAD}}{V_{C2}V_{BUS}}k_{BOOST}\frac{\pi}{3}\right)+\left(1+\frac{D_0R_E}{2}\frac{P_{LOAD}}{V_{C2}V_{BUS}}k_{BOOST}\frac{\pi}{3}\right). \tag{9.25}$$

D_0 is steady state duty cycle. Notice that the current i_2 figures in the dc bus voltage v_{BUS} transfer function (9.22), and the dc bus voltage figures in the current transfer functions (9.23). Substituting (9.22) into (9.23) and vice versa, we can eliminate i_2 from (9.23) and v_{BUS} from (9.22). However, in that case the dc bus voltage transfer function will be a third order function, which is complex and difficult to analyse and use in the controller synthesis.

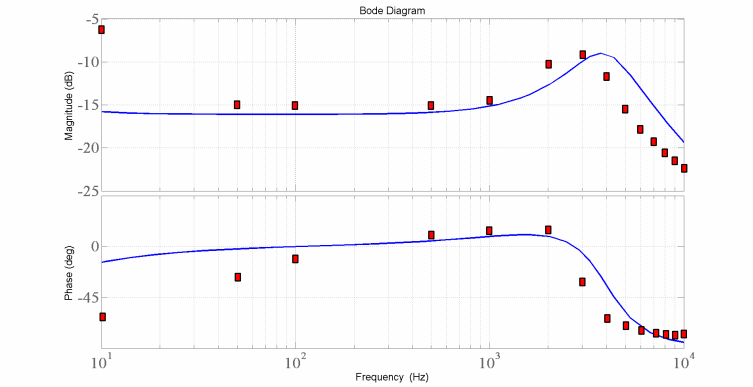
As shown in (9.10), the equivalent inductance L_E depends on the resonant inductor L_S and ratio of the resonant to the switching frequency. The inductor L_S is normally very small, in order of several hundred *nH*. If the DC-DC2 operates close to resonant frequency, it follows from (9.10) that the equivalent inductance L_E is order of μH. Also, the resistance R_E is quite small in comparison to the resistance R_0. Therefor, we can assume that dominant frequency of the DC-DC2 circuit is much greater than dominant frequency of the dc bus circuit. It will be shown in the following section that the dc bus controller bandwidth is normally limited to a few hundred Hz. That means the dc bus circuit frequency of interest is below 1 kHz. On another hand, the dominant frequency of the DC-DC2 circuit is above 1 kHz. Hence, last part of (9.22) and (9.23) could be neglected.

9.2.3. Matlab/Simulink Model Verification

To verify transfer functions (9.22) and (9.23), simulation of the large signal model (9.13) and (9.14) has been performed in Matlab/Simulink. Frequency response at different frequencies has been simulated and compared with bode diagram of the transfer functions (9.22) and (9.23). Fig. 9.5 (a) illustrates frequency characteristics of the transfer function $v_{BUS}(s)/i_{REC}(s)$. The solid blue line is computed from (9.22) and the red dots are the simulation of the entire large signal model (9.13), (9.14). Please, note that at low frequency, below 1kHz, the model magnitude and phase characteristics closely match the simulation. At frequency above 1 kHz, the model underestimates the magnitude and phase, because we have neglected the last part in the model. In the applications of our interest (three-phase boost rectifiers with electrolytic dc bus capacitor), the voltage controller is quiet slow, and the model (9.22) is accurate enough. However, if the boost converter is used in an application that requires high bandwidth of the dc bus voltage control, the simplified model is not sufficient; the effect of the DC-DC2 converter must be taken into account and the full model used. Fig. 9.5 (b) illustrates bode diagram of the transfer function $i_2(s)/i_{REC}(s)$. The solid blue line is calculation from (9.23) and the red squares are the simulation of the entire large signal model (9.13) and (9.14). Notice that at low frequency, below 50Hz, the magnitude and phase response of the small signal model and the large signal model are quite different (magnitude is underestimated and the phase is overestimated).



(a)



(b)

Fig. 9.5 Bode diagram of the system transfer functions. a) $v_{BUS}(s)/i_{REC}(s)$ and b) $i_2(s)/i_{REC}(s)$. Red dots/squares: simulated values, blue line: value computed from (9.22) and (9.23).

At frequencies above 100Hz, the magnitude and phase responses are quite well matched. As mentioned in section 9.1, the DC-DC2 converter operates in open loop and therefore no need for closed loop control of the voltage error Δv_C.

9.3. Control Scheme

9.3.1. The Control Objective

The primary control objective is to asymptotically regulate the dc bus voltage v_{BUS} to a desired reference $v_{BUS(REF)}$. The secondary control objective is regulate the rectifier current in order to obtain $2\pi/3$ radians square waveform of the mains current with minimum total harmonic distortion factor (THD) and the partial weighted harmonic distortion factor (PWHD) [13].

The control scheme of the proposed boost rectifier is illustrated in Fig. 9.6. Please, note that the control scheme is more or less state of the art cascaded control [106], [115], [131], [132]. Two cascaded controllers can be identified: an inner current controller G_{iREC} and an outer voltage controller G_{vBUS}. The inner current controller regulates the rectifier current, while the outer controller regulates the dc bus voltage v_{BUS} and generates the reference i_{REC_REF} for the rectifier current controller. Synthesis of the rectifier current controller is state of the art [132], and it is not discussed in the dissertation. The dc bus voltage controller design and synthesis is discussed in detail.

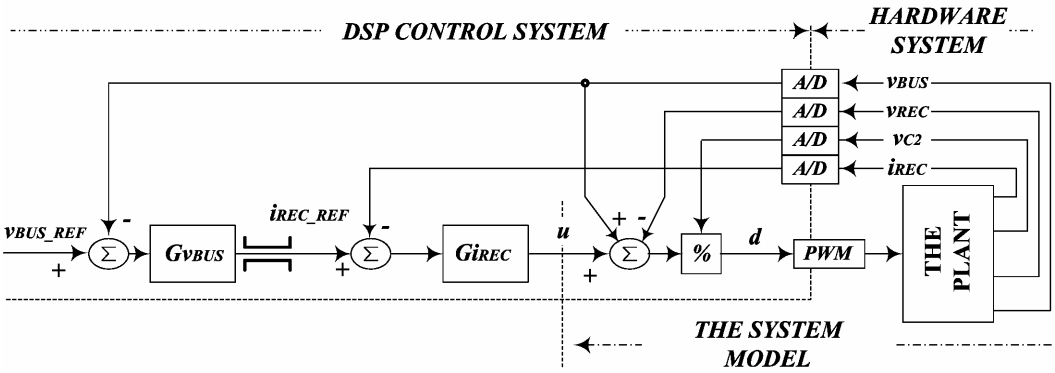


Fig. 9.6 The boost converter control structure.

9.3.2. The DC Bus Voltage Controller

The control block diagram is illustrated in Fig. 9.7. The rectifier current control loop appears in the dc bus voltage loop as transfer function that can be, for simplicity of the analysis, approximated by first order transfer function

$$\frac{i_{REC}(s)}{i_{REC\_REF}(s)} \cong \frac{1}{sT_{REC}+1}. \tag{9.26}$$

Let us consider that the bus voltage controller is a conventional proportional-integral (PI) controller $k_P + \frac{k_I}{s}$. The dc bus voltage closed loop transfer function is

$$\frac{v_{BUS}(s)}{v_{BUS\_REF}(s)} = \frac{-s^2 k_P L_0 P_{LOAD} + s\left(V_{REC}^2 k_P - k_I L_0 P_{LOAD}\right) + V_{REC}^2 k_I}{D_{BUS}(s)}, \tag{9.27}$$

$$\begin{aligned} D_{BUS}(s) = {} & s^3 C_B V_{BUS} V_{REC} T_{REC} + s^2 \left(C_B V_{BUS} V_{REC} - k_P L_0 P_{LOAD}\right) \\ & + s\left(V_{REC}^2 k_P - k_I L_0 P_{LOAD}\right) + V_{REC}^2 k_I \end{aligned}. \tag{9.28}$$

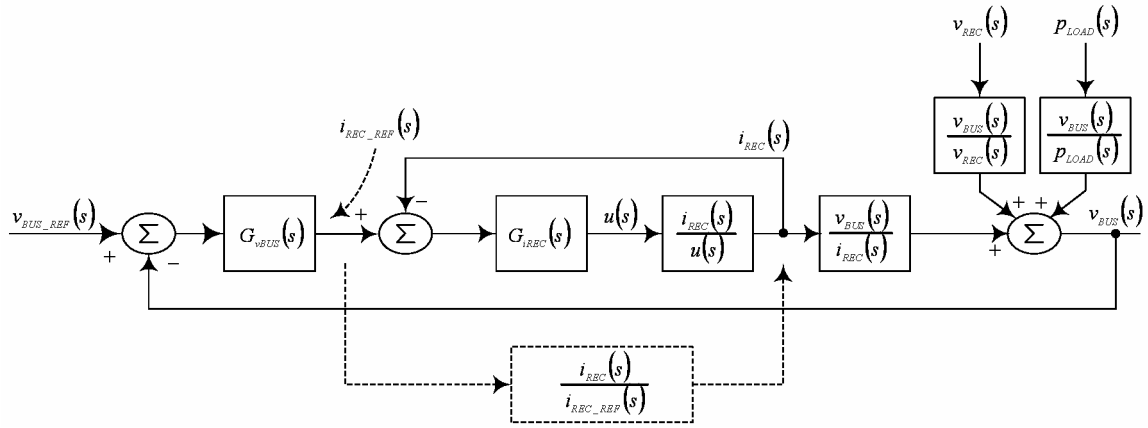


Fig. 9.7 Simplified small signal block diagram.

As a well known issue, the boost converter operating in continuous conduction mode (CCM) is a non-minimum phase system [112]-[114]. This is caused by the boost inductor that imposes right half plane zero (RHPZ) in the dc bus voltage transfer function. A system with the RHPZ is naturally stable system if it operates in open loop. However, when the system is in closed loop, the RHPZ appears in denominator of the dc bus voltage transfer function and as that it limits the system bandwidth [112]-[114], [131]. It was shown in section 8.2.2.1 that the boost inductor of the proposed boost rectifier is up to 50% smaller than that of the ordinary single-switch boost rectifier. That means the RHPZ frequency is higher and therefore the dc bus voltage bandwidth can be higher too. Moreover, the smaller boost inductor, the higher bandwidth of the rectifier current controller [132].

For simplicity of the analysis and the voltage controller design, one can assume that the boost inductor (L_0) is small enough. Thus, the RHPZ and the current controller response time T_{REC}) could be neglected. This yields the simplified transfer function

$$\frac{v_{BUS}(s)}{v_{BUS\_REF}(s)} \cong \frac{V_{REC}\left(sk_P + k_I\right)}{s^2 C_B V_{BUS} + sV_{REC} k_P + V_{REC} k_I}. \tag{9.29}$$

Proportional and integral gains of the voltage controller are computed from (9.29) using the Butterworth criteria ($\zeta_{BUS}=0.7$) [131].

$$\begin{aligned} k_P &= 4\pi f_B \frac{C_B V_{BUS}}{V_{REC}} \\ k_I &= 4\pi^2 f_B^2 \frac{C_B V_{BUS}}{V_{REC}} \end{aligned}, \tag{9.30}$$

where f_B is the dc bus voltage controller bandwidth.

9.3.2.1. The Bandwidth versus the Rectifier Current Ripple

A three-phase diode boost rectifier that operates in CCM is not a ripple-free converter. The dc bus voltage is not zero ripple voltage, as given in (8.28) [116]. The voltage ripple is reflected on the rectifier current reference via the dc bus voltage controller G_{vBUS}. To avoid distortion of the rectifier current, a few solutions are proposed in the literature [134]-[136]. The simplest one is to design the dc bus voltage controller with low bandwidth. Another solution is ripple cancellation techniques [134], or the voltage dead zone control [135], [136]. In this dissertation, a conventional technique is considered; the voltage controller bandwidth is low enough to avoid significant distortion of the rectifier current.

Let us find maximum bandwidth for the rectifier current ripple given as a parameter. Peak-to-peak dc bus voltage ripple has been computed in section 8.2.2.2 as

$$\Delta v_{BUS} \cong \frac{2}{35}\frac{2P_{LOAD}}{V_{BUS}\left(6\omega_m C_{BUS}\right)}, \tag{9.31}$$

where $\omega_m = 2\pi f_m$ is the mains angular frequency. The voltage ripple equation (9.31) is valid only if the rectifier current is constant (the current ripple is small enough to be neglected $\Delta i_{REC} << I_{REC}$). The ripple imposed on the current reference by the dc bus voltage ripple via the voltage controller is

$$\Delta i_{REC} = \Delta v_{BUS}\frac{\sqrt{\left(k_P 6\omega_m\right)^2 + k_I^2}}{6\omega_m}. \tag{9.32}$$

The rectifier current ripple at 6th harmonic of the mains frequency can be defined as relative ripple $\Delta(pu)$ in respect to the rectifier average current (8.4)

$$\Delta i_{REC} = \Delta(pu)\cdot I_{REC} = \Delta(pu)\cdot k_{BOOST}\frac{\pi}{3}\frac{P_{LOAD}}{V_{BUS}}, \tag{9.33}$$

where k_{BOOST} is the boost factor (8.8). From (9.32) and (9.33) it follows that

$$\Delta(pu)\cdot k_{BOOST}\frac{\pi}{3} = \frac{2}{35}\frac{2}{C_{BUS}}\frac{\sqrt{\left(k_P 6\omega_m\right)^2 + k_I^2}}{\left(6\omega_m\right)^2}. \tag{9.34}$$

Substituting (9.30) into (9.34) yields a biquadratic function with the dc bus voltage controller bandwidth f_B as unknown variable. Real and positive solution of that equation gives maximum bandwidth f_{Bmax} for the relative current ripple $\Delta(pu)$ given as the design parameter.

$$f_{B\max} 6\sqrt{2} f_m \sqrt{\sqrt{1+\Delta^2(pu)8.75}-1} \tag{9.35}$$

Note that the dc bus capacitance C_{BUS} does not figure in (9.35). The maximum bandwidth depends on the current ripple and the mains frequency only. The bandwidth versus current ripple is plotted in Fig. 9.8.

Experimental waveforms of the ac component of the rectifier current and the dc bus voltage are depicted in Fig. 9.9 (a). The amplitude spectrum of the rectifier current is depicted in Fig. 9.9 (b).

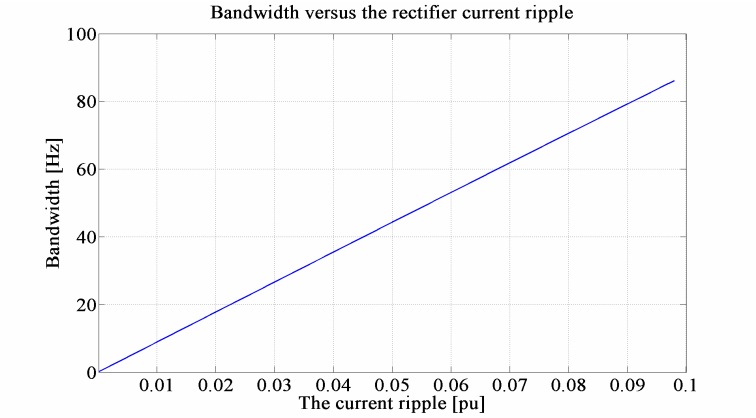
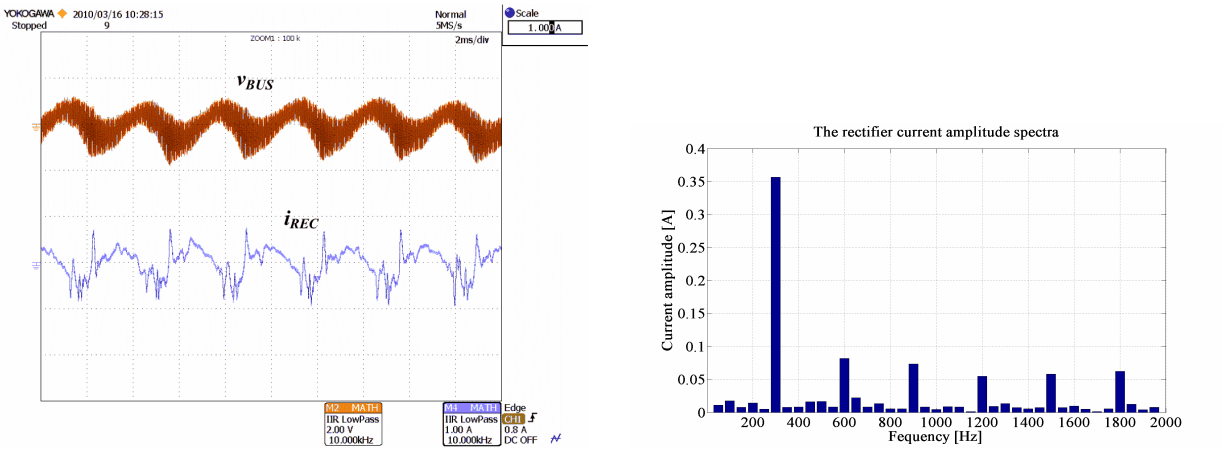


Fig. 9.8 The controller bandwidth versus the rectifier current ripple at 300Hz.



(a) (b)

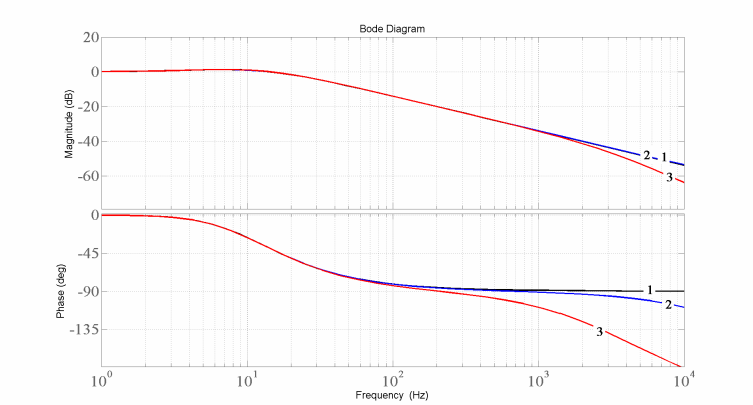
Fig. 9.9 a) Experimental waveforms of the rectifier current i_{REC} [1A/div] and the dc bus voltage v_{BUS} [2V/div]. b) Amplitude spectra of the rectifier current. V_{BUS}=650V, $V_{MAINS(RMS)}$=400V, P_{LOAD}=5500W, C_{BUS}=820μF and f_{BOOST}=50Hz.

9.3.3. Matlab/Simulink Simulation Results

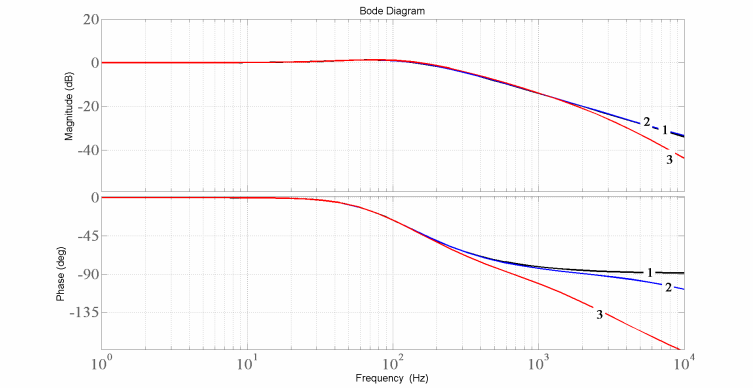
The voltage controller has been designed using simplified transfer function (9.29), for two different value of the bandwidth, f_B=10Hz and f_B=100Hz. Then, frequency response of the dc bus voltage control has been computed for different conditions; simplified model (9.29), the response time (T_{REC}=0) of the current controller neglected, and a system without approximations (9.27). The results are presented in Fig. 9.10. Notice, there is not significant difference in the magnitude response for the full model and approximated one. In the phase response, however, there is significant deviation at frequency above 1 kHz.

The boost rectifier with control was simulated using a Matlab/Simulink average model (9.13), (9.14). In this model, we have assumed that $i_{S(AV)}$=$i_{D(AV)}$=1/2 $i_{2(AV)}$. The simulation has been done for two different controller bandwidths, f_B=10Hz and f_B=100Hz. The dc bus voltage and rectifier current response on the step load are illustrated in Fig. 9.11. In the first case, the dc bus voltage has over-shoot and under-shoot of approximately 70V (11%) with settling time of approximately 100ms. The rectifier current ripple can be neglected. In the case that the controller bandwidth is 100Hz, the over-shoot and under-shoot are

approximately 5V (0.7%). The current ripple is however greater, approximately 0.5A (4.5% of the rectifier current). The voltage balancing error $\Delta v_C = v_{C1} - v_{C2}$ and compensation current i_2 averaged over the switching period are depicted in Fig. 9.12. The voltage error is very small, below 15mV. The average current i_2 follows the shape of the rectifier current and the instantaneous duty cycle, as predicted in (8.36).



(a)



(b)

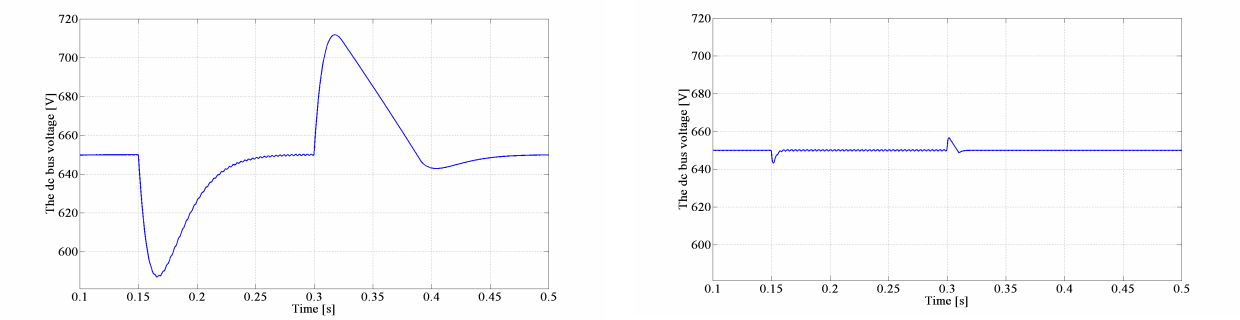
Fig. 9.10 Frequency response of the dc bus voltage controller under different conditions; 1) simplified model (33), 2) neglected the current control response time (T_{REC}=0), and 3) a system without approximations. a) f_B=10Hz and b) f_B=100Hz.

9.3.4. Experimental Results

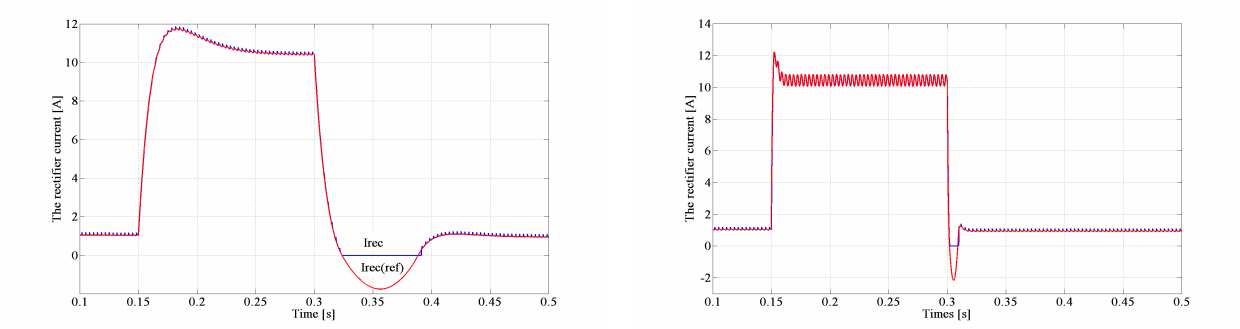
The model and control scheme proposed in this chapter have been experimentally verified on a 5.5kW prototype. The control algorithm, PWM and protection functions were implemented in a fixed-point 32bit digital signal processor (DSP). The rectifier current controller is executed at 100 kHz, while the dc bus voltage controller is executed at 5 kHz. The dc bus voltage controller was designed for bandwidth of 50Hz.

The rectifier specification is: V_{BUS}=650V, P_{LOAD}=5500W, V_{MAINS}=400V, C_{B1}=C_{B2}=1600μF (C_{BUS}=800μF), L_0=300μH, f_{SW1}=100 kHz, f_{SW2}=50 kHz.

Fig. 9.13 (a) shows waveforms of ac component of the rectifier voltage and current. Note the 300Hz component in the current waveform. This harmonic is caused by the dc bus voltage ripple via the voltage controller.

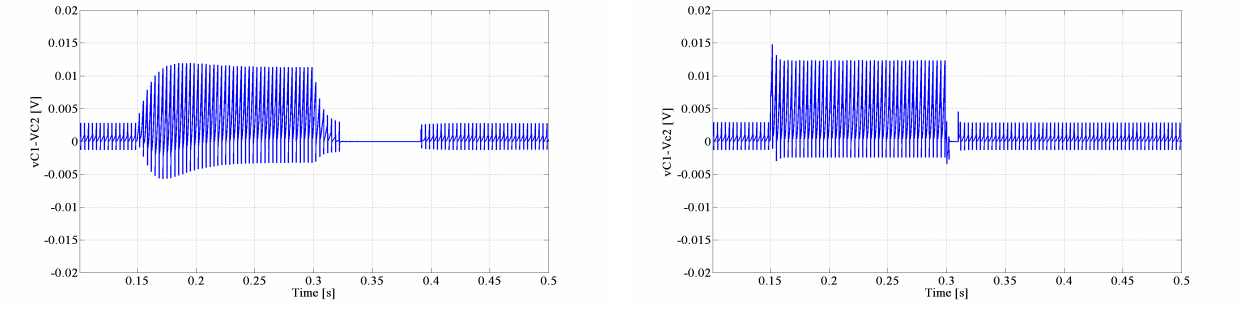


(a) (b)

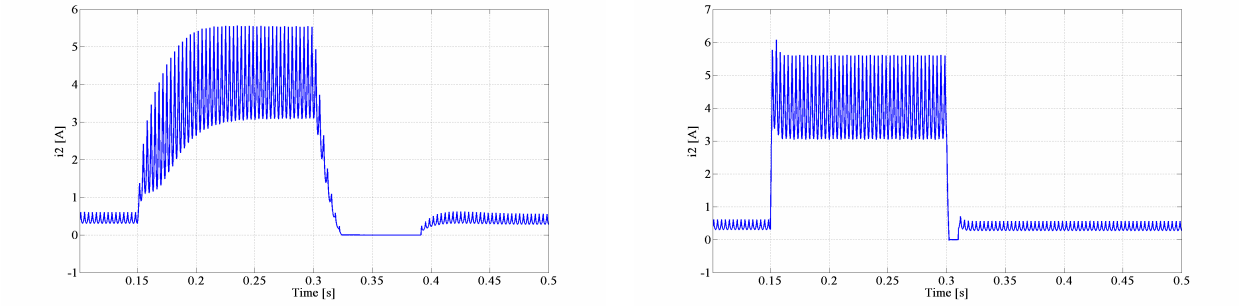


(c) (d)

Fig. 9.11 Simulation of the boost rectifier under step load variation (10% to 100% to10%). a) and c) the dc bus voltage, and b) and d) the rectifier current. The controller bandwidth f_B=10Hz (a, b), and f_B=100Hz (c, d). P_{LOAD}=550-5500W, V_{BUS}=650V, V_{REC}=600V, L_0=300µH, C_{BUS}=800µF.



(a) (b)

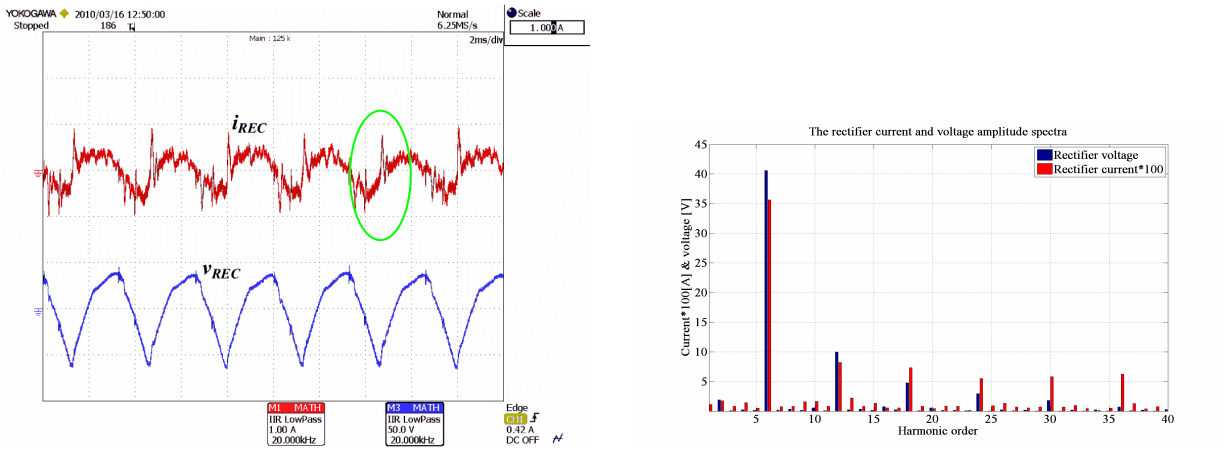


(c) (d)

Fig. 9.12 Simulation of the boost rectifier under step load variation (10% to 100% to10%). (a, c) the balancing voltage error Δv_C and (b, d) the current i_2 that is averaged over the switching period. The controller bandwidth f_B=10Hz (a, b), and f_B=100Hz (c, d). P_{LOAD}=550-5500W, V_{BUS}=650V, V_{REC}=600V, L_0=300µH, C_{BUS}=800µF.

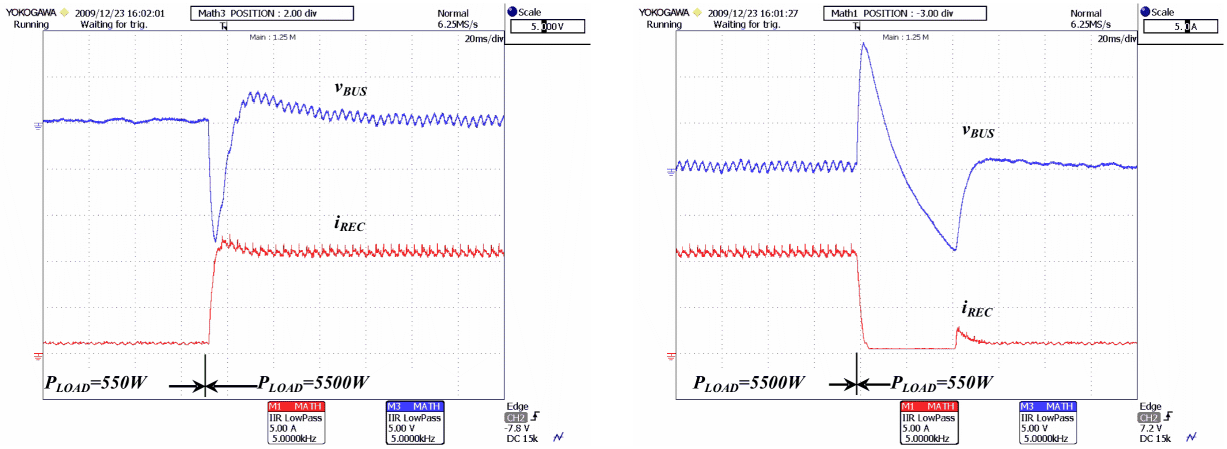
The spikes circled in the green are caused by the notches that are coming from the mains supply. Those disturbances can be reduced by the current controller having higher bandwidth or using some advanced current controller techniques, such as resonant or repetitive controller[138]-[139].

Performance of the dc bus voltage controller was tested on variation of the dc bus load. Experimental waveforms of the dc bus voltage and rectifier current are depicted in Fig. 9.14. The controller response on step load, 10% to 100% (550W to 5500W) is illustrated in Fig. 9.14 (a). The voltage undershoot is approximately 13 V (2% of the dc bus voltage) and response time is approximately 10ms. Fig. 9.14 (b) shows the waveforms when the load is reduced from 100% to 10%. The voltage over-shoot is approximately 14V (2.15%). Notice that the rectifier current is zero during the transient because the rectifier is a uni-directional device that does not allow the current in opposite direction. Thus, the current controller is saturated during this time. As a consequence, the dc bus voltage has an undershoot of approximately -9V. Once the current controller is out of saturation, the dc bus voltage settles down at the reference. This effect could be reduced, even completely eliminated by appropriate current control, but this is not subject of this dissertation.



(a) (b)

Fig. 9.13 The voltage controller response on step load. The rectifier current i_{REC} [1A/div] and ac component of the dc bus voltage v_{BUS} [50V/div]. a) Step load from 10% to 100%, and b) from 100% to 10%. V_{BUS}=650V, V_{MAINS}=400V, L_0=325µH, C_{BUS}=800µF and f_{BOOST}=50Hz.



(a) (b)

Fig. 9.14 The voltage controller response on step load. The rectifier current i_{REC} [5A/div] and ac component of the dc bus voltage v_{BUS} [5V/div]. a) Step load from 10% to 100%, and b) from 100% to 10%. V_{BUS}=650V, V_{MAINS}=400V, L_0=325µH, C_{BUS}=800µF and f_{BOOST}=50Hz.

10. SINGLE PHASE OPERATION

10.1. Short Introduction

Three-phase induction motors are the most popular motors in industry and other applications since the age of Tesla [1]-[3]. The three-phase motors are more efficient, less cost, last longer and have better torque/speed characteristic than single-phase motors. However, very often the three-phase public network is not available in some area where it may not be economical to install three-phase distribution network. In such applications, conversion from single-phase to three-phase is necessary.

A multi-phase system (including a three-phase system) can be represented by an equivalent two-phase system and vice versa. Single-phase system, however, cannot be represented by a multi-phase system of direct order [137]. Two-phase to three-phase transformation is easily possible by the use of the Scott transformer, while single-phase to three-phase transformation is not possible by the use of passive devices such as transformers. For this, more complex conversion systems, such as motor-generator groups or semiconductor power converters are used. The first solution has no practical value in the era of advanced power converters. Static power converters are used in most applications.

The single-phase supplied rectifier with passive LC dc bus filter and three-phase pulse width modulated (PWM) inverter is the most common solution, as shown in Fig. 10.1 (a). The dc bus capacitor is a large electrolytic capacitor, while the inductor is small or absent. Such a rectifier works as a peak detecting circuit; the dc bus voltage is charged on the peak mains voltage and the mains current is a train of narrow pulses. Apart the fact that such a rectifier is cost effective and robust, the drive manufacturers do not recommende this solution because of a few limitations:

-The input current is distorted, with peaks that are 5 to 10 times of the fundamental RMS current. The total harmonic distortion factor is as high as 150%, even higher. The power factor is low.

-A bulky dc bus capacitor is necessary to keep the dc bus voltage ripple acceptably low.

-A filter inductor must be used to limit peak of the input current. The inductance value is however limited because the dc bus voltage quickly decays with the inductance.

-The dc bus voltage is reduced in comparison to three-phase supplied drive. Hence, available motor voltage is reduced too.

-The drive life time is limited by the dc bus capacitor life time (the capacitor is the most stressed component).

-The drive may be de-rated by 50% when supplied from single-phase, which means higher installation cost per kW.

The single-phase single-switch and double-switch boost rectifier is the most popular solution in applications that require a boosted dc bus voltage and sinusoidal or pseudo-sinusoidal input current, Fig. 10.1 (b), (c), [66]. This topology is often used in low power supplies such as PC and small telecom supplies. In variable speed drives, however, this topology is rarely used because of cost, size and efficiency.

The split-capacitor three-leg rectifier/inverter is used in low cost low power variable speed drive applications, such as air-conditioning and home appliances [67], [68], Fig. 10.1 (d). This topology offers the lowest count of the active and passive components in comparison to the other solutions. However, two drawbacks make this topology inappropriate in higher power industrial applications; 1) The dc bus capacitor current stress at low frequency, and 2) the output current ripple.

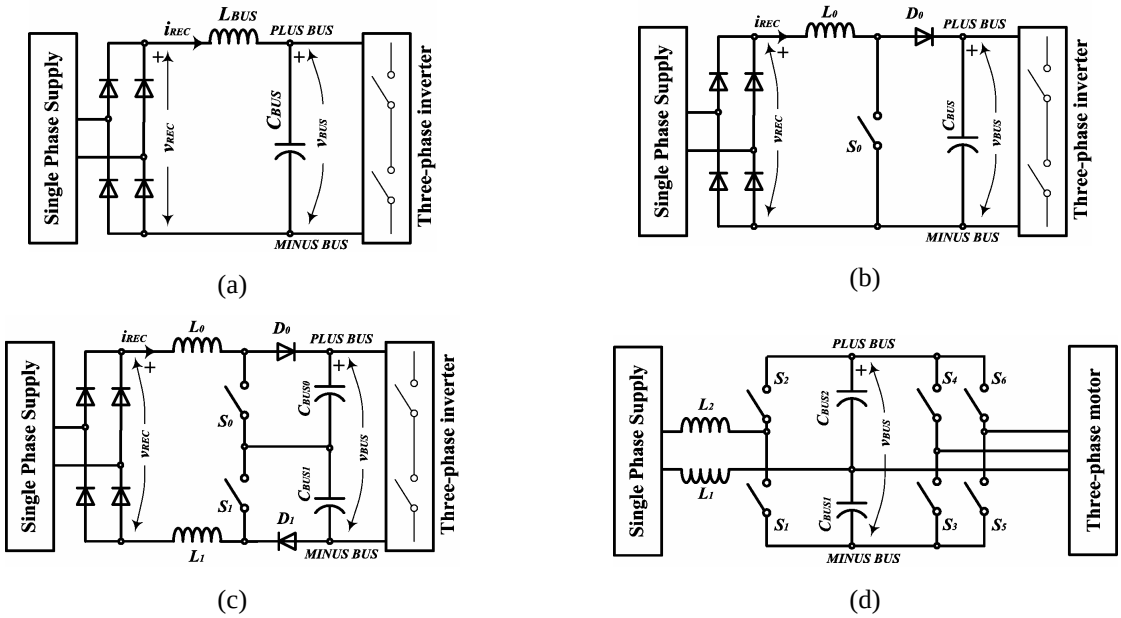


Fig. 10.1 State of the art solutions. a) Diode rectifier with passive filter, b) single switch boost rectifier and c) double boost rectifier.

A three-phase diode boost rectifier based on half-dc-bus-voltage rated topology has been presented in chapter 8 and [116]. The main feature of the topology is that the switches and diodes are rated at half of the dc bus voltage and fraction of the rectifier current. Power rating, size and efficiency of the entire rectifier strongly depend on the ratio of the dc bus voltage to the rectifier voltage (the boost factor). For example, if the boost factor is low, the power converter efficiency is as high as 98 to 99%.

In this chapter, three-phase half-dc-bus-voltage rated boost rectifier that operates under single-phase supply conditions is analyzed. In section 10.2 the principle of the proposed solution is analyzed and the main equations are derived. Further, in section 10.3, and 10.4, the main conversion structure is analyzed and design guidelines are given. The dc bus capacitor design is discussed in section 10.5.

10.2. Single Phase Operation of the Half-DC-Bus-Voltage Rated Boost Rectifier

10.2.1. The Principle

The basic principle of single-phase supplied three-phase boost rectifier and relevant waveforms are illustrated in Fig. 10.2 (a). Notice that the circuit diagram is the same as Fig.

8.4 (b), except the input rectifier is a single-phase rectifier instead of the three-phase rectifier. Idealized waveforms are depicted in Fig. 10.2 (b).

The boost rectifier consists of a single-phase diode rectifier, two uni-directional dc-dc converters, namely DC-DC1 and DC-DC2, and two series connected capacitors C_{B1} and C_{B2}. The DC-DC1 converter is connected in three points; the rectifier plus rail, the dc bus plus rail, and mid point of the capacitors C_{B1} and C_{B2}. The DC-DC1 converter generates the compensation voltage v_0, which is used as an intermediate voltage to regulate the rectifier current i_{REC} and the dc bus voltage v_{BUS}.

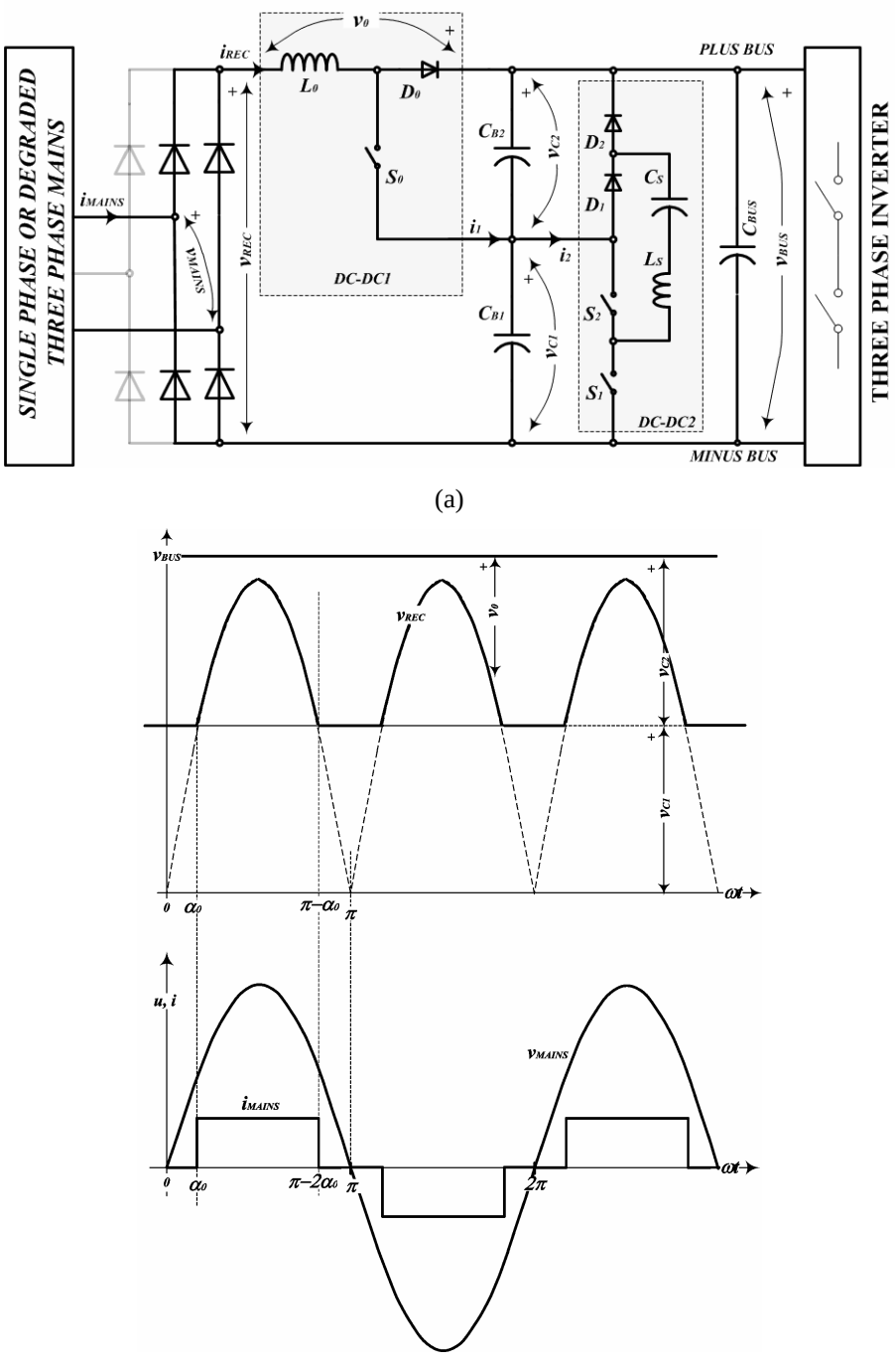


Fig. 10.2 a) Circuit diagram of the half-dc-bus-voltage-rated boost rectifier under single-phase supply conditions. b) Waveforms of the dc bus voltage v_{BUS}, rectifier voltage v_{REC}, the mains current i_{MAINS} and voltage v_{MAINS}.

The average current i_1 which flows from the DC-DC1 converter into the capacitors mid point is not zero. Since the capacitors average current must be zero in steady state, one additional converter DC-DC2 is used to compensate the current i_1 and maintain ratio between the voltages v_{C1} and v_{C2} constant.

Fig. 10.3 shows waveforms of the mains voltage and current and the dc bus voltage when the proposed boost rectifier and the ordinary diode rectifier with capacitive filter are used. The waveforms are recorded at 4000W load.

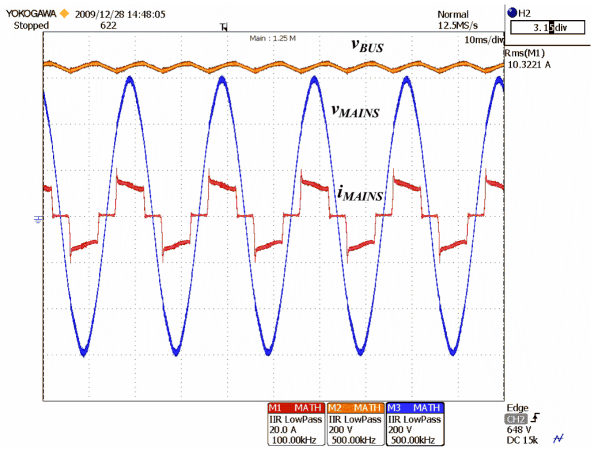


Fig. 10.3 Experimental waveforms of the mains voltage v_{MAINS} [200V/div] and current i_{MAINS} [20A/div] and the dc bus voltage v_{BUS} [200V/div]. $V_{BUS(AV)}$=650V, $V_{mains(RMS)}$=400V, P_{LOAD}=4000W, C_{BUS}=820μF.

10.2.2. A Short Analysis

Let the mains voltage be purely sinusoidal voltage

$$v_{mains}(t) = V_{PEAK}\sin(\omega_m t). \tag{10.1}$$

Also, let us assume that the rectifier current i_{REC} is constant during a period that the rectifier instantaneous voltage is greater than half of the dc bus voltage (see Fig. 10.2 (b)).

$$i_{REC}(t) = \begin{cases} I_{REC} & \alpha_0 \le \omega_m t \le \pi - \alpha_0 \\ 0 & otherwise \end{cases} \tag{10.2}$$

The threshold angle α_0 is

$$\alpha_0 = \arcsin\frac{v_{BUS}}{2V_{PEAK}} = \arcsin\frac{k_{BOOST}}{2}, \tag{10.3}$$

where the boost factor was defined in (8.4) as

$$k_{BOOST} = \frac{v_{BUS}}{V_{PEAK}}. \tag{10.4}$$

The rectifier current (10.2) is idealized. It has been assumed that the switching frequency is far higher than the mains frequency, and therefore small boost inductor L_0 is used. This is a correct assumption because the switching frequency is as high as 50 kHz or even higher in comparison to the mains frequency of 50Hz. As a consequence of such an

idealization, the current fall time and rise time are zero. That means the current instantaneously commutes from zero to I_{REC} at instant $\alpha = \alpha_0$ and from I_{REC} to zero at instant $\alpha = \pi - \alpha_0$. This will be discussed shortly after.

The threshold angle α_0 and the conducting angle $\pi - 2\alpha_0$ versus the boosting factor k_{BOOST} are plotted in Fig. 10.4. Notice that the minimum angle α_0 is 30° (π/6) and the maximum conducting angle $\pi - 2\alpha_0$ is 120° (2π/3).

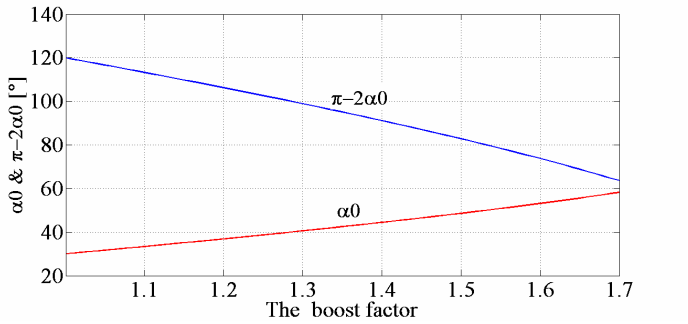


Fig. 10.4 The threshold angle α_0 and conducting angle π-$2\alpha_0$ versus the boost factor.

The rectifier voltage is

$$v_{REC}(t) = \begin{cases} \dfrac{v_{BUS}}{k_{BOOST}} \sin \omega_m t & \alpha_0 \le \omega_m t \le \pi - \alpha_0 \\ \dfrac{v_{BUS}}{2} & otherwise \end{cases}. \tag{10.5}$$

To find the magnitude of the rectifier current, one can use the instantaneous input power,

$$p_{IN}(t) = v_{REC}(t) i_{REC}(t) = \begin{cases} \dfrac{v_{BUS}}{k_{BOOST}} I_{REC} \sin \omega_m t & \alpha_0 \le \omega_m t \le \pi - \alpha_0 \\ 0 & otherwise \end{cases}. \tag{10.6}$$

Assume that the conversion losses can be neglected. Thus, the average input power P_{IN} is equal to the load power P_{LOAD},

$$P_{IN} = P_{LOAD} = \frac{1}{\pi} \int_0^{\pi} p_{IN}(\omega_m t) d(\omega_m t) = \frac{v_{BUS}}{k_{BOOST}} I_{REC} \frac{2}{\pi} \cos \alpha_0 . \tag{10.7}$$

The rectifier peak current is computed from (10.7) as

$$I_{REC} = \frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \frac{\pi}{2 \cos \alpha_0}, \tag{10.8}$$

where the angle α_0 (10.3) is a function of the boost factor (10.4).

10.2.2.1. THD, PH and PWHD versus the Boost Factor

The mains current is quasi-square waveform with magnitude I_{REC} and duration of π-$2\alpha_0$ radians. The current can be expanded in Fourier series

$$i_{MAINS} = \sum_{k=1}^{+\infty} I_k \sin\left(k\omega_m t + \psi_k\right) = \frac{P_{LOAD}}{v_{BUS}} 2k_{BOOST} \sum_{k=1}^{+\infty} \frac{\cos k\alpha_0}{k\cos\alpha_0} \sin\left(k\omega_m t\right). \tag{10.9}$$

The mains RMS current and the first harmonic RMS current are

$$I_{RMS} = \frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \frac{\pi}{2\cos\alpha_0} \sqrt{\frac{\pi - 2\alpha_0}{\pi}}, \qquad I_{(1)RMS} = \frac{P_{LOAD}}{v_{BUS}} \sqrt{2} k_{BOOST}. \tag{10.10}$$

Fig. 10.5 illustrates the mains peak and RMS current versus the boost factor k_{BOOST}.

Total harmonic distortion factor (THD), partially weighted harmonic distortion factor (PWHD) and power factor (PF) are computed from (10.10) as

$$THD = \frac{\sqrt{I_{RMS}^2 - I_{(1)RMS}^2}}{I_{(1)RMS}} = \sqrt{\frac{\pi}{8} \frac{\left(\pi - 2\alpha_0\right)}{\cos\alpha_0} - 1}, \qquad PWHD = \sqrt{\sum_{k=14}^{40} \frac{1}{k} \left(\frac{\cos(k\alpha_0)}{\cos\alpha_0} \right)^2}, \tag{10.11}$$

$$PF = \frac{S}{P_{LOAD}} = \frac{\pi}{2\sqrt{2}\cos\alpha_0} \sqrt{\frac{\pi - 2\alpha_0}{\pi}}.$$

THD and PF versus the boost factor are plotted in Fig. 10.6. The minimum THD that is possible to obtain is approximately 31% at minimum angle $\alpha_0 = 30°$. This is the same THD that can be obtained with the three-phase diode boost rectifier.

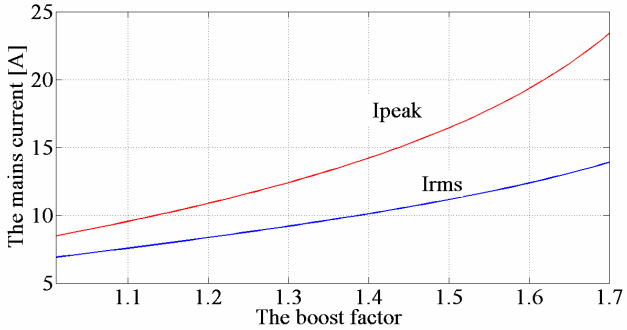


Fig. 10.5 The mains peak and RMS current versus the boost factor.

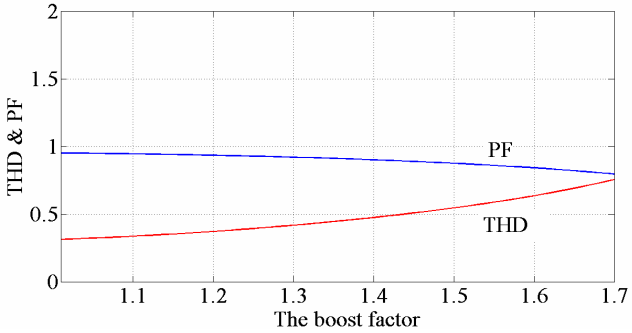


Fig. 10.6 Total harmonic distortion (THD) and power factor (PF) versus the boost factor.

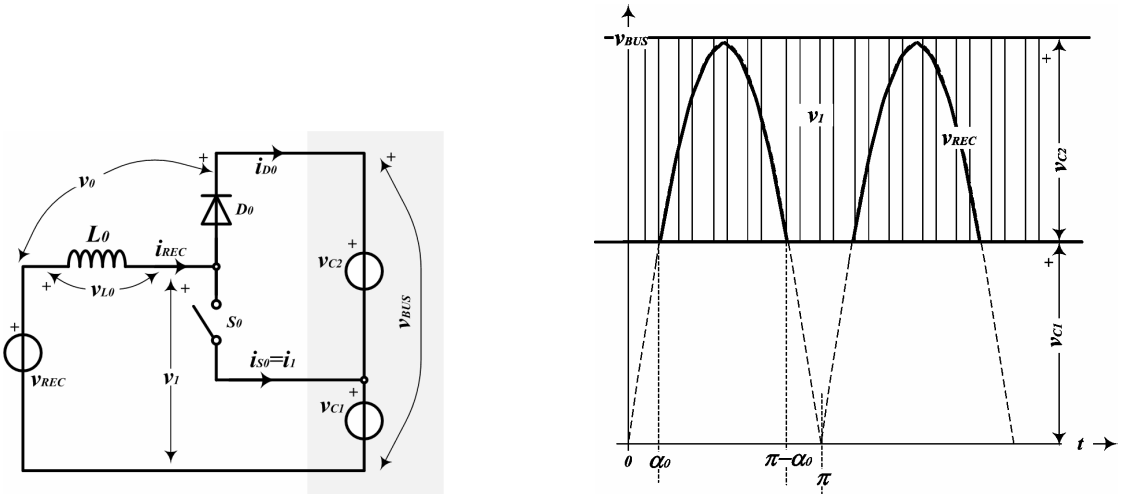
Remark: The THD is computed taking into account all higher harmonics (2 to ∞), while the PWHD factor is computed using IEC 61000-3-12 norm definition (8.13), [13].

10.3. The DC-DC1 Converter under Single Phase Supply

The DC-DC1 converter basically operates in the same way as the three-phase supplied rectifier. Therefore, main part of the analysis given in chapter 8 will not be repeated here.

10.3.1. An Ideal Circuit Analysis

An equivalent circuit diagram of the DC-DC1 and waveforms of the dc bus voltage v_{BUS}, the rectifier voltage v_{REC} and switching voltage v_1 are depicted in Fig. 10.7.



(a) (b)

Fig. 10.7 a) The DC-DC1 converter equivalent circuit. b) The dc bus voltage v_{BUS}, the rectifier voltage v_{REC} and switching voltage v_1.

The duty cycle is computed from (8.15) and (10.5) as

$$d(\omega_m t)=\begin{cases} 2\left(1-\dfrac{\sin\omega_m t}{k_{BOOST}}\right) & \alpha_0 \le \omega_m t \le \pi-\alpha_0 \\ 1 & otherwise \end{cases}. \tag{10.12}$$

Maximum boost factor when the rectifier is supplied from three-phase mains has been defined under condition that the rectifier current is continuous. However, this criterion cannot be used in single phase supply because the rectifier current is naturally discontinuous (zero during period α_0). The criterion for single-phase supply can be controllability of the dc bus voltage; the peak of the input voltage cannot be lower than half of the dc bus voltage. From this we have

$$k_{BOOST(\max)} = \lim_{\alpha_0 \to \frac{\pi}{2}} (2\sin\alpha_0) = 2. \tag{10.13}$$

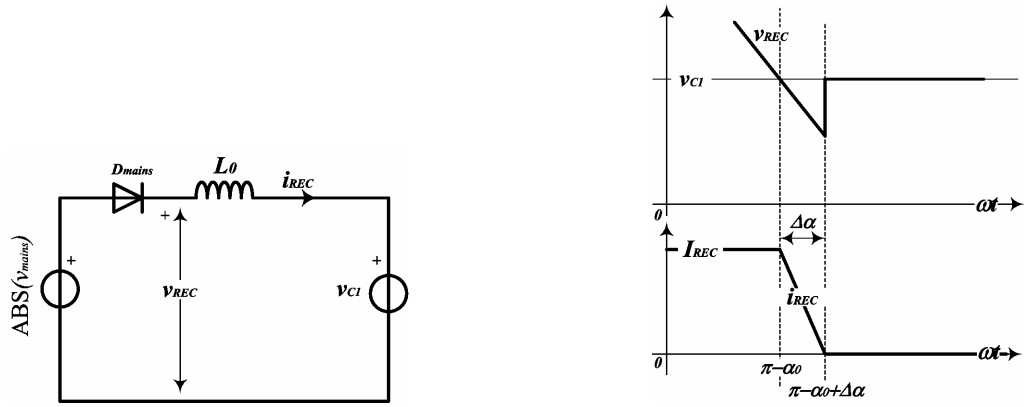
This value is, of course, not realistic because in such a case the conduction period of the rectifier current is zero, and therefore the peak current is infinite. In most applications, the boost factor is often not greater than 1.5, and therefore the limitation (10.13) has no relevance.

10.3.2. The Mains Diode Commutation Effect

Once the rectifier voltage reaches the voltage v_{C1}, at the angle $\alpha = \pi - \alpha_0$, the duty cycle is limited to 1 (the boost inductor is permanently connected to the v_{C1} via the switch S_0). Then, the current i_{REC} will start decreasing towards zero. After delay $\Delta\alpha$, the current reaches zero and mains diode D_{mains} is blocked. The current remains zero and the rectifier voltage v_{REC} jumps to the v_{C1} and the commutation is finished. Fig. 10.8 shows waveforms of the rectifier current and voltage.

The commutation angle is approximated as

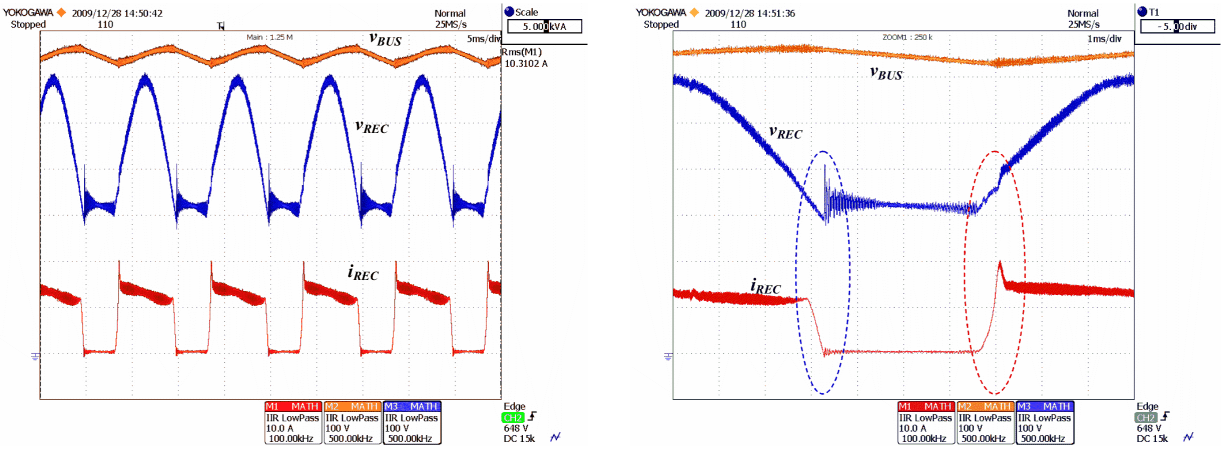
$$\Delta\alpha \cong \frac{\omega_m L_0 I_{REC} k_{BOOST}}{v_{BUS} \sin\alpha_0} . \tag{10.14}$$



(a) (b)

Fig. 10.8 Commutation of the mains diode. a) the equivalent circuit, and b) zoom of the rectifier voltage and current.

Fig. 10.9 (a) shows experimental waveforms of the rectifier voltage v_{REC} and current i_{REC}. Note that the rectifier current is not constant during the conduction period (α_0, π-$2\alpha_0$). The current variation is caused by the dc bus voltage ripple that is reflected to the rectifier current reference via the dc bus voltage controller. Fig. 10.9 (b) shows a zoomed in plot of the waveforms. Please, note two irregularities in the current waveform. The first one is the mains diode commutation effect (denoted by the blue circle). The second irregularity is over-shoot (denoted by the red circle). The current over-shoot is caused by saturation of the rectifier current controller (the wind up effect). This problem could be fixed by proper design of the rectifier current controller.



(a) (b)

Fig. 10.9 a) Experimental waveforms of the rectifier voltage v_{REC} [100V/div] and current i_{REC} [10A/div] and the dc bus voltage v_{BUS} [100V/div]. b) Zoom. $V_{BUS(AV)}=650V$, $V_{MAINS(RMS)}=400V$, $P_{LOAD}=4000W$, $C_{BUS}=820\mu F$.

10.3.3. The Switch and Boost Diode Stress Analysis

The switch average and RMS current computed over the mains half period are

$$I_{S0(AV)} = I_{REC}\frac{1}{\pi}\int_{\alpha_0}^{\pi-\alpha_0} 2\left(1-\frac{\sin\omega_m t}{k_{BOOST}}\right)d(\omega_m t) = \frac{P_{LOAD}}{v_{BUS}}\left(k_{BOOST}\frac{(\pi-2\alpha_0)}{\cos\alpha_0}-2\right), \tag{10.15}$$

$$I_{S0(RMS)} = \sqrt{\frac{1}{\pi}\int_{\alpha_0}^{\pi-\alpha_0} I_{REC}^2\, 2\left(1-\frac{\sin\omega_m t}{k_{BOOST}}\right)d(\omega_m t)} = \frac{P_{LOAD}}{v_{BUS}}\frac{1}{\cos\alpha_0}\sqrt{\pi\left(\left(\frac{\pi}{2}-\alpha_0\right)-\frac{\cos\alpha_0}{k_{BOOST}}\right)}. \tag{10.16}$$

The switch conduction losses are

$$P_{S0} = V_{S0}I_{S0(AV)} + r_{S0}I_{S0(RMS)}^2. \tag{10.17}$$

The switch S_0 is approximated by threshold voltage V_{S0} and dynamic resistance r_{S0}. The switching losses averaged over the mains half period are

$$P_{Sw} = \frac{1}{\pi}\int_{\alpha_0}^{\pi-\alpha_0}\frac{v_{BUS}I_{REC}}{2V_N I_N}(E_{ON}+E_{OFF})f_{SW}\,d(\omega_m t) = \frac{P_{LOAD}}{2V_N I_N}k_{BOOST}(E_{ON}+E_{OFF})f_{SW}\frac{\pi-2\alpha_0}{2\cos\alpha_0}, \tag{10.18}$$

where f_{SW} is switching frequency. E_{ON} and E_{OFF} are switching energy at given conditions; rated voltage V_N and current I_N.

Similar calculation could be applied on the boost diode D_0.

$$I_{D0(AV)} = \frac{P_{LOAD}}{v_{BUS}}\left(2-k_{BOOST}\frac{(\pi-2\alpha_0)}{2\cos\alpha_0}\right) \tag{10.19}$$

$$I_{D0(RMS)} = \frac{P_{LOAD}}{v_{BUS}}\frac{k_{BOOST}\pi}{2\cos\alpha_0}\sqrt{\frac{4\cos\alpha_0-(\pi-2\alpha_0)k_{BOOST}}{\pi k_{BOOST}}} \tag{10.20}$$

$$P_{D0}=\underbrace{V_{D0}I_{D0(AV)}+r_{D0}I_{D0(RMS)}^2}_{CONDUCTION}+\underbrace{\frac{P_{LOAD}}{2V_NI_N}k_{BOOST}E_Q f_{SW}\frac{\pi-2\alpha_0}{2\cos\alpha_0}}_{SWITCHING} \tag{10.21}$$

The diode is approximated by threshold voltage V_{D0} and dynamic resistance r_{D0}. E_Q is reverse recovery energy at given conditions; rated voltage V_N and current I_N.

10.3.4. Boost Inductor

The inductor losses averaged over the switching period (local average) have been discussed in section 8.2.2 and given by (8.23). Here, that equation is re-used and adapted to single-phase condition taking into account that the inductor current is zero if the input instantaneous voltage is lower than half of the dc bus voltage. The inductor local average losses are

$$P_{L0}(\omega_m t)=\begin{cases}\underbrace{R_{L0(DC)}\left(\frac{P_{LOAD}}{v_{BUS}}k_{BOOST}\frac{\pi}{2\cos\alpha_0}\right)^2}_{LOW\ \ FREQUENCY}\\ \underbrace{+\left(R_{L0(fSW)}+R_{C(fSW)}\right)\frac{\Delta i_{REC}^2(\omega_m t)}{12}}_{HIGH\ \ FREQUENCY}\end{cases} \quad \alpha_0\le\omega_m t\le\pi-\alpha_0, \qquad \begin{matrix}0 & otherwise\end{matrix} \tag{10.22}$$

where $R_{L0(DC)}$ is the inductor winding resistance at low frequency, $R_{L0(fsw)}$ is the inductor winding resistance at the switching frequency. The resistance $R_{C(fsw)}$ is the core equivalent resistance [92]. The losses averaged over half of the mains period can be computed as

$$\begin{aligned}P_{L0(AV)}&=\frac{1}{\pi}\int_{\alpha_0}^{\pi-\alpha_0}P_{L0}(\omega_m t)d(\omega_m t)=\underbrace{R_{L0(DC)}\left(\frac{P_{LOAD}}{v_{BUS}}k_{BOOST}\frac{\pi}{2\cos\alpha_0}\right)^2\frac{\pi-2\alpha_0}{\pi}}_{LOW\ \ FREQUENCY}\\ &\underbrace{+\left(R_{L0(fSW)}+R_{C(fSW)}\right)\Delta i_{\max}^2\frac{16^2}{12\pi}\int_{\alpha_0}^{\pi-\alpha_0}\left(\frac{\sin(\omega_m t)}{k_{BOOST}}-\frac{1}{2}\right)^2\left(1-\frac{\sin(\omega_m t)}{k_{BOOST}}\right)^2 d(\omega_m t)}_{HIGH\ \ FREQUENCY}.\end{aligned} \tag{10.23}$$

Another parameter that is important for design of the boost inductor is the peak current,

$$I_{L0(PEAK)}=\frac{P_{LOAD}}{v_{BUS}}k_{BOOST}\frac{\pi}{2\cos\alpha_0}+\frac{\Delta i_{REC(\max)}}{2}. \tag{10.24}$$

10.4. The DC-DC2 Converter Operation under Single Phase Supply

The DC-DC2 converter has been analyzed in detail in chapter 8, and therefore the main part of analysis will not be repeated, except a few details that are necessary to follow the discussion.

From (10.2), (10.8) and (10.12) one can find local average value of the current $i_{2(AV)}$,

$$i_{2(AV)}(t)=i_{S0(AV)}(t)=i_{REC}(t)d(t)=$$
$$\begin{cases}\dfrac{P_{LOAD}}{v_{BUS}}k_{BOOST}\dfrac{\pi}{\cos\alpha_0}\left(1-\dfrac{\sin\omega_m t}{k_{BOOST}}\right) & \alpha_0\le\omega_m t\le\pi-\alpha_0\\ 0 & otherwise\end{cases}. \tag{10.25}$$

The switches and diodes average and RMS current over the half mains period are

$$i_{S0(AV)}=\frac{P_{LOAD}}{v_{BUS}}\left(k_{BOOST}\frac{(\pi-2\alpha_0)}{2\cos\alpha_0}-1\right), \tag{10.26}$$

$$I_{S0(RMS)}=\frac{P_{LOAD}}{v_{BUS}}\frac{\pi}{\cos\alpha_0}\frac{1}{2\sqrt{2}}\sqrt{\pi\frac{T_{S2}}{T_0}}\times\sqrt{\left(\left(\frac{2k_{BOOST}^2+1}{2}\right)(\pi-2\alpha_0)-4k_{BOOST}\cos\alpha_0+\frac{\sin 2\alpha_0}{2}\right)}. \tag{10.27}$$

The switch and diode conduction losses are

$$P_S=V_S I_{S(AV)}+r_S I_{S(RMS)}^2,$$
$$P_D=V_{DF} I_{S(AV)}+r_D I_{S(RMS)}^2, \tag{10.28}$$

where the switches and diodes are approximated by constant threshold voltage V_S and V_{DF} and dynamic resistance r_S and r_D. Switching losses are neglected since the switches commute at zero current conditions. If necessary, the losses due to the switch parasitic capacitance can be taken into account.

The resonant circuit RMS current computed over a half the mains period is

$$i_{2RMS}=\frac{P_{LOAD}}{v_{BUS}}\frac{\pi}{2\cos\alpha_0}\sqrt{\pi\frac{T_{S2}}{T_0}}\times\sqrt{\left(\left(\frac{2k_{BOOST}^2+1}{2}\right)(\pi-2\alpha_0)-4k_{BOOST}\cos\alpha_0+\frac{\sin 2\alpha_0}{2}\right)}. \tag{10.29}$$

Fig. 10.10 shows experimental waveforms of the dc bus voltage v_{BUS}, the rectifier voltage v_{REC}, and current i_{REC} and the resonant circuit current i_{2R}. Fig. 10.10 (b,c,d) shows zoom of the waveforms at different operating points; b) start of the mains diode conduction ($\omega_m t=\alpha_0$) , c) end of the mains diode conduction ($\omega_m t=\pi-2\alpha_0$), and d) peak of the rectifier voltage ($\omega_m t=\pi/2$).

10.5. The DC Bus Capacitor Design

Design of the dc bus capacitor in single-phase rectifiers is a critical design step. Unlike three-phase boost rectifiers, where the dc bus capacitor current stress is very low, the dc bus capacitor in single-phase boost rectifiers is stressed on the second harmonic. The current magnitude is order of the fundamental harmonic, even higher in case of the passive rectifier with LC filter.

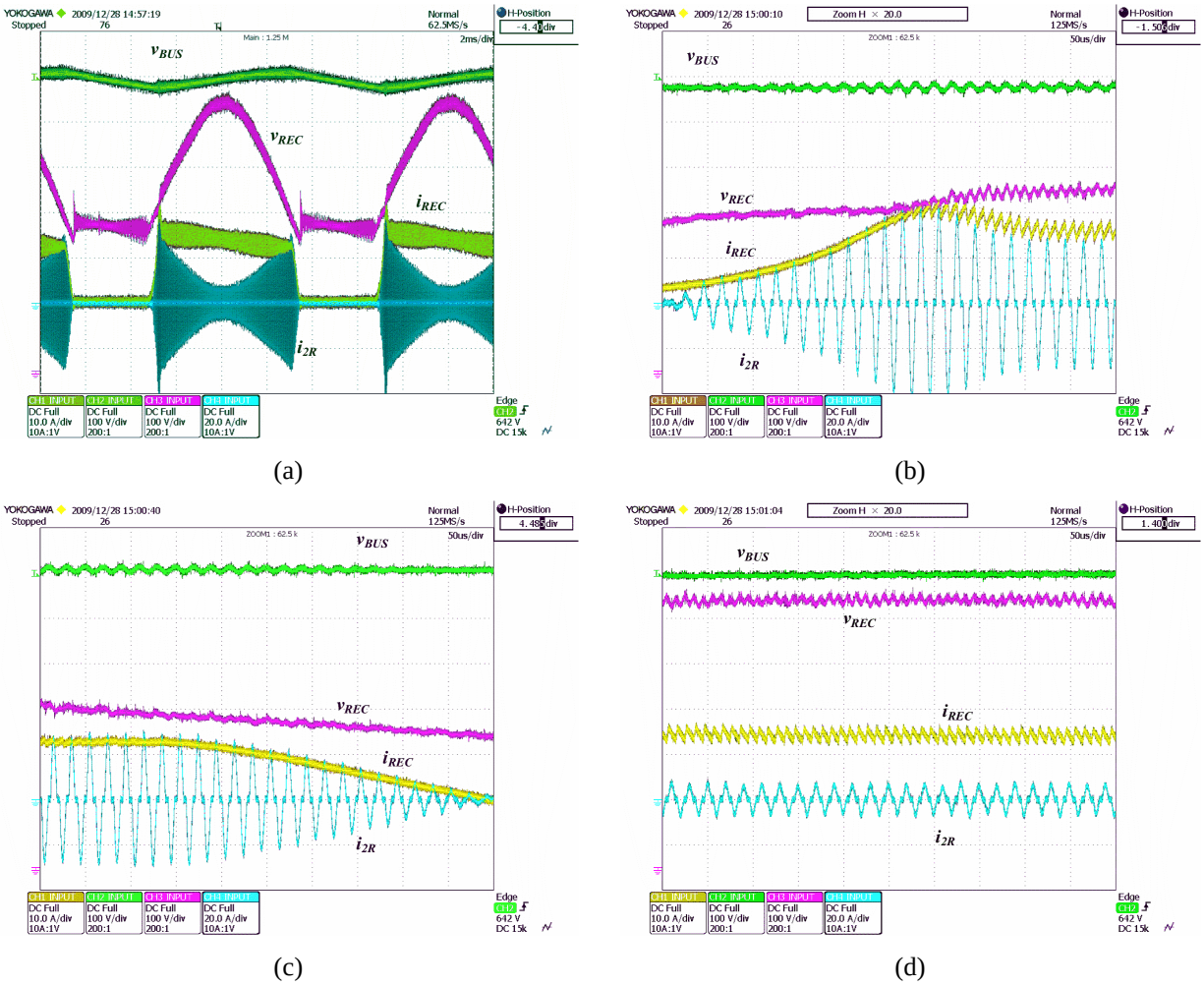


Fig. 10.10 Experimental waveforms of the rectifier voltage v_{REC} [100V/div] and current i_{REC} [10A/div], the dc bus voltage v_{BUS} [100V/div] and the resonant current i_{R2} [20V/div]. b) start of the mains diode conduction ($\omega_m t=\alpha_0$), c) end of the mains diode conduction ($\omega_m t=\pi-2\alpha_0$) and d) zoom at peak of the rectifier voltage ($\omega_m t=\pi/2$). $V_{BUS(AV)}$=650V, $V_{MAINS(RMS)}$=400V, P_{LOAD}=4000W, C_{BUS}=820µF.

The dc bus capacitor is designed for two criteria; low frequency current ripple, in this case twice the mains frequency (100Hz) and the dc bus voltage ripple. To compute the current and voltage ripple, the instantaneous power balance is used.

$$p_{IN} = v_{REC} i_{REC} = P_{LOAD} + v_{BUS} i_{CBUS} \,, \tag{10.30}$$

where i_{CBUS} is the dc bus capacitor current. It is assumed in (10.30) that instantaneous power of the capacitors C_{B1}, C_{B2} and C_S, and inductors L_0 and L_S could be neglected in comparison to the dc bus capacitor C_{BUS}. Substituting (10.6) into (10.30) yields the dc bus capacitor current

$$i_{CBUS}(t) = \frac{P_{LOAD}}{v_{BUS}} \begin{cases} \dfrac{\pi}{2\cos\alpha_0}\sin\omega_m t - 1 & \alpha_0 \le \omega_m t \le \pi - \alpha_0 \\ -1 & otherwise \end{cases}, \tag{10.31}$$

where α_0 is the threshold angle (10.3).

10.5.1. The Voltage Ripple

From (10.31) and the dc bus circuit one can write a differential equation

$$C_{BUS}\frac{dv_{BUS}}{dt}=-\frac{P_{LOAD}}{v_{BUS}} \qquad \pi-\alpha_0\le\omega_m t\le\pi+\alpha_0\,. \tag{10.32}$$

Peak-to-peak voltage ripple is computed from (10.32) as

$$\Delta v_{BUS}=\frac{P_{LOAD}}{v_{BUS(AV)}}\frac{2\alpha_0}{C_{BUS}\omega_m}\,. \tag{10.33}$$

The dc bus capacitance is computed from (10.33) as

$$C_{BUS}\ge\frac{P_{LOAD}}{v_{BUS(AV)}}\frac{2\alpha_0}{\omega_m\Delta v_{BUS(\max)}}\,, \tag{10.34}$$

where $\Delta v_{BUS\max}$ is maximum dc bus voltage ripple given as a design parameter.

Fig. 10.11 illustrates the dc bus capacitance versus the boosting factor. The capacitance is normalized on 1kW and 1V peak-to-peak ripple. This means, the value from the graph has to be multiplied by the load power in [kW] and divided by the peak-to-peak voltage ripple in [V]. For example, the boosting factor is k_{BOOST}=1.25, the power rating is P_{LOAD}=11kW and the voltage ripple is Δv_{BUS}=20V. From the graph in Fig. 10.11 it follows that the dc bus capacitance is $C_{BUS}\ge$3630μF.

10.5.2. The Capacitor Current Stress

Assuming that the dc bus voltage ripple is negligible in comparison to the average dc bus voltage, $\Delta v_{BUS}<<v_{BUS(AV)}$, we can compute the capacitor current ripple as

$$I_{CBUS(RMS)}=\frac{P_{LOAD}}{v_{BUS(AV)}}\sqrt{\left(\frac{\pi}{2\cos\alpha_0}\right)^2\left(\frac{\pi-2\alpha_0}{2\pi}+\frac{\sin 2\alpha_0}{2\pi}\right)-1}\,. \tag{10.35}$$

Fig. 10.12 illustrates the capacitor ripple current versus the boost factor. The capacitor RMS current is normalized to 1kW. Hence, to compute the absolute current ripple, the value from the graph in Fig. 10.12 has to be multiplied by the load power given in [kW].

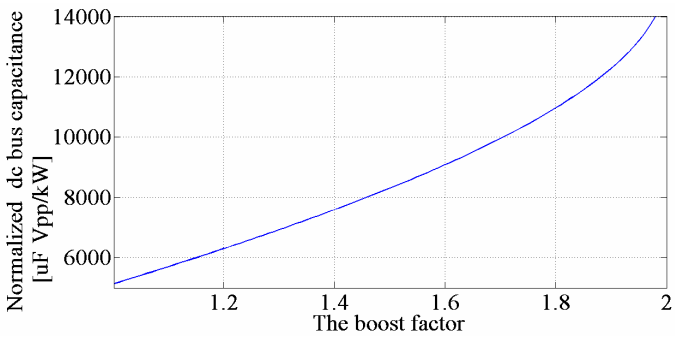


Fig. 10.11 The dc bus capacitance normalized on 1kW dc bus load and 1Vpp the dc bus voltage ripple

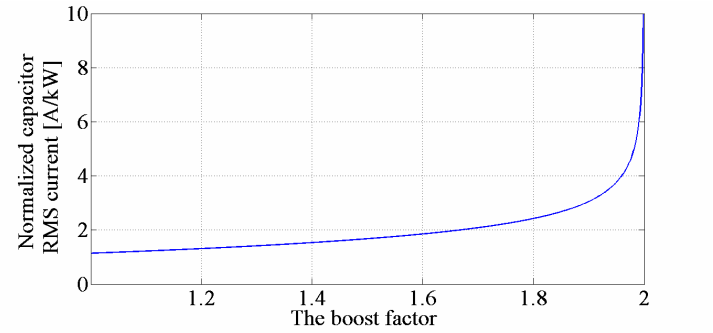


Fig. 10.12 The capacitor RMS current normalized on 1kW of the dc bus load.

11. DISCUSSION AND CONCLUSIONS

11.1. Comparison with State of the Art Solutions

In this chapter, the half-dc-bus-voltage rated boost rectifier is compared with state of the art solutions. The comparison is done for three-phase and single-phase supplied system. The size of the active components (switches and diodes), filter inductor(s) and capacitor(s) and conversion losses are compared.

11.1.1. Three Phase Operation

In this section, the new boost rectifier supplied from three-phase mains is compared with some state of the art solutions. Three parameters are compared: rating of active switches, the conversion losses and size of the passive components.

11.1.1.1. Semiconductor Switches

Like it has been done in chapter 6, the switches comparison is based on two parameters, the switch utilization factor and the switch voltage rating.

- **The Switch Utilization Factor**

The switch utilization factor of the DC-DC1 converter is computed by the definition,

$$SUF = \frac{P_{LOAD}}{S_{SW}} = \frac{P_{LOAD}}{\sum_{j=1}^{N} V_{S\max(j)} I_{S\max(j)}}. \tag{11.1}$$

In some applications, the switch apparent power can be determined as

$$S_{SW} = \sum_{j=1}^{N} V_{S\max(j)} I_{S(AV)(j)}, \tag{11.2}$$

where $I_{S(AV)}$ is the switches average current. The switch apparent power definition (11.2) could be used in resonant converters when the IGBTs are used as switches. In that case, the switches losses depend mainly on the switch average current, while the RMS and peak current have no significant influence on the losses. Definition (11.2) will be used to compute the switch utilization factor of DC-DC2.

The switch utilization factor of the new boost converter is computed from the definition (8.4), (8.30) and (8.42) as

$$SUF_{HB} = \frac{1}{\pi k_{BOOST} - 2}. \tag{11.3}$$

The switch utilization factor of the ordinary single-switch boost (SSW) converter is

$$SUF_{SSW} = \frac{3}{2\pi k_{BOOST}}. \tag{11.4}$$

Fig. 11.1 shows the switch utilization factor versus the boosting factor for the ordinary single switch boost converter, the electronic smoothing inductor (ESI) and the hybrid boost converter proposed in this dissertation. As seen, the ESI has the highest utilization factor. However, it operates only at the fixed boosting factor of 0.955. The proposed boost converter shows better switch utilization factor in entire range of the boost factor (1 to 1.73).

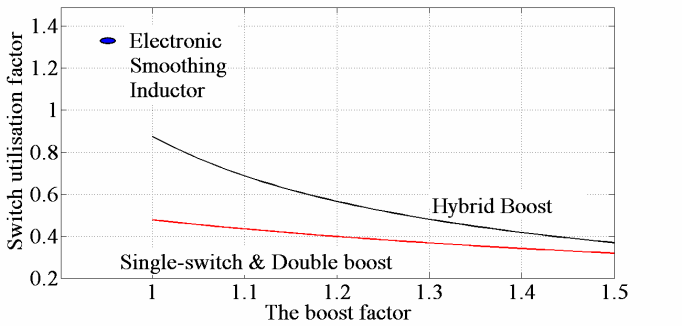


Fig. 11.1 The switches utilization factor versus boosting factor and different topologies.

o The Switches Voltage Rating

As mentioned in chapter 6, section 6.2.1.1, the switch voltage rating is a factor that cannot be compared by simple comparison of the switch utilization factor. A semiconductor switch conduction and switching performance depend strongly on the switch voltage rating and the switch technology. Lower voltage rating means lower conduction losses, better switching performance, higher efficiency and lower cost. For example, let us consider a 400V three-phase rectifier. The dc bus voltage is v_{BUS}=700 to 800V. For the ordinary single switch boost converter, the switch and boost diode voltage rating is 1000V to 1200V. For such voltage rating, 1200V IGBT and 1000V fast diode are used. In this case, maximum switching frequency is limited by the switching performance of the devices, mainly by the IGBT. To reduce switching losses, soft switching techniques are often used [57], [58]. This however requires additional passive and active components, which make the switch utilization factor even worst than (11.4). In contrast to this, in the proposed hybrid half-dc-bus-voltage rated boost rectifier, the switches and diodes voltage rating is 500V. In this case, 600V rated IGBT or 500V super junction MOSFET and ultra-fast boost diode can be used. Switching losses of 600V rated IGBT and boost diode are three to four times lower than switching losses of a 1200V rated IGBT and boost diode. Conduction losses of a 600V rated device are also lower in comparison to a 1200V rated device. If the IGBT losses are compared with high voltage MOSFETs, the difference in conduction losses is significant, because the drain source on-state resistance strongly depends on the voltage rating [41].

11.1.1.2. The Boost Inductor Size

Size of an inductor could be defined in general case as

$$size \approx L_0 I_{PEAK} I_{RMS} . \tag{11.5}$$

where L_0 is inductance at rated current, I_{RMS} the inductor RMS current and I_{RMS} is the inductor peak current.

As the inductor current is the same for the both topologies, the new one and ordinary single-switch, the inductors relative size (11.5) is ratio the inductance of half-dc-bus-voltage-rated topology to the inductance of the single-switch topology,

$$\frac{size_{(HB)}}{size_{(SSW)}} \approx \frac{L_{0(HB)} I_{PEAK(HB)} I_{RMS(HB)}}{L_{0(SSW)} I_{PEAK(SSW)} I_{RMS(SSW)}} = \frac{L_{0(HB)}}{L_{0(SSW)}}, \tag{11.6}$$

where subscript $_{(HB)}$ and $_{(SSW)}$ denote hybrid topology and single switch topology.

The inductance of the ordinary single-switch boost rectifier is computed from the current ripple

$$\Delta i_{REC} = \frac{v_{BUS}}{L_0 f_{SW}} \left(d - d^2\right), \tag{11.7}$$

where duty cycle d is

$$d(t) = \left(1 - \frac{\sin \omega_m t}{k_{BOOST}}\right)\Bigg|_{\pi/3 < \omega_m t \le 2\pi/3}. \tag{11.8}$$

Fig. 11.2 illustrates the inductor relative size (11.6) versus the boosting factor. The inductor of single-switch boost topology is taken as reference.

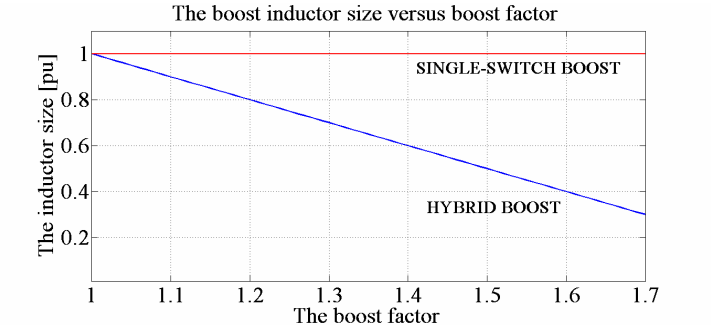


Fig. 11.2 The boost inductor relative size versus the boosting factor.

11.1.1.3. Conversion Losses

The switch losses of the ordinary single switch boost rectifier are

$$\begin{aligned} P_{S0} &= \underbrace{V_{S0} I_{S0(AV)} + r_{S0} I_{S0(RMS)}^2}_{CONDUCTION\ LOSSES} + \underbrace{\frac{P_{LOAD} k_{BOOST}}{V_N I_N} \left(E_{ON} + E_{OFF}\right) f_{SW}}_{SWITCHING\ LOSSES}, \\ P_{D0} &= \underbrace{V_{D0} I_{D0(AV)} + r_{D0} I_{D0(RMS)}^2}_{CONDUCTION\ LOSSES} + \underbrace{\frac{P_{LOAD} k_{BOOST}}{V_N I_N} E_Q f_{SW}}_{SWITCHING\ LOSSES}. \end{aligned} \tag{11.9}$$

The switch RMS and average currents are

$$\begin{aligned} I_{S0(AV)} &= \frac{P_{LOAD}}{v_{BUS}} \left(\frac{\pi}{3} k_{BOOST} - 1\right), \\ I_{S0(RMS)} &= \frac{P_{LOAD}}{v_{BUS}} \frac{\pi}{3} k_{BOOST} \sqrt{1 - \frac{3\sqrt{3}}{\pi k_{BOOST}}}. \end{aligned} \tag{11.10}$$

The diode average and RMS currents are

$$I_{D0(AV)} = \frac{P_{LOAD}}{v_{BUS}},$$
$$I_{D0(RMS)} = \frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \frac{\pi}{3} \sqrt{\frac{3\sqrt{3}}{\pi k_{BOOST}}}. \quad (11.11)$$

TABLE 11-1 shows parameters of the boost switch and diode used in the ordinary single-switch boost rectifier. The rectifier specification (power, voltage and switching frequency) is the same as for the new boost rectifier, TABLE 8-2.

TABLE 11-1: Specification of the switch and diode for the ordinary 5.5kW single switch boost rectifier.

S_0: MOSFET 1000V 20A			D_0: FAST DIODE 1000V 20A		
V_{S0}	r_{S0}	$*E_{ON}+E_O$	V_{D0}	r_{D0}	$*E_Q$
0	600mΩ	30µJ/A	1.25 V	15 mΩ	15µJ/A
*Switching losses at V_N=600V T_J=150˚C					

Fig. 11.3 shows ratio of the total losses of the proposed topology to the losses of a standard single switch boost converter. Note that the relative losses vary between 50% and 95%, depending on the conversion power P_{LOAD} and boost factor. This result clearly illustrates advantage of the proposed solution in comparison with state of the art solutions.

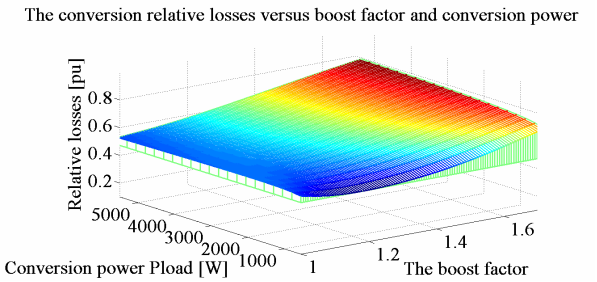


Fig. 11.3 Comparison of the conversion losses of the proposed boost rectifier versus an ordinary single-switch boost rectifier. v_{BUS}=650V. The losses were computed from the losses model (8.33), (8.43) and (11.9).

11.1.2. Single Phase Operation

In this section, the new boost rectifier operating in single-phase supply mode will be compared with two state of the art solutions, single-switch boost rectifier and the ordinary diode rectifier. Size of the boost inductor and the switch utilisation factor will be compared for the new boost rectifier and the ordinary single switch rectifier. The mains current quality and the dc bus capacitor current and losses are compared for the presented rectifier and diode rectifier with passive *LC* filter.

11.1.2.1. The Boost Inductor Size

The inductor peak and RMS current for single-switch boost topology are

$$I_{RMS(SSW)} = \frac{P_{LOAD}}{v_{BUS}} k_{BOOST} \sqrt{2}$$
$$I_{PEAK(SSW)} = \frac{P_{LOAD}}{v_{BUS}} k_{BOOST} 2 \quad . \tag{11.12}$$

Using (8.20), (10.8), (10.10) and (11.12) one can compute relative size of the proposed boost rectifier

$$relative\ size = \frac{sizeL_{0(HB)}}{sizeL_{0(SSW)}} = \frac{1}{16\sqrt{2}} \left(\frac{\pi}{\cos\alpha_0} \right)^2 \sqrt{\frac{\pi - 2\alpha_0}{\pi}} \ , \tag{11.13}$$

where subscripts *(HB)* and *(SSW)* denote the hybrid boost rectifier and the single switch boost rectifier.

Fig. 11.4 shows relative size of the boost inductor (comparison of the inductor for the proposed boost rectifier and the ordinary single switch boost rectifier) versus the boost factor. The inductor is approximately 50% at minimum boost factor $k_{BOOST}=1$ and approximately 95% at maximum boost factor $k_{BOOST}=1.7$.

11.1.2.2. The Switches Utilization Factor

The switch utilization factor of the hybrid boost converter is computed from the definition (6.1) as

$$SUF_{HB} = \frac{2\cos\alpha_0}{\pi k_{BOOST} + 2\left(k_{BOOST}(\pi - 2\alpha_0) - 2\cos\alpha_0\right)} . \tag{11.14}$$

The switch utilization factor of the ordinary single-switch boost converter is

$$SUF_{SSW} = \frac{1}{4 k_{BOOST}} \tag{11.15}$$

Fig. 11.5 shows the switch utilisation factor plotted versus the boost factor. Note that the proposed topology has greater the switch utilisation factor than the ordinary single-switch boost converter if the boost factor is lower than 1.55. When the boost factor is greater than 1.55, the ordinary single-switch topology has slightly greater switch utilisation factor than the new one.

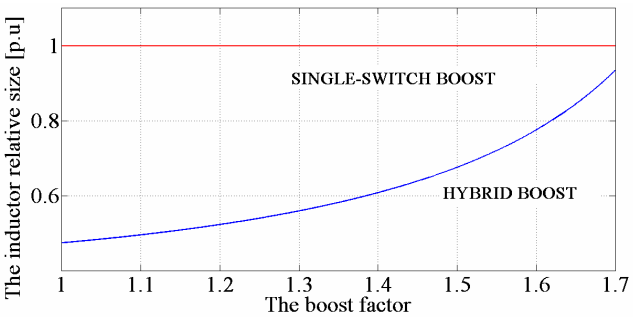


Fig. 11.4 The boost inductor size versus the boost factor. The inductor size is normalized on the single-switch boost inductor size.

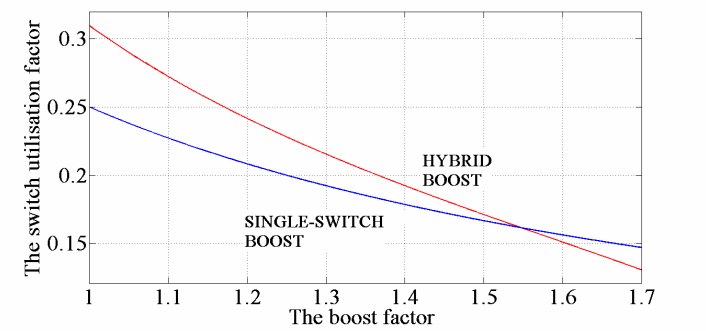


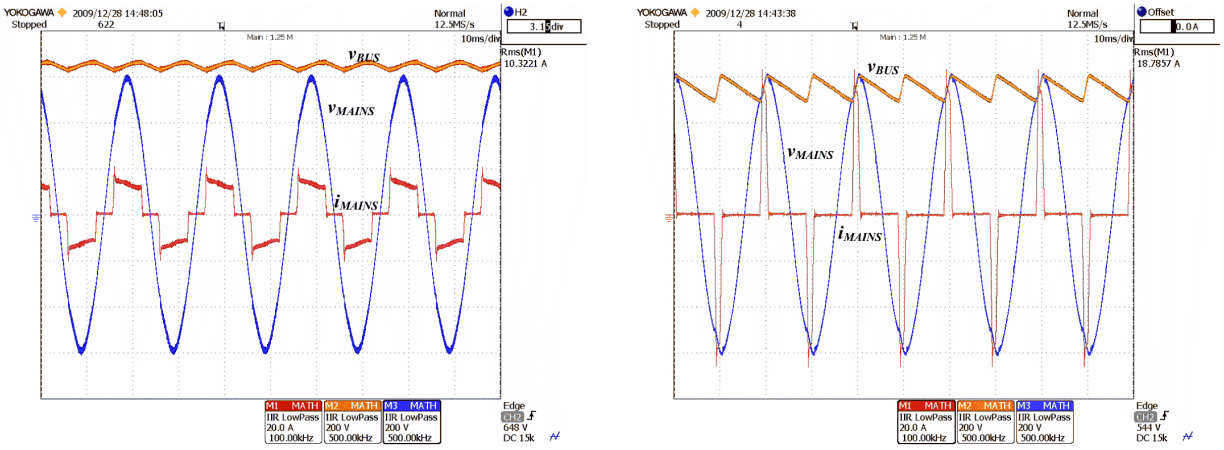
Fig. 11.5 The switch utilization factor versus the boost factor.

11.1.2.3. The Mains Current Quality and DC Bus Capacitor Stress

Fig. 11.6 shows waveforms of the mains voltage and current and the dc bus voltage when the proposed boost rectifier is used, Fig. 11.6 (a) and the ordinary diode rectifier with capacitive filter is used, Fig. 11.6 (b). The waveforms are recorded at power of 4000W. The most important parameters are summarized in TABLE 11-2. P_{CBUS} is the dc bus capacitor losses computed from the capacitor RMS current and equivalent series resistance (ESR) given as data sheet parameter.

TABLE 11-2: Comparison of the ordinary diode rectifier and the proposed boost rectifier.

	Diode rectifier with passive LC filter	**The new boost rectifier**
$I_{mains(RMS)}$	**18.8 A**	**10.3 A**
$I_{mains(PEAK)}$	**60 A**	**15 A**
THDi	**170 %**	**45 %**
Δv_{BUS}	**100 V**	**35 V**
$I_{CBUS(RMS)}$	**17.7 A**	**5.4 A**
P_{CBUS}	**62.5 W**	**5.8 W**



(a) (b)

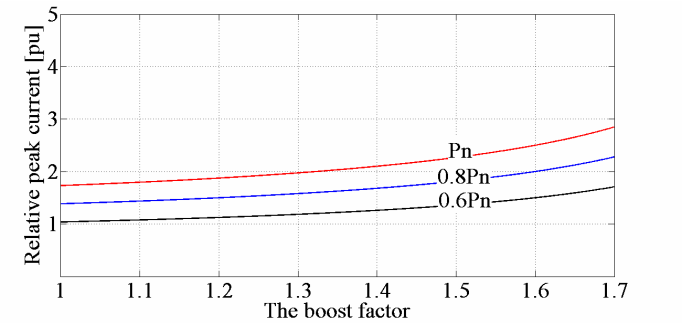
Fig. 11.6 a) Experimental waveforms of the mains phase-to-phase voltage v_{MAINS} [200V/div], the dc bus voltage v_{BUS} [200V/div] and the mains current i_{MAINS} [20A/div] when the drive is single-phase supplied. a) The drive with the proposed topology, and b) a drive with diode rectifier and passive LC filter. $V_{BUS(AV)}$=650V, $V_{MAINS(RMS)}$=400V, P_{LOAD}=4000W, C_{BUS}=820µF.

11.2. Three Phase versus Single Phase Supply

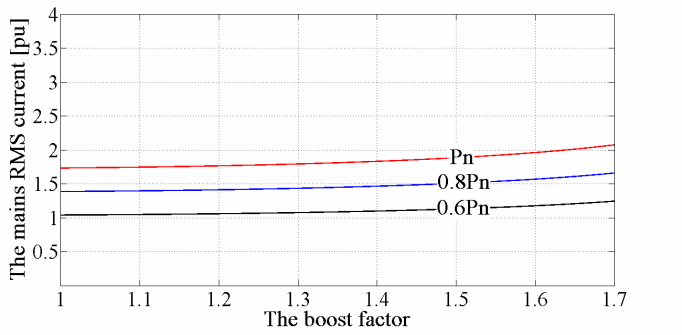
Very often, a variable speed drive is designed to operate in three-phase as well as in single-phase supply mode. In this section, the hybrid boost rectifier supplied from three-phase and single-phase mains is discussed. The following parameters are compared: The mains peak and RMS current, the switches and diodes losses, and size of the boost inductor.

11.2.1. The Mains Current

Equations for the relevant variables (peak, average and RMS currents) of three-phase supplied diode boost rectifier have been developed in chapter 8. Those equations are re-used and relative currents are computed. The relative currents are computed as ratio of the currents of single-phase supplied rectifier to the currents of the three-phase supplied rectifier. The currents for single-phase supply are computed at three different loads: nominal (Pn), 80% of nominal (0.8Pn) and 60% of nominal (0.6Pn).



(a)



(b)

Fig. 11.7 a) The mains peak current and b) RMS current versus the boost factor. The currents are computed as ratio between currents of single-phase supplied rectifier at different load (Pn, 0.8Pn and 0.6Pn) and three-phase supplied rectifier at nominal load (Pn).

Fig. 11.7 shows the mains peak current and RMS current versus boost factor. Please notice that RMS and peak current increase with the boost factor. At nominal power, single-phase supplied rectifier draws 73% more current at minimum boost factor. This is the factor of $\sqrt{3}$, which is ratio of single-phase to three-phase current at the same power.

11.2.2. The Switches Losses

The switch losses are computed from (10.17), (10.18) and (10.21) and compared with the losses of three-phase supplied rectifier (8.33), (8.35) and (8.43). Fig. 11.8 shows the relative power losses that are computed as ratio of power losses of three-phase supplied rectifier to the single-phase supplied rectifier at different load (nominal, 80% of nominal and 60% of nominal). At nominal power, the losses are approximately 10% greater than that of three-phase supplied rectifier if the boost factor is lower than 1.3. At maximum boost factor, the losses are approximately 30% greater.

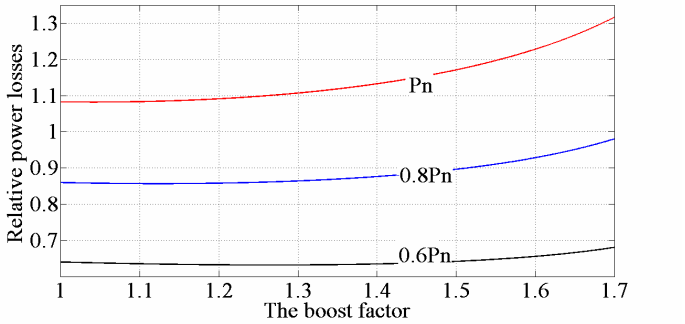


Fig. 11.8 Relative power losses versus the dc bus load. The power losses are computed as ratio of the power losses of single-phase supplied rectifier at different load (Pn, 0.8Pn and 0.6Pn) to the three-phase supplied rectifier at nominal load (Pn).

11.2.3. The Inductor Size

The size of the boost inductor for single-phase and three-phase supplied rectifier can be compared using the same method that was used in section 11.1.1.2. From (8.4), (8.20) and (10.8) one can define the inductor relative size as

$$relative\ size = \frac{size_{(SP)}}{size_{(TP)}} = \left(\frac{P_{LOAD(SP)}}{P_{LOAD(TP)}}\right)^2 \frac{9}{4(\cos\alpha_0)^2}\sqrt{\frac{\pi - 2\alpha_0}{\pi}}\,, \tag{11.16}$$

where subscripts $_{(SP)}$ and $_{(TP)}$ denote single-phase and three-phase. $P_{LOAD(SP)}$ is load of single-phase supplied rectifier and $P_{LOAD(TP)}$ is load of single-phase supplied rectifier. The inductor relative size versus the boosting factor is plotted in Fig. 11.9.

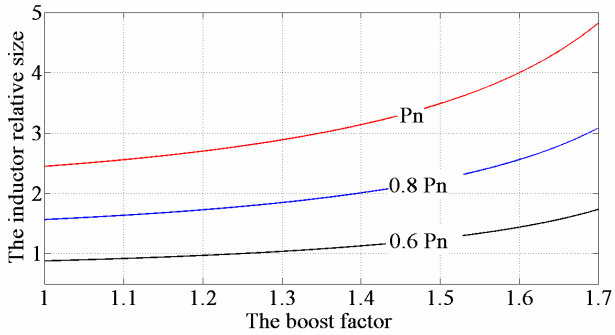


Fig. 11.9 Relative size of the boost inductor. The size is computed as ratio of the size of single-phase supplied rectifier at different load (Pn, 0.8Pn and 0.6Pn) to three-phase supplied rectifier at nominal load (Pn).

11.3. Conclusions

A novel three-phase diode boost rectifier based on the half-dc-bus-voltage-rated topology has been proposed and discussed in part three of the dissertation. The topology has been extensively analysed and some design guidelines given. Modelling aspects and the control scheme have been given too. The proposed topology including control scheme has been verified by Matlab/Simulink simulation and a set of experiments on a laboratory prototype. The simulation and experimental results has confirmed theoretical analysis. Single-phase operation of the proposed boost rectifier has been discussed and experimentally verified too.

The advantages of the proposed solution over single-switch and double boost rectifier are:

- Power semiconductor switche size and losses. The switches utilization factor of the new boost rectifier is higher than that of the state of the art solutions. This means that the switch cost is lower. The switch voltage rating is half of that of the single-switch boost rectifier. Therefore, better and more efficient devices could be used.
- The passive power components size and losses. The boost inductor is smaller than the inductor of single-switch boost rectifier. Thus, the inductor losses are reduced by factor 1.5 to 2. However, in comparison to the double-boost topology, the inductor of the proposed rectifier is slightly bigger.

Regarding the mains current quality and the dc bus voltage boost, there is not a difference between the new topology and state of the art single-switch and double boost topology. The mains current is square waveform with conduction angle of $2\pi/3$ radians, while the dc bus voltage is boosted and actively controlled. However, compared to the state of the art passive diode rectifier, the current shape is significantly better. THD is approximately 30% instead of 100 to 150%, while the peak and RMS current are reduced by factor of 3.5 and 1.5. The dc bus voltage quality is better too in comparison to simple diode rectifier.

A disadvantage of the proposed boost rectifier is need for an auxiliary dc-dc converter to control the capacitors mid point voltage. The auxiliary converter is rated at a fraction of the conversion power. Therefore, the losses of that auxiliary converter can be quite low in comparison to the total conversion losses [116]. It will be shown in chapter 12 that the auxiliary converter can be re-used as a part of the interface dc-dc converter that has been discussed in chapter 4.

The proposed boost rectifier can effectively be a replacement for passive diode rectifiers as well as single-switch and double boost rectifier.

PART FOUR: THREE-TERMINAL ENERGY STORAGE AND PFC DEVICE

12. THE PRINCIPLE

12.1. Introduction

As discussed in the part two and three of the dissertation, some technical issues in application of modern controlled electric drives are still challenging issues. The following issues are identified as the most critical issues:

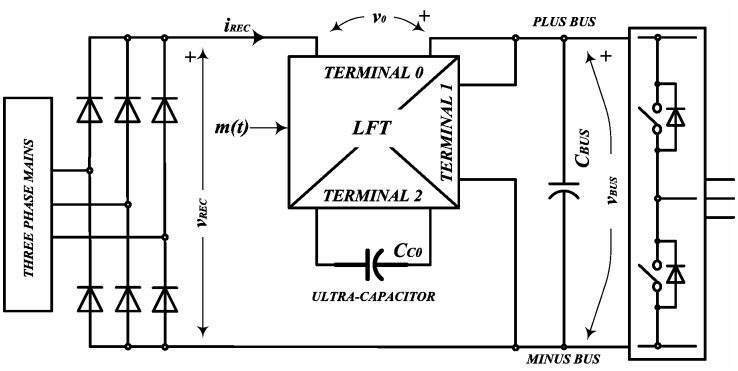
1) Saving of the drive system braking energy,
2) The system immunity on the mains power supply interruption,
3) The drive input current quality,
4) The drive dc bus voltage control and stability,
5) Single-phase supply, and
6) Reduction of the mains peak power.

The issues 1 and 2 have been discussed and a new solution proposed in the part two, chapters 3 to 6. The issues 3 to 5 have been discussed and a new solution proposed in the part three, chapters 7 to 11. In the part four, a solution for the six issues is discussed.

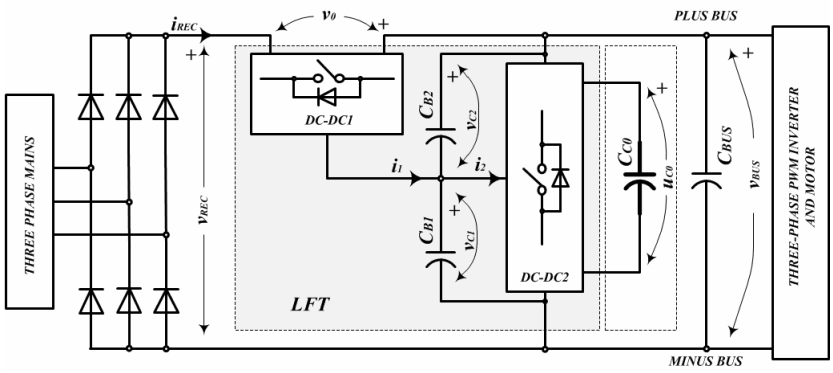
The three-terminal energy storage and power factor correction device is proposed as a solution to solve the above-mentioned issues. In chapter 12, the three-terminal energy storage and power factor correction (PFC) device is analysed and some design guidelines are given. The model and control aspects are discussed in chapter 13. The proposed solution is validated by Matlab/Simulink simulation and a set of experiments on a 5.5kW laboratory prototype. The results are presented and discussed.

12.2. The Principle

The basic principle of the proposed regenerative electric drive with the three-terminal energy storage and PFC device is illustrated in Fig. 12.1 (a). One can distinguish three-phase diode rectifier, dc bus capacitor C_{BUS}, dc bus load, storage capacitor C_{C0} and the three-terminal power converter designated as the loss-free transformer (LFT). The terminal 0 is connected between the rectifier and the dc bus plus rail, the terminal 1 is connected in parallel with the dc bus, and the terminal 2 is connected on the storage capacitor C_{C0}. The storage capacitor is an electrical double layer capacitor (EDLC), well know as the ultra-capacitor. The LFT is controlled by a control variable $m(t)$. Internal structure of the LFT is depicted in Fig. 12.1 (b). The LFT is composed of two dc-dc converters, namely DC-DC1 and DC-DC2, and two series connected capacitors C_{B1} and C_{B2}. Role of the DC-DC1 converter is to generate the voltage v_0 in order to regulate the rectifier current i_{REC} and boost the dc bus voltage v_{BUS}. The DC-DC2 converter has two roles. The first one is to assist to the DC-DC1 converter when the drive is supplied from the mains. More precisely, the DC-DC2 converter has the role to maintain the voltage v_{C1} and v_{C2} in a constant ratio $v_{C1}=v_{C2}=v_{BUS}/2$. The second role of the DC-DC2 converter is to be the interface between the ultra-capacitor C_{C0} and the drive when the drive operates in the braking mode or the ultra-capacitor motoring mode [48].



(a)



(b)

Fig. 12.1 a) Regenerative three-phase variable speed drive with the dc bus voltage boost function using the three-terminal loss-free transformer (LFT) with energy storage. b) Realization using two dc-dc converters and an ultra-capacitor.

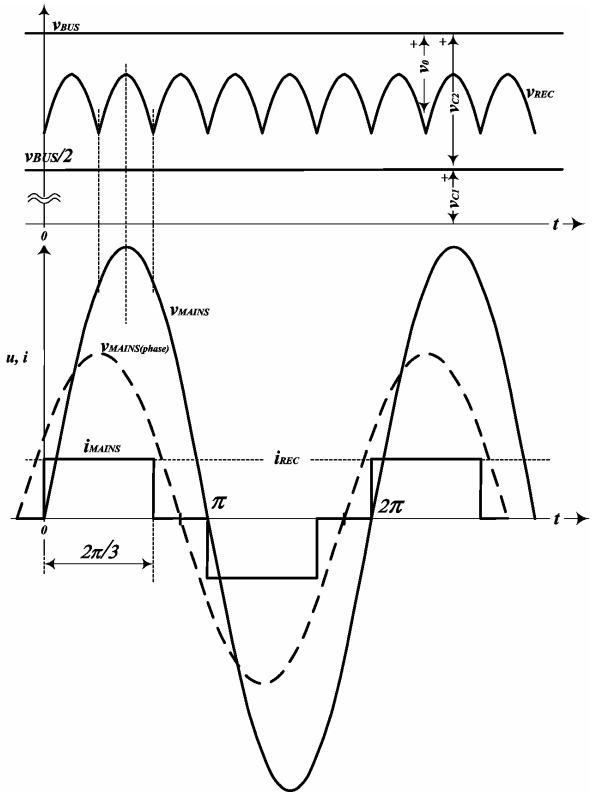


Fig. 12.2 The rectifier voltage v_{REC}, the dc bus voltage v_{BUS}, the mains voltage v_{MAINS} and current i_{MAINS}.

12.2.1. The System Operating Modes

A controlled electric drive with the ultra-capacitor energy storage device may operate in several different modes, depending on the drive load and status of the mains. The operating modes are described hereafter. Fig. 12.3 shows the power-flow diagrams, and Fig. 12.4 shows the waveforms for different operating modes. The signification of the voltages V_{BUSmax}, $V_{BUS(REF)}$, V_{BUSmin}, U_{C0max}, U_{C0inM} and U_{C0min} that appear in Fig. 12.4 is discussed later on in the following section.

a) Motoring mode from the mains (**MM**). The drive is supplied from the mains and running in the motoring mode. The input and output power are equal, $P_{IN}=P_{OUT}$. The power ΔP circulates between the converters DC-DC2 and DC-DC1. This circulating power contributes boosting and control of the dc bus voltage v_{BUS}. The ultra-capacitor power is $P_{C0}=0$ and the ultra-capacitor voltage is constant $u_{C0}=U_{C0inM}$. The DC-DC1 actively regulates the dc bus voltage to the reference $V_{BUS(REF)}$, where the reference is higher than the mains phase to phase peak voltage.

b) Braking-energy storing mode (**B**). The drive runs in braking mode. The braking energy is stored in ultra-capacitor C_{C0} via the converter DC-DC2. The drive input power is $P_{IN}=0$. The ultra-capacitor power P_{C0} is positive according to the diagram, Fig. 12.3. The ultra-capacitor voltage increases towards U_{C0max}. The DC-DC2 converter actively regulates the dc bus voltage to the reference V_{BUSmax}.

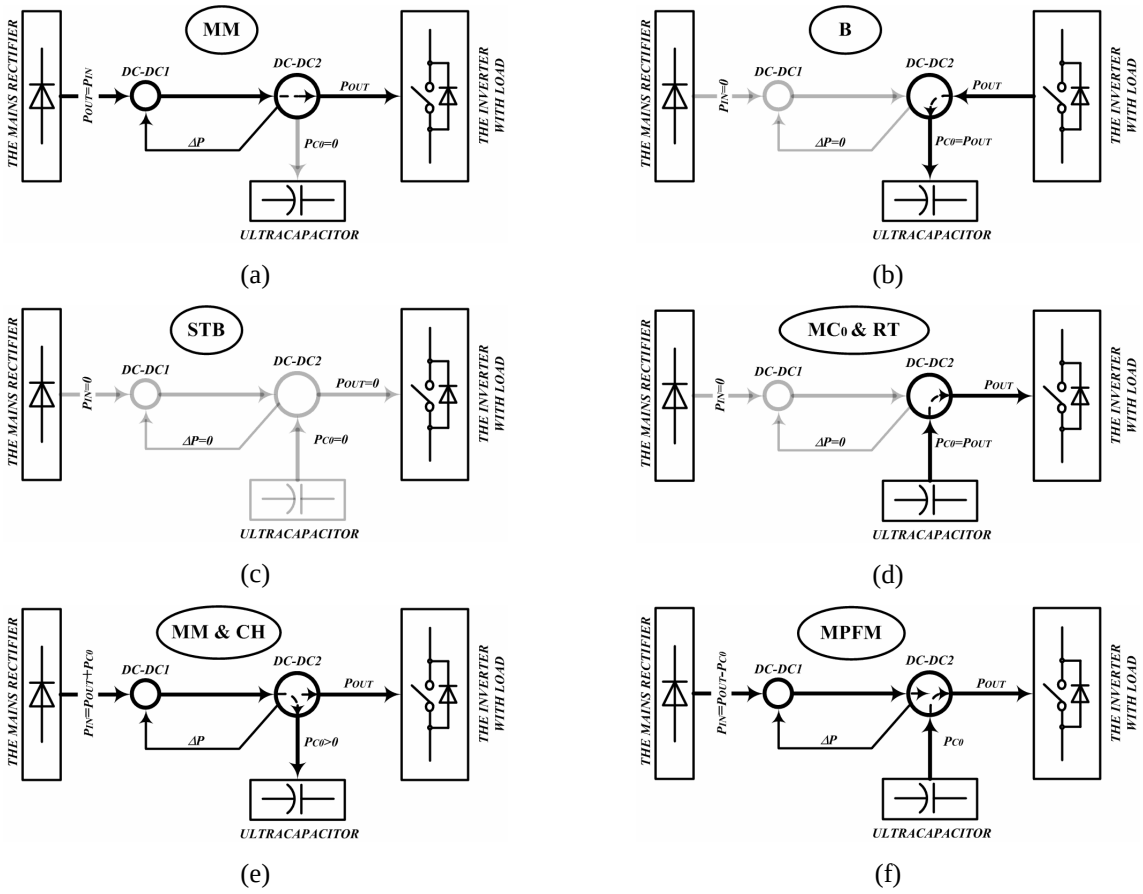


Fig. 12.3 Power flow for different operating modes a) the mains motoring mode (MM), b) barking mode (B), c) stand by mode (STB), d) energy recovery mode (MC0) and ride-through mode (RT), e) the ultra-capacitor charging mode (MM-CH) and f) the mains peak power filtering mode (MPFM).

c) Standby mode (**STB**). The drive is in the standby mode, and no energy flow between the input, output and the ultra-capacitor. The DC-DC2 converter actively regulates the dc bus voltage to the reference V_{BUSmax}.

d-1) Motoring-energy recovery mode (**MC$_0$**). The drive operates in motoring mode. The energy required for the drive acceleration is recovered from the ultra-capacitor via the converter DC-DC2. The power P_{C0} is negative and the ultra-capacitor voltage decreases towards U_{C0inM}. The DC-DC2 converter actively regulates the dc bus voltage to the reference V_{BUSmax}.

d-2) The ride-through operation mode (**RT**). The mains supply is interrupted, and therefore the drive is supplied from the ultra-capacitor via the power converter DC-DC2. The power P_{C0} is negative and the ultra-capacitor voltage decreases towards U_{C0min}. The DC-DC2 converter actively regulates the dc bus voltage to the reference V_{BUSmin}.

e) The ultra-capacitor charging mode (**MM-CH**). The mains supply is recovered and then the ultra-capacitor is charged to the pre-defined intermediate voltage $u_{C0}=U_{C0inM}$. The DC-DC1 converter actively regulates the dc bus voltage to the reference $V_{BUS(REF)}$.

f) The mains peak power filtering mode (**MPFM**). The drive operates in the mains motoring mode. If the load high during a short period, the input power is limited and the drive load is supplied from the ultra-capacitor. Once the load is reduced, the ultra-capacitor is re-charged from the mains.

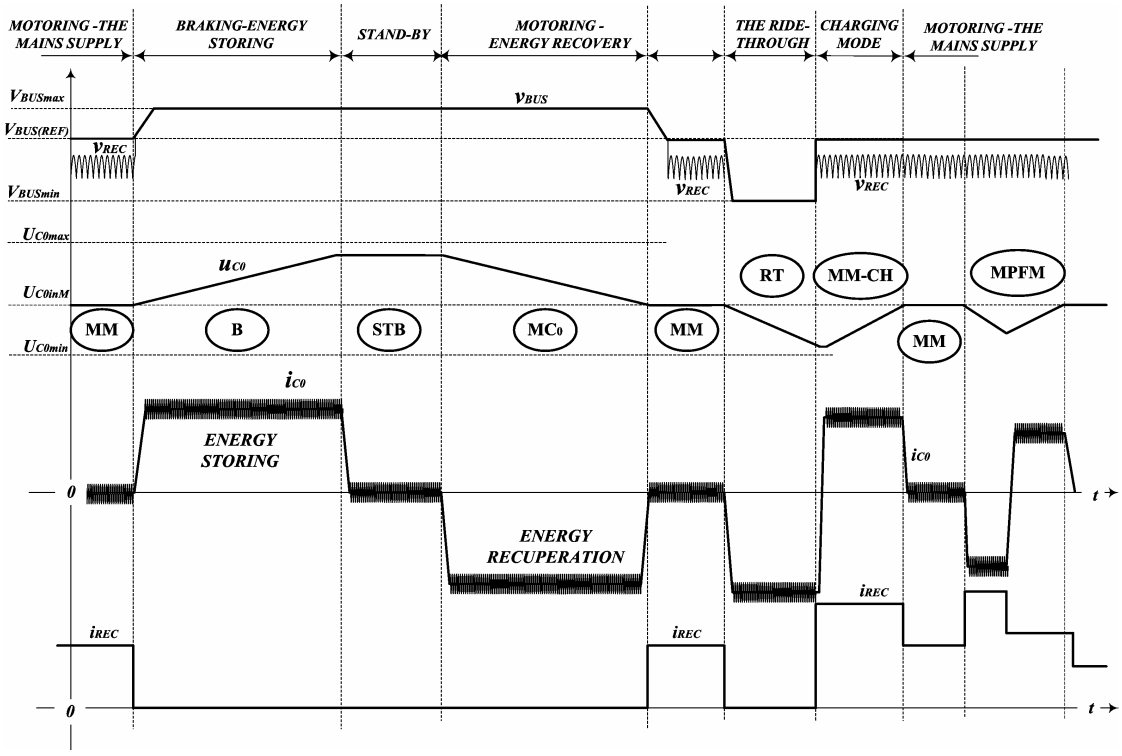


Fig. 12.4 Waveforms at different operating modes of the drive system: the mains motoring mode (MM), braking mode (B), stand by mode (STB), energy recovery mode (MC_0) and ride-through mode (RT), e) the ultra-capacitor charging mode (MM-CH) and the mains peak power filtering mode (MPFM).

12.2.2. The DC Bus Voltage Reference

Fig. 12.5 illustrates the signification of the reference voltages V_{BUSmax} $V_{BUS(REF)}$ and V_{BUSmin}. The OBF signifies Over-Braking Fault, and USF signifies Under Supply Fault. When the system operates in the mains motoring mode, the dc bus voltage is regulated to the reference $V_{BUS(REF)}$ that must be greater than the maximum of the supply voltage (to be able to control the rectifier current). In order to avoid unnecessary charge and discharge of the ultra-capacitor, the dc bus voltage references V_{BUSmin} and V_{BUSmax} must stay outside of the normal operation range, as shown in Fig. 12.5. On other side, to prevent the system fault, either OBF or USF, the dc bus voltage references must not be in the forbidden regions. Therefore, the reference V_{BUSmin} is located within an interval [*USF*, *Min Input Voltage*] while the reference V_{BUSmax} is located within an interval [$V_{BUS(REF)}$, OBF]. The reference V_{BUS} is located within an interval [*Max Input Voltage*, OBF].

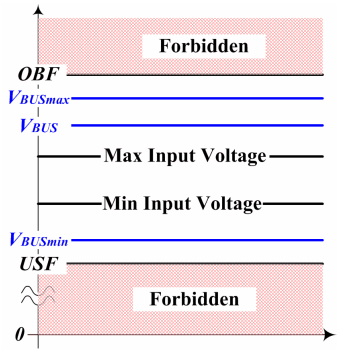
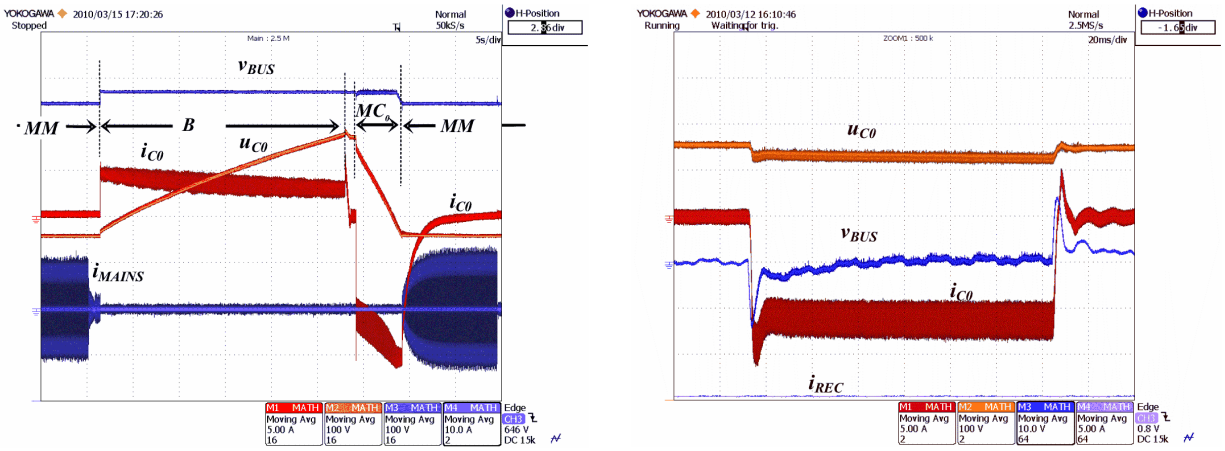


Fig. 12.5 Definition of the reference voltages V_{BUSmax}, $V_{BUS(REF)}$ and V_{BUSmin}.

Fig. 12.6 illustrates the capability of the drive system to store and recover the braking energy. Waveforms of the dc bus voltage v_{BUS}, the rectifier current i_{REC}, the ultra-capacitor current i_{C0} and voltage u_{C0} when the drive operates in motoring/braking/motoring cycle are shown. The drive runs in the motoring mode (**MM**) and is supplied from the mains. The ultra-capacitor voltage is U_{C0inM}, while the dc bus voltage is regulated to the reference $V_{BUS(REF)}$. Once the drive load becomes negative, the drive starts the braking phase (**B**) and the energy is transferred from the load to the drive dc bus. The dc bus voltage v_{BUS} elevates towards the upper reference V_{BUSmax} and then stays regulated to that level. At the same time, the input current i_{MAINS} falls to zero. The ultra-capacitor voltage increases and the current decreases since the charging/discharging power is assumed constant. When the braking phase is finished, the drive load becomes again positive and the drive turns to motoring mode again (**MC$_0$**), but this time supplied from the ultra-capacitor. The current i_{C0} turns negative and the voltage u_{C0} starts to decrease towards the reference U_{C0inM}. Once the ultra-capacitor voltage reaches the reference U_{C0inM}, the current drops to zero and the dc bus voltage falls to the nominal value V_{BUS}. The ultra-capacitor discharge phase is finished and the drive is supplied from the mains again (**MM**).

Fig. 12.7 illustrates the drive immunity on the mains short interruption. The drive runs in the mains motoring mode (**MM**), and at some instant the mains is interrupted. The dc bus voltage falls to the minimum V_{BUSmin}, and stays at that level regulated by the dc bus voltage controller. The drive is in the ride-through mode (**RT**), being supplied from the ultra-capacitor. The ultra-capacitor voltage decreases below U_{C0inM} towards U_{Cimin}. Once the mains

is recovered after 1.5s, the ultra-capacitor is re-charged to U_{C0inM}. This is the mains motoring and charging mode (**MM-CH**).



(a) (b)

Fig. 12.6 a) Experimental waveforms of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div], the dc bus voltage v_{BUS} [100V/div] and the mains current i_{MAINS} [5A/div] during an entire braking-motoring cycle of the drive system. b) Zoom of transition from stand-by to the ultra-capacitor motoring mode and stand by mode. The ultra-capacitor voltage is approximately U_{C0}=550V. The rectifier current i_{REC} is shown instead of the mains current i_{MAINS}.

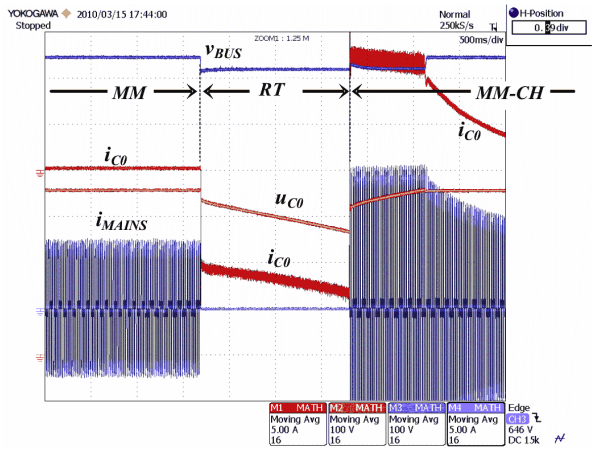
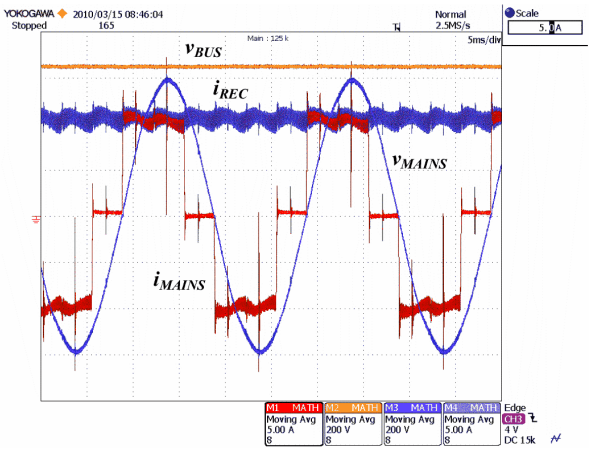


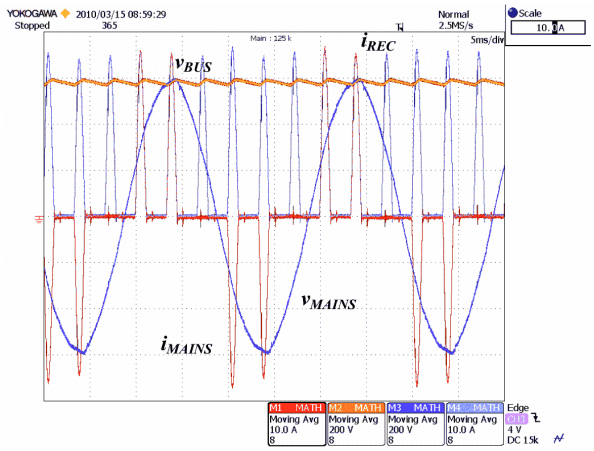
Fig. 12.7 Experimental waveforms of the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div], the dc bus voltage v_{BUS} [100V/div] and the mains current i_{MAINS} [5A/div] during the mains interruption.

Fig. 12.8 (a) illustrates the system capability to control the dc bus voltage and reduce distortion of the mains current. Waveforms of the dc bus voltage v_{BUS}, the mains phase-to-phase voltage v_{MAINS}, the rectifier current i_{REC} and the mains current i_{MAINS} are shown. The mains current is a square waveform of $2\pi/3$ radians with magnitude of approximately 10A. The RMS current is 8.28A RMS. The dc bus voltage is constant and ripple-free. More details of control performance in presence of step variation of the load are discussed in the following chapter. For comparison, the waveforms of the standard diode rectifier are shown in Fig. 12.8 (b). The mains current amplitude spectrais is shown in Fig. 12.8. (c). The current total harmonic distortion factor (THD) is 29.5% and partially weighted harmonic distortion factor

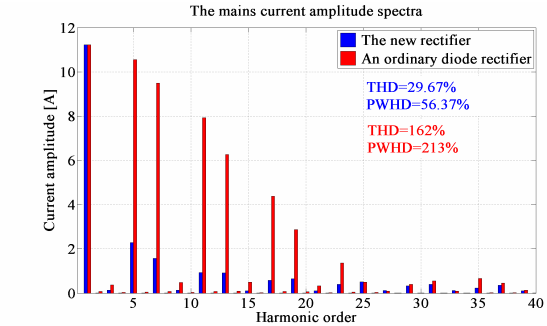
(PWHD) is 54%. The THD is lower than the requirement, of 48%, [13]. However, the PWHD is slightly higher than the limit of 46%, defined by the standard [13].



(a)

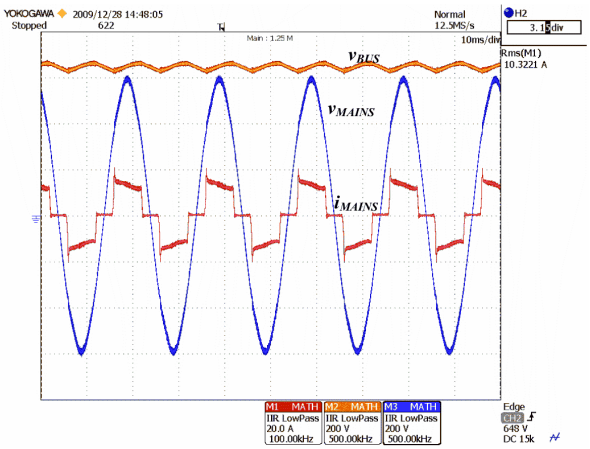


(b)

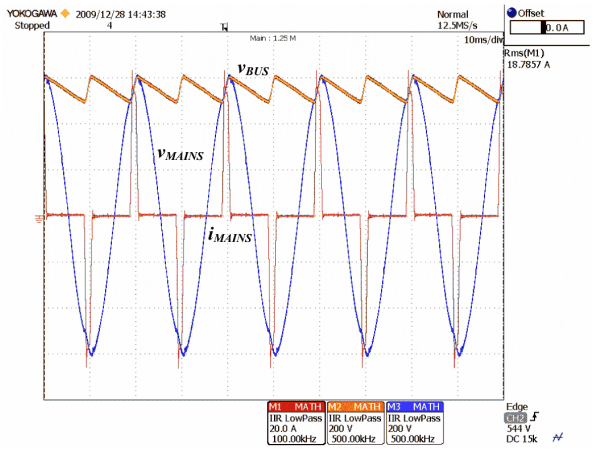


(c)

Fig. 12.8 a) Experimental waveforms of the mains phase-to-phase voltage v_{MAINS}, the dc bus voltage v_{BUS} [200V/div], the rectifier current i_{REC} and the mains current i_{MAINS} [10A/div] when the drive operates in the mains motoring mode (MM). b) The same waveforms when a standard diode rectifier is used. The mains current scale is [10A/div]. c) The mains current amplitude spectra. The red bars are current spectrum of a standard diode rectifier and the blue bars are current spectra of the new drive rectifier. V_{BUS}=650V, V_{MAINS}=400V P_{LOAD}=5500W.



(a)



(b)

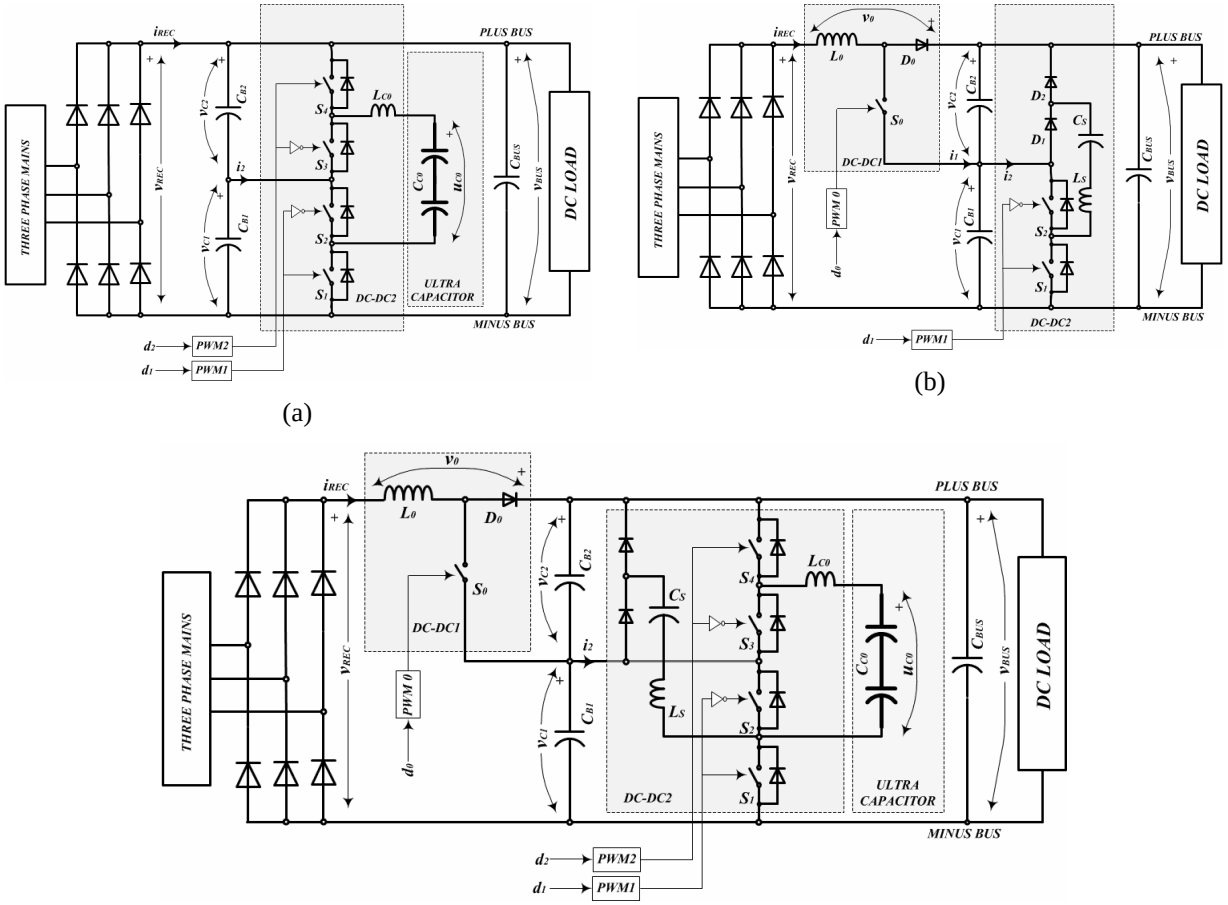
Fig. 12.9 a) Experimental waveforms of the mains phase-to-phase voltage v_{MAINS}, the dc bus voltage v_{BUS} [200V/div], the rectifier current i_{REC} and the mains current i_{MAINS} [20A/div] when the drive is single-phase supplied. a) The drive with the proposed topology, and b) a drive with diode rectifier and passive filter. $V_{BUS(AV)}$=650V, $V_{MAINS(RMS)}$=400V, P_{LOAD}=4000W, C_{BUS}=820µF.

Fig. 12.9 illustrates the drive capability to run on single-phase supply. It could be degradation of the mains supply (one phase lost) or the application requirement (rural area without three phase supply). The waveforms of the mains voltage and current and the dc bus voltage are shown. Fig. 12.9 (a) illustrates waveforms when the proposed solution is used and Fig. 12.9 (b) illustrates waveforms when a standard diode rectifier is used. The waveforms are recorded at nominal power of 4000W. Note significant difference in the mains peak and rms current and also the dc bus voltage ripple.

12.3. Three-terminal Energy Storage and Power Factor Correction Device

12.3.1. Basic Principle

Realisation of the three-terminal energy storage and power factor correction device is discussed in this section. Fig. 12.10 (a) shows circuit diagram of the solution that was proposed and discussed in part two of the dissertation. Fig. 12.10 (b) shows circuit diagram of the solution that was proposed and discussed in part three of the dissertation. Combining those two solutions into one, yields a solution that solves all the problems mentioned in the introduction, section 12.1. Circuit diagram is depicted in Fig. 12.10 (c).



(a) (b)

(c) **A+B=C**

Fig. 12.10 Evolution of the three-terminal energy storage and PFC device. a) Topology of parallel connected ultra-capacitor and interface dc-dc converter, b) half-dc-bus-voltage rated boost rectifier, and c) energy storage end PFC device as a combination of the previous two topologies.

Note that this circuit corresponds to circuit of Fig. 12.1 (b) (the DC-DC1 converter, two series connected capacitors and the DC-DC2 converter).

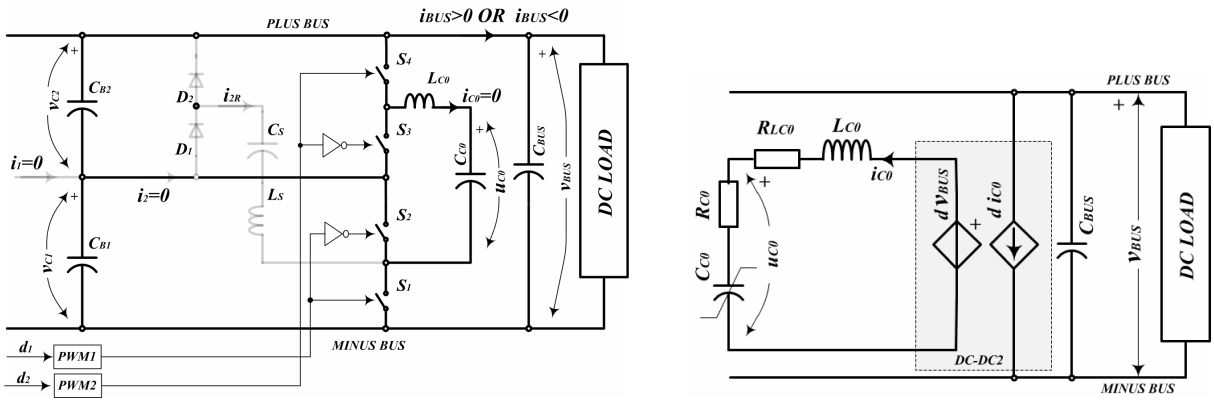
The DC-DC1 converter is a switch/diode cell with a filter inductor L_0. The inductor is connected on the rectifier plus rail, the diode D_0 is connected on the dc bus plus rail and the switch S_0 is connected to the mid-point of the capacitors C_{B1} and C_{B2}. The DC-DC2 converter is composed of the following devices: a switching leg S_1S_2 connected in parallel with the bottom capacitor C_{B1}, the switching leg S_3S_4 connected in parallel with the top capacitor C_{B2} and a diode leg D_1D_2 connected in parallel with the top side capacitor C_{B2}. Mid-points of the legs S_1S_2 and S_3S_4 are connected to the ultra-capacitor via a filter inductor L_{C0}. A resonant circuit L_SC_S is connected between the S_1S_2 mid-point and the diode D_1D_2 mid-point.

12.3.2. The DC-DC2 Converter Operating Modes

As already mentioned in the previous section, the DC-DC2 converter has two roles: 1) to control power flow between the drive and the ultra-capacitor when the drive operates in braking and ultra-capacitor motoring mode. 2) To assist to DC-DC1 converter and balance the voltages v_{C1} and v_{C2} when the drive operates in the mains motoring mode. The converter circuit diagram in different operating modes is given in Fig. 12.11 and Fig. 12.12.

12.3.2.1. The Ultra-capacitor Energy Transfer Mode

In this operating mode, the rectifier current is zero, and therefore the cell D_1D_2 and L_SC_S circuit (this part of DC-DC2 converter assists to the DC-DC1 converter) can be drooped from the circuit, as illustrated in Fig. 12.11 (a).



(a) (b)

Fig. 12.11 The DC-DC2 converter operating in the ultra-capacitor energy transfer mode and b) an equivalent circuit diagram [48].

Four switches denoted as S_1-S_4 and a filter inductor L_{C0}, that are connected in a three-level topology [92] controls power flow between the ultra-capacitor C_{C0} and the dc bus. More precisely, the circuit is active whenever the drive operates in the braking mode (charging the ultra-capacitor) or motoring mode from the ultra-capacitor (discharging the ultra-capacitor). The switches S_1-S_4 are controlled by two duty cycles d_1 and d_2. Detailed analysis of the DC-DC2 converter operating in the ultra-capacitor energy transfer mode was given in chapter 8, section 8.3. Here, in this chapter, very simplified analysis that is necessary to follow the dissertation is presented. For this, it will be assumed that $v_{C1}=v_{C2}$ and $d_1=d_2=d$. Simplified

circuit diagram depicted in Fig. 12.11 (b) is considered. Resistance R_{C0} is the ultra-capacitor internal resistance, which is assumed as frequency independent resistance. Resistance R_{LC0} is the inductor parasitic resistance, which includes the wire resistance and the core equivalent resistance [92].

The circuit in Fig. 12.11 (b) is described by equation

$$L_{C0}\frac{d\langle i_{C0}\rangle}{dt}=\langle v_{BUS}\rangle d-u_{C0}-R_{LC0}\langle i_{C0}\rangle, \tag{12.1}$$

where the symbol $\langle x\rangle$ denotes moving average value of a variable x.

From (12.1) and steady state condition follows duty cycle d

$$\begin{aligned} d&=\frac{u_{C0}+R_{LC0}i_{C0}}{v_{BUS}}\\ d_{\min}&=\frac{u_{C0\min}-R_{LC0}i_{C0\max}}{v_{BUS\max}}\\ d_{\max}&=\frac{u_{C0\max}+R_{LC0}i_{C0\max}}{v_{BUS\min}} \end{aligned}. \tag{12.2}$$

The ultra-capacitor current and voltage are controlled by the controllers via the duty cycle *d*.

12.3.2.2. The Mains Motoring Mode

Let us assume that the drive operates in the mains motoring mode. As mentioned, in this mode there is no power flow between the drive and ultra-capacitor. Hence, the ultra-capacitor current is zero (the ultra-capacitor stand-by). As the current is zero, the top side switches S_3S_4 can be drooped from the circuit, as illustrated in Fig. 12.11 (a).

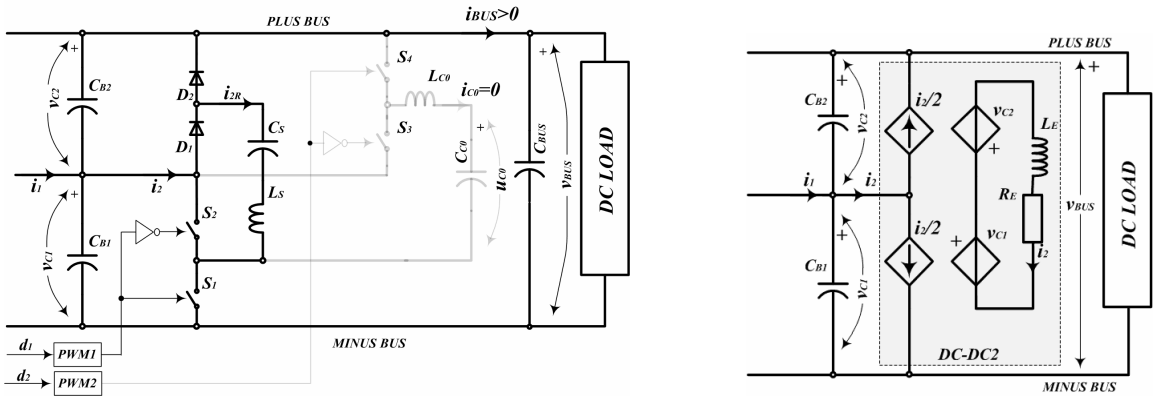


Fig. 12.12 a) The DC-DC2 converter operating in the mains motoring mode, and b) an equivalent circuit diagram.

As already discussed and mentioned in chapter 9, the circuit of Fig. 12.11 (a) is a variant of the switched capacitor converter. A leg S_1S_2 is connected across the bottom capacitor C_{B1}, and a leg D_1D_2 is connected across the top capacitor C_{B2}. The capacitor C_S is the main switched capacitor that transfers the energy from the bottom capacitor C_{B1} to the top capacitor C_{B2}, and the inductor L_S is an auxiliary inductor. The role of the inductor L_S is to

minimize the conduction losses and ensure the zero current switching condition (ZCS). The switches S_1 and S_2 are driven with complementary control signals at period T_{S2}. The duty cycle is d_1 and depends on the ultra-capacitor voltage (12.2), and is normally around 50%.

An equivalent circuit diagram of the DC-DC2 converter is given in Fig. 12.11 (b). The inductance L_E is an equivalent inductance of the resonant circuit, given as

$$L_E = L_S \frac{\pi^2}{2}\left(\frac{T_{S2}}{T_0}\right)^2, \tag{12.3}$$

where $T_0 = 2\pi\sqrt{L_S C_S}$ is the resonant period.

The current sources i_D and i_S are approximated by $i_2/2$, as it was already discussed in section 9.1. For simplicity of the analysis, one can assume that the capacitors C_{B1} and C_{B2} are large enough to maintain the voltages v_{C1} and v_{C2} constant over the switching cycle T_{S2}. The switches and diodes are modeled by constant voltage sources V_{S0} and V_{DF0}.

One complete cycle T_{S2} can be divided into four stages, namely stage A to stage D. Simplified model, topology stages and the waveforms are given in Fig. 12.13.

Stage A: Switch S_1 is closed at the instant t=0. The capacitor C_S is charged from v_{C1} via the switch S_1 diode D_1 and the inductor L_S. The current i_{2R} and voltage v_{CS} increase. Once reaches the maximum, the current starts to decrease towards zero ($L_S C_S$ resonant circuit).

Stage B: The current i_{2R} reaches zero and diode D_1 is blocked at the instant $t=T_0/2$. The current remains zero until commutation of the switch S_2.

Stage C: The switch S_2 is closed at the instant $t=dT_{S2}$. The capacitor C_S is discharged into v_{C2} via the switch S_2, diode D_2 and the inductor L_S. The current i_{2R} increases in negative direction in respect to the direction in Fig. 12.12. The voltage v_{CS} decreases. After reaching the maximum, the current starts to decrease towards zero ($L_S C_S$ resonant circuit).

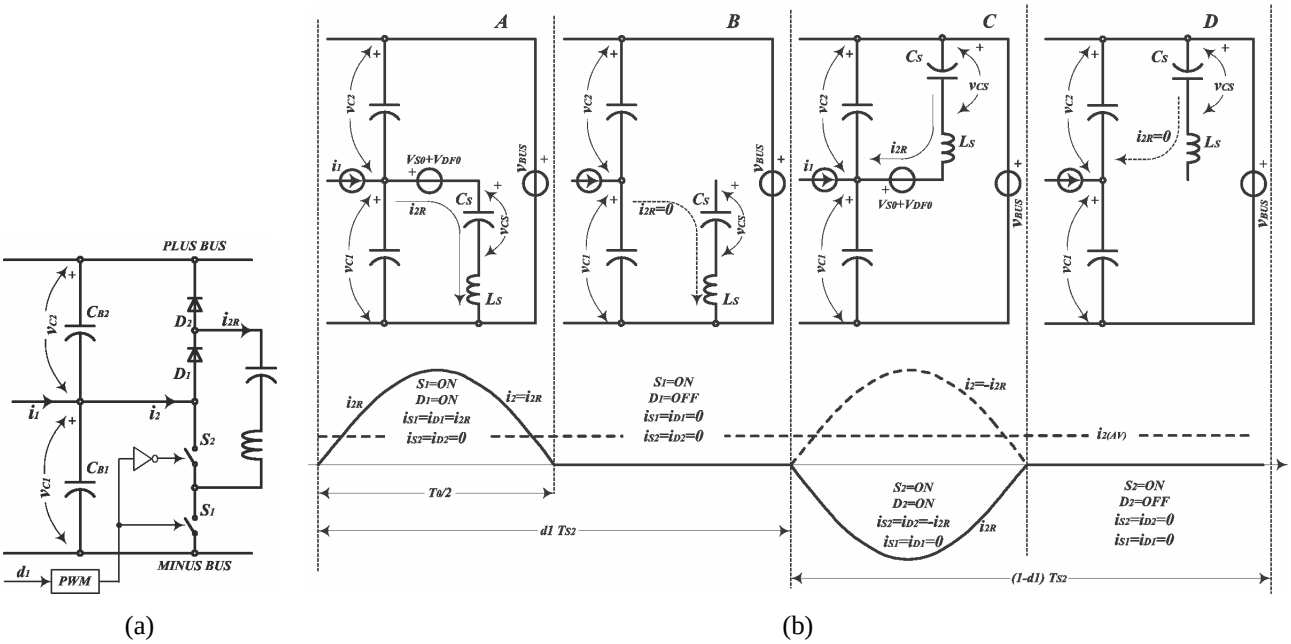


Fig. 12.13 a) Circuit diagram of the converter DC-DC2 based on ZCS switched capacitor converter. b) Different topological stages of the converter. A) S1, D1 are conducting, B) S1 is conducting D1 is blocking, C) S2, D2 are conducting, and D) S2 is conducting D2 is blocking.

Stage D: The current i_{2R} reaches zero and diode D_2 is blocked at the instant $t=dT_{S2}+T_0/2$. The current remains zero until the commutation of the switch S_1 at the instant $t=T_{S2}$. One switching cycle is finished.

12.3.2.3. Zero Current Switching Conditions and L_SC_S Design

To achieve the ZCS, the resonant current i_{R2} must fall to zero before next commutation of the S_1S_2 switch cell. Otherwise, the switch cell commutates at non-zero current conditions. As a consequence, the switching losses of the S_1S_2 and D_1D_2 will be quiet high. To satisfy the ZCS condition, the resonant frequency must be

$$\omega_0 = \frac{1}{\sqrt{L_S C_S}} \geq \frac{1}{\min\left(d_{\min}, (1-d_{\max})\right)} \frac{2\pi}{T_{S2}}, \tag{12.4}$$

where the maximum and minimum duty cycle have been defined in (12.2) as a function of the dc bus voltage and the ultra-capacitor voltage.

From the ZCS condition follows that

$$L_S C_S \leq \left(\min\left(d_{\min}, (1-d_{\max})\right) \frac{T_{S2}}{2\pi} \right)^2. \tag{12.5}$$

The capacitor and inductor can be selected using same optimization method that was discussed in chapter 9, section 9.3.2.2.

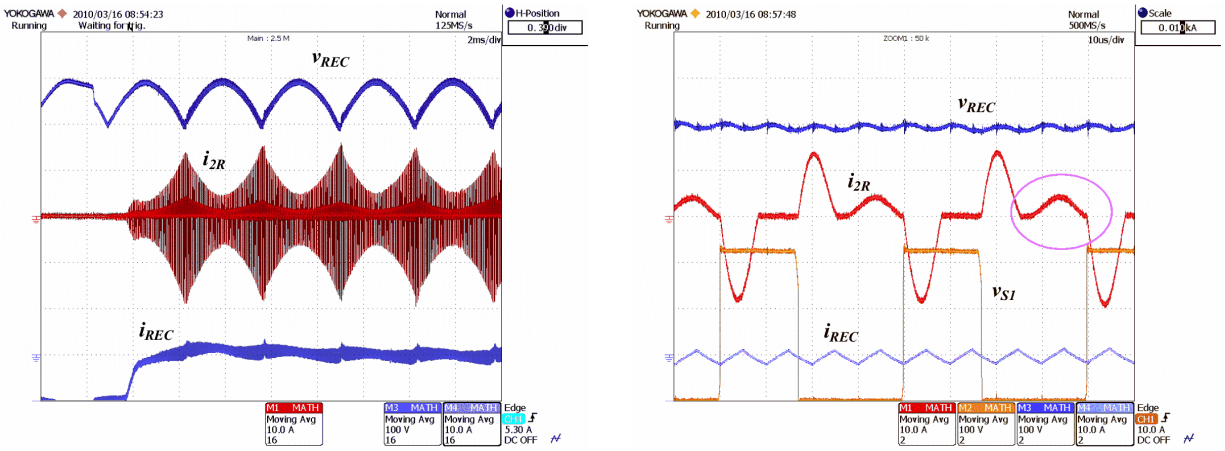
Fig. 12.14 (a) shows experimental waveforms of the rectifier voltage v_{REC}, resonant current i_{2R} and the rectifier current i_{REC}. Magnitude of the current directly follows the rectifier current magnitude and inversely follows magnitude of the rectifier voltage. More precisely it follows the difference between the dc bus voltage and rectifier voltage. This was discussed and explained in chapter 8. Fig. 12.14 (b) shows zoom of those waveforms and waveform of voltage v_{S1} (the bottom switch S_1 voltage in Fig. 12.13). In the current waveform, note an anomaly that is denoted in the pink. Once the current reaches zero, it is expected that the current remains zero until the next switching sequence. However, the current has another peak, with lower magnitude and slightly lower frequency. In this particular case, the commutation is still soft commutation; the current falls to zero before next commutation. However, this is only a coincidence. If duty cycle is different (in this case lower) the commutation will not be soft. The switch will commute at non-zero current conditions.

To investigate the root-cause of this anomaly, let us refer on the real circuit diagram, which is shown in Fig. 12.15 (a). In the real set-up circuit, the main dc bus capacitor C_{BUS} is dislocated from the dc-dc converter board and capacitors C_{B1}, $C_{B2.}$ This is indicated by the parasitic inductance L_γ in the circuit diagram in Fig. 12.15 (a). Thus, an additional parasitic resonant circuit is created by the parasitic inductance L_γ and the capacitors C_{B1}, C_{B2}. The parasitic resonant circuit is excited each time the switches S_1S_2 commutate. The voltages v_{C1} and v_{C2} therefore oscillates around the average value. This is visible in the waveforms in Fig. 12.15 (b). Once the voltage becomes greater than the voltage of the resonant capacitor C_S, the diode D_1 starts to re-conduct and charge the capacitor C_S.

Fig. 12.16 shows the waveforms after some modifications on the real circuit have been done. The first modification: An additional small inductance is connected between the dc bus capacitor and the converter board. Waveforms are shown in Fig. 12.16 (a). Note that the voltage ripple is greater than that in case without the additional inductance. The re-conduction time is longer and therefore the commutation is hard.

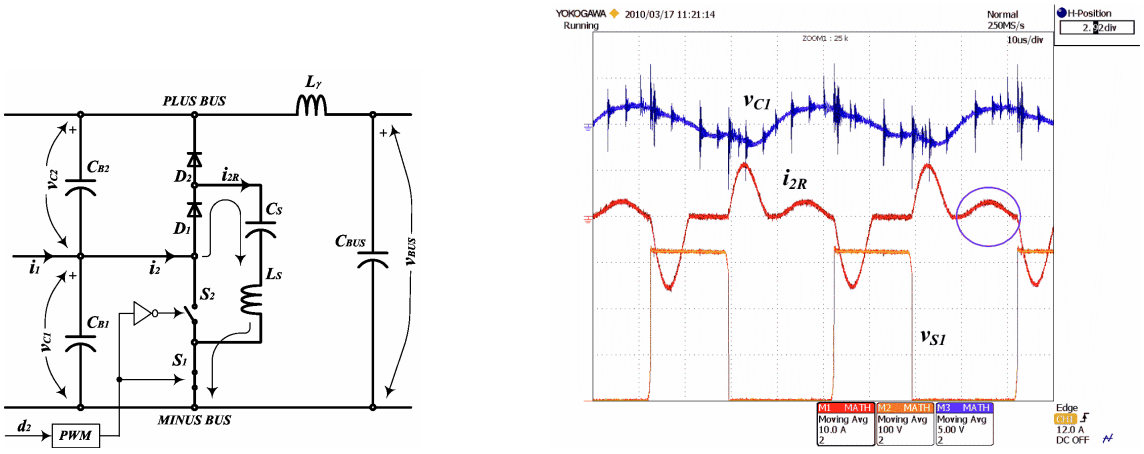
The second modification: An additional inductor of 50μH is connected between the dc bus capacitor and the converter board. Fig. 12.16 (b) shows the waveforms. The voltage ripple is smaller than that of the first case. The voltage waveform is regular triangular waveform. The resonant current is regular, no re-conduction of the diode D_1. The switches commutate at the zero current condition.

The third modification: An additional dc bus capacitor is connected close to the converter board. In this case the parasitic inductance is significantly reduced. Fig. 12.17 shows the waveforms. The voltage ripple is smaller than before. The resonant current is regular, without re-conduction. The switches commutate at the zero current condition.



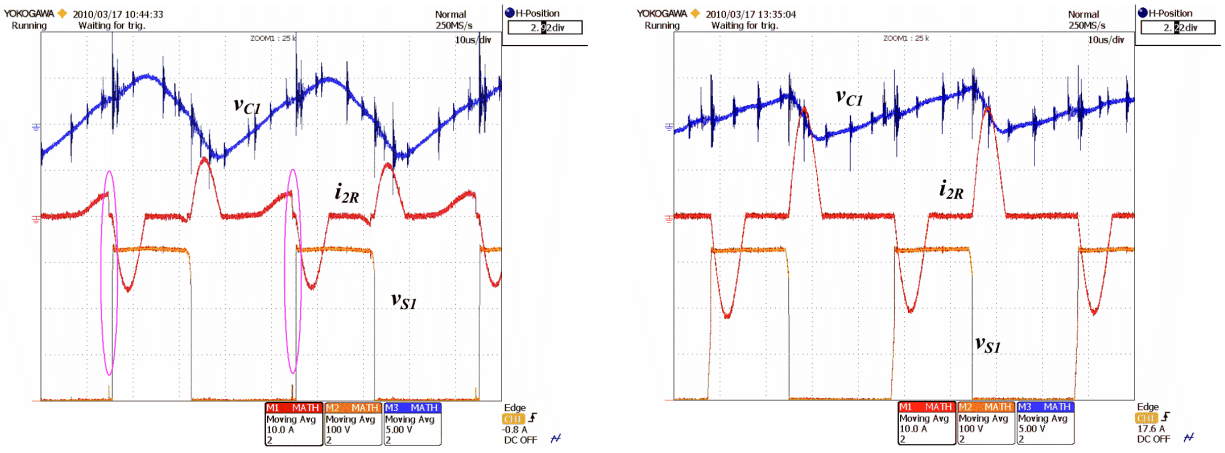
(a) (b)

Fig. 12.14 a) Experimental waveforms of the rectifier current i_{REC}, the resonant circuit current i_{2R} [10A/div] and the rectifier voltage v_{REC} [100V/div]. The conversion power step from 10% to 100%. The bus voltage is V_{BUS}=650V and nominal load P_{LOAD}=5500W. b) Zoom of the waveforms including the bottom switch voltage v_{S1} [100V/div].



(a) (b)

Fig. 12.15 a) The equivalent circuit including real value of the components. b) The waveforms of the resonant circuit current i_{2R} [10A/div], ac component of the bottom filter capacitor voltage v_{C1} [5V/div], and the bottom switch voltage v_{S1} [100V/div].



(a) (b)

Fig. 12.16 The waveforms of the resonant circuit current i_{2R} [10A/div], ac component of the bottom filter capacitor voltage v_{C1} [5V/div], and the bottom switch voltage v_{S1} [100V/div]. a) The parasitic inductance L_{BUS} is slightly increased. b) An additional filter inductor of 50μH between the dc bus capacitor and the converter board.

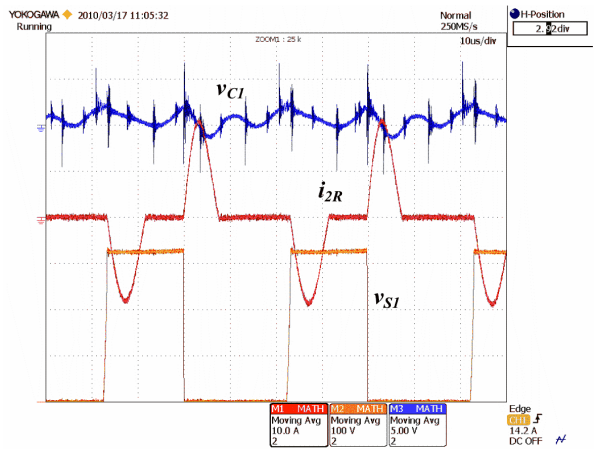


Fig. 12.17 The waveforms of the resonant circuit current i_{2R} [10A/div], ac component of the bottom filter capacitor voltage v_{C1} [5V/div], and the bottom switch voltage v_{S1} [100V/div]. The dc bus capacitor is connected on the board (the parasitic inductance L_γ significantly reduced).

13. MODELING AND CONTROL SCHEME

The modelling and control scheme are discussed in this chapter. The large and small signal model of the entire conversion system (the ultra-capacitor, the dc-dc converter and drive converter) is developed. Some of the model derivations are re-used from chapter 5 and chapter 9. In the second part of this chapter, the control objective and control scheme are discussed. The model and control scheme are validated by Matlab/Simulink simulation and a set of experimental measurements. The results are presented and discussed.

13.1. The System Model

13.1.1. Large Signal Model

The large signal (nonlinear) model of the entire power conversion system is depicted in Fig. 13.1. The input rectifier is modeled by a voltage source v_{REC}. The dc bus capacitor is modeled as an ideal capacitor C_{BUS} and its equivalent series resistance R_{ESR}.

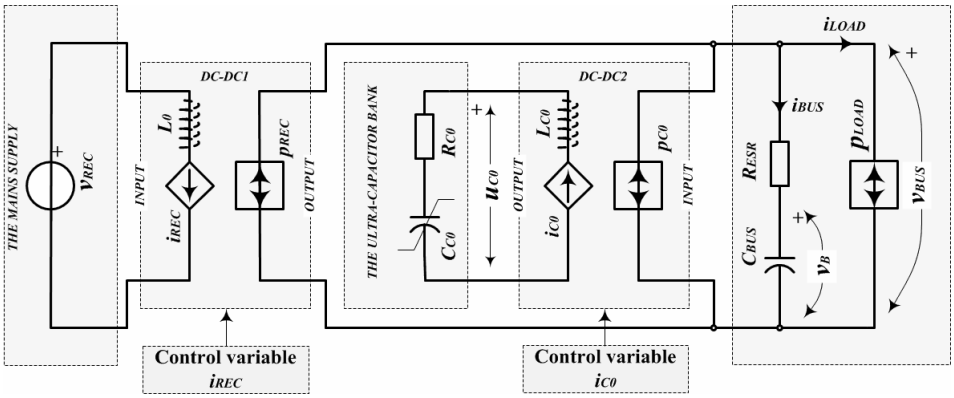


Fig. 13.1 Large signal model of the three-terminal energy storage and power factor correction device, rectifier and inverter load.

The system of Fig. 13.1 is described by the instantaneous power equation

$$C_{BUS}\frac{dv_B}{dt}=\frac{p_{REC}}{v_{BUS}}-\frac{p_{C0}}{v_{BUS}}-\frac{p_{LOAD}}{v_{BUS}}, \tag{13.1}$$

where the rectifier and the ultra-capacitor instantaneous power is

$$p_{REC}=v_{REC}i_{REC}-\underbrace{i_{REC}L_0\frac{di_{REC}}{dt}}_{\equiv 0}, \tag{13.2}$$

$$p_{C0}=u_{C0}i_{C0}+\underbrace{i_{C0}L_{C0}\frac{di_{C0}}{dt}}_{\equiv 0}. \tag{13.3}$$

Instantaneous power of the filter inductor L_{C0} and the boost inductor L_0 are neglected in (12.2) and (12.3).

The ultra-capacitor circuit is described by the following equations

$$(C_0 + 2k_C u_C)\frac{du_C}{dt} = i_{C0}, \tag{13.4}$$

$$u_{C0} = u_C + R_{C0} i_{C0}, \tag{13.5}$$

$$v_{BUS} = v_B + R_{ESR}\left(\frac{p_{REC}}{v_{BUS}} - \frac{p_{C0}}{v_{BUS}} - \frac{p_{LOAD}}{v_{BUS}}\right). \tag{13.6}$$

13.1.2. Small Signal Model

Appling the small signal approximation and Laplace transformation on (13.2)-(13.6) yields transfer functions in matrix form

$$\begin{bmatrix} u_{C0}(s) \\ v_{BUS}(s) \end{bmatrix} = \begin{bmatrix} G_{C0}(s) & 0 \\ G_{BUS}(s) & G_{BUS}(s) \end{bmatrix} \underbrace{\begin{bmatrix} i_{C0}(s) \\ i_{REC}(s) \end{bmatrix}}_{CONTROL} + \begin{bmatrix} 0 & 0 \\ G_P(s) & G_{vREC}(s) \end{bmatrix} \underbrace{\begin{bmatrix} p_{LOAD}(s) \\ v_{REC}(s) \end{bmatrix}}_{DISTURBANCE}. \tag{13.7}$$

The system output variables are u_{C0} and v_{BUS}, the control variables are i_{C0} and i_{REC}, and the disturbance variables are p_{LAOD} and v_{REC}. The transfer functions are

$$\begin{aligned} G_{BUS(C0)} &= \left.\frac{v_{BUS}(s)}{i_{C0}(s)}\right|_{\substack{i_{REC}(s)=0 \\ p_{LOAD}(s)=0 \\ v_{REC}(s)=0}} = -\frac{(1+sC_{BUS}R_{ESR})(U_{C0}+I_{C0}R_{C0})}{sC_{BUS}V_{BUS}}, \\ G_{BUS(REC)} &= \left.\frac{v_{BUS}(s)}{i_{REC}(s)}\right|_{\substack{i_{C0}(s)=0 \\ p_{LOAD}(s)=0 \\ v_{REC}(s)=0}} = \frac{V_{REC}(1+sC_{BUS}R_{ESR})}{sC_{BUS}V_{BUS}}, \end{aligned} \tag{13.8}$$

$$G_{C0}(s) = \left.\frac{u_{C0}(s)}{i_{C0}(s)}\right|_{\substack{i_{REC}(s)=0 \\ p_{LOAD}(s)=0 \\ v_{REC}(s)=0}} = R_{C0}\frac{s + \dfrac{C_0 - 2kI_{C0}R_{C0} + 2k(U_{C0}+I_{C0}R_{C0})}{R_{C0}(C_0 + 2k(U_{C0}-I_{C0}R_{C0}))^2}}{s + \dfrac{2kI_{C0}}{(C_0+2k(U_{C0}-I_{C0}R_{C0}))^2}} = R_{C0}\frac{s+\omega_Z}{s+\omega_P},$$

$$\begin{aligned} G_P(s) &= \left.\frac{v_{BUS}(s)}{p_{LOAD}(s)}\right|_{\substack{i_{C0}(s)=0 \\ i_{REC}(s)=0 \\ v_{REC}(s)=0}} = -\frac{(1+sC_{BUS}R_{ESR})}{sC_{BUS}V_{BUS}}, \\ G_{vREC}(s) &= \left.\frac{v_{BUS}(s)}{v_{REC}(s)}\right|_{\substack{i_{C0}(s)=0 \\ i_{REC}(s)=0 \\ p_{LOAD}(s)=0}} = \frac{I_{REC}(1+sC_{BUS}R_{ESR})}{sC_BV_{BUS}}. \end{aligned} \tag{13.9}$$

Remark: When the transfer function $G_{BUS(C0)}$ was being developed, it was assumed that the ultra-capacitor is an infinite capacitance.

Fig. 13.2 shows block diagram of the small signal model of the system (13.1)-(13.6)

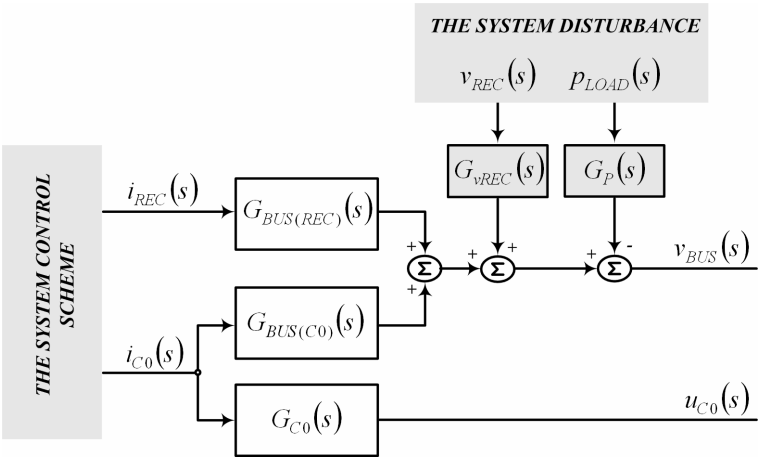


Fig. 13.2 Small signal model of the entire power conversion system.

13.2. Control Aspects

13.2.1. The Control Objectives

The primary control objective is to asymptotically regulate the dc bus voltage to the reference, where the reference depends on the system-operating mode. The secondary control objective is to regulate the rectifier current to be constant or quasi-constant in order to reduce the mains current total harmonic distortion (THD). The last control objective is to regulate the ultra-capacitor state of the charge, where the state of charge reference depends on the operating mode.

13.2.2. Control Scheme

The control scheme is illustrated in Fig. 13.3. Note two sections, namely *DC-DC1 CONTROL* and *DC-DC2 CONTROL*. The first control block consists of the controllers G_{iREC} and G_{vBUS}. The controller G_{iREC} regulates the rectifier current, while the controller G_{vBUS} asymptotically regulates the dc bus voltage to the reference $V_{BUS(REF)}$. The block denoted as *DC-DC2 CONTROL* consists of the ultra-capacitor current controller G_{iC0}, the ultra-capacitor voltage controller G_{uC0} and two dc bus voltage controllers, $G_{vBUSmax}$ and $G_{vBUSmin}$. The mid-point voltage balancing controller is not illustrated in the control structure. It was discussed in chapter 6.

13.2.3. Operational Modes

From control perspective, the system may operate in three different modes: 1) the rectifier mode, 2) the ultra-capacitor energy transfer mode and 3) the mains peak power filtering mode.

13.2.3.1. The Rectifier Mode

Fig. 13.4 illustrates the control scheme when the drive operates in the rectifier (the mains motoring) mode. When operates in this mode, the drive is supplied from the mains. The dc bus voltage is actively controlled by the DC-DC1 converter to the reference $V_{BUS(REF)}$.

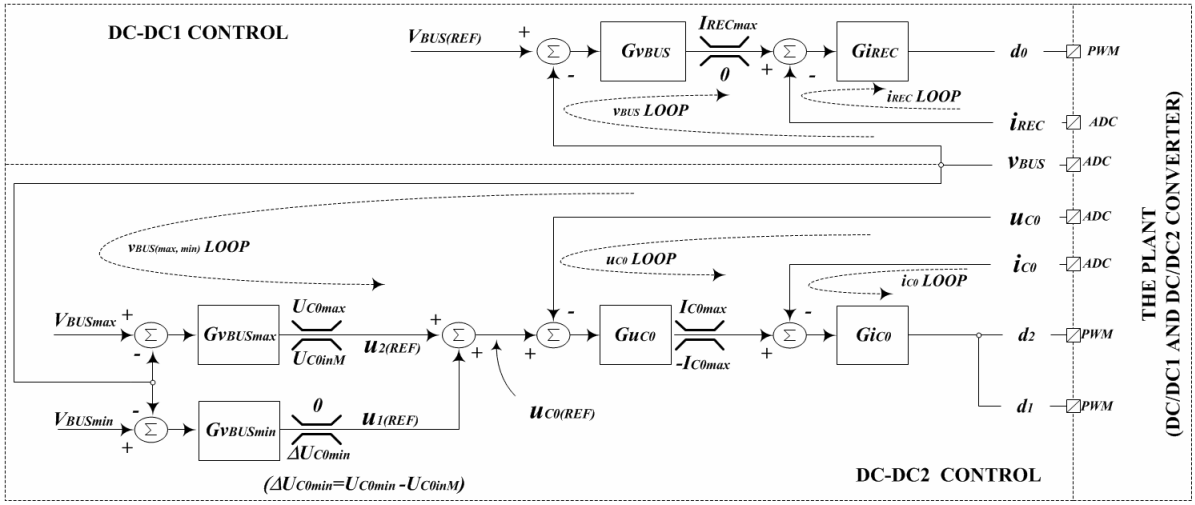


Fig. 13.3 The control scheme of the three-terminal energy storage and power factor correction device.

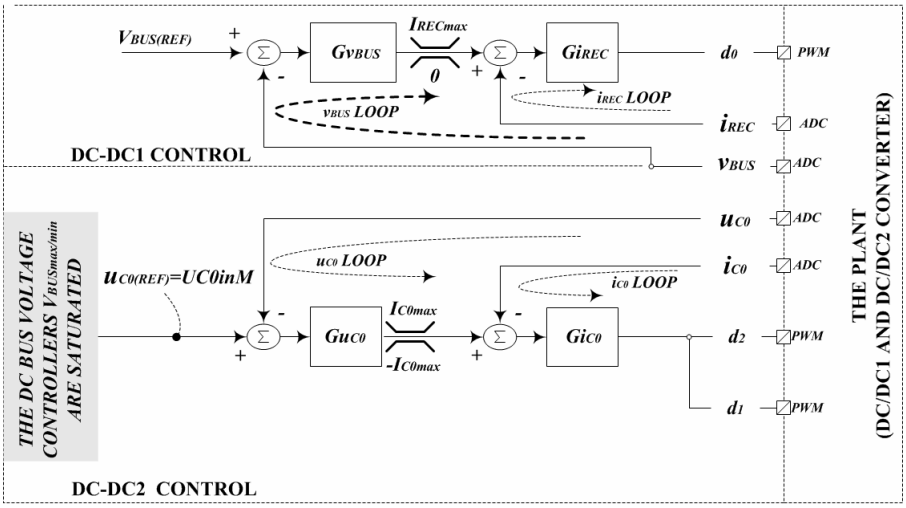


Fig. 13.4 The control scheme in the rectifier mode. The dc bus min/max voltage controllers are saturated (deactivated).

As mentioned before, in chapter 12 (Fig. 12.5 (a)), the dc bus voltage is $v_{BUS}=V_{BUS(REF)}$, where the reference $V_{BUS(REF)}$ is lower than the reference V_{BUSmax} and greater than the reference V_{BUSmin}. Thus, the controller $G_{vBUSmax}$ is saturated at U_{C0inM}, while the controller $G_{vBUSmin}$ is saturated at zero. Please, note that the controllers $G_{vBUSmax}$ and $G_{vBUSmin}$ are designed in such a way to have $out \downarrow \; if \; error > 0$ & $out \uparrow \; if \; error < 0$, where *out* is the controllers output $u_{1(REF)}$ and $u_{2(REF)}$, and *error* is the controllers input (the dc bus voltage control error). The symbols $\uparrow$ and $\downarrow$ denote that the variable increases and decreases respectively.

The ultra-capacitor voltage reference is constant,

$$u_{C0(REF)} = u_{1(REF)} + u_{2(REF)} = 0 + U_{C0inM} = U_{C0inM} . \tag{13.10}$$

The controller G_{uC0} regulates the ultra-capacitor voltage to the intermediate reference U_{C0inM} in order to prevent power flow between the ultra-capacitor and the drive.

Fig. 13.5 shows the small signal model and control scheme of the system working in the rectifier mode. As the dc bus voltage controllers are saturated, the ultra-capacitor voltage (small signal) reference is zero.

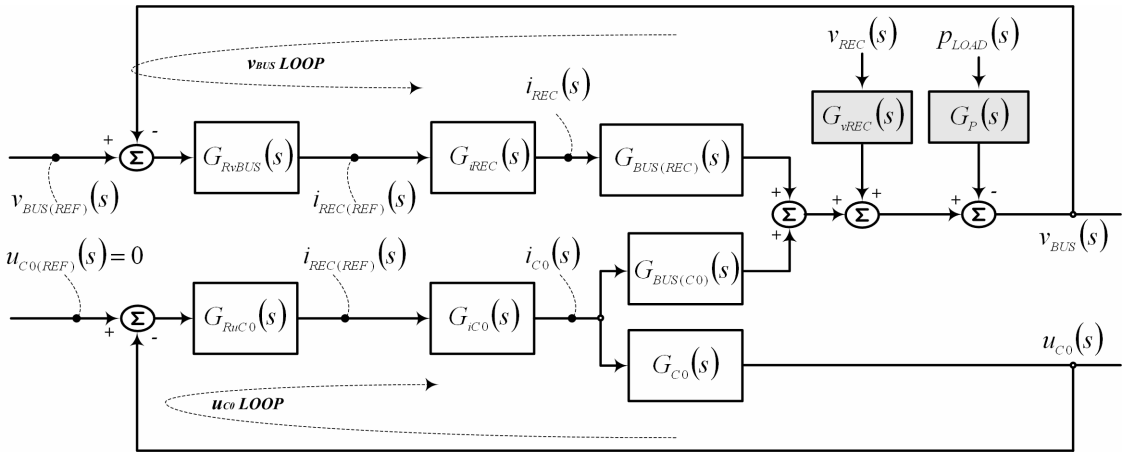


Fig. 13.5 Small signal block diagram of the control system operating in the rectifier mode.

13.2.3.2. The Ultra-capacitor Energy Transfer Mode

In the ultra-capacitor energy transfer mode, two sub-modes can be distinguished: a) the braking mode, and b) ride-through mode. Fig. 13.6 and Fig. 13.7 depict the control scheme and small signal control block diagram.

o Braking Mode

The drive load is negative (the motor works as a generator). Because the rectifier is a uni-directional device, the dc bus capacitor is charged and the dc bus voltage v_{BUS} increases. As the dc bus voltage increases, the dc bus voltage error decreases. Thus, the boost voltage controller trays to regulate the dc bus voltage and reduce the rectifier current reference towards zero. Once the reference reaches zero, the boost voltage controller is saturated, and can be neglected in the analysis.

Once the dc bus voltage reaches the reference V_{BUSmax}, the dc bus voltage controller $G_{vBUSmax}$ is out of saturation, while the controller $G_{vBUSmin}$ stays saturated at zero. Thus, the ultra-capacitor voltage reference $u_{C0(REF)}$ starts to increase from U_{C0inM} towards U_{C0max},

$$U_{C0inM} < u_{C0(REF)} \uparrow \leq U_{C0\max}. \tag{13.11}$$

The ultra-capacitor current is set by the controller G_{uC0} at such a level to maintain the dc bus voltage constant v_{BUS}=V_{BUSmax}. If the braking energy is greater than the ultra-capacitor capability, the ultra-capacitor will be fully charged to the maximum voltage U_{C0max} before the end of the braking phase. The dc bus voltage controller $G_{vBUSmax}$ will be saturated at U_{C0max}, and the ultra-capacitor voltage reference will stop increasing. The ultra-capacitor voltage will stay constant and the current i_{C0} will fall to zero; charging of the ultra-capacitor is finished. Then, the dc bus voltage will start increasing until activation of the braking resistor or the drive over-voltage (over-braking fault) protection.

When the drive operates in motoring mode, the ultra-capacitor has to be discharged to the intermediate value U_{C0inM} in order keep the ultra-capacitor ready for next braking cycle. The dc bus voltage controller $G_{vBUSmax}$ regulates the dc bus voltage to V_{BUSmax}. Output of the

controller $G_{vBUSmax}$ decreases and therefore the ultra-capacitor voltage reference decreases towards U_{C0inM}. The ultra-capacitor is discharged, supplying the drive load.

$$U_{C0inM} \le u_{C0(REF)} \downarrow < U_{C0\max}. \tag{13.12}$$

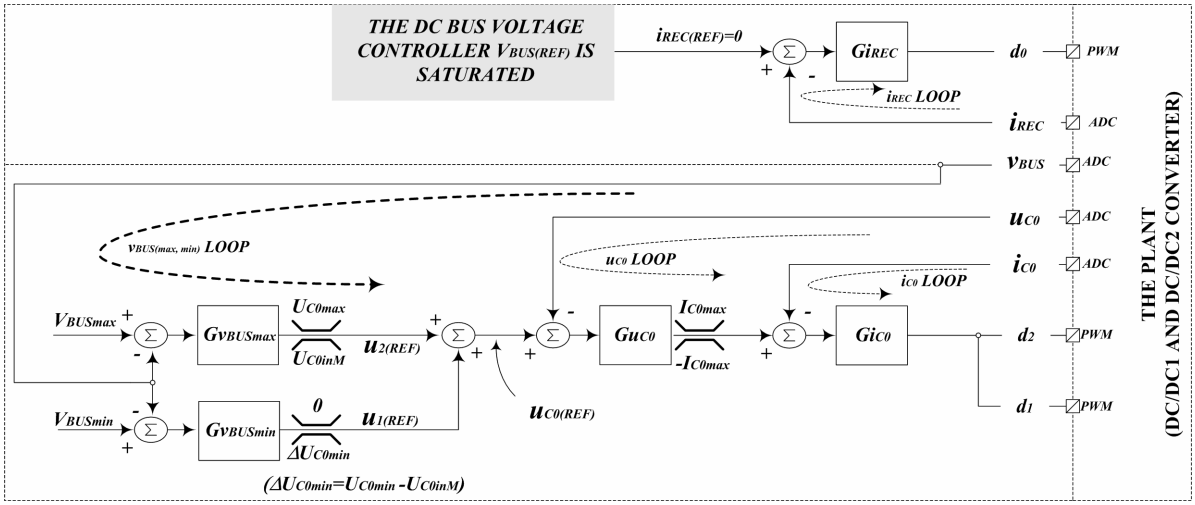


Fig. 13.6 Control scheme in the ultra-capacitor energy transfer mode. The rectifier control system is saturated (deactivated).

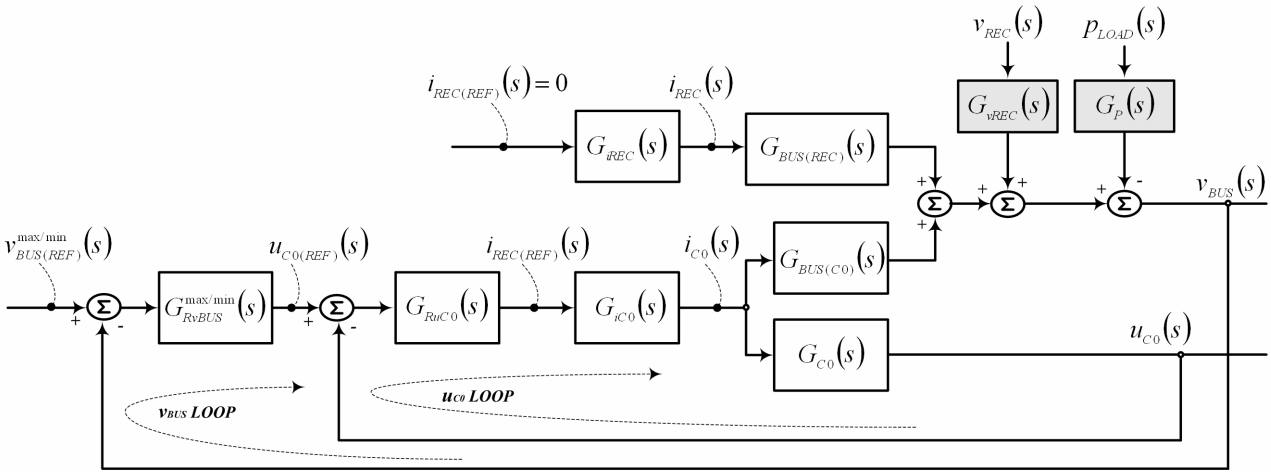


Fig. 13.7 Small signal block diagram of the control system operating in the ultra-capacitor energy transfer mode.

Once the ultra-capacitor is discharged to the intermediate level U_{C0inM}, the dc bus voltage controller $G_{vBUSmax}$ is saturated at the reference U_{C0inM}. The ultra-capacitor voltage reference is therefore constant

$$u_{C0(REF)} = U_{C0inM} + 0 = U_{C0inM}. \tag{13.13}$$

The ultra-capacitor voltage is regulated to the intermediate reference, $u_{C0}=U_{C0inM}$. Therefore, the ultra-capacitor current falls to zero and discharging is finished. The dc bus capacitor is discharged and the dc bus voltage decreases. Once it reaches the reference

$V_{BUS(REF)}$, the boost voltage controller G_{vBUS} goes out of saturation and the DC-DC1 converter starts to regulate the dc bus voltage. The drive is supplied again from the mains.

o The Ride-Through Mode

When the mains is interrupted, the dc bus voltage starts to decrease until it reaches the minimum V_{BUSmin}. At that instance, the controller $G_{vBUSmin}$ goes out of saturation and the output $u_{1(REF)}$ starts to decrease below zero towards $\Delta U_{C0min}=U_{C0min}-U_{C0inM}$. Since the controller $G_{vBUSmax}$ stays saturated at U_{C0inM}, the ultra-capacitor voltage reference starts to decrease below U_{C0inM} towards U_{C0min}.

$$(U_{C0inM}+U_{C0\min}-U_{C0inM}=U_{C0\min})\geq u_{C0(REF)}\downarrow> U_{C0inM}\,, \tag{13.14}$$

The ultra-capacitor is discharged deeper while the dc bus voltage is regulated to the minimum level $v_{BUS}=V_{BUSmin}$. Once the mains is recovered, the dc bus voltage starts to increase to the nominal voltage (defined by the mains voltage). At same time, the ultra-capacitor is charged and its voltage increases towards U_{C0inM} in order to be ready for next interruption.

If the power interruption is longer than the specified, the ultra-capacitor will be discharged to the lower minimum level U_{C0min}. Then, the ultra-capacitor current will fall to zero and the dc bus voltage will start decreasing until reaches the under supply fault (USF) level. The drive will fail in the USF and the complete system will be stopped.

o The Mains Peak Power Smoothing Mode

When the drive operates in the mains peak power filtering mode, the DC-DC1 and DC-DC2 control blocks are active. The dc bus boost voltage controller is active continuously, while the dc bus voltage min/max controllers operate complementary. Equivalent control block diagram that illustrates this operating mode is depicted in Fig. 13.8.

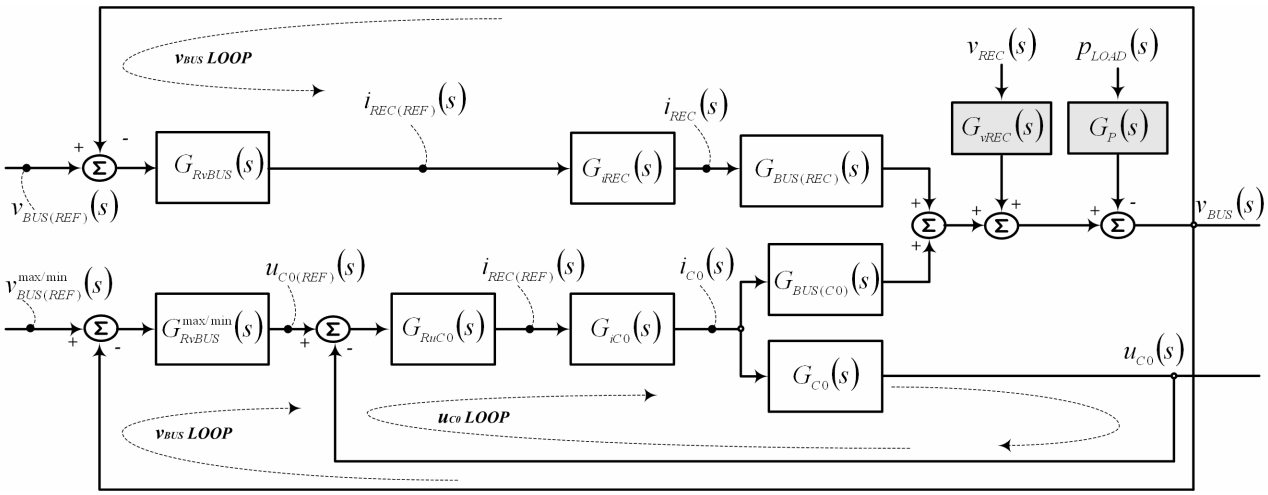


Fig. 13.8 Small signal block diagram of the system operating in the mains peak power filtering mode. All controllers are active.

13.3. Simulation and Experiments

The model and control algorithm proposed in this chapter were simulated by the average model (13.1)-(13.6) implemented in Matlab/Simulink and verified by a set of experiments. Some of the simulation and experimental results are presented and discussed hereafter. All relevant parameters of the system and control are summarized in TABLE 13-1.

TABLE 13-1: The conversion system and control parameters. Sampling time for the dc bus voltage controllers and the ultra-capacitor filter is $T_S = 200\mu s$.

ULTRA-CAPACITOR SIDE		DC BUS SIDE	
U_{C0max}	780 V	V_{BUSmax}	675 V
U_{C0inM}	350 V	V_{BUS}	650V
U_{C0min}	250 V	V_{BUSmin}	625 V
Δu_{C0}	3 V	C_{BUS}	820 μF
i_{C0max}	15 A	R_{ESR}	200 mΩ
C_{C0}	0.3 F	f_{BUS}	50Hz
k_C	0.000143 F/V	$G_{vBUS(max)}$	$G_{vBUS\min}(s) = -\frac{0.145s + 32}{s}$
			$G_{vBUS\max}(z) = -0.145 - \frac{0.0065}{1 - z^{-1}}$
R_{C0}	2 Ω	$G_{vBUS(min)}$	$G_{vBUS\min}(s) = -\frac{0.2s + 45}{s}$
			$G_{vBUS\min}(z) = -0.2 - \frac{0.009}{1 - z^{-1}}$
k_{PC0}	5	f_{BOOST}	50Hz & 1Hz
T_F	$G_F(s) = \frac{1}{0.1s + 1}$	$G_{vBUS(boost)}$	$G_{vBUS(boost)}(s) = \left\{\frac{0.56s + 88}{s} \,\&\, \frac{0.0112s + 0.035}{s}\right\}$
	$G_F(z) = \frac{1}{500(1 - z^{-1}) + 1}$		$G_{vBUS(boost)}(z) = \left\{0.56 + \frac{0.0176}{1 - z^{-1}} \,\&\, 0.0112 + \frac{7 \cdot 10^{-6}}{1 - z^{-1}}\right\}$

The control algorithm, PWM and protection functions were implemented in a fixed-point 32 bit digital signal processor (DSP). The complete control algorithm is executed at

three different rates: the rectifier current control at 100 kHz, the ultra-capacitor current control at 25 kHz and the dc bus voltage control at 5 kHz. The controllers were designed as the standard proportional-integral (PI) controllers. The controller parameters were computed in continuous time domain (s), and then translated into discrete time domain, (z), using the approximation $s = \frac{1 - z^{-1}}{T_S}$, where is the sampling period is $T_{S(iREC)} = 10\mu s$, $T_{S_{iC0}} = 40\mu s$ and $T_{S(vBUS)} = 200\mu s$.

13.3.1. Simulation Results

Fig. 13.9 shows waveforms simulated during an entire operating cycle: the mains motoring (**MM**), braking (**B**), the ultra-capacitor motoring (**MC$_0$**) and the mains motoring mode (**MM**). Fig. 13.10 shows the dc bus voltage and the mains current waveforms during transition from the mains motoring mode to braking mode.

Fig. 13.10 shows the dc bus voltage and the mains current during transition from the mains motoring mode to the braking mode. Once the dc bus load becomes negative, the dc bus voltage starts to rise from the reference $V_{BUS(REF)}$ =650V towards the reference V_{BUSmax}=655V, while the mains current drops to zero. The dc bus voltage overshoot is small, approximately 15V, which is 2.3% of the nominal voltage.

Fig. 13.11 shows the dc bus voltage and the mains current waveform during transition from the ultra-capacitor motoring mode to the mains motoring mode. The dc bus voltage falls from the reference V_{BUSmax} =655V towards the reference $V_{BUS(REF)}$=650V, while the mains current rises slowly. Note, the dc bus voltage undershoot is small, around 1V that is 0.15% of the nominal voltage.

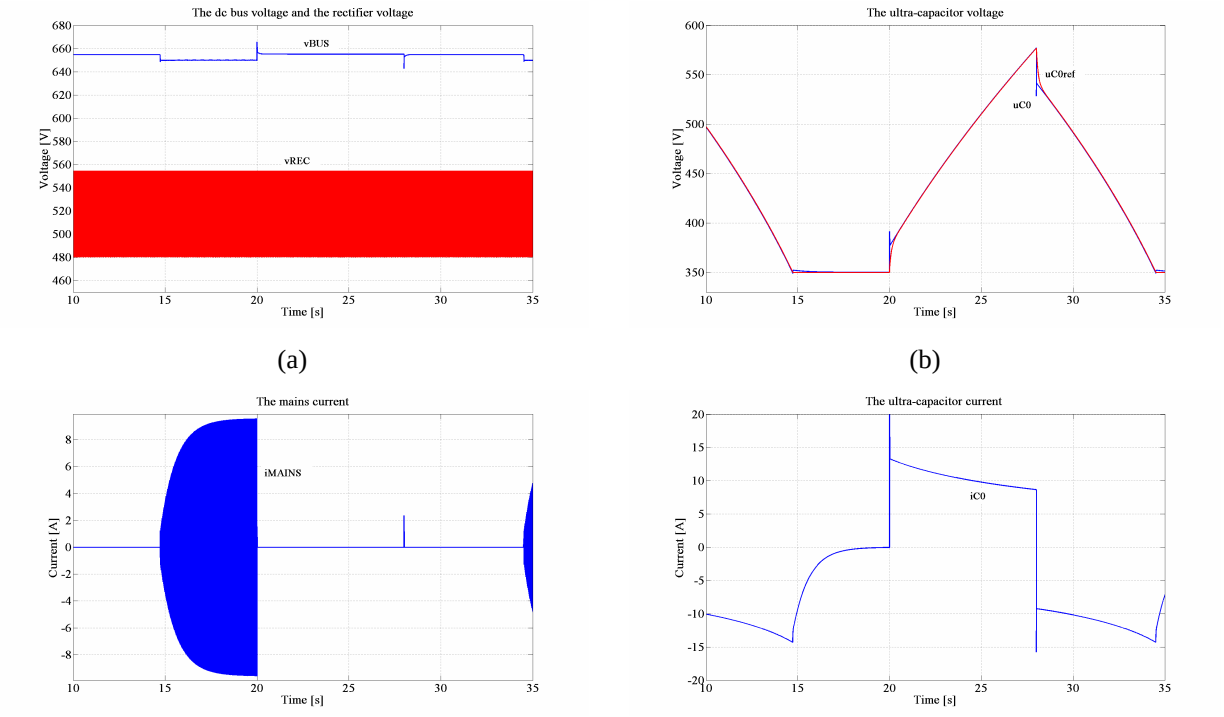
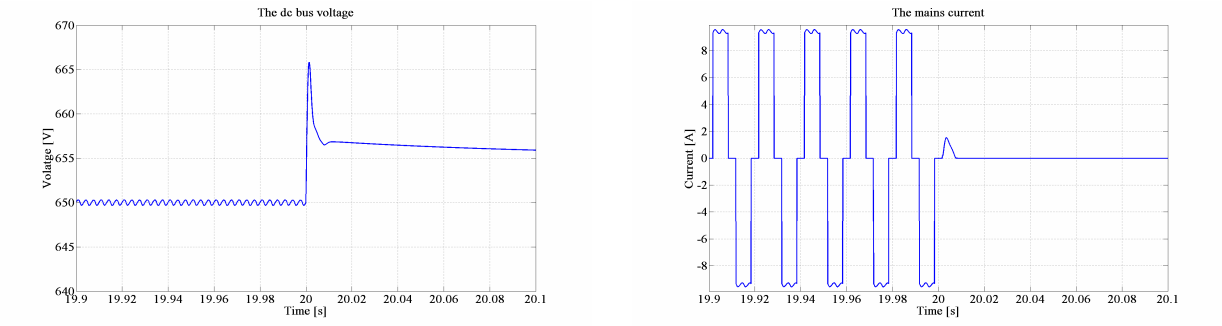
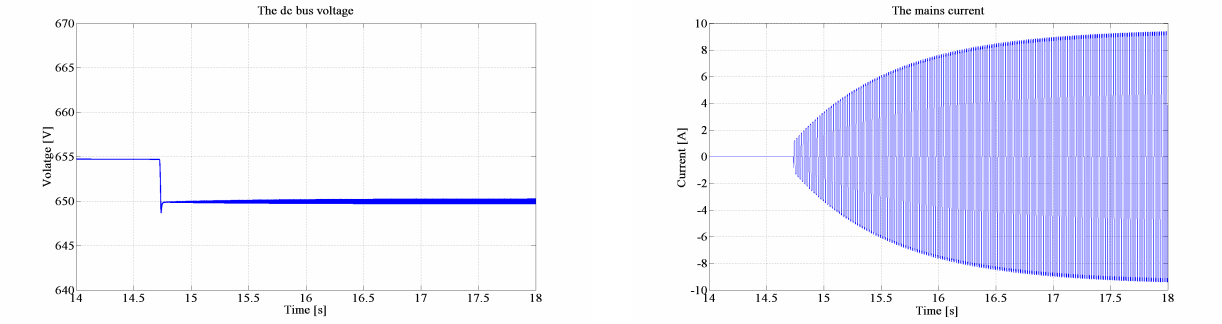


Fig. 13.9 Simulated waveforms of the dc bus voltage v_{BUS}, rectifier voltage, the ultra-capacitor voltage u_{C0} and current i_{C0} during an entire cycle; the mains motoring (**MM**), braking (**B**), the ultra-capacitor motoring (**MC$_0$**) and the mains motoring mode (**MM**). P_{LOAD}=+/- 5000W, C_{BUS}=820µF, C_{C0}=0.4F, V_{MAINS}=400Vrms.



(a) (b)

Fig. 13.10 Simulated waveforms of the dc bus voltage v_{BUS} and the mains current i_{MAINS} during transition from the mains motoring mode to braking mode. P_{LOAD}=+/- 5000W, C_{BUS}=820µF, C_{C0}=0.4F, V_{MAINS}=400Vrms.

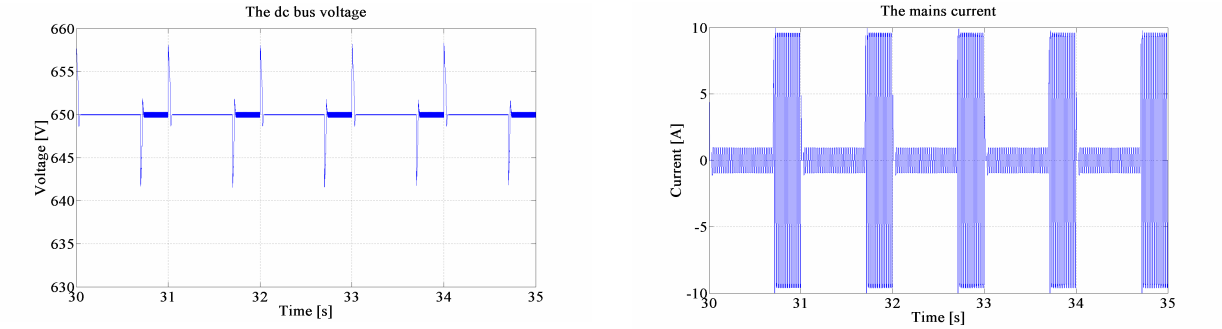


(a) (b)

Fig. 13.11 Simulated waveforms of the dc bus voltage v_{BUS} and the mains i_{MAINS} current during transition from the ultra-capacitor motoring mode to the mains motoring mode.

13.3.1.1. The Mains Peak Power Smoothing

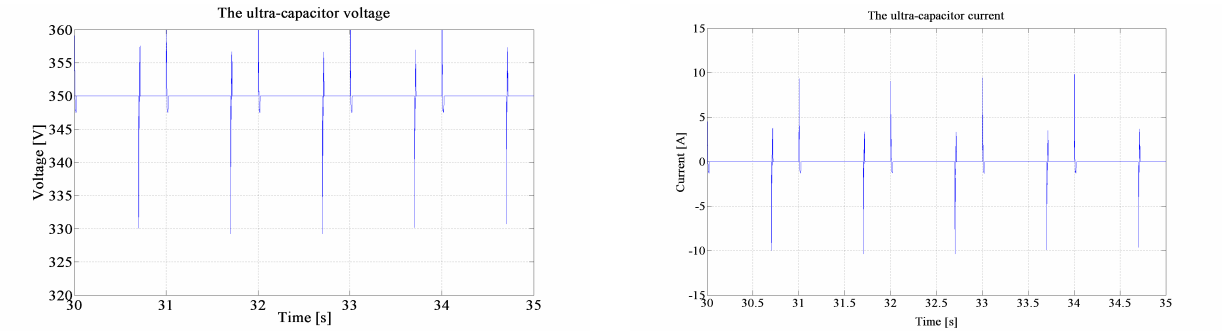
Fig. 13.12 and Fig. 13.13 illustrate the drive system behaviour in presence of a discontinuous load. The dc bus load is cycling between 10% and 100% with repetition period of 1s and duty cycle of 35%. Waveforms of the dc bus voltage and the mains current when the mains peak power filter mode is not active (the voltage controller bandwidth is f_{BOOST}=50Hz) are shown in Fig. 13.12.



(a) (b)

Fig. 13.12 Simulated waveforms of the dc bus voltage v_{BUS} and the mains i_{MAINS} current when the load is cycling 10% to 100% to 10%. The bus voltage is v_{BUS}=650V, the mains phase-to-phase voltage V_{MAINS}=400Vrms, the dc bus capacitor C_{BUS}=820µF and the boost voltage controller bandwidth is f_{BOOST}=50Hz.

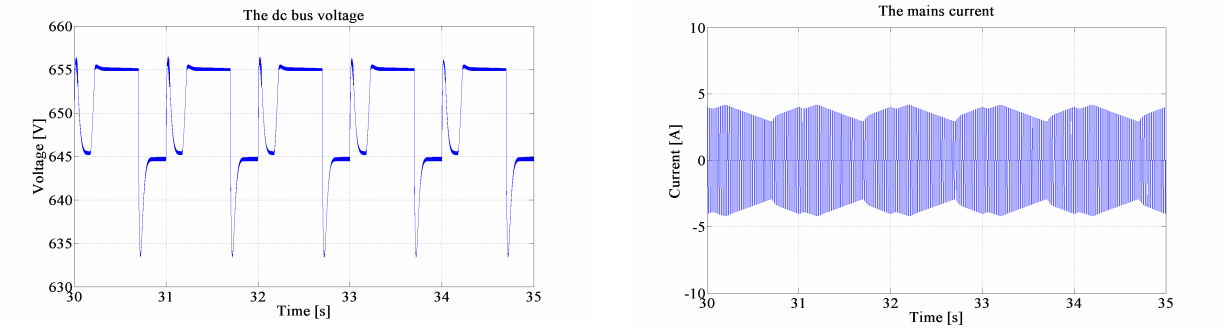
The dc bus is regulated to the reference $V_{BUS(REF)}$ =650V. Magnitude of the mains current is modulated by the dc bus load, and varies from approximately 1A (at light load) to 9.5A (at full load). Fig. 13.13 shows waveforms of the ultra-capacitor current and voltage. The current is zero with narrow positive and negative spikes. The spikes are caused by the dc bus min/max voltage controller because difference between the dc bus voltage references is narrow, in this case V_{BUSmax} - V_{BUSmin} =10V.



(a) (b)

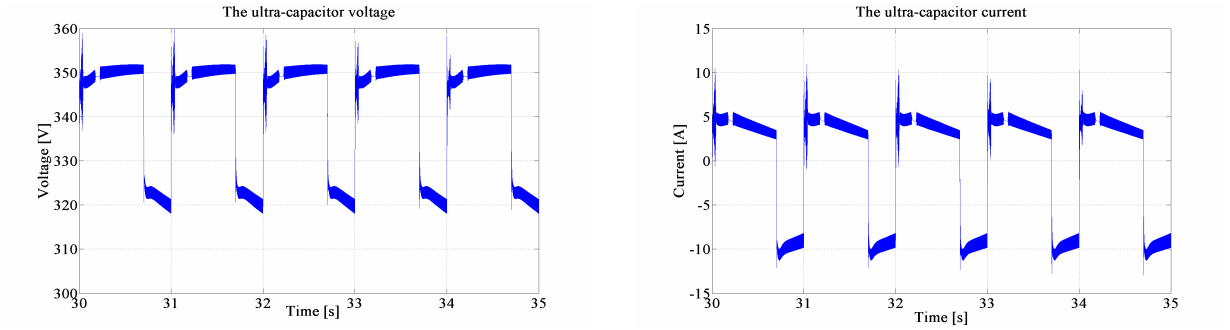
Fig. 13.13 Simulated waveforms of the ultra-capacitor voltage and current when the load is cycling 10% - 100% -10%. The bus voltage is v_{BUS}=650V, the mains phase-to-phase voltage V_{MAINS}=400Vrms, the dc bus capacitor C_{BUS}=820μF and the boost voltage controller bandwidth is f_{BOOST}=50Hz.

The system behavior is simulated when the mains peak power filter mode is active (the voltage controller bandwidth is f_{BOOST}=1Hz). Fig. 13.14 shows the dc bus voltage and the mains current waveforms. The dc bus voltage regularly commutates between V_{BUSmin}=645V and V_{BUSmax}=655V. The mains current is slightly modulated, but with much lower variation in comparison the previous case. Fig. 13.15 shows the ultra-capacitor voltage and current waveforms. The current commutates between -9A (full load on the dc bus side) and 5A (light load on the dc bus side). Discontinuity is the ultra-capacitor voltage is in the voltage drop on the ultra-capacitor internal resistance R_{C0}.



(a) (b)

Fig. 13.14 Simulated waveforms of the dc bus voltage v_{BUS} and the mains i_{MAINS} current when the load is cycling 10% - 100% -10%. The bus voltage is v_{BUS}=650V, the mains phase-to-phase voltage V_{MAINS}=400Vrms, the dc bus capacitor C_{BUS}=820μF and the boost voltage controller bandwidth is f_{BOOST}=1Hz.



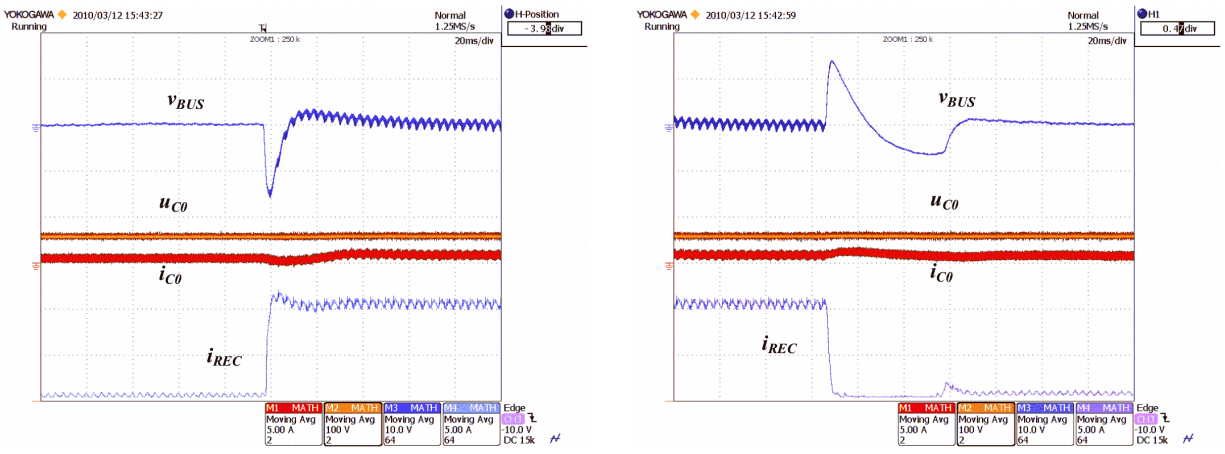
(a) (b)

Fig. 13.15 Simulated waveforms of the ultra-capacitor voltage and current when the load is cycling 10% - 100% -10%. The bus voltage is v_{BUS}=650V, the mains phase-to-phase voltage V_{MAINS}=400Vrms, the dc bus capacitor C_{BUS}=820μF and the boost voltage controller bandwidth is f_{BOOST}=50Hz.

13.3.2. Experimental Results

13.3.2.1. The DC Bus Voltage Controller $G_{BUS(REF)}$ Performance

Fig. 13.16 illustrates the functionality of the dc bus voltage boost controller, G_{VBUS}, in presence of a step change in the dc bus load. Fig (a) shows the rectifier current, ac component of the dc bus voltage and the ultra-capacitor voltage and current when the dc bus load is stepped from 10% to 110%. The controller response time is approximately 10ms, while the voltage undershoot is approximately -15V. Fig. 13.16 (b) shows the waveforms when the load is stepped from 110% to 10%. The voltage overshoot is approximately 12V. The controller response time is slightly greater than that of the previous case. The reaction time is extended because the rectifier current is limited at zero. It cannot be negative because the input rectifier is uni-directional device. The ultra-capacitor current remains zero, because it should not be power flow between the ultra-capacitor and the drive.



(a) (b)

Fig. 13.16 Experimental waveforms of the rectifier current i_{REC} [5A/div], the ac component of the dc bus voltage v_{BUS} [10V/div], the ultra-capacitor voltage u_{C0} [100V/div] and current i_{C0} [5A/div]. a) The dc bus load step from 10% to 110%, and b) from 110% to 10%. V_{BUS}=650V, V_{MAINS}=400Vrms, L_0=325μH, C_{BUS}=820μF and f_{BOOST}=50Hz.

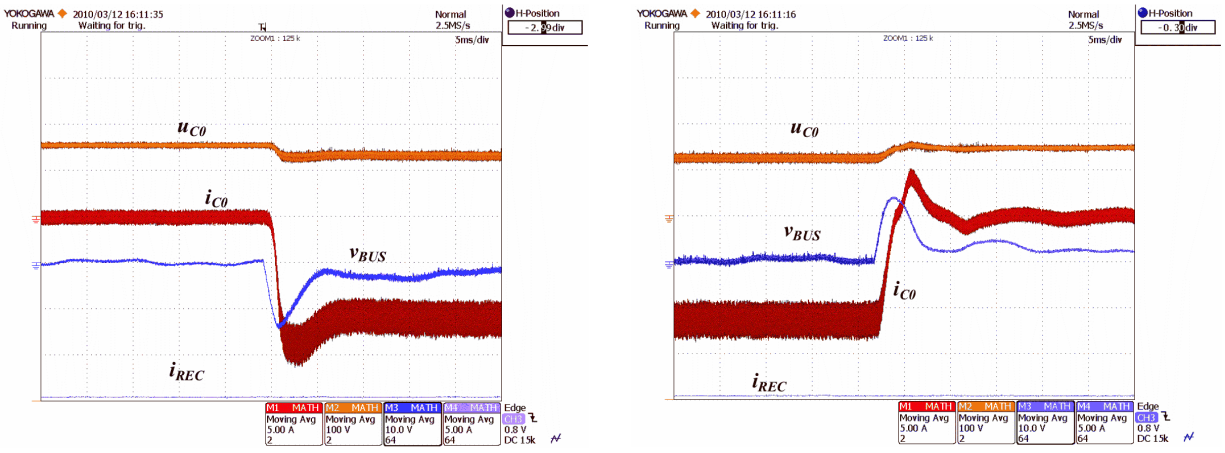
13.3.2.2. The DC Bus Voltage Controller G_{BUSmax} Performance

Fig. 13.17 illustrates the functionality of the dc bus voltage braking controller, $G_{VBUSmax}$. The ultra-capacitor is charged on 550V. Fig. 13.17 (a) shows the ultra-capacitor voltage and current, ac component of the dc bus voltage and rectifier current when the drive switches from stand-by mode to the ultra-capacitor mode. The controller response time is approximately 5 ms, while the voltage undershoot is approximately -13V. Fig. 13.17 (b) shows the waveforms when the drive switches from the ultra-capacitor mode to the stand-by mode. The voltage overshoot is approximately 12V. The controller response time is similar to the previous one.

13.3.2.3. The Mains Peak Power Smoothing Controller Performance

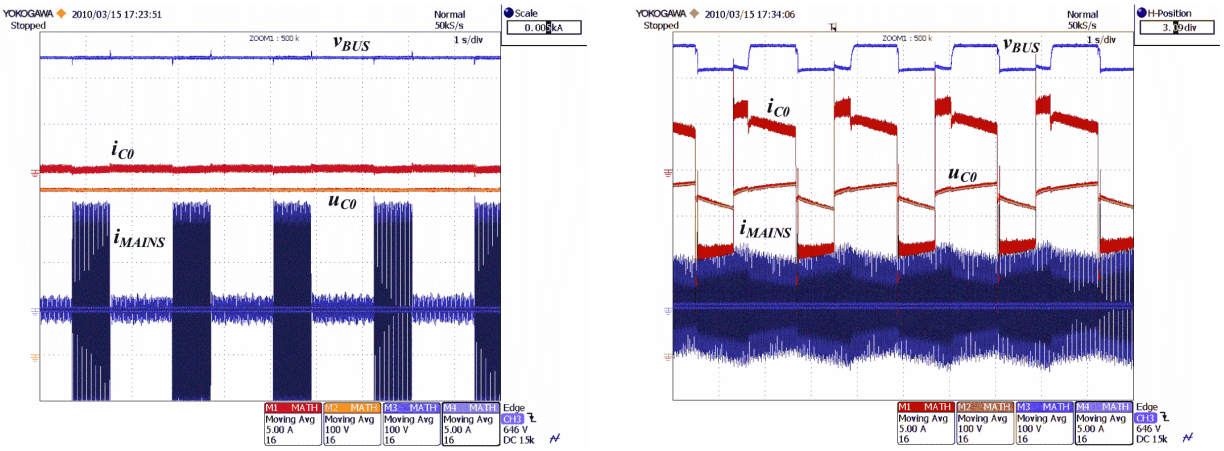
The capability of the drive system to reduce the mains peak power is tested and results are illustrated in Fig. 13.18 . The waveforms of the ultra-capacitor voltage u_{C0} and current i_{C0}, the dc bus voltage v_{BUS} and the mains current i_{MAINS} are shown. The dc bus load is cycling between 10% and 100% with repetition period of 2.2s and duty cycle of 40%. Fig. 13.18 (a) illustrates a case when the peak power filtering function is deactivated (the dc bus voltage boost controller bandwidth is 50Hz). As one can see from the waveform, the dc bus voltage is well regulated at the reference $V_{BUS(REF)}$=650V. The ultra-capacitor current is zero. The mains current is modulated with the load and it varies from 1A up to 11A.

Fig. 13.18 (b) illustrates a case when the peak power filtering function is activated (the dc bus voltage boost controller bandwidth is 1Hz). The dc bus voltage is well regulated at two different references V_{BUSmax}=675V and V_{BUSmin}=625V. The ultra-capacitor current commutates between -8A (the dc bus load is 100%) and 6A (the dc bus load is 10%). The mains current magnitude is approximately 6A, continuous without significant variations.



(a) (b)

Fig. 13.17 Experimental waveforms of the dc bus voltage v_{BUS} [10V/div] and the mains i_{MAINS} current [5A/div], the ultra-capacitor voltage u_{C0} [100V/div] and current i_{C0} [5A/div]. a) Transition from stand-by to the ultra-capacitor motoring mode and b) transition from the ultra-capacitor motoring mode to stand-by mode. V_{BUS}=675V, u_{C0}=550V, V_{MAINS}=400V, L_0=325μH, C_{BUS}=820μF and f_{BOOST}=50Hz.



(a) (b)

Fig. 13.18 Experimental waveforms of the dc bus voltage v_{BUS} [100V/div] and the mains current i_{MAINS} [5A/div] the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div], when the load is cycling (10% to 100% to 10%). V_{BUS}=650V, V_{MAINS}=400V, C_{BUS}=820μF,P_{LOAD}=5500W. a) f_{BOOST}=50Hz and b) f_{BOOST}=1Hz.

14. CONCLUSION

In this part of the dissertation, a new solution for the ultra-capacitor based regenerative electric drive has been proposed. The proposed solution intents to successfully solve some the technical issues that still exist in the application of controlled electric drives: 1) Saving of the braking energy, 2) extension of the drive system ride-through capability (immunity on the mains interruption), 3) the drive input current quality, 4) the drive dc bus voltage control, 5) single phase operation and 6) smoothing of the mains peak power.

The proposed solution has been theoretically analysed. The analyses results are confirmed by the Matlab/Simulink simulation and a set of experiments on an industrial prototype. The conversion efficiency has been computed and is between 97% and 99%. Please, note that the ultra-capacitor efficiency is excluded from this calculation. As it was discussed in chapter 3, the ultra-capacitor efficiency strongly depends on the capacitor size and conversion power, the smaller capacitor the lower efficiency. Therefore, efficiency of the entire drive system depends on the ultra-capacitor size.

In comparison to state of the art solutions, such as regenerative rectifiers or matrix converters, the proposed solution has the following advantages:

1) The system ride-through capability is extended. The drive autonomy time is a design parameter. Depending on the application, the ride-through time could be extended up to 15s. Above this, it is not cost effective to use the ultra-capacitors. Instead, electrochemical battery can be better solution. This limit will move up with development of the new generation of ultra-capacitors [72].

2) The system functionality, including braking capability is not linked to the mains reliability.

3) Operation of the drive system in single-phase supply mode is possible.

4) The mains peak power is controlled and the drive effects on the mains are reduced. This is particularly important in case of a weak supply network. Also, smoothing of the input power allows better sizing of the drive installation (smaller cabling cabinet, fuses and contactors).

A disadvantage of the proposed solution is the input current total harmonic distortion (THD) that cannot be lower than 30%. However, according to the existing standards [13], THD of 30% is sufficient for general purpose industrial drive applications.

PART FIVE: CONCLUDING REMARKS AND PERSPECTIVES

15. THE DISSERTATION CONTRIBUTION

Contribution of the dissertation could be summarized as follows:

- **The Ultra-capacitor Application in Power Conversion**

A comprehensive analysis of the ultra-capacitor as an energy storage device for power conversion applications has been performed. The ultra-capacitor macro model has been discussed. The conversion losses model, which takes into account frequency of the capacitor current and the frequency dependent resistance of the capacitor, has also been developed.

- **Parallel Connected Energy Storage Device for Controlled Electric Drives**

Regenerative controlled electric drive with braking capability and extended ride-through capability, using parallel connected ultra-capacitor as an energy storage device has been extensively analysed. Such a drive concept allows saving and recovery of the drive braking energy in most of controlled electric drive applications. Moreover, the drive ride-through capability can be extended, depending on an application need.

- **Interface DC-DC Converter**

Three-level dc-dc converter as interface between the ultra-capacitor and the controlled electric drive has been proposed and discussed. The advantages of the three-level dc-dc converter have been clearly identified and discussed.

- **The System Model and Control Scheme**

Dynamic nonlinear and small signal linear model of the controlled electric drive with the ultra-capacitor and dc-dc converter has been developed. The model takes into account all the relevant effects that are present in such a complex power conversion system. A novel control scheme has been also proposed. The control scheme allows control of the ultra-capacitor current, the ultra-capacitor state of the charge (SOC) and the dc bus voltage. The advantages of the proposed control scheme have been identified and discussed.

- **Three-terminal Power Factor Correction Device**

The mains current quality, dc bus voltage control and operation on single-phase supply have been discussed. A novel boost dc-dc converter based on the half-dc-bus-voltage rated topology has been proposed as a solution for the above-mentioned issues. The new topology has been theoretically analysed and the concept verified by a set of experiments. Modelling aspects and control scheme have been discussed. Particular attention has been paid on the model of the resonant dc-dc converter that is used to balance the dc bus mid-point voltage. The advantages of the new topology have been clearly identified and discussed.

- **Three-terminal Power Factor Correction and Energy Storage Device**

The three-terminal energy storage and power factor correction device for controlled electric drive applications has been proposed. The proposed three-terminal device is a

solution that solves some of the technical issues that still exist in application of controlled electric drives. The proposed solution has been deeply analysed and the concept verified by a set of experiments. The advantages and disadvantages have been clearly identified and discussed

o Publications

Most of the work presented in the dissertation is in publication and review process for *IEEE Transaction on Industrial Electronics.*

[1] **Petar J. Grbović,** Philippe Delarue and Philippe Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-DC-BUS-voltage rated boost converter: Modeling and control aspects," *IEEE Trans. Industrial Electronics*, in review process.

[2] **Petar J. Grbović,** Philippe Delarue, Philippe Le Moigne and Patrick Bartholomeus, "The Ultra-capacitor Based Regenerative Controlled Electric Drives with Power Smoothing Capability," *IEEE Trans. Industrial Electronics*, accepted for publication.

[3] **Petar J. Grbović,** Philippe Delarue, Philippe Le Moigne and Patrick Bartholomeus, "A Three-Terminal Ultra-Capacitor Based Energy Storage and PFC Device for Regenerative Controlled Electric Drives," *IEEE Trans. Industrial Electronics*, accepted for publication.

[4] **Petar J. Grbović,** Philippe Delarue, Philippe Le Moigne and Patrick Bartholomeus "Modeling and control of the ultra-capacitor based regenerative controlled electric drive system," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2087290, 2010.

[5] **Petar J. Grbović,** Philippe Delarue and Philippe Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-DC-BUS-voltage rated boost converter," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2050757, 2010.

[6] **Petar J. Grbović,** Philippe Delarue, Philippe Le Moigne and Patrick Bartholomeus, "Regenerative controlled electric drive with extended ride-through capability using an ultra-capacitor as energy storage device," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2048838, 2010.

[7] **Petar J. Grbović,** Philippe Delarue, Philippe Le Moigne and Patrick Bartholomeus, "A bi-directional three-level dc-dc converter for the ultra-capacitor applications," *IEEE Trans. Industrial Electronics*, Vol 57. No.10, pp. 3415-3430, October 2010.

16. CONCLUSIONS AND PERSPECTIVES

16.1. General conclusion

16.1.1. The Ultra-capacitor in Electric Drives and Other Power Conversion Applications

The ultra-capacitor as an energy storage device dedicated for power conversion has been discussed in the first part of the dissertation. In comparison to state of the art electrochemical batteries, ultra-capacitors have higher power density, higher efficiency, longer life time and greater cycling capability. In comparison to state of the art electrolytic capacitors, ultra-capacitors have higher energy density. All those advantages make ultra-capacitors the most suitable candidate for power conversion applications with a need for short-term energy storage, up to 15s. Some of the possible applications are industrial controlled electric drives, hoisting applications, power transmission/distribution networks, traction drives and UPS in building and IT centres.

State of the art ultra-capacitor technology is the double layer capacitor with activated carbon electrodes. Beside this technology, there are four different technologies under development: 1) Nano tube capacitor, 2) Nano-gate capacitor, 3) EeStore high voltage multilayer capacitor and 4) Mega-farad ultra-capacitor. All the technologies under development promise higher energy density than state of the art ultra-capacitors. Some of them, for example technology 3) and 4), promise energy density even greater than state of the art electrochemical batteries.

The ultra-capacitor macro model has been discussed. Proper electrical model is essential for the ultra-capacitor losses and temperature evaluation and the conversion system control analysis and synthesis. The first order RC model is sufficiently accurate if dominant frequency of the ultra-capacitor current is well below or above the capacitor cut-off frequency. Otherwise, the second or higher order model is necessary to accurately compute the capacitor losses and internal temperature. For the most commercially available ultra-capacitors, lower cut-off frequency is around 0.1Hz, while the upper cut-off frequency is around 10Hz. The first order RC model is sufficient for analysis and synthesis of the power converter controllers.

The concept of the ultra-capacitor based regenerative electric drive has been discussed in part two of the dissertation. The ultra-capacitor is employed as the energy storage device to store the drive braking energy and restore the energy whenever it is possible. Moreover, the ultra-capacitor is used as an emergency power supply in case of the mains interruption. Unlike electrochemical batteries, the ultra-capacitor state of charge (SOC) strongly depends on the terminal voltage. Thus, it is not practical and convenient to connect the ultra-capacitor directly to the controlled electric drive. An interface dc-dc converter is necessary. State of the art topologies are discussed and the new three-level dc-dc converter topology is proposed. The proposed topology is analysed and design guidelines are given. Model of the entire conversion system is developed and new control scheme is proposed. Objective of the proposed control is to control the ultra-capacitor current and the dc bus mid-point voltage. The second control objective is to asymptotically regulate the dc bus voltage at desired

reference, depending on the operating mode. The ultra-capacitor state of charge (SOC) control is the third control objective.

In comparison to state of the art solutions, such as back-to-back and matrix converters, the proposed ultra-capacitor based controlled electric drive converter shows the following advantages.

- The system ride-through capability is extended. The drive autonomy is a design parameter. Depending on the application, the ride-through time can be extended up to 15s. Above this, it is not cost effective to use the ultra-capacitors. Electrochemical batteries are more suitable solution. This limit will move up with development of the new generation of ultra-capacitors.
- The system functionality, including braking capability and reliability is not linked to the mains reliability.

Regarding to the three-level interface dc-dc converter, the following advantages compare to state of the art topologies are identified.

- The semiconductors losses are smaller than that of the two-level topology and isolated topologies.
- The output inductor is smaller than that of the ordinary two-level topology. The inductor size depends on the ultra-capacitor minimum voltage, and varies between 25% and 50% of that of the two-level converter.
- The input filter capacitor is smaller too. The capacitor volume varies between 10% and 25% of that of the two-level converter.

16.1.2. Novel Diode Boost Rectifier

The novel three-phase diode boost rectifier using the half-dc-bus-voltage-rated topology has been proposed and discussed in part three of the dissertation. The proposed boost converter consists of two dc-dc converters and two series connected dc bus capacitors. The first converter regulates the rectifier current and boosts the dc bus voltage above the mains phase-to-phase peak voltage. This converter is state of the art dc-dc converter, which is connected on the rectifier plus rail, the dc bus plus rail and the dc bus capacitors mid-point. The second dc-dc converter is an auxiliary converter that assists to the first one. This converter is a variant of the series resonant converter that operates in discontinuous conduction mode, type 1. Nonlinear model and small signal model of the entire rectifier have been discussed. Particular attention has been paid on the auxiliary resonant dc-dc converter model. Control scheme has been proposed and validated by simulation and a set of experiments.

The advantages of the proposed boost rectifier compared to the ordinary single-switch and double-boost rectifier can be summarized as follows.

- The switches utilization factor is higher than that of state of the art solutions. Therefore, the switches cost is lower.
- The switches voltage rating is half of that of the single-switch boost rectifier. Thus, better and more efficient devices could be used.
- The boost inductor is smaller than the inductor of single-switch boost rectifier.
- The conversion efficiency is greater than that of state of the art solutions.

Some inconveniences of the proposed boost rectifier are identified too.

- The need for an auxiliary dc-dc converter to control the dc bus capacitors mid-point voltage. This converter is rated on a fraction of the total conversion power. Therefore the conversion losses can be quite low in comparison to the total conversion losses.
- The input current total harmonic distortion factor (THD) and partially weighted harmonic distortion factor (PWHD). Because of operation principle of three-phase diode boost rectifier operating in continuous conduction mode (CCM), the THD cannot be reduced below 30%, while the PWHD is around 55%. However, according to the existing standards [13], THD of 30% is sufficiently low for industrial drive applications, while PWHD is slightly above the limit. The PWHD, however, can be reduced below 46% as required by the standard by the use of 6^{th} harmonic injection [140].

The new boost rectifier is an effective replacement for passive diode rectifiers as well as single-switch and double boost rectifier. This topology could be used in three-phase supplied and single –phase supplied three-phase controlled electric drives.

16.1.3. All Together

In last part of the dissertation, a compilation of the parallel-connected energy storage device (discussed in part two of the dissertation) and the new boost rectifier (discussed in part three of the dissertation) is proposed. The proposed solution intents to successfully solve the following technical issues that still exist in application of controlled electric drives: 1) Saving of the braking energy, 2) extension of the drive system ride-through capability (immunity on the mains interruption), 3) the drive input current quality, 4) the drive dc bus voltage control, 5) single phase operation and 6) smoothing of the mains peak power. The proposed solution is theoretically analysed and design guidelines are given. The concept has been validated by simulation and a set of experiments.

Compared to state of the art solutions, such as regenerative back to back and matrix converters, the proposed solution has the following advantages.

- The system ride-through capability is extended.
- The system functionality, including braking capability is not linked to the mains reliability.
- Single-phase supply operation is possible too.
- The mains peak power is controlled and the drive effects on the mains are reduced. This is particularly important if the electric drive is supplied from a weak public supply network. Moreover, smoothing of the input power allows better sizing of the drive installation (smaller cabling cabinet, fuses and contactors).
- The conversion efficiency is greater that that of state of the art solutions.

16.2. Perspectives for Future Work

Perspectives for future work on the project can be summarized as follows.

16.2.1. Commissioning and Self–tuning of the System Controllers

The first objective for future work on this project would be the system commissioning and self-tuning process. Two parameters have to be well known for proper tuning of the system controllers: 1) Capacitance of the dc bus capacitor, and 2) capacitance of the ultra-capacitor. The first one is important for the dc bus voltage controllers' adjusment, while the second one is important for the ultra-capacitor state of charge (SOC) controller adjustment.

16.2.2. On-line Monitoring and the Ultra-capacitor Life Time Estimation

The ultra-capacitor lifetime prediction is another aspect to be considered. In certain applications, such as critical industrial processes [10], unexpected interruptions of the system are not allowed. Hence, failures such as end of life of the ultra-capacitor must be predicted and preventive replacement done on time. For this, on-line lifetime estimation is essential. Some work has been already done in field of electrolytic capacitors failure prediction [141]. Similar concept can be used to predict end of life of the ultra-capacitor.

REFERENCES

[1] T. M. Jahns, and E. L. Owen, "AC adjustable-speed drives at the millennium: how did we get here?," *IEEE Trans. Power Electronics*, Vol. 16, No. 1, pp. 17-25, January 2001.

[2] B. Bose (Editor), "Adjustable speed ac drive systems," *IEEE Press*, pp. 1-23, 1980.

[3] S. N. Vukosavic, "Digital control of electric drives," Springer, 2007.

[4] B. J. Baliga, "Power semiconductor devices for variable frequency drives," Proceedings of the *IEEE*, pp. 1112-1122, 1994.

[5] Sang-Min Kim and Seung-Ki Sul, "Control of rubber tyred gantry crane with energy storage based on supercapacitor bank," *IEEE Trans. Power Electronics*, Vol. 21, No. 5, pp. 1420-1427, September 2006.

[6] A. T. de Almedia, F. J. T. E. Ferriera, and D. Both, "Technical and economical consideration in the application of variable speed drives with electric motor systems", *IEEE Trans. Industry Applications*, Vol. 41, No. 1, pp. 188-199, January/February 2005.

[7] R. A. Epperly, F. L. Hoadley and R. W. Piefer, "Considerations when applying ASD's in continuous processes," *IEEE Trans. Industry Applications*, Vol. 33, pp 389-396, March/April 1997.

[8] C. J. Melhorn, A. Braz, P. Hofmann and R. J. Mauro, "An evaluation of energy storage techniques for improving ride-through capability for sensitive customers on underground networks," *IEEE Trans. Industry Applications*, Vol. 33, No. 4, pp.1083-1095, July/August 1997.

[9] A. Van Zyl, R. Spee, A. Faveluke and S.Bhowmik, "Voltage sag ride-through for adjustable-speed drives with active rectifiers," *IEEE Trans. Industry Applications*, Vol. 34, pp 1270-1277, November/December 1998.

[10] A. von Jouanne, P. N. Enjeti and B. Banerjee, "Assessment of ride-through alternatives for adjustable-speed drives," *IEEE Trans. Industry Applications*, Vol. 35, No. 4, pp. 908-916, July/August 1999.

[11] M; H.J. Bollen, "Understanding power quality problems, voltage sags and interruptions", IEEE Press Series on Power Engineering, 2000.

[12] D. A. Paice, "Power electronic converter harmonics – multipulse methods for clean power," IEEE PRESS, New York, (1995).

[13] International standard, IEC 610006-12-3.

[14] A. Rufer, D. Hotellier and P. Barrade, "A supercapacitor-based energy storage substation for voltage compensation in weak transportation networks," *IEEE Trans. Power Delivery*, Vol.19 No. 2, pp 629 – 636, April 2004.

[15] A. Rufer and P. Barrade, "A supercapacitor-based energy-storage system for elevators with soft commutated interface," *IEEE Trans. Industry Applications*, Vol. 38, No.5, pp. 1151-1159, September/October 2002.

[16] J. R. Rodríguez, J. W. Dixon, J. R. Espinoza, J. Pontt and P. Lezana," PWM Regenerative Rectifiers: State of the Art," *IEEE Trans. Industrial Electronics*, Vol. 51, No. 1, pp.5-22, February 2005.

[17] M. Venturini, "A new sine wave in sine wave out, conversion technique which eliminates reactive elements," in *Proc. POWERCON 7*, 1980, pp. E3_1-E3_15.

[18] P. W. Wheeler, J. Rodríguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review," *IEEE Trans. Industrial Electronics*, Vol. 42, No. 2, pp.276-288, April 2002.

[19] C. Attaianese, V. Nardi, and G. Thomasso, "High performance supercapacitor recovery system for industrial drive applications," In Proc. of APEC Vol. 3, 2004, pp. 1635-1641.

[20] S. Tominaga, I. Suga, H. Araki, H. Ikejima, M. Kusuma and K. Kobayashi, "Development of energy saving elevator using regenerated power storage system," In proc. of PCC-Osaka 2002, pp. 890-895.

[21] J. L. Duran-Gomez, P. N. Enjeti, A. Von Jouanne, "An approach to achieve ride-through of an adjustable-speed drive with flyback converter modules powered by super capacitors," *IEEE Trans. Industry Applications*, Vol. 38, No. 2, pp.514-522, March/April 2002.

[22] W. Tongzhen, W. Sibo and Q. Zhiping,"A supercapacitor based ride-through system for industrial drive applications," In Proc. of 2007 IEEE International Conference on Mechatronics and Automation, pp.2833-2837, 2007, Harbin, China.

[23] Z. Chlodnicki, and W. Koczara, "Supercapacitor storage application for reduction drive negative impact on supply grid," In Proc. of Compatibility in Power Electronics, 2005, pp. 78-84. 2005.

[24] K. Inoue, K. Ogata and T. Kato, "An efficient induction motor drive method with a regenerative power storage system driven by an optimal torque," In Proc. of IEEE Power Electronics Specialist Conference, PESC 2008, pp. 359-364.

[25] S. Eckroad, "Handbook of Energy Storage for Transmission or Distribution Applications," EPRI Technical Update, December 2002.

[26] R. Kotz, M. Carlen, "Principles and applications of electrochemical capacitors," Electrochemical Acta, Vol. 45, pp. 2483-2498, May 2000.

[27] L. Solero, A. Lidozzi and J. A. Pomilio, "Design of multiple-input power converter for hybrid vehicle," *IEEE Trans Power Electronics*, Vol. 20, No. 5, pp. 1007-1016, September 2005.

[28] M. B. Camara, H. Gualous, G. Gustin, A. Berthon and B. Dakyo, "DC-DC converter design for supercapacitor and battery management in hybrid vehicle applications-polynomial control strategy," *IEEE Trans Industrial Electronics*, Vol. 57, No. 2, pp. 587-597, February 2010.

[29] A. L. Allegre, A. Bouscayrol, P. Delarue, P Barrrade, E. Chattot and S. E. Fassi, "Energy storage system with supercapacitor for an innovative subway," *IEEE Trans Industrial Electronics*, accepted for future publications.

[30] L. Jih-Sheng and D. J. Nelson, "Energy management power converters in hybrid electric and fuel cell vehicle," *Proceedings of IEEE*, Vol. 95, No. 4, pp.766-777, April 2007.

[31] A. Rufer, "Power-electronic interface for a supercapacitor-based energy-storage substation in DC-transportation networks", In Proc. EPE2003.

[32] R. M. Schupbach and J. C. Balda, "35kW ultracapacitor unit for power management of hybrid electric vehicle: bi-directional dc-dc converter design," In Proc of PESC'04, pp. 2157-2163, Aachen 2004.

[33] W. Lhomme, P. Delarue, P. Barrad, A. Bouscaroy, and A. Rufer, "Design and control of a supercapacitor storage system for traction applications", In Proc. of IAS 2005, pp. 2013-2020.

[34] L. Gao, R. A. Dougal and S. Liu, "Power enhancement of an actively controlled baterry/ultracapacitor hybrid," *IEEE Trans. Power Electronics*, Vol. 20, No. 1, pp. 236-243, January 2005.

[35] M. Ortúzar, J. Moreno and J. Dixon, "Ultracapacitor-based auxiliary energy system for an electric vehicle: implementation and evaluation," *IEEE Trans. Industrial Electronics*, Vol. 54, No. 4, pp. 2147-2156, August 2007.

[36] Zhang, J.-S. Lai, R.-Y. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc-dc converters," *IEEE Trans. Power Electronics*, Vol. 22, No. 4, pp. 1145-1153, July 2007.

[37] S. Inoue and H. Akagi, "A bidirectional dc-dc converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electronics*, Vol. 22, No. 6, pp. 2299-2306, December 2007.

[38] G. Ma, W. Qu, G.Yu, Y. Liu, N. Liang and W. Li, "A zero-voltage-switching bidirectional dc-dc converter with state analysis and soft-switching-oriented design consideration," *IEEE Trans. Industrial Electronics*, Vol. 56, No. 6, pp. 2174-2184, June 2009.

[39] R. Xinbo, L. Bin Li, C. Qianhong, T. Siew-Chong, C. K. Tse, "Fundamental considerations of three-level dc–dc converters: Topologies, analyses, and control," *IEEE Trans. Circuits and Systems I: Regular Papers*, Vol. 55, No. 11, pp. 3733 – 3743, December 2008.

[40] K. Jin, M. Yang, X. Ruan, M. Xu, "Three-level bi-directional converter for fuel cell/battery hybrid power system," Accepted for future publications in *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2009.2031197.

[41] P. J. Grbović, "High-voltage auxiliary power supply using series-connected MOSFETs and floating self-driving technique," *IEEE Trans. Industrial Electronics*, Vol. 56, No. 5, pp. 1446-1455, May 2009.

[42] G. Guidi, T. M. Undeland, and Y. Hori, "An optimized converter for battery supercapacitor interface", In proc. of PESC'07, pp. 2976-2981.

[43] P. Thounthong, S. Raël, and B. Davat, "Control strategy of fuel cell and supercapacitors association for a distributed Generation system," *IEEE Trans. Industrial Electronics*, Vol. 54, No. 6, pp. 3225-3233, December 2007.

[44] L. Gao, R. A. Dougal and S. Liu, "Power enhancement of an actively controlled baterry/ultracapacitor hybrid," *IEEE Trans. Power Electronics*, Vol. 20, No. 1, pp. 236-243, January 2005.

[45] M. B. Camara, H. Gualous, F. Gustin and A. Berthon, "Design and new control of DC-DC converters to share energy between supercapacitors and batteries in hybrid vehicles," *IEEE Trans. Vehicular Technology*, Vol. 57, No. 5, pp.2721-2735, September 2008.

[46] A. Payman, S. Piefederici and F. Meibody-Tabar, "Energy management in a fuel cell/supercapacitor multisource/multiload electric hybrid system," IEEE Trans Power Electronics, Vol. 24, No. 12, pp.2681-2691, December 2009.

[47] W. Greenwell and A. Vahidi, "Predictive control of voltage and current in a fuel cell-ultracapacitor hybrid," IEEE Trans Industrial Electronics, Vol. 57, No. 6, pp. 1954-1963, June 2010.

[48] P. J. Grbović, P. Delarue, P. Le Moigne and P. Bartholomeus, "Regenerative controlled electric drive with extended ride-through capability using an ultra-capacitor as energy storage device," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2048838.

[49] A. R. Prasad, P. D. Ziogas and S. Manias, "An active factor correction technique for three-phase diode rectifiers," *IEEE Trans. Power Electronics*, Vol. 6. No. 1, pp.83-92, January 1991.

[50] A. W. Kelley, and W. F. Yadusky, "Rectifier design for minimum line current harmonics and maximum power factor," *IEEE Trans. Power Electronics*, Vol. 7, No. 2, pp. 332-341, April 1992.

[51] M. Rastogi, R. Naik, and N. Mohan, "A Comparative Evaluation of Harmonic Reduction Techniques in Three-phase Utility Interface of Power Electronic Loads," *IEEE Trans. Industry Applications*, Vol. 30, No. 5, pp. 1149-1155, September/October 1994.

[52] J. W. Kolar, H. Ertl and F. C. Zach, "A comprehensive design approach for a tree-phase high frequency single switch discontinuous mode boost power factor corrector based on analytically derived normalized converter component rating," *IEEE Trans. Industry Applications*, Vol. 31, No. 3, pp.569-582, May/June 1995.

[53] E. H. Ismail, and R. Erickson, "Single-switch 3 φ pwm low harmonic rectifiers," *IEEE Trans. Power Electronics*, Vo. 11, No. 2, pp. 338-346, March 1996.

[54] M. Tou, K. Al-Haddad, G. Olivier, and V. Rajagopalan, "Analysis and design of single-controlled switch three-phase rectifier with unity power factor and sinusoidal input current," *IEEE Trans. Power Electronics*, Vol. 12, No. 4, pp 608-614, July 1997.

[55] Y. Jang, and M. Jovanovic, "A new input-voltage feed-forward harmonic-injection technique with nonlinear gain for single-switch, three phase, DCM boost rectifiers," *IEEE Trans. Power Electronics*, Vol. 28, No. 1, pp. 268-277, March 2000.

[56] D. Dah-Chuan Lu, D. Ki-Wai Cheng, and Yim-Shu Lee, "A single switch continuous conduction mode boost converter with reduced reverse recovery and switching losses," *IEEE Trans. Industrial Electronics*, Vol. 50, No. 4, pp. 767-776, August 2003.

[57] Y. Jang and M. M. Jovanovic´, "A new, soft switching, high power factor boost converter with IGBTs," *IEEE Trans. Power Electronics*, Vol. 17, No. 4, pp. 469-476, July 2004.

[58] Y. Jang, M. M. Jovanovic´, Kung-Hui Fang, and Yu-Ming Chang, "High power factor soft switched boost converter," *IEEE Trans. Power Electronics*, Vol. 21, No. 1, pp.98-104, July 2007.

[59] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Conf. Rec. IEEEAPEC'95*, 1995, pp. 434–439.

[60] O. Garica, M. D. Martinez-Avial, J. A. Cobos, J. Uceda, J. Gonzales, and J. A. Navas, "Harmonic reducer converter", *IEEE Trans. Industrial Electronics*, Vol. 50, N_0 2, pp. 322-327, April 2003.

[61] H. Ertl, J. W. Kolar and F. C. Zach, "A constant output current three-phase diode bridge employing a novel "electronic smoothing inductor". Proc. of the international Conferences PCIM, Nürnberg, Germany, June 22 – 24, pp. 645 – 651, (1999).

[62] C. Klumpner, A. Timbus, F. Blaagjerg and P. Thogersen, "Adjustable speed drives with square-wave input current: A cost effective step in development to improve their performances," In IEEE Proc. Of IAS 2004, pp.600-607.

[63] H. Ertl and J. W. Kolar, "A constant output current three-phase diode bridge rectifier employing a novel "electronic smoothing inductor"," *IEEE Trans. Industrial Electronics*, Vol. 52, No.2, pp.454-461, April 2005.

[64] P. Pejovic, "Low harmonics three-phase diode bridge rectifiers based on the current injection principle," Academic Mind, Belgrade 2005.

[65] O. García, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A Survey ,"*IEEE Trans. Power Electronics*, Vol. 18, No. 3, pp. 749-755, May 2003.

[66] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Trans. Industrial Electronics*, Vol. 50, No. 5, pp. 962-981, October 2003.

[67] C. B. Jacobina, M.B. Correa, E.R. da Silva, A.M. Lima "Induction motor drive system for low-power applications", *IEEE Trans. Industry Applications*, Vol. 35, No. 1, January/February 1999.

[68] D.-C. Lee, Y.-S. Kim, "Control of single-phase-to-three-phase ac-dc-ac PWM converters for induction motor drives", *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 2, pp. 797-804, April 2007.

[69] B. E. Conway, "Electrochemical supercapacitors, scientific fundamentals and technological applications, "Kluwer Academic/Plenum Publisher, New York 1999.

[70] A. Schneuwly and R. Gallay, "Properties and applications of supercapacitors: From the state-of-the-art to future trends," In proc of PCIM 2000.

[71] V. Hermann, A. Schneuwly and R. Gallay, "High performance double-layer capacitor for power electronic applications," In. proc. of PCIM 2001.

[72] F. A. Burke, "Ultracapacitors: Present and Future," Proceedings of the Advanced Capacitor World Summit 2003, Washington, D.C., August 2003.

[73] Marin S. Halper, James C. Ellenbogen, "Supercapacitor: a brief overview," http://www.mitre.org. March 2006.

[74] S. Eckroad (project manager), "Electrochemical capacitors for utility applications," EPRI Final Report, August 2005.

[75] F.Belhachemi, S.Raiel and B. Davat, "A physical based model of power electric double-layer supercapacitors," In Proc. of Industry Applications Conference, Volume 5, pp. 3069 – 3076, 2000.

[76] S. Buller, E. Karden, D. Kok, and R. W. Doncker, "Modeling the dynamic behaviour of supercapacitors using impedance spectroscopy ," *IEEE Trans. Industry Application*, vol. 38, no. 6, pp. 1622-1626, November/December 2002.

[77] S. Buller, "Impedance-Based Simulation Models for Energy Storage Devices in advanced Automotive Power Systems," PhD Dissertation, *Institute for Power Electronics and Electrical Drives RWTH Aachen University*, February 2003.

[78] D. R. Middlebrook, V. Vorperian and J. Lindal, "The N Extra Element Theorem," *IEEE Trans Circuits and systems*. 1, Fundamental theory and applications, Vol. 45, No. 9, pp. 919-935, September 1998.

[79] D. Riu, N. Retière and D. Linzen, "Half-order modeling of supercapacitors," In proc. of Industry Applications Conference, pp. 2550-2554, 2004.

[80] R. Farande, M. Gallina and D.T. Son, "A new simplified model of double-layer capacitors," In Proc. of International conference Clean Electrical Power, ICCEP '07, pp. 706-710. 2007.

[81] T. Funaki and Takashi Hikihara, "Characterisation and modeling of the voltage dependency of capacitance and impedance frequency characteristics of packed EDLCs," *IEEE Trans Power Electronics*, Vol. 23, No. 3, pp. 1518-1525, May 2008.

[82] M. Kurtz, "Handbook of applied mathematics for engineers and scientists," McGRAW-Hill, Inc.

[83] D. Linzen, "Impedance-Based Loss Calculation and Thermal Modelling of Electrochemical Energy Storage Devices for Design Considerations of Automotive Power Systems," PhD Dissertation, *Institute for Power Electronics and Electrical Drives RWTH Aachen University*, December 2005.

[84] J. Schindall, "New [Old] Technologies for Energy Storage," NRC Emerging Technologies Study October 16, 2007.

[85] J. M. Miller, U. Deshpande, "Ultracapacitor technology: state of technology and application to active parallel energy storage systems," 17th International Seminar on Supercapacitors and Hybrid Energy Storage Systems, pp.9-25, December 2007.

[86] R. Signorelli, D. Ku, J. Kassakian and J. Schindall, "Fabrication and electrochemical testing of the first generation carbon-nanotube based ultracapacitor cell," 17th International Seminar on Supercapacitors and Hybrid Energy Storage Systems, pp.70-79, December 2007.

[87] R. Signorelli, J. Schindall, D, Sadoway, J. Kassakian, "High energy and power density nanotube ultracapacitor design, modelling, testing and predicting performance," 19th International Seminar on Supercapacitors and Hybrid Energy Storage Systems, December 2009.

[88] M. Okamura, K. Hayashi, T. Tanikawa and H. Ohta, "The nanogate-capacitor has finally been launched by our factory," In Proc of The 17th International Seminar on Double Layer Capacitors and Hybrid Energy Storage Devices December 10-12, 2007.

[89] R. D. Weir and C. W. Nelson, "Electrical energy storage unit (EESU) utilizing ceramic and integrated circuit technologies for replacement of electrochemical batteries," US Patent 7 033 4060 B2, April 2006.

[90] B. G. Ezzat, "New mega-farad ultracapacitors," *IEEE Trans Ultrasonics, ferroelectrics, and frequency control*, Vol. 56, No1, pp. 14-21, January 2009.

[91] LS Mtron ultra-capacitors data sheet, http://www.ultracapacitor.co.kr.

[92] P. J. Grbović, P. Delarue, P. Le Moigne and P. Bartholomeus, "A bi-directional three-level dc-dc converter for the ultra-capacitor applications," *IEEE Trans. Industrial Electronics*, Vol. 57, No. 10, pp.3415-3430, October 2010.

[93] S. Inoue and H. Akagi, "A bidirectional dc-dc converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electronics*, Vol. 22, No. 6, pp. 2299-2306, December 2007.

[94] M. Bartoli, A. Reatti and M. Kazimerczuk, "Modelling iron-powder inductors at high frequencies," In Proc; IAS, 1994, pp.1225-1232.

[95] M. K. Kazimiruczuk, G. Sancineto, G. Grandi and A. Massarini, "High-frequency small-signal model of ferrite core inductors," *IEEE Trans. Magnetics*, Vol. 35, No. 5, pp. 4185-4191, September 1999.

[96] G. Grandi, M. K. Kazimiruczuk, A. Massarin, U. Raggiani and G. Sancineto, "Model of laminated iron core inductors for high frequencies," *IEEE Trans. Magnetics*, Vol. 40, No. 4, pp.1839-1845, July 2004.

[97] J. Li, T. Abdallah and C. R. Sullivan, "Improved calculation of core loss with non sinusoidal waveforms," In Proc of IEEE Industry Application Society Annual Meeting, Oct. 2001, pp. 2203-2210.

[98] K. Venkatachalam, C.R. Sullivan, T. Abdallah and T. Tacca, "Accurate prediction of ferrite core loss with non sinusoidal waveforms using only Steinmetz parameters," In proc of IEEE Workshop on Computers in Power Electronics, June 2002, pp.1-6.

[99] W. A. Roshen, "A practical, accurate and very general core loss model for non-sinusoidal waveforms," *IEEE Trans. Power Electronics*, Vol. 22, No. 1, pp. 30-40, January 2007.

[100] P. J. Grbović, "Feed forward control of turn off performances of an IGBT in short circuit conditions", in Proc. EPE'07.

[101] L. Lorenz, G. Deboy and I. Zverev, "Matched pair of CoolMOS transistor with SiC schottky diode-advantages in applications," *IEEE Trans. Industry Applications*, Vol. 40, No. 5, pp.1265-1272, September/October 2000.

[102] W. Shen, "Design of high-density transformers for high-frequency high-power converters," PhD Dissertation, pp. 70-71, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, July 2006.

[103] http://www.mag-inc.com/design/software.

[104] B. J. Baliga, "Fundamentals of power semiconductor deices," Springer publisher.

[105] B. J. Baliga, "The future of power semiconductor devices technology," Proceedings of the IEEE, Vol. 89, No. 6, pp. 822-832, June 2001.

[106] R. W. Erickson and D. Maksimovic´, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2002.

[107] V. Vorperian, "Simplified Analysis of PWM Converters Using Model of PWM Switch Part I: Continuous Conduction Mode," *IEEE Trans. Aerospace and Electronic Systems*, Vol. 24, No. 3, pp. 490-496, May 1990.

[108] Siu-Chung Wong, C. K. Tse, M. Orabi and T. Ninomiya, "The method of double averaging: an approach for modeling power factor correction switching converters," *IEEE Trans. Circuits and systems-: Regular papers*, Vol. 53, No. 2, pp. 454-462, February 2006.

[109] V. A. Caliskan, G. C. Verghese and A. M. Stankovic´, "Multifrequency averaging of DC-DC converters, " *IEEE Trans. Power Electronics*, Vol. 14, No. 1, pp. 124-133, January 1999.

[110] X. Liu, A. J. Forsyth and A. M. Cross, "Negative input resistance compensator for a constant power load," *IEEE Trans. Industrial Electronics*, Vol. 54, No. 6, pp. 3188-3196, December 2007.

[111] J. Wang and D. Howe, "A power shaping stabilizing control strategy for dc power systems with constant power loads," *IEEE Trans. Power Electronics*, Vol. 23, No. 6, pp. 2982-2989, November 2008.

[112] F. A. Himmelstoss, J. W. Kolar and F. C. Zach, "Analysis of a smith-predictor-based control concept eliminating the right-half plane zero of continuous mode boost and back-boost DC-DC converters," In Proc. Of IECON'91, pp. 423-428.

[113] B. M. Kwon, H. S. Ryu, D. W. Kim and O. K. Kwon, "Fundamental limitations imposed by RHP poles and zeros in SISO systems," In Proc. of SICE 2001 Nagoya, pp.170-175.

[114] P. J. Grbović, P. Delarue, P. Le Moigne and P. Bartholomeus, "Modeling and control of the ultra-capacitor based regenerative controlled electric drive systems," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2087290, 2010.

[115] N. Mohan, T. M. Undeland and W. P. Robbins, "Power electronics; converters, applications and design," John Wiley & Sons, Inc, 1995.

[116] P. J. Grbović, P. Delarue and P. Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-DC-BUS-voltage rated boost converter," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2050757.

[117] L. Rossetto, *Member*, S. Buso, and G.Spiazzi," Conducted EMI issues in a 600W single phase boost PFC design," *IEEE Trans. Industry Application*, Vol. 36, No. 2, pp. 578-585, March/April 2000.

[118] S. Wang, P. Kong, and F. C. Lee, Fellow, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electronics*, Vol. 22, No. 4, pp.1410-1416, July 2007.

[119] T. Nussbaumer, K. Raggl, J. W. Kolar, "Design guidelines for interleaved single-phase boost PFC circuits," *IEEE Trans Industrial Electronics*, Vol. 56, No. 7, pp. 2559-2573, July 2009.

[120] M. Shen F. Z. Peng and L. M. Tolbert, "Multilevel dc-dc power conversion system with multiple dc sources," *IEEE Trans. Power Electronics*, Vol. 23, No.1, pp. 420-426, January 2008.

[121] Vorperian, "Analysis of resonant converters," PhD Thesis, California Institute of Technology, 1984.

[122] EPCOS Metallized Polypropylene (MKP/MFP) capacitors datasheet. http://www.epcos.com.

[123] Whi-Khi Chen (Editor),"The circuits and filters handbook," CRC Press, Second edition, 2002.

[124] P. R. K. Chetty, "Resonant power supplies: their history and status, "*IEEE Aerospace and Electronic Systems Magazine*, Vol. 7, No. 4, pp.23-29, April 1992.

[125] V. Vorperian, "Approximate small-signal analysis of the series and parallel resonant converters," *IEEE Trans. Power Electronics*, Vol. 4, No. 1, pp. 15-24, January 1989.

[126] J. M. Carrasco, E. Galvan, G. E. Valderrama, R. Ortega and A. M. Stankovic´," Analysis and experimentation of nonlinear adaptive controllers for the series resonant converter," *IEEE Trans. Power Electronics*, Vol. 15, No. 3, pp.536-544, May 2000.

[127] A. F. Witulski, A. F. Hernandez and R. W. Erickson, "Small signal equivalent circuit modelling of resonant converters," *IEEE Trans. Power Electronics*, Vol. 6, No. 1, pp.11-26, January 1991.

[128] M. E. Elbuluk, G. C. Verghese and J. G. Kassakian, "Sampled-data modelling and digital control of resonant converters," *IEEE Trans. Power Electronics*, Vol. 3, No. 3, pp344-354, July 1988.

[129] M. G. Kim and M. J. Youn, "A discrete time domain modelling and analysis of controlled series resonant converter," *IEEE Trans. Industrial Electronics*, Vol. 38, No. 1, pp. 32-40, February 1991.

[130] G. B. Jopung, J. G. Cho and G. H. Cho, "A generalised quantum resonant converter using a new quantum resonant module," *IEEE Trans. Power Electronics*, Vol. 7, No. 4, pp.666-672, October 1992.

[131] W. Levine (Editor), "The control handbook," *IEEE Press*, 1996.

[132] S. Buso and P. Mattaveli, "Digital control in power electronics," Morgan & Clayopool, 2006.

[133] P. J. Grbović, P. Delarue and P. Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-DC-BUS-voltage rated boost converter: Modeling and control aspects," *IEEE Trans. Industrial Electronics*, in review process.

[134] H. C. Chen, S. H. Li and C. M. Liaw, "Switch mode rectifier with digital robust ripple compensation and current waveform controls," *IEEE Trans Power Electronics*, Vol. 19, No. 2, pp. 560-566, March 2004.

[135] A. Prodic´, J. Chen, D. Maksimovic´and R. W. Erickson, "Self tuning digitally controlled low harmonics rectifier having fast dynamic response," *IEEE Trans Power Electronics*, Vol. 18, No. 1, pp. 420-428, January 2003.

[136] Prodic´, D. Maksimovic´ and R. W. Erickson, "Dead-zone digital controllers for improved dynamic response of low frequency rectifiers," *IEEE Trans Power Electronics*, Vol. 21, No. 1, pp. 173-181, January 2006.

[137] P. C. Krause, O. Wasynczuk and S. D. Sudhoff, Analysis of electric machinery and drive systems, IEEE Press Power Engineering Series, John Wiley & Sons Inc. Publications.

[138] P. Mattavelli and F. P. Marafao, "Repetitive-based control for selective harmonic compensation in active power filters," *IEEE Trans Industrial Electronics*, Vol. 51, No. 5, pp. 1018-1024, October 2004.

[139] G. Escobar, A. A. Valdez, J. Leyva-Ramos and P. Mattavelli, "Repetitive-based controller for a UPS inverter to compensate unbalance and harmonic distortion," *IEEE Trans Industrial Electronics*, Vol. 54, No. 1, pp. 504-510, February 2007.

[140] Apparatus and Method for Mains Harmonic Reduction in AC Drive Circuits, Patent application EP2124328 (A1), Siemens AG (D).

[141] H. Ma and L. Wang, "Fault diagnosis and failure prediction of aluminum electrolytic capacitors in power electronic converters," Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE, pp. 842-847.

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Books:

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Transactions and journals:

1. Petar J. Grbović, Philippe Delarue and Philippe Le Moigne, "The Ultra-capacitor Based Regenerative Controlled Electric Drives with Power Smoothing Capability," *IEEE Trans. Industrial Electronics*, acepted for publication.
2. Petar J. Grbović, Philippe Delarue and Philippe Le Moigne, "A Three-Terminal Ultra-Capacitor Based Energy Storage and PFC Device for Regenerative Controlled Electric Drives," *IEEE Trans. Industrial Electronics*, accepted for publication.
3. Petar J. Grbović, Philippe Delarue and Philippe Le Moigne, "Modelling and control of the ultra-capacitor based regenerative controlled electric drive system," *IEEE Trans. Industrial Electronics,* 10.1109/TIE.2010.2087290, 2010.
4. Petar J. Grbović, Philippe Delarue and Philippe Le Moigne, " A novel three-phase diode boost rectifier using hybrid half-DC-BUS-voltage rated boost converter," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2050757, 2010.
5. Petar J. Grbović, Philippe Delarue, Philippe Le Moigne and Patrick Bartholomeus, "Regenerative controlled electric drive with extended ride-through capability using an ultra-capacitor as energy storage device," *IEEE Trans. Industrial Electronics*, 10.1109/TIE.2010.2048838, 2010.
6. Petar J. Grbović, Philippe Delarue, Philippe Le Moigne and Patrick Bartholomeus, "A bi-directional three-level dc-dc converter for the ultra-capacitor applications," *IEEE Trans. Industrial Electronics,* Vol. 57, No 10, pp. 3415-3530, October 2010.
7. Petar J. Grbović, Francois Gruson, Nadir idir, and Philippe Le Moigne, "Turn-on Performance of Reverse Blocking IGBT (RB-IGBT) and Optimization Using Advanced Gate Driver," *IEEE Trans. Power Electronics*, Vol. 25, No. 4, pp. 970-980, April 2010.
8. Petar J. Grbović, "High Voltage Auxiliary Power Supply Using Series-Connected MOSFETs and Floating Self-Driving Technique," *IEEE Trans. Industrial Electronics,* Vol. 56, No. 5, pp.1446-1455, May 2009.
9. Petar J. Grbović, "Input Serial Output Parallel (ISOP) Connected High Voltage Power Supplies Based on Simple Master/Slave Control technique", *IEEE Trans. Power Electronics*, Vol. 24, No. 2, pp. 316-328, February 2009.
10. Petar J. Grbović, "Loss-Free Balancing Circuit for Series Connection of Electrolytic Capacitors Using an Auxiliary Switch Mode Power supply," *IEEE Trans. Power Electronics*, Vol. 24, No. 1, pp. 221-231, January 2009.
11. Petar J. Grbović, "An IGBT Gate Driver for Feed-Forward Control of Turn-on Losses and Reverse Recovery Current," *IEEE Trans. Power Electronics*, Vol. 23, No. 2, pp. 643-652, March 2008.

International conferences:

1. Petar J. Grbović and Michel Arpiliere, "IGBT Cross Conduction Phenomenon - Origin and Simple Protection Gate Driving Technique," in Proc. EPE'09.
2. Petar J. Grbović, "Feed Forward Control of Turn off Performances of an IGBT in Short Circuit Conditions", in Proc. EPE'07.

3. Petar J. Grbović, “Auxiliary Power Supplies in Low Power Inverters for Three Phase Tesla Induction Motors”, in Proc. PCIM’06, Nurnberg 2006.
4. Petar J. Grbović, “The Gate Drive Requirements for New Generation of High Current Low Voltage IGBTs Employed in Motor Converters”, in Proc. PEDS’05, Kuala Lumpur 2005.
5. Petar J. Grbović and Perry Field, “Analysis of a Possibility to use 1200V IGBT Devices in Snubberless Medium Power Motor Converters Supplied from the 600V Mains”, in Proc. EPE’05, Dresden 2005.
6. Petar J. Grbović, Slobodan N. Vukosavic´, ”A Novel Step Down Auxiliary Power Supply Employed in a Micro Drive for Three Phase Tesla’s Induction Motor”, in Proc. PCIM’05, Nurnberg 2005.
7. Petar J. Grbović, Slobodan N. Vukosavic´, “An Auxiliary Power Supply Based on the Phase Voltage Ripple Employed in a Micro Inverters for Feeding a Three Phase Tesla’s Induction Motor”, in Proc. EPE’05, Dresden 2005.
8. Petar J. Grbović, “Challenges in Using new Generations of High Current Low Voltage IGBTs”, in Proc. of PCIM’05, Nurnberg 2005.
9. Petar J. Grbović, Duro Basic´ “A Novel Active Gate Drive for Snubber-less IGBT operation”, EPE-PEMC’04, Riga 2004 (The paper was cancelled due to the patent application).

International patents:

1. Petar J. Grbović, “Convertisseur de puissance à source de courant utilisant des transistors a effet de champ normalement”INPI 1000066622.
2. Petar J. Grbović, “Dispositif de commande d'un transistor de puissance” The patent N_0 RUE2072 is pending in the French and European Patent Office.
3. Petar J. Grbović, “Convertisseur de puissance utilisant un redresseur à transistors normalement fermés” The patent N_0 RUE2069 is pending in the French and European Patent Office
4. Petar J. Grbović, “Onduler a base de transistors a effet de champ normalament fermes” The patent N_0 RUE2068 is pending in the French and European Patent Office
5. Dr. Heirnich Jelinek, Petar J. Grbović, “An option for power plant applications using Ultra capacitors,” The patent is pending in the Austrian and European Patent Office.
6. Petar J. Grbović, Philippe Baudesson and Philippe LeMoigne“ Energy recovery device in a variable frequency drive,” Pub. No.: WO/2010/046262.
7. Petar J. Grbović, Philippe Baudesson and Philippe LeMoigne, “Variateur de vitesse avec super-condensateur,” Demande de brevet europeen, N_0 EP 2 131 483 A1.
8. Petar J. Grbović, Philippe Baudesson and Philippe LeMoigne“Methode for recovering power in a variable speed drive”, Pub. No.: WO/2009/147186.
9. Petar J. Grbović, “Methode and system for managing the temperature in a speed controller,” United States Patent Application 20080251589 A1.
10. .Petar J. Grbović “Switche mode power supply system and speed variator comprising such a system,” United States Patent US 7, 596, 004 B2.
11. Petar J. Grbović, “Power factor correction device for variable speed drive,” United States Patent 7 420 351 B2.
12. Petar J. Grbović, “Device for powering a variable speed drive,” United States Patent, 7, 336, 052 B2.
13. Petar J. Grbović, “Power transistor control device,” United States Patent, 7, 368, 972 B**2**.

RESUME EN FRANÇIAS

Au cours de l'histoire humaine, la force motrice fut d'abord celle des animaux et des esclaves, la puissance hydraulique, puis l'éolien. Au 18ième siècle, il s'agissait de la machine à vapeur inventée par James Watt. Avec l'invention de l'électricité, l'énergie électrique s'est peu à peu imposée. Les premiers moteurs étaient à courant continu et à la fin du 18ième siècle, Nikola Tesla inventa le système triphasé, ainsi que le plus connu des moteurs : le moteur asynchrone. Du fait de leurs nombreux avantages par rapport aux machines à courant continu, les moteurs asynchrones devinrent prédominants dans la plupart des applications à vitesse constante. Toutefois, le principal inconvénient de ces moteurs restait la difficulté à contrôler leur vitesse, constituant un facteur limitant pour les applications à vitesse variable.

Les premiers développements de variateurs de vitesse électronique datent de la première moitié du 20ième siècle, entre 1910 et 1940. Ils étaient basés sur des tubes électroniques comme les thyratrons et les ignitrons. Ces « interrupteurs d'électronique de puissance » n'ont pas eu un large succès dans les applications industrielles du fait de leur complexité et de problèmes de fiabilité. Au début des années 1960, le premier thyristor a été inventé et l'ère des convertisseurs de puissance à semiconducteurs a commencé, ainsi que l'essor des variateurs de vitesse. Quatre décennies plus tard, au début du 21ième siècle, les variateurs modernes basse tension sont exclusivement dédiés aux moteurs triphasés, qu'ils soient asynchrones ou synchrones à aimants permanents. Les convertisseurs d'électronique de puissance utilisés sont des onduleurs à source de tension modulée en largeur d'impulsion (MLI) et ils utilisent des semiconducteurs de puissance de type Silicium (Si) à savoir des diodes et des transistors bipolaires à grille isolée (IGBTs). Récemment, les composants au Carbure de Silicium (SiC) ont fait leur apparition (diodes schottky (SBD) et transistors à effet de champ FET), sans grand succès pour le moment, du fait de leur coût élevé et d'un problème de maturité.

Avec le développement rapide des applications électriques, les variateurs électroniques deviennent d'importants consommateurs d'énergie. De nos jours, 70% de la production mondiale d'électricité est consommée par des variateurs de vitesse, pour le transport, l'industrie, l'électroménager etc. Ces solutions ne résolvent pas tous les problèmes: récupération de l'énergie de freinage, immunité face aux coupures du réseau d'alimentation,

qualité du courant d'entrée, contrôle et stabilité du bus continu, fonctionnement monophasé, et puissance crête appelée sur le réseau.

La plupart des applications modernes des variateurs de vitesse, comme les ascenseurs, les grues, les machines-outils, etc… sont caractérisées par un fort déséquilibre entre leur puissance moyenne et leur puissance crête. De plus, ces applications requièrent un freinage à puissance nominale. Dans les variateurs de vitesse classiques, l'énergie mécanique emmagasinée dans la charge en mouvement est dissipée via une résistance. Les pertes énergétiques dans de telles applications s'élèvent à hauteur de 30 à 50% de l'énergie consommée. A l'heure actuelle, dans un contexte de crise énergétique, l'efficacité de ces systèmes d'entraînement devient une préoccupation prioritaire qui nécessite des réponses industrielles à très court terme.

Les variateurs modernes sont sensibles aux coupures du réseau d'alimentation. Ces coupures sont susceptibles d'interrompre le fonctionnement du variateur et de bloquer une ligne entière de production. Ces interruptions sont extrêmement coûteuses et inacceptables quand le variateur est utilisé dans un processus critique comme l'extraction de pétrole ou l'industrie du verre. De telles industries ont rapporté des pertes allant de 10k$ à 1M$ par interruption. Un autre problème introduit par le variateur lui-même est la qualité du courant prélevé sur le réseau. Les redresseurs à diodes classiques équipés de filtres LC prélèvent un courant à fort contenu harmonique. L'alimentation monophasée de variateurs triphasés est une autre problématique de la qualité de l'énergie, par exemple lors de la déconnexion d'une phase du réseau d'alimentation. Dans certaines applications comme les pompes d'irrigation, le fonctionnement monophasé constitue même le mode de fonctionnement normal.

Les deux solutions les plus fréquemment évoquées pour récupérer l'énergie de freinage des variateurs de vitesse sont les convertisseurs réversibles AC-DC-AC indirects, et les convertisseurs AC-AC, appelés convertisseurs matriciels. Ces variateurs utilisent l'énergie du réseau lors des phases d'accélération, et réinjectent de l'énergie dans le réseau lors des phases de freinages (décélération). Le principal inconvénient incombant à ces solutions, vient du fait que cette fonctionnalité est fortement dépendante de la qualité et de la fiabilité du réseau d'alimentation. Chaque interruption d'alimentation perturbe le variateur de vitesse, et celui-ci s'arrête complètement de fonctionner lorsque l'interruption dépasse une période réseau. Les fonctionnements en monophasé sont limités, voir impossibles pour les convertisseurs matriciels. De plus, certains variateurs de vitesse ont une forte demande en courant durant les phases d'accélération et de décélération. Ces variations importantes de

courant aux bornes du variateur de vitesse ajoutent des perturbations et des pertes sur les réseaux d'alimentation peu fiables.

Un autre concept de variateur de vitesse à récupération d'énergie est basé sur un convertisseur classique AC-DC-AC à diode, équipé d'un dispositif de stockage d'énergie. Ce concept revient au gout du jour, grâce aux larges applications qu'offrent les nouveaux condensateurs double couches électrochimiques (EDLC), aussi appelé supercondensateurs. En comparaison aux actuelles batteries électrochimiques, les supercondensateurs ont une densité de puissance élevée, un meilleur rendement, une durée de vie plus longue, ainsi que de meilleures performances dynamiques. Tous ces avantages font des supercondensateurs les meilleurs candidats pour les applications de puissance nécessitant un stockage énergétique. Dans notre cas, les super-condensateurs viennent stocker l'énergie durant les phases de freinage du variateur de vitesse. Cette énergie est ensuite réutilisée lors des phases d'accélération suivantes. Les variateurs de vitesse utilisant un tel concept de récupération d'énergie peuvent alimenter des ascenseurs, des machines à outils ayant des séquences accélération-décélération rapides, ainsi que d'autres applications sollicitant souvent la fonction freinage du variateur de vitesse. De plus, les supercondensateurs peuvent assurer la fonctionnalité UPS (alimentation sans interruption – uninterruptable power supply) et ainsi permettre au variateur de vitesse de rester sous tension lors des microcoupures d'alimentation, ce qui est déterminant pour des applications industrielles critiques où les arrêts sont très couteux.

Dans la première partie de ce document, une introduction générale est donnée. Puis, dans la deuxième partie de ce document, sera présenté le concept de variateur de vitesse à récupération d'énergie basé sur les supercondensateurs. Les supercondensateurs sont utilisés comme élément de stockage d'énergie lors des freinages, et comme source d'énergie lorsque cela est possible. De plus, les supercondensateurs sont utilisés comme alimentation de secours lors des microcoupures de courant. A la différence des batteries électrochimiques, l'état de charge (SOC) des supercondensateurs dépend fortement de la tension à leurs bornes. Ainsi, il n'est pas possible de connecter directement les supercondensateurs au variateur de vitesse. Il est nécessaire d'utiliser une interface électronique DC-DC. L'état de l'art sur ces topologies est présenté, et un nouveau convertisseur multiniveaux DC-DC est proposé. Celle-ci est analysée et les règles de conception sont exposées. Le modèle complet du système de conversion est ensuite développé et un contrôle/commande est proposé. L'objectif de la partie contrôle est triple. Le premier objectif est de réguler le courant du supercondensateur ainsi

que le point milieu du bus continu du hacheur multiniveaux. Le second objectif est de faire tendre la tension du bus continu vers la tension de référence dépendant du mode d'exploitation choisi. Le dernier objectif est de contrôler l'état de charge du supercondensateur.

La troisième partie de ce document présente un variateur de vitesse triphasé novateur à pont redresseur à diode en entrée mais doté d'un convertisseur élévateur alimenté par la demi-tension du bus continu. Ce convertisseur élévateur est composé de deux convertisseurs DC-DC ainsi que de deux condensateurs en série sur le bus continu. Le premier convertisseur régule le courant continu de sortie du redresseur d'entrée et élève la tension du bus continu à une valeur supérieure à la tension composée réseau crête. Ce convertisseur est connecté entre la borne + du bus DC et le point milieu des capacités du bus DC.

Le deuxième convertisseur DC-DC est un convertisseur auxiliaire qui assiste le premier. Ce convertisseur est un convertisseur résonnant série fonctionnant en mode discontinue (type 1). Le modèle complet, non-linéaire et de petit signal, est présenté, ainsi que le mode de contrôle, le tout étant validé expérimentalement. Les avantages du hacheur élévateur original proposé comparativement aux solutions connues sont le rendement de conversion plus élevé ainsi que la taille réduite des composants aussi bien actifs (diodes et interrupteurs de puissance) que passifs (inductances et condensateurs). Cependant, le taux de distorsion harmonique du courant total (THD) ainsi que le taux de distorsion harmonique pondérée partiel (PWHD) restent élevé. Le THD tourne autour des 30% alors que le PWHD tourne autour de 55%. Comme les normes acceptent un THD de 30% pour les variateurs de vitesse utilisés à des fins industrielles tant que le PWHD est légèrement en dessous de la valeur limite, le nouveau convertisseur élévateur est une solution viable pour remplacer les convertisseurs passif à diode tout comme les redresseur à prélèvement sinus utilisant des hacheurs boost ou double boost. Cette topologie peut être utilisée aussi bien sur les variateurs monophasés que les variateurs triphasés.

Dans la quatrième partie de ce document, une solution regroupant les deux solutions précédentes est présentée. Cette solution permet de résoudre les problèmes techniques actuels qui existent dans la variation de vitesse :

1) Récupérer l'énergie de freinage

2) Empêcher les disfonctionnements du variateur de vitesse lors des microcoupures

3) Augmenter la qualité du courant d'entrée du variateur de vitesse

4) Contrôler la tension continu (bus DC) du variateur de vitesse

5) Permettre un fonctionnement dégradé lors de la perte d'une phase réseau

6) Lisser les pics de puissance provoqués par la charge et prélévés habituellement sur le réseau

La solution proposée à été analysée et les règles de conception ont été exposées. Le concept a été validé par des simulations sur Matlab/Simulink et un prototype a été réalisé et testé en laboratoire. Si on compare la solution innovante proposée avec les solutions non industrielles envisagées habituellement pour la variation de vitesse (convertisseur matriciel – convertisseur classique avec stockage, convertisseur MLI réversible…), la solution originale proposée a les avantages suivant :

- Capacité du variateur de vitesse à rester fonctionnel lors des microcoupures d'alimentation est améliorée. La durée de microcoupure maximale tolérée est alors un paramètre de dimensionnement du stockage.
- La fonctionnalité système du variateur de vitesse, incluant sa capacité de freinage, n'est pas reliée à la fiabilité de l'alimentation
- Le fonctionnement en marche dégradée lors de la perte d'une phase réseau est simple à gérer et amène à de très bonnes performances.
- Les pics de puissance sont limités, et conduisent à une réduction des contraintes électriques au niveau réseau.
- La consommation électrique du système est fortement réduite grâce au stockage et au développement d'une solution électronique à haut rendement.

Dispositif correcteur de facteur de puissance à base de super-condensateur pour variateur de vitesse

Les variateurs de vitesse modernes sont exclusivement basés sur l'utilisation de moteurs triphasés alimentés par des onduleurs à modulation de largeur d'impulsion (MLI). La plupart des applications modernes de la variation de vitesse, comme les ascenseurs, les grues et les machines-outils sont caractérisées principalement par un rapport élevé entre la puissance crête et la puissance moyenne et une forte demande de freinage à la puissance nominale. Dans les variateurs de vitesse ordinaires, l'énergie de freinage, qui est de l'ordre de 30 à 50% de l'énergie consommée, est dissipé dans une résistance. Outre les problèmes « énergétiques », les interruptions et dégradations de la tension d'alimentation ainsi que la qualité du courant d'entrée et la fluctuation de la charge, sont d'autres questions à aborder et à résoudre.

Le super-condensateur dédié aux applications de conversion de puissance est ainsi proposé. Un variateur de vitesse équipé avec des super-condensateurs est présenté dans la thèse. Les super-condensateurs, interconnectés par un convertisseur DC-DC sont utilisés pour stocker et ré-injecter l'énergie de freinage. De plus, le convertisseur DC-DC contrôle le courant du redresseur et la tension du bus DC. Le THD du courant d'entrée est ramené à 30%. La tension du bus DC est élevée et en permanence contrôlée et lissée indépendamment de la charge et de la variation de la tension réseau. Pour terminer, les pics de puissance peuvent être lissés. La solution présentée est analysée théoriquement et vérifiée par un ensemble de simulations et expérimentations. Les résultats sont présentés et commentés.

Ultra-capacitor based regenerative energy storage and power factor correction device for controlled electric drives

Modern controlled electric drives are exclusively based on three-phase motors that are fed from three-phase pulse width modulated (PWM) inverters. Most of modern controlled electric drive applications, such as lifts, cranes and tooling machines are characterized by high ratio of the peak to average power, and high demand for braking at the rated power. In ordinary drives, the braking energy, which represents 30-50% of the consumed energy, is dissipated on a braking resistor. Apart from the "energetic" issue, the mains interruption and degradation, the input current quality and the load fluctuation are additional issues to be addressed and solved.

The ultra-capacitor dedicated for power conversion applications has been discussed. In comparison to electrochemical batteries, the ultra-capacitors have higher power density and efficiency, longer life time and greater cycling capability. This makes the ultra-capacitor an excellent candidate for power conversion applications.

A new electric drive converter equipped with the ultra-capacitor is presented in the dissertation. The ultra-capacitor with an inter-connection dc-dc converter is used to store and recover the drive braking energy. Moreover, the dc-dc converter controls the rectifier current and the dc bus voltage. The drive input current THD is reduced to 30%. The dc bus voltage is boosted and controlled constant and ripple free regardless on the load and the mains voltage variation. Moreover, the drive input peak power can be smoothed. The presented solution is theoretically analysed and verified by set of simulations and experiments. The results are presented and discussed.