Design and Optimization of InterCell Transformers for Parallel MultiCell Converters

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Abstract

In recent years, the interest for parallel multicell converters has grown, which is partially due to the possibility of coupling the inductors used to connect the different commutation cells together. Coupling the inductors to form an InterCell Transformer (ICT) does not usually modify the output current, but it reduces the current ripple in the windings and the flux swing in some regions of the core. It can be shown that this brings a reduction of copper and core losses in the magnetic component. The reduction of the phase current ripple also reduces the difference between turn on and turn off current in the switches, which brings a reduction of switching losses for devices generating more losses at turn off than at turn on.

The design of an ICT is not that different from any other magnetic component but it is very specific and inherent features must be taken into account. Taking full benefit of the potential advantages of ICTs requires the development of special tools and methods which are the focus of the study. We show how to design ICTs considering several topologies and different methods, from the most precise and time-consuming to the less accurate but more quickly calculated. The explanation of the ICT design is divided in four main parts: Copper Losses, Core Losses, Flux Density Saturation and Thermal Aspects.

Further attention is given to high frequency copper losses since complex phenomena such as skin and proximity effects highly influence the ICT design. Based on Finite Element Method simulations, smart practices are suggested to reduce high and low frequency copper losses, not only in ICTs but also in inductors and transformers. Simple tables are developed to help transformer designers to identify the best configuration of conductors inside a given core window, depending on the current waveform and frequency, number of turns and geometrical parameters.

Optimization routines to reduce the ICT total mass, volume, losses or cost are developed and multidimensional interpolation of pre-simulated values of AC resistance and leakage inductance is used to speed up the optimization routine. Comparison of ICT designs with regard to core and conductor material, number of cells and switching frequency is performed. Comparison with regular inductors is also made in order to verify the benefits of this kind of magnetic component.

Multilevel converter control aspects applied to three-phase systems is also investigated in terms of the ICT flux. Zero sequence signals, specific for a PWM strategy and converter/load topology, are created in order to minimize the flux in ICTs and consequently reduce even further the mass and size of these components. Comparison between several PWM methods are performed and experimentally verified.

Keywords:

- Interleaved Converters
- Parallel MultiCell Converters
- InterCell Transformers
- Copper Losses
- ICT Design
- ICT Optimization
- PWM Methods

Résumé

Les convertisseurs multicellulaires parallèles permettent de traiter des puissances importantes et de profiter d'une certaine standardisation des équipements. Ces dernières années, ces structures ont connu un regain d'intérêt lié notamment à la possibilité de couplage magnétique des inductances. Ce couplage aboutit à un composant magnétique aux propriétés très différentes appelé Transformateur Inter-Cellules (ICT) ; il ne modifie pas le courant de sortie, par contre il réduit l'ondulation de courant dans les bobines et l'ondulation de flux dans certaines parties du noyau. On peut montrer que ce couplage entraîne une réduction des pertes Joules dans les conducteurs et des pertes magnétiques dans le noyau. La réduction de l'ondulation de courant diminue également le courant efficace dans les semiconducteurs ce qui réduit les pertes par conduction, et la différence entre le courant à l'amorçage et au blocage des interrupteurs, ce qui permet la diminution des pertes dans les semiconducteurs lorsque les pertes au blocage sont supérieures aux pertes à l'amorçage.

Le dimensionnement d'un ICT n'est pas fondamentalement différent de celui fait pour d'autres composants magnétiques en ce sens qu'il est basé sur le respect de certaines valeurs limites (induction, température) ce qui suppose une évaluation des différentes pertes et l'élaboration d'un modèle thermique. Par contre, la manière d'évaluer ces différentes grandeurs est tout à fait spécifique et n'a que quelques points communs avec les méthodes de calcul des inductances et des transformateurs Dans ce travail de thèse, on montre comment dimensionner ces ICTs en considérants plusieurs topologies et méthodes différentes, correspondant à différents niveaux de sophistication et de complexité. L'explication de ce dimensionnement est divisée en quatre parties : Pertes Cuivre, Pertes Fer, Densité de Flux de Saturation et Aspects Thermiques.

L'évaluation des pertes cuivre liées aux composantes alternatives des ICTs constituent un point particulièrement délicat dans la mesure où elles résultent de la combinaison de deux facteurs eux-mêmes difficiles à évaluer ; l'inductance de fuite qui détermine l'amplitude des courants alternatifs mais dépend des flux principalement non canalisés et circulant dans l'air (volume d'étude important, effets 3D…), et la résistance équivalente des bobinages qui en haute fréquence est sujette à des phénomènes complexes comme les effets de peau et de proximité.

En se basant sur l'utilisation d'un logiciel simple mais néanmoins robuste et fiable pour calculer précisément les résistances en haute fréquence et les inductances de fuite des ICTs, plusieurs astuces permettant de réduire les pertes cuivre non seulement des ICTs mais aussi des transformateurs et des inductances sont suggérées. Des tableaux simples sont développés pour aider le concepteur de transformateurs à identifier la meilleur configuration de conducteurs dans une fenêtre de bobinage en prenant en compte la forme d'onde du courant, le nombre de tours des enroulements, la fréquence des courants et les paramètres géométriques.

Des formules analytiques et des outils de calcul adéquats ont ensuite été utilisés pour développer des routines d'optimisation ayant pour but la réduction de la masse, du volume, des pertes ou du coût des ICTs. Des interpolations multidimensionnelles des valeurs pré-simulées des résistances et inductances de fuite en haute fréquence sont utilisées afin de réduire le temps d'exécution de la routine d'optimisation. Plusieurs dimensionnements des ICTs ont été comparées vis-à-vis des matériaux du noyau et des conducteurs, du nombre de

cellules de commutation et de la fréquence de découpage. Des comparaisons avec des selfs ont également été faites afin de montrer les avantages de ces ICTs.

Des aspects de la commande des convertisseurs multiniveaux triphasés ont également été étudiés vis-à-vis du flux circulant dans les ICTs. Des homopolaires, spécifiques pour chaque stratégie MLI et chaque topologie convertisseur/charge, sont créées afin de minimiser le flux dans les ICTs et par conséquent de réduire davantage la masse et la taille de ces composants. Des comparaisons entre différentes méthodes de MLI sont effectuées et vérifiées expérimentalement.

Mots Clés :

- Convertisseurs Entrelacés
- Convertisseurs Multicellulaires Parallèles
- Transformateurs Inter-Cellules
- Pertes Cuivre
- Dimensionnement des ICTs
- Optimisation des ICTs
- Modulation de Largeur d'Impulsion (MLI)

Résumé en Français

Dimensionnement et Optimisation de Transformateurs Inter-Cellules pour les Convertisseurs Multicellulaires Parallèles

Introduction Générale

L'augmentation de la densité de puissance des convertisseurs est un des principaux objectifs de l'Electronique de Puissance moderne, et cela peut être atteint par la miniaturisation de convertisseurs de puissance. Les convertisseurs multiniveaux sont une option intéressante pour l'augmentation de la puissance totale et spécifique. Les convertisseurs multiniveaux série augmentent le nombre de niveaux de tension délivrée à la source de courant.et les convertisseurs parallèle augmentent le nombre de niveaux de courant et de tension de part et d'autre de la cellule de commutation. Ils augmentent également la fréquence apparente de ceux grandeurs. Ces deux caractéristiques permettent la réduction des filtres passifs associés à ces convertisseurs.

En utilisant un composant passif spécial, les convertisseurs parallèles peuvent avoir des grandeurs internes réduits, ce qui n'est pas le cas de son homologue série. Ces composants passifs sont des inductances couplées magnétiquement nommées Transformateurs Inter-Cellules (ICT) par analogie avec les transformateurs interphases des redresseurs.

Cette thèse se concentre sur ces composants et a comme but de répondre à certaines question, comme :

- Quels sont les phénomènes principaux liés au dimensionnement des ICTs?
- Comment dimensionner et optimiser un ICT d'une façon assez précise en prenant en compte tous les phénomènes associés ?
- Quelle est l'influence, dans le dimensionnement d'un ICT, des paramètres comme la structure, le nombre de cellules de commutation en parallèle ou les matériaux utilisés dans les bobines et noyaux ?
- Comment optimiser l'ICT ?
- Quelle est l'influence d'un ICT dans un système triphasé ?

Les Transformateurs Inter-Cellules constituent un sujet assez nouveau dans la littérature scientifique alors que récemment leurs applications dans le marché ont nettement augmenté. L'originalité du travail présenté ici est principalement liée à l'approche utilisée pour le dimensionnement et l'optimisation d'un ICT. Des méthodes précises pour le calcul des pertes fer et cuivre associées à des modèles thermiques permettent de dimensionner le meilleur ICT vis-à-vis d'un objectif qui peut être le volume, le poids, le prix ou, en contraignant le problème, les pertes totales.

Le travail présenté dans cette these inclue, en plus du travail sur les ICTs, plusieurs résultats originaux qui peuvent être utiles pour l'étude et le dimensionnement des inductances et des transformateurs. Un de ces résultats est un tableau permettant definir la configuration

de bobine qui minimise les pertes cuivre dans un transformateur. D'autres résultats originaux et intéressants sont des signaux homopolaires qui peuvent être ajoutés aux références d'un système triphasé pour minimiser les flux des ICTs utilisés pour coupler des systèmes triphasés.

Le manuscrit est composé de cinq chapitres qui vont être succinctement résumés :

- Chapitre I : Transformateurs inter-cellules pour les convertisseurs entrelacés.
- Chapitre II : Analyses de pertes cuivre.
- Chapitre III : Dimensionnement de transformateurs inter-cellules.
- Chapitre IV : Optimisation de transformateurs inter-cellules.
- Chapitre V : ICTs dans les systèmes triphasés.

Chapitre I – Transformateurs Inter-Cellules pour les Convertisseurs Entrelacés

Les convertisseurs entrelacés sont une bonne solution pour l'électronique de puissance actuelle dont l'un des principaux buts consiste à augmenter la densité de puissance des convertisseurs. Initialement, les études portant sur les topologies, les techniques de commande, les aspects des défauts, le fonctionnement, etc. ont été développés en se basant sur les convertisseurs multiniveaux série. Les règles de dualité montrent que la plupart des analyses menées sur ces types de convertisseurs peuvent être transposées aux convertisseurs multiniveaux parallèle.

La mise en parallèle des cellules de commutation permet l'augmentation de la puissance à la sortie du convertisseur en utilisant des semiconducteurs standards. L'entrelacement des signaux de commande de ces cellules de commutation permet la réduction des ondulations des courants de sortie ainsi que l'accroissement de performance en régime transitoire du convertisseur.

Afin d'expliquer les avantages des convertisseurs multiniveaux parallèles, un hacheur abaisseur (convertisseur Buck) parallèle multicellulaire sera pris comme référence. Il est représenté en Figure 1.

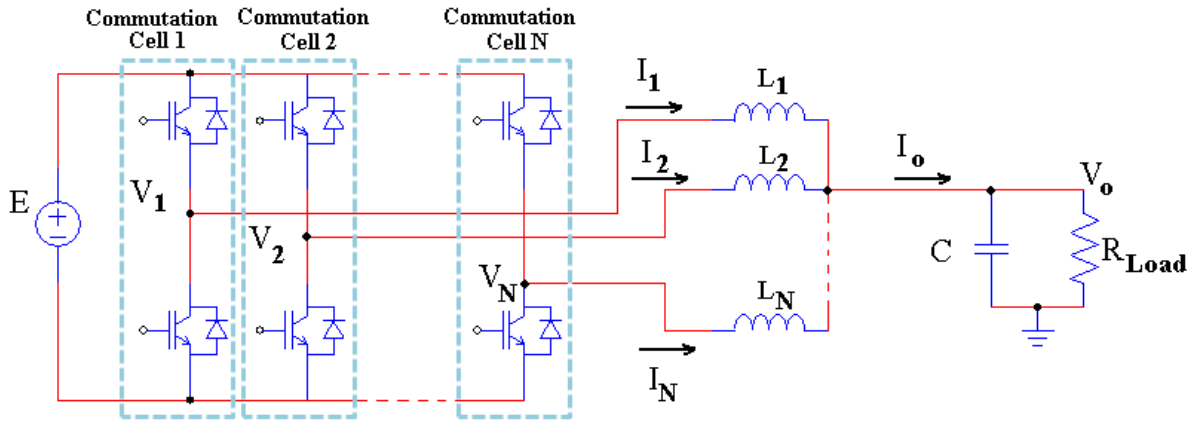


Figure 1 : Hacheur abaisseur parallèle multicellules.

Dans cette figure, le convertisseur est constitué de N cellules de commutation interconnectées par les inductances séparées (L_1=L_2=…=L_N=L). Etant donné qu'il s'agit d'un système symétrique, chaque inductance est traversée par un courant égal à I_o/N. Chaque

cellule de commutation a le même rapport cyclique (α), cependant, leurs porteuses correspondantes sont déphasées les unes des autres de $2\pi/N$. Ainsi, la tension des points milieu admettent une forme rectangulaire (entre 0V et +E) et ce avec le même déphasage et la même fréquence.

En considérant constante la tension aux bornes du condensateur C, l'ondulation du courant de chaque phase est calculée comme suit :

$$\Delta I_x = \frac{\alpha(1-\alpha)E}{LF_s} \tag{1}$$

Avec E, la tension du bus continu et F_s, la fréquence de commutation du convertisseur. L'ondulation du courant de sortie est déterminée à l'aide du rapport cyclique relatif α'[22]:

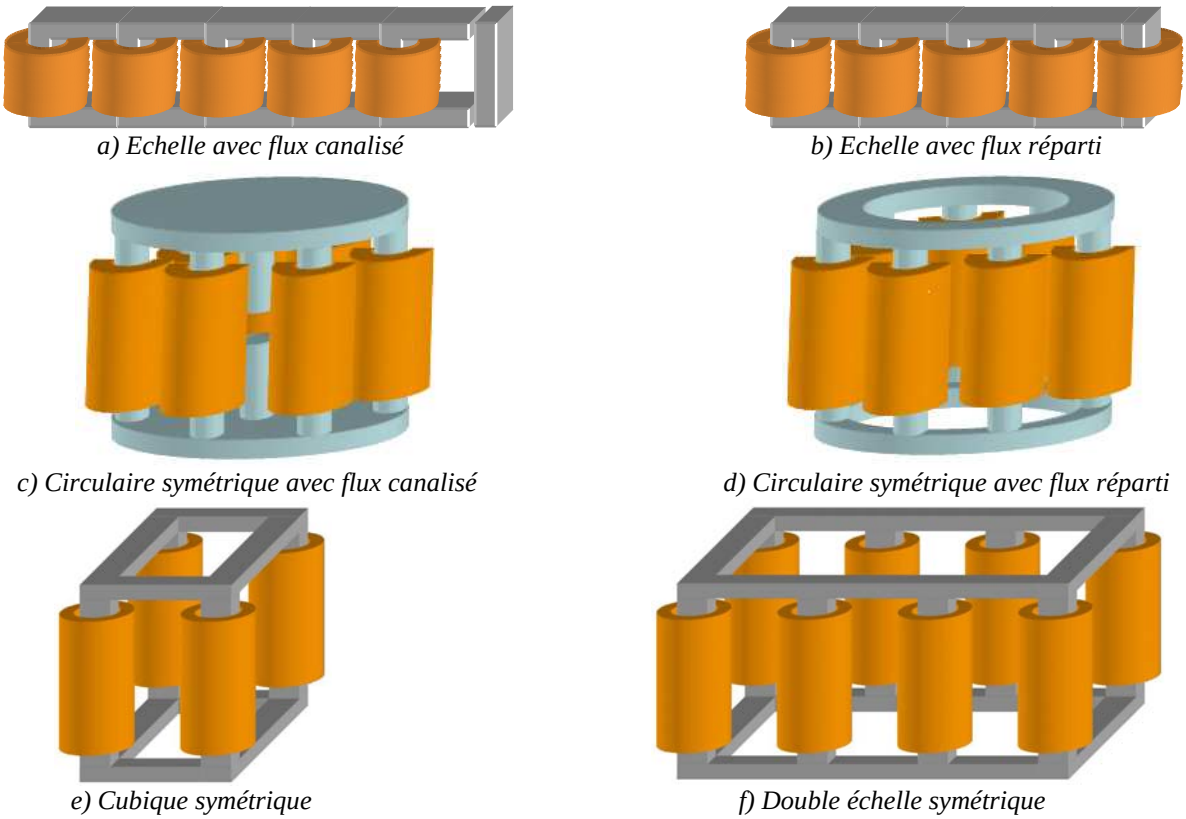
$$\forall i \in \{0,1,...,N-1\}, \forall \alpha \in \left[\frac{i}{N}, \frac{i+1}{N}\right], \alpha' = N\alpha - i \tag{2}$$

L'ondulation du courant de sortie est ainsi :

$$\Delta I_o = \frac{\alpha'(1-\alpha')}{N^2} \cdot \frac{E}{LF_s} \tag{3}$$

La mise en parallèle massive des cellules de commutation utilisant de simples inductances pour les connecter n'est pas recommandée à cause de l'augmentation de l'ondulation du courant dans chaque cellule. Pour résoudre ce problème, des transformateurs inter-cellules peuvent être utilisés afin de réduire l'amplitude et augmenter la fréquence des courants de toutes les cellules, vue qu'elles sont couplés magnétiquement.

Dans ce chapitre, plusieurs topologies d'ICT à 2 ou N-cellules sont représentées (comme ceux de la Figure 2) et quelques spécificités de ces composants sont décrites et étudiées.



a) Echelle avec flux canalisé

b) Echelle avec flux réparti

c) Circulaire symétrique avec flux canalisé

d) Circulaire symétrique avec flux réparti

e) Cubique symétrique

f) Double échelle symétrique

Figure 2 : Transformateurs Inter-cellules.

L'utilisation des ICTs dans l'industrie et les études de recherche réalisées par la communauté scientifique sont en augmentation. Initialement, leur principale application consistait à réaliser une connexion parallèle entre les cellules de commutation des Modules des Régulateurs de Tension (VRM) qui sont composés principalement de hacheurs abaisseurs pour les applications fort courant basse tension telles que les alimentations pour les micro-ordinateurs. Plus tard, l'utilisation de ces composants magnétiques a été étendue aux différentes plages de puissances et topologies.

Le dimensionnement et l'optimisation des ICTs vont être détaillés dans ce manuscrit. Le prochain chapitre va être consacré à un aspect très important du dimensionnement : les pertes cuivres à hautes fréquences.

Chapitre II – Analyses des Pertes Cuivre

Introduction

Les pertes cuivre représentent le principal aspect de dimensionnement des ICTs puisque ces pertes sont très souvent beaucoup plus importantes que les pertes fer pour différentes topologies utilisées dans différentes applications.

Le choix du matériau conducteur (cuivre, aluminium ou même un autre matériau) est très important. Si les effets haute fréquence sont pris en considération, le choix du nombre de tours et celui du nombre de couches de chaque bobine peut être même plus important que celui du matériau. La position et la forme de la section du conducteur joue un rôle très important dans le dimensionnement comme il va être montré dans ce qui suit.

Les effets de peau et de proximité sont les deux plus importants effets haute fréquence liés aux pertes cuivre dans les inductances et les transformateurs. Le calcul analytique de ces derniers est maîtrisé pour les cas simples. Le calcul analytique de l'effet de peau est possible pour un conducteur placé loin d'autres conducteurs et des noyaux magnétiques. Quant à la formule calculant l'effet de proximité, elle ne peut être utilisée que quand les conducteurs sont placés dans un champ magnétique 1D (par exemple dans la fenêtre de bobinage d'un transformateur avec la géométrie adéquate). Pour tous les autres cas, des simulations par éléments finis (FEM) en 2 ou 3 dimensions doivent être réalisées afin de prédire avec précision la résistance AC, qui peut croître significativement avec la fréquence de commutation et ses multiples, et évaluer précisément les pertes cuivre résultantes.

Les pertes liées à l'entrefer, aux têtes des bobines et aux conducteurs dans les inductances ont été évaluées en utilisant les simulations par éléments finis. Nous avons montré la différence entre le comportement des pertes cuivre dans les inductances et dans les transformateurs. En effet, l'entrefer n'augmente pas nécessairement les pertes cuivre dans les transformateurs, contrairement au cas de l'inductance.

Il a été remarqué que la partie d'une bobine se trouvant à l'extérieur de la fenêtre du noyau peut générer des pertes beaucoup plus importantes que la partie se trouvant à l'intérieur. Cette constatation montre qu'il peut être dangereux d'utiliser directement les équations de Dowell pour calculer les pertes cuivre afin de dimensionner les ICTs.

Nous avons examiné quelques techniques essayant de réduire les pertes cuivre dans les ICTs et nous avons conclu que :

- Rajouter un matériau magnétique à certains endroits de l'ICT réduit les pertes cuivre dans certains cas et les augmente dans d'autres. Par contre, dans tous les cas, ceci augmente les pertes fer et aussi le poids final de l'ICT.

- Plus les conducteurs sont dispersés sur la verticale de la fenêtre du noyau plus les pertes cuivre sont réduites, mais il en va de même pour l'inductance de fuite. Cette solution n'est donc pas une bonne solution pour les ICTs.
- L'entrelacement des bobinages est une solution efficace pour réduire l'effet de proximité. Cependant, cette alternative réduit aussi l'inductance de fuite, ce qui n'est pas désirable pour le dimensionnement des ICTs.
- La mise en parallèle des conducteurs dans des fils plus fins ne réduit pas les pertes cuivre à haute fréquence. Pour réduire les pertes liées aux courants AC, il faudrait plutôt utiliser du fils de Litz. Cependant, cette solution est coûteuse, et conduit à un faible facteur de remplissage de la fenêtre. Comme les ICTs sont principalement parcourus soit par des courants continus (hacheurs), soit par des courants à basse fréquence (onduleurs), ceci n'est généralement pas une bonne solution.
- En concernant le dimensionnement d'un ICT, c'est souvent un choix adéquat du nombre de tours et de la forme du conducteur qui permet de maintenir les pertes cuivre haute fréquence à un niveau acceptable et d'obtenir le meilleur compromis global (somme des pertes cuivre AC et DC, ou même performance globale de l'ICT).

Fréquence Limite

Position d'une bobine dans la fenêtre

Conformément à la formule de Dowell qui décrit la variation de la résistance d'un bobinage dans un transformateur, si l'épaisseur de la couche (et des conducteurs) et la fréquence (et par conséquent l'épaisseur de peau) sont fixées, le rapport R_{AC}/R_{DC} des conducteurs augmente avec le nombre de couches de conducteurs, comme le montre la Figure 3. D'autre part, si le noyau et le nombre de spires sont relativement imposés, le concepteur doit rechercher le nombre de couches et le nombre de spires par couche qui minimisent les pertes cuivre.

Prenons l'exemple d'un transformateur où une bobine doit rentrer dans l'espace qui lui est réservé dans la fenêtre de bobinage. Cette fenêtre admet une largeur L et une hauteur Z.

Si nous devons mettre dans cet espace, par exemple, 12 spires, nous pouvons déduire 6 configurations possibles de disposition des conducteurs dans la fenêtre, comme montré dans la Figure 4 :

– Configuration 1 - 1 couche de 12 spires

– Configuration 2 - 2 couches de 6 spires

– Configuration 3 - 3 couches de 4 spires

– Configuration 4 - 4 couches de 3 spires

– Configuration 5 - 6 couches de 2 spires

– Configuration 6 - 12 couches de 1 spire

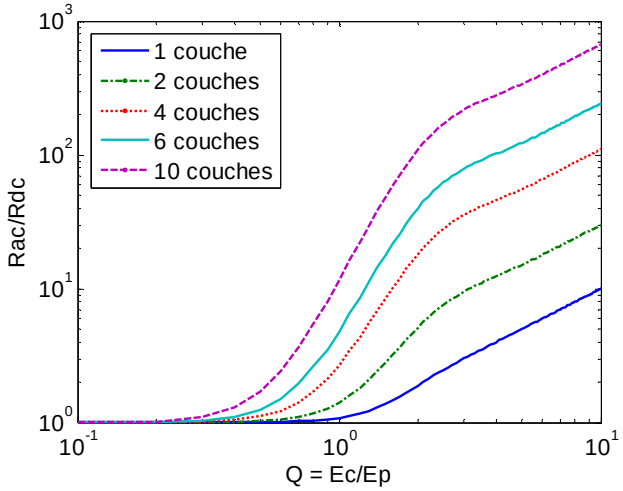
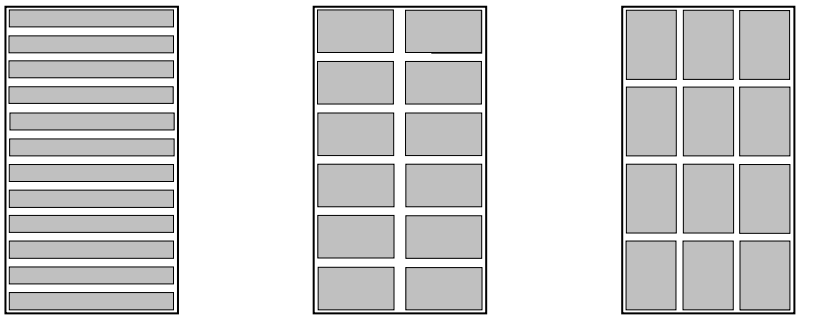
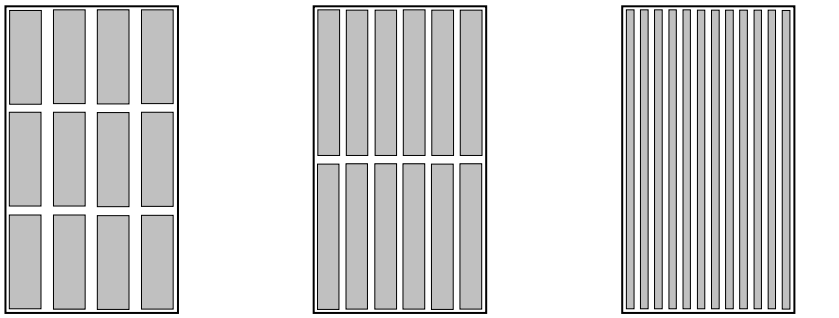


Figure 3 : Variation de la résistance AC avec la fréquence.

Dans toutes ces configurations, les sections des conducteurs sont égales (résistances DC égales). Cependant, leurs dimensions (W_w et H) ne le sont pas (résistances AC différentes). Pour cette raison, la détermination de la configuration permettant le moins de pertes n'est ni immédiate, ni unique ; elle dépend de la fréquence.



a) 1 couche de 12 spires *b) 2 couches de 6 spires* *c) 3 couches de 4 spires*



d) 4 couches de 3 spires *e) 6 couches de 2 spires* *f) 12 couches de 1 spire*

Figure 4 : Configurations pour mettre 12 conducteurs dans la fenêtre de bobinage.

La formule de Dowell, qui calcule le rapport (Fr) entre la résistance AC (R_{AC}) et la résistance DC (R_{DC}) est présentée ci-dessous :

$$Fr = \frac{R_{AC}}{R_{DC}} = Q\frac{\sinh 2Q + \sin 2Q}{\cosh 2Q - \cos 2Q} + 2Q\frac{m^2 - 1}{3}\frac{\sinh Q - \sin Q}{\cosh Q + \cos Q} \quad (4)$$

où 'm' est le nombre de couches de la bobine et Q est le rapport entre l'épaisseur de la couche (Wc) et l'épaisseur de peau (E_p).

Afin de comparer les pertes associées à chaque configuration, l'équation (4) a été utilisée pour calculer '*Fr*'. Noter que toutes les configurations ont le même R_{DC} et, en conséquence, plus *Fr* est petit plus les pertes sont faibles.

Dans la Figure 5, *Fr* a été calculé pour toutes les configurations, et pour une plage de fréquence allant de 10Hz à 1MHz. Les dimensions de la fenêtre de bobinage sont W_w = 7,24mm et H= 13,1mm.

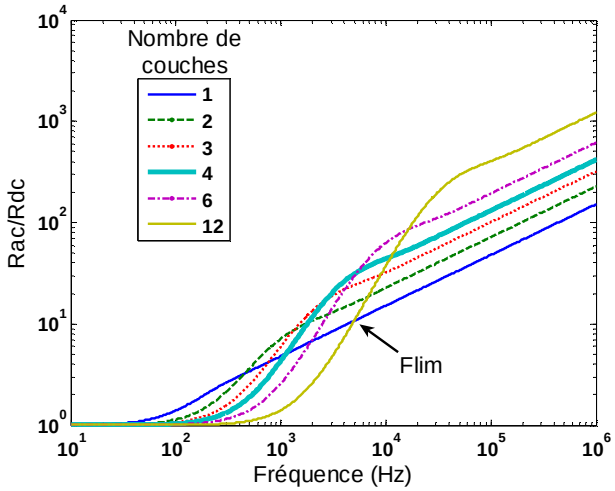


Figure 5 : Variation de la résistance AC avec la fréquence pour chaque configuration de la Figure 4.

La même procédure montrée ci-dessus pour une bobine de 12 spires a été réalisée pour des bobines de 'N_t' spires, avec 'N_t' variant de 2 à 30. Pour chacune des bobines, toutes les configurations possibles ont été calculées et le comportement décrit dans la section précédente a été observé là aussi:

– Pour les basses fréquences, la configuration avec 'N_t' couches est celle qui a le moins de pertes,

– Pour les hautes fréquences, la configuration avec 1 seule couche est celle qui a le moins de pertes,

– Par rapport aux pertes cuivre, les autres configurations ne sont jamais plus intéressantes que les 2 extrêmes (soit 'N_t' couches d'une spire, soit une couche de 'N_t' spires).

Variation de la fréquence limite

La fréquence limite pour chaque bobine de 'N_t' spires change par rapport à la largeur de la fenêtre de bobinage. Afin de vérifier comment cela change, plusieurs courbes comme celles de la Figure 5 ont été générées pour différentes largeurs de fenêtre. Un algorithme a été développé permettant d'identifier automatiquement la fréquence limite pour chaque largeur. Le comportement de cette fréquence est illustré dans la Figure 6 et ce pour des bobines de nombre de spires 'N_t' différents.

La Figure 6 montre que plus la fenêtre est large, plus la fréquence limite est basse. Si nous faisons attention aux courbes, nous pouvons noter que la fréquence limite est une fonction quadratique de la largeur de la fenêtre. Ceci veut dire que si nous multiplions la fréquence limite par le carré de la largeur correspondante, nous trouverons toujours la même constante, pour n'importe quelle largeur. Les valeurs des constantes trouvées pour des bobines de 2 à 30 spires sont montrées dans le Tableau 1.

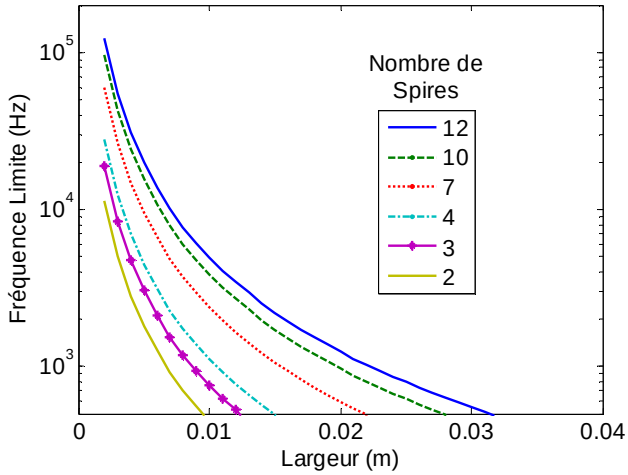


Figure 6 : Variation de la fréquence limite.

N_t	$F_{lim}*W_W^2$	N_t	$F_{lim}*W_W^2$	N_t	$F_{lim}*W_W^2$
		11	0.4395	21	1.0563
2	0.0451	12	0.4945	22	1.1246
3	0.0759	13	0.5513	23	1.1940
4	0.1115	14	0.6095	24	1.2653
5	0.1507	15	0.6695	25	1.3373
6	0.1929	16	0.7308	26	1.4093
7	0.2378	17	0.7932	27	1.4839
8	0.2851	18	0.857	28	1.5582
9	0.3346	19	0.9226	29	1.6346
10	0.3860	20	0.9886	30	1.7101

Tableau 1 : Constantes observées pour différent nombre de spires.

Ce tableau est un outil simple à utiliser pour choisir la configuration qui entraîne le moins de pertes. Le concepteur doit simplement multiplier la fréquence du courant qui passe dans le transformateur par le carré de la largeur de la fenêtre. Si le résultat est plus grand que la constante dans le Tableau 1 correspondant au nombre de spires de la bobine, alors la configuration avec 1 couche de 'N_t' spires entraîne moins de pertes. Dans le cas contraire, c'est la configuration avec 'N_t' couches d'une spire qui est préférable.

Comme la formule de Dowell est une approximation unidimensionnelle d'un phénomène tridimensionnel, des simulations intensives par éléments finis 2D ont été effectuées afin de vérifier la validité des constantes trouvées en utilisant une formulation analytique 1D. L'isolant entre conducteurs et noyaux et la circulation de courants non sinusoïdaux n'ont pas été pris en compte dans le cadre du présent travail.

Chapitre III – Dimensionnement des Transformateurs Inter-Cellules

Le dimensionnement des ICTs touche des phénomènes similaires à ceux rencontrés pour le dimensionnement d'une inductance ou d'un transformateur. L'objectif de ce dimensionnement dépend de l'application dans laquelle l'ICT est utilisé. Le but étant, en général, de minimiser le volume, le poids, le prix ou les pertes, ou la combinaison de ces grandeurs.

Des modèles plus ou moins précis peuvent être utilisés pour représenter tous les phénomènes existants. Ceci dépend du degré d'exactitude et du temps disponible pour finir le dimensionnement. Dans ce travail un dimensionnement plus général est expliqué tout en prenant en considération les quatre principaux aspects suivants : les pertes cuivre, les pertes fer, l'induction de saturation et des calculs thermiques. Le dimensionnement d'un ICT bi-cellules utilisé dans les convertisseurs avec deux cellules de commutation est d'abord présenté. Ce dimensionnement et celui d'un ICT N-cellules (séparées ou monolithiques) utilisé dans un convertisseur avec N cellules de commutation sont ensuite comparés.

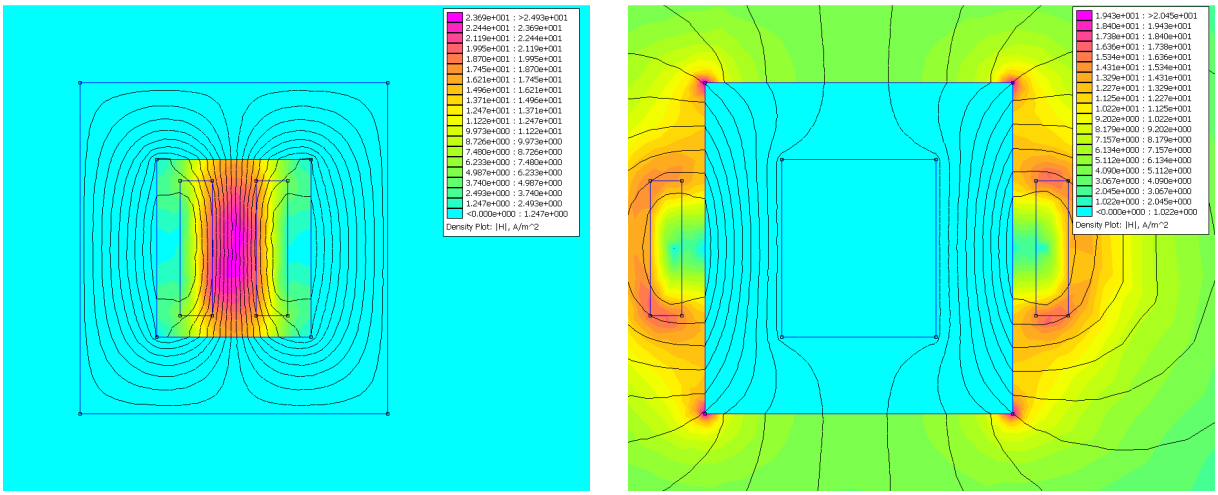
En ce qui concerne les pertes cuivre, nous avons présenté une méthode basée sur les simulations par éléments finis (FEM) en deux dimensions (2D). Cette simulation estime, avec précision, les résistances alternatives pour toutes les fréquences reliées au courant de chaque phase. Cette méthode de simulation est beaucoup plus rapide que celle basée sur les simulations FEM en trois dimensions (3D). Elle prend en considération les différences entre les résistances alternatives à l'extérieur et à l'intérieur de la fenêtre de bobinage.

Dans un ICT, les courants haute fréquence de mode commun ont des formes d'onde triangulaires à N fois la fréquence de commutation. Quant aux courants de mode différentiel, ils peuvent avoir des formes différentes, mais surtout ils ont une fréquence fondamentale égale à la fréquence de commutation. Pour diminuer les pertes cuivre en haute fréquence, les conducteurs doivent avoir un excellent facteur de forme, par contre cela peut entrainer l'augmentation des pertes cuivre en basse fréquence.

Généralement, les pertes fer et les pertes cuivre dépendent de l'inductance de fuite d'un ICT ; c'est pourquoi la valeur de cette inductance doit être estimée avec précision. Ainsi, nous avons développé une méthode de calcul de l'inductance de fuite basée sur les simulations FEM 2D. Cette méthode repose sur le calcul de quatre inductances linéiques : deux sont liées à la partie du bobinage à l'intérieur de la fenêtre ($L_{leaklfint}$ et $L_{leakhfint}$) et les deux autres à l'extérieur ($L_{leaklfext}$ et $L_{leakhfext}$). Afin de bien assimiler ce modèle, considérons un transformateur construit à partir d'un noyau UI et de deux bobines, une dans chaque jambe verticale.

Initialement, nous réalisons deux simulations d'une coupe frontale de ce transformateur mais seulement avec les conducteurs à l'intérieur de la fenêtre de bobinage comme indiqué dans la Figure 7a. La première simulation permet le calcul de l'inductance linéique à basse fréquence $L_{leaklfint}$ (H/m) ; elle est réalisée à la fréquence de modulation ou en continu selon le type de conversion envisagée. La seconde est réalisée à haute fréquence (typiquement la fréquence de commutation du convertisseur) et permet de déduire l'inductance linéique à haute fréquence $L_{leakhfint}$ (H/m). Ces deux simulations dépendent du volume à l'intérieur de la fenêtre de bobinage

Un deuxième groupe de simulations est à prévoir par la suite. En effet, nous simulons, en deuxième temps, une coupe frontale de ce même transformateur mais uniquement avec les conducteurs à l'extérieur de la fenêtre de bobinage, comme indiqué en Figure 7b. Ainsi, nous pouvons calculer les inductances linéiques $L_{leaklfext}$ et $L_{leakhfext}$ (H/m).



a) Conducteurs à l'intérieur de la fenêtre de bobinage *b) Conducteurs à l'extérieur de la fenêtre de bobinage*

Figure 7 : Simulations par éléments finis d'un transformateur inter-cellule (valeur absolue de l'intensité du champ magnétique).

Pour calculer l'inductance de fuite totale relative à la basse et à la haute fréquence, nous utilisons les équations suivantes:

$$L_{leaklf} = L_{leaklf\,\mathrm{int}}\, d_{\mathrm{int}} + L_{leaklfext}\, d_{ext} \tag{5}$$

$$L_{leakhf} = L_{leakhf\,\mathrm{int}}\, d_{\mathrm{int}} + L_{leakhfext}\, d_{ext} \tag{6}$$

où d_{int} est la longueur de la spire moyenne à l'intérieur de la fenêtre de bobinage et d_{ext} est la longueur de la spire moyenne à l'extérieur de la fenêtre.

Des résultats expérimentaux confirment la fiabilité de cette méthode.

Concernant le calcul des pertes fer, quelques modèles ont été évoqués. Les formes d'onde et les amplitudes des flux à haute fréquence ont été examinées. Lorsque la charge a un comportement capacitif, la forme d'onde du flux dans les bobines des ICTs à deux cellules (ou monolithiques) est triangulaire et dépend du rapport cyclique. Dans un ICT de type cyclique cascade à N cellules ou dans les jambes de liaison des ICTs monolithiques, les formes d'ondes de flux sont plus compliquées. Ces flux et les pertes qu'ils engendrent sont plus ou moins importants selon la séquence d'alimentation des différentes phases, et les séquences favorables ont été identifiées.

Pour le calcul des pertes fer, nous utilisons une équation de Steinmetz plus générale qui s'adapte bien à différents modèles de pertes fer des noyaux commercialisés par les différents constructeurs. Cette équation est présentée ci-dessous.

$$P_{av} = K_c \cdot \left(ct_0 T^2 - ct_1 T + ct_2\right)\left(s.f^{\alpha_s} + t + u.f^{\alpha_u} + v.f^{\alpha_v}\right) B_p^{\left(w.f^{\beta_w} + x.f^{\beta_x} + y + z.f^{\beta_z}\right)} \tag{7}$$

La saturation du noyau dépend des flux haute et basse fréquence. Le flux haute fréquence dépend essentiellement de la tension appliquée aux bornes des ICTs. Quant au flux à basse fréquence, il dépend du courant à basse fréquence, de la reluctance du noyau et surtout de la reluctance équivalente de l'air qui est inversement proportionnelle à l'inductance de fuite. La somme des deux flux doit, évidemment, être inférieure au produit de l'induction de saturation et la section transversale.

L'augmentation maximale de la température d'un ICT est choisie en fonction de la température ambiante et de la température maximale supportée par l'isolant du conducteur ou le matériau du noyau magnétique. La valeur de l'augmentation de la température est estimée en utilisant un modèle basé sur le calcul de la surface totale de l'ICT S qui est en contact directe avec l'air. La température de l'ICT peut être calculée en utilisant un coefficient d'échange thermique (basé sur la pratique ou sur des formules empiriques) et les pertes totales dissipées par les bobines et le noyau P_t. Le coefficient d'échange thermique H_{exc} dépend, généralement, de divers paramètres tels que la température ambiante, la pression atmosphérique, l'orientation du composant, les dimensions de la surface S et etc. L'équation déterminant l'augmentation de la température est la suivante :

$$\Delta T = {}^{P_t}\!\!\diagup\!\!{}_{S \cdot H_{exc}} \tag{8}$$

Les ICTs Monolithiques Existants

Quelques ICTs monolithiques ont été développés au sein de notre groupe de recherche. Trois d'entre eux ont été dimensionnés durant la thèse de doctorat de Valentin Costan. Deux de ces derniers ont été développés et testés. Le troisième a été construit durant cette présente thèse. L'ICT « Monobobine » est une version 2D de la topologie à double échelle. Deux ICTs à six-cellules ont été construits afin d'être utilisés dans un convertisseur ayant 12 cellules de commutation en parallèle. Chaque ICT est composé de six bobines aussi bien dans la direction verticale que dans la direction horizontale, et ce, en utilisant six noyaux en ferrite de type E.

La Figure 8 présente l'ICT développé au laboratoire. Il est à noter qu'un ICT à six-cellules a été placé côte à côte avec l'autre, mais ils n'ont en commun qu'une jambe à forte perméabilité et ils ne sont donc quasiment pas couplés. Douze noyaux type E ont été utilisés pour construire cet ICT.

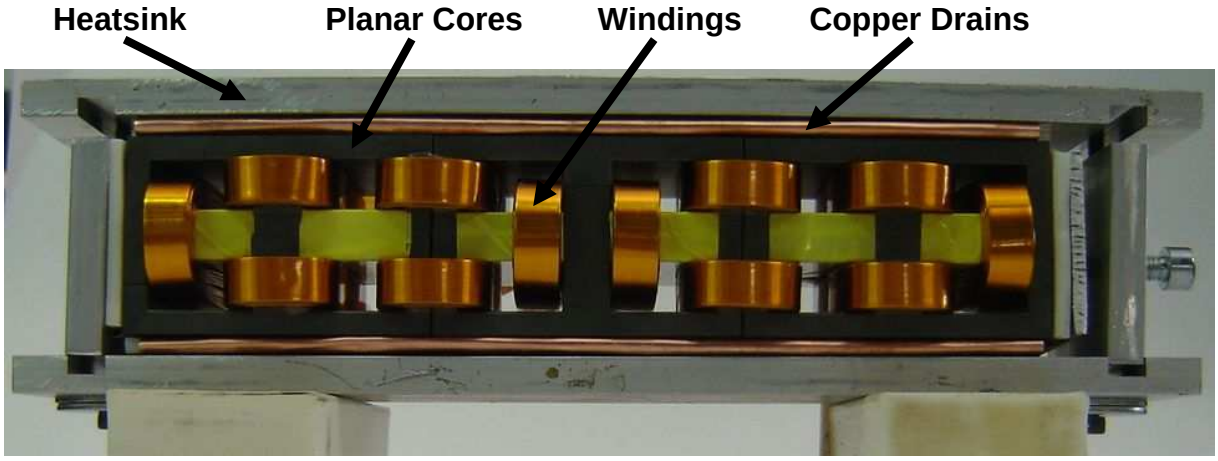


Figure 8 : ICT « MONOBOBINE ».

Les résultats expérimentaux utilisant cet ICT sont montrés sur la Figure 9. Les courants des six cellules de commutation sont montrés ainsi qu'une des tensions commutées (trait vert) et aussi la tension du bus continu (trait bleu). Il est à noter que chaque courant triangulaire à une fréquence égale à six fois la fréquence de commutation. On peut aussi remarquer la présence de courants magnétisants de faible amplitude.

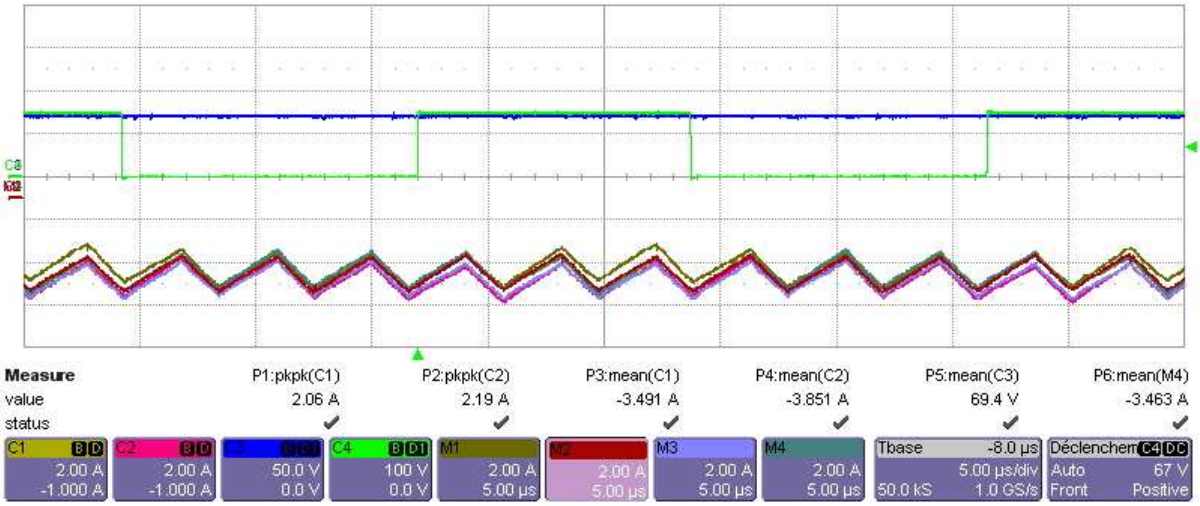


Figure 9 : Les courants dans les six cellules de commutations.

Chapitre IV – Optimisation des Transformateurs Inter-Cellules

Ce chapitre est dédié à l'optimisation des ICTs et utilise les modèles présentés dans le chapitre précédent. Des méthodes d'optimisation ainsi que des stratégies ont été examinées. Le choix des méthodes et stratégies les plus adéquats ainsi que les logiciels pour les implanter a été justifié. L'optimisation des variables et des paramètres, les contraintes et les objectifs ont été sélectionnés pour le cas d'ICTs à 2 et à *N* cellules.

Afin d'accélérer le processus d'optimisation, aucune simulation à éléments finis n'a été inclue dans la boucle d'optimisation. Par contre, une interpolation de valeurs pré-simulées stockées dans des matrices multidimensionnelles (SOR) a été réalisée. Ce processus s'avère beaucoup plus rapide que les simulations à éléments finis. Les matrices multidimensionnelles ont été générées pour quelques topologies et sont actuellement générées pour d'autres topologies. Des simulations étaient nécessaires afin de prédire les valeurs des inductances de fuites alternatives et continues ainsi que les résistances équivalentes alternatives relatives aux courants de mode commun et différentiels de la partie de la bobine à l'extérieur de la fenêtre de bobinage.

Concernant les simulations avec le logiciel FEMM, l'influence de la densité de maillage et les limites de la simulation ont été examinées pour chercher le meilleur compromis entre temps de simulation et précision. Ceci est assez important lors de la génération des matrices multidimensionnelles et ce vu qu'un grand nombre de simulations est nécessaire.

Les algorithmes d'optimisation ont été développés en utilisant quelques modèles présentés dans le Chapitre III et l'approche et le SOR expliqués dans ce chapitre. Le premier algorithme est lié au dimensionnement des ICTs à deux cellules ayant la structure représentée dans la Figure 7 et utilisée dans un convertisseur Buck.

La première étape consiste à rentrer toutes les informations concernant le processus d'optimisation : les variables, les paramètres, les contraintes et les objectifs. Ceci est réalisé en utilisant un fichier Excel (Figure 10). Après quelques itérations, l'algorithme d'optimisation peut converger ou non et les résultats sont renvoyés au même fichier Excel.

	A	B	C	D	E	F	G	H	I	J
2	**Function**	**Description**	**Name**	**Initial Value**	**Unit**	**Include?**	**Min Value**	**Max Value**		
3										
4	***OptimizationVariable***	Conductor width	ec	0.35	mm	☑ Include	0	100000		
5		Conductor height	hc	320.00	mm	☑ Include	0	100000		
6		Inter-winding distance	eww	64.00	mm	☑ Include	0	100000		
7		Core leg width	eli	27.00	mm	☑ Include	0	100000		
8		Core depth	di	35.00	mm	☑ Include	0	100000		
9		Number of turns	Nt	12.00		☑ Include	0	100000		
10		Switching frequency	Fs	20000	Hz	☐ Include	1000	100000		
11										
12	***Fixed Values***	Horizontal winding-core distance	ewc	0.00	mm					
13		Insulation thickness	eins	0.20	mm					
14		Input voltage	Vin	200	V					
15		Output DC current	Idcout	500	A					
16		Calculation temperature	Tc	100	°C					
17		Core material (3C90 Philips(20-200kHz))				CUSTOM				
18		relative permeability	Mur	1.80E+03		0				
19		saturation induction	Bsat	2.50E-01	T	0.00				
20		alpha, frequency Steinmetz coeffient	alpha	1.45E+00		0.00				
21		beta, Induction Steinmetz coeffient	beta	2.75E+00		0.00				
22		Gain, Steimetz coefficient	Cm	2.65E-03		0.00				
23		Temperature Correction coefficient 0	ct0	2.45E+00		0.00				
24		Temperature Correction coefficient 1	ct1	3.10E-02		0.00				
25		Temperature Correction coefficient 2	ct2	1.65E-04		0.00				
26		Core mass density	Dmi	5.00	Kg/l					
27		Core price	Pri	1.00	$/Kg					
28		Conductor material (Copper)				CUSTOM				
29		Resistivity	ro	2.26E-08	Ωm	1.85E-08				
30		Conductor mass density	Dmc	8.96	Kg/l	6.00				
31		Conductor price	Prc	10.00	$/Kg	11.00		Counter	257	
32		Number of harmonics calculated	Nh	200						
33		Duty Cycle	D	0.25						
34		Thermal exchange coefficient	Hexc	15.00	W/m²/°C					
35										
36	***Contraints***	Core width	ei	0.00	mm	☐ Include				
37		Core height	hi	0.00	mm	☐ Include				
38		Maximum output current ripple	Ioutrmax	100.00	A	☑ Include				
39		Maximum induction in core's leg	Bmax	0.35	T	☑ Include				
40		Maximum losses	Pmax	100.00	W	☑ Include				
41		Maximum volume	Volmax	0.00	mm3	☐ Include				
42		Maximum weight	Mmax	0.00	Kg	☐ Include				
43		Maximum price	Prmax	0.00	$	☐ Include				
44		Maximum RMS current density	Jmax	5.00	A/mm²	☑ Include				
45		Maximum Temperature Rise	Dtmax	30.00	°C	☑ Include				
46										
47	***Objectives***	(Total Mass)								

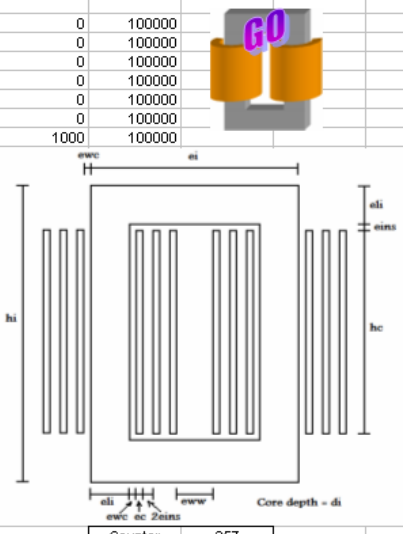
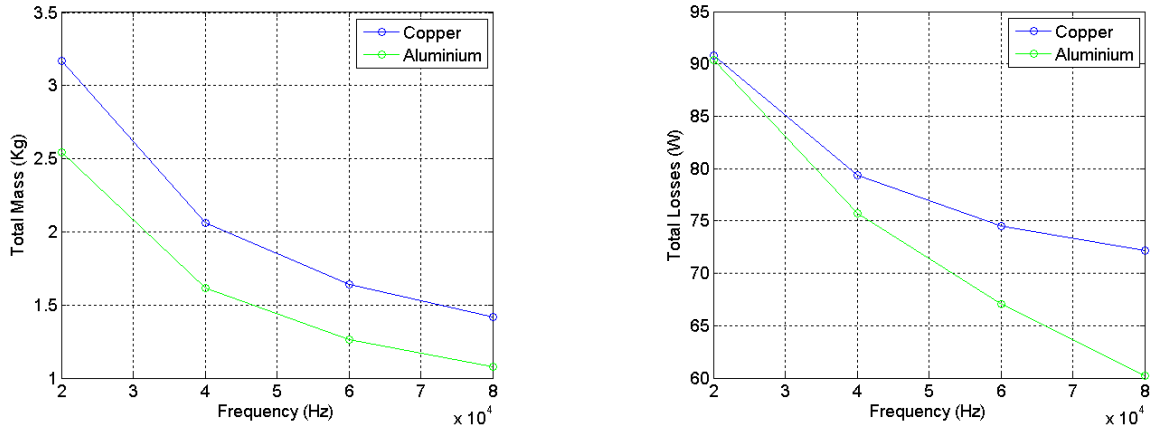


Figure 10 : Le fichier Excel utilisé pour rentrer les informations concernant l'optimisation.

Les algorithmes d'optimisation développés durant ces travaux de thèse ont été utilisés pour comparer l'utilisation de différents conducteurs et matériaux de noyau.

Les résultats montrent que les ICTs ayant les noyaux faits de matériau nanocristallin sont plus petits en taille et moins lourds que ceux ayant les noyaux faits de ferrite et ce vu que le premier matériau admet une densité de flux de saturation plus élevée. Toutefois, la différence de poids est nettement réduite pour de plus hautes fréquences car dans ce cas le dimensionnement est plus lié aux pertes fer qu'à l'induction de saturation et les ferrites redeviennent donc compétitives.

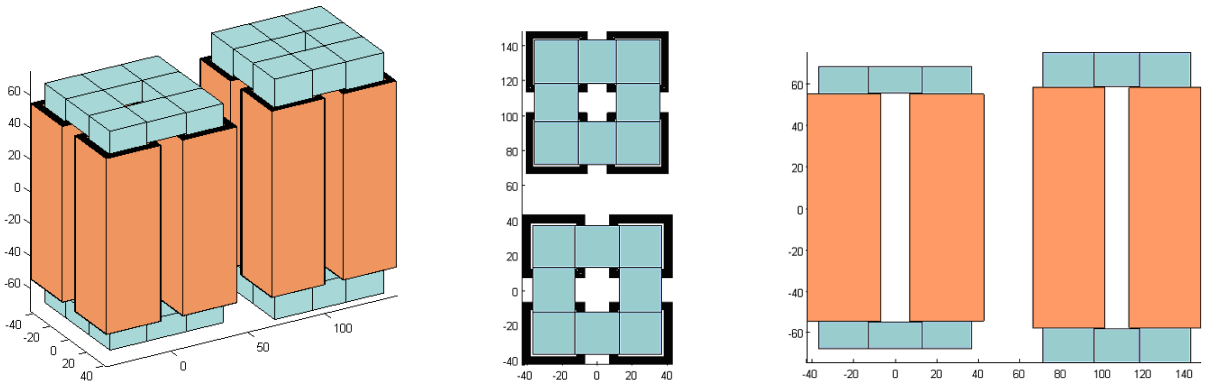
Comme exemple des résultats obtenus avec l'algorithme décrit ci-dessus, on peut chercher à minimiser le poids total de l'ICT à 4 cellules double échelle, pour quatre fréquences différentes et pour deux matériaux conducteurs utilisés pour le bobinage (cuivre et aluminium). La masse et les pertes totales des solutions optimisées sont montrées dans la Figure 11. Il est à noter que les ICTs faits avec l'aluminium présentent un poids et des pertes moindres. Bien que l'aluminium soit plus résistif que le cuivre, sa densité massique est beaucoup plus faible ; c'est pourquoi les ICTs faits d'aluminium sont toujours moins lourds.



a) Total mass *b) Total losses*

Figure 11 : Comparaison des ICTs optimisés avec différents types de conducteurs.

La forme finale de l'ICT est représentée dans la Figure 12 dans le cas d'une fréquence de commutation égale à 20kHz. La plus grande différence entre ces deux résultats réside dans la quantité de matériau conducteur. Puisque l'aluminium est beaucoup plus résistif, quasiment le double du matériau doit être utilisé afin d'obtenir les mêmes pertes ohmiques pour les deux matériaux. L'ICT basé sur l'aluminium reste néanmoins beaucoup plus léger. De plus, l'aluminium est beaucoup moins cher que le cuivre, et dans ces exemples, l'aluminium se présente comme étant le meilleur choix.



a) Vue 3D *b) Vue du dessus* *c) Vue de côté*

Figure 12 : Forme final des ICTs optimisés en utilisant des matériaux conducteurs différents (échelle en millimètre).
ICT à gauche : fait avec aluminium. *ICT à droite : fait avec cuivre.*

Augmenter le nombre de cellules fait augmenter, dans le cas des exemples montrés dans ce chapitre, le poids total de l'ICT. Cependant, si le système entier composé par un convertisseur, un ICT et un filtre (condensateur) est optimisé, le résultat pourrait être différent. En effet, si on augmente le nombre de phases, la fréquence apparente de sortie augmente et l'ondulation du courant dans chaque cellule diminue, ce qui entraine des condensateurs de sortie plus petits.

Les résultats d'optimisation montrent que les ICTs sont généralement moins lourds et produisent moins de pertes que les inductances simples quand ils sont insérées dans les convertisseurs entrelacés.

Chapitre V – ICT dans les systèmes triphasés

Dans ce chapitre, l'utilisation des ICTs dans les systèmes triphasés alternatifs est analysée. Les techniques de MLI (Modulation de Largeur d'Impulsion) concernant la disposition des porteuses et l'injection du signal d'ordre zéro (homopolaire) pour les convertisseurs triphasés parallèles sont révisés. L'influence de chaque technique et méthode concernant le flux généré au sein de l'ICT a été détaillée pour deux topologies différentes : quand deux (ou plus) sous-charges identiques n'ont pas de connexion électrique et quand ces sous-charges ont leurs neutres connectés ; ce qui revient au cas où il y a une seule charge en regard du flux généré dans le noyau d'un ICT.

Pour chaque topologie et chaque technique de disposition de la porteuse, une homopolaire rajoutée à la référence a été créée par l'intermédiaire d'un balayage d'offsets et d'un calcul du flux. Ces homopolaires optimales ont été créées afin de minimiser l'ondulation maximale du flux dans le ICT ; ce qui joue un rôle primordial dans le dimensionnement du noyau.

L'ondulation maximale du flux n'est pas le seul paramètre qui conditionne l'ajustement de la taille du noyau. En fait, l'ondulation globale du flux est aussi importante puisqu'elle génère les pertes fer qui ont une influence directe sur la taille du noyau. C'est pourquoi des comparaisons des homopolaires optimales avec d'autres homopolaires ont été proposées en analysant la forme d'onde temporelle du flux durant une période du fondamental et aussi en calculant l'ondulation maximale du flux.

Dans le cas où les neutres sont connectés, les techniques POD et PD génèrent la même ondulation du flux. La méthode optimale développée (PWMBCNP) est celle qui génère la plus faible ondulation maximale du flux et aussi la plus faible ondulation globale pour les indices de modulation supérieurs à 0,465. Un exemple de cette homopolaire et de la référence modifiée par l'homopolaire est donné dans la Figure 13, pour un indice de modulation égal à 0,7. Pour les indices de modulation inférieurs à 0,465, les méthodes de MLI discrètes sont intéressantes.

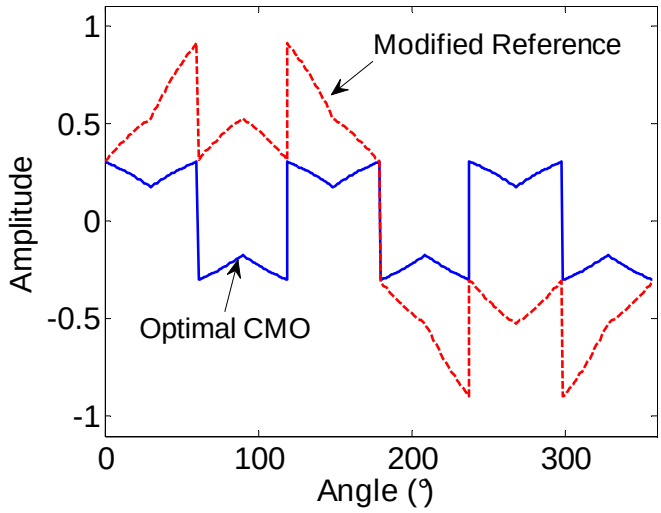


Figure 13 : CMO optimales pour les hauts indices de modulation

En général, les topologies avec les neutres séparés génèrent moins de flux dans l'ICT que les topologies où les neutres sont connectés. Quand ces neutres sont déconnectés, les techniques POD et PD génèrent différentes ondulations du flux. Si la technique PD est

utilisée, généralement les méthodes MLI discrètes créent des ondulations de flux moins importantes ; la méthode DPWM3 s'est avéré être la méthode optimale. Quand la technique POD est utilisée, les méthodes MLI continues sont celles qui donnent les ondulations de flux les moins importantes ; la méthode optimale a été créée et on l'a nommé PWMBC. Un exemple de l'homopolaire créée et de la référence modifiée par l'homopolaire est donné dans la Figure 14, pour un indice de modulation égale à 0,7. Dans la topologie « neutres séparés », la technique POD crée des ondulations de flux moins importantes que la technique PD.

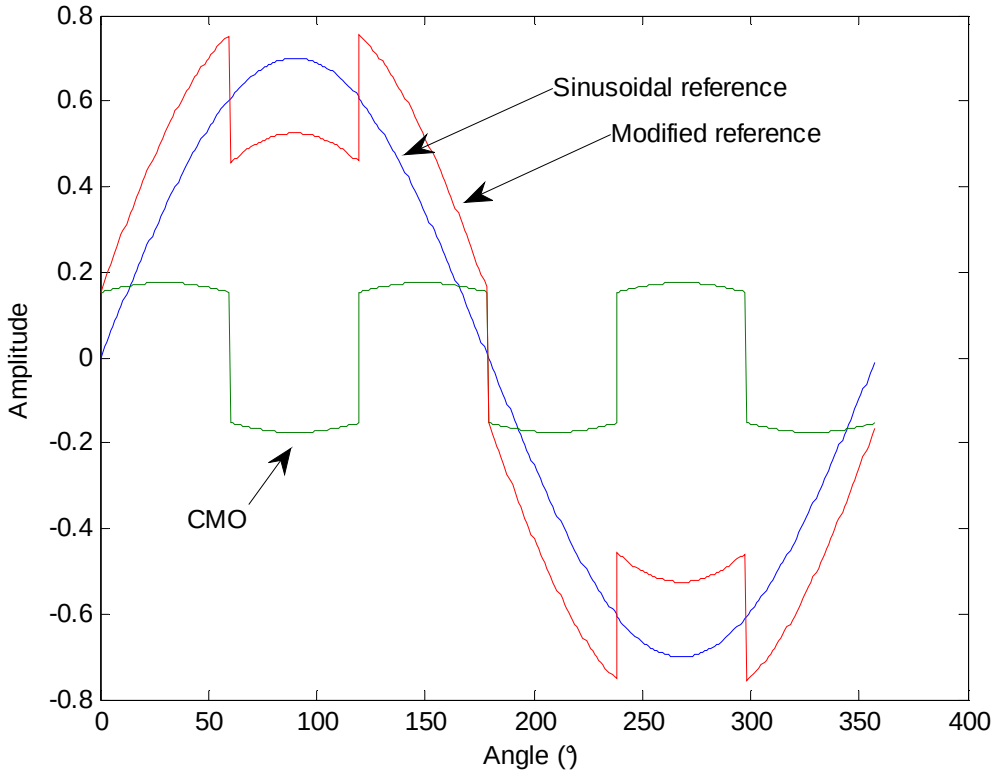


Figure 14 : Les formes d'ondes de modulation de la méthode PWMBC (Mi=0.7).

Afin de vérifier les avantages de la PWMBC par rapport aux méthodes de MLI les plus répandues, une comparaison est réalisée. Le flux haute fréquence pour tous les angles de la période du fondamental est calculée pour chaque méthode de MLI appliquée à un système contenant deux cellules de commutation par phase. La plus haute ondulation de flux de chaque méthode de MLI a été représentée dans la Figure 15 et ce pour des indices de modulation allant de 0.1 à 0.9.

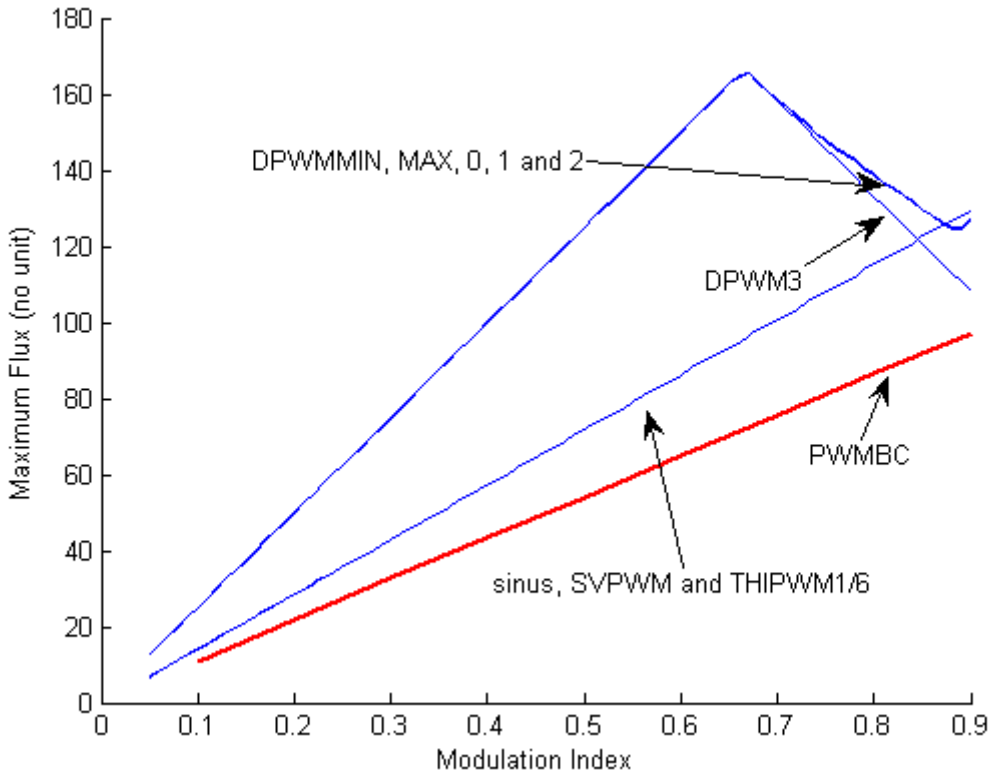


Figure 15 : L'ondulation maximale du flux calculée pour différentes méthodes de MLI.

Noter que la méthode PWMBC génère toujours moins d'ondulation de flux que les autres méthodes et que la réduction du flux est approximativement égale à 22% par rapport aux méthodes de MLI continues. Il est intéressant de signaler que les méthodes de MLI discrètes produisent beaucoup plus d'ondulation de flux que les autres méthodes. Ceci constitue un inconvénient majeur pour ce type de MLI.

La plupart des analyses développées dans ce chapitre ont été confirmées par des résultats expérimentaux et ce en utilisant deux onduleurs triphasés connectés à deux charges résistives triphasées à travers des inductances. Les deux cas (neutres connectés ou non) ont été vérifiés. Les résultats expérimentaux trouvés coïncident parfaitement aux résultats issus du calcul et des simulations réalisées sur logiciel PSIM.

Etant donné que la différence de courant entre deux phases dans ICT est une image du flux circulant dans ce composant, sur la Figure 16 les différences de courant de la phase U du montage expérimental sont représentées. Ces résultats ont été obtenus en utilisant une tension de bus continu approximativement égale à 150V, un indice de modulation égal à 0,7, une fréquence de commutation égale à 4kHz, une fréquence de modulation égale à 50Hz et une sous-charge de 4kW.

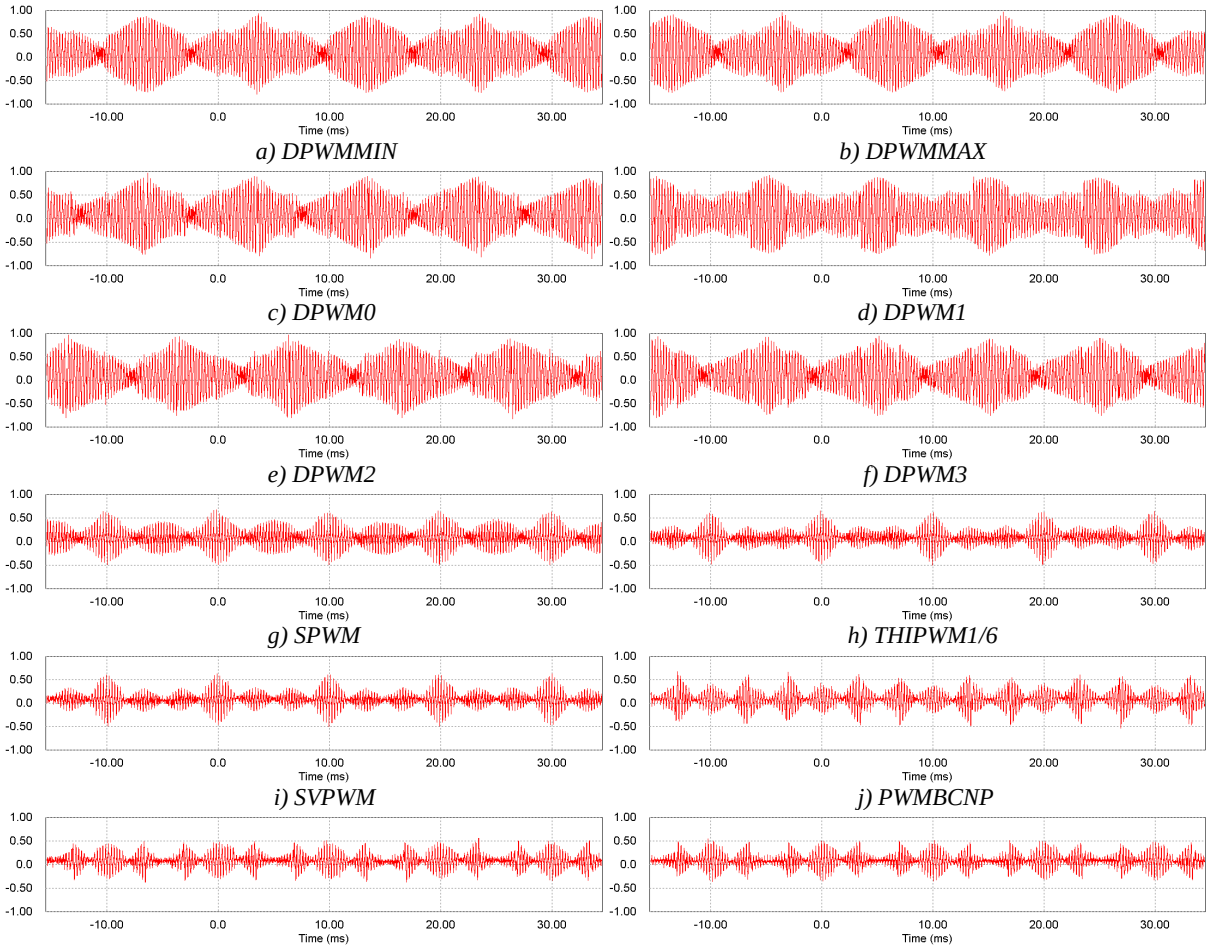


Figure 16 : La différence des courants mesurés pour différentes méthodes de MLI.

Les résultats expérimentaux coïncident très bien avec les résultats de simulation obtenus. Noter que la MLI vectorielle à trois niveaux (SV3PWM) présente des formes d'onde similaires à celles de la PWMBC. Ceci est dû à la similitude des homopolaires pour certains indices de modulation.

En résumant les différents résultats présentés dans cette section, nous pouvons dire que l'homopolaire optimale concernant la minimisation du dimensionnement de l'ICT n'est pas celles présentées ci-dessus vue que les pertes fer ne sont pas prises en compte dans les algorithmes développés dans cette thèse. La solution serait inclure ces algorithmes dans les boucles d'optimisation présentées dans le Chapitre IV.

Conclusions

L'idée initiale de mon doctorat était l'étude des pertes cuivres haute fréquences dans les enroulements des transformateurs inter-cellules. Pour cette raison l'effet de peau et l'effet de proximité ont été analysés en détail et de cette étude plusieurs conclusions et règles d'usage ont été formulés. Un résultat important est un ensemble de tableaux qui ont été créés pour aider les concepteurs de transformateurs à choisir la meilleure position des bobinages dans les transformateurs.

On ne s'est pas restreint aux pertes cuivre et c'est pour ça qu'une grande partie du travail a été dédié à la conception de ce type de transformateur. Le dimensionnement des transformateurs inter-cellules a été divisé en 4 parties principales, qui sont liées au calcul de 4 grandeurs clés : Pertes cuivre, pertes fer, flux magnétique et température du transformateur. Plusieurs modèles ont été évoqués et quelques uns ont été retenus. Nous avons montré qu'il y a plusieurs paramètres qui interviennent dans le dimensionnement des transformateurs inter-cellules et que par conséquent l'optimisation de ces composants serait nécessaire. Plusieurs algorithmes d'optimisation ont été donc développés et des matrices de résultats ont été traitées par interpolation multidimensionnelle pour faciliter et accélérer leur utilisation. Ceci évite de recourir à la simulation par éléments finis au sein de la boucle d'optimisation elle même.

La dernière partie du travail s'est concentrée sur l'utilisation des transformateurs inter-cellules dans les systèmes triphasés. L'influence des méthodes MLI et de la composante homopolaire sur le dimensionnement des ces composant a été étudiée Des formes de composantes homopolaires spécifiques pour chaque stratégie MLI et chaque topologie convertisseur/charge ont été créées afin de minimiser le flux dans les transformateurs permettant ainsi de réduire davantage la masse et la taille de ces composants. Des comparaisons entre différentes méthodes MLI ont été effectuées et vérifiées expérimentalement.

Contents

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List of Symbols Used

a_n	Amplitude of the nth Harmonic
A_s	Core's Cross-Section Area
B_p	Peak Flux Density
d_{int}	Average Turn Length Inside the Core Window
d_{out}	Average Turn Length Outside the Core Window
E	DC Bus Voltage
f	Frequency
Fl	Ratio between the AC and the DC inductance
F_{lim}	Limit Frequency
Fr	Ratio between the AC and the DC resistance
Fr_{eq}	Equivalent Ratio between the AC and the DC resistance for a given waveform
Fr_n	Ratio between the AC and the DC resistance for the n^{th} harmonic
Fr_p	Ratio between the AC and the DC resistance of the p^{th} layer
Fs	Switching Frequency
h	Core Window Height
H_{exc}	Thermal Exchange Coefficient
I_{CM}	Common Mode Current
I_{DC}	DC Load Current
I_{DCx}	DC Current of Commutation Cell "x"
I_{DM}	Differential Mode Current
I_o	Output Current
I_x	Current of Commutation Cell "x"
L	Self Inductance of an ICT
L_{leak}	Leakage Inductance
L_x	Inductance of the xth inductor
M	Mutual Inductance of an ICT
Mi	Modulation Index
N	Number of Paralleled Commutation Cells

n	Number of the Harmonic
N_t	Number of Turns
p	Position of the Winding Layer
P_{cu}	Copper Losses
P_t	Total Losses
Q	Dowell's Factor. Conductors thickness divided by the skin depth
R_{DCint}	DC Resistance of the part of the winding inside the core window
R_{DCout}	DC Resistance of the part of the winding outside the core window
$Rel\ldots$	Reluctance of a Part of the Magnetic Circuit
S	Total Surface of a Component
T	Current Period
U,V,W	Phases of a Three-Phase System
V_o	Output Voltage
V_x	Switched Voltage of Commutation Cell "x"
W_w	Winding Area Width
α'	Modified Duty Cycle
α , D	Duty Cycle
δ , Ep	Skin Depth
ΔI_o	Output Current Ripple
ΔI_x	Current Ripple of Commutation Cell "x"
ΔT	Temperature Rise of a Magnetic Component
η	Porosity Factor
μ	Permeability
μ_0	Permeability of the Free Space
μ_r	Relative Permeability
σ	Electrical Conductivity
ϕ	Magnetic Flux
ϕ_{DC}	DC Flux in the Wound Leg
ϕ_{max2}	Maximum Flux Ripple in an 2-Cell ICT
ϕ_{maxN}	Maximum Flux Ripple in an N-Cell ICT

Glossary of Terms

3DPHI	3D Power Hybrid Integration Project
APOD	Alternative Phase Opposition Disposition
CMO	Common Mode Offset
CPWM	Continuous PWM Methods
DPWM	Discontinuous PWM Methods
DPWM0	60° Discontinuous PWM - Suitable for 30° Leading Power Factor
DPWM1	60° Discontinuous PWM - Suitable for Unity Power Factor
DPWM2	60° Discontinuous PWM - Suitable for 30° Lagging Power Factor
DPWM3	30° Discontinuous PWM
DPWMMAX	120° Discontinuous Modulation - Held to Positive Rail
DPWMMIN	120° Discontinuous Modulation - Held to Negative Rail
FEM	Finite Element Method
FEMM	Finite Element Method Magnetics – This is a specific software
ICT	InterCell Transformer
LAPLACE	Laboratoire Plasma et Conversion d'Energie
MATLAB	Numerical Analysis Program
MMF	Magnetomotive Force
NPC	Neutral Point Clamped
PD	Phase Disposition
POD	Phase Opposite Disposition
PS	Phase Shift
PSIM	Power Electronic Simulation Software
PWM	Pulse Width Modulation
PWMBC	Optimal PWM Method in Terms of the ICT Flux – Dual Load Case
PWMBCNP	Optimal PWM Method in Terms of the ICT Flux – Single Load Case
RMS	Root Mean Square
SOR	Set of Results
SPWM	Sinusoidal Pulse Width Modulation
SV3PWM	Three-level Centered Space Vector Modulation
SVM	Space Vector Modulation
SVPWM	Two Level Centered Space Vector Modulation
THD	Total Harmonic Distortion
THIPWM1/6	3rd Harmonic Zero Sequence Signal Injection
VRM	Voltage Regulator Modules
VSI	Voltage Source Inverter

Publications

Several parts of the PhD research presented in this thesis have been published by the author during the course of the research work. These publications are listed below:

1. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Winding Position in Power Transformers to Reduce copper Losses: Non-Sinusoidal Currents* In: IEEE Transactions on Power Electronics. To be published.
2. F. Forest; B. Gelis; J.-J. Huselstein; B. Cougo; E. Laboure; T. Meynard. *Design of a 28V-to-300V-12kW Multi-Cell Interleaved Flyback Converter Using InterCell Transformers* - In: IEEE Transactions on Power Electronics. vol. 25, no. 8, pp. 1966-1974, 2010.
3. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Optimal PWM method for flux reduction in InterCell Transformers coupling double three-phase systems* In: XIIIème conférence Electronique de Puissance du Futur, 2010, Saint-Nazaire - France.
4. F. Forest; B. Gelis.; J.-J. Huselstein; B. Cougo; E. Laboure; T. Meynard. *Conception et réalisation d'un Flyback à huit cellules 28V-300V-12kW utilisant des transformateurs intercellulaires* In: XIIIème conférence Electronique de Puissance du Futur, 2010, Saint-Nazaire - France.
5. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Parallel MultiCell Converters for High Current: Design of InterCell Transformers* In: International Conference on Industrial Technology, 2010, Vina del Mar, Chile.
6. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Winding Position in Power Transformers to Reduce copper Losses: Non-Sinusoidal Currents* In: IEEE Energy Conversion Congress and Exposition, 2009. San Jose - USA.
7. B. Cougo; V. Costan; T. Meynard; F. Forest; E. Laboure. *A New Intercell Transformer for Interleaved Converters* In: 13th European Conference on Power Electronics and Applications, 2009. Barcelona - Spain.
8. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Calculation of Inductances in Intercell Transformers by 2D Simulation* In: COMPUMAG, 2009. Florianopolis - Brazil.
9. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Calculation of Copper Losses in Intercell Transformers by 2D Simulation* In: COMPUMAG, 2009. Florianopolis - Brazil.
10. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Pre-processing of Inductances for Intercell Transformer Optimization* In: COMPUMAG, 2009. Florianopolis - Brazil.
11. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Positionnement de bobines de transformateurs de puissance minimisant les pertes cuivre* In: European Journal of Electrical Engineering, vol. 12/2, pp. 209-223, 2009.
12. B. Cougo; T. Meynard; F. Forest; E. Laboure. *Positionnement de bobines de transformateurs de puissance minimisant les pertes cuivre* In: XIIème conférence Electronique de Puissance du Futur, 2008, Tours - France.

General Introduction

This PhD research combines intellectual and financial contributions of several persons and organizational entities. Financially speaking, the support of the PhD student was entirely covered by the CNPq (National Council for Scientific and Technological Development), a Brazilian public organization of which objective, among others, is to fund Brazilians to acquire scientific and technological skills around the world.

Some laboratories, universities and technology companies have directly and indirectly contributed to the study presented here. This work is part of a greater project called 3DPHI (3D Power Hybrid Integration). This project is related to the hybrid integration of power electronic systems and aims to develop new technologies considering aspects such as: topologies, designs, materials, procedures, passive components…

The thesis was all developed at the "*Laboratoire Plasma et Conversion d'Energie*" (LAPLACE), at Toulouse, France, supervised by Professor Thierry Meynard. Actually, this laboratory was the founder of the 3DPHI, and this is one of the reasons why several researchers indirectly contributed to this work.

Among all the laboratories integrating the 3DPHI project, two of them had a direct participation on the scientific discussions: IES Montpellier, represented by Professor François Forest; and SATIE/LGEP, represented by Professor Eric Labouré. In fact, different studies were developed thank to the collaboration of these three laboratories and some of them resulted in different conference and journal papers.

The optimization of the magnetic component studied in this thesis was first developed during the partnership of our research group with Professors Philippe Viarouge and Jérôme Cros, of the Laboratoire d'Electrotechnique, Electronique de Puissance et Commande Industrielle (LEEPCI) of the University of LAVAL, at Quebec, Canada.

The topology most investigated in this study is a consequence of technical discussion between our group and Alain Lacarnoy, from the UPS manufacturer APC/MGEUPS. We have also been collaborating with LIEBHERR Aerospace (at Toulouse), to evaluate the potential of the ICT for application in high speed drives (several tens of kW, several tens of thousand rpm). This partnership contributed significantly to the comprehension of the design and optimization of magnetic components and the development of new techniques applied to three-phase systems.

Characterization and realization of some magnetic components were also performed by the company CIRTEM (at Toulouse), which allowed verifying some of the assumptions made during the study.

THE RESEARCH

Increasing the power density of converters is one of the main objectives in Power Electronics and this may be achieved by the miniaturization of power converters. Multilevel converters are a good option to increase total power and specific power. Both series and parallel multilevel converters increase the number of levels of the current and/or voltage at the

input/output of the converter. They also increase the apparent frequency of these values. These two characteristics provide the reduction of passive filters usually found in static converters. As will be seen in Chapter I, by the use a special passive component, parallel multilevel converters have some internal values reduced, which is not the case of its series counterpart. These passive components are magnetically coupled inductances called InterCell Transformers (ICT).

The present dissertation focuses on these components and aims at answering some questions, such as:

- What are the main phenomena related to an ICT design?
- How to precisely design and optimize an ICT considering all related phenomena?
- What is the influence, in the ICT design, of parameters such as the structure, the number of paralleled cells or the conductor and core materials?
- How should we optimize the ICT?
- What is the influence of an ICT in three-phase systems?

InterCell Transformers are a relatively new subject in the scientific literature which has recently seen a growing application market. The originality of the work presented here is mainly related to the approach used to design and optimize an ICT. Accurate methods for calculating copper and core losses combined with thermal model allow predicting the best ICT regarding one of the main objectives: minimization of the volume, weight, price or total losses.

The work developed in this dissertation presents several original results which may be useful for professionals in Power Electronics using not only ICTs but also regular inductors and transformers. One of these results is a table containing some constants which may be used to tell which configuration should be adopted when inserting a winding inside the core window of a transformer. Other interesting original results are the zero sequence signals created to minimize the flux in the ICTs used to magnetically couple multiple three-phase systems.

DISSERTATION OVERVIEW

In the first chapter we compare the widely studied series multilevel converter with its dual counterpart: the parallel multilevel converter. The parallelization of commutation cells combined with interleaving techniques provides especially high output current while using standard semiconductors. It also reduces the output ripple and increases the converter's dynamics. We show that massive parallelization is only possible by the use of a special magnetic component: the InterCell Transformer (ICT). Several topologies and type of ICTs are presented as well as the main applications in the industrial and in the academic environments.

Second chapter deals with a very important aspect of an ICT design: high frequency copper losses. Discussion about related phenomena (in particular Skin and Proximity effects) allows understanding the techniques and smart practices which must be adopted in order to reduce copper losses. For that purpose, a comparison between analytical formulation and simulation using Finite Element Method (FEM) softwares is made and the validity of each method is identified. At the end of the chapter, a simple method is developed to help

transformer designers to identify the best configuration of conductors inside a given core window.

The ICT design is considered in the third chapter. The analysis is divided in four main aspects: copper losses, core losses, core saturation and temperature rise of the ICT. More or less accurate models of all related phenomena are considered, depending on the existing development tools and available time. Copper losses are calculated considering the different phenomena in different parts of the winding. Core loss calculation relies on different models and on the information given by manufacturers. Core saturation is avoided by predicting low and high frequency fluxes, which are calculated using reluctance models having parameters mainly determined by FEM simulation. The ICT temperature calculation, although very important, relies on simple models and is a weak point of the design process.

Chapter IV uses some of the models explained in the preceding chapter to develop optimization algorithms aiming to reduce the ICT weight, volume, losses or costs. Precise FEM simulation of leakage inductance and AC resistance of ICTs take a significant time if inserted in an optimization loop. For this reason several simulations are performed varying all the parameters which may modify the leakage inductance and AC resistance, which are the frequency, number of turns and geometrical parameters. The results are stored in multidimensional matrices which have the values locally interpolated for the use in the optimization loop. The last section of this chapter is dedicated to the comparison of ICT designs with regard to core and conductor material, number of cells and switching frequency. Finally a comparison between converters made with coupled or uncoupled inductors is presented.

In the last chapter, the use of ICTs in three-phase systems is considered. We start it showing the equivalence between PWM strategies used for series and parallel multilevel converters. The influence of carrier disposition methods in the flux flowing in the ICT is presented for two different load configurations: the first where there is only one regular three-phase load, and the second where the load is divided into two equal sub-loads and their neutral points are not connected. The injection of zero sequence signals in the output voltage reference changes the flux flowing in the ICT. For this reason optimal zero sequence signals were developed to minimize the ICT flux and consequently the ICT weight and size. Experimental results verify the analysis presented in this chapter and validate the flux reduction provided by the developed optimal zero sequence signals.

General conclusions close the text along with some suggestions about the directions the future research should take.

Chapter I

InterCell Transformer for Interleaved Converters

I.1 Multilevel Converters

There has been about 50 years since multilevel conversion was first described in the literature [1]. Several inverters generating phase-shifted 50Hz square voltages were connected to 50Hz transformers with the secondaries in series summing these square voltages to increase power and reduce THD. In the second generation of converters, the 50Hz transformer was placed on the rectifier side thus allowing direct connection of the outputs of the inverters fed by floating DC buses (topology later classified as "Cascaded" converters). Provided the parasitic capacitance of this transformer is low enough, switching at more than 50Hz is possible, and interleaving can then be considered with respect to the switching frequency. The next significant step came in the 70s with the Neutral Point Clamped Inverter, the first converter generating a multilevel voltage without any magnetic component. In the early 90s the Flying Capacitor [2] was introduced, followed by the Stacked MultiCell [3] and many combinations of all these different techniques.

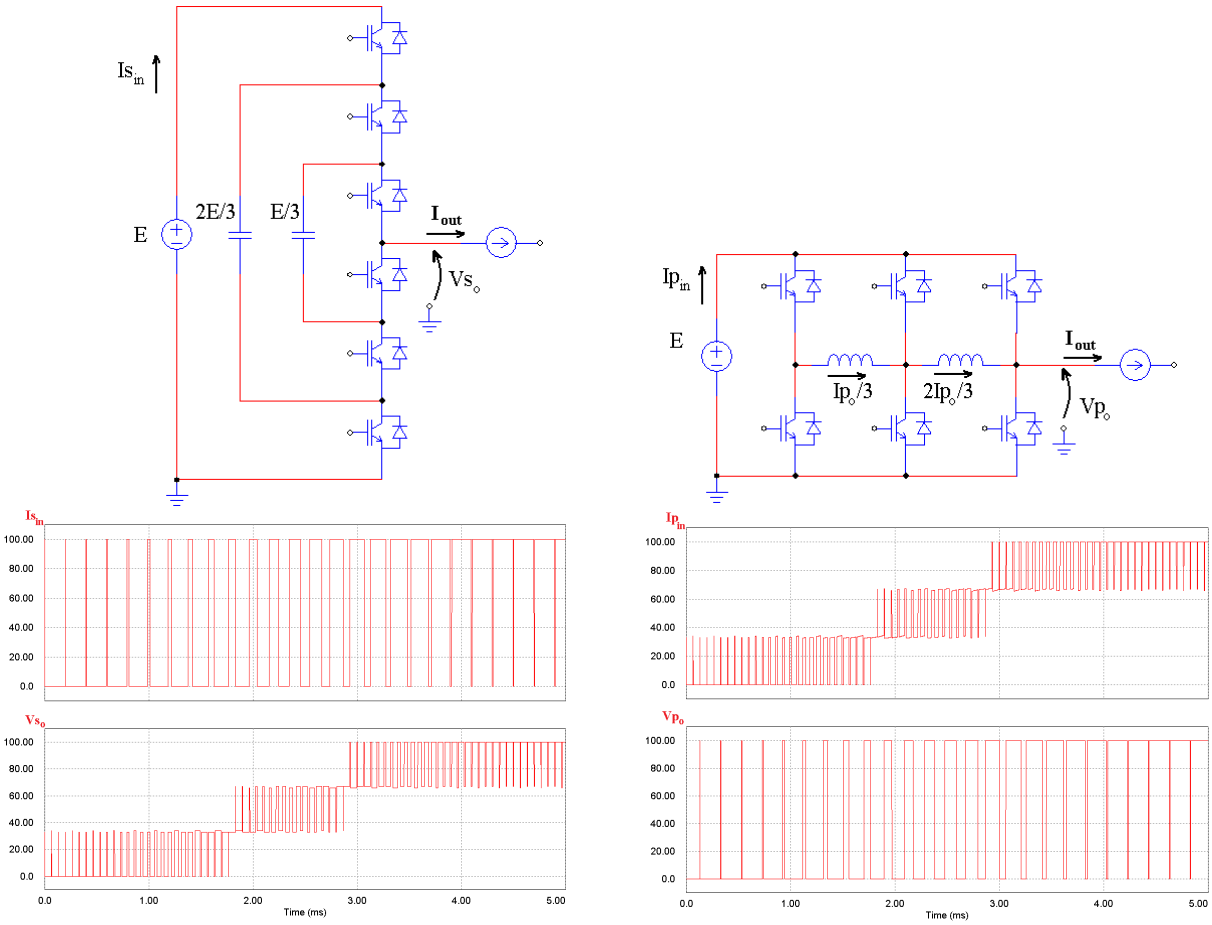
Speaking of converters or commutation cells connected in parallel through inductors to handle higher currents, it seems that they have been around for so long that it is very difficult to identify the introduction of the concept. In this field, it seems that interleaving has always been here and even the use of magnetic coupling was known in the 50s under the name of interphase transformers allowing cancellation of low frequency harmonics. More recently, the transposition of this principle to the domain of switching frequency has received a lot of attention in the field of Voltage Regulator Modules used for the supply of microprocessors with drastic dynamic requirements.

Strangely enough, the link between Multilevel converters or MultiCell converters on the one hand, and Interleaved converters, on the other hand, has not been always obvious. In the following introduction, we will try to show this link, and in the last chapter, we will also use this link to transpose the three-phase modulation concepts developed for Multilevel converters to the case of Interleaved converters.

I.1.1 Series or Parallel Multilevel Converters

Duality rules show that the multilevel output voltage of series multicell converters transposes in the form of a multilevel input current in parallel converters. As an example, in the series multicell topology of Figure I.1a a four-level voltage waveform at $3F_s$ can be generated across the current source using phase-shifted control signals [4][5], and in the parallel multicell of Figure I.1b, a four-level current at $3F_s$ is taken from the voltage source [6]. The corresponding waveforms are given for a duty cycle ramping from 0 to 95%.

However, an even better solution for paralleling commutation cells is obtained using star-connected inductors carrying equal currents (Figure I.2). The most obvious advantage of this topology is that it generates four-level waveforms at $3F_s$ on both sides.



a) Series Multicell *b) Parallel Multicell*

Figure I.1: Two dual multilevel topologies and corresponding waveforms (E=100V, I_{out}=100A, F_s=5kHz).

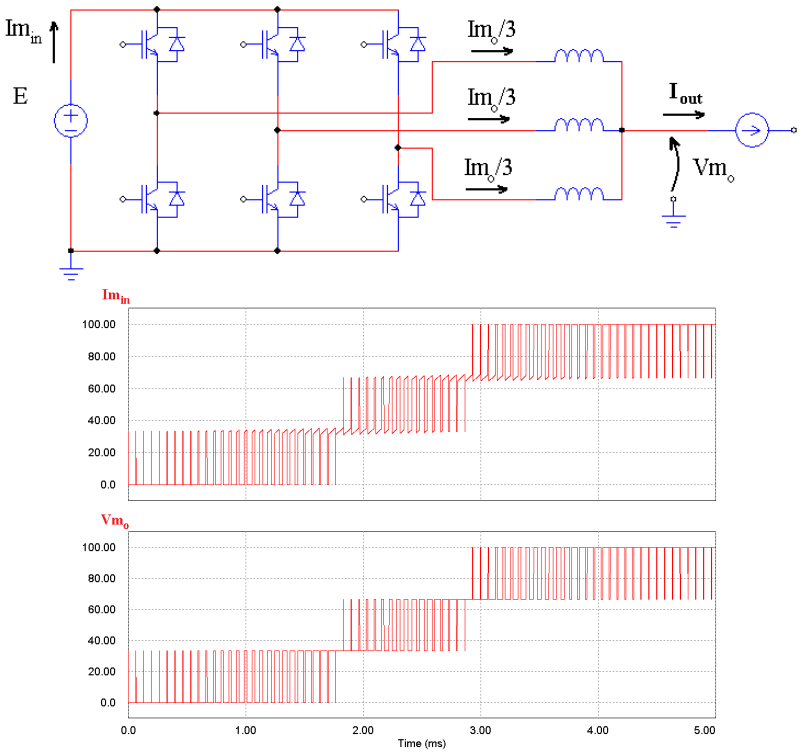


Figure I.2: Parallel multicell converter and corresponding input and output waveforms (E=100V, I_{out}=100A, F_s=5kHz).

The second advantage is that the energy stored in the star-connected inductors directly contributes to the filtering of the output current. To evaluate this topology in terms of trade-off between the energy stored in passive components and the quality of the current and voltage waveforms, we give in Figure I.3 and Figure I.4 the waveforms obtained with series and parallel three-cell converters equipped with the same input filter, the same energy stored in the output inductors (50µH\100A for the series multicell, 3 times 150µH\33.3A for the parallel multicell), and the same energy in the output capacitor. In this comparison, the energy stored in the flying capacitors appears as an extra price to pay for. As can be seen from the waveforms, the output current ripple is exactly the same in both converters, but the multilevel operation at the input side of the parallel multicell gives a significant reduction of the current ripple.

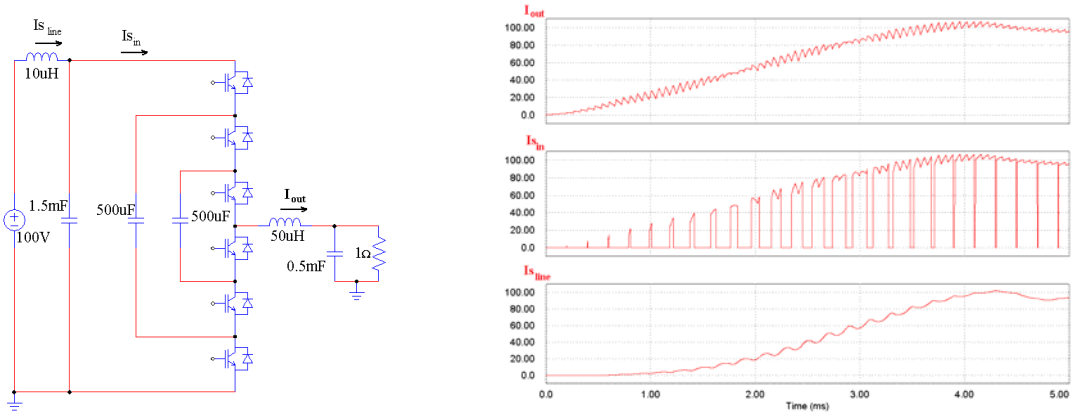


Figure I.3: Series multicell converter and filter waveforms (F_s=5kHz).

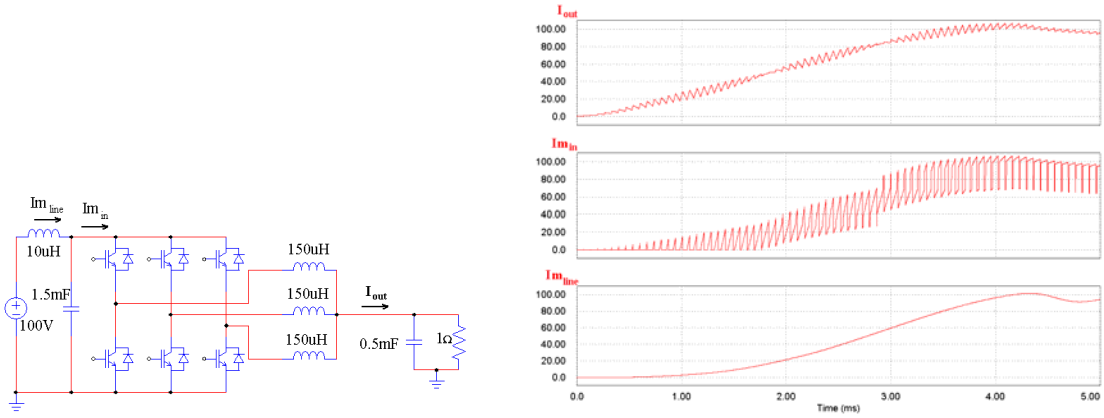


Figure I.4: Parallel multicell converter and filter waveforms (F_s=5kHz).

The circuits in Figure I.1a and Figure I.1b are the dual of each other. Their voltage and current waveforms are swapped which explains that they are equivalent in terms of energy to be stored in the filters. The circuits in Figure I.1b and Figure I.2 share many properties, but they do not have the same energy stored in the inductors, and they do not deliver the same output voltage waveform. Since the circuit in Figure I.2 is similar, but better than the one in Figure I.1b, the dual of first should be better than the dual of the latter (Figure I.5). Unfortunately, circuits that cannot be drawn without crossing unconnected wires do not have a dual, which means that in this case, the dual does not exist.

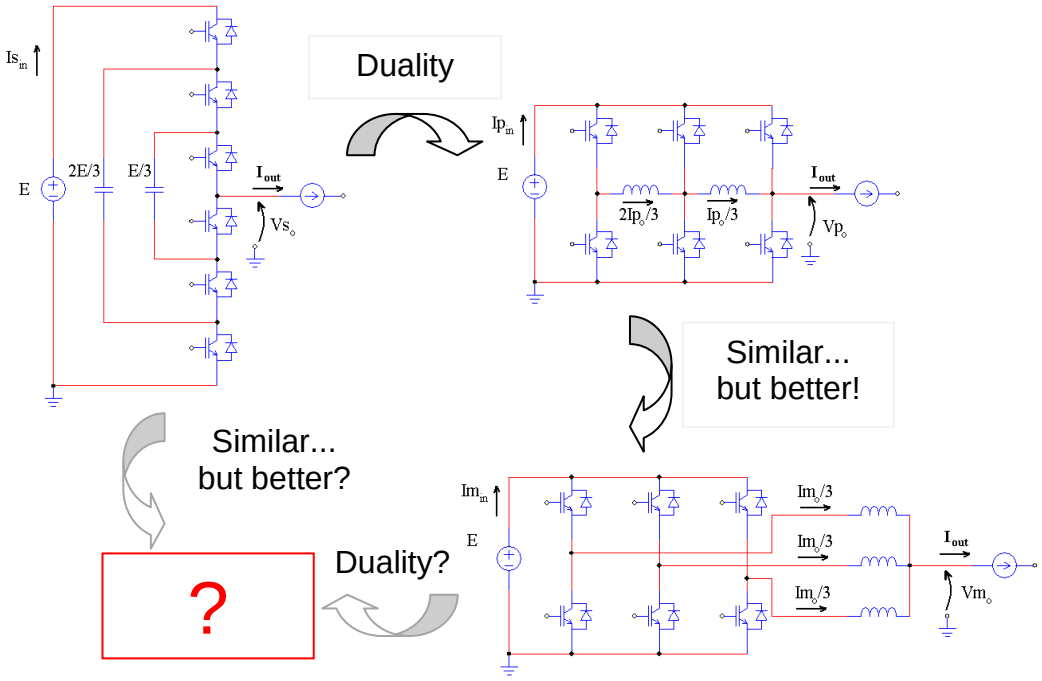


Figure I.5: Duality and similarity between series and parallel multilevel converters.

To be quite complete we should add that there is a special case where this dual exists; with 2 cells only, the dual can be found and it is indeed a three-level circuit that is of interest despite the fact that the load is floating. This circuit, which is presented in Figure I.6, can for example be used as a very good three-level chopper to control the energy flowing between a battery or supercapacitor and a DC bus.

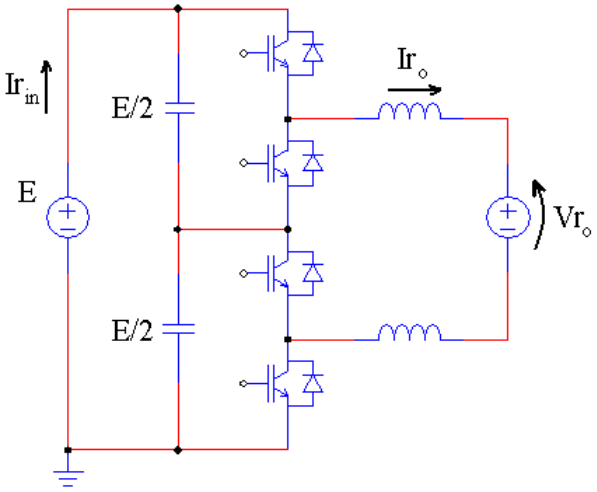


Figure I.6: 3-level version of the dual of the parallel circuit of Figure I.2 .

I.1.2 Interleaved Parallel Converters

Paralleling techniques can be applied to many different types of power converters, such as: Flyback [7][8], boost [9][10], AC choppers [11][12][13], resonant converters [14] and especially in regular DC choppers [15][16][17][18] and inverters [19][20][21]. For the purpose of explaining an extra advantage of parallel multilevel converter, a parallel multicell Buck converter will be used as a reference and it may be represented by the converter shown in Figure I.7.

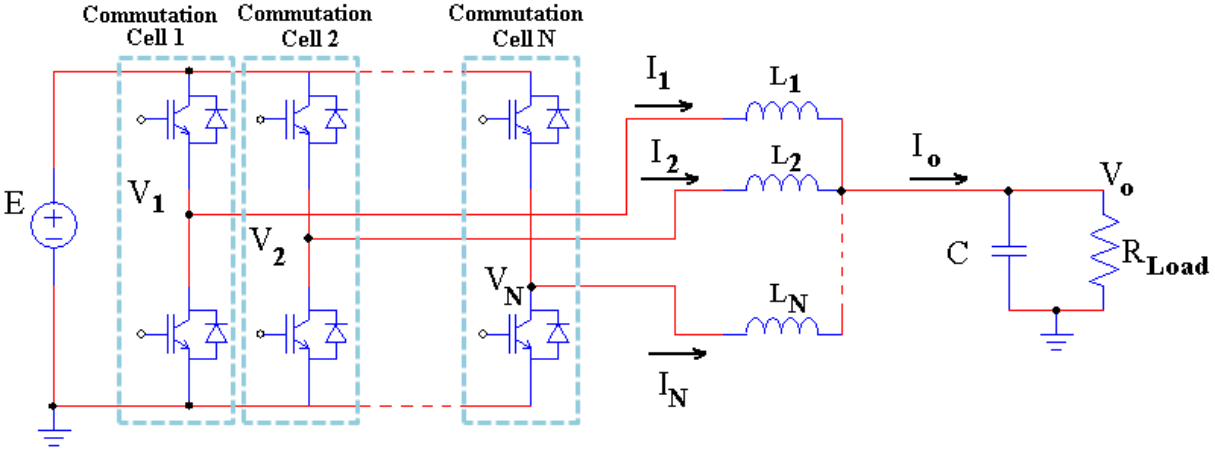


Figure I.7: Parallel Multicell Buck.

In this figure, the converter has N commutation cells interconnected by separate inductors (L_1=L_2=…=L_N=L). Since it is a symmetrical system, each inductor carries a current equal to I_o/N. Each commutation cell has the same duty cycle (α) but their corresponding carriers have a phase difference of $2\pi/N$. Thus, voltages V_1,…,V_N are rectangular voltages (with levels 0 and +E) with the same phase difference and frequency.

Considering the output voltage a constant value due to the presence of an output filter represented by capacitor C, the current ripple in each commutation cell is calculated as follows:

$$\Delta I_x = \frac{\alpha(1-\alpha)E}{LF_s} \tag{I-1}$$

where E is the DC bus voltage and F_s is the switching frequency of the converter. The ripple of the output current is determined by the aid of relative duty cycle α' [22]:

$$\forall\, i \in \{0,1,\ldots,N-1\},\ \forall \alpha \in \left[\frac{i}{N},\frac{i+1}{N}\right],\ \alpha' = N\alpha - i \tag{I-2}$$

As a result, the output current ripple is:

$$\Delta I_o = \frac{\alpha'(1-\alpha')}{N}\cdot\frac{E}{LF_s} \tag{I-3}$$

In order to verify the advantage of interleaving the phases, the ratio between the output current ripple and the maximum phase current ripple ($\Delta I_0/\Delta I_{x(max)}$) is shown in Figure I.8 for each duty cycle and for 1, 2, 3 and 4 phases. It is clear by this figure that the higher the number of interleaved phases, the smaller the ripple in the output current. As a consequence, a smaller output filter may be used. Also, we can see that the output current ripple reaches zero when the duty cycle is equal to a multiple of $1/N$. As in all interleaved converters, the

apparent frequency in the output is equal to N times the switching frequency of each commutation cell. Thus, the associated filter may be further reduced.

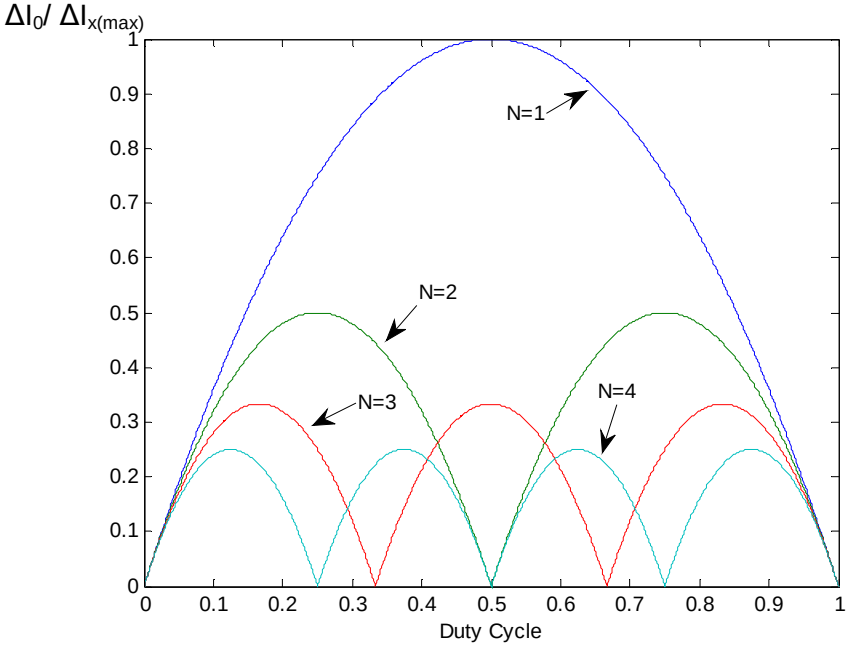


Figure I.8: Reduction of the output current ripple when increasing the number of cells.

The reduction of the total weight of the inductances used in the output of the parallel buck converters when the number of phases is increased can be verified by the reduction of the energy stored in these inductors. If the output current ripple is constant, each inductor of an N-cell converter has the inductance shown in the equation below:

$$L = \frac{L_s}{N} \tag{I-4}$$

where L_s is the inductance of a single cell converter. The energy stored in the inductor of a single cell converter is equal to

$$W_s = \frac{L_s I^2}{2} \tag{I-5}$$

and the total energy stored in the N inductors of an N-cell converter is

$$W_N = N\frac{L\left(I/N\right)^2}{2} = \frac{L_s I^2}{2N^2} = \frac{W_s}{N^2} \tag{I-6}$$

Compared to a single cell converter, an N-cell converter has N^2 times less energy stored in their output inductors, for the same output ripple. This stored energy reduction leads to another important advantage of this type of converter: the improvement of the dynamic response. For example, if there is a step on the duty cycle of a buck converter, both overshoot and response time are reduced if the number of cells are increased.

I.1.3 Limitations of the Use of Interleaved Converters

One could think about building a converter having a very high number of cells with very small inductors in each. From a realistic point of view, this is not an easy task since the phase shift between the commutation cells is equal to $2\pi/N$, which is usually provided by

carriers having different phases. Such a phase shift is impractical if using digital control based on discrete time carriers.

Another negative aspect of massive paralleling is the current imbalance in each cell. Any type of difference between each commutation cell may be the origin of an important imbalance. The differences may be related to the active components (different conduction resistances or conduction threshold), the passive components (different inductances and winding resistances) or even to the control circuit (different duty cycles due to the discretization of carriers and reference signals). A complete study about this problem is presented in [22]. In [23] authors discuss about digital control using an FPGA with the purpose of reducing the influence of cell differences in the current imbalance.

The major drawback about paralleling a high number of commutation cells is the augmentation of the current ripple in each cell if the output current ripple is fixed. As shown in Figure I.8, the maximum ripple of the current in each cell is equal to *N* times the maximum current ripple in the output. It means that, for example, if we want to parallelize 10 commutation cells and we fix the maximum output ripple to be 1% of the output current, the ripple in each cell will be equal to 100% of the DC current flowing in each cell. High current ripple in each cell leads to high copper losses in the semiconductors and in the inductors and also to high core losses in the inductor.

Reducing the current ripple in each phase is possible by providing a magnetic coupling between the inductors as it will be shown in the next section.

I.1.4 Coupled or Uncoupled Inductors

There is an extra advantage when using parallel converters if we compare them to their counterparts: the reduction of the ripple of internal quantities. It can be achieved by coupling the inductors at the output of such converters. The coupled inductors, also known as InterCell Transformers (ICT), reduce the ripple of the current in each phase of the parallel converter without changing the output current. The main benefit of such a component is the reduction of the high frequency copper and core losses of the magnetic component used to connect all phases, as explained in [24].

To understand how current ripple of each cell is reduced, a 2-cell Buck converter shown in Figure I.9 will be used. Commutation cells are connected to the load by two inductors or only one ICT.

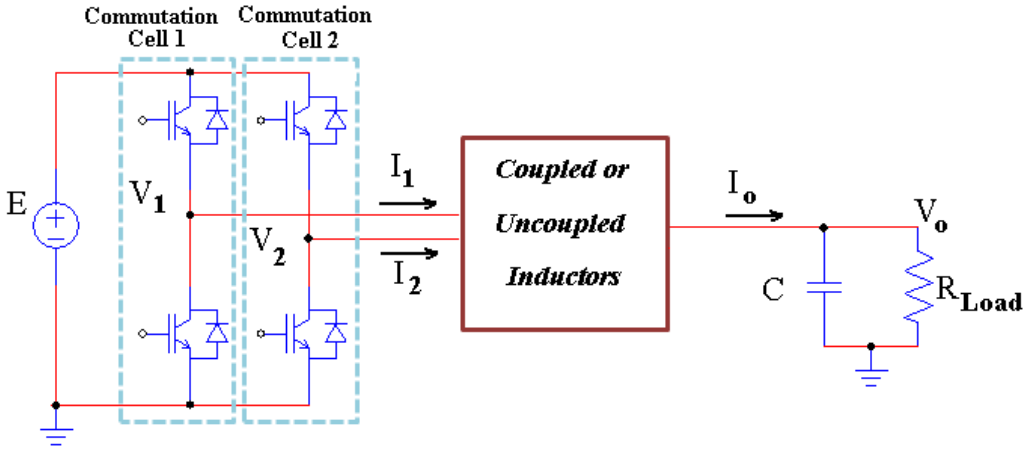
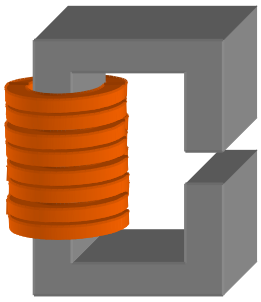


Figure I.9: 2-cell Buck converter using coupled or uncoupled inductors.

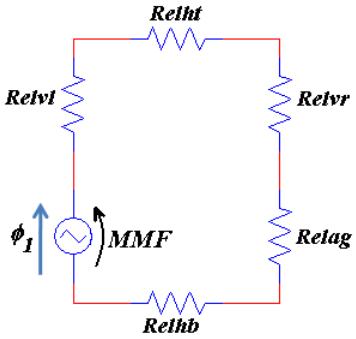
Each inductor is made, for example, of a core having an airgap on the right leg and the winding on the left leg, as shown in Figure I.10a. In Figure I.10b, this inductor is represented by a magnetic circuit where *Relvl* and *Relvr* are the reluctances of the left and right vertical legs respectively and *Relht* and *Relhb* are the reluctances of the top and bottom horizontal legs respectively. *Relag* is the equivalent reluctance of the airgap and ϕ_x is a triangular flux "source" which is induced by the square voltage applied across the terminals of the inductance. This flux source may be calculated as follows:

$$\phi_x(t) = \frac{\int (V_x - V_o)dt}{N_t} \tag{I-7}$$

where N_t is the number of turns of the winding.



a) Airgapped inductor



b) Equivalent magnetic circuit

Figure I.10: Inductor and its magnetic circuit.

Usually the airgap reluctance is much higher than the core reluctances and therefore the magnetomotive force (MMF) which appears across the flux source is practically equal to MMF across the airgap reluctance. This MMF is equal to the flux times the airgap reluctance and the current which flows in the inductor (I_x) is equal to this MMF divided by the number of turns. Thus we conclude that:

$$I_x(t) = \frac{Relag \cdot \int (V_x - V_o)dt}{{N_t}^2} = \frac{\int (V_x - V_o)dt}{L_x} \tag{I-8}$$

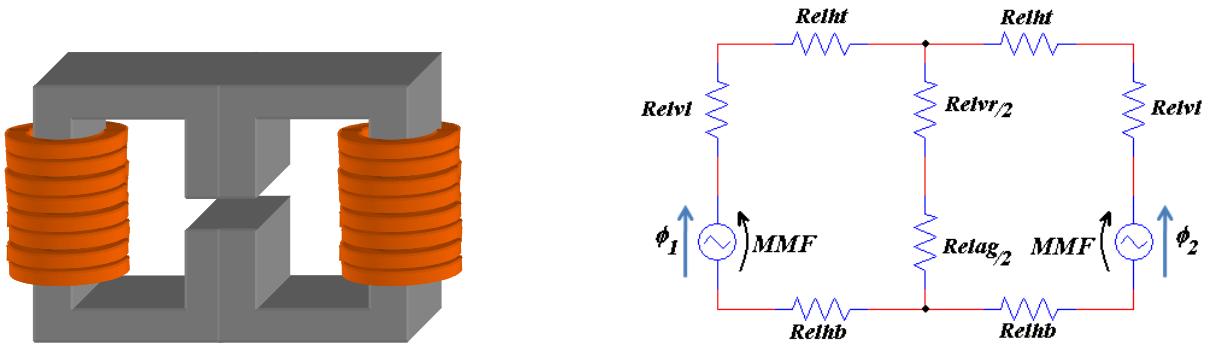
where L_x is the inductance of one of the inductors.

If we want to magnetically couple both inductors, we could join them together as shown in Figure I.11a, which gives the magnetic circuit of Figure I.11b. In this new configuration, the total airgap reluctance is half that of a single inductor. The flux imposed by each commutation cell is summed in the central leg and the MMF across the new airgap reluctance can be calculated as

$$MMF(t) = (\phi_1(t) + \phi_2(t)) \cdot Relag/2 = \frac{Relag \cdot \int (V_1 + V_2)dt}{2 \cdot N_t} \tag{I-9}$$

Since the airgap reluctance is much higher than the core reluctance, this MMF will be the same as those across the two flux sources. It means that the currents in both windings will be practically the same and equal to:

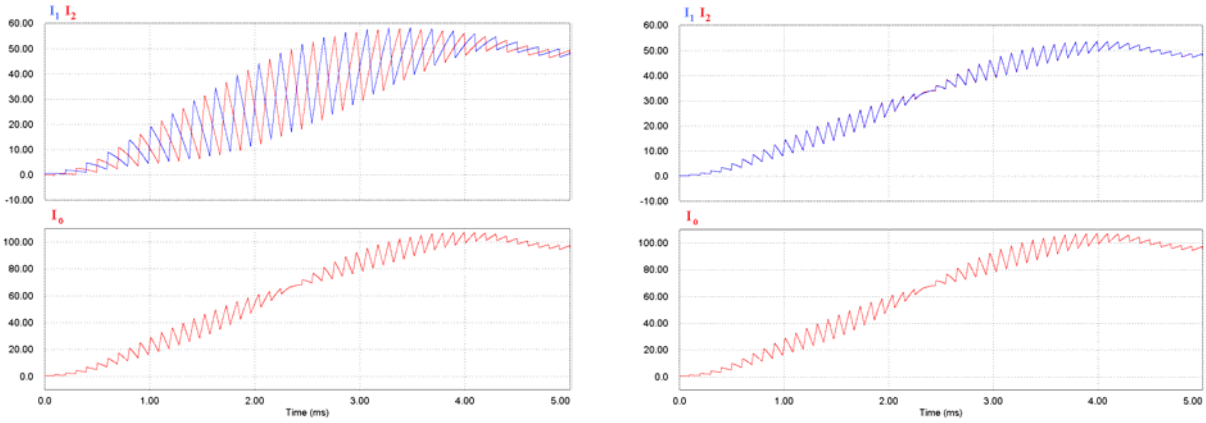
$$I_1(t) \cong I_2(t) \cong \frac{Relag \cdot \int (V_1 - V_2)dt}{2 \cdot {N_t}^2} = \frac{\int (V_1 + V_2)dt}{2 \cdot L_x} \tag{I-10}$$



a) Coupled inductor *b) Equivalent magnetic circuit*

Figure I.11: ICT and its magnetic circuit.

By equation (I-10) we note that each commutation cell current is a result of a 3-level voltage (V_1-V_2) applied to an inductor with twice the inductance of each individual inductor. Thus the maximum current ripple in the coupled inductors is 4 times smaller than the current ripple of individual inductors, and the output current does not change. Since cell currents are both the same when using coupled inductors, they are practically equal to half the output current. This is shown in Figure I.12 which is a result of simulations performed using software PSIM. In these simulations, duty cycle was swept from 0 to 1 and the following parameters were used: E=100V, F_s=5kHz, C=0.5mF, R_{LOAD}=1Ω and total equivalent filtering inductance = 150uH.



a) With regular inductors *b) With coupled inductor*

Figure I.12: Cell and output currents for uncoupled and coupled inductors.

Note that, indeed, the cell current had its maximum value divided by 4 when inductors are coupled. Also each cell current presents no ripple when the ripple in individual inductors was the maximum (when duty cycle is equal to 0.5).

The use of ICTs (or coupled inductors) allows the massive parallelization of commutation cells. Types and topologies of ICTs will be presented in the next section.

I.2 InterCell Transformers

Coupling inductors to reduce current ripple in commutation cells is a subject which has been studied in the past 15 years and from now on we will call this component an InterCell Transformer (ICT) by analogy with the even more ancient InterPhase Transformers. The first ICT presented in this dissertation was the one in Figure I.11a which is a direct association of two gapped inductors. In fact the central leg with an airgap is optional. In particular, when the number of cells increases, less energy is needed for filtering and very soon the leakage flux flowing freely through the surrounding air is enough.

There are several topologies of ICT with two or more phases. They are generally divided into two different types: monolithic or separate.

I.2.1 Monolithic Transformers

One technique of coupling inductors is by putting together all windings in the same magnetic core. This type of ICT is called monolithic transformer and, as presented in [24], may be divided in three different groups:

- Ladder topologies
- Circular topologies
- Circular topologies based on standard cores

Ladder topologies are the structures most found in the literature [15][16][25][26][27]. Examples of ladder topologies are shown in Figure I.13, for a 5-cell converter. In Figure I.13a, the flux produced by each winding is guided through the right-most branch where an airgap controls the filtering inductance of this ICT. In Figure I.13b, it is a symmetrical topology and, as a consequence, the flux produced by each winding flows through the air around the windings. In the latter topology the filtering inductance is more difficult to calculate since it strongly depends on the flux flowing in the air outside the winding window.

Based on the explanation of section I.1.4, and provided that the core reluctances of both topologies of Figure I.13 are much lower than the reluctance of surrounding air and the reluctance of the airgap, the AC magnetic potential across each winding has the same value. Therefore the AC currents in the windings are identical.

a) Ladder with guided flux leg *b) Ladder with distributed leakage flux*

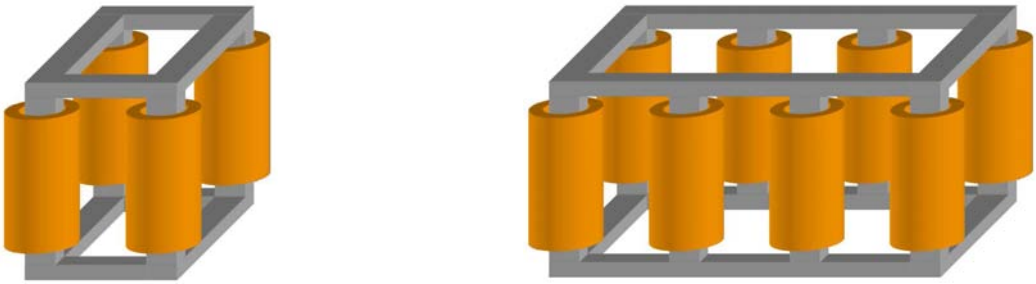
Figure I.13: Ladder InterCell Transformers.

Examples of circular topologies are shown in Figure I.14, for a 7-phase converter. In Figure I.14a, the flux produced by each winding is guided through the central branch where an airgap controls the filtering inductance of this ICT. In Figure I.14b, a symmetrical version of the one in Figure I.14a is shown. In this ICT, which was first described in [28], the flux produced by each winding flows through the air around the windings.

a) Symmetric circular core with central leg *b) Symmetric circular core without central leg*

Figure I.14: Circular InterCell Transformers.

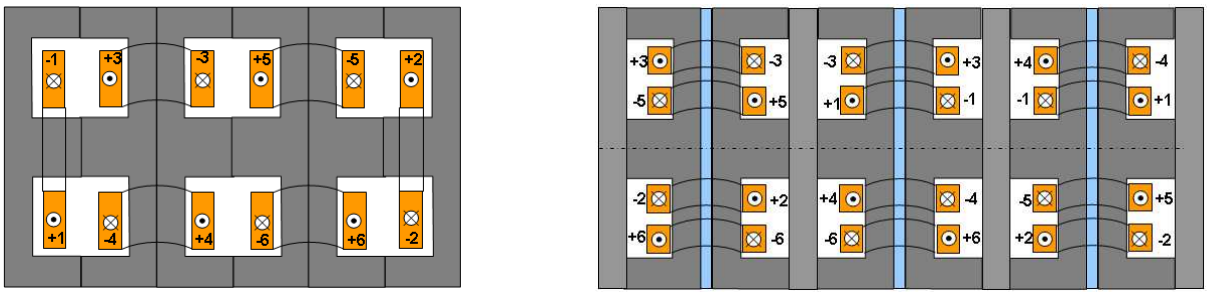
All these topologies of Figure I.14 are very difficult to build. A ring or a disc made of magnetic material (such as ferrite) must be joined to the wound legs which may have round or square cross section. In Figure I.15 we also show circular topologies, but these are more realistic ICTs since they may be made with I-cores. In Figure I.15a we present the "CUBE" or "square ladder", which is used in a 4-cell converter. This ICT is also symmetric but it may be easily assembled by using I-cores. In Figure I.15b, a generalization of the cube for *N* cells (where *N* is an even number greater than 4) is shown. This type of ICT is named here as "rectangular ladder" or "double ladder".



a) Cubic core *b) Double ladder core*

Figure I.15: Double Ladder InterCell Transformers.

Circular topologies based on standard cores were the focus of the work developed by Valentin Costan [24] in our laboratory. Examples of these topologies may be seen in Figure I.16. These two examples are based on ferrite cores of types "E" and "I". In Figure I.16a, each cell is connected to one winding while in Figure I.16b there are two windings per cell. In the latter topology, the magnetizing and leakage fluxes are better distributed in the core thanks to a special winding configuration explained in details in [24][29].



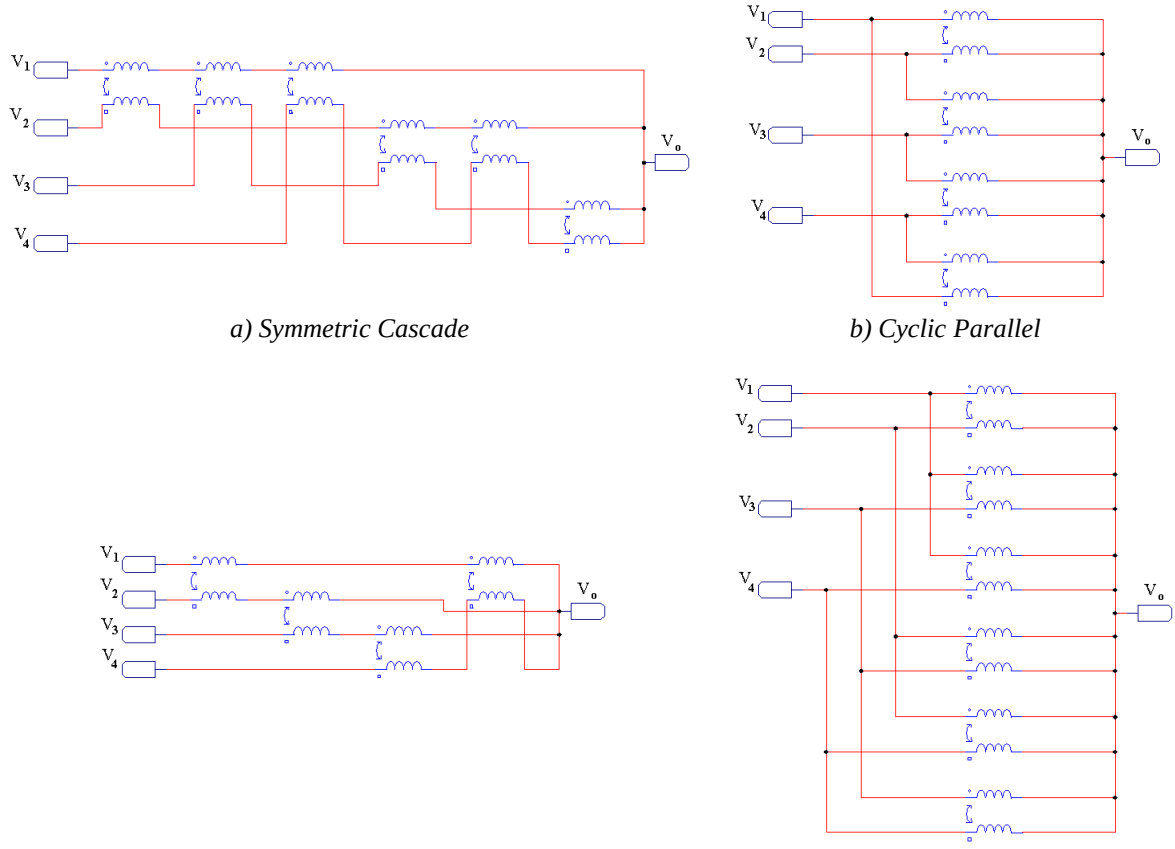
a) One winding per commutation cell *b) Two windings per commutation cell*

Figure I.16: Circular topologies of ICTs based on standard cores.

I.2.2 Separate Transformers

In the Separate ICTs configuration, the system is composed of several two-winding transformers [17][30][31]. We may connect them by different ways. Each topology is composed by several two-winding transformers, each winding connected to a different phase as shown in the different examples of Figure I.17. The number of separate transformers which must be used in an N-phase interleaved converter depends on the adopted topology. The use of separate transformers is specially interesting when developing modular converters.

Each particular topology has its own advantages and disadvantages: Symmetric Cascade, firstly presented in [30], makes use of a high number of ICTs but requires a small inductance in each one in order to efficiently filter the current. Symmetric Parallel may be interesting to be used in high current applications. Cyclic Cascade and Cyclic Parallel needs only *N* ICTs (where *N* is the number of commutation cells of the parallel converter) but their filtering capability is not interesting when the number of phases is high. A deeper comparison between these topologies may be found in [30][32].



a) Symmetric Cascade *b) Cyclic Parallel*

c) Cyclic Cascade *d) Symmetric Parallel*

Figure I.17: 4-phase ICT topologies using separate 2-cell ICTs.

I.2.3 ICT Drawbacks

The use of ICTs allows reducing current ripple in each commutation cell of an interleaved parallel converter. Therefore ICTs are usually lighter and smaller than inductors and that is why they are preferable to connect paralleled commutation cells.

However the design of these magnetic components is not simple as it will be seen in Chapter III. N-cell ICTs have complicate magnetic flux flowing through the core when *N* is greater than 2.

Since two or more windings are wound on the same core, special attention must be taken concerning the saturation of the magnetic material. Depending on the core's permeability, a small difference between currents of different cells can saturate one part of the core. This current imbalance may be caused by a difference of impedance of each commutation cell or also by different voltages provided by each commutation cell due to different dead times and switch characteristic discrepancies.

Another aspect which worries the designers of parallel interleaved converters is the failure of one or more commutation cells. When inductors are used in interleaved converters, a cell presenting a failure may be isolated (by fuses or another switches) and the resulting converter may be reconfigured to operate at a lower power. Each cell will carry an overcurrent which may be taken into account during the design process. However, if the converter is connected by ICTs, simply isolating the faulty cell and reconfiguring the system does not solve the problem. The winding connected to the faulty cell will be opened and consequently the ICT core will saturate. A strategy to solve this problem is presented in [33].

I.3 Applications of InterCell Transformers

The use of ICTs in the industry and their investigation by the scientific community is now growing. Initially their main applications were found to be the parallel connection of commutations cells of Voltage Regulator Modules (VRM) which are mainly composed of Buck converters for high-current low-voltage applications such as voltage sources for microcomputers. Later the use of such magnetic components was extended to different power range and topologies. At this point we list some of the most common applications:

I.3.1 Low Voltage

They are mainly used in VRM for loads requiring currents up to 100A and voltage as low as 1.2V [15][26]. We may find in the market SMD coupled inductors for 2 to 5 phases, as those shown in Figure I.18, which operate at frequencies as high as 2MHz. These magnetic components are mostly used in multi-phase switching regulator for Servers, Desktops, Graphic Card Notebook Computers, Telecommunication Switches and Routers.

a) 2-cell ICTs [34] *b) N- cell ICTs [35]*

Figure I.18: Commercial ICTs used in VRMs.

I.3.2 Not So Low Voltage

Buck converters

Coupled inductors used in buck converters for the range of 30V to 300V are usually found in the literature to show the behavior of the circuit and to validate the theory developed for these magnetic components.

However, authors in [36] develop a set of four coupled inductors to a four-cell interleaved 1kW bi-directional 14V to 42V DC/DC converter for automotive applications.

In [37], the design of a 12-cell ICT is validated by experimental results. The optimization of the switching signals in order to reduce core losses is shown in [6]. In [38], authors compare the use of monolithic and separate ICTs.

Step-up converters

These converters have a more direct application in the industry, especially for the automotive market. For example, two-phase coupled inductors are developed by Honda R&D to integrate eco-friendly electric vehicles [39]. These inductors are to be inserted in a 70V-to-210V boost converter.

Flyback converters are developed for aeronautic applications. For example, a 28V-to-300V 12kW multi-cell interleaved flyback converter was developed by using 8 commutation cells connected through ICTs, as shown in Figure I.19 [7]. One of the main advantages of this topology is the modular form of the single magnetic stage, which makes this solution a good candidate to reach high values of power density.

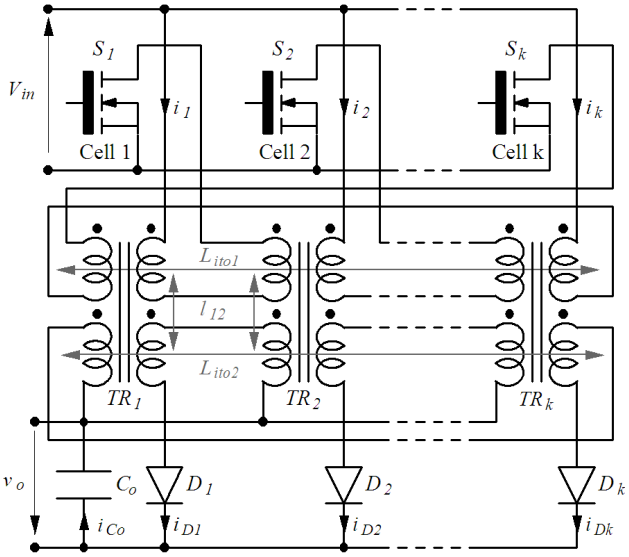


Figure I.19: ICT flyback converter with separate transformers [7].

Inverters

Three-phase AC loads such as synchronous and asynchronous motor may be fed by separate three-phase inverters in order to reduce current ripple and the weight of the whole system, as it will be explained in Chapter V. The parallel connection of the inverters can be made through ICTs.

With the purpose of restraining the loop-current caused by disparity of amplitude and phase of different module's output voltage, authors in [40] develop a parallel inverter system based on coupled inductors.

In [41], authors develop a three-phase bidirectional inverter using a 3-cell ICT to provide significant reduction in harmonic distortion, while in [42] authors focus on a multilevel Discontinuous Space Vector PWM method for a 3-level 3-phase PWM VSI using a 3-phase split-wound coupled inductor.

I.3.3 High Voltage

A 60MW DC/DC converter was designed to supply the main magnets of the Proton-Synchrotron accelerator at the European Organization for Nuclear Research (CERN). This converter makes use of some monolithic three-phase coupled inductors weighting 4 tons each [43]. Thanks to the magnetic coupling, the total weight of the inductors was reduced to almost 1/3 of the uncoupled version previously designed.

I.4 Conclusions

Interleaved multilevel converters are an attractive solution to increase power density and efficiency of power electronic systems. Initially the study of topologies, control techniques, fault aspects, operation and etc., was focused on series multilevel converters. Duality rules show that most of the analysis performed for series multilevel converters may be transposed to parallel multilevel converters.

The parallelization of commutation cells allows the augmentation of the output load while using standard semiconductors. Interleaving the switching signals of these cells reduce the output current ripple and increase the dynamic performance of the converter.

Massive parallelization of commutation cells using regular inductors to connect them is not recommended due to the increase of the current ripple in each cell. To solve this problem, InterCell Transformers may be used since the current of all the cells are magnetically coupled, reducing its amplitude and increasing its frequency.

In this chapter, several ICT topologies for 2 or N-cell topologies were shown as well as some issues associated with their use. We have also presented some applications where these types of transformers are currently being used.

The design and optimization of ICTs will be presented in this dissertation, but next chapter will consider a very important aspect of their design: copper losses at higher frequencies.

Chapter II

Copper Loss Analysis

II.1 Introduction

Copper losses are one of the main aspects of an ICT design since it is usually greater (and maybe much greater) than core losses for various topologies used in different applications. The choice of the conductor material (copper, aluminum or even another material) is very important. Perhaps even more important is the choice of the number of turns and the number of layers of each winding when high frequency effects are taken into account. The position and shape of the conductor's cross-section play an important role in the design as it will be seen in the next section.

High frequency phenomena such as skin and proximity effects are not so simple to model and calculate and since they are an important part on the total copper losses of an ICT, a brief explanation about them will be presented below.

II.1.1 Skin Effect

Figure II.1 shows a round conductor carrying a sinusoidal current. This current induces magnetic flux outside the conductor but also inside it, as represented by the blue loop. Since this flux flows inside a conductive material, by the Lenz Law internal currents will appear so their flux will oppose to the main one. These induced currents are called "Eddy current" and they are represented by the green dashed loops in the figure. Regarding their direction, we can see that they tend to reduce the current density in the central part of the conductor but they increase the current density at the surface. The higher the frequency, the smaller the surface through which the total current will flow. This is shown in Figure II.2, where simulations using Finite Element Method (FEM) software are presented. The FEM software is called FEMM [44].

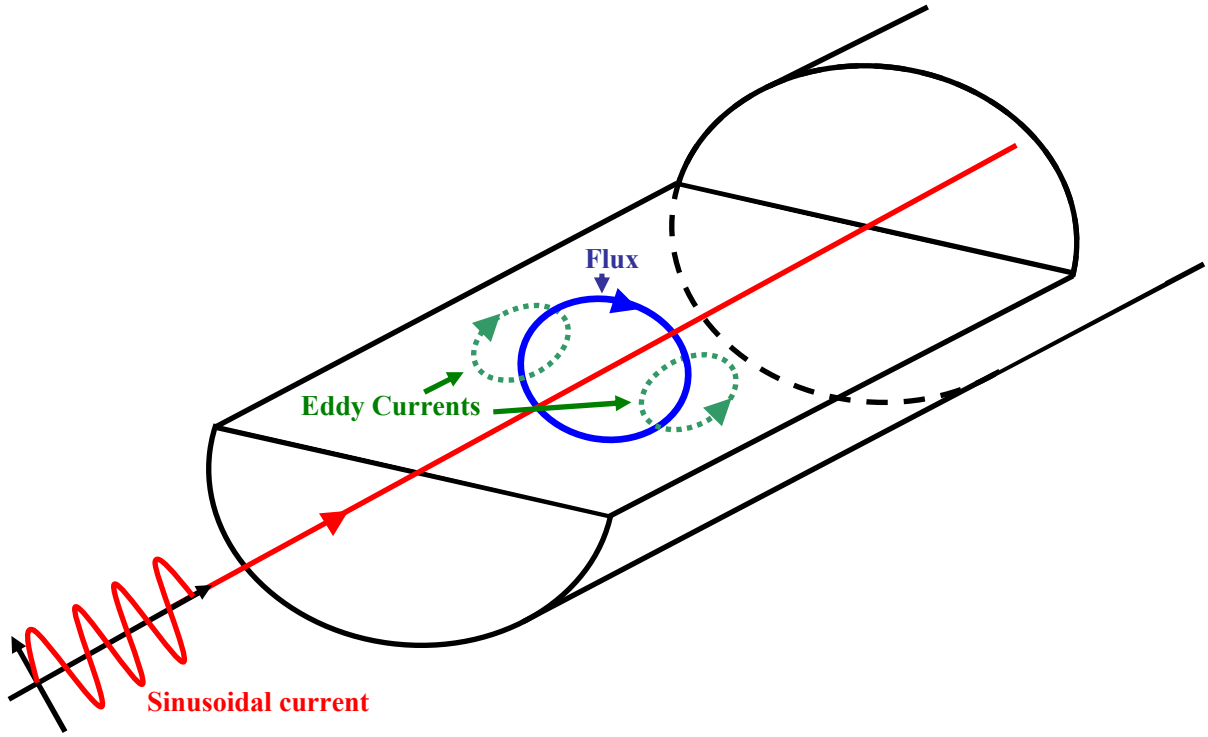
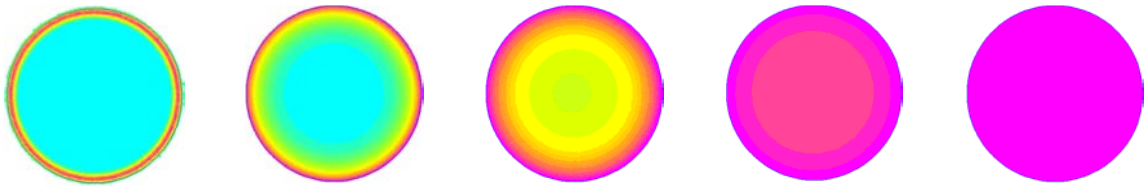


Figure II.1: Skin effect in conductors.



a) Very high frequency *b) High frequency* *c) Medium frequency* *d) Low frequency* *e) DC*

Figure II.2: Current distribution in conductors for different frequencies.

The distance from the surface to where the current density is *1/e* times (where *e* is the natural log base) the surface current density is called skin depth or penetration depth and it can be calculated as:

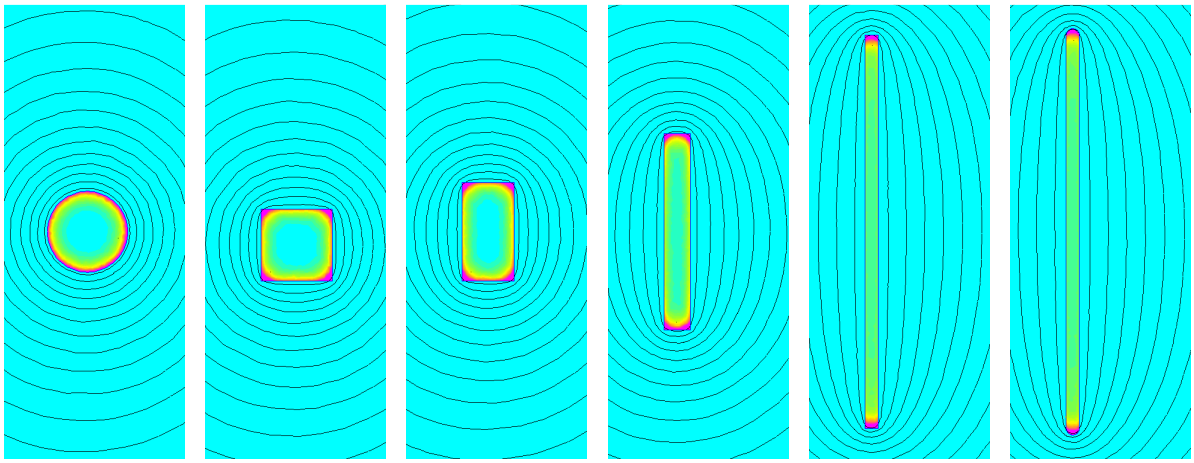
$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{II-1}$$

where $\omega = 2\pi f$ is the current frequency in radians per second, μ is the permeability of the conductor, which is usually equal to the permeability of the free space ($\mu_0 = 4\pi \cdot 10^{-7}$H/m) and σ is the electrical conductivity of the material

This equation may be re-written as

$$\delta = \sqrt{\frac{1}{\pi\mu_0\sigma f}} \tag{II-2}$$

The higher the frequency, the thinner the skin depth and, as a consequence, the higher the equivalent AC resistance (R_{AC}) due to the fact that the current flows through a smaller section. For this reason, conductors with the same cross-section do not have the same AC resistance if they have different shapes, as shown Table II-1, related to the shapes shown in Figure II.3. In the simulation, the current frequency is equal to 10kHz and the conductors are made of copper at 20°C.



a) Round *b) Square* *c) Thick Rectangular* *d) Thin Rectangular* *e) Thinner Rectangular* *f) Thinner Rectangular, round end*

Figure II.3: Skin effect in conductors with different shapes (same current density scale for all shapes).

	Round	Square	Thick rectangle	Thin rectangle	Thinner rectangle	Thinner rectangle, round end	
Corresponding draw in Figure II.3	a	b	c	d	e	f	
Thickness (mm)	Radius	1.643	1.2	0.6	0.3	0.3	
Width (mm)	0.927	1.643	2.25	4.5	9	9	**DC resistance**
Cross Section (mm^2)	2.7	2.7	2.7	2.7	2.7	2.7	2.7
Resistance per unit length (mΩ/mm)	27.37	29.34	28.24	21.79	13.71	13.29	6.39

Table II-1: AC resistance per unit length for different cross-section shapes.

TIP #1: For the same cross-section area, thinner conductors engender fewer losses. Round end engender fewer losses than rectangular ones.

Since AC resistance changes depending on the shape of the conductors, different formulas were developed for conductors with different shapes. Equation (II-3) is related to round conductors [45] while equation (II-4) is related to square-shaped conductors with equal cross-sectional area [46].

$$\frac{R_{AC}}{R_{DC}} = \frac{\gamma}{2} \cdot \frac{ber\gamma \cdot bei'\gamma - bei\gamma \cdot ber'\gamma}{ber'^2\,\gamma + bei'^2\,\gamma} \tag{II-3}$$

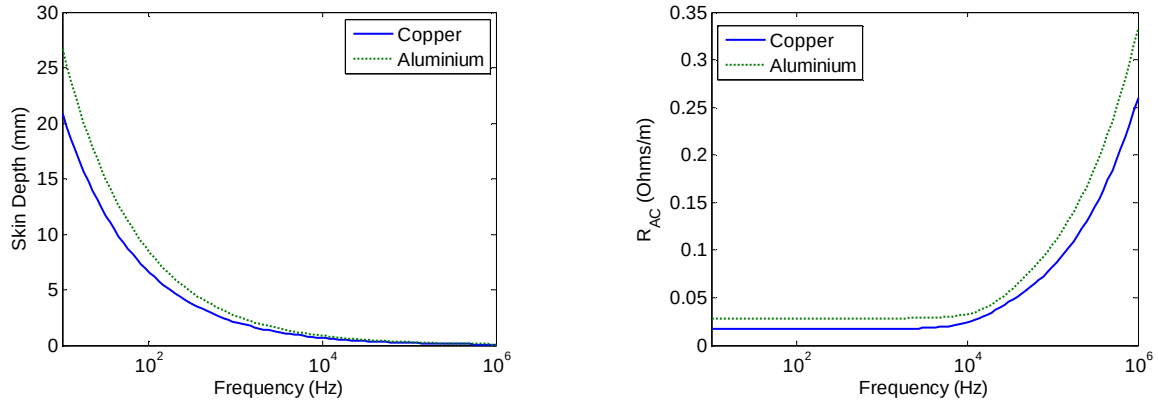
where $\gamma = D \big/ \delta\sqrt{2}$, D is the diameter of the round conductor and *ber* and *bei* are respectively the real and imaginary part of zero order Bessel function (also called Kelvin functions).

$$\frac{R_{AC}}{R_{DC}} = Q\frac{\sinh 2Q + \sin 2Q}{\cosh 2Q - \cos 2Q} \tag{II-4}$$

where $Q = \frac{\sqrt{\pi} \cdot D}{2 \cdot \delta}$.

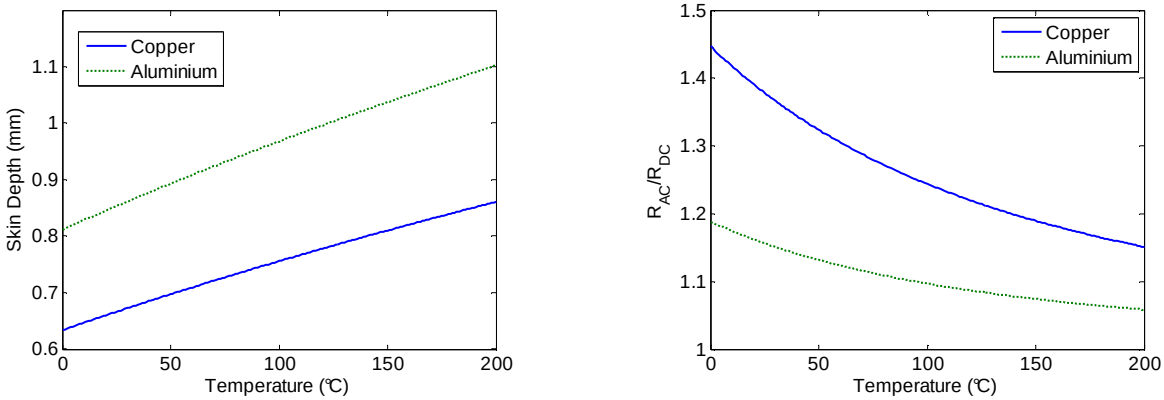
As seen in equation (II-2), skin depth depends on the conductivity (or resistivity) of the conductor. As a consequence, different materials present different behavior concerning the skin depth and AC resistance. This can be seen in Figure II.4 where the variation of the skin depth and resistance with frequency are shown for squared cross-section copper and aluminium conductors at 20°C (conductor width equal to 1mm). Note that although aluminium is much more resistive than copper, there is a region around 20kHz where the resistance difference is reduced.

Conductivity generally varies with the temperature, and as a consequence, skin depth and resistance also depend on the temperature. For example, the variation of AC/DC resistance ratio versus temperature is shown in Figure II.5 for copper and aluminium conductors with the same geometry and cross section. Note that the higher the temperature the lower the AC/DC resistance ratio although resistivity of both materials increase. It means that, when the temperature increases, the resistance of a conductor increases less at higher frequencies than at lower frequencies. This is shown in Figure II.5c where the DC and AC (at 10kHz) resistances are plotted for different temperatures.

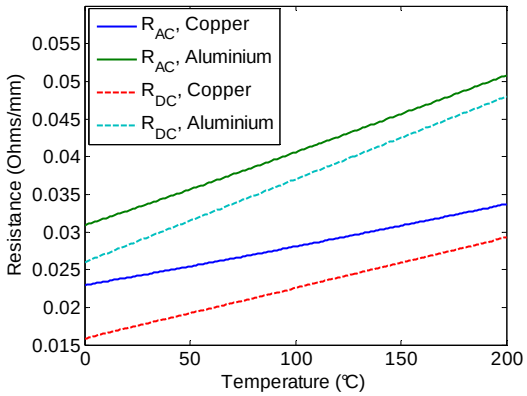


a) Skin depth *b) AC resistance per unit length*

Figure II.4: Skin depth and AC resistance for different materials.



a) Skin depth *b) AC/DC resistance ratio*



c) AC and DC resistance rise

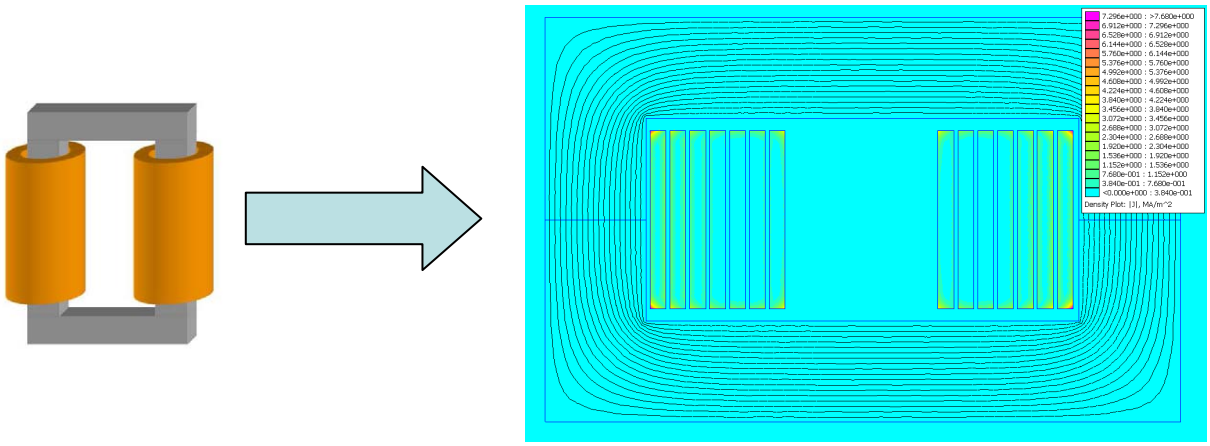
Figure II.5: Skin depth and AC resistance for different temperatures.

II.1.2 Proximity Effect

If one conductor carrying high frequency current is placed close to another conductor, the first will induce eddy current in the second one and vice-versa if the second originally carries high frequency current. This is called the proximity effect and it is typically the case of transformers and inductors.

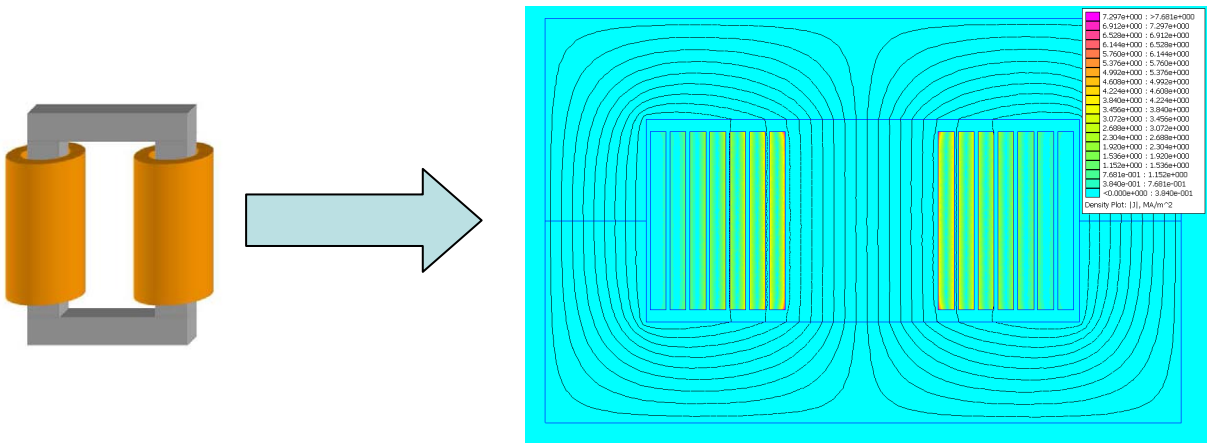
As a general rule, in inductors, the higher the number of turns, the greater this effect and the higher the AC resistance. In transformers, the higher the number of layers (and not the number of turns per layer), the greater the effect and the higher the AC resistance.

To better understand this effect, let's compare both inductors and transformers by regarding the results of FEM simulations. Figure II.6 shows the current density distribution and flux lines of the core window of a hypothetical inductor composed of 2 windings, one wound in the left leg of the core and the other in the right leg. Figure II.7 shows the current density distribution and flux lines of the core window of a hypothetical transformer having the same dimensions and windings as the inductor of Figure II.6, but the left winding is the primary and the right winding is the secondary.



a) UI core inductor *b) Current density*

Figure II.6: Current distribution in conductors inside the core window of an inductor.



a) UI core transformer *b) Current density*

Figure II.7: Current distribution in conductors inside the core window of a transformer.

Note that for the transformer, the flux in the air inside the core window flows vertically and that is why current is concentrated in the left and right side of each conductor. For the inductor, the magnetic field distribution inside the core window is approximately circular and that is why current is concentrated in the outer part of the conductor related to the center of the core window.

Due to the 2 or 3 dimensional nature of the magnetic field in the air surrounding the conductors of an inductor, no analytical formulation of the AC resistance can be found in the literature. On the other hand, AC resistance for transformers is widely studied after the paper written by Dowell.

II.2 High Frequency Copper Losses in Transformers

Dowell, in his famous paper from 1966 [47] solves the problem of calculating the AC resistance of conductors in a transformer for sinusoidal current. He explains the proximity effect mathematically, solving Maxwell's equations for 1D model of transformers. Originally, his work considers rectangular-section conductors, which occupy the entire core window. Later, adjustments are proposed to address the problem of round wires and conductors that do not fill the entire core window height.

In order to present Dowell's formulae let's consider the transformer of Figure II.8. Specifically, we consider only the region inside the core window where both primary and secondary winding are placed, imposing the ampere-turn compensation inside the core window. In this window there are conductors with rectangular cross-section which occupy the entire height of the window. With this geometry and considering high permeability core material, the magnetic field inside the window is strictly vertical as seen in Figure II.7.

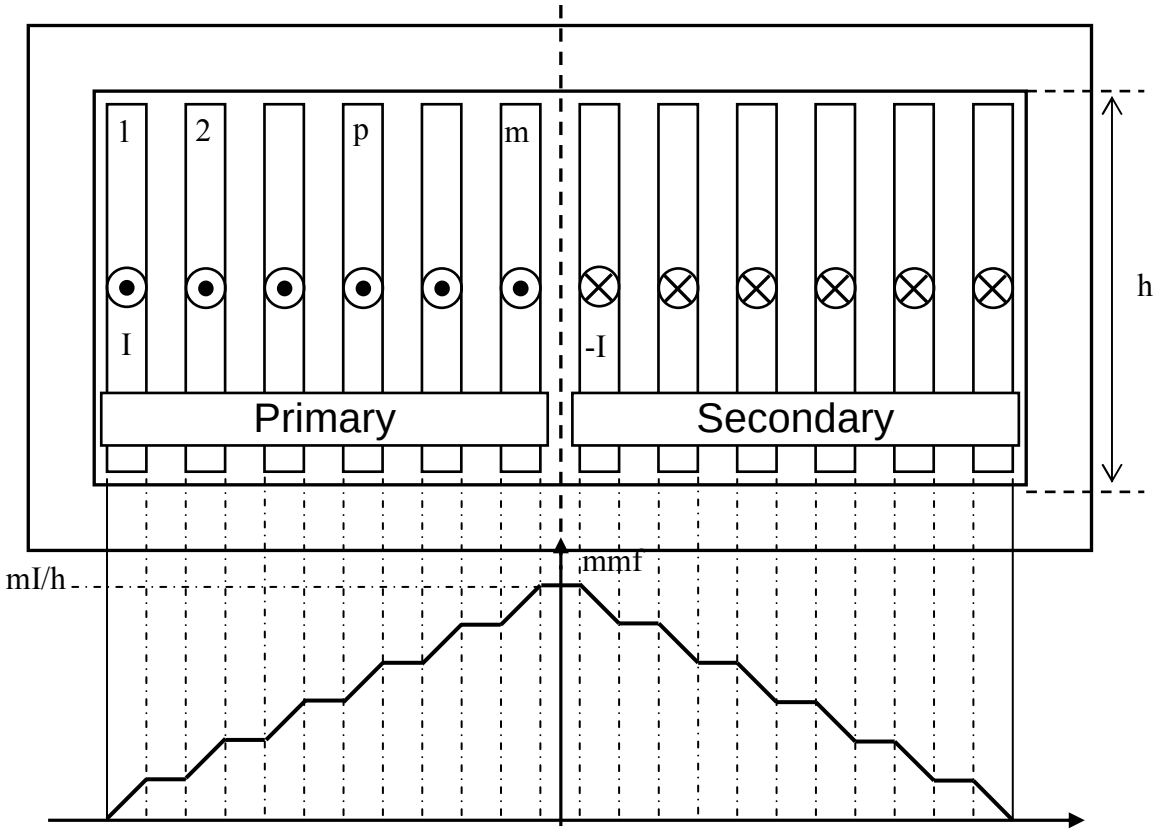


Figure II.8: Transformer parameters used to explain Dowell's formula.

Taking only one winding as reference, if conductors are serially connected and they have the same thickness (d), then the equivalent AC resistance of the winding (R_{AC}) is

calculated by using a resistance ratio Fr (R_{AC}/R_{DC}) which can be derived from the following formula:

$$Fr = \frac{R_{AC}}{R_{DC}} = Q\frac{\sinh 2Q + \sin 2Q}{\cosh 2Q - \cos 2Q} + 2Q\frac{m^2 - 1}{3}\frac{\sinh Q - \sin Q}{\cosh Q + \cos Q} \quad \text{(II-5)}$$

where m is the number of layers of the winding and Q is the ratio between the conductor's thickness and the skin depth, or

$$Q = {}^{d}\!/_{\delta} = d\sqrt{\pi\mu_0\sigma f} \quad \text{(II-6)}$$

According to equations (II-5) and (II-6), the greater the number of layers, the higher the R_{AC}/R_{DC} ratio. Also this ratio increases if the frequency increases. This is shown in Figure II.9.

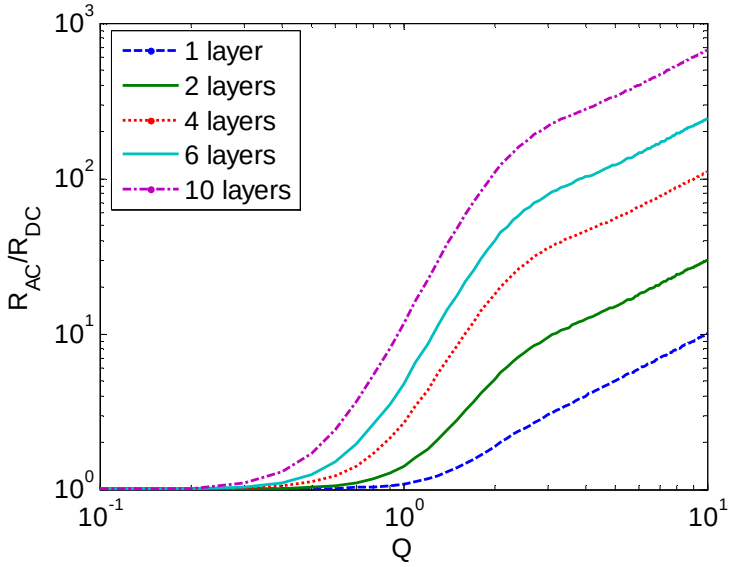


Figure II.9: Variation of the AC resistance with the factor Q.

Dowell's formula is exact for the conditions mentioned above. However, if there is more than one conductor per layer, if the conductors do not fill the entire window height or if the conductor cross-section is not rectangular, the formula is not exact and little modifications must be made in order to approximate the formula to the real value of Fr.

Dowell has proposed a modification of his formula by introducing a coefficient called "porosity factor" η. This porosity factor is the ratio between the total height occupied by all conductors in a window and the window height. He used it to modify the conductivity as shown in equation (II-7). In the literature, this factor is widely used and it was called differently such as "conductor spacing factor" [48], "layer porosity" [49][50] or even "layer copper factor" [51][52]. Figure II.10 explains more in details how it is calculated.

$$\sigma_m = \sigma\eta \qquad \text{and so} \qquad Q = {}^{d}\!/_{\delta} = d\sqrt{\pi\mu_0\sigma\eta f} \quad \text{(II-7)}$$

According to [53], the porosity factor has no theoretical base due to an error in Dowell's original demonstration. However in this paper it is re-interpreted as an empirical correcting factor modeling 2D effects of the fields.

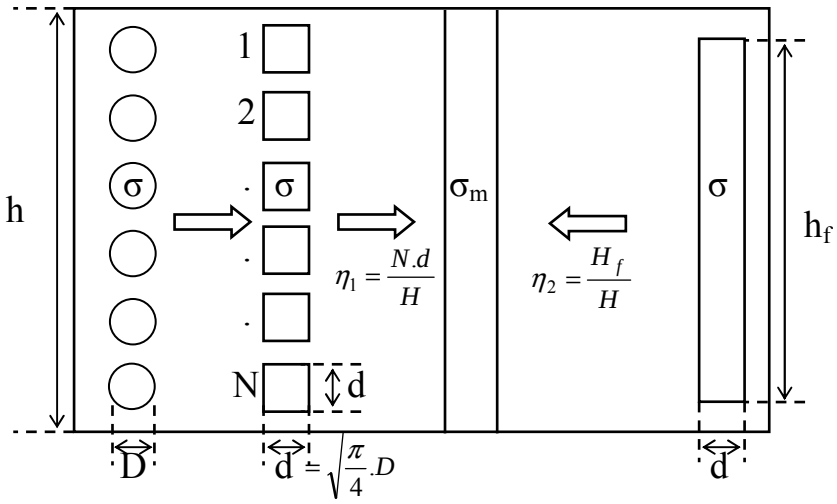
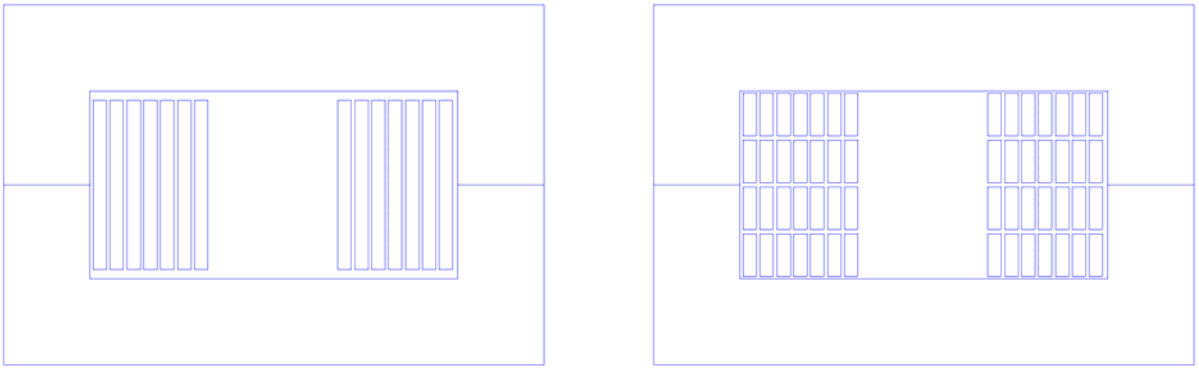


Figure II.10: Porosity factor definition for different conductor shapes.

The porosity factor does not guarantee an exact value of *Fr*. It is an approximation of which validity is examined in [54][55][56][57][58]. To investigate the validity of Dowell's formula, we will compare the values of *Fr* resulting from the analytical calculation and 2D FEM simulation. It is applied for a transformer having 7 layers in two different cases: 1 foil conductor per layer, 4 rectangular conductors per layer. An example of the simulated structures is shown in Figure II.11 and the results are shown in Figure II.12. Note that for low values of *Q*, analytical calculation results are closer to the case where conductors are distributed in one layer. This is because 2D effects are more important when there is only one conductor per layer. If the frequency is increased, factor *Q* also increases and consequently Dowell's equation gives results with important errors when porosity factor is low.

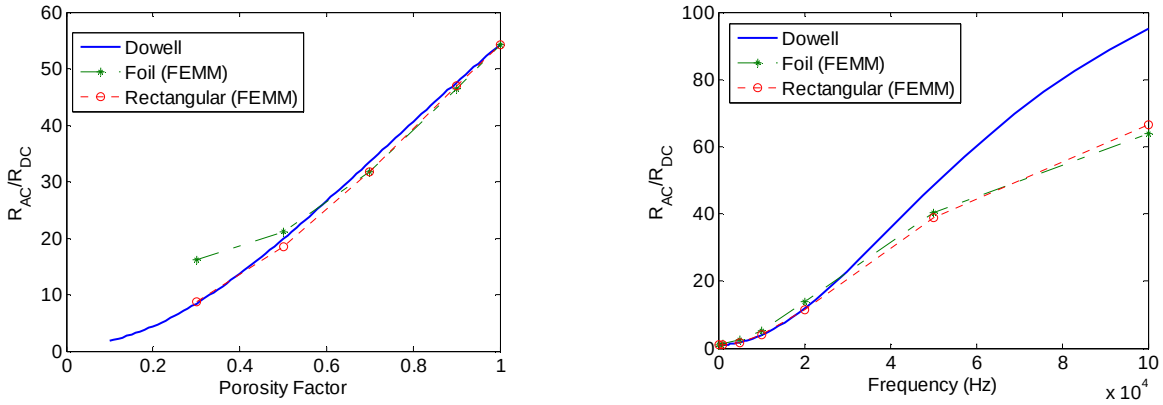


a) 1 foil conductor per layer *b) 4 rectangular conductors per layer*

Figure II.11: Simulated structures.

Besides the porosity factor, the distance between each layer may also change the value of *Fr*. The accuracy of 1D models concerning this fact is discussed in [48][50][51][57][59][60].

Dowell's formula also applies to round conductors as shown in Figure II.10 but its validity is discussed in [46][56][57][58][61][62]. In [3] the author presents an expression to calculate *Fr* for round conductors using the inherent orthogonality between skin effect and proximity effect for the analysis of these transformers and equation (II-3). According to the author, this new formula is more precise than Dowell's approximation and it is in good agreement with experimental results.



a) Different porosity factors, Q=2 *b) Different frequencies, η=0.5*

Figure II.12: Comparison between Dowell's formula and FEM simulation for two structures.

When the porosity factor is low in foil windings, 2D effects are important even when factor Q is close to 1. The effect of resistance rising due to the second dimension of the field inside the core is called in the literature as "edge effects" and it was addressed in [58][63][64][65].

In order to precisely predict copper losses, especially when 2D effects are not negligible, several authors make use of FEM simulation to obtain more precise results [66][67][68]. However each simulation is specific to the design problem and it may not be applicable to other transformers. Besides that, usually FEM softwares are expensive and time-consuming, which may limit a transformer design in an industrial environment.

II.2.1 Separate Losses for Each Layer

Paying attention to Figure II.7, we note that induced current is different for each layer of a transformer. It means that the equivalent AC resistance of each layer is different. Actually Dowell's equation calculates an equivalent AC/DC resistance ratio (Fr) for all layers, which is the average value of the AC/DC resistance ratio of each individual layer (Fr_p).

Formulae to calculate Fr_p for each layer are found in different references [46] [69][70][71]. We show below the expression in terms of the notation adopted in this text:

$$Fr_p = Q \cdot \frac{\left(p^2 + (p-1)^2\right)(\sinh 2Q + \sin 2Q) - 4p(p-1)(\sinh Q \cos Q + \cosh Q \sin Q)}{\cosh 2Q - \cos 2Q} \qquad \text{(II-8)}$$

where p is the position of the layer starting from the one which is close to the minimum energy, as shown in the transformer represented in Figure II.8.

The more internal the layer, the higher its index p. Analyzing equation (II-8), it is clear that more internal layers have higher Fr_p and as a consequence generate higher copper losses. The evolution of Fr_p for each layer is shown in Figure II.13 where we plot it for two different Q factors. Loss difference between layers is enormous and it increases when the number of total layers increases and also when frequency gets higher.

TIP #2: In the winding design, the inner most layers (in the core window) must have the smallest length as possible since they have the highest Fr_p.

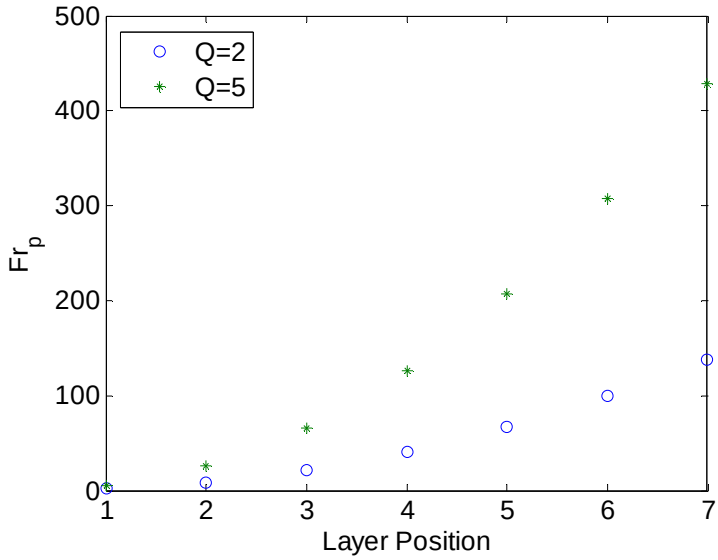


Figure II.13: Evolution of Fr_p for transformers with different total number of layers.

To validate equation (II-8), FEM simulation was performed to calculate Fr_p for one of the ICTs designed in the laboratory which will be presented in the next chapter. The ICT has 14 turns, one in each layer and it is made of foil copper winding. Calculation was made for frequency equal to 300kHz and the simulated structure is shown in Figure II.14. Comparison of the simulated values of Fr_p and those calculated using equation (II-8) is shown in Table II-2 as well as the percentage of copper losses of each turn compared to the total copper losses of the winding. A very good agreement is obtained using equation (II-8) since the difference between simulated and calculated Fr_p is not greater than 2% (except for the first layer which is close to 7%). Note that almost 20% of the total AC copper losses are concentrated in the last layer while only 0.05% is related to the first layer. Fortunately, in this case, the last layer is in contact with the air and heat can be more easily evacuated, which is not the case for all structures.

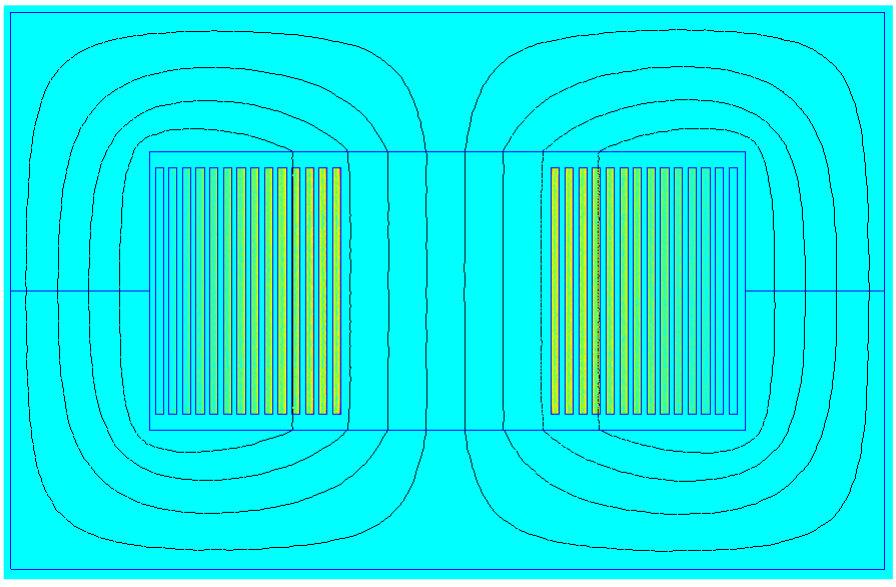


Figure II.14: Simulated ICT (current density plot).

Layer Position (*p*)	FEM Simulation		Equation (II-8)	
	Fr_p	Losses (%)	Fr_p	Losses (%)
1	2.44	0.06	2.29	0.05
2	11.52	0.27	11.37	0.27
3	29.92	0.71	29.54	0.71
4	57.60	1.37	56.78	1.36
5	94.11	2.24	93.11	2.24
6	139.88	3.33	138.53	3.33
7	196.13	4.67	193.02	4.63
8	260.16	6.19	256.60	6.16
9	333.27	7.93	329.26	7.91
10	417.85	9.95	411.00	9.87
11	508.72	12.11	501.82	12.05
12	608.60	14.49	601.73	14.45
13	716.67	17.06	710.72	17.07
14	824.37	19.62	828.79	19.90

Table II-2: Simulated and calculated AC/DC resistance ratios for each layer of a transformer.

II.2.2 Copper Losses for Non-Sinusoidal Current Waveforms

In switch-mode power converters, the waveform of the current flowing through transformers and inductors may assume different shapes when compared to sinusoidal. For example, in forward converters the current waveform is typically pulsed, while in full bridge converters feeding resistive load it is a square waveform. In inductors and ICTs, current has typically a triangular waveform.

In cases where the current is not sinusoidal, Dowell's formula can also be used [48] [72][73], but the amplitude of each harmonic of the current must be found, by means of Fourier series, as shown below:

$$i(t) = I_{dc} + \sum_{n=1}^{\infty} I_n \cos(n\omega t + \theta_n) \tag{II-9}$$

where I_{dc} is the continuous value of the current, I_n is the amplitude of the nth harmonic with corresponding phase θ_n.

Copper losses in the transformer are given as the sum of the losses of each harmonic:

$$P_{cu} = R_{dc}\left({I_{dc}}^2 + \sum_{n=1}^{\infty} Fr_n \frac{{I_n}^2}{2} \right) \tag{II-10}$$

where Fr_n is the ratio between the AC resistance of the nth harmonic and the DC resistance, and is given by the equation below:

$$Fr_n = \sqrt{n}Q \frac{\sinh 2\sqrt{n}Q + \sin 2\sqrt{n}Q}{\cosh 2\sqrt{n}Q - \cos 2\sqrt{n}Q} + 2\sqrt{n}Q \frac{m^2 - 1}{3} \frac{\sinh \sqrt{n}Q - \sin \sqrt{n}Q}{\cosh \sqrt{n}Q + \cos \sqrt{n}Q} \tag{II-11}$$

where Q is the ratio between the conductor's thickness and the skin depth related to the fundamental frequency.

Developing equation (II-10) we may define an equivalent AC/DC resistance ratio (Fr_{eq}) which is specific for a given waveform:

$$Fr_{eq} = \sum_{n=1}^{\infty} Fr_n . a_n{}^2 \quad \text{having} \quad a_n = \frac{I_n}{\sqrt{2} \cdot I_{RMS}} \tag{II-12}$$

where I_{RMS} is the RMS value of the high frequency current waveform which can be used to calculate copper losses as shown below:

$$P_{cu} = R_{dc}\left(I_{dc}{}^2 + Fr_{eq} . I_{RMS}{}^2\right) \tag{II-13}$$

Figure II.15 shows the equivalent AC/DC resistance ratio for different waveforms. Square waveform has higher Fr_{eq} than the others since it has higher harmonic content. It is not a general rule but usually waveforms with higher RMS/peak ratio have also higher AC/DC resistance ratio.

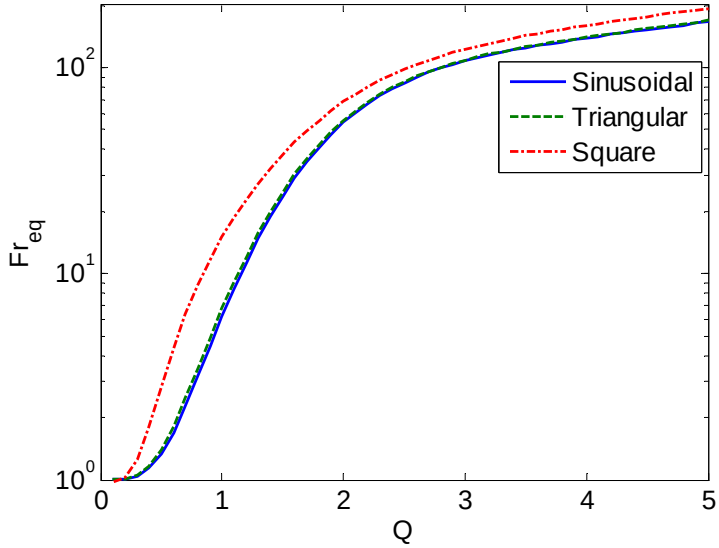


Figure II.15: Fr_{eq} for different current waveforms.

A formula to calculate the optimum foil or layer thickness in multilayer transformers is presented in [74]. This formula is developed by using the RMS value of the current passing through the winding conductors and from its derivative. Also, the equations may be applied to any periodic current waveform, avoiding the need of Fourier analysis, which is computationally more complicated.

Discussion about the use of single-layer or multi-layer winding is also made in [75]. The authors analyze these two options by considering some non-sinusoidal current waveforms and small thickness-to-skin-depth ratio. In their analyses, authors also make use of concepts as optimum layer thickness and optimum number of layers. In [76], the same analysis is performed in the presence of DC current.

II.2.3 Extra Copper Losses

Analytical equations showed above are all valid for conductors inside transformer's core window in the case where magnetic flux flows in only 1 dimension inside the window. When this is not the case, 2D or 3D effects are usually important and no general analytical calculation of AC resistance is found in the literature.

Two cases will be investigated: copper losses on the part of the winding which is not inside the core window and extra copper losses due to airgaps.

II.2.3.1 Copper Losses for the Winding Outside the Core Window

Several transformers have at least a small part of the winding placed outside the core window. This is the case of the ICTs developed in our research group, as it can be seen in Figure II.16 where a monolithic 12-cell ICT is shown. Actually, only transformers made using pot cores have all the winding entirely surrounded by magnetic material.

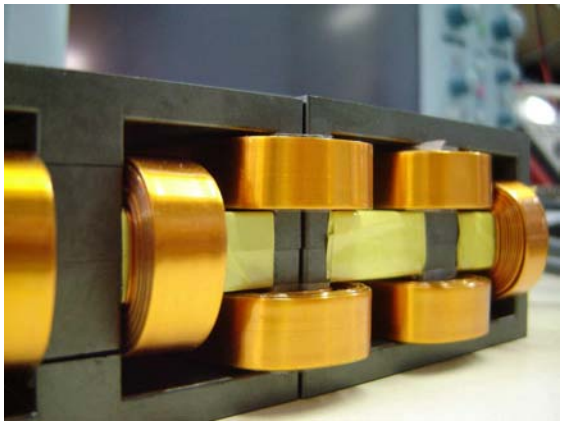
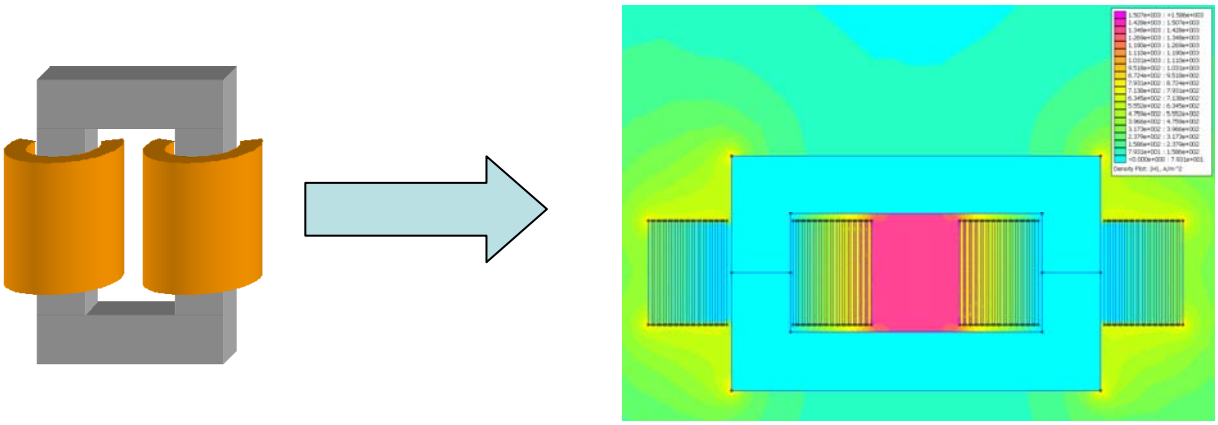


Figure II.16: End-turns of monolithic ICT developed in the laboratory.

Depending on the structure of the core, the greatest part of the core is outside the core window, such as the ones made with UI-cores. Most transformers made with planar cores have winding end-turns which are not so large and usually designers consider that the AC resistance per unit length of this part of the winding is the same as the one inside the core window which implicitly means that Dowell's equation is used everywhere.

However we will show below that this approximation may not be a good option in some common cases. For this, let's consider the transformer of Figure II.17a composed of two windings, one in each leg of the UI-core. 2D FEM simulation of this transformer is shown in Figure II.17b.



a) UI core transformer *b) FEM simulation using 14 layers*

Figure II.17: Transformer and FEM simulation (magnetic field distribution).

We will also use the same structure but in another configuration. Instead of 14 turns in 14 layers, we will simulate conductors in the "horizontal position", i.e. 1 layer with 18 turns, in this case. Simulations are performed for these two configurations, at two different frequencies: 10kHz and 1MHz. Figure II.18 shows the current density plot of the simulations performed for the two configurations. Only the winding at the right leg is shown along with the copper losses (P_{cu}) calculated for each part of the winding.

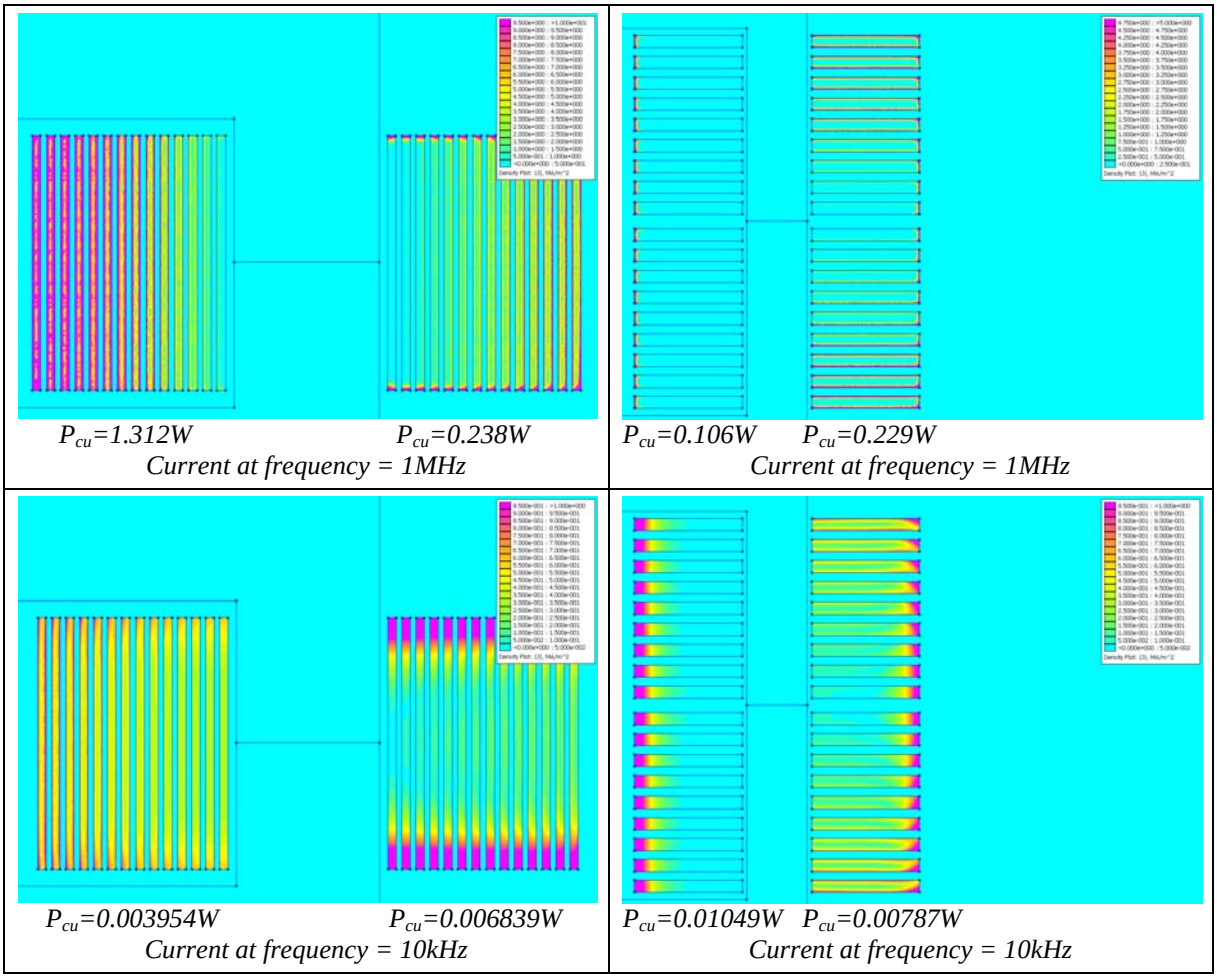


Figure II.18: Copper losses inside and outside the core window, for different configurations and frequencies (current density plot).

The absolute value of copper losses is not important in this comparison. What is interesting to note are the relative values between different configurations and frequencies. Obviously, the higher the frequency, the higher the losses for the same configuration.

Note that outside the window, proximity effect is important even in the vertical direction when conductors are in the horizontal position.

When conductors are in the vertical position, losses are greater inside than outside the core window for higher frequencies. For lower frequencies it is the contrary; higher losses are generated outside.

When conductors are in the horizontal position, it is the contrary. Lower losses occur outside for lower frequency while losses for higher frequencies are greater in the part of the winding outside the core window.

These observations show that designers should not use Dowell's formula for all configurations and frequencies. By using this formula, overestimation (or even worst, underestimation) of the total copper losses can lead to important errors when designing ICTs and transformers.

II.2.3.2 Copper Losses due to Airgaps

It is well known that airgaps increase high frequency copper losses in inductors, especially when conductors are close to them. Figure II.19 shows an example of the current induction in the region close to the airgap of a transformer. To give an idea of how much extra copper loss are generated by airgaps, a transformer and an inductor with the same structure, having 6 turns in each leg, will be simulated for different airgap lengths placed in the middle of the wound legs.

Usually transformers do not have airgaps but ICTs may have, especially if more robustness against current imbalance is desired. Results of all simulations are shown in Figure II.20. Note in Figure II.20a that in an inductor, the presence of airgap significantly increases the AC resistance while in the simulated transformer it decreases. It can be explained observing that in a transformer, the inclusion of an airgap reduces the main leakage flux inside the core window. AC resistance reduction caused by this fact is greater than AC resistance increase due to the energy concentration around the airgap. Figure II.20b shows that this AC resistance reduction in transformers occurs for all the frequencies.

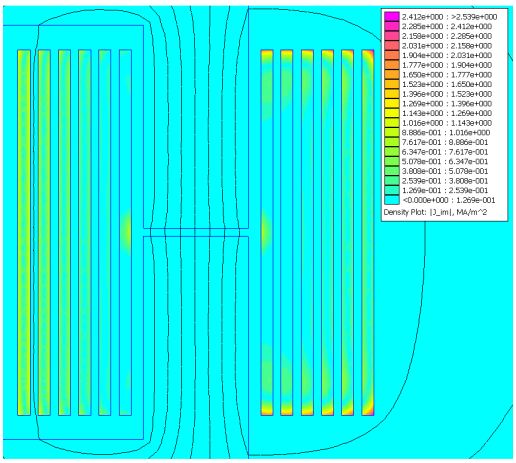
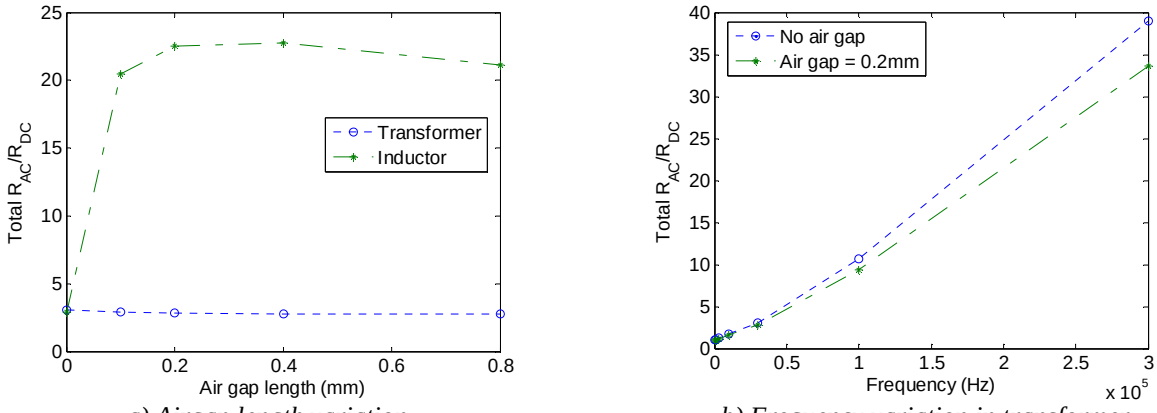


Figure II.19: High frequency current induction close to airgap (current density distribution).



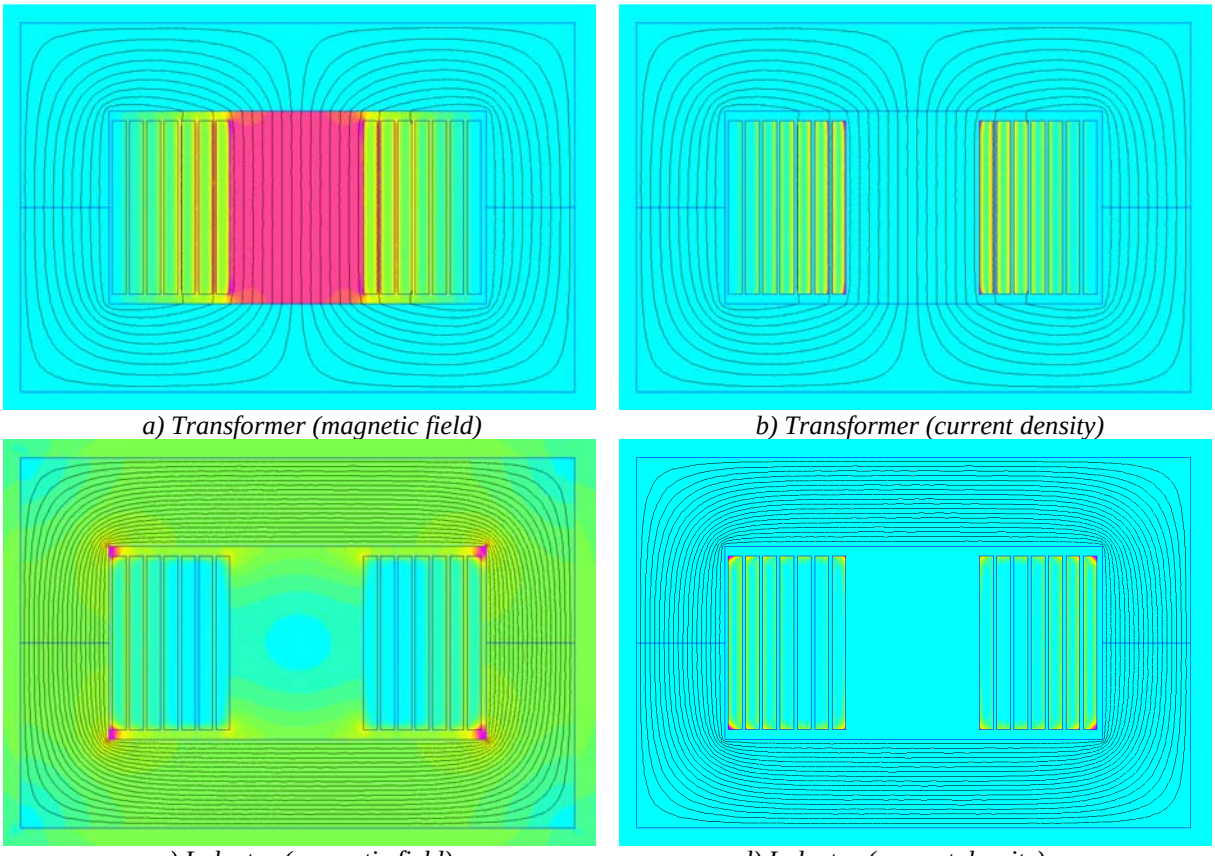
a) Airgap length variation *b) Frequency variation in transformer*

Figure II.20: Influence of airgap in the AC/DC resistance ratio.

II.2.4 Copper Losses in Inductors

Some designers use directly Dowell's equation to predict copper losses in inductors. This is not a good approach since the field inside the core window does not have a one dimensional characteristic. Also inductors usually have airgaps which increase copper losses, especially at high frequencies.

In order to show the differences between inductor and transformer, the structure of Figure II.11a will be simulated as a transformer and also as an inductor. In the transformer mode, currents of different windings have opposite directions inside the core window while they have the same direction for the case of an inductor. The magnetic field and current distribution inside the core window for the transformer and inductor cases can be seen in Figure II.21, for a simulation at a relatively high frequency. Note that in the transformer, the energy is concentrated in the air between the windings while in an inductor it is mainly in the material surrounding the windings. It is clear that the greater the energy in the region close to the conductors, the higher the current density in this conductor. Thus we note that, for the transformer, higher copper losses are observed in the conductors in the center of the window while in the inductor it happens in the conductors close to the vertical legs of the core. Since they have the same scale, higher copper losses are observed for the transformer than for the inductor in the frequency we have simulated. But this is not the case for all frequency as it is shown in Figure II.22 where the evolution of *Fr* with the frequency for this transformer and this inductor is presented.



a) Transformer (magnetic field) *b) Transformer (current density)*

c) Inductor (magnetic field) *d) Inductor (current density)*

Figure II.21: Current density and magnetic field distribution for transformer and inductor (same color scale for inductor and transformer).

For lower frequencies, since the conductors are tall but thin, skin effect is important in this inductor but it is moderate in this transformer (given that the field is mainly vertical in this transformer's window). However, when the frequency is high, proximity effect is much more important in the transformer than in the inductor.

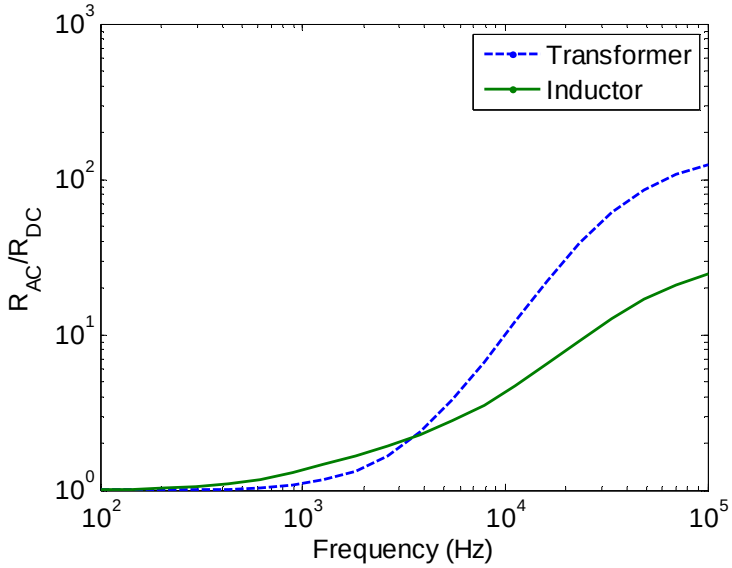


Figure II.22: Evolution of the AC/DC resistance ratio in transformer and inductor.

II.2.5 Trying to Reduce Copper Losses

With the purpose of trying to reduce copper losses in ICTs, some ideas will be discussed below.

II.2.5.1 Inserting Magnetic Material Close to the End-Turn

One idea is to extend the magnetic core so the part of the winding outside the core window is almost surrounded by a magnetic material. This is shown in Figure II.23 for the two structures simulated in Figure II.18, having conductors in the horizontal and vertical position. As done before, Figure II.23 also shows copper losses for both structures using the same frequencies: 10kHz and 1MHz. Comparing this figure with Figure II.18, no difference in the copper losses is observed for the part of the winding inside the core. However, concerning the part of the winding outside the core (which is now close to the inserted magnetic material), copper losses are reduced for the case of horizontal conductors in higher frequencies and also for the case of vertical conductors in lower frequencies. For the other two cases, the insertion of the magnetic material increases copper losses. Therefore the designer may only extend the magnetic material when skin and proximity effects are important in the direction where the material will be inserted (in the example above, it is the vertical direction).

In an ICT design, extending the core material may not be a good idea since core losses and the total weight will increase. However, the leakage inductance increases, thus reducing the current ripple. This may reduce high frequency copper losses. We can see that it is not so easy to evaluate if extending the core is a good idea to an ICT design.

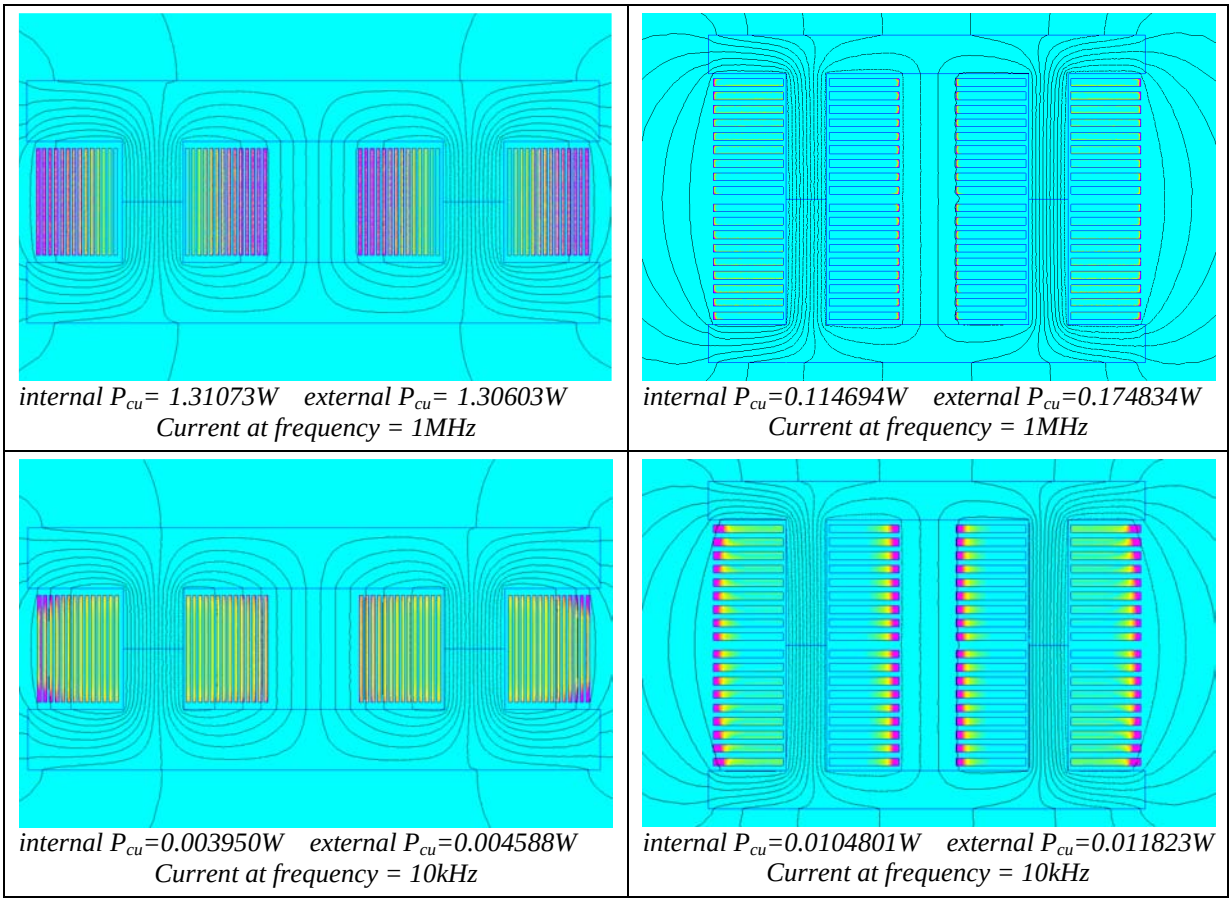


Figure II.23: Copper losses inside and outside the core window, with extension of the magnetic material of the core (current density plot).

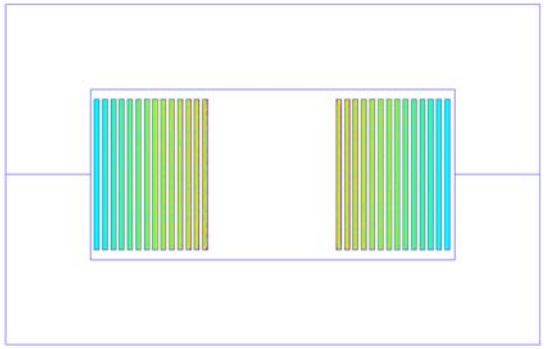
II.2.5.2 Inserting Magnetic Material Inside the Core Window

Inserting a magnetic material inside the core window in the space between two windings will certainly increase the leakage inductance of the transformer or ICT, as can be seen in Table II-3. However, it is not clear that it reduces copper losses.

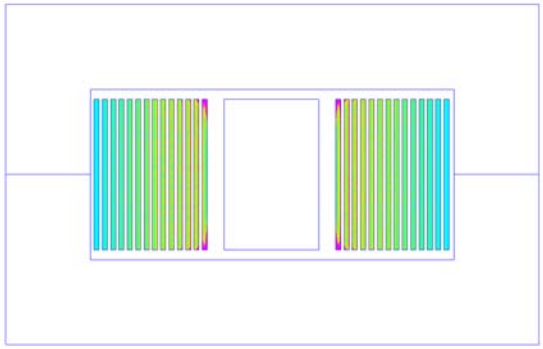
Six configurations will be used in the comparison as shown in Figure II.24. In some of them, materials with different relative permeabilities (μ_r) will be used in the central leg. Simulations of these ICTs are performed in order to calculate total copper losses in the part of the winding inside the core window for a given frequency and current. Regarding the results shown in Table II-3, some conclusions can be made:

1. Inserting one leg having large airgap increases copper losses;
2. Significant copper loss reduction is only observed when the leg really touches both upper and lower core legs;
3. Strong copper loss reduction happens when the material in the central leg has high permeability. However, in this case the component turns into 2 different inductors and the coupling characteristic of ICTs is lost.

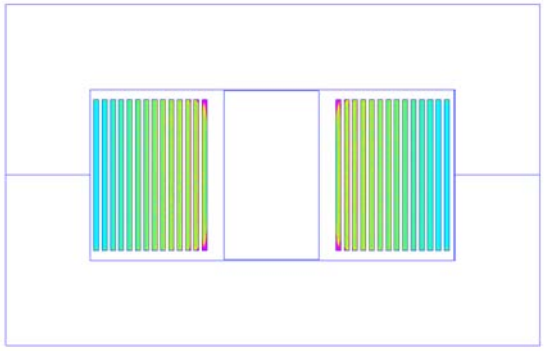
As a final conclusion, inserting magnetic material inside the core window is not a good idea to reduce high frequency copper losses in the windings although it may be a good option to increase leakage inductance. However, the insertion of a central leg also increases the DC or low frequency flux in the core and depending on the design, the core and the central leg can saturate, especially if the inserted central leg has a reduced cross section.



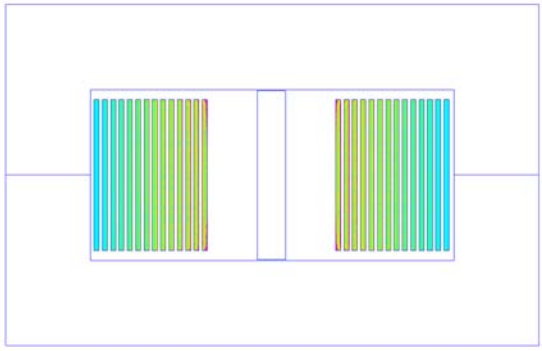
a) No magnetic leg



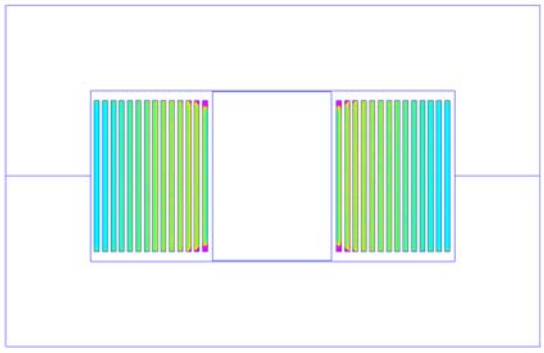
b) Small magnetic leg



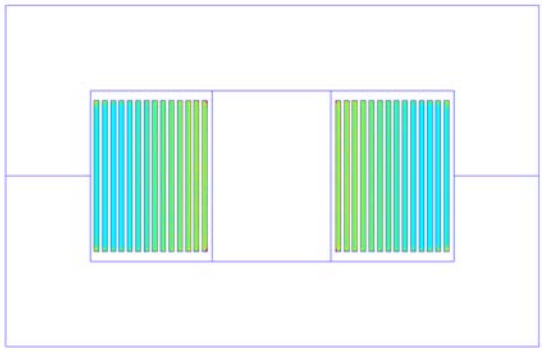
c) Tall magnetic leg



d) Tall and thin magnetic leg



e) Tall and large magnetic leg



f) Large magnetic leg touching the core

Figure II.24: Insertion of different magnetic legs in the transformer winding window.

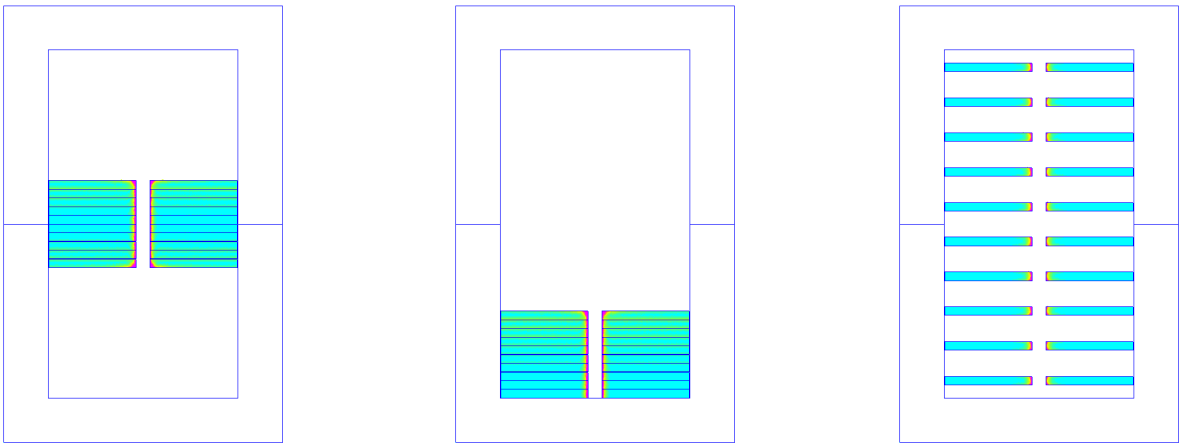
Configuration	Copper Losses (W)	Leakage Inductance (µH)
No magnetic leg	0.67069	6.56
Small magnetic leg, μ_r = 500	0.74175	36.3
Tall magnetic leg, μ_r = 500	0.60768	275
Tall and thin magnetic leg, μ_r = 500	0.62934	98.1
Tall and large magnetic leg, μ_r = 500	0.63038	333
Tall and large magnetic leg, μ_r = 50	0.60092	141
Tall and large magnetic leg, μ_r = 1800	0.65702	374
Large magnetic leg touching the core, μ_r = 1800	0.09643	2196
Large magnetic leg touching the core, μ_r = 50	0.58245	202

Table II-3: Simulated copper losses for different configurations.

II.2.5.3 Changing the Winding Place and Porosity Factor Inside the Core Window

Another manner to reduce high frequency copper losses is by changing the porosity factor. According to equations (II-5) and (II-7) and Figure II.12, the smaller is the porosity factor, the lower copper losses are. Thus the core window height could be increased in order to reduce copper losses. In fact, this will have the desired result although core losses and weight of the transformer will be increased.

Supposing that the core has fixed window height and width, we could investigate how factor *Fr* changes with the position. This will be done by considering windings with 1 layer and 10 turns. It will be placed in 3 different positions: concentrated in the center of the window, in the bottom, and spread in the core window. These configurations are shown in Figure II.25 a, b and c, respectively.



a) Centered in the window *b) Close to the bottom* *c) Spread in the window*

Figure II.25: Current density of a 10-turn transformer when conductors are placed in different locations inside the core window.

In the three cases, porosity factor is equal to 0.25 and according to Dowell's equation all the configurations should have the same *Fr*. This is not the real case as it can be seen in Table II-4 where the results of simulations are shown for a fixed frequency and different porosity factor.

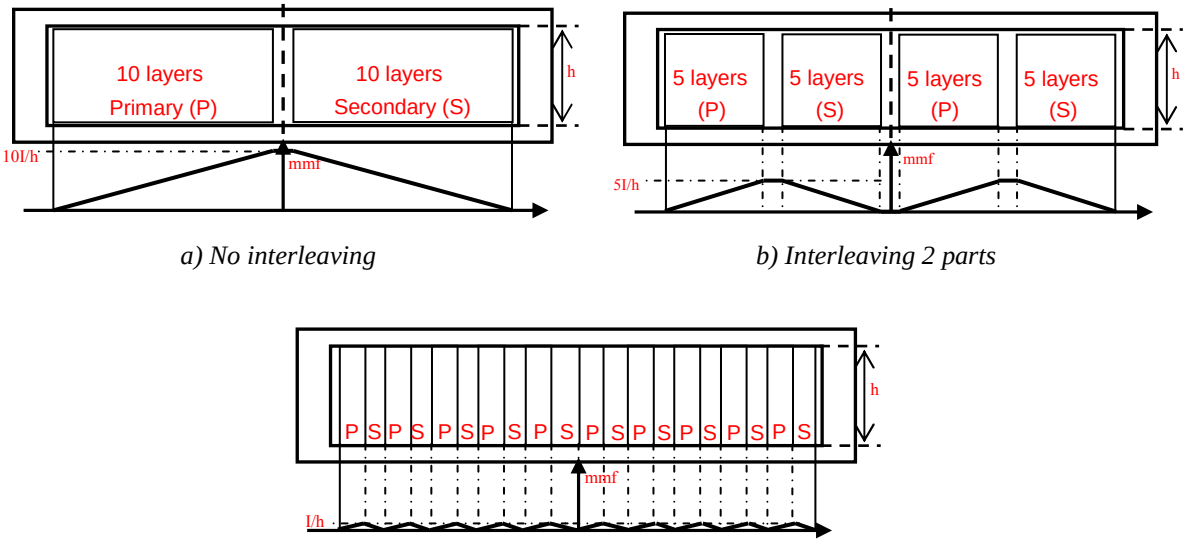
Indeed copper losses are reduced when porosity factor gets smaller. Regarding the position of conductors, higher losses are observed when windings are concentrated close to the core. The best option is to equally space all the turns inside the window. Note that by doing so, copper losses (and also leakage inductance) are reduced to almost half of what it is when winding is concentrated somewhere, for this specific example.

Filling Factor (%)	Position	Fr
98	Centered	47.71
83	Centered	44.25
50	Centered	37.96
25	Centered	35.59
25	Bottom	42.87
25	Spread	19.18

Table II-4: Simulated copper losses for different conductors' location and filling factor.

II.2.5.4 Interleaving the Windings

Interleaving windings is a well known technique to reduce leakage inductance and high frequency copper losses in transformers. By breaking up the windings into smaller sections and interleaving them, the energy inside the window is reduced as shown in Figure II.26 where a transformer with windings having 10 layers are interleaved.



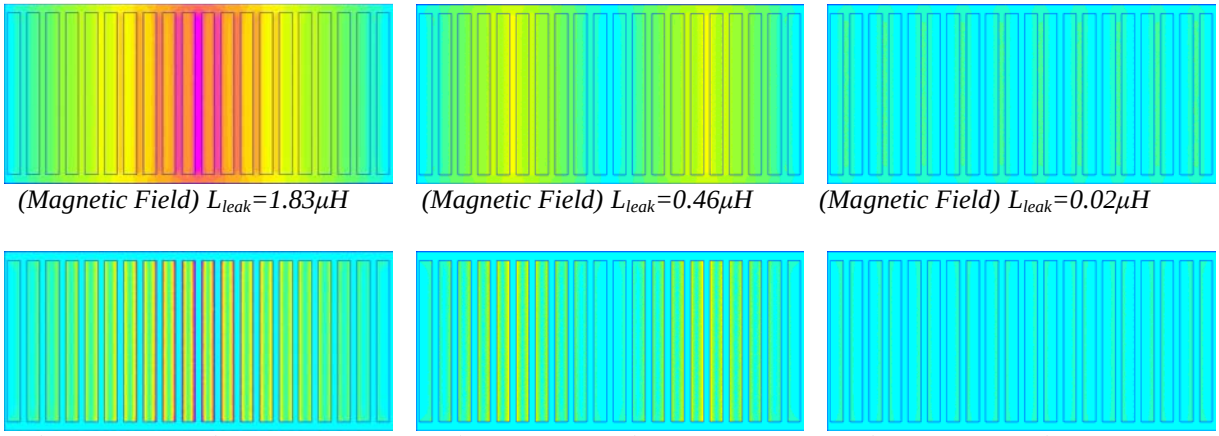
a) No interleaving *b) Interleaving 2 parts*

c) Interleaving all conductors

Figure II.26: Energy reduction by interleaving windings.

Figure II.27 shows the magnetic field and the current density plot of simulations of transformers having windings composed by 10 layers each. In the first configuration there is no interleaving. In the second configuration each winding is divided into 2 parts having 5 layers each. And in the last configuration all the layers are interleaved. Conductors have thickness equal to 0.8mm and height equal to 10mm. Dowell's filling factor is equal to 0.9 and simulation frequency is equal to 100kHz.

The evolution of *Fr* and the leakage inductance with the frequency for these configurations is shown in Figure II.28. Note that both the leakage inductance and resistance are strongly reduced by interleaving windings, especially for higher frequencies.

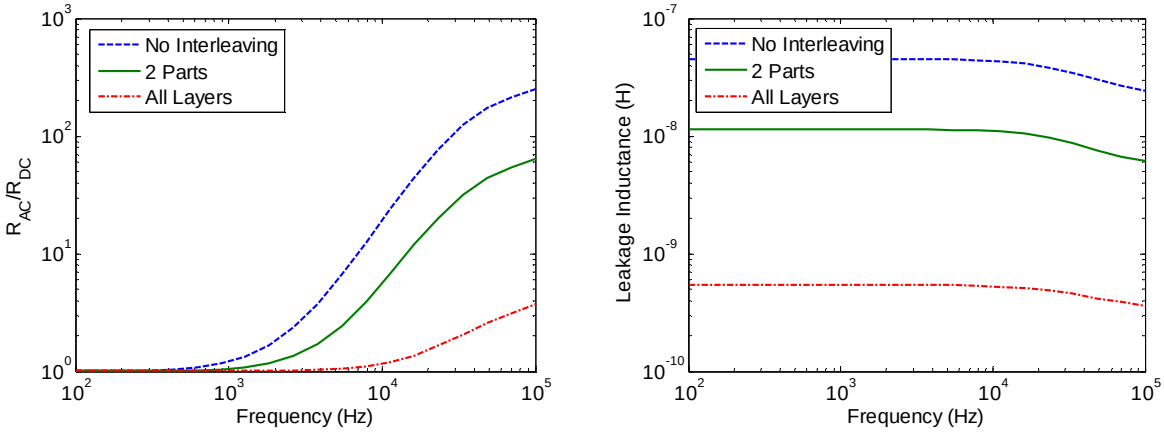


(Magnetic Field) L_{leak}*=1.83µH* *(Magnetic Field)* L_{leak}*=0.46µH* *(Magnetic Field)* L_{leak}*=0.02µH*

(Current Density) Fr=4690 *(Current Density) Fr=1208* *(Current Density) Fr=89.5*

a) No interleaving *b) Interleaving 2 parts* *c) Interleaving all conductors*

Figure II.27: Simulation of interleaved windings.



a) AC/DC resistance ratio *b) Leakage inductance*

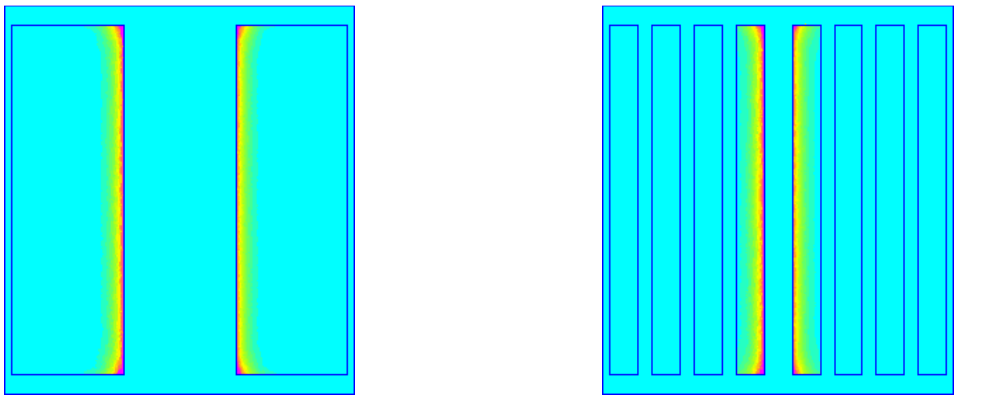
Figure II.28: Fr and leakage inductance reduction by interleaving windings.

In an ICT design, interleaving windings is a good idea when the external circuit is sufficiently inductive to limit the current ripple (e.g. motors).

II.2.5.5 Litz Wire

"The smaller the conductor thickness, the lower the AC/DC resistance factor (or R_{AC}/R_{DC}) of this conductor". By considering this phrase, one could try to reduce losses by subdividing conductors of the winding into several thinner conductors insulated from each other. This is not a good practice!

Actually, simply paralleling these thinner conductors will not change the equivalent AC resistance as shown in Figure II.29 where one solid wire is divided into 4 thinner wires having the same total cross-section and simulated for a given frequency. Since each thinner conductor occupies different positions in the field inside the core window, the AC current is not evenly distributed among the conductors in parallel; they mainly circulate in the innermost conductors and approximately in the same copper section as in the case of a solid wire. As a result, the AC resistance is approximately the same in these two cases.



a) Solid conductor (Fr=14.80) *b) Paralleled conductors (Fr=14.77)*

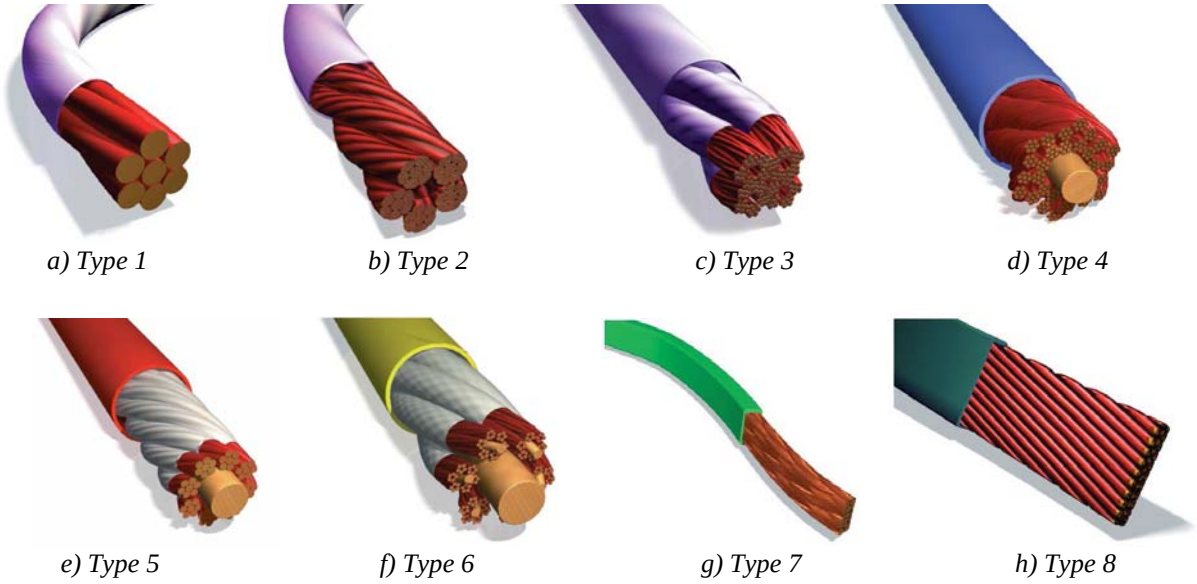
Figure II.29: Current density in solid and paralleled conductors.

Paralleling windings is only interesting if:

- thinner conductors are put in the same layer (i.e. if they see the same field) and the resulting layer is thinner than the original one;

- thinner conductors are interleaved the same way as shown in the last sub-section;
- thinner conductors are twisted similar to Litz wires.

Litz wires are fine conductor which are woven or twisted in such a manner that they successively occupy the same position in the field. These conductors, which are individually insulated, are connected in parallel at the terminations of the winding. There are different types of Litz wires, depending on the number of thin conductors and the number of bundles (set of twisted wires), as shown in Figure II.30 which was obtained from [77].



a) Type 1 *b) Type 2* *c) Type 3* *d) Type 4*

e) Type 5 *f) Type 6* *g) Type 7* *h) Type 8*

Figure II.30: Litz wire types and construction [77].

For high frequency and low power applications, Litz wires containing several very fine woven wires are used although they have poor copper utilization. On the other hand, high power applications usually require the use of Litz wires containing few wires in a single bundle.

The theoretical copper utilization factor, which is the total copper area divided by the total area occupied by the Litz wire, is shown in Table II-5 [78] where the number of levels stands for the number of times bundles are twisted together. For example, if the number of strands per twist is equal to 3, it means that Litz wire at Level 1 has only one bundle containing 3 fine twisted wires. Litz wire at Level 2 contains 3 Litz wire at Level 1 twisted together, resulting on a wire having 9 fine wires. Levels are used to provide flexibility in fitting the winding to the available area and to improve utilization factor.

# wires/ bundle	**3**		**4**		**5**		**6**	
	Total # of wires	**Utilization factor**	**Total # of wires**	**Utilization factor**	**Total # of wires**	**Utilization factor**	**Total # of wires**	**Utilization factor**
Level 1	3	0.65	4	0.69	5	0.69	6	0.67
Level 2	9	0.42	16	0.47	25	0.47	36	0.44
Level 3	27	0.28	64	0.32	125	0.32	216	0.30
Level 4	81	0.18	256	0.22	625	0.22	1296	0.20
Level 5	243	0.12	1024	0.15				

Table II-5: Utilization factor of Litz wires [78].

In real Litz wires, utilization factors are smaller than the ones shown in the table above since usually round conductors are used and insulation occupies a certain space. Also note that DC resistance of Litz wires is higher than that of a single wire having the same copper cross-section area. This is because each fine wire is twisted and consequently they have greater length than straight wires. Optimization of windings made of Litz wire is presented in [62][79].

II.2.5.6 Conclusions about High Frequency Copper Loss Reduction

The best way to reduce high frequency copper losses is to design the ICT (or a transformer) so that skin and proximity effects are minimized. This is usually done by increasing the layer width and reducing its thickness (usually using foil winding). However cores may have strange elongated shapes which possibly increase core losses. In addition, the part of the winding outside the core window should not be neglected because 2D or 3D magnetic field may induce high copper losses in foil windings.

Reducing the number of turns is also a good solution to reduce copper losses, but consequences on the core flux density and core losses must be taken into account. Global optimization of the transformer is the best option to find the best trade-off between copper and core losses, temperature rise, weight and volume.

II.3 Limit Frequency

In a power transformer design, sometimes the number of turns necessary on the primary and on the secondary is primarily chosen as the mutual and leakage inductances are relatively defined. There are cases where the transformer designer does not have a vast option of cores available, and so the geometry of the core window is fixed. Also, a maximum utilization of the winding window must be used in order to reduce DC or low frequency AC copper losses. In such cases, the designer must take special attention on how many layers and how many turns in each layer are chosen so the high frequency copper losses are minimized.

For example, if we take Figure II.31 as the basis of our analysis, the winding on the right side of the core must fit in the core window, specifically in the space reserved to it (represented by the light grey area at the right side), which has width W_w and height H. Analysis presented here is valid for transformers made with pot-cores or planar cores since the greatest part of the winding is contained inside the core window.

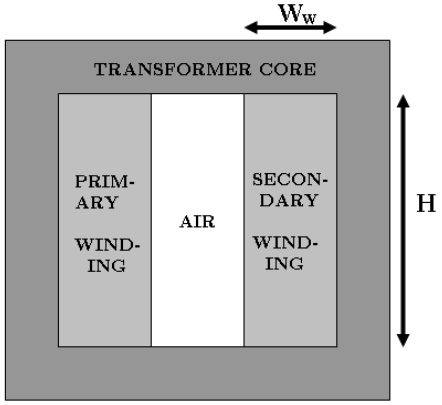
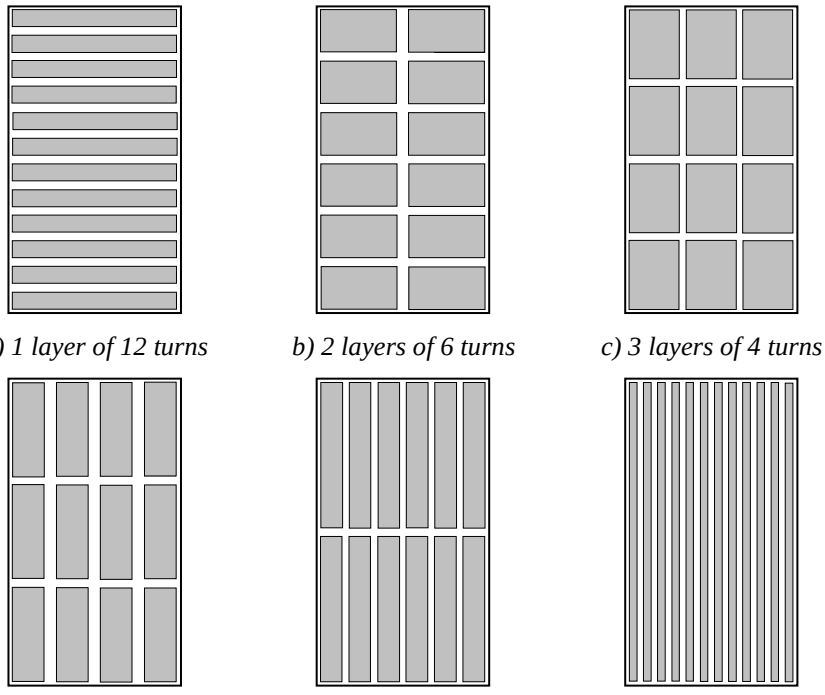


Figure II.31: Core window and winding area.

As shown in Figure II.32, if the winding has, for example, 12 turns, there are 6 different ways of fitting the conductors inside the winding area, if the conductor's shape is not already defined. They are: a) 1 layer of 12 turns, b) 2 layers of 6 turns, c) 3 layers of 4 turns, d) 4 layers of 3 turns, e) 6 layers of 2 turns and f) 12 layers of 1 turn. If conductors have round cross-section, the analysis shown here may be used with some approximations which could be part of future work.



a) 1 layer of 12 turns *b) 2 layers of 6 turns* *c) 3 layers of 4 turns*

d) 4 layers of 3 turns *e) 6 layers of 2 turns* *f) 12 layers of 1 turn*

Figure II.32: Configurations for fitting 12 conductors inside the winding area.

The conductor cross-section areas are the same in all these configurations, but in each of them the conductor dimensions *Wc* and *Hc* are different. For this reason, it is not direct to say that the copper losses are higher in the 12-layer configuration than in the 1-layer configuration. It depends on the frequency, as will be seen below.

In order to calculate high frequency copper losses or AC resistance of each configuration, some preliminary considerations must be made:

1. Insulation between conductors is negligible.
2. All the turns, in one specific configuration, have the same dimensions (*Wc* and *Hc*).
3. The field inside the core window is perfectly vertical (assumed in order to use Dowell's equations)

In order to compare the losses associated to each configuration, equation (II-5) was used to calculate *Fr*. Note that all configurations have the same DC resistance, and consequently the one which has the lowest *Fr* is the one which has the lowest losses.

In Figure II.33, *Fr* was calculated for all possible configurations of a transformer with 12 turns, and for a frequency range from 10Hz to 1MHz. The winding area has dimensions W_w=7.24mm and *H*=13.1mm.

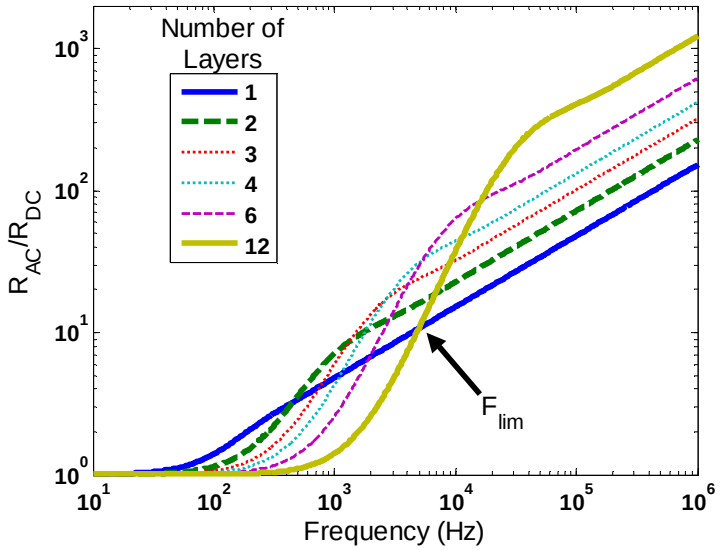


Figure II.33: Variation of the AC resistance with the frequency for each of the configurations of Figure II.32.

By analyzing these curves and several other curves created for windings with N_t turns, some conclusions may be made:

- For lower frequencies, the configuration with N_t layers (from now on called *Configuration B*) is the one which has lower losses.
- For higher frequencies, the configuration with 1 layer (from now on called *Configuration A*) is the one which has lower losses
- With regard to copper losses, the other configurations are never better than the 2 extreme ones (N_t layers of 1 turn or 1 layer of N_t turns).

By the use of MATLAB 7.1, innumerous graphs were generated and it was observed that the 3 conclusions stated above are valid independently of the dimensions of the winding area. Those graphs have the same form as the one in Figure II.33 but the frequency in which *Configuration A* has lower losses than *Configuration B* changes with the winding area width W_w. From now on, this frequency will be called the "Limit Frequency" (F_{lim}).

Note that Fr and F_{lim} can only vary with the winding area width but not with its height since Dowell's formula is a 1D approach.

For a visual explanation of this phenomenon, we have investigated the current distribution in a 12-turn winding of a transformer. A total current of 1A peak is imposed in each turn and current densities are calculated using FEMM software. Thanks to the transformer symmetry only the top half of the secondary is shown in Figure II.34. Four simulations were performed using the configurations of Figure II.32: *Configuration A* using current at frequencies of 3kHz (Figure II.32a) and 300kHz (Figure II.32b) and *Configuration B* using the same currents and frequencies (Figure II.32c and Figure II.32d respectively). Note that Figure II.32a and Figure II.32c, and Figure II.32b and Figure II.32d have the same scale in the color legend. For better visualization, Figure II.32e and Figure II.32f show the 1D representation of the current density of Figure II.32a, b, c and d, in a line crossing all conductors.

By this figure we can conclude that, when frequency is high, *Configuration A* has small area with high current density while *Configuration B* has greater area. That's why there

are higher losses in multilayer windings. On the contrary, when frequency is low, *Configuration A* has a large area with high current density while *Configuration B* has a small area. That's why there are higher losses in single layer windings.

Table II-6 shows the results of *Fr* for this specific example.

	Current Frequency	
	3kHz	300kHz
Configuration A	3.53	35.59
Configuration B	1.07	219.96

Table II-6: Fr for simulations shown in Figure II.34.

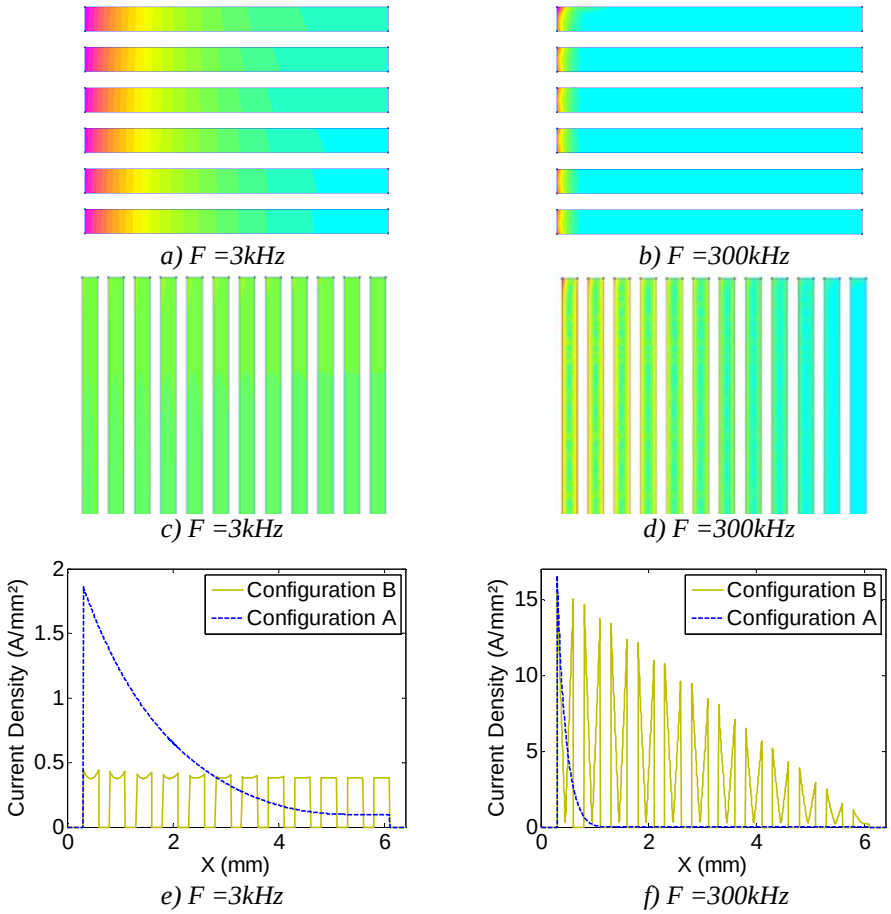


Figure II.34: Current density simulation of configurations A and B. a), b), c), d): 2D representation. e), f) 1D representation in horizontal direction.

Another way of explaining this phenomenon is: in high frequencies, the proximity effect is more important than the skin effect and so the smaller the number of layers the lower the losses. Alternatively, in low frequencies, the skin effect is not so important but the proximity effect is even less important, and so the configurations with high number of layers have lower losses since their conductors are thinner.

The frequency ranges in which the proximity effect is more important than the skin effect and vice-versa are determined by the winding area width, as explained before. Next section shows how this can be done.

II.3.1 Limit Frequency Variation

As observed in previous section, the Limit Frequency for each winding of N_t turns changes with the winding area width. With the purpose of verifying how, several curves similar to the one of Figure II.33 were generated for different window widths. An algorithm was developed to automatically identify the Limit Frequency for each width. The Limit Frequency behavior is shown in Figure II.35, for windings of different number of turns N_t.

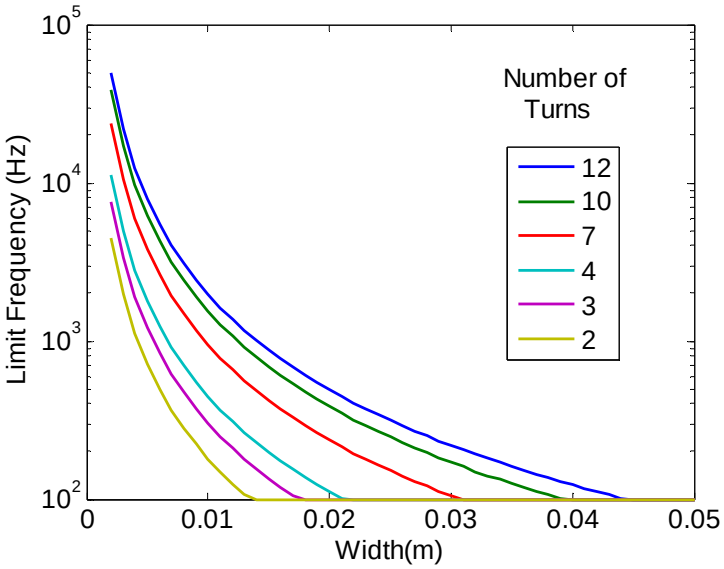


Figure II.35: Limit Frequency variation.

Regarding this figure, the wider the winding area, the lower the Limit Frequency. Following the same line of explanation of last section, if the winding area is wider, the conductors will be wider as well and the skin effect will be even more important than the proximity effect. This results in a reduction of the Limit Frequency.

Another interesting information we can extract from this graph is the region of preference of one configuration over the other. For example, if we have to build a transformer with 12 turns, we find, in the graph of Figure II.35, the point corresponding to the frequency of the current flowing through the transformer and the winding area width. If this point is above the curve for 12 turns, it means that the configuration with 1 layer of 12 turns results in lower losses. Otherwise, if the point is below the curve, the configuration with 12 layers of 1 turn results in lower losses.

Paying closer attention to the curves, one can note that the Limit Frequency is a quadratic function of the winding area width. It means that if we multiply the Limit Frequency and the square of its corresponding width, we will find the same constant, for every window width. These constants are shown in Table II-7, for winding from 2 to 30 turns.

This table is an easy tool to choose which configuration gives lower losses. Designers should only multiply the frequency of the current flowing through the transformer and the square of the winding area width. If the resulting number is greater than the constant in Table II-7 corresponding to the number of turns of the winding, then the configuration with 1 layer of N_t turns results in lower losses, otherwise it is the configuration with N_t layers of 1 turn which is preferable.

N_t	$F_{lim}*W_w^2$	N_t	$F_{lim}*W_w^2$	N_t	$F_{lim}*W_w^2$
		11	0.4395	21	1.0563
2	0.0451	12	0.4945	22	1.1246
3	0.0759	13	0.5513	23	1.1940
4	0.1115	14	0.6095	24	1.2653
5	0.1507	15	0.6695	25	1.3373
6	0.1929	16	0.7308	26	1.4093
7	0.2378	17	0.7932	27	1.4839
8	0.2851	18	0.857	28	1.5582
9	0.3346	19	0.9226	29	1.6346
10	0.3860	20	0.9886	30	1.7101

Table II-7: Observed constants for different number of turns.

II.3.1.1 Analytical Explanation about the Constants

As seen before, the configuration inducing lower losses are either the one having 1 layer with N_t turns or the one having N_t layers with 1 turn in each layer. So, in order to analyticaly find the Limit Frequency, we must find which frequency gives the same Fr with Dowell's equations for the two configurations. Equation (II-14) is related to the configuration having 1 layer with N_t turns while equation (II-15) is related to the configuration having N_t layers with 1 turn.

$$Fr_A = Q_A \frac{\sinh 2Q_A + \sin 2Q_A}{\cosh 2Q_A - \cos 2Q_A} \tag{II-14}$$

$$Fr_B = Q_B \frac{\sinh 2Q_B + \sin 2Q_B}{\cosh 2Q_B - \cos 2Q_B} + 2Q_B \frac{N_t{}^2 - 1}{3} \frac{\sinh Q_B - \sin Q_B}{\cosh Q_B + \cos Q_B} \tag{II-15}$$

where Q_A and Q_B are the corresponding ratios between conductors thickness and skin depth. They are given by the equations below:

$$Q_A = {W_w}/{\delta} = W_w \sqrt{\sigma \pi \mu f} \tag{II-16}$$

$$Q_B = {W_w / N_t}/{\delta} = \frac{W_w}{N_t} \sqrt{\sigma \pi \mu f} = \frac{Q_A}{N_t} \tag{II-17}$$

Solving for Fr_1=Fr_2, we have:

$$N_t \frac{\sinh 2N_t Q_B + \sin 2N_t Q_B}{\cosh 2N_t Q_B - \cos 2N_t Q_B} - \frac{\sinh 2Q_B + \sin 2Q_B}{\cosh 2Q_B - \cos 2Q_B} - 2\frac{N_t{}^2 - 1}{3} \frac{\sinh Q_B - \sin Q_B}{\cosh Q_B + \cos Q_B} = 0 \tag{II-18}$$

The left part of equation (II-18) gives the curves of Figure II.36 related to each winding having N_t turns. For better visualization, we have chosen to show the curves for windings having from 2 to 15 turns.

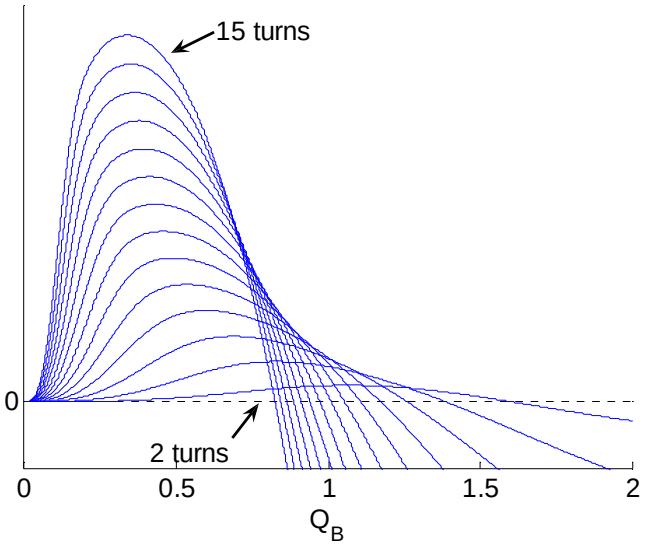


Figure II.36: Curves of equation (II-18), for each winding having N_t turns.

Analyzing these curves we note that for each winding having N_t turns, there is a unique $Q_B = Q_0$ which satisfies equation (II-18). This happens at a frequency equal to the Limit Frequency. Since Q_B is given by equation (II-17), we note that

$$Q_0 = \frac{W_w}{N_t}\sqrt{\sigma\pi\mu F_{\lim}} \tag{II-19}$$

or

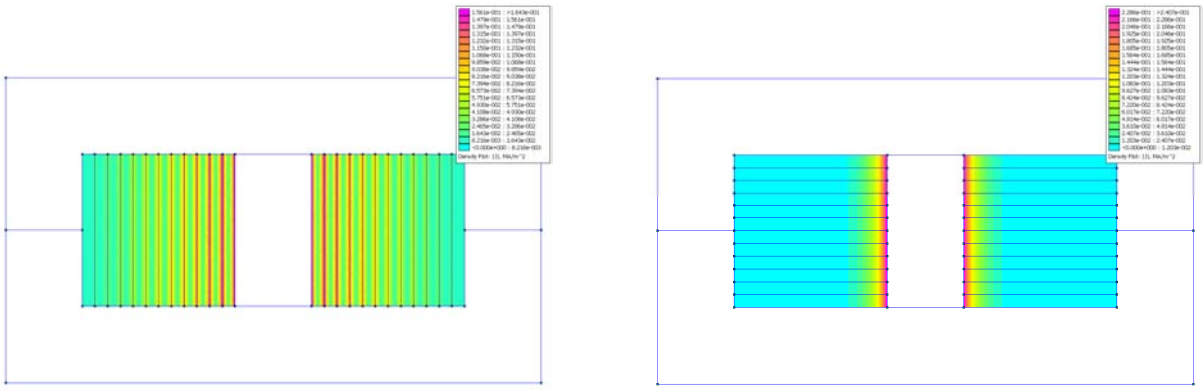
$$F_{\lim} W_w{}^2 = \frac{(N_t Q_0)^2}{\sigma\pi\mu} \tag{II-20}$$

By equation (II-20) we verify that the product of the Limit Frequency and the square of the window width is a constant for each winding having N_t turns, if the permeability and conductivity of the conductor are considered constant. Table II-7 was generated for conductors made of copper at 20°C, having $\mu = 4\pi\cdot10^{-7}$N/A^2 and $\sigma = 58\cdot10^6$S/m.

II.3.1.2 FEM Simulations

In order to evaluate the precision of Dowell's formula and Table II-7, FEM simulations using software FEMM were performed. Figure II.37 shows an example of the problem having winding window width W_w=12mm.

Simulations for several different frequencies were performed and the R_{AC}/R_{DC} ratio was obtained for each frequency. Results are presented in Figure II.38 and compared to Dowell's equation applied to this example. Note that both simulation and calculation have very close results.



a) 12 layers of 1 turn *b) 1 layer of 12 turns*

Figure II.37: Simulated transformers.

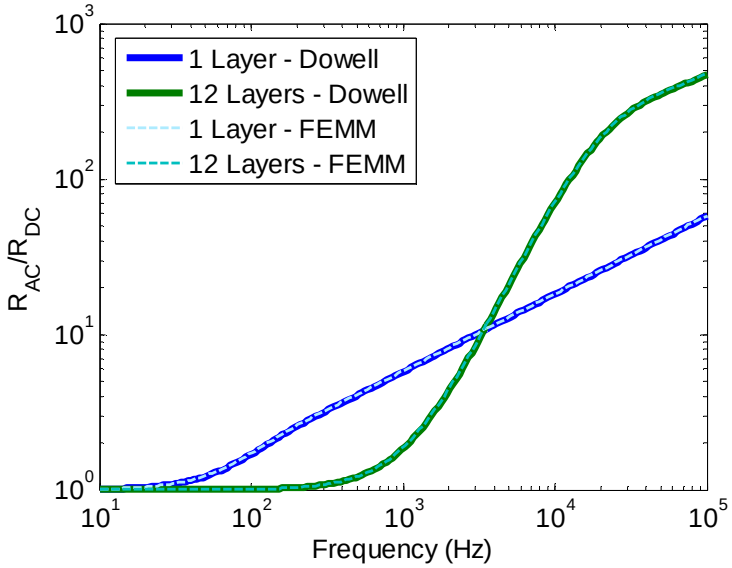


Figure II.38: Simulation and analytical calculation of the Fr behavior for the example above.

Also using FEMM software, a set of simulations was performed with the purpose of finding the Limit Frequency for windings having N_t turns and different winding width. After finding all F_{lim}, the constants could be calculated (F_{lim}*W_w^2) and shown in Table II-8. Note that these values are very close to those of Table II-7 and that the difference is not greater than 0.5%. This confirms that Dowell's equation can be used to calculate the Limit Frequency and the constants used to tell which winding position produces lower losses.

N_t	F_{lim}*W_W^2	N_t	F_{lim}*W_W^2	N_t	F_{lim}*W_W^2
		11	0.4410	21	1.0601
2	0.0452	12	0.4962	22	1.1291
3	0.0761	13	0.5533	23	1.1992
4	0.1118	14	0.6118	24	1.2703
5	0.1512	15	0.6719	25	1.3428
6	0.1935	16	0.7334	26	1.4156
7	0.2386	17	0.7963	27	1.4896
8	0.2861	18	0.8604	28	1.5647
9	0.3357	19	0.9257	29	1.6409
10	0.3874	20	0.9924	30	1.7183

Table II-8: Constants found by simulation.

II.3.2 The Influence of Non-Sinusoidal Currents

Although the values in Table II-8 are useful for giving a general overview of the choice on the position of the winding, the results only apply to sinusoidal currents which is not the case for most of switch-mode power supply transformers or InterCell Transformers. Therefore we analyze the influence of non-sinusoidal current flowing through conductors in windings and how it modifies the choice of the number of turns and layers which minimize copper losses.

In order to verify the influence of non-sinusoidal currents on the Limit Frequency, Dowell's formula for each harmonic will first be used. Later simulations using FEM software will be carried out with the purpose of obtaining more precise results and evaluating the use of Dowell's formula.

The same approach used in the last section may be applied here. In order to analyticaly find the Limit Frequency, we must match the equation of losses (equation (II-13)) for the two configurations. P_1 is the equation related to the configuration of 1 layer of N_t turns, and P_2 is the equation related to the configuration of N_t layers of 1 turn.

$$P_1 = R_{dc}\left({I_{dc}}^2 + \sum_{n=1}^{\infty} \frac{{a_n}^2}{4} \sqrt{n} Q_A \frac{\sinh 2\sqrt{n}Q_A + \sin 2\sqrt{n}Q_A}{\cosh 2\sqrt{n}Q_A - \cos 2\sqrt{n}Q_A} \right) \tag{II-21}$$

$$P_2 = R_{dc}\left[{I_{dc}}^2 + \sum_{n=1}^{\infty} \frac{{a_n}^2}{4} \left(\sqrt{n}Q_B \frac{\sinh 2\sqrt{n}Q_B + \sin 2\sqrt{n}Q_B}{\cosh 2\sqrt{n}Q_B - \cos 2\sqrt{n}Q_B} + 2\sqrt{n}Q_B \frac{{N_t}^2 - 1}{3} \frac{\sinh \sqrt{n}Q_B - \sin \sqrt{n}Q_B}{\cosh \sqrt{n}Q_B + \cos \sqrt{n}Q_B} \right) \right] \tag{II-22}$$

Using equations (II-16) and (II-17) and solving for $P_1 = P_2$, we find the following expression:

$$\sum_{n=1}^{\infty} {a_n}^2 \left(N_t \frac{\sinh 2\sqrt{n}N_tQ_B + \sin 2\sqrt{n}N_tQ_B}{\cosh 2\sqrt{n}N_tQ_B - \cos 2\sqrt{n}N_tQ_B} - \frac{\sinh 2\sqrt{n}Q_B + \sin 2\sqrt{n}Q_B}{\cosh 2\sqrt{n}Q_B - \cos 2\sqrt{n}Q_B} - 2\frac{{N_t}^2 - 1}{3} \frac{\sinh \sqrt{n}Q_B - \sin \sqrt{n}Q_B}{\cosh \sqrt{n}Q_B + \cos \sqrt{n}Q_B} \right) = 0 \tag{II-23}$$

Equation (II-23) depends basically of 3 parameters: the number of turns in the winding (N_t), the number of harmonics in the current (n) and the amplitude of each harmonic (a_n). Having these 3 values, we can find Q_B=Q_0 which solves this equation as shown for the case of sinusoidal currents.

The influence of each harmonic (n and a_n) in the value of Q_0 is difficult to be analytically analyzed since equation (II-23) is given by a relatively complicated expression. However, Figure II.39 gives us an insight of such an influence, for a winding of 12 turns (N_t =12). In this figure, the x-axis is the ratio between the amplitude of the harmonic and the amplitude of the fundamental. We have plotted the influence of the 3rd and the 5th harmonics.

Note that in both curves adding harmonics decreases the value of Q_0. The higher the amplitude of the harmonic, the smaller the value of Q_0, and consequently the smaller the Limit Frequency. Also, the higher the frequency of the harmonic, the smaller the value of Q_0.

For a given type of waveform, the harmonic content changes depending on the duty cycle (D) of the static converter. As a result, the value of Q_0 also changes when the duty cycle is modified. As an example, Figure II.40 shows the variation of Q_0 with the duty cycle, for a

triangular current. Since the harmonic content of the triangular current is symmetric about the value D=0.5, we only plot the values of Q_0 for duty cycles from 0.05 to 0.5, for a number of turns N_t from 2 to 15. Note that the closer the duty cycle from 0.5, the higher the value of Q_0 since the harmonic content is lower for this duty cycle.

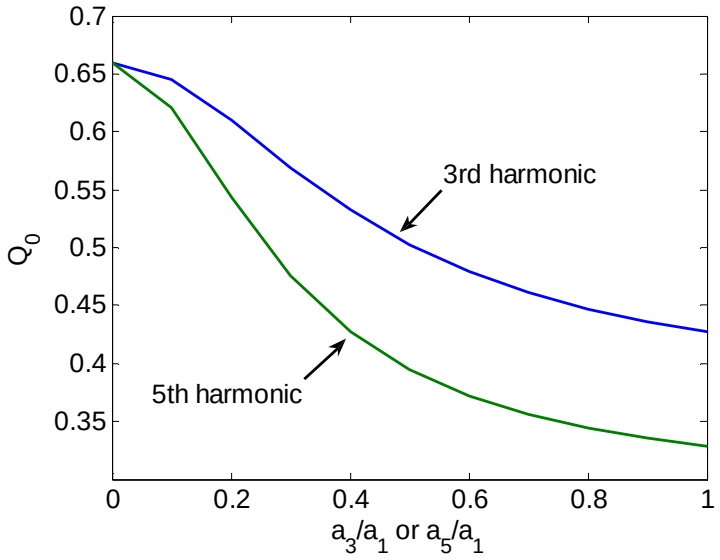


Figure II.39: Variation of Q_0 with the amplitude of the 3rd and 5th harmonics.

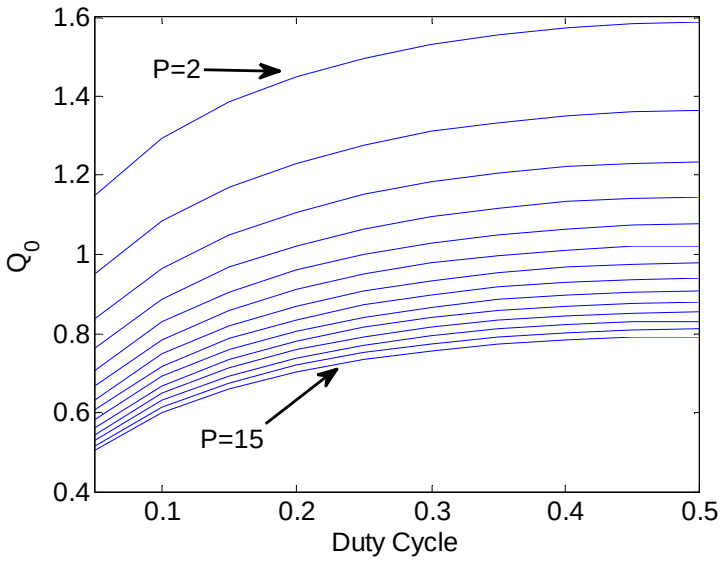


Figure II.40: Variation of Q_0 with the duty cycle.

Also, for some types of waveforms, the rise and fall times play an important role in the harmonics and, as a consequence, they modify the value of Q_0. If we take a square waveform as an example, the value of Q_0 changes with regard to the ratio between the rise/fall times (tr) and the fundamental period (T) as shown in Figure II.41.

High values of tr result on less square-shape currents. This contributes to diminish the harmonic content of the current and consequently to increase the value of Q_0.

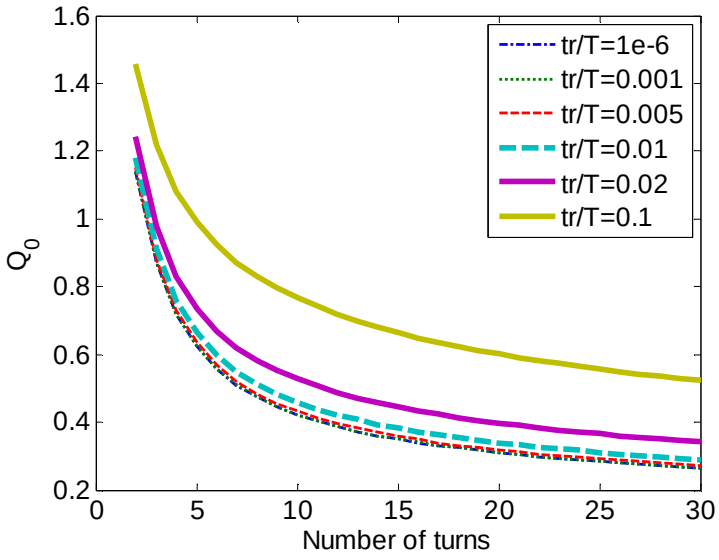


Figure II.41: Variation of Q_0 with the rise and fall times.

With the values of Q_0 found for each winding of N_t turns and for each type of current waveform, we can set up a table for each type of current waveform containing the values of $F_{lim}*W_w^2$ used to decide which configuration leads to lower losses.

Instead of showing one table for each type of waveform, we decided to aproximate their values by a polynome of 4th degree (equation (II-24)) and show all results in a compact form in Table II-9. Note that this table contains the coefficients to be multiplied by the powers of the number of turns, as shown in the equation below, for each of the main types of current waveforms found in switch-mode power supplies, shown in Figure II.42. In this table, we used D=0.5 and tr/T=0.01.

$$F_{\lim} * W_w{}^2 = C_4 p^4 + C_3 p^3 + C_2 p^2 + C_1 p + C_0 \qquad \text{(II-24)}$$

In order to illustrate the difference in the product $F_{lim}*W_w^2$ between different waveforms, we have calculated, using the coefficients in Table II-9, this product for windings containing 2, 10 and 20 turns. We included these values in the final columns of Table II-9.

Comparing the exact values found by equation (II-23) and those aproximated by the 4th order polynomes, it was found that the error is below 3.4% for N_t=2 and far below 1.2% for N_t>2.

Similar to Table II-7, Table II-9 is an easy tool used to choose which configuration is the one resulting in fewer losses. The designer should only multiply the frequency of the current flowing through the transformer and the square of the winding area width. If the resulting number is greater than the result of the polynome described by the coefficients in Table II-9 corresponding to current waveform, then the configuration with 1 layer of N_t turns results in fewer losses, otherwise it is the configuration with N_t layers of 1 turn which is preferable.

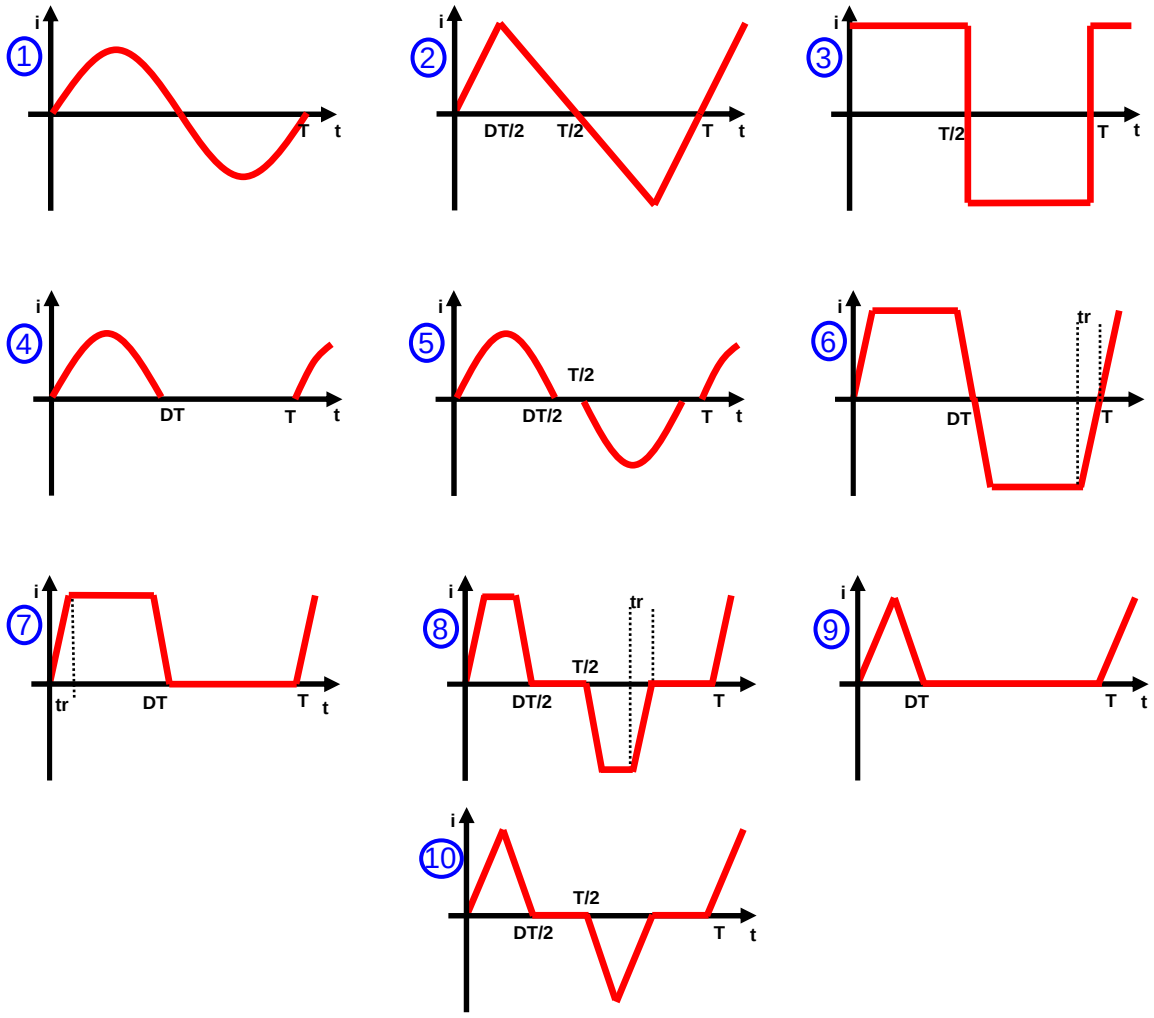


Figure II.42: Typical current waveforms found in switch-mode power supplies.

Wave form	C4	C3	C2	C1	C0	$F_{lim}*W_W^2$ (N_t =2)	$F_{lim}*W_W^2$ (N_t =10)	$F_{lim}*W_W^2$ (N_t =20)
1	$4.37x10^{-7}$	$-4.09x10^{-5}$	0.001954	0.023832	-0.011582	0.0436	0.3856	0.9893
2	$3.81x10^{-7}$	$-3.54x10^{-5}$	0.001688	0.023247	-0.010411	0.0426	0.3592	0.9072
3	$-3.22x10^{-8}$	$9.62x10^{-7}$	$1.15x10^{-4}$	0.005359	0.012158	0.0233	0.0779	0.1681
4	$3.17x10^{-7}$	$-2.96x10^{-5}$	0.001414	0.019137	-0.007055	0.0366	0.2993	0.7554
5	$1.93x10^{-7}$	$-1.80x10^{-5}$	$8.63x10^{-4}$	0.011759	-0.002811	0.0240	0.1850	0.4644
6	$-1.30x10^{-8}$	$-4.00x10^{-7}$	$1.59x10^{-4}$	0.006581	0.011075	0.0249	0.0923	0.2012
7	$-1.36x10^{-8}$	$-3.91x10^{-7}$	$1.61x10^{-4}$	0.006591	0.011053	0.0249	0.0926	0.2020
8	$-1.87x10^{-8}$	$5.55x10^{-8}$	$1.45x10^{-4}$	0.006564	0.009554	0.0233	0.0896	0.1964
9	$2.97x10^{-7}$	$-2.76x10^{-5}$	0.001307	0.017984	-0.006425	0.0346	0.2795	0.7031
10	$1.70x10^{-7}$	$-1.59x10^{-5}$	$7.66x10^{-4}$	0.010906	-0.003275	0.0215	0.1682	0.4214

Table II-9: 4^{th} order polynomial coefficients related to equation (II-24) *and results.*

II.3.2.1 FEM Simulations

In order to evaluate the accuracy of Dowell's formula and Table II-9, simulations using FEMM software were performed using the same structure as in Sub-Section II.3.1.2.

Since FEMM only simulates sinusoidal currents we were obligated to simulate for each frequency separately and then sum up all losses to post calculate an equivalent AC resistance in order to compare with analytical calculation using Dowell's formula. The formula of the equivalent AC resistance is shown in equation (II-12).

Simulations of a triangular current for several different fundamental frequencies were performed and the ratio R_{ACeq}/R_{DC} was obtained for each fundamental frequency. Each triangular current was simulated up to the 11th harmonic. This is plotted in Figure II.43. Also in this figure we plot the curves calculated by Dowell's equation for this specific configuration. Note that Dowell's formula and FEMM simulation give very close results.

Also using FEMM, a set of simulations was performed varying the number of turns N_t in the windings, the winding area width W_w and the type of current waveform, in order to find the Limit Frequencies. After finding all those Limit Frequencies, we could calculate the constants ($F_{lim}*W_w^2$) for each winding of N_t turns, to compare with the values found in Table II-9. For all types of current waveform shown in this chapter, there is no error greater than 4.0% for N_t=2 and 1.74% for N_t>2, which validates Table II-9.

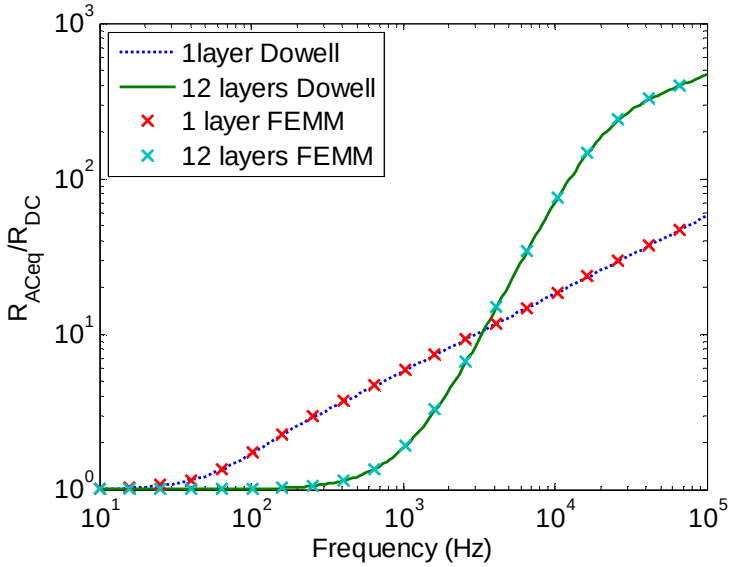


Figure II.43: AC resistance variation by simulation in a FEM software and analytical calculation.

II.4 Conclusions

High frequency copper losses have a significant influence on the design of InterCell Transformers. It is important for a designer to understand the phenomena related to these losses in order to design small and compact ICTs.

Skin and proximity effects are the two most important high frequency effects related to copper losses in inductors and transformers and their analytical calculation is restricted to simple cases. Analytical calculation of skin effect is possible for a conductor placed far from other conductors and magnetic cores and proximity effect formulas may only be used when the conductors are placed inside a 1D magnetic field (e.g. inside a transformer core window with appropriate geometry). For all other cases, 2D or 3D FEM simulation is needed to precisely predict the AC resistance (which can increase very significantly at the switching frequency and its multiples), and accurately evaluate the resulting copper losses.

Using FEM simulations, losses related to airgaps, to the end-turn of windings and to conductors in an inductor have been evaluated. We have shown the difference between copper loss behavior in inductors and in transformers. Contrary to what happens in an inductor, airgaps do not necessarily increase copper losses in transformers.

It was observed that the part of the winding outside the core window may generate much higher losses than the one inside it, which does not allow using directly Dowell's equations to calculate copper losses in ICT designs.

We investigated some techniques to try to reduce copper losses in ICTs and we concluded that:

- Adding magnetic material in some parts of the ICT reduce copper losses for some cases and increase them for other cases. In all cases it increases core losses and the final weight of the ICT.
- Placing the conductors as spread out as possible in the vertical direction of the core window reduces copper losses and leakage inductance, but this is not a practical solution.
- Interleaving windings is a very effective way to reduce proximity effect but it also reduces the leakage inductance, which may not be wanted when designing ICTs.
- Paralleling conductors into thinner wires does not reduce high frequency copper losses. Instead we may use Litz wires, which is an expensive solution. However, special attention must be taken since this type of wire may have a poor utilization factor. In ICTs flowing mainly DC or low frequency currents, this is generally not a very good solution.
- When designing an ICT, most of the time a smart choice of the number of turns and the conductor's shape is enough to keep high frequency copper losses in an acceptable level.

The shape (and later the position) of a fixed number of turns in a fixed winding window was investigated with the purpose of reducing losses. Based on Dowell's formula, constants which relate the number of turns of a winding, the fundamental frequency of the current passing through the winding and the winding area width were found for different types of current waveforms. These constants are an easy tool for transformer and especially for ICT designers. They indicate the orientation of the conductors inside the winding area which results in lower AC copper losses.

Since Dowell's formula is a 1D approximation of a 3D phenomenon, intensive 2D FEM simulation was carried-out to verify the validity of the constants found. Insulation between conductors was not taken into account and it will be part of future work.

Chapter III

InterCell Transformer Design

III.1 Introduction

The objective of a magnetic component design depends on the application where this element will be inserted. For certain applications, price is the main characteristic which must be reduced. For aerospace applications, the main concern is total weight, and for traction applications, it might be volume or footprint which is crucial for the design.

The design of an ICT is not that different from any other magnetic component. It involves the same phenomena as an inductor or transformer design but the formulation still needs to be quite different because the relative importance of these phenomena is quite different. In [15], a two-phase coupled inductor based on an E+I ferrite core to be used in a buck converter is shown. These coupled inductors were used in order to improve the response of low-voltage DC-DC converter. In the same article, also a 4-phase coupled inductor in a ladder structure with leakage leg is designed.

In [38], procedures for ICT design and inductor design are presented, and output filters for PWM inverters using these two types of component are compared. Based on the method explained in [80], a specific design method is developed to achieve this comparison based on toroidal core shapes.

Similar design technique is used in [7] to build ICTs used in an 8-cell Flyback. The main specificity of this design is the reduction of the leakage inductance of the primary/secondary which is always a limiting factor of this type of converter, even in its multicell version.

In this section a more general design will be explained. We will try to show how to design ICTs considering several topologies and different methods, from the most precise and time-consuming to the fastest but less accurate. We will explain the design of an ICT by separating it in 4 main parts:

1. Copper Losses: where we calculate the losses in the windings, taking into account all the frequencies present in the current flowing through them.

2. Core Losses: where we verify the high frequency flux waveforms flowing through the core legs and we calculate magnetic losses based on different models.

3. Flux Density Saturation: where DC or low frequency flux is calculated and added to the high frequency flux in order to keep it within a certain range.

4. Thermal: where total losses are calculated and the temperature rise of the ICT is established by using simple thermal models.

III.2 Two-Cell ICTs

Two-cell ICT is probably more frequently used in the industry and it is also easier to be designed than an N-cell ICT. Thus its design will be explained first and in the next section we will show the differences between ICT designs for two or more commutation cells.

A 2-cell ICT is to be used in applications where only two commutation cells are available. The typical diagram is shown in Figure III.1, where a basic DC chopper is used as an example of interleaved converter. In this case, the leakage inductance of the ICT must be high enough to keep the current ripple at a level determined by the designer.

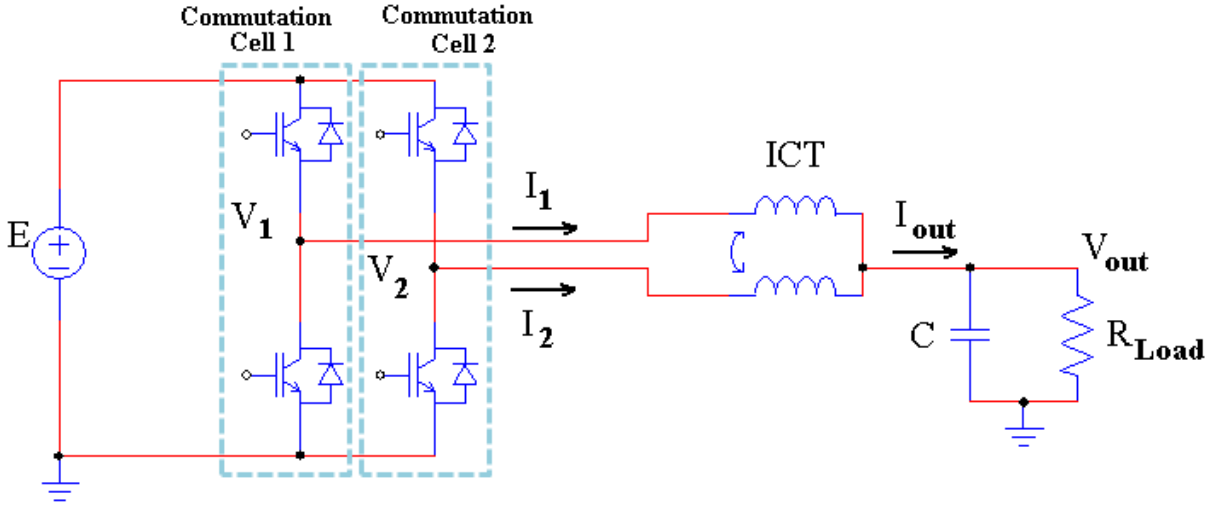
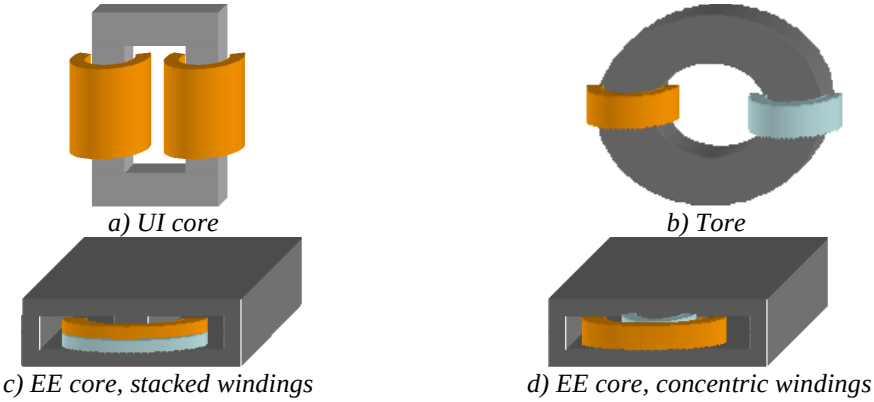


Figure III.1: Two-cell intercell transformer used in an interleaved converter.

Since the ICT has only two windings, a variety of core shapes may be used and some of them are shown in Figure III.2. The choice of the core shape depends basically on the availability of the material, size and price. It strongly influences the design process since shapes in Figure III.2a and b typically result in ICTs with higher leakage inductance values than those in Figure III.2c and d. This is due to the fact that the leakage energy is mainly concentrated in the region between the windings in Figure III.2c and d while it is spread out in the space around the ICTs of Figure III.2a and b.



a) UI core *b) Tore*

c) EE core, stacked windings *d) EE core, concentric windings*

Figure III.2: Two-cell ICTs using different core shapes.

The ICT in Figure III.2d is not actually considered in the design of a two-cell ICT as its windings are not symmetrical. The outer winding is longer than the inner one, which may cause current imbalance in the final converter. It should be noted that this is not a particular

problem for N-phase ICTs in cyclic cascade topology since two 2-cell ICTs are used in each cell, which allows connecting the shorter winding of the first ICT in series with the longer winding of the second ICT and makes the circuit symmetric.

III.2.1 Copper Loss Calculation

A complete analysis of copper losses was presented in the last chapter. Skin and proximity effects were reviewed and calculation and simulation of losses in conductors were performed in order to clarify the phenomena associated to copper losses in ICTs.

One of the first choices to be made before starting an ICT design is related to the type of conductors used: round cross section or rectangular cross section; one or more wires in parallel; made of copper, of aluminium, or other material?

The choice of the cross section shape depends on the application and the availability of wires. Usually round wires are more easily found in the market, available in different sizes and insulators. Further it is usually easier to wind with this type of conductor. On the other hand, windings made of conductors with rectangular cross section, such as foil or helical windings, have higher fill factor which is a great advantage when designing compact structures. When the current flowing through the winding has high DC or low frequency component and also high frequency ripple, conductors with important cross section must be used but the designer must reduce skin and proximity effects as much as possible by using rectangular cross section or Litz wire [78]. In an optimized ICT design, the optimization algorithm has the role of finding the conductor's cross section area and shape and also the position of turns inside the core window in order to determine the best trade off between total copper losses and the optimization objective.

As explained in the last chapter, paralleling conductors in a winding does not significantly reduce copper losses (except if Litz wire is used) and so the advantage is only that it can be used to increase flexibility in the winding process.

The use of copper or aluminium is also an important choice. Aluminium is more resistive than copper but since copper price has dramatically increased in the past few years [81], aluminium becomes a very good option for a low cost ICT design. In [82] the author gives an example using a high-frequency transformer made of multilayer foil winding, where the foil thickness is optimized with regard to the AC resistance as shown in [74]. In this example, although the winding made of aluminium is 28% larger than the one made of copper, it is 6.6 times cheaper based on metal commodity prices. Also, it is less heavy since aluminium's mass density is approximately 3.3 times smaller than that of copper.

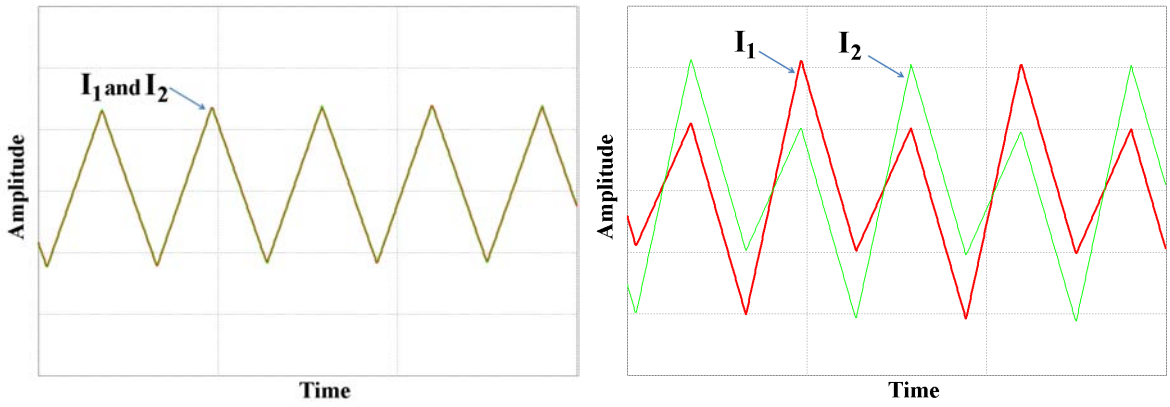
We will start the analysis of copper losses in the design of an ICT by taking the case where a maximum of phenomena and cases can be observed. That is why we choose the example of Figure II.17a. In this case, 2D and/or 3D simulation is necessary since a great part of the windings is outside the core window and 1D model does not apply, as explained in the last chapter. Furthermore, this ICT will be used in 2-cell inverter, as the one in Figure III.1, with fundamental frequency F_m and switching frequency F_s.

The use of 3D FEM simulation may result in accurate calculation of copper losses, but it is very time consuming. Depending on the geometry and precision needed for the 3D simulation, it may not be compatible with limited computational resources. Also, if the ICT is to be optimized, it is unpractical to insert a 3D simulation inside the optimization loop. In these cases, 2D FEM simulation can be considered as shown before.

ICT design is complex but for a given application, it is possible to simplify the problem by making appropriate assumptions. Addressing the ICT design in the general case is more difficult because we need a more complete description of the different phenomena. For example, when the ICT is made of a material with a high permeability and no airgap, the magnetizing current is negligible and we obtain waveforms such as those in Figure III.3a. In this case, the AC copper losses are calculated by evaluating the AC resistance of the windings carrying equal currents at twice the switching frequency and multiples. To obtain an accurate estimate of these resistances, FEM simulations at different frequencies can be made.

When the core material has a lower permeability or when an airgap is used, the magnetizing inductance is lower and the current waveforms are quite different (Figure III.3b).

In this case, we need a second set of 2D simulations with different base frequencies (switching frequency instead of twice the switching frequency) and different supply conditions (opposite currents instead of equal currents).



a) Low reluctance core *b) High reluctance core*

Figure III.3: Currents in the two phases of an ICT.

The drawing of the transformer in the FEM software is the same for both simulations. When simulating the magnetizing current, the current imposed in each winding must have the same direction inside the core window, as shown in Figure III.4a. This simulation is the same as for an inductor. However, when simulating the coupled current, the current imposed in each winding must have opposite directions inside the core window, as shown in Figure III.4b. This simulation is the same as for an ideal transformer. For the case of 2 cells, the magnetizing current is equal to the differential mode current (I_{DM}) and the coupled current is equal to the common mode current (I_{CM}).

a) Magnetizing (differential mode) current *b) Coupled (common mode) current*

Figure III.4: Current directions when simulating coupled and magnetizing currents.

Usually, FEM softwares only allow sinusoidal current simulation, but Fourier analysis may be applied to account for non-sinusoidal currents. Both magnetizing current and coupled

current must be decomposed into Fourier series, and simulation for each important harmonic must be carried out. The easiest way to calculate total AC copper losses is to simulate the behavior for each frequency and then sum up all results to post calculate 4 equivalent AC resistances, which are:

$R_{ACeqintDM}$ (AC equivalent resistance of the conductors inside the core window, due to the differential mode current, $(I_1\text{-}I_2)/2$),

$R_{ACeqextDM}$ (AC equivalent resistance of the conductors outside the core window, due to the differential mode current, $(I_1\text{-}I_2)/2$),

$R_{ACeqintCM}$ (AC equivalent resistance of the conductors inside the core window, due to the common mode current, (I_1+I_2)) and

$R_{ACeqextCM}$ (AC equivalent resistance of the conductors outside the core window, due to the common mode current, (I_1+I_2)).

The equation of the ratio between the equivalent AC resistance and the DC resistance has the following form:

$$Fr_{eq} = \frac{R_{ACeq}}{R_{DC}} = \sum_{n=1}^{\infty} Fr_n a_n{}^2 \qquad \text{(III-1)}$$

where Fr_n is the ratio between the equivalent AC resistance and the DC resistance of the n^{th} harmonic and a_n is the amplitude of the n^{th} harmonic of the current (either the differential mode or the common mode), normalized as shown in equation (II-12).

The DC resistances of the conductors inside and outside the core window (R_{DCint} and R_{DCext} respectively) are generally different because their lengths are different. For example, in the transformer in Figure II.17a, the length of the conductors inside the core window is equal to the core window depth, while the mean length of the conductors outside the core window is equal to the mean turn length minus the core window depth.

Two examples will be used to illustrate the method. The ICT of Figure II.17a, drawn with 6 turns in each winding, was simulated using FEMM software.

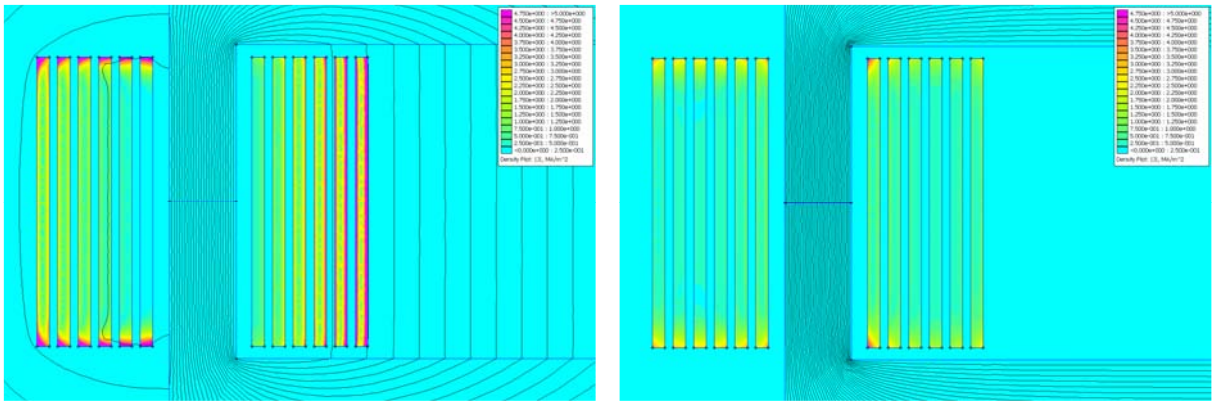
III.2.1.1 Conductors in "Vertical" Position

The first example is an ICT having 6 turns connected in series. The winding is made of copper foil conductors. Simulations were made at fundamental frequency equal to 15kHz and temperature equal to 20°C. Simulation output graphs, for one specific frequency, are shown in Figure III.5. The colors in this figure indicate the absolute value of current density in each conductor. The total current in each conductor is the same although they have different current densities.

In Figure III.5a, we show the distribution of the common mode current. Note that inside the winding window the proximity effect is very important and that 2D effects are not so visible. It means that copper losses in these conductors could be precisely calculated by using Dowell's equations. On the other hand, outside the winding window there is a strong 2D effect but the field intensity is much lower. As a result, for this frequency, copper losses are higher inside than outside the winding window.

In Figure III.5b we show the distribution of the differential mode current. Note that inside and outside the winding window the proximity effect is important and that 2D effects are not negligible. It means that copper losses in these conductors could not be calculated by

using Dowell's equations. Also note that copper losses are approximately the same inside and outside the winding window.



a) Common mode current *b) Differential mode current*

Figure III.5: FEMM simulation of a simple ICT (Current density plot), using "vertical" conductors.

The ratios between AC and DC resistances simulated using FEMM are shown in Table III-1 along with the first 5 terms of the Fourier series of the common and differential mode currents when the duty cycle is equal to 0.25 (as the one shown in Figure III.3b).

Harmonic	**a_n I_{DM}**	**Fr_n ext-DM**	**Fr_n int-DM**	**a_n I_{CM}**	**Fr_n ext-CM**	**Fr_n int-CM**
1	0.9360	1.64	1.43	0.9927	3.12	2.28
2	0.3309	2.12	1.81	0	4.78	5.86
3	0.104	2.58	2.26	0.1103	6.58	11.29
4	0	3.07	2.78	0	8.55	17.97
5	0.0374	3.58	3.38	0.0397	10.60	25.30
		Fr_{eq} ext-DM	**Fr_{eq} int-DM**		**Fr_{eq} ext-CM**	**Fr_{eq} int-CM**
Total		1.70	1.48		3.17	2.42

Table III-1: AC/DC resistance ratio simulation results for example using vertical conductors.

The amplitudes of higher order harmonics are small and, as a consequence, they have a negligible influence in the total equivalent AC resistance. That is why it is reasonable to simulate a few harmonics only.

Note that the equivalent AC/DC resistance ratios for the conductors outside the core window are different from those related to the conductors inside. Also, these ratios are usually higher for common mode current since its fundamental frequency is the double of that of the differential mode current.

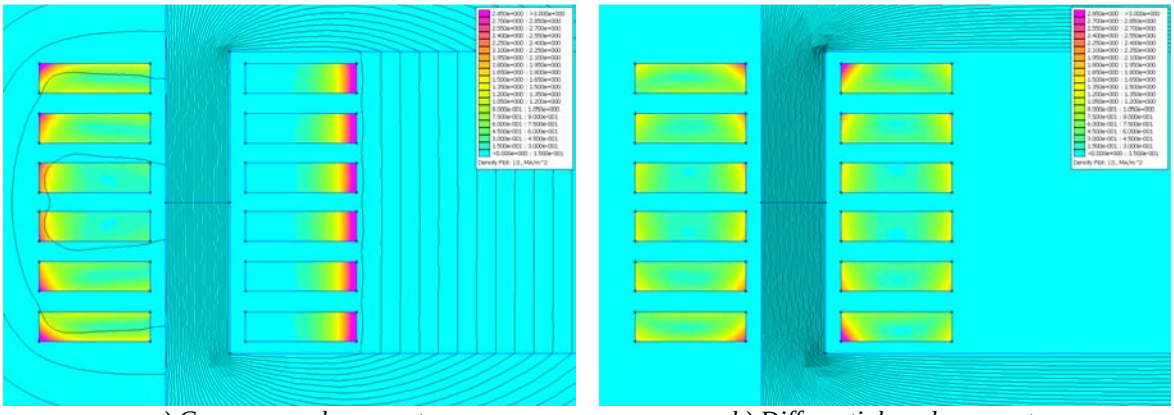
III.2.1.2 Conductors in "Horizontal" Position

The second example is an ICT having also 6 turns connected in series. It is a helical coil winding using flat helical copper conductors. Conductors have the same cross-section area than those in the first example. Simulations were made at fundamental frequency equal to 15kHz and temperature equal to 20°C. Simulation output graphs, for one specific frequency, are shown in Figure III.6. The colors in this figure also indicate the absolute value of the current density in each conductor.

In Figure III.6a, we show the distribution of the common mode current. Note that inside the winding window the proximity effect is not important since we have only 1 layer

and 2D effects are not significant. On the other hand, outside the winding window there is a strong 2D effect and that is why we can see proximity effect in the vertical direction. The distortion of flux lines is higher outside, the intensity is higher inside; for this frequency and this geometry, FEM simulation shows that the influence of the intensity is predominant and makes copper losses higher inside than outside the winding window.

In Figure III.6b we show the distribution of the differential mode current. Note that inside and outside the winding window the proximity effect is not important and skin effects are more apparent. Also note that copper losses are approximately the same inside and outside the winding window.



a) Common mode current *b) Differential mode current*

Figure III.6: FEMM simulation of a simple ICT (Current density plot), using "horizontal" conductors.

As done for the first example, the ratios between AC and DC resistances simulated using FEMM are shown in Table III-2 along with the first 5 terms of the Fourier series of the differential mode and common mode currents when the duty cycle is equal to 0.25 (as the one shown in Figure III.3b).

Harmonic	**a_n I_{DM}**	**Fr_n ext-DM**	**Fr_n int-DM**	**a_n I_{CM}**	**Fr_n ext-CM**	**Fr_n int-CM**
1	0.9360	2.69	2.79	0.9927	2.35	3.85
2	0.3309	4.20	4.13	0	3.81	5.39
3	0.104	5.26	5.13	0.1103	5.13	6.57
4	0	6.10	5.96	0	6.22	7.57
5	0.0374	6.82	6.69	0.0397	7.13	8.47
		Fr_{eq} ext-DM	**Fr_{eq} int-DM**		**Fr_{eq} ext-CM**	**Fr_{eq} int-CM**
Total		2.88	2.96		2.39	2.89

Table III-2: AC/DC resistance ratio simulation results for example using horizontal conductors.

When comparing both tables above, we can see that, for this specific case, using "vertical" conductors, the equivalent AC resistance outside the winding window is greater than the one inside the winding window. This is because the fundamental high frequency is not high enough to cause proximity effect losses higher than the losses due to the horizontal field outside the window (which is very weak inside). Of course this is not a general rule and different results can be obtained if the geometry is "pulled or compressed" along the horizontal or the vertical axis, if the number of turns is different, if the frequency is different and probably also if the material used for conductors is different.

III.2.1.3 Copper Losses Calculation Related to High Frequency Current

Having the four AC/DC resistance ratios, we can calculate the four equivalent AC resistances as shown below:

$$R_{ACeqintDM} = Fr_{eqint-DM} \cdot R_{DCint} \quad \text{(III-2)}$$

$$R_{ACeqextDM} = Fr_{eqext-DM} \cdot R_{DCext} \quad \text{(III-3)}$$

$$R_{ACeqintCM} = Fr_{eqint-CM} \cdot R_{DCint} \quad \text{(III-4)}$$

$$R_{ACeqextCM} = Fr_{eqext-CM} \cdot R_{DCext} \quad \text{(III-5)}$$

The total high frequency copper losses in both winding are calculated using these resistances and the RMS value of the differential mode current (I_{DM}) and the common mode current (I_{CM}), as shown below. Note that this is true even if I_{DM} and I_{CM} have harmonics of the same frequency, if the symmetry in the ICT guarantees equal resistances in both windings. This is demonstrated in Appendix C.

$$P_{HFcu} = \left(R_{ACeqintDM} + R_{ACeqextDM}\right) \cdot I_{DM}^2 + \left(R_{ACeqintCM} + R_{ACeqextCM}\right) \cdot I_{CM}^2 / 4 \quad \text{(III-6)}$$

This approach for calculating total high frequency copper losses is fast since it makes use of simple and fast 2D simulation FEM software to simulate 3D geometries. About six 2D simulations are usually sufficient to fairly represent the equivalent high frequency resistances related to the non-sinusoidal current flowing in InterCell Transformers. Therefore, this method is suitable to be used in the design and optimization of ICTs.

III.2.1.4 Design Tip: Errors When Using Global R_{AC}/R_{DC} Ratio

As explained before, Dowell's equations and other related formulas give the ratio R_{AC}/R_{DC} for a winding having m layers, which is the average of the ratio R_{AC}/R_{DC} of each layer. If we have a "winding+core" configuration where each layer has different length, it means that each turn will have different DC resistance and consequently the AC resistance calculated by Dowell's equations or by the procedure shown above will be quite different from the real one.

If we take the configuration of the two examples shown above, it is clear that when conductors are in the horizontal position, each turn has the same length. However, if the conductors are in the vertical position, each turn has a different length outside the window and this can lead to an error in the high frequency resistance calculation. Suppose that the configuration shown in Figure III.5 has the following characteristics: 6 turns; each conductor has 0.3mm width and 7mm height and it is made of copper at 20°C; the core has a square section with 4mm width and 4mm depth and it is made of a high permeability material. Table III-3 shows, for each turn, the results of R_{AC}/R_{DC} simulated using FEMM at 100kHz as well as the length, the DC resistance and the AC resistance. In the bottom of this table, the total AC resistance is compared to the AC resistance calculated if an average R_{AC}/R_{DC} and length were calculated as it is usually done. The analysis is shown only for the part of the winding which is outside the core window since the turns inside the core window have the same length.

Note that, for this case, the precise AC resistance is 5.5% higher than the one calculated with the average value. In a configuration where the number of turns is much higher, proximity effect is more important and the outer turns will have an even more important R_{AC}/R_{DC}. As a consequence the error may turn out to be much higher than the one presented in this example and the ICT will have much higher losses than initially estimated.

Turn position (from the most internal to the most external)	R_{AC}/R_{DC}	Turn Length (mm)	R_{DC} (mΩ)	R_{AC} (mΩ)
1	5.61	14.20	0.12	0.65
2	4.83	16.20	0.13	0.64
3	5.44	18.20	0.15	0.81
4	6.60	20.20	0.17	1.09
5	8.54	22.20	0.18	1.56
6	12.31	24.20	0.20	2.45
Total R_{AC} accounting for different R_{AC}/R_{DC} and different length in each turn				7.21
Total R_{AC} using the same R_{AC}/R_{DC} and length for each turn				6.83

Table III-3: AC/DC resistance ratio simulation results for each turn of the example using vertical conductors.

III.2.1.5 Copper Losses Calculation Related to Low Frequency Currents

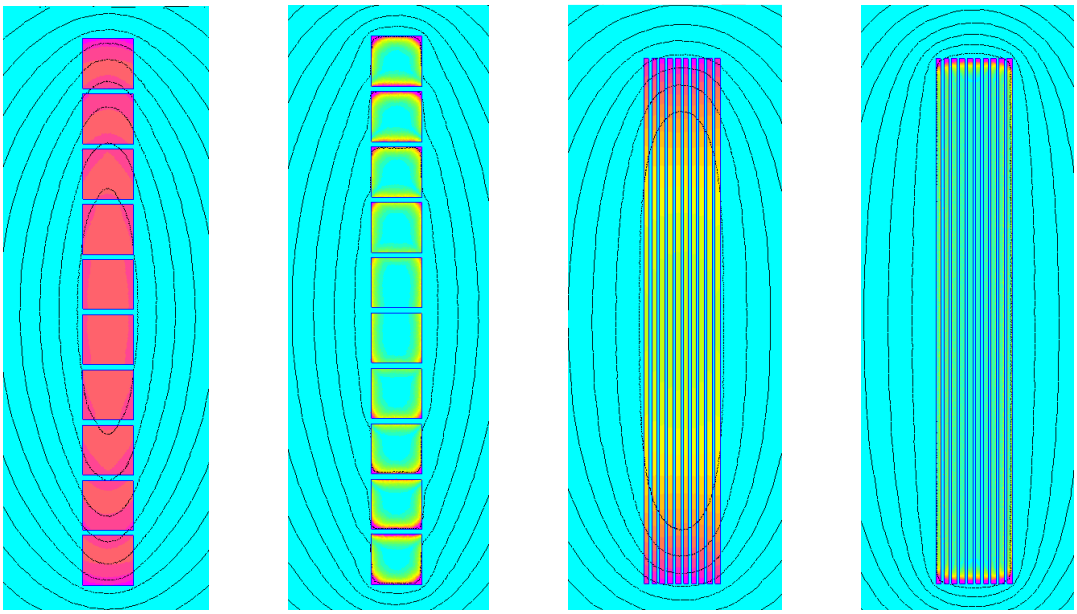
Estimating DC copper losses is usually an easy task. It can be derived from the conductor's length, cross section, and resistivity (the latter possibly adjusted as a function of the estimated temperature). Low frequency copper losses (typically at 50 or 60Hz) are often calculated using the same DC resistance, implicitly assuming that skin and proximity effects are not important at low frequency. In this section, we want to show that this assumption is not always valid and it may induce important errors.

For this purpose let's take the example of a group of 10 conductors in the air surrounded by a 2D magnetic field (in this case, created by the current flowing through these conductors). We will compare the AC/DC resistance ratio (Fr) of these conductors for a current at two different frequencies: 50Hz and 5kHz. We will also change the conductor's cross-section dimensions. The first has a square cross-section (10mm thick, 10mm high). The second has the same cross-section area (100mm²) but it has a thickness equal to 1mm and it is 100mm high. The simulation results showing the current density of these two conductors at the two frequencies are shown in Figure III.7 along with their corresponding AC/DC resistance ratio.

As seen in Chapter II, for high frequency, making the conductor thinner reduces its AC resistance. On the other hand, for low frequency, making the conductor thinner may increase its AC resistance. This phenomenon can be explained as follows:

- For high frequency, the 2D magnetic field creates very important skin effect in both directions of the square conductor since skin depth is much smaller than the conductor's thickness. When the conductor is made thinner, the skin effect in the thinner direction is extremely attenuated since the conductor's thickness becomes smaller than the skin depth. The skin effect is intensified in the other direction but only a small surface supports a high current density and the overall AC resistance is reduced.
- For low frequency, the skin depth is much higher than the thickness of the square-section conductor and consequently the AC resistance is approximately the DC resistance. However, when the conductor is made thinner, one direction has always the length smaller than the skin depth, but the other becomes much

higher than the skin depth. Consequently, skin effect can be observed in this direction and the AC resistance is increased.



a) Freq = 50Hz Fr = 1.03 | *a) Freq = 5kHz Fr = 11.3* | *a) Freq = 50Hz Fr = 1.18* | *a) Freq = 5kH Fr = 6.64*

Figure III.7: FEMM simulation of conductors with different dimensions but with the same cross-section area, at two different frequencies (current density plot).

The problem illustrated above can be found in an inductor or ICT design. When they are used at the output of parallel multilevel inverters, the main current component is at the fundamental frequency, but there is also a less important high frequency current at the switching frequency and/or *N* times this frequency.

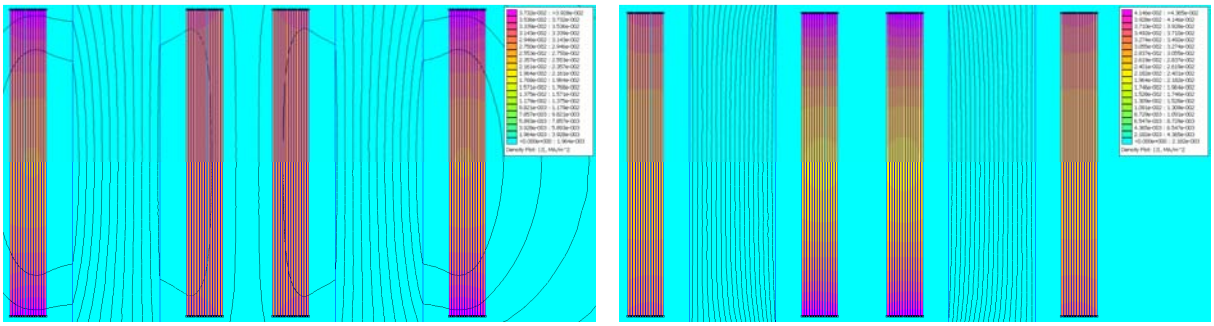
Depending on the design parameters, foil or Litz wire must be used to allow both low and high frequency currents to flow without creating high losses. If foil winding is adopted, the conductor must be very thin to reduce high frequency effects. If the copper section is kept constant, the conductor must be made very high. In this case, the designer has to be careful not to underestimate low frequency losses.

In order to show the problem, we will use the example of an ICT and an inductor constructed in the same way, i.e., the same core and the same windings (the inductor is made of two windings in series, one in each side of the core). The structure chosen is the one of Figure II.17a, which is made of 2 windings of 16 turns each. Conductors have width equal to 1mm, height equal to 60mm and are made of aluminium at 20°C. FEM simulation is shown in Figure III.8 for both structures and current flowing at 50Hz.

In the ICT simulation there is skin effect at 50Hz in the part of the winding outside the winding window since the magnetic field has a strong 2D characteristic. It is not the case inside the window where the magnetic field is mainly vertical and the conductor width is small compared to the skin depth at 50Hz. In the inductor simulation, the field has 2D characteristic inside and outside the window.

The linear AC resistances (resistance per unit length) calculated making use of the simulations above are shown in Table III-4. Note that, for this case, the error if using DC resistance instead of the real resistance can reach 9% for the part of the winding outside the ICT core window and 13% for the internal part of the inductor's winding. If these types of magnetic components are to be used in applications such as motor drives the error may be

even more important since higher fundamental frequencies are involved. Moreover, it can be even worse if an airgap exists in the core, even for low frequency currents.



a) ICT simulation *b) Inductor simulation*

Figure III.8: Current density distribution simulation of ICT and inductor at low frequency current (50Hz).

Winding	Winding total linear resistance (mΩ/m) at 0Hz	Winding total linear resistance (mΩ/m) at 50Hz	AC/DC resistance ratio
External part (ICT)	11.61	12.62	1.09
Internal part (ICT)	11.61	11.65	1.00
External part (Inductor)	11.61	12.00	1.03
Internal part (Inductor)	11.61	13.15	1.13

Table III-4: Winding resistances at low frequency.

Important Conclusion #1: DC resistance should not be used to calculate low frequency copper losses for ICTs designs employing foil winding. Instead, FEM simulation is recommended to precisely calculate the AC resistance.

III.2.2 Leakage Inductance Calculation

ICT filtering capabilities strongly rely on the leakage inductance of such devices. That is why it is very important to predict the leakage flux flowing in the air or in a magnetic material used for this purpose.

In most of ICT designs, the leakage inductance directly influences both copper (strong influence) and core losses (slight influence). It also affects the maximum magnetic flux density in the core. In order to understand how, let's use one of the models of Figure III.9 applied to the circuit of Figure III.1.

In the model of Figure III.9a, L is the self inductance and M the mutual (or magnetizing) inductance of the ICT. Since it is an ICT, the mutual inductance is negative (note the points in Figure III.9) and the leakage inductance is equal to twice the difference between the values of the inductances, or

$$L_{leak} = 2(L - M) \tag{III-7}$$

If the series resistance of the ICT is neglected, the currents and voltages of the ICT are linked by the following equations (refer to Figure III.1):

$$V_1 - V_o = V_{1o} = L\frac{dI_1}{dt} - M\frac{dI_2}{dt} \quad \text{and} \quad V_2 - V_o = V_{2o} = L\frac{dI_2}{dt} - M\frac{dI_1}{dt} \tag{III-8}$$

which can be rewritten as

$$I_1 = \frac{\int (LV_{1o} + MV_{2o})dt}{(L^2 - M^2)} \quad \text{and} \quad I_2 = \frac{\int (LV_{2o} + MV_{1o})dt}{(L^2 - M^2)} \tag{III-9}$$

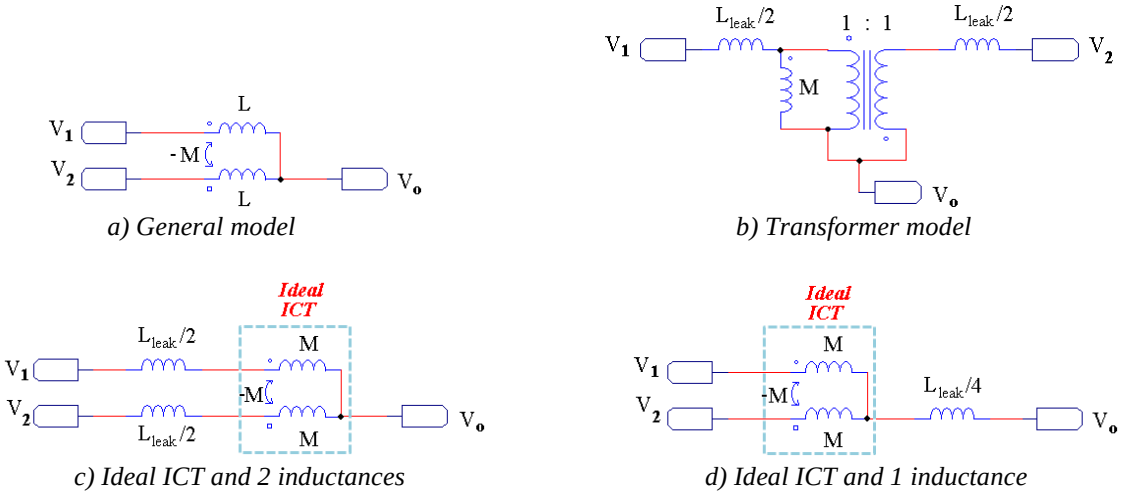
Supposing that the self and mutual inductances are much higher than the leakage inductance, which is usually the case in an ICT, equation (III-9) can be rewritten as

$$I_1 = I_2 = \frac{I_{CM}}{2} = \frac{\int (V_{1o} + V_{2o})dt}{(L_{leak})} \tag{III-10}$$

As it was expected, both current are equal and have triangular waveform at $2 \cdot F_s$ since V_1 and V_2 are square voltages phase-shifted by180°. From now on this current will be called common mode current (I_{CM}). Note that if the leakage inductance is not negligible compared to the mutual inductance, the differential mode current I_{DM} at frequency F_s will be important and can be calculated as the difference of the currents in equation (III-9), as shown below:

$$\frac{I_2 - I_1}{2} = I_{DM} = \frac{\int (V_2 - V_1)dt}{2(L + M)} = \frac{\int (V_2 - V_1)dt}{2\left(2L - L_{leak}/2\right)} \tag{III-11}$$

Note that the differential mode current only depends on the difference of the switched voltages and the self and mutual inductances. It depends very weakly of the leakage inductance since it is usually much smaller than the self inductance. Differential mode current has a trapezoidal waveform and its maximum value occurs at $\alpha=0.5$.



a) General model *b) Transformer model*

c) Ideal ICT and 2 inductances *d) Ideal ICT and 1 inductance*

Figure III.9: ICT electrical models.

When leakage inductance is much smaller than self inductance, the differential mode current can be neglected, otherwise both common mode and differential mode current must be calculated to evaluate copper losses. Equations (III-12) and (III-13) stand for the calculation of, respectively, the peak-to-peak common mode and differential mode currents in the circuit of Figure III.1, which is used in a buck converter switching at duty cycle α and having DC bus voltage equal to E.

$$I_{CM\ pp} = \frac{\alpha'(1-\alpha')E}{(2F_s L_{leak})} \quad \text{(III-12)}$$

$$I_{DMpp} = \frac{(1-|1-2\alpha|)E}{\left(4F_s\left(2L - {L_{leak}}/{2}\right)\right)} \quad \text{(III-13)}$$

The relative duty cycle α' is the one calculated for interleaved converter and its value is shown in equation (I-2). The common mode current depends on the relative duty cycle and the differential mode current depends on the real duty cycle. Copper losses caused by these two currents are calculated as shown in the last sub-chapter. Remember that the above formulas apply to the currents flowing in each cell. In the load, the differential mode currents of the two phases cancel out and the common mode currents add up, so that the high frequency current on the load side is I_{CM}.

The calculation of the self inductance L is usually an easy task. It is done the same way as for the case of a regular inductor. Either we calculate it using the nominal inductance (A_L) given by the core manufacturer and we multiply it by the square of the number of turns of one winding, or we use the value of the permeability, cross section and mean path length of the core. Calculating the leakage inductance is much more difficult.

Classical calculation of leakage inductance in transformers is found in many references, such as in [69] or in [83]. The formulas are only valid for the part corresponding to the energy inside the core window. Equation (III-14) shows the calculation of the simplest case corresponding to Figure III.10, where there is no winding interleaving. In the formula, N_t is the number of turns of one winding, l_{av} is the mean turn length (or the core depth in most of the cases), μ_0 is the air permeability and the others are geometrical parameters shown in Figure III.10.

$$L_{leak} = l_{av} \cdot \mu_0 \cdot \frac{N_t^{\,2}}{h} \cdot \left[b_3 + \left(\frac{b_1 + b_2}{3} \right) \right] \quad \text{(III-14)}$$

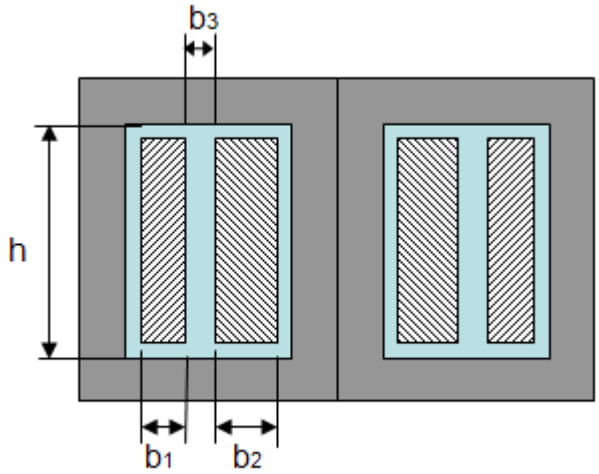


Figure III.10: Geometrical parameters of a transformer used for leakage energy calculation inside the core window

This formula is valid if no 2D or 3D effects exist inside the winding window, i.e. when the conductors totally fill the window height. Also it is only valid for DC or low frequency currents. Besides the resistance, leakage inductance is also changed by skin and proximity effects as explained by Dowell [47]. Leakage energy decreases in the winding region but not in the region between the windings. The inductance reduction factor F_L, which is equal to the ratio between the inductance at a certain frequency and the inductance at 0Hz is calculated as shown below:

$$F_L = \frac{L_{AC}}{L_{DC}} = \frac{3 \cdot Z'' + \left(N_l^2 - 1\right) G''}{m^2 \left|Q_L\right|} \tag{III-15}$$

where m is the number of layers, Z'' and G'' are the imaginary part of Z and G respectively which are

$$Z = Q_L \coth\left(Q_L\right) \quad \text{and} \quad G = 2Q_L \tanh\left(Q_L / 2\right) \quad \text{for} \quad Q_L = Q\sqrt{2j} \tag{III-16}$$

Q is the Dowell's factor presented in Chapter II and $j = \sqrt{-1}$.

III.2.2.1 Leakage Inductance Simulation

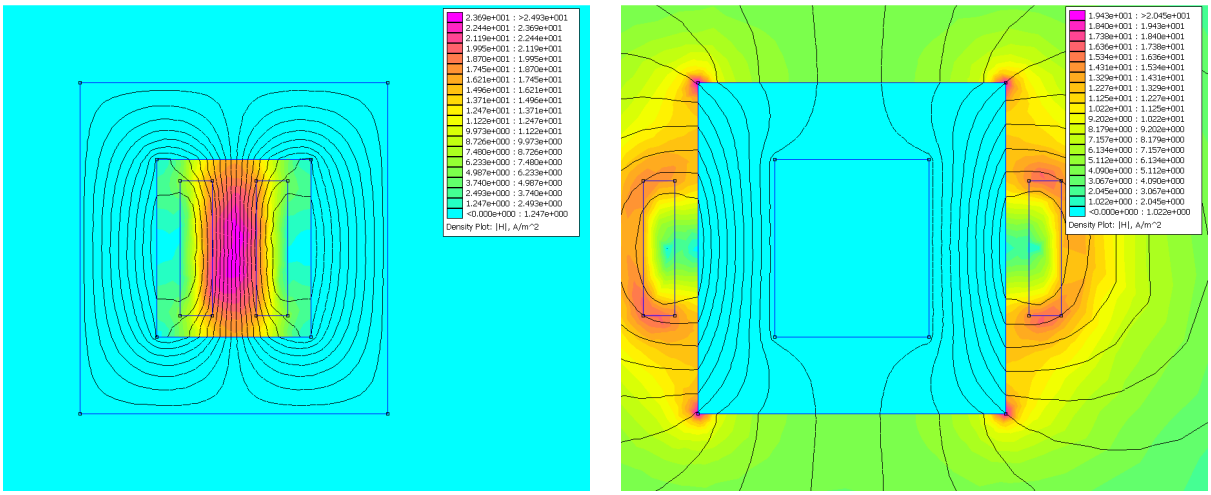
To estimate the leakage inductance outside the window and inside the window in realistic conditions, the use of FEM solvers seems to be the only solution [67][84][85][86].

The use of 3D FEM simulation may result in accurate calculation of the leakage inductance, but it is very time consuming. Depending on the geometry and precision needed for the 3D simulation, it is sometimes unrealizable due to limited computational resources. Also, if the ICT is to be optimized, it is unpractical to insert 3D simulation inside the optimization loop. Thus, appropriate 2D FEM simulation can be considered in order to have a fast estimation of the total leakage inductance [87][88][89][90].

Here we will present a simple procedure that allows calculating the leakage inductance and reluctance of intercell transformers, based on 2D FEM simulations. This procedure relies on the calculation of 4 linear inductances (inductance per unit of length): two related to the part of the winding inside the core window ($L_{leaklfint}$ and $L_{leakhfint}$) and two related to the outside ($L_{leaklfext}$ and $L_{leakhfext}$). For a better understanding of this model, let's consider the transformer of Figure II.17a.

Initially, we perform two simulations of a frontal cut of this transformer only with the conductors inside the core window, as shown in Figure III.11a. The first simulation is made in low frequency or DC, depending on the converter's application, which allows calculating the low frequency inductance per unit length $L_{leaklfint}$ (in H/m). The second one is made in high frequency (typically the switching frequency of the converter) and gives the high frequency inductance per unit length $L_{leakhfint}$ (in H/m). Both of them are related to the volume inside the core window.

Then, a second set of simulations is needed. We simulate a frontal cut of this transformer only with the conductors outside the core window, as shown in Figure III.11b. Thus we can calculate the inductances per unit length $L_{leaklfext}$ and $L_{leakhfext}$ (in H/m).



a) Conductors inside the core window *b) Conductors outside the core window*

Figure III.11: FEM simulation of intercell transformer (absolute value of the magnetic field intensity).

To calculate the total leakage inductance related to low and high frequencies, we use the following equations:

$$L_{leaklf} = L_{leaklfint} d_{int} + L_{leaklfext} d_{ext} \quad \text{(III-17)}$$

$$L_{leakhf} = L_{leakhfint} d_{int} + L_{leakhfext} d_{ext} \quad \text{(III-18)}$$

where d_{int} is the average turn length inside the core window and d_{ext} is the average turn length outside the core window.

These two leakage inductances have different influences in the design of an ICT. L_{leaklf} is associated to the low frequency magnetic flux flowing through the core and it will be explained how in the next sub-section. Alternatively, L_{leakhf} is associated to the current ripple in the circuit and to equations (III-12) and (III-13).

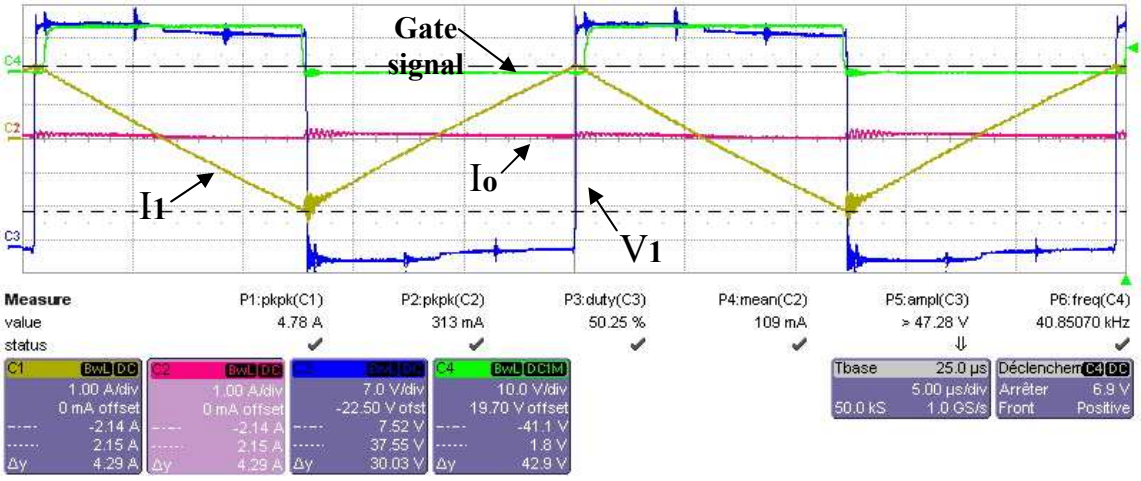
III.2.2.2 Experimental Results

A middle power inductor, shown in Figure III.12, was used to verify the accuracy of the simulation. This inductor has 14 turns in each leg and it is appropriate to be used as an intercell transformer. It is made using a Mega Flux magnetic alloy powder core with a relative permeability equal to 40.

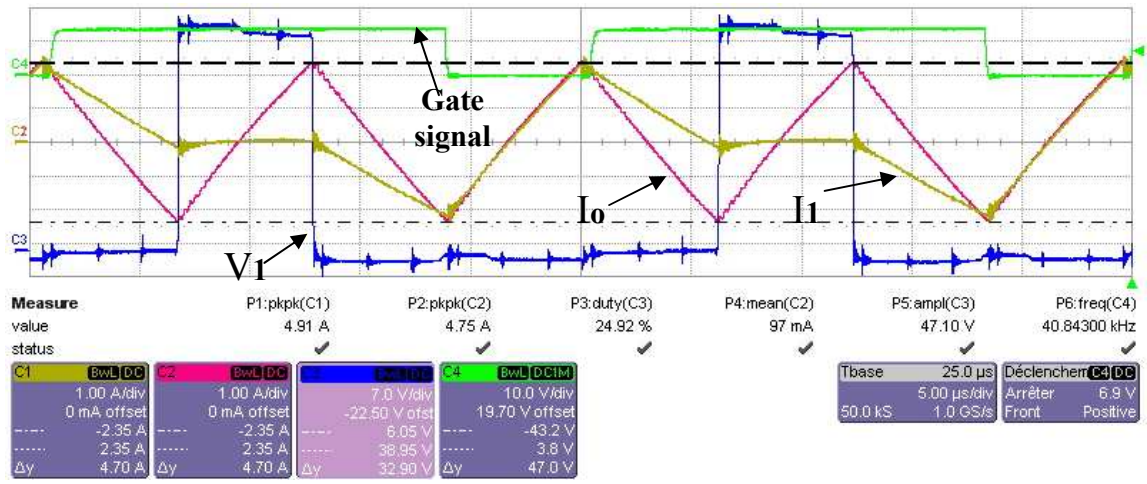
Each winding was connected to a commutation cell as in Figure III.1, switching 47V at 40.8kHz. Commutation cells deliver switching signals 180° out of phase. In order to predict the leakage and magnetizing inductances we make use of equations (III-12) and (III-13). First we take a duty cycle of 0.50. At this value, the differential mode current reaches its maximum value and the common mode current is zero. Like this the current flowing through the ICT has a triangular waveform at the switching frequency and the output current ripple is zero. Experimental curves associated to this case are shown in Figure III.13a.

Next we reduce the duty cycle to 0.25; at this point, the common mode current is maximum and the differential mode current is 3/16 times its maximum (maximum found at a duty cycle of 0.5). Thus, the ICT current is the sum of a triangular current at twice the switching frequency and a triangular current at the switching frequency. Consequently the common mode current value can be measured and the leakage inductance can be calculated. Experimental curves associated to this case are shown in Figure III.13b.

Figure III.12: Intercell transformer.



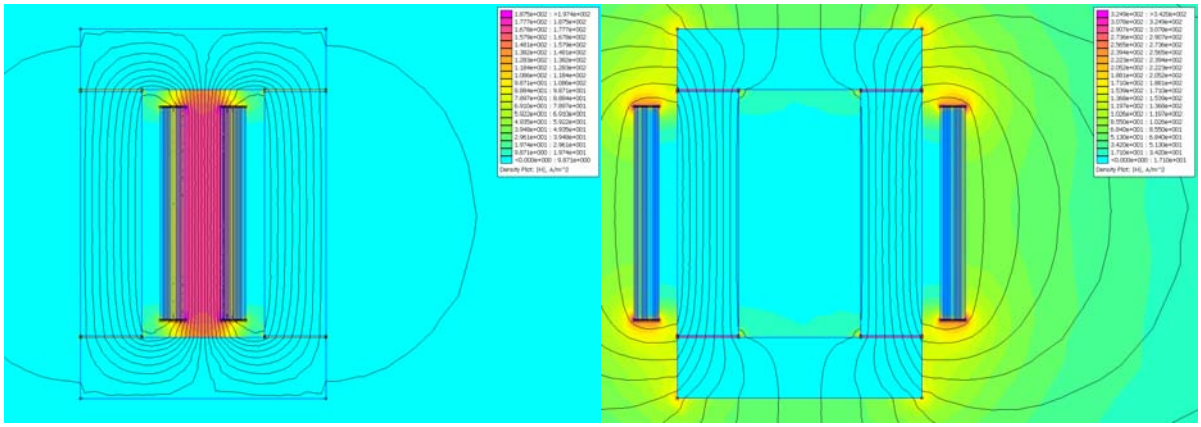
a) α = 0.50



b) α = 0.25

Figure III.13: Experimental waveforms at different duty cycles.

Simulations of this ICT were performed using FEMM software to calculate the leakage inductance at high frequencies. Examples of the simulation output graphs are shown in Figure III.14. Results found are shown in Table III-5 for simulations carried out at 40kHz as well as inductances calculated from experimental results.



a) Conductors inside the core window *b) Conductors outside the core window*

Figure III.14: FEMM simulation of the intercell transformer of Figure III.12 (magnetic field intensity).

Winding	Simulation	Experimental
$L_{leakhfext} \cdot d_{ext}$ (µH)	55	
$L_{leakhfint} \cdot d_{int}$ (µH)	3.5	
L_{leakhf} (µH)	58.5	61.1
L_{maghf} (µH)	69	62

Table III-5: Simulation and experimental results.

Note that there is only 4.25% of difference between the simulated and measured leakage inductance. The magnetizing inductance was also analytically calculated and its value was the same as the one found in the simulation. Experimentally this value is quite different due to the material properties which considerably vary with the temperature and flux frequency.

The procedure used to predict leakage flux by using FEM simulation was also verified with other transformers tested in the laboratory.

III.2.3 Core Loss Calculation

Core losses are often lower than copper losses in ICT designs. However it is often quite difficult to extract heat from the core, therefore it is important to evaluate these losses and try to minimize them. To calculate core losses, three main aspects must be taken into account: the core loss model, the flux density waveforms and the type of magnetic material and core. Each aspect will be discussed in more details below.

III.2.3.1 Core Loss Mechanisms

Authors usually identify three fundamental mechanisms of core losses: hysteresis losses, classical eddy current losses and excess eddy current losses. A good reference about all the mechanisms causing core losses is shown in [91].

Hysteresis losses

Hysteresis losses are defined by the *B(H)* curve of the core material. The hysteresis cycle, which is specific for each material, gives relevant characteristics such as the magnetic permeability (μ), the saturation flux density (B_s), the remnants flux density (B_r) and the coercivity (H_c). For a given alternating magnetic field (H), a magnetic material stores the field energy and restores it during one period of the alternating field. The difference between these two energies is the energy dissipated inside the core, which can be calculated by the area of the hysteresis cycle. Therefore hysteresis losses can be calculated using the maximum flux density B_m in the material for a given alternating magnetic field, oscillating at frequency f, as shown in the equation below [92].

$$P_{hyst} = f \cdot \oint HdB = k_{hyst} \cdot f \cdot B_m{}^{b} \tag{III-19}$$

where k_{hyst} is a hysteresis losses coefficient and b is the magnetic losses coefficient.

Classical eddy current losses

It is similar to the eddy current generated inside conductors in a winding when high frequency current flows through them. Magnetic flux created by windings flows inside the core. Since the core material has a finite resistance, eddy currents will flow inside it in order to compensate the flux variation caused by the alternating flux. This current flowing in the core engenders the so-called classical eddy current losses.

These losses are dependent on the peak flux density (B_p), the frequency (f) and the internal resistivity of the magnetic material (ρ) and they can be approximated by [92]:

$$P_F = k_F \cdot \frac{f^2 \cdot B_p^2}{\rho} \tag{III-20}$$

where k_F is an eddy current loss coefficient.

Excess eddy current losses (or supplementary losses)

This mechanism is the most complex and it theory is based on the Bloch walls. These are "walls" separating magnetic domains which have uniform field inside them. These domains change their size according to the magnetic field applied to them and in this way Bloch walls change their length or they can be moved elsewhere. The result is eddy currents around these Bloch walls. Bloch walls movement depends on the material conductivity, field intensity and frequency and the impurity level and the supplementary losses can be expressed by [92]:

$$P_s = k_s \cdot f^{1.5} \cdot B_p^{1.5} \tag{III-21}$$

where k_s is a parameter which depends on the core geometry and material.

III.2.3.2 Core Loss Models

Firstly it must be pointed out that ICTs are usually designed for high frequency switching devices and thus only adequate core materials will be investigated. It means that models presented in this sub-section are applied to core materials such as ferrites, iron powder and nanocrystallines. These types of materials have high electrical resistivity and consequently almost negligible classical eddy current losses. Also, supplementary core losses may only be important in very high frequency applications. It is clear that hysteresis losses are the most important for this type of material used in an ICT design.

The most classical model used to calculate core losses is the Steinmetz model [93] but it is valid for sinusoidal excitation. Since the area of the hysteresis loop increases when augmenting the peak flux density (B_p) in the material, the increasing energy loss can be measured as a function of this value. Steinmetz model establishes an empirical equation which calculates the mean core loss density (P_{av}, in W/m³) as a function of the excitation frequency and the peak flux density, as shown in the equation below:

$$P_{av} = K_c \cdot f^{\alpha} \cdot B_p^{\beta} \tag{III-22}$$

Coefficients K_c, α and β are determined by best-fitting measured loss data. The main drawback to this representation is the fact it is accurate only over limited ranges of frequency and flux density. It represents core losses fairly well for values of B_p lower than the knee of the initial magnetization curve [91]. Usually manufacturers use various sets of coefficients to represent core losses of their cores and materials, where each set is adjusted to more accurately represent core losses over a particular frequency and/or flux density ranges. As a consequence, discrepancies may be observed when calculating core losses at the boundaries of each range.

With the purpose of improving the curve fitting, different models were created. Some manufacturers modify Steinmetz model to take into account the parameters variation with regard to the temperature, as the one given in [94] and shown below:

$$P_{av} = C_T \cdot K_c \cdot f^{\alpha} \cdot B_p^{\beta} = \left(ct_0 \cdot T_c^{\,2} - ct_1 \cdot T_c + ct_2\right) \cdot K_c \cdot f^{\alpha} \cdot B_p^{\beta} \tag{III-23}$$

In [94], coefficients ct_0, ct_1, ct_2 are estimated for having C_T equal to 1 at temperature T_c equal to 100°C.

Authors in [80] propose a more general formulation to improve the accuracy of the calculation for a large frequency range. This is shown in equation (III-24).

$$P_{av} = K_c \cdot \left(K_{c1} . f^{\alpha_1} + K_{c2} . f^{\alpha_2}\right) . B_p^{\left(\beta - \alpha_\beta f\right)} \tag{III-24}$$

We will use an even more general equation which fits very well for some cores and which can also be used with the coefficients given by manufacturers for the 3 equations above. The frequency dependency is decomposed in 4 terms and the Steinmetz's coefficient β is also decomposed in 4 terms where 3 of them are related to the frequency. This formulation is shown in equation (III-25).

$$P_{av} = K_c \cdot \left(ct_0 \cdot T_c^{\,2} - ct_1 \cdot T_c + ct_2\right)\left(s.f^{\alpha_s} + t + u.f^{\alpha_u} + v.f^{\alpha_v}\right) . B_p^{\left(w.f^{\beta_w} + x.f^{\beta_x} + y + z.f^{\beta_z}\right)} \tag{III-25}$$

Manufacturer Micrometals shows another formulation in [95] specifically for iron powder materials. They develop a new core loss model separating it into two terms, one related to hysteresis losses and the other to eddy current losses. They are shown in equation (III-26) where coefficients *a, b, c* and *d* are determined by "best-fitting" measured data. In [95], authors compare this formulation with simple Steinmetz model and measured data for their cores. Their results show a considerable improvement in the core loss prediction.

$$P_{av} = \frac{f}{\frac{a}{B_p^{\,3}} + \frac{b}{B_p^{\,2.3}} + \frac{c}{B_p^{\,1.65}}} + df^{\,2} B_p^{\,2} \tag{III-26}$$

All the models above are valid for sinusoidal flux density waveforms which are not actually the case for ICTs and other magnetic components used in power electronics. In [92]

the authors show that core losses are greater if using non-sinusoidal excitation when compared to sinusoidal, for the same product $f.B_p$. In [96], authors show that DC bias current also alters core losses.

Thus different models were developed. Reference [96] proposes a model for squared voltage waveform and DC bias flux density where some preliminary measurement must be made over the magnetic material in order to find specific coefficients. In [97] authors propose a methodology to estimate core losses under PWM or dc bias ripple voltage excitations. Their experiments showed that it is possible to implement simple methods to estimate magnetic losses under PWM or dc bias conditions by adding individual minor loop losses.

Losses separation is also applied in [98] where Roshen introduces a practical, general and accurate model, for core loss calculations in case of nonsinusoidal voltage waveforms. His model is applicable to metallic and non-metallic core material and to low and high frequency excitations.

Some models were developed taking Steinmetz's as basis. This is the case of the Modified Steinmetz Equation (MSE), presented in [99] and based on the idea that core losses depend on the flux density variation speed (dB/dt). Another model is the Generalized Steinmetz Equation (GSE), which supposes that core losses are dependent of the instantaneous value of flux density (B) and its variation speed (dB/dt). In order to take into account the time-history of the flux waveform, method iGSE (Improved GSE), presented in [100], proposes the substitution of the instantaneous value of the flux density to its peak-to-peak value. In this last approach, loss calculation is segmented and it takes into account minor and major hysteresis cycles. Reference [100] shows good agreement between core losses calculated by iGSE and measured ones, for nonsinusoidal flux density.

III.2.3.3 High Frequency Flux Density Calculation

The application of any of the methods shown in the last sub-section depends on the determination of the flux density flowing in the core. Some of the methods require the peak or the instantaneous value, while others depend on the time derivative. Hence it is fundamental to find out the waveforms of the flux flowing in an ICT core.

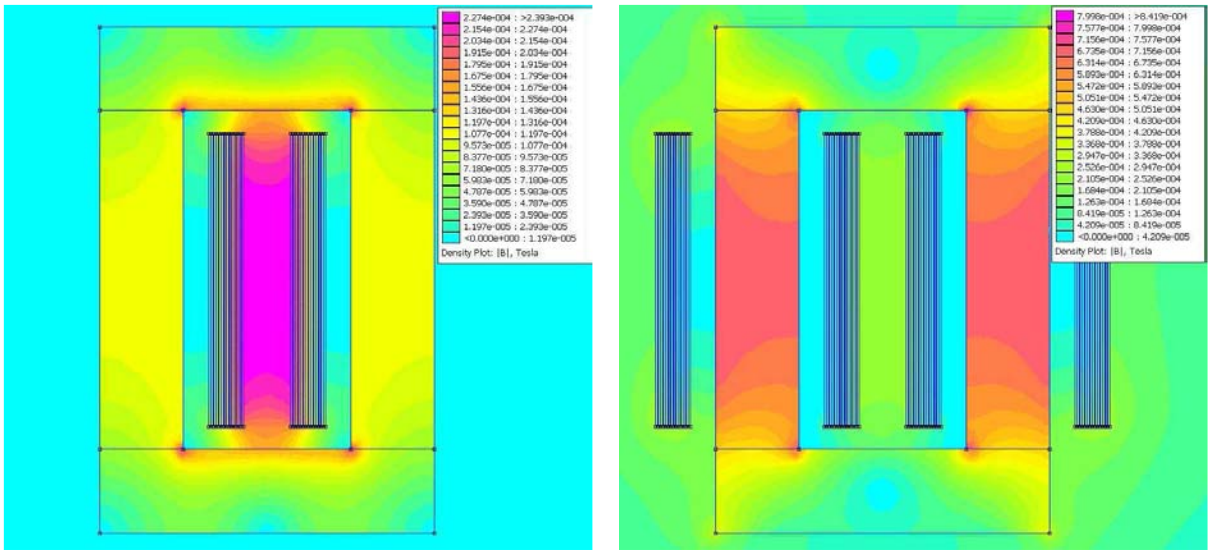
First we will recall the relations concerning magnetic flux (ϕ), the magnetomotive force (MMF), current (I), voltage (V), reluctance (Rel) and the number of turns of a winding (N_t). It is shown in equation (III-27).

$$MMF = N_t \cdot I = Rel \cdot \phi$$
$$V = -N_t \cdot \frac{d\phi}{dt} \qquad \text{(III-27)}$$

Then a magnetic circuit of the ICT must be chosen in order to determine the fluxes flowing in each part of the core. Depending on the ICT topology, different magnetic circuits may be used.

Flux is more uniform inside the core for ICTs where the core encloses all the winding, which is close to the case of Figure III.2c and Figure III.2d. For cases where there is an important part of the winding outside the core window (Figure III.2a and Figure III.2b), the flux induced by the voltage applied across the winding will only entirely exist in the wound leg of the core. This fact is shown in Figure III.15 where FEMM simulation results show the magnetic flux density for the case where the core encloses all the winding (Figure III.15a) and when there is a part of the winding outside the core window (Figure III.15b). It should be noted that since all core legs have the same cross section, the flux in Figure III.15a is

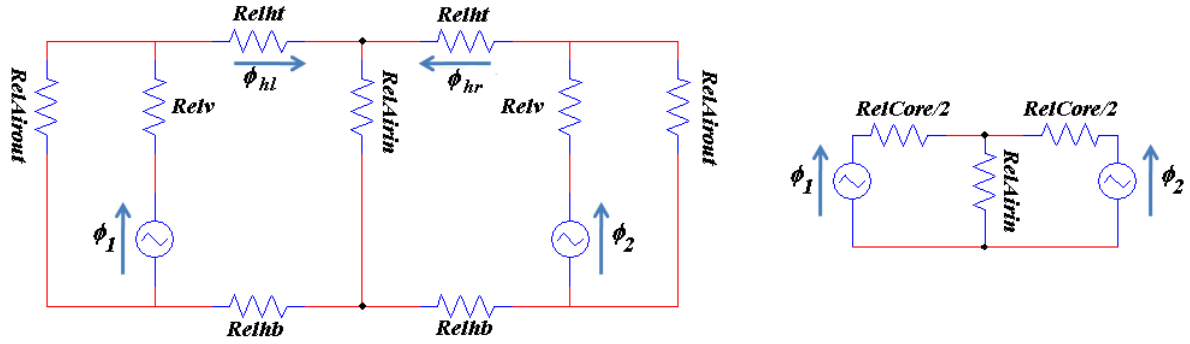
approximately the same in the whole core while in Figure III.15b the flux is much higher in the wound legs than in the horizontal legs.



a) Conductors only inside the core window *b) Conductors inside and outside the core window*

Figure III.15: Flux density distribution inside ICT.

To calculate the flux flowing in the ICT, we will start by a more general case which makes use of a magnetic circuit to model transformers having a significant part of the winding outside the core window (Figure III.16a). Later this general model will be simplified to consider transformers having almost the entire winding surrounded by magnetic material (Figure III.16b).



a) General case *b) Simplified model*

Figure III.16: Reluctance models of the ICT magnetic circuit.

In the model of Figure III.16a, reluctances *RelAirin* and *RelAirout* are related to the whole leakage energy stored in the air between the windings and in the air outside the ICT, respectively. These reluctances can be calculated by using the high frequency leakage inductances $L_{leakhfout}$ and $L_{leakhfin}$, presented in Sub-Section III.2.2.1, as shown in the equations below. *Relv* is the reluctance of each wound vertical legs and *Relht* and *Relhb* are half the reluctances of the top and bottom horizontal legs respectively.

$$RelAirin = \frac{N_t^2}{L_{leakhfin}} \tag{III-28}$$

$$RelAiriout = \frac{N_t^2}{\left(L_{leakhfout} / 2\right)} \tag{III-29}$$

Flux "sources" ϕ_1 and ϕ_2 carry a flux which results of the voltage applied across each winding. Taking Figure III.1 as an example, we can see that since the output voltage (V_o) is practically continuous, there are rectangular voltage waveforms across the windings and so fluxes ϕ_1 and ϕ_2 are both triangular (but phase-shifted of 180° as imposed by the control signals of the two cells).

If the core reluctances are much smaller than the equivalent air reluctances (*RelAirin* and *RelAirout*), the top and bottom horizontal legs are almost equipotential and both fluxes are added up through the three air reluctances in parallel. The magnetomotive force across these reluctances is imposed across both windings which imposes AC currents I_1 and I_2 to have practically the same amplitude, same phase and a fundamental frequency equal to twice the switching frequency.

When taking the general case (Figure III.16a), fluxes ϕ_1 and ϕ_2 flow only through the wound legs. To calculate the flux flowing in the left and right horizontal legs (ϕ_{hl} and ϕ_{hr} respectively), the magnetic circuit must be solved. If we consider that the core reluctance is much smaller than the equivalent air reluctances, these fluxes are equal to:

$$\phi_{hl} = \phi_1 - \frac{\mathrm{Re}\,lAirin}{\mathrm{Re}\,lAirout + 2\cdot\mathrm{Re}\,lAirin}(\phi_1+\phi_2) \quad \text{and} \quad \phi_{hr} = \phi_2 - \frac{\mathrm{Re}\,lAirin}{\mathrm{Re}\,lAirout + 2\cdot\mathrm{Re}\,lAirin}(\phi_1+\phi_2) \tag{III-30}$$

Fluxes ϕ_1 and ϕ_2 can be calculated as follows:

$$\phi_1(t) = \frac{\int (V_1 - V_o)dt}{N_t} \quad \text{and} \quad \phi_2(t) = \frac{\int (V_2 - V_o)dt}{N_t} \tag{III-31}$$

Their amplitude can be written as:

$$\phi_1 = \phi_2 = \frac{\alpha(1-\alpha)E}{(2F_s N_t)} \tag{III-32}$$

And the amplitude of the high frequency flux density flowing through the wound legs of a 2-cell ICT is given by:

$$B_p = \phi_1 / A_s = \phi_2 / A_s = \frac{\alpha(1-\alpha)E}{(2F_s N_t A_s)} \tag{III-33}$$

where A_s is the core's cross-section area.

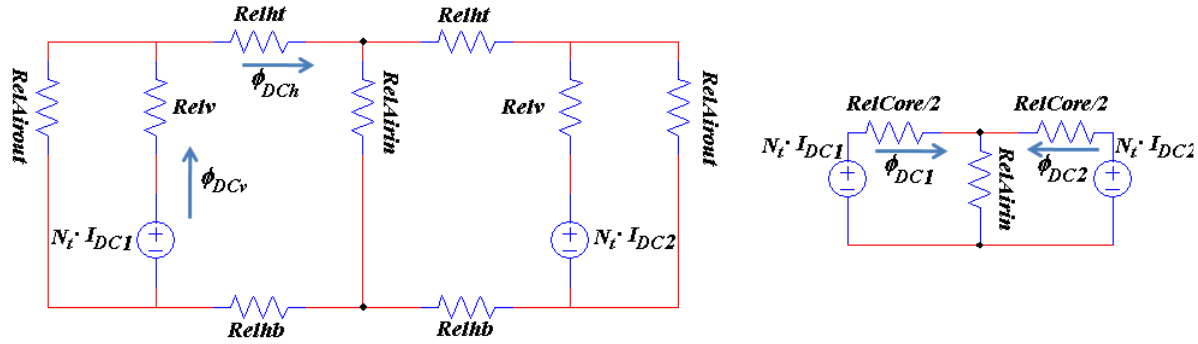
For the simplified circuit of Figure III.16b, since there is no energy outside the core window, *RelAirout* is made infinite and the reluctances of the legs are combined so that *RelCore/2 = Relht+Relv+Relhb*, where *RelCore* is the total core reluctance.

In a first version of the design tool, the flux density was calculated using equation (III-33) and the core losses were estimated using this flux density. Later versions used a more realistic flux waveform based on the reluctance model. Such a waveform can be used to calculate core losses using more accurate models, but despite a high research effort and an abundant litterature in this field, we believe that there is still some work to be done to obtain such models.

III.2.3.4 Low Frequency Flux Density Calculation

The same simple magnetic circuits may be used to estimate the DC or low frequency flux flowing through the core. DC or low frequency load current (I_{DC}) depends mainly of the load and not actually of the ICT. As a consequence, the magnetic circuits of Figure III.17

represent this case where we see now the magnetomotive force (*MMF*) generated by the winding currents.



a) General case *b) Simplified model*

Figure III.17: Simplified model of the ICT magnetic circuit for DC or low frequency current.

For balanced systems, DC currents of both commutation cells (I_{DC1} and I_{DC2}) have the same value which is equal to half the load current. If we analyze the circuit of Figure III.17a, the DC flux in the wound leg (ϕ_{DCv}) and the DC flux in the horizontal leg (ϕ_{DCh}) may be calculated as follows if we consider that the core reluctances are negligible:

$$\phi_{DCh} = \frac{N_t \cdot I_{DC}}{4 \cdot RelAirin} \tag{III-34}$$

$$\phi_{DCv} = \frac{N_t \cdot I_{DC}}{4} \cdot \frac{2 \cdot RelAirin + RelAirout}{RelAirin \cdot RelAirout} \tag{III-35}$$

Note that if there is a current difference (ΔI_{DC}) between the two windings, an extra DC flux (ϕ_e) will circulate in the core. If the equivalent air reluctances (*RelAirin* and *RelAirout*) are much greater than the core reluctances, this extra DC flux can be approximated by:

$$\phi_e = \frac{N_t \cdot \Delta I_{DC}}{2 \cdot Relht + 2 \cdot Relhb + 2 \cdot Relv} = \frac{N_t \cdot \Delta I_{DC}}{RelCore} \tag{III-36}$$

By this equation, note that the higher the permeability of a core material, the smaller the core reluctance; as a consequence, the current imbalance must be as small as possible to keep the core out of the saturation region.

It should be noted that equation (III-34) can be used to calculate the DC flux for the simplified model. However, if the core reluctances are not negligible, the DC fluxes are given by:

$$\phi_{DC1} = \phi_{DC2} = \frac{N_t \cdot I_{DC1}}{2 \cdot RelAirin + RelCore/2} = \frac{N_t \cdot I_{DC}}{(4 \cdot RelAirin + RelCore)} \tag{III-37}$$

An important observation which must be made here is that maximum flux density in an ICT is the combination of the DC and high frequency flux density calculated above. The designer must choose the core material and cross section and the number of turns so the material supports this flux density.

III.2.3.5 Core Material

Core losses are calculated after estimating high frequency and DC fluxes and using one of the core loss models presented above. The model used to estimate losses is chosen according to available information related to the material and core, either provided by

manufacturers or acquired by previous experimentation. The choice of the material is strongly influenced by the application and final objective.

Figure III.18 shows an approximate relative region for each core material in a comparative plot where one of the axes stands for saturation flux density of the material and the other axis stands for the core loss density at a specific frequency and flux density amplitude. Figure III.19 gives an idea of the frequency range where each material could possibly be used and their relative cost per unit volume.

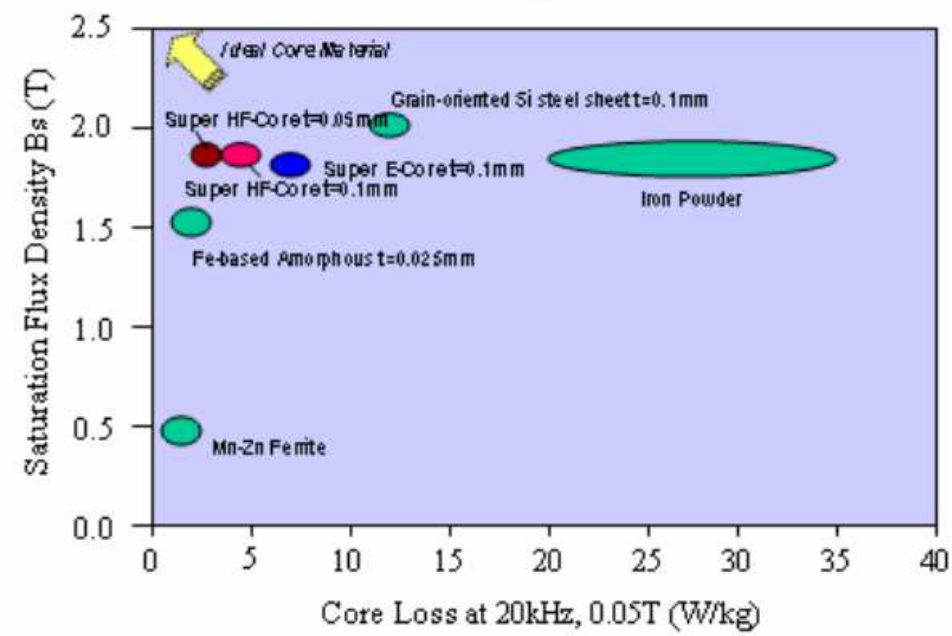


Figure III.18: Comparison between core materials with regard to saturation flux density and core loss density.

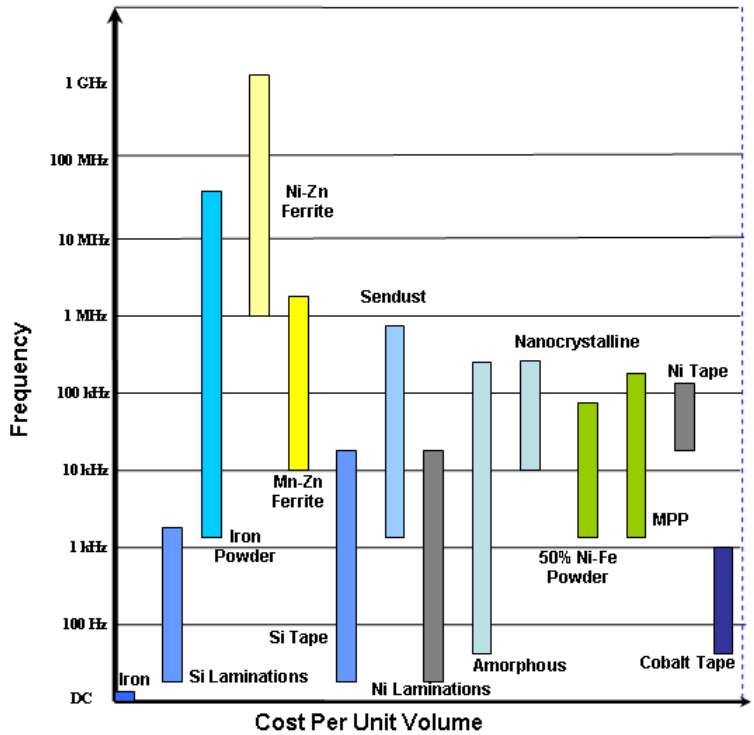


Figure III.19: Comparison between core materials with regard to operation frequency and relative cost per unit volume.

Based on these figures, if the objective is to reduce the cost of the ICT, low cost materials such as ferrites and some iron power are usually used. On the other hand, ICTs using this type of material will not achieve the highest power density. The use of ferrite usually leads to lower core losses (when compared to iron powder) although they are usually bulky since the saturation flux density in this type of material is relatively low (between 0.15T and 0.6T) [24].

Having the minimization of the ICT weight as the main objective, more expensive material achieving higher performance could be chosen. Nanocrystalline and amorphous cores are examples of this type of material. Usually they support higher flux density values and generate less core losses.

In order to choose the core, it is obvious that the designer has to take into account core shapes, price, availability, operation frequency and other specificities of the application for which the ICT is being designed.

III.2.4 Thermal Aspects

This is one of the most important aspects in an ICT design although it is less studied. In the presence of core and copper losses, the temperature of a magnetic component is a function of several parameters such as: the ambient temperature, the exchange surface, the component volume, the color of the materials used in the component's fabrication, the air flux around the component, among others.

In an ICT, transformer or inductor design, the most important temperature-related parameter which must be calculated is the temperature rise of all their composing parts. The temperature rise is the difference between the final temperature of the component and the ambient temperature. Acceptable values of temperature rise usually depend on the maximum ambient temperature defined by the application and the maximum temperature supported by the composing parts, such as core cases or copper insulation.

In order to calculate this temperature rise, some thermal models are used to analytically predict the temperature of magnetic components [51][101] but their complexity hinders their utilization in an optimization process [102]. Other conventional methods are commonly used in the literature and will be evoked in this sub-section.

In [51], the author estimates the surface temperature (T_s) of the magnetic component by using a derivation of the Stefan-Boltzmann law which calculates T_s based on the ambient temperature (T_∞), the total radiation surface (S) and the surface emissivity (ε).

The concept of thermal resistances is used by several authors. In [103][104][105], the temperature rise (ΔT) of a transformer is calculated as follows:

$$\Delta T = R_{th} \cdot P_t \tag{III-38}$$

where R_{th} is an equivalent thermal resistance of the whole transformer and P_t represents the total losses dissipated by this transformer.

Another model applies Newton's law of cooling to result in an overall effect of convection. Like this the temperature rise is calculated using the total losses of the transformer, the total surface and a thermal exchange coefficient (or convection heat transfer coefficient) H_{exc} which usually depends on several parameters such as the ambient

temperature, atmospheric pressure, component orientation, size of the surface *S*, among others. The temperature rise equation is shown below:

$$\Delta T = {P_t}/{S \cdot H_{exc}} \qquad \text{(III-39)}$$

The calculation of the thermal exchange coefficient is a tricky task. In [51], the author calculates this coefficient to include the effect of forced air velocity *v* as follows:

$$H_{exc} = 4.54 + 4.1v \qquad \text{(III-40)}$$

In the ICT design presented here, we decided to adopt the model described by equation (III-39). The total surface of the ICT is calculated taking into account the entire surface which is contact with the air. Obviously a precise calculation of this surface is not possible since real components have complex forms (specially those using conductors with round cross-section) and the real surface depends on the manner and on the spaces left during technical winding process. Note that this model supposes that the winding and the core are thermally connected and that the temperature in the entire ICT is the same.

III.3 N-Cell ICTs

As mentioned in Chapter I, applications where very high current is needed make use of interleaved converters where the number of parallel commutation cells is sometimes greater than 2. In this case, an N-cell ICT is to be used in applications where *N* commutation cells are available. The typical diagram is shown in Figure III.20, where a basic DC chopper is used as an example of interleaved converter. Since *N* cells are interleaved, usually a small leakage inductance of the ICT is enough to keep the current ripple at a level determined by the designer.

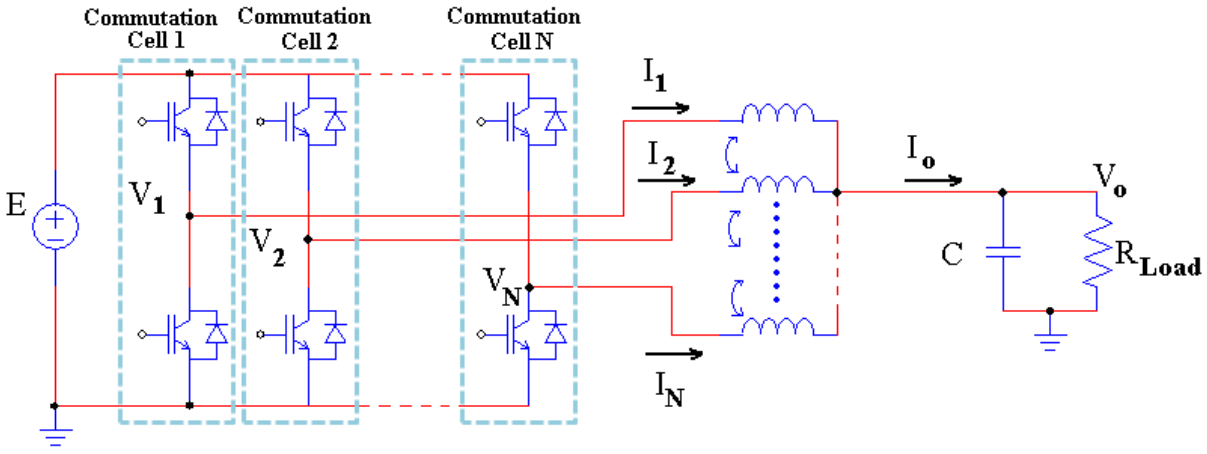


Figure III.20: N-phase intercell transformer used in an N-cell interleaved converter.

The N-cell ICT may be constructed in a monolithic component or using several separate 2-cell ICTs. The design of both options is a little different and it will be shown separately.

III.3.1 Separate 2-cell ICTs

When using separate ICTs, different topologies are possible and the most popular were shown in Figure I.17. Analysis presented in [32] show that cyclic cascade topology (Figure I.17c) is an interesting topology since it makes use of few transformers and some of its characteristics may be improved by permuting the order of the commutation cells. The design of *N* separate ICTs will be explained for this topology but the design for the others is quite similar.

III.3.1.1 Cyclic Cascade 4-cell ICT

As an example, let's take the 4-cell converter coupled by 4 x 2-cell cyclic cascade ICTs shown in Figure III.21 as the reference to our analysis.

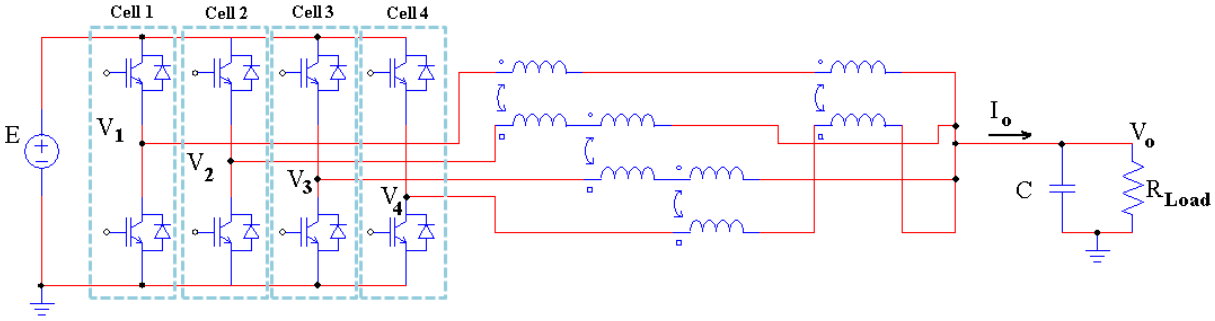


Figure III.21: 4-cell interleaved converter coupled by 4 x 2-cell ICTs (cyclic cascade topology).

Note that Cell1 is magnetically coupled with Cell2 and Cell4, and since these two cells are coupled with Cell3, all the cells are coupled together.

III.3.1.1.a Copper losses calculation

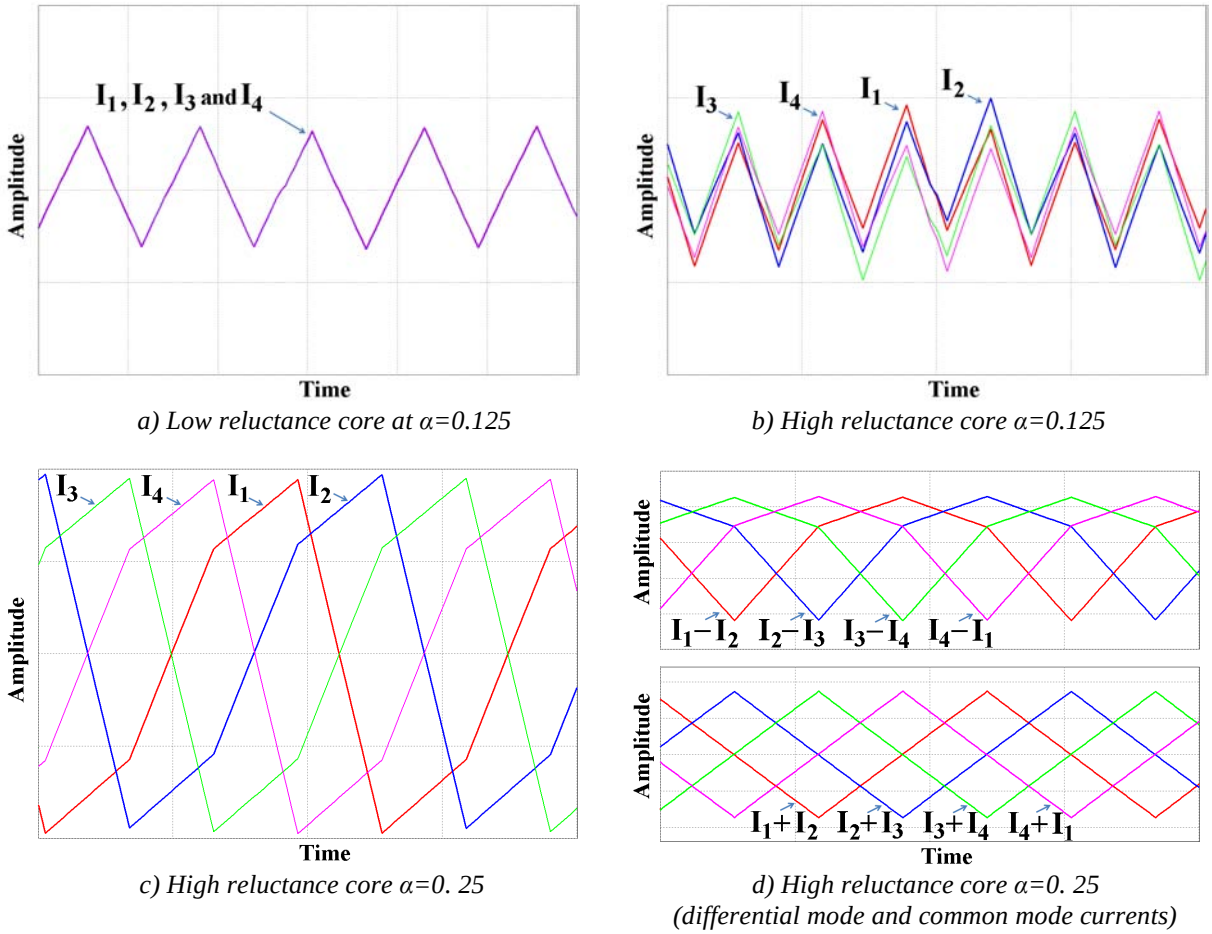
The same analysis presented in Sub-Section III.2.1 can be used for this case. Differential mode and common mode currents must be calculated in order to estimate total losses. In a low reluctance N-cell ICT, common mode current has a triangular waveform flowing at *N* times the switching frequency. Differential mode current is important when the ratio between the core reluctance and the equivalent leakage reluctance is high. When using high reluctance cores, differential and common mode currents have complex waveforms as shown in Figure III.22

If using FEM software which only allows sinusoidal current simulation, Fourier analysis may be applied to study the ohmic losses in conductors flowing non-sinusoidal currents.

Both the differential mode current and the common mode current must be decomposed into Fourier series, and simulation for each important harmonic must be carried out. As explained for the 2-cell case, 4 equivalent AC resistances should be calculated: $R_{ACeqintDM}$, $R_{ACeqextDM}$, $R_{ACeqintCM}$ and $R_{ACeqextCM}$.

The total high frequency copper losses are calculated by using these resistances and the amplitude of the fundamental of the differential mode current and of the common mode current as shown in equation (III-6).

Low frequency copper losses may be calculated in the same way as for the 2-cell converter. The use of FEM simulation must be considered for cases where low frequency currents flow through a very flat conductor.



a) Low reluctance core at α=0.125

b) High reluctance core α=0.125

c) High reluctance core α=0. 25

d) High reluctance core α=0. 25 (differential mode and common mode currents)

Figure III.22: Currents in the 4 cells of a 4x2-cell ICTs.

III.3.1.1.b Leakage inductance calculation

A converter with a high number of interleaved commutation cells in parallel needs less inductance in the filtering stage to attain an acceptable output current ripple.

The leakage inductance of each 2-cell ICT may be calculated in order to predict the flux flowing in the material and the current ripple. The calculation is the same as the one shown in Sub-Section III.2.2. If the winding is surrounded by core material, equation (III-14) may be used. However if there is a part of the winding outside the core window, 2D or 3D FEM simulation must be used in order to precisely estimate leakage inductance related to this part. This is shown in Sub-Section III.2.2.1.

The question in this section is: how to use these calculated and simulated leakage inductances (L_{leak}) to predict current and flux ripple in an N-cell ICT?

To simplify the analysis, a model first shown in [106] will be used. The equivalent circuit is shown in Figure III.23 where an instantaneous power converter is used to average the voltage of all the commutation cells. Total leakage inductance (L_{leakT}) is the sum of each individual leakage inductance of each 2-cell ICT. Inductors L_{eq} are related to the magnetizing inductance, but the current they flow is not the differential mode current. The differential mode current is half the difference of the currents of two commutation cells wound in the same transformer. For cases where high permeability cores are used, L_{eq} becomes very high and negligible current flow through these inductors.

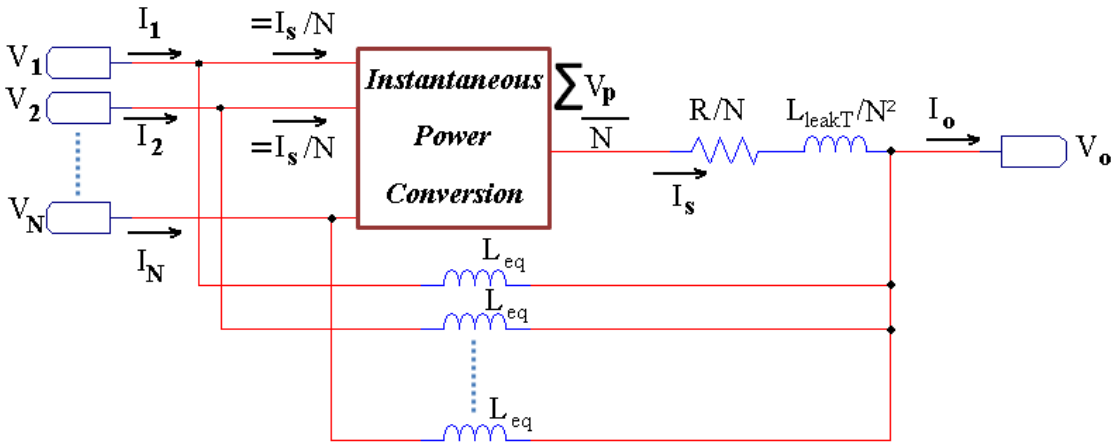


Figure III.23: Equivalent model of a symmetric ICT composed by N cells.

In the case where L_{eq} is very high, the output current can be calculated as:

$$I_o = \frac{\int\left(\sum V_k - V_o\right)dt}{N\left(L_{leakT}/N^2\right)} = \frac{\int\left(\sum V_k - V_o\right)dt}{L_{leak}} \qquad \text{(III-41)}$$

If we define the common mode currents as the currents entering the block Instantaneous Power Conversion, the common mode current is always given by:

$$I_{CM} = \frac{\int\left(\sum V_k - V_o\right)dt}{N \cdot L_{leak}} \qquad \text{(III-42)}$$

Differential mode currents can be approximated by

$$I_{DM}(k,k+1) \approx \frac{(I_{Leq_k} - I_{Leq_{k+1}})}{2} = \frac{\int(V_k - V_o)dt - \int(V_{k+1} - V_o)dt}{2 \cdot L_{eq}} = \frac{\int(V_k - V_{k+1})dt}{2 \cdot L_{eq}} \qquad \text{(III-43)}$$

In order to calculate copper losses, the peak-to-peak common mode and differential mode currents flowing through the ICT should be calculated. The common mode current peak-to-peak value is shown in the equation below for the buck converter having *N* cells in the cyclic cascade topology:

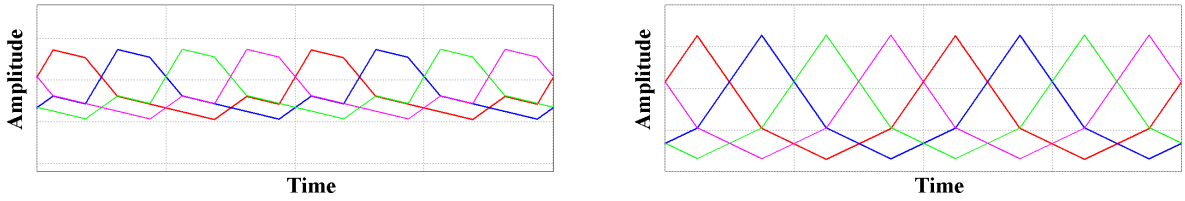
$$I_{CM} = \frac{\alpha'(1-\alpha')E}{\left(N^2 F_s L_{leak}\right)} \qquad \text{(III-44)}$$

III.3.1.1.c Core loss calculation

The same core models can be applied to calculate core losses in an N-cell ICT. The main difference is the fact that flux waveforms change when comparing to a 2-cell ICT used in a 2-cell buck.

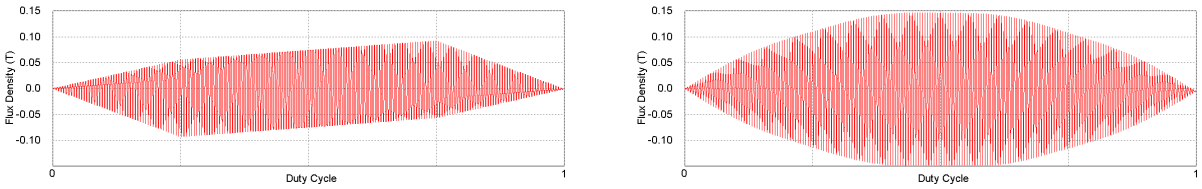
For the 2-cell case, the high frequency flux flowing through the core has only triangular waveform when the load has capacitive characteristics. However, as shown in [24], the flux is quite different when more than 2 commutation cells are used.

For the example of Figure III.21, the flux density in an ICT has the waveform shown in Figure III.24a and b, for duty cycle equal to 0.125 and 0.25 respectively. In Figure III.25a, duty cycle is swept from 0 to 1 and the flux density inside the same ICT is shown. It is compared to the flux density in a 2-cell ICT used in a 2-cell buck converter at the same conditions (frequency, DC bus voltage and duty cycle sweeping).



a) α=0.125 *b) α=0.25*

Figure III.24: Flux density waveforms in a 2-cell ICT inserted in a 4-cell Buck converter.



a) In a 4-cell buck converter *b) In a 2-cell buck converter*

Figure III.25: Flux density waveforms in a 2-cell ICT inserted in a 4-cell and 2-cell Buck converters.

Note that the flux in an ICT put in a 4-cell interleaved buck has a peak-to-peak flux twice smaller than the flux in the same ICT inserted in a 2-cell buck operating at the same conditions. In [24], the flux reduction variation regarding the number of cells is presented for the case of sinusoidal fluxes. However, since most of the applications of ICTs are in converters having commutation cells, we decided to present it for the case of Buck converters. Table III-6 shows the variation of the maximum peak-to-peak flux (ϕ_{maxN}) in a 2-cell ICT used in a N-cell buck converter compared to maximum peak-to-peak flux (ϕ_{max2}) in a 2-cell ICT used in a 2-cell buck converter (equation (III-32)). The same comparison is also shown for sinusoidal fluxes.

Number of commutation cells	**2**	**3**	**4**	**5**	**6**	**7**
$\phi_{maxN} / \phi_{max2}$ **(sinusoidal fluxes)**	1	0.577	0.707	0.85	1	1.154
$\phi_{maxN} / \phi_{max2}$ **(Buck converter)**	1	0.5	0.5	0.66	0.833	0.908

Table III-6: Ratio of the peak-to-peak flux in N-cell and 2-cell ICTs.

This table confirms that the higher the number of commutation cells, the higher is the peak-to-peak flux flowing in 2-cell ICTs. This is a major drawback when increasing the number of commutation cells [6]. The case with 2 commutation cells seems a bad solution when compared to the other cases, but it is not. Actually, in a converter with 2 commutation cells only one 2-cell ICT is necessary while in a converter with *N* commutation cells, *N* times 2-cell ICTs are needed.

If the core material used has mainly hysteresis losses and a simple core loss model is used, the peak-to-peak flux may be used. Thus Table III-6 associated to equation (III-32) may be used to predict this flux.

Concerning low frequency or DC flux, the same analysis of Sub-Section III.2.3.4 may be used. The only difference is the fact that the current of each commutation cell is now equal to the output current divided by the number of commutation cells. Thus, the equation for the DC flux of the simplified magnetic circuit shown in Figure III.17b can be calculated as:

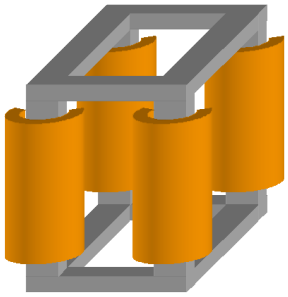
$$\phi_{DC} = \frac{N_t \cdot I_{DC}}{N \cdot \left(2 \cdot RelAir + RelCore/2\right)} \qquad \text{(III-45)}$$

Concerning the choice of the core material and the temperature rise calculation, the same discussion and formulae presented before may be applied.

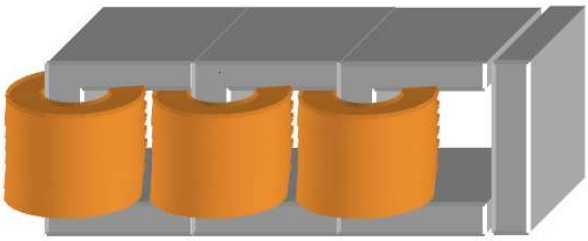
III.3.2 Monolithic N-cell ICTs

In a monolithic ICT, all the windings connected to commutation cells share the same magnetic core. Compared to separate ICTs, monolithic have some advantages and disadvantages. The main drawback is the complexity of construction of such a component. However the main gain is the reduction of the flux flowing in the material as it will be explained shortly.

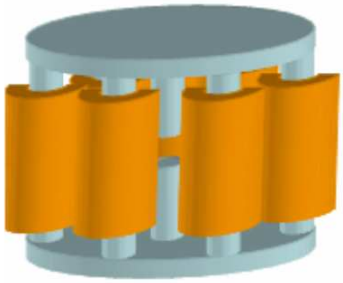
Main topologies are shown in Figure III.26 while in Figure III.27 we show a 4-cell converter coupled by 4-cell double ladder ICT (or also called here the "CUBE" ICT, Figure III.26a). This circuit will be the reference to our analysis. Note that, for this case, all the commutation cells are magnetically coupled together.



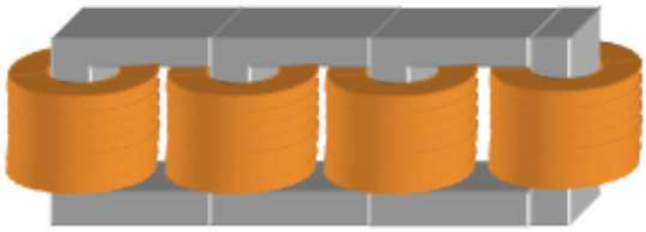
a) Double Ladder



b) Ladder with guided leakage flux



c) Symmetric core with central leg



d) Ladder with distributed leakage flux

Figure III.26: Different topologies of monolithic InterCell Transformers.

In order to calculate copper losses, leakage inductances and final ICT temperature, the same models and procedures described for N x 2-cell ICTs may be used. They were presented in Sub-Section III.3.1.1. The only comment is related to FEM simulations performed to estimate alternative resistances and leakage inductances. If 3D FEM simulation is available, precise values for resistances and inductances will be obtained. Otherwise, 2D FEM simulation must be used and some approximations may be admitted.

Figure III.28 suggests the 2D geometries which must be simulated for each monolithic topology. The results of the AC resistance and leakage inductance per unit length simulated for the part outside the core window, inside the core window and inside it but close to an airgap (Figure III.28c and d) must be multiplied by its corresponding conductor's length (either outside, inside or inside close to airgap) in order to calculate the total AC resistance and leakage inductance.

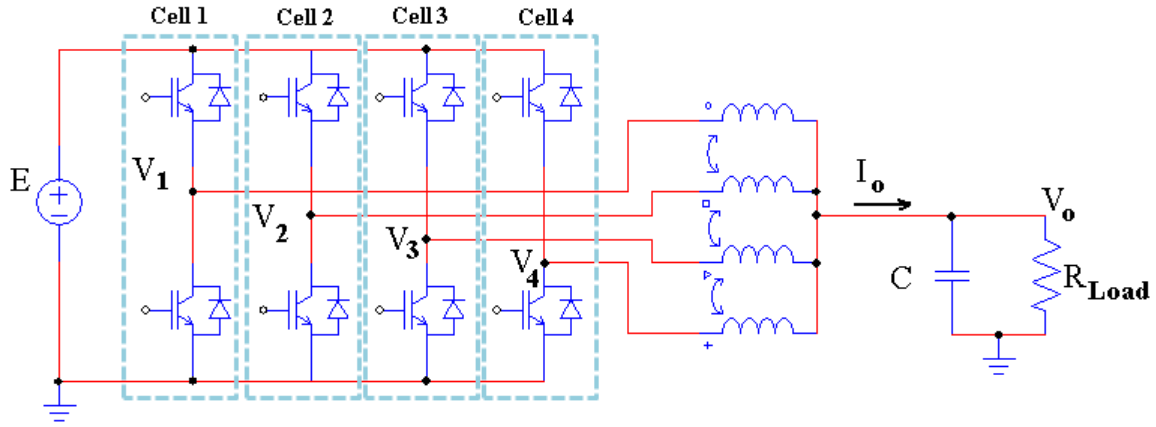


Figure III.27: 4-cell interleaved converter coupled by a 4-cell ICT (monolithic topology).

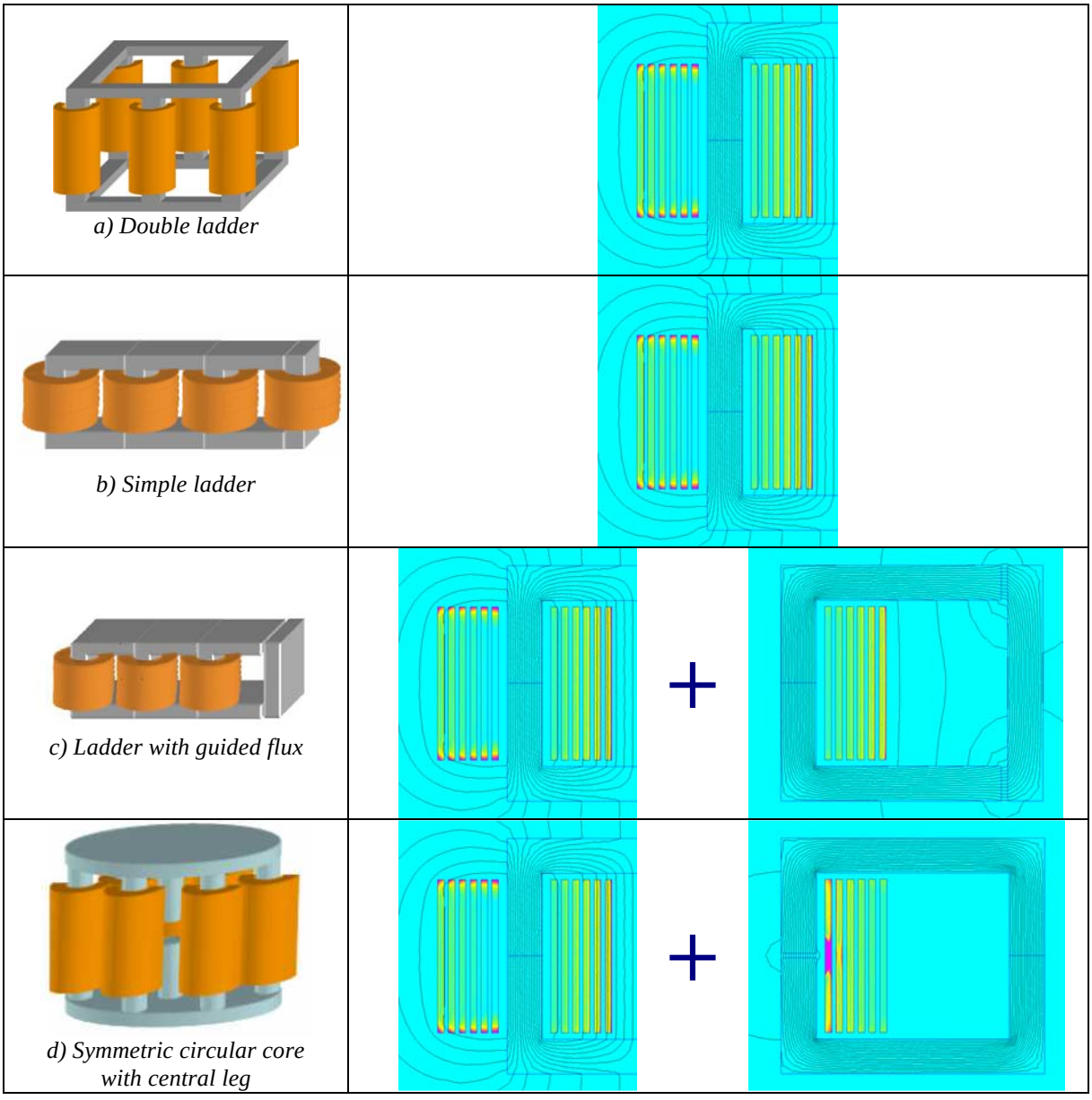


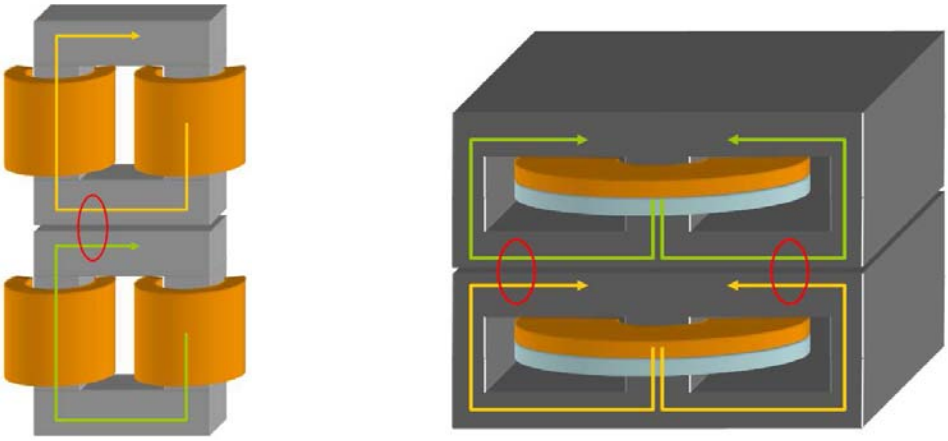
Figure III.28: 2D FEM simulations approximated for predicting AC resistance and leakage inductance.

III.3.2.1 High and Low Frequency Flux Calculation

In monolithic ICTs as the ones shown in Figure III.26, the flux in the wound leg has a triangular waveform and it can be calculated the same way as made for the 2-cell ICT used in converters with 2 commutation cells, as shown in equation (III-31). However, for the circular symmetric and double ladder topologies, the flux in the transversal legs (legs connecting the wound legs) is equal to the ones calculated for separate ICTs. In [6][24], authors show the equivalence between separate and monolithic ICT.

If monolithic ICTs are made by joining together separate ICTs, there some ways of doing that which will reduce either the magnetizing or the leakage fluxes. If we glue together two magnetic circuits, the flux on the joined legs will be summed and the reduction of the flux will be more important if the flux circulating in these legs are equal in magnitude and have opposite signs.

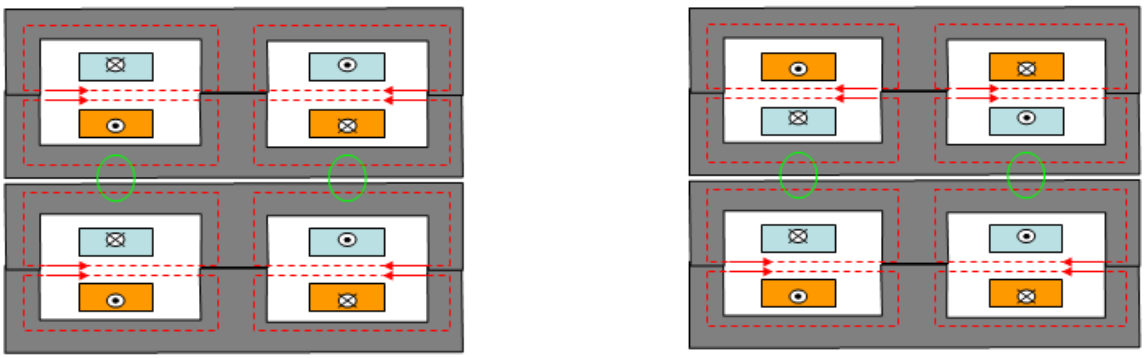
Using separate cores of Figure II.17a and c, there are some ways of joining them in order to reduce the magnetizing flux of the joint leg. This is shown in Figure III.29.



a) ICTs with UI cores *b) ICTs with E cores*

Figure III.29: Compensating magnetizing flux by joining transformers together.

To explain the leakage flux reduction, let's use the case of Figure III.29b. Figure III.30a illustrates the lines of leakage flux associated with each coil. We can see that in this case there is an addition of leakage flux in the joint column.



a) Leakage flux addition *b) Leakage flux compensation*

Figure III.30: Leakage flux addition or reduction.

In a two winding transformer, coils can be swapped without changing the magnetizing flux. So, as shown in Figure III.30b, after a permutation of coils of a transformer, we obtain leakage flux compensation in the column. This aspect is very interesting in the case of intercell transformers, because the continuous components of the flux circulate mainly in the leakage reluctances. Thus, the compensation of the leakage flux also results in the cancellation of continuous components of the flux in the joint legs.

III.3.2.1.a Permutation of commutation cells

Based in the separate/monolithic equivalence and in the fact that flux reduction occurs when joining fluxes with the same magnitude and phase-shift as close as possible to 180°, authors in [24] propose the permutation of adjacent commutation cells in order to reduce the flux in the transversal legs. There is an optimal permutation depending on the number of commutation cells, as presented in [6]. This technique was already patented by researchers of the 3DPHI project [29].

Table III-7 is created by showing the variation of the maximum peak-to-peak flux (ϕ_{maxN}) in a 2-cell ICT used in an N-cell buck converter compared to maximum peak-to-peak flux (ϕ_{max2}) in a 2-cell ICT used in a 2-cell buck converter with the number of cells *N*, before and after using optimal permutation [6].

Number of commutation cells	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
ϕ_{maxN} / ϕ_{max2} **(before permutation)**	0.5	0.5	0.66	0.833	0.908	1	1.142	1.3	1.393	1.5	1.636
ϕ_{maxN} / ϕ_{max2} **(after permutation)**	0.5	0.5	0.5	0.611	0.5	0.5	0.5	0.58	0.5	0.5	0.5

Table III-7: Ratio of the peak-to-peak flux N-cell and 2-cell ICTs in transversal legs after optimal permutation.

It is interesting to note that optimal permutation keeps the high frequency flux in the transversal legs close to half the flux in the wound legs even when the number of commutation cells increases. It means that no oversizing of the transversal leg section is necessary when designing a monolithic ICT.

III.3.2.1.b Low frequency flux

A simple magnetic circuit may be used to estimate the DC or low frequency flux flowing through the core. If we take the "CUBE" as the reference ICT, its equivalent magnetic circuit may be represented as the one shown in Figure III.31. By the symmetry of this circuit, it is clear that low frequency flux in the transversal legs (which flows through *RelCoreh* in the figure below) is less than half the flux in the wound legs. Analyzing the circuit in balanced mode (I_{DC1}=…=I_{DCN}), the DC flux in the wound legs of an N-cell double ladder ICT may be calculated as follows:

$$\phi_{DC} = \frac{N_t \cdot I_{DC}}{N \cdot \left(RelCorev + RelAirout\,//\,(RelCoreh + RelAirin)\right)} \tag{III-46}$$

The flux in the horizontal legs (ϕ_h) may be calculated with the following formula

$$\phi_h = \frac{\phi_{DC}}{2} - \frac{\left(\frac{N_t \cdot I_{DC}}{N} - \phi_{DC} \cdot RelCorev\right)}{2 \cdot RelAirout} \tag{III-47}$$

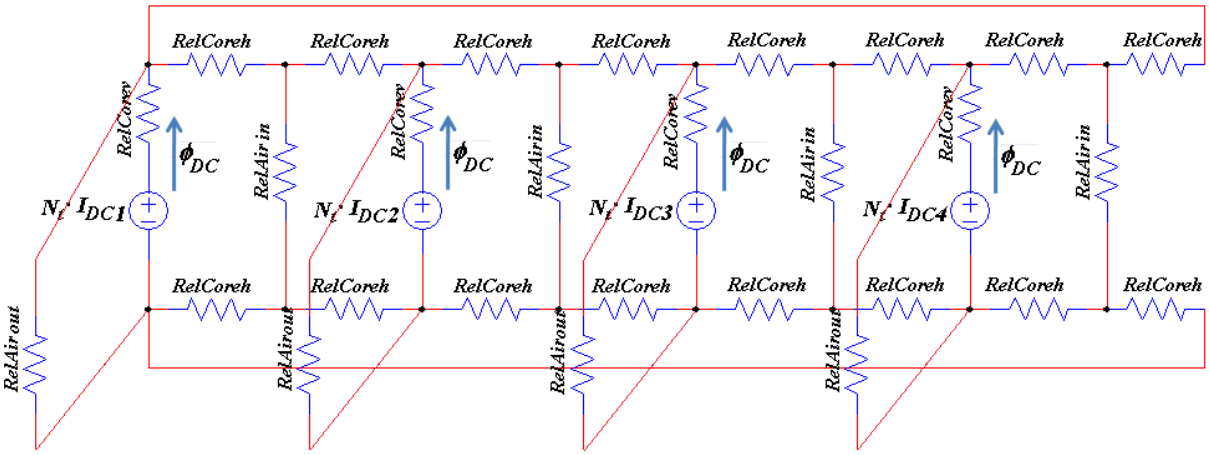
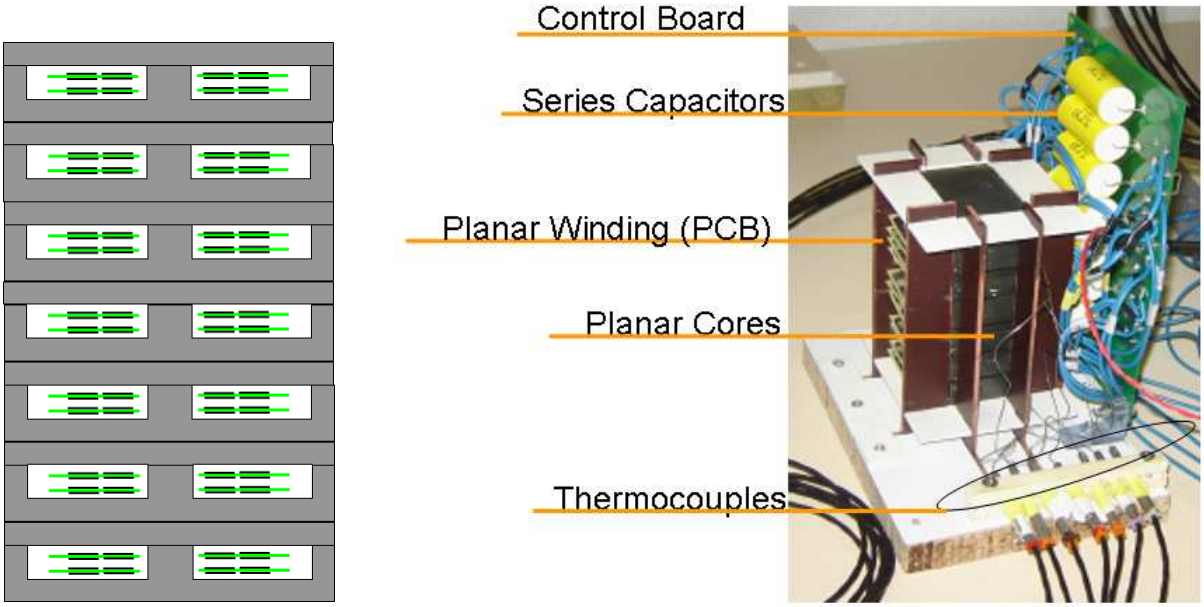


Figure III.31: Magnetic circuit of the CUBE ICT for DC or low frequency current.

III.3.2.2 Existing Monolithic ICTs

Some monolithic ICTs were developed in our research group. Three of them were designed during the PhD thesis of Valentin Costan. Two of them were realized and tested. The first one, called "Basso Cambo" is a 7-cell ICT constructed by assembling 7 ferrite cores of type E and 7 of type PLT, as shown in Figure III.32a. A photograph of the constructed ICT with the electronic board used to obtain experimental results is shown in Figure III.32b. This ICT was built in order to evaluate core losses and the temperature behavior in these magnetic components stacked this way.



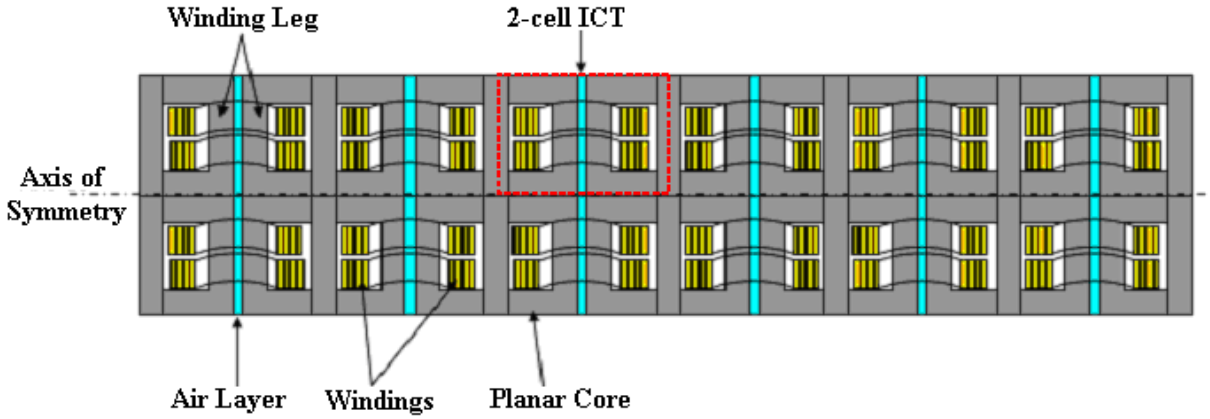
a) Cores assembling *b) Prototype*

Figure III.32: "Basso Cambo" ICT built to evaluate core losses.

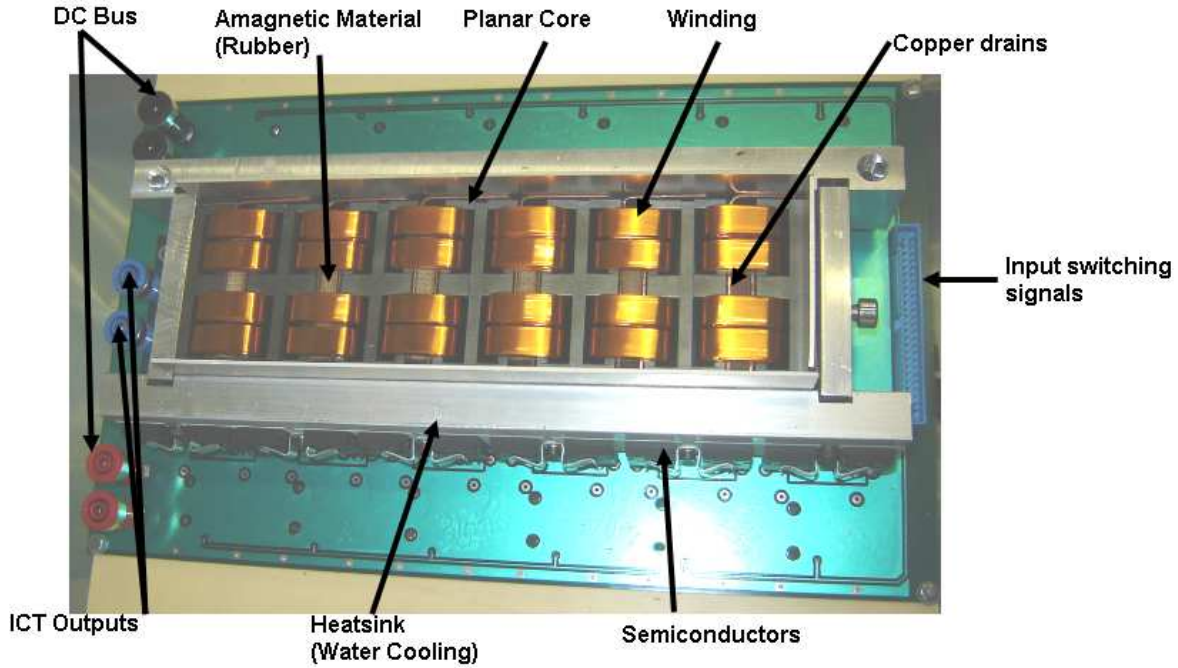
The second ICT was proposed having in mind some objectives, such as: to build a compact high power converter containing many interleaved cells; to employ a topology of intercell transformers based on standardized cores which are easy to cool; to carry out tests to compare the efficiency of the converter using commutation cells regularly phase-shifted or using an optimal permutation.

The ICT was built by joining together separate ICTs as shown in Figure III.33a. It was constructed having 12 cells intended to be used as 2 separate 6-cell ICTs in a buck converter operating in the "opposition method". It comprises 24 windings since it has 12 cells connected to 12 separate ICTs. This ICT was called "LEEI" and it was assembled by using 12 cores of E type and 7 cores of PLT type.

The results given in [24] demonstrate the reduction of total losses when applying optimal permutation of commutation cells. The balance of the cell currents has been experimentally verified for the system in the "6x6" configuration (opposition method).



a) Core and winding assembling

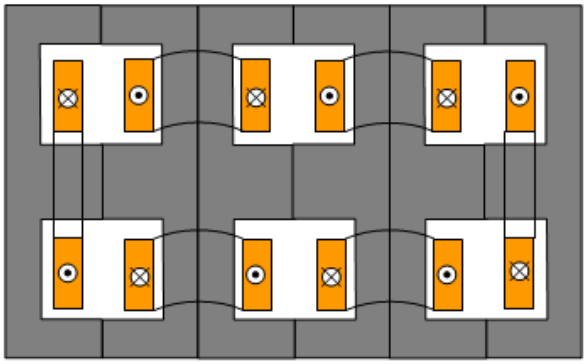


b) Prototype

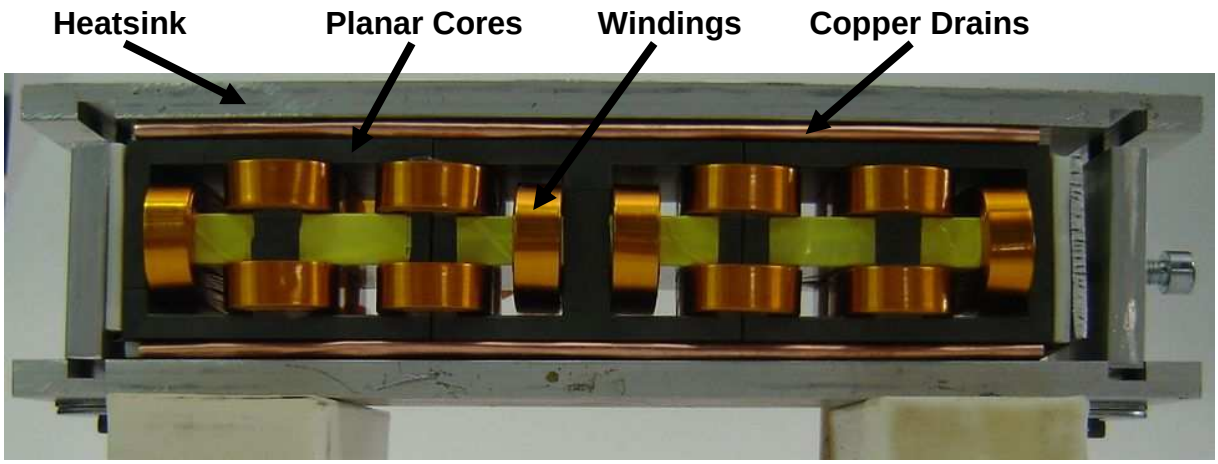
Figure III.33: "LEEI" ICT.

The third was built during the present thesis. The "MONOBOBINE" ICT is a 2-dimmensional version of a double ladder topology. Two 6-cell ICTs were constructed in order to be used with the same converter used to test the last ICT. Each ICT is composed by 6 windings wound either in vertical or horizontal direction, using 6 ferrite cores of E type, as shown in Figure III.34a.

Figure III.34b presents the real ICT assembled in the laboratory. Note that one 6-cell ICT was placed side-by-side with the other one and that they are magnetically coupled. 12 E-cores were used to construct this ICT but they were placed in a horizontal position, different from the drawing of Figure III.34a where the E-cores have vertical position.



a) Core and winding assembling



b) Prototype

Figure III.34: "MONOBOBINE" ICT.

Experimental results when using this ICT are shown in Figure III.35. Currents of the 6 commutation cells are shown as well as one of the switched voltages (bright green trace) and the DC bus voltage (blue trace). Note that each current has a triangular shape at 6 times the switching frequency. Also, small differential mode currents are observed.

Core reluctance is not comparable to the equivalent air reluctance and so it is not the reason why current differences are perceived. Actually this is due to imperfections when cores were assembled together. Since the E-cores are not perfectly equal, when joining them together by all different surfaces, the mechanical connections are not perfect, causing undesired airgaps. These airgaps cause flux imbalance inside the cores and that is why we could not attain the rated values for which the ICT was designed. When DC bus voltage and DC current were increased, more important differential mode current was observed, such as the one shown in Figure III.36a, until a moment where one core leg clearly saturates and high current peaks are detected as the one in Figure III.36b. Simulations inserting some airgaps in this structure confirm the current imbalance experimentally observed.

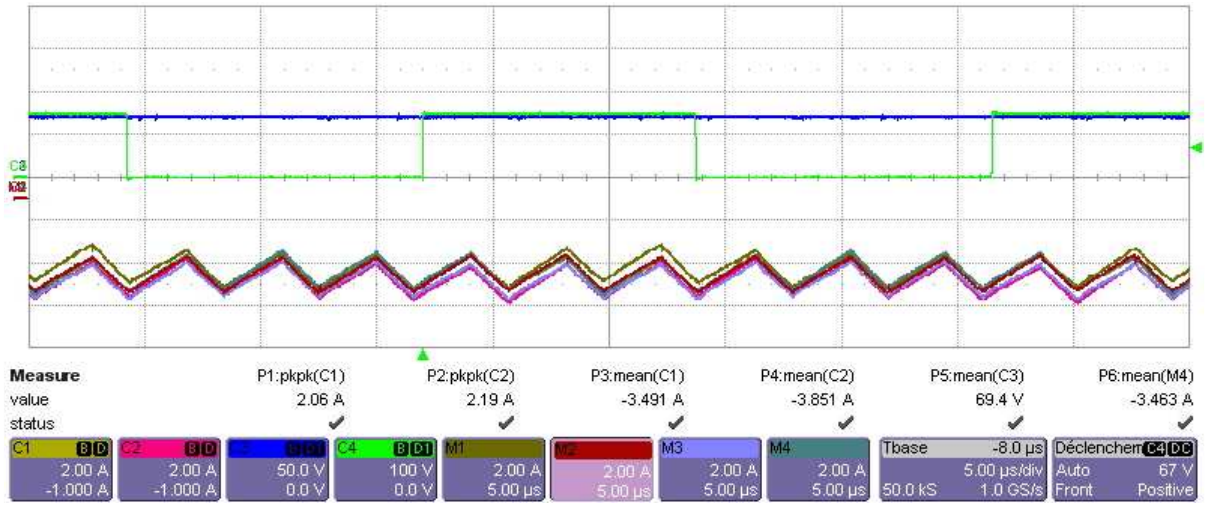
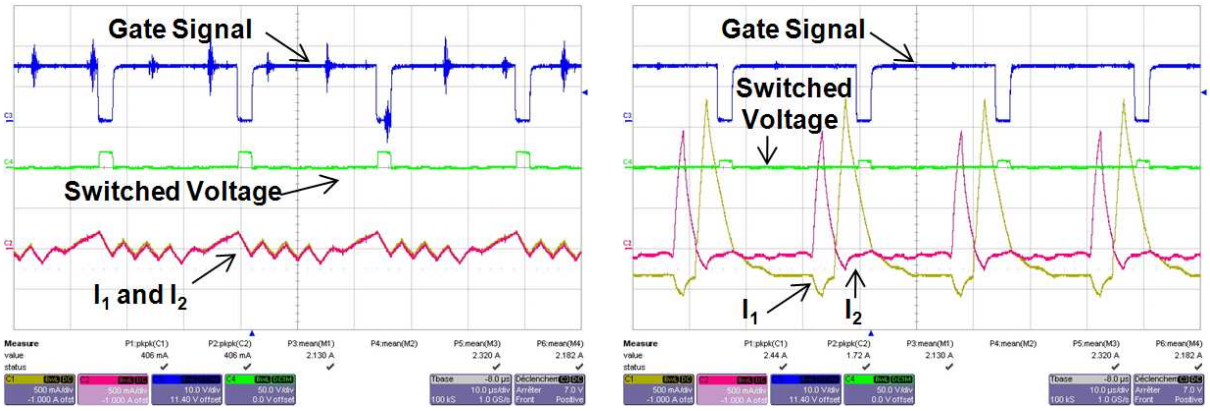


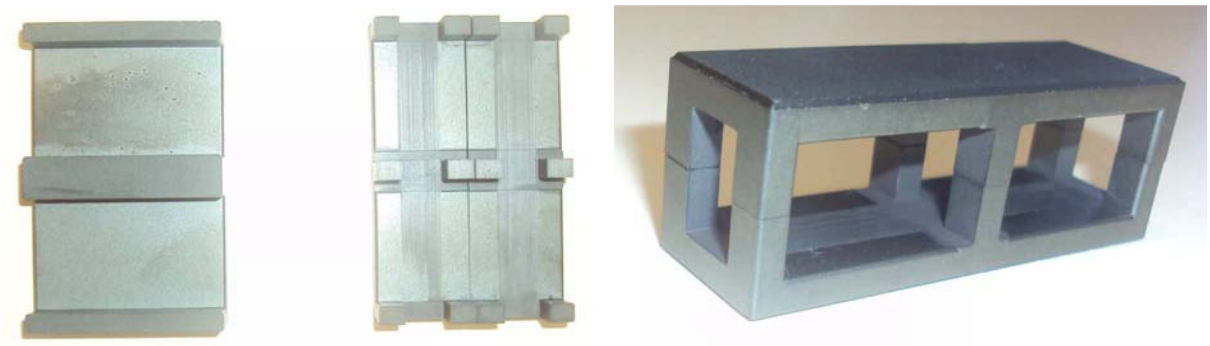
Figure III.35: Currents in the 6 commutation cells.



a) Low DC current *b) Higher DC current*

Figure III.36: High differential mode current and core saturation.

With the purpose of eliminating this type of problem, monolithic ICTs could be constructed from a unique magnetic piece. Machining a magnetic material block is a hard task. In our laboratory we could machine an E-core E58/11/38 made of ferrite material 3F3 in order to form a 6-cell double ladder ICT as shown in Figure III.37. In this structure, only the top and bottom parts are joined and imperfections could appear in the wound legs. This is less problematic than the airgaps in the MONOBOBINE ICT since these imperfections could be uniform in the 6 legs, causing differential mode currents but no current imbalance. For the moment, only the core is machined. Winding construction and experimentation will be made in the future.



a) Before and after machining *b) 6-cell ICT core*

Figure III.37: E-core machining to create a 6-cell monolithic ICT core.

The last monolithic intercell transformer presented here is a CUBE ICT (4-cell double ladder topology). This ICT, which is shown in Figure III.38, was designed and constructed by CIRTEM for high current applications, using many concepts presented in this chapter. It will be used in a 100V-to-200V boost converter having input current of 500A and switching frequency of 18kHz.

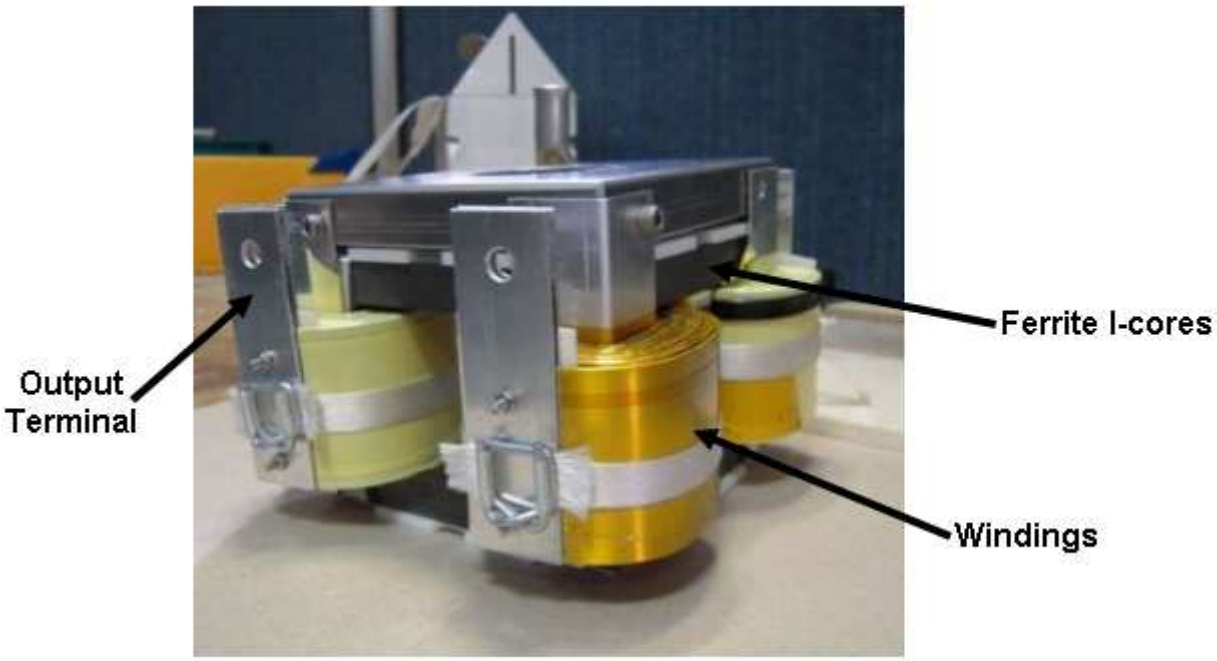


Figure III.38: CUBE ICT designed and constructed by CIRTEM.

III.4 Conclusions

ICT design involves phenomena which are quite similar to those described for inductor or transformer design, but the design process is quite different. The objective of this design depends on the application where the ICT will be used. Usually the goal is to minimize volume, weight, price or losses, or a combination of them.

Either more precise or more inaccurate models may be used to represent all the existing phenomena, depending on the required accuracy and the available time to complete the design.

In this section a more general design was explained taking into account 4 main aspects: copper losses, core losses, flux density saturation and thermal calculation. First the design of 2-cell ICTs used in converters having 2 commutation cells was presented. Later the design of N-cell ICTs (either separate or monolithic) used in an N-cell converter was compared to the 2-cell case and the differences were explained.

Regarding copper losses, we have presented a method based on 2D FEM simulations which precisely estimates AC resistances for all the frequencies related to the current flowing through a commutation cell. This method is much faster than making use of 3D FEM simulations and it takes into account the differences between the AC resistance outside and inside the core window. In an ICT, common mode currents have triangular waveforms at N times the switching frequency while differential mode currents may have or not triangular waveforms, but it has fundamental frequency equal to the switching frequency. Also it was shown that conductors having an excellent form factor regarding high frequency effects may have poor performance at lower frequencies, such as currents at 50Hz or 60Hz, when placed outside the core window of an ICT.

In general both copper and core losses depend on the leakage inductance of an ICT and that is why it should be precisely predicted. For this matter, we have also presented a leakage inductance calculation method based on 2D FEM simulations. Experimental results confirm the accuracy of this method.

Concerning core loss calculation, some models were evoked. Waveforms and amplitudes of high frequency flux were investigated. When the load has capacitive characteristic, the flux waveform is in 2-cell ICTs is triangular and depends on the duty cycle. In an N-cell ICT, the flux waveform has a more complicated shape. In this transformer, changing the order of connections between the commutation cell and the ICT, flux reduction and consequently core loss reduction is observed.

Core saturation depends on the high and low frequency fluxes. High frequency flux depends mainly on the voltage applied to the ICT terminals while the low frequency flux depends on the low frequency current, core reluctance and mainly the equivalent air reluctance which is inversely proportional to the leakage inductance. Obviously, the sum of both fluxes must be inferior to the product of the core's saturation flux density and cross section.

Depending on the ambient temperature, the maximum temperature rise of the ICT may be chosen so the conductor insulation or the core material is capable to support it. The temperature rise is estimated using a model based on the calculation of the total ICT surface which is in direct contact with the air. The ICT temperature can be calculated by using a thermal exchange coefficient (based on experimental practice or empirical formulas) and the total losses dissipated by the winding and the core.

Next chapter will show how to use all the models and equations presented in this chapter in an optimization process with the aim of minimizing the ICT weight, volume, price or total losses.

Chapter IV

InterCell Transformer Optimization

IV.1 Introduction

Depending on the field of application, designing an "optimal ICT" has a very different meaning. For example, ICTs for converters in satellites should be as light as possible since the price to place a certain payload into orbit is very high.

If the ICT is designed for high-current low-voltage VRMs to be used in servers or telecommunication switches and routers, the designer's main concern will probably be the efficiency. In other cases, reducing cost is the main requirement.

The optimization routines described in this chapter allow minimizing one of these characteristics. Multi criteria optimization is not addressed but could be derived using the models presented here.

In the previous chapter we have shown various models used to calculate copper and core losses, temperature rise and the flux inside ICTs. In this chapter we will choose and use some of these models to create a number of optimization algorithms which can be used to find the best ICT for a certain application, regarding a certain objective. In these routines, more or less sophisticated models will be used resulting in different trade-off between speed and accuracy.

IV.1.1 Choosing the Software for the Optimization

Choosing the software or softwares to be used is not an easy task. We would like to use softwares we are familiar with, which are user-friendly, fast and accurate, which include database type functions, graphical user interface, powerful calculation functions and optimization routines, 3D visualization, Finite Element Analysis.... Things get more complicated when we add the need to share these routines with people from different institutions or companies.

As a first step we were quite happy to discover that many of the tasks listed above could be handled by Excel which is definitely a widely accepted software! The first routines have therefore been developed in Excel using the solver function.

We later moved to MATLAB mainly for reasons of "readability" and because it is easier to control FEMM and perform Finite Element Analysis as a post treatment to check the optimized result. MATLAB has also the great advantage of having an easy user-interface of calculation using complex numbers. In addition, it is very easy to deal with N-dimension matrices, which will be necessary in the optimization, as will be explained later.

IV.1.2 Choosing the Optimization Method

Given the loss models developed previously, it is quite easy to formulate the ICT design process as a single criterion optimization problem. The formulation is quite intuitive and we just have to explain what we want to do. For example, "we want to make the ICT as small as possible". But we know from experience that making it too small will cause high losses and that these losses will be difficult to evacuate because the device is small. Having a small exchange surface, the temperature will increase to an unacceptable level and the device will thus be destroyed.

This means that we need a thermal model to evaluate the temperature increase, and we need to design the ICT such that the temperature does not exceed the temperature allowed for the materials used.

One of the first questions to be considered is if we should optimize one or more objectives. The greatest problem is to tell which objective is more important than others, and especially how much important. This is why for the moment, mono-objective optimization is chosen. Later on, mono-objective algorithms developed here may be transformed on multi-objective if necessary.

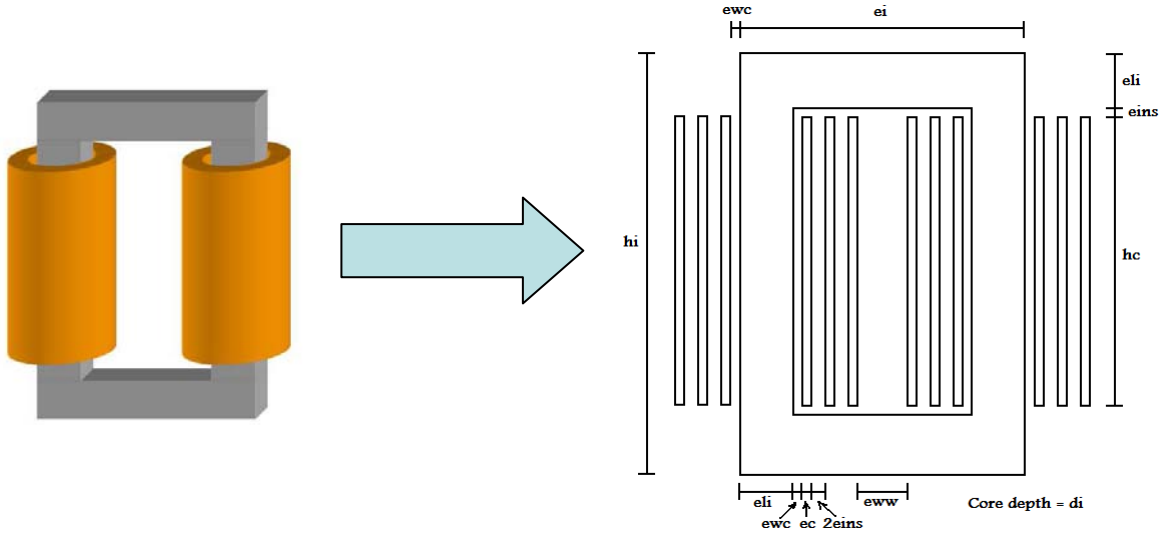
In terms of optimization problems, minimizing the ICT weight or losses seems to be a simple problem with only one optimal solution inside the solution space. Thus algorithms based on a variation of gradient methods may be used instead of using complicate and time-consuming methods based on genetic algorithms.

Since MATLAB is being used, function *FMINCON* [107] will be employed as the main function to search for the minimum value of an optimization function having non linear constraints.

IV.1.3 Choosing the Optimization Variables, Parameters, Constraints and Objectives

In this section, the design process will be described using the example of a 2-cell ICT used in 2-cell Buck converter such as the one shown in Figure III.1.

The 2-cell ICT is shown in Figure IV.1a and in Figure IV.1b the main geometrical parameters of this ICT are presented.



a) UI-core ICT *b) Geometrical parameters*

Figure IV.1: Two-cell ICT and geometrical parameters.

All the values related to the optimization problem must be organized in four groups: Variables, Parameters, Constraints and Objectives. Some of the values related to the ICT are not part of these groups; they are only intermediate values used in the calculation or final results to characterize the ICT.

We should start the approach by choosing the possible "Objectives". We can add as many as we want but the main objectives found in the industry are the minimization of total losses, weight, volume or price.

Choosing the "Variables" is a difficult task. Since it is a general optimization example, we decided to be as general as possible. Thus the geometrical parameters of the ICT may all be altered. It does not mean that all geometrical parameters shown in Figure IV.1b are considered as variables.

First of all, the maximum number of geometrical variables is the minimum number of values which describe the whole ICT, i.e. all geometrical values which are a combination of others must be eliminated. For example, core height (*hi*) is equal to the conductor's height (*hc*) plus twice the conductor's insulation thickness (*eins*) plus twice the core width (*eli*). At least one of these values may not be an optimization variable. Since *eins* and *eli* are also present in the horizontal direction, they should be considered as variables. It is not advisable to use *hi* as a variable because *hc* would be calculated as a function of the other 3 values and it might have a negative value, which has no physical meaning. On the other hand, if *hc* is chosen as a variable, *hi* is calculated as a function of the other 3 values and it will always have a positive value since the other 3 are always positive. It means that the choice of the optimization geometrical variables must be made so that no other calculated parameter has the possibility of having a negative value.

Also there are some variables which can be fixed in order to not overload the optimization process. For example, if the insulation thickness (*eins*) is an optimization variable, it is likely that this variable achieves the minimum value as possible (fixed by the voltage difference between turns) for any optimization process. So it is prudent to have this value as an optimization "parameter" and not a "variable". For similar reasons, the distance between the core and the first layer of the winding (*ewc*) should also be a parameter.

Non-geometrical variables which are important for an ICT optimization should be the number of turns (N_t) and the switching frequency of the Buck converter (F_s). Usually the higher the switching frequency, the smaller and less expensive the magnetic component. It means that the switching frequency can be considered as a variable only when the price to pay for an increase frequency is taken into account; for example, this is the case when switching losses are evaluated and global optimization of the system (Buck+ICT) is considered.

Hence, optimization variables in our example are: *ec, hc, eww, eli, di,* N_t and F_s.

Next step is to choose the "Constraints". This is a very important action since the final optimization result depends very strongly on these values. Depending on the application, geometrical constraints such as the maximum ICT height, width or depth, may be important. However there are 2 values which always need to be considered as constraints: the maximum temperature rise (*Dtmax*), and the maximum flux density in the core (*Bmax*). Constraint *Dtmax* is chosen taking into account the maximum ambient temperature defined by the application and the maximum temperature supported by the different materials (magnetic core, core cases or winding insulation). Constraint *Bmax* depends on the core material the designer will use in the optimization. It should be noted that when weight minimization is desired, it is important not to impose the value of the current ripple. We know that allowing a high current ripple gives a high RMS current and high conduction losses, and specifying a very low current ripple means an inductance with a large value and a lot of magnetic energy stored; these two extremes lead to bulky ICT/inductors and the best one is somewhere in between. Setting the maximum output current ripple (*Ioutrmax*) to a very high value allows the current ripple to vary during the optimization and it is a good practice to find the smaller or lighter ICT.

Since it is a mono-objective optimization, maximum weight, volume, price and losses may also be considered as constraints. Other constraints can be added to minimize errors or undesired consequences of poor models used in the optimization routine. For example, maximum equivalent current density (*Jmax*) flowing through the winding conductors may be used to minimize anomalies caused by the use of simple thermal model which considers a perfect thermal coupling between windings and core.

All the values used to calculate the objective function and constrained values, and which are not used as variables, must be used as fixed parameters. In our case, values related to the core and copper characteristics, to the thermal model and to the electrical circuit (input voltage, output current and duty cycle) are considered as fixed parameters. An important parameter is the "Calculation Temperature" *Tc*, which is used to calculate values related to core and copper losses. Note that in our approach the inductance value is not chosen as a parameter. Instead, leakage and magnetizing inductances are calculated based on geometrical variables and parameters.

IV.1.4 Choosing the Optimization Strategy

As explained in the last chapter, depending on the application, leakage inductance and high frequency resistance are critical parameters for the design of ICTs. Analytical formulation of the field distribution inside the window is easily obtained under the assumption that the window is rectangular and that its depth is infinite. However, real components are often far from this assumption, and the field outside the window (which cannot be easily modeled) may have a very significant contribution to the overall leakage inductance and AC resistance.

The use of 3D FEM simulation is an option to evaluate the leakage inductance and AC resistances, but it is very time consuming. On the other hand, we believe that there are a number of cases where 2D FEM simulation can give a good estimate of these two quantities. However, although 2D FEM simulations are much faster than 3D, it is sometimes impractical to make use of them inside an optimization process. The time necessary for the main optimization algorithm to call the FEM software, draw the 2D model, simulate it and acquire the resulting inductance values is enormous compared to a simple equation resolution or table reading.

For very specific applications where the optimization algorithm will run only few times, inserting 2D FEM simulation inside the optimization loop may not be a problem. In our case, algorithms are developed in a research environment and various different cases and situations will be tested.

One suggestion to speed up the optimization process is the use of approximate analytical models which can be corrected by FEM simulation at the end of each optimization [108]. To explain this method procedure, let's take the problem of calculating the ratio between the AC and DC resistance of the part of the winding outside the core window (Fr_{ext}). As we saw in chapters II and III, inside the core window Dowell's formulation (equation (II-5) which calculates Fr_{int}) can be used. However, outside the core window, no analytical formulation is found in the literature. So we could make an artificial supposition that $Fr_{ext} = K_c \cdot Fr_{int}$ and we proceed as follows:

- The first optimization is made using only analytical methods and an optimal resulting geometry is calculated.
- FEM simulation of the resulting geometry is performed.

- The simulated AC/DC resistance ratio ($Fr_{extSIMU}$) is divided by the calculated Fr_{int} and a new coefficient K_c is found.
- This new coefficient is used in the next optimization.
- This process is repeated until K_c converges to a certain value.

Usually a few iterations are enough to allow K_c to converge. In this strategy, the number of FEM simulations is the number of iterations while in the strategy which directly inserts the FEM simulation in the optimization loop, the number of simulations is equal to the number of optimization steps, which is usually very high when compared to the number of iterations. For the cases developed during this PhD thesis, the typical number of steps is usually around 150 and the typical number of iterations needed to have K_c not varying more than 1% is ten times less.

The main drawback of this strategy is the fact that it converges to an existing and exact solution (i.e. confirmed by FEM), but it is not guaranteed that it is the optimal solution.

Other strategies are even faster and more precise, but they all need a pre-simulated set of desired values in order to calculate the leakage inductance (L_{leak}) or the AC/DC resistance ratios of the part of the winding outside the core window (Fr_{ext}). In our case, results of 2D FEM simulations are stored in an N-dimensional matrix where N is the number of geometrical parameters of the magnetic device which may modify L_{leak} or Fr_{ext} (which is usually 4 or 5) plus the parameters related to the frequency and the number of turns. This makes a total of 7 or 8 dimensions as it will be explained in the next sub-chapter.

One of the strategies is based on Response Surface Method [109][110]. Another approach is based on regular fitting of the set of results in an equation which is a function of the parameters used to create the N-dimensional matrix. Polynomial fitting using least square method may be used but the main drawback is the fact that because the set of results has N dimensions, many terms and coefficients are necessary. Since we have no a priori information about the system, it is difficult to choose the variables in each term of the polynomial.

Possibly the best idea to speed up the process of obtaining the desired leakage inductance and AC/DC resistance ratios is to make a local interpolation of the values of the set of results. Lookup table reading applied to electromagnetic problems is usually employed in optimization of machines [111][112], transformers [113] and arbitrary structures [114], in the modeling of electromagnetic behavior of magnetic materials [115] and also in the calculation of currents in machines [116]. This strategy is especially interesting in cases where many different optimizations are needed, for different devices and applications, which is usually the case in the industrial environment.

Multi-dimensional linear interpolation will be explained in the next section as well as the simulations required to compose the sets of results.

IV.2 Building the Set of Responses and Multi-Dimensional Interpolation

As seen in Chapter III, it is necessary to perform one FEM simulation in order to predict the low frequency (or DC) leakage inductance used to calculate low frequency flux in the core. Another simulation is needed to calculate the same leakage inductance, but at a higher frequency, so the current ripple can be calculated.

Regarding the AC resistances, some simulations are needed depending on the current waveform. Usually 3 simulations for the common mode current and 3 for the differential mode current are enough for good approximation of the total AC resistance as explained in Sub-Section III.2.1.3.

The idea is to replace these 8 simulations by simple table reading and interpolation. Tables, also called "set of responses" (SOR), are created for each ICT topology, although some tables may be used for several topologies.

Four SOR are needed for each optimization routine. They are related to:

4. DC leakage inductance per unit length;
5. AC/DC leakage inductance ratio;
6. AC/DC resistance ratio regarding the differential mode current;
7. AC/DC resistance ratio regarding the common mode current;

All SOR may be created by using the same structure to be simulated. However, simulation of DC leakage inductance depends on fewer parameters and consequently it will be explained first.

IV.2.1 DC or Low Frequency Leakage Inductance

In our analysis we will just deal with the energy outside the core because we assume that the calculation inside the core is possible. When the calculation of the energy inside the core window cannot be done analytically, the same method described here may be used to evaluate the leakage flux inside the window.

Concerning the leakage inductance related to the energy outside the core window, we may simulate it by using the model represented in Figure IV.2. Note that both windings are represented only outside the core window and that, independently of the number of turns and conductor cross-section shape, it is represented by a rectangular conductor with N_t turns.

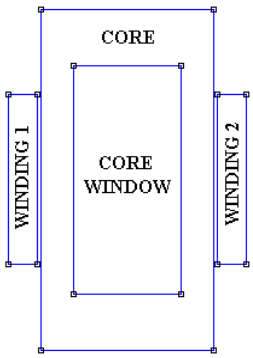


Figure IV.2: Simple model for the simulation of the energy outside the window of an intercell transformer.

In Figure IV.3 all the parameters which may change the leakage inductance are represented. By previous simulations, 3 conclusions could be stated:

1. If we shrink or expand the transformer, maintaining the ratios between all geometrical parameters shown in Figure IV.3, the leakage inductance per unit length remains the same. This is consistent with what occurs inside the core window, represented by equation (III-14). In this equation, if all geometrical dimensions (b_1, b_2, b_3, h and l_{av}) are scaled by a factor K, the leakage inductance per unit length (L_{leak}/l_{av}) does not change.

2. Leakage inductance is proportional to the square of the number of turns in the winding, independently of the shape of the core and winding. This is also coherent with what occurs inside the core window, represented by equation (III-14).
3. Parameter *F* (core leg width) has a negligible influence on the leakage inductance if it is greater than 8% of *A* (core width). This can be seen in Figure IV.4, where the leakage inductance per unit length was simulated for different values of *F* when compared to *A*. The leakage inductance does not vary more than 0.3% if *F/A* is greater than 0.08, which is usually the case for regular transformers and cores available on the market.

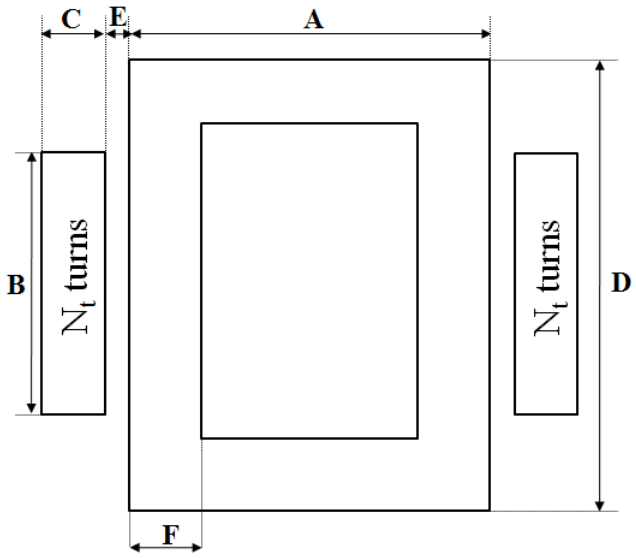


Figure IV.3: Transformer parameters.

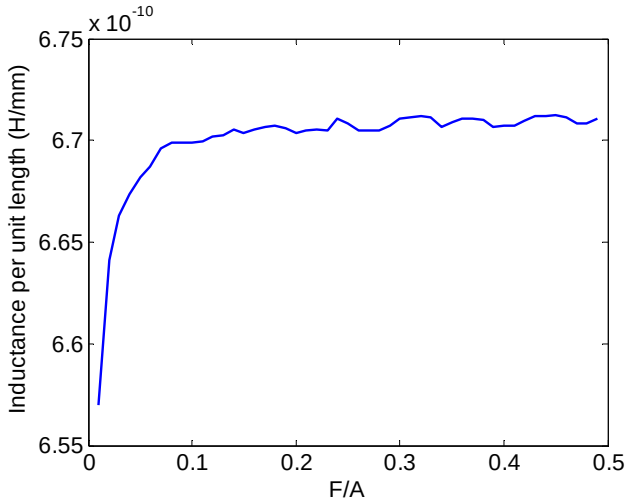


Figure IV.4: Variation of the leakage inductance per unit length with the core leg width.

By conclusions 2 and 3, we assume that parameters *F* and N_t are not essential parameters when creating the N-dimensional matrix containing the pre-calculated leakage inductance values. By conclusion 1, we observe that we just need to simulate a transformer normalized in geometry. We did it by fixing parameter *A* as the reference parameter. Parameters *C*, *D* and *E* should be related to *A*, but *B* is related to *D* since *B* can never be greater than *D*. This leads us to a SOR with 4 dimensions (*B/D*, *C/A*, *D/A*, *E/A*).

IV.2.1.1 Number of Points to be Simulated

The number of points needed in each dimension must be wisely chosen in order to minimize the interpolation error and the size of the 4-dimensional matrix. For this purpose, simulations were performed by varying each parameter at once (starting from a standard set of parameters) and using small steps. The result is shown in Figure IV.5. Note that in fact parameter *F* does not significantly modify the leakage inductance. Also, since the other curves have smooth shapes, a small number of points is needed to reliably represent the leakage inductance behavior related to the transformer geometry. The smooth behavior of the leakage inductance with the variation of geometrical parameters was also observed for various initial sets of parameters.

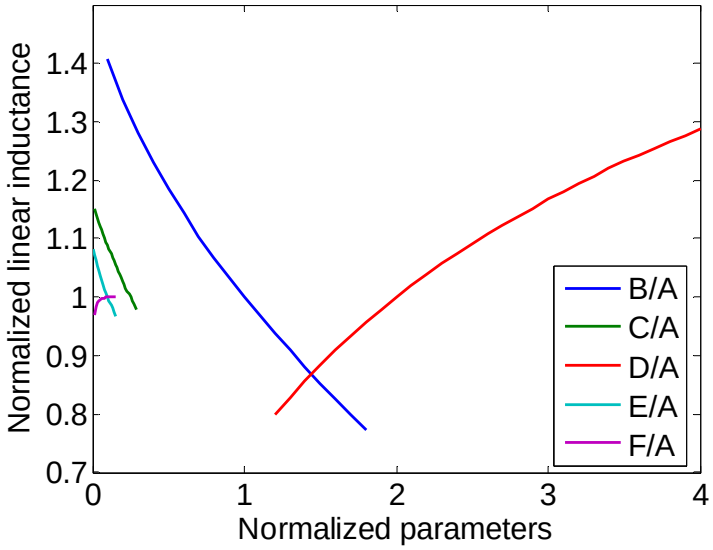


Figure IV.5: Example of variation of the normalized leakage inductance per unit length.

The number of points in each dimension was chosen to be equal to 12 in order to have a reliable representation of all reasonable core shapes. Two or three extra points were added to each dimension to extend the mapping region and include unrealistic shapes that could still be considered by the algorithm during optimization. The values of each parameter used in the matrix construction are shown below:

B/D = {0.1, 0.2, 0.3, 0.4, 0.5, 0.55, 0.6, 0.65, 0.7, 0.75, 0.8, 0.85, 0.9, 0.95, 1}

C/A = {0.001, 0.01, 0.05, 0.1, 0.1333, 0.1667, 0.2, 0.2333, 0.2667, 0.3, 0.3333, 0.3667, 0.4, 0.5}

D/A = {0.01, 0.2, 0.6364, 1.0727, 1.5091, 1.9455, 2.3818, 2.8182, 3.2545, 3.6909, 4.1273, 4.5636, 5, 10}

E/A = {0, 0.01, 0.02, 0.03, 0.04, 0.05, 0.06, 0.07, 0.08, 0.09, 0.1, 0.15, 0.2, 0.5}

Values are stored in a 15x14x14x14 4-dimensional matrix containing 41160 values. The number of FEM simulations needed is the same as the number of values in the matrix, and so simulation boundaries and mesh density must be carefully chosen so the total time to create the matrix is reasonable.

IV.2.1.2 The Influence of Mesh Generation and Simulation Boundaries

For accurate simulation of the leakage inductance due to the part of the winding outside the core, fine mesh and large simulation area are needed. This leads to high simulation time and memory requirements, which is troublesome in optimization processes.

Simulations were carried out using FEMM software in order to investigate the influence of these parameters. Figure IV.6 shows an example of simulation to calculate $L_{leaklfext}$, where simulation boundaries are rectangular. Table IV-1 shows the variation of the number of nodes, the total simulation time and the calculated $L_{leaklfext}$ with the ratio between the total simulation area and the area occupied by the transformer (*Asimu/Atransfo*). All simulations were performed with a very high mesh density. The last column compares the calculated $L_{leaklfext}$ to the most accurate result (which is simulated with the largest area). Note that when the total simulation area is greater than 81 times the transformer area, the error in the leakage inductance calculation is less than 2% but it takes a relatively long time (around 11 seconds).

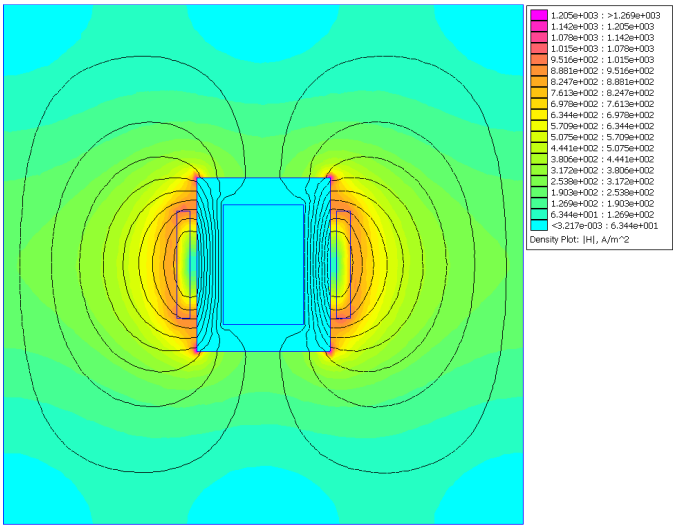


Figure IV.6: FEMM simulation of intercell transformer with rectangular boundaries (magnetic field intensity).

Asimu/Atransfo	Number of nodes	Simulation time (s)	Linear inductance (µH/m)	L/Lmax
9	5980	1.57	0.6654	0.8252
36	24323	4.62	0.7697	0.9545
81	55552	11.37	0.7904	0.9803
144	98514	21.80	0.7976	0.9892
225	154776	38.71	0.8018	0.9944
324	221667	59.46	0.8032	0.9962
441	301219	85.90	0.8044	0.9977
576	394215	122.91	0.8049	0.9982
729	498975	160.50	0.8061	0.9997
900	616652	206.51	0.8063	1.0000

Table IV-1: Simulated leakage inductance with rectangular simulation boundaries (fine mesh).

Table IV-2 also shows the variation of the number of nodes, the simulation total time and the calculated $L_{leaklfext}$, but now for simulations using round boundaries. Note that results are almost the same as in Table IV-1 but they are slightly more precise than using rectangular boundaries.

Asimu/Atransfo	Number of nodes	Simulation time (s)	Linear inductance (µH/m)	L/Lmax
9	5981	1.77	0.6766	0.8389
36	24377	4.82	0.7726	0.9579
81	55458	11.07	0.7920	0.9820
144	98104	22.32	0.7990	0.9907
225	153334	38.00	0.8021	0.9945
324	220846	58.86	0.8038	0.9967
441	300743	86.49	0.8049	0.9980
576	391767	121.07	0.8054	0.9986
729	495594	160.89	0.8062	0.9996
900	610968	209.49	0.8065	1.0000

Table IV-2: Simulated leakage inductance with round simulation boundaries (fine mesh).

The influence of the mesh density in the simulation is presented in Table IV-3. The maximum distance between 2 nodes was changed as shown in the first column (*Dtransfo/Dnodes*). It shows the ratio between the minimum transformer dimension (either the height or the width) and the maximum distance between 2 nodes. Simulations were performed for a round boundary with simulation area equal to 4 times the transformer total area. Using a maximum distance between 2 nodes 25 times smaller than the transformer dimension causes an error less than 1% and the simulation is fast.

Dtransfo/Dnodes	Number of nodes	Simulation time (s)	Linear inductance (µH/m)	L/Lmax
1	515	0.76	0.6607	0.9702
4	547	0.76	0.6624	0.9726
9	999	0.76	0.6669	0.9792
16	2386	0.77	0.6713	0.9856
25	5532	0.97	0.6762	0.9929
36	11313	2.28	0.6786	0.9964
49	20685	4.36	0.6797	0.9980
64	34834	7.21	0.6804	0.9990
81	55850	11.84	0.6808	0.9995
100	84456	19.21	0.6811	1.0000

Table IV-3: Simulated leakage inductance with variation of maximum distance between two nodes (round boundary, Asimu/Atransfo=4).

Comparing these 3 tables we observe that good trade-off between a simple, precise and fast simulation may be achieved if two different mesh regions are defined: one small region having fine mesh which simulates the greatest part of the energy and one larger region having coarse mesh which takes into account the rest of the energy. Table IV-4 shows the results of two simulations where the larger boundary was chosen so the ratio between the total simulated area and the transformer area is equal to 441 and the maximum distance between 2 nodes is 25 times smaller than the smallest transformer dimension. Both simulations are fast and precise (error smaller than 1% when compared to the most precise simulation) and this technique is suitable to be used in an optimization process. Figure IV.7 shows the mesh distribution for this case having *Asimu/Atransfo*=9 for the small region.

Asimu/Atransfo (small region)	Number of nodes	Simulation time (s)	Linear inductance (µH/m)	L/Lmax (round Simu)
9	7004	1.73	0.8033	0.9961
2.25	1938	0.72	0.7994	0.9912

Table IV-4: Simulated leakage inductance with 2 round simulation boundaries (Asimu/Atransfo=441, Dtransfo/Dnode=25).

If we need to simulate the leakage inductances due to the part of the winding inside the core, it is not affected by the total simulation area since the leakage energy due to the conductors inside the core is entirely contained inside the winding area. This is valid if we

assume that the core does not have relative permeability smaller than 200, for less than 1% of leakage inductance calculation error. On the other hand, this simulation is affected by the maximum distance between 2 nodes in the same way as shown in Table IV-3.

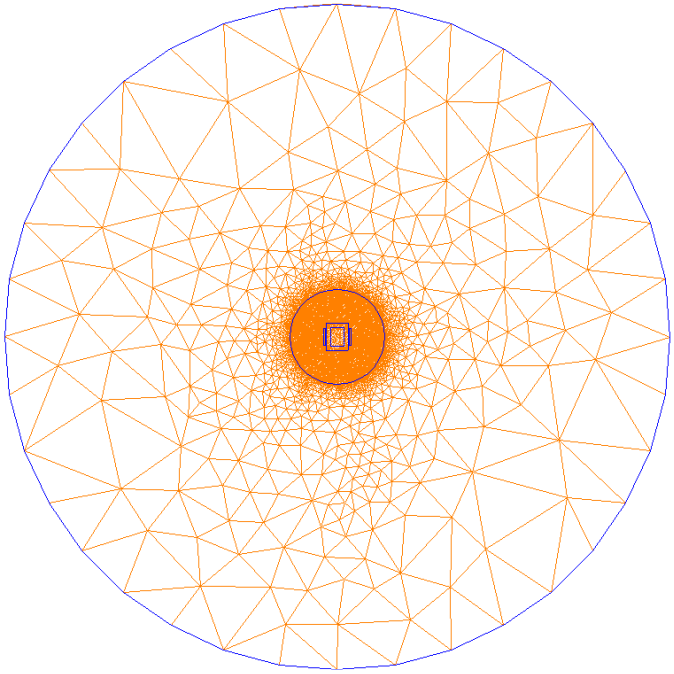
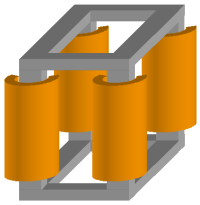
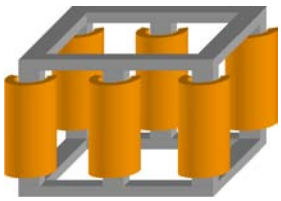


Figure IV.7: Mesh density of the FEMM simulation for good trade-off between precision and fast results.

The 4-dimensional matrix was created and it took about 53 hours to be completed with 41160 values. The computer used has Windows Vista operational system and Pentium dual-core (1.46GHz) processor. It may seem a long time but note that the 4-dimensional matrix may be used several times in different transformer designs and also to different ICT optimization, as the ones shown in Figure IV.15.

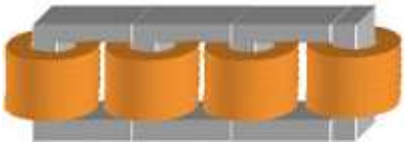


a) Symmetrical cubic ICT



b) Symmetrical 6-phase ICT

c) Symmetric circular ICT



d) Ladder with distributed leakage flux

Figure IV.8: Different topologies of monolithic intercell transformer which may use the 4-dimensional matrix to speed up the optimization process.

IV.2.2 High Frequency Leakage Inductance and AC Resistance

Only one structure may be used to simulate the high frequency AC/DC resistance ratios related to the differential mode current and to the common mode current (Fr_{extDM} and Fr_{extCM} respectively), and also the AC leakage inductance $L_{leakhfext}$. This is shown in Figure

IV.9. Note that each turn is represented since in this case skin and proximity effects are important.

For this structure there are other parameters which may influence the simulation of Fr_{extDM}, Fr_{extCM} and $L_{leakhfext}$ which are the number of turns and the frequency. In Figure IV.9 all the geometrical parameters which may change the leakage inductance are represented. By previous simulations, 2 conclusions could be stated:

1. Contrary to the conclusions for the other case, if we shrink or expand the transformer, maintaining the ratios between all geometrical parameters shown in Figure IV.9, Fr_{extDM}, Fr_{extCM} and $L_{leakhfext}$ change their values. In fact, it was observed that these values remain the same only if we change the frequency so the factor Q (equation (II-4)) remains the same.
2. Like in the other case, parameter F has a negligible influence on Fr_{extDM}, Fr_{extCM} and $L_{leakhfext}$ if it is greater than 8% of A.

By these conclusions, we assume that parameter F is not essential to create the N-dimensional matrices. By conclusion 1, we observe that we just need to simulate a transformer normalized in geometry and that another important simulation variable is Q and not the frequency. Parameter H must not be used as variable since in an optimization routine it may be greater than C, which is physically impossible. Instead, a filling factor coefficient $Kr = N_t \cdot H/C$ may be used. Consequently, the SOR has 7 dimensions which are B/D, C/A, D/A, E/A, N_t, Kr and Q.

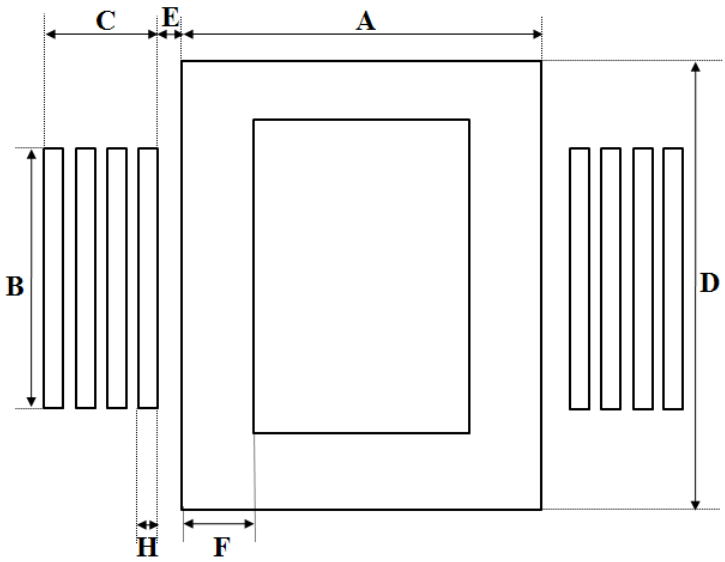


Figure IV.9: ICT geometrical parameters taking turns into account.

IV.2.2.1 Number of Points to be Simulated

Since the 3 matrices which must be created have 7 dimensions each, the number of points needed in each dimension must be wisely chosen so we have good trade-off between the interpolation error, the size of the matrices and the time to create them. The simulation of each point in one of these matrices takes much longer than the simulation of leakage inductances at 0Hz. This will be explained in the next sub-section. Thus, a smaller number of

points in each dimension will be considered and consequently poorer accuracy must be admitted.

Values of each parameter used in the matrix construction are shown below:

$B/D = \{0.2, 0.5, 0.7, 0.95\}$

$C/A = \{0.05, 0.2, 0.4, 0.5\}$

$D/A = \{0.2, 0.5, 0.8, 1.25, 2, 5\}$

$E/A = \{0.01, 0.04, 0.07, 0.1, 0.15\}$

$N_t = \{1, 2, \ldots, 30\}$

$Kr = \{0.5, 0.75, 1\}$

$Q = \{1, 2, 3, 5\}$

The values of the leakage inductance are stored in a 4x4x6x5x30x3x4 7-dimensional matrix containing 172800 values. However the matrices which will store the values of Fr_{extDM} and Fr_{extCM} are a little bit different. As explained in Sub-Section III.2.1.4, to precisely predict AC resistance we must find the AC/DC ratios for each layer. As a result, matrices storing these values must have another dimension where the memory space needed is dynamically assigned depending on the number of turns. This is easily made using MATLAB.

Finally the number of FEM simulations needed is equal to 2 x 172800, since the simulation related to the common mode and the differential mode currents are necessary. Thus the simulation boundaries and mesh density must be even more carefully chosen so the total time to create the matrix is reasonable.

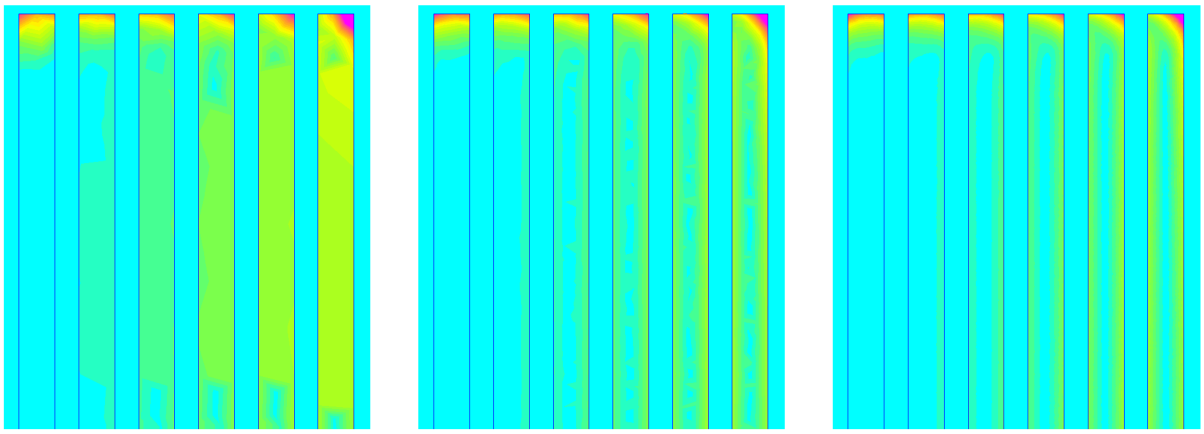
IV.2.2.2 The Influence of Mesh Generation and Simulation Boundaries

We have used the same strategy as shown above which consists on creating two regions outside the core: one small region with high mesh density and another larger region with coarse mesh density. This is enough to precisely predict leakage inductance. However to be able to account for skin and proximity effects, adequate mesh density is needed inside each conductor.

In order to investigate the influence of mesh density in this case, simulations were carried out using FEMM software. Figure IV.10 shows an example of simulations of the current density inside the conductor of an ICT, for different mesh densities and factor *Q* equal to 5. Note that the scale used in all the figures are the same and so we can see that copper losses can not be precisely computed for coarse mesh density.

Table IV-5 shows the variation of the number of nodes, the total simulation time and the calculated Fr_{extCM} with the ratio between the skin depth and the maximum distance between 2 nodes (*Ep/Dnodes*). The last column compares the calculated Fr_{extCM} to the most accurate one (which is simulated with the highest mesh density). Note that the maximum distance between 2 nodes must be smaller than 1/4 of the skin depth so the error is less than 1%.

Due to the fact that many simulations must be performed to create the 8-dimensional matrices, we decided to accept stronger error and to choose *Ep/Dnodes* = 2, for the simulations used to create the matrices.



a) Ep/Dnodes=0.2 *b) Ep/Dnodes=1* *c) Ep/Dnodes=5*

Figure IV.10: Comparison between FEMM simulations of the current density for different mesh density.

Ep/Dnodes	Number of nodes	Simulation time (s)	AC/DC resistance ratio, Fr_{extCM}	Fr_{extCM} / Fr_{extCM_max}
0.5	2583	1.98	26.66	1.2167
1	4409	2.92	23.95	1.0930
2	10536	5.81	22.52	1.0278
3	21027	11.18	22.20	1.0129
4	31836	18.15	22.07	1.0069
5	50605	30.71	21.97	1.0024
10	170118	147.96	21.91	1.0000

Table IV-5: Simulated AC/DC resistance ratio for different mesh densities.

IV.2.2.3 Reducing Simulation Boundaries

Given that the structures we simulate are symmetric, we may reduce the simulation time by reducing the simulation area as shown in Figure IV.11. Only one fourth of the total area may be simulated if appropriate conditions are imposed on the lower and left boundaries of this figure. On the left boundary we must impose the magnetic vector potential *A* equal to zero so no flux lines are allowed to trespass it. No condition must be imposed in the lower boundary since all flux lines "arrive" vertically at this boundary.

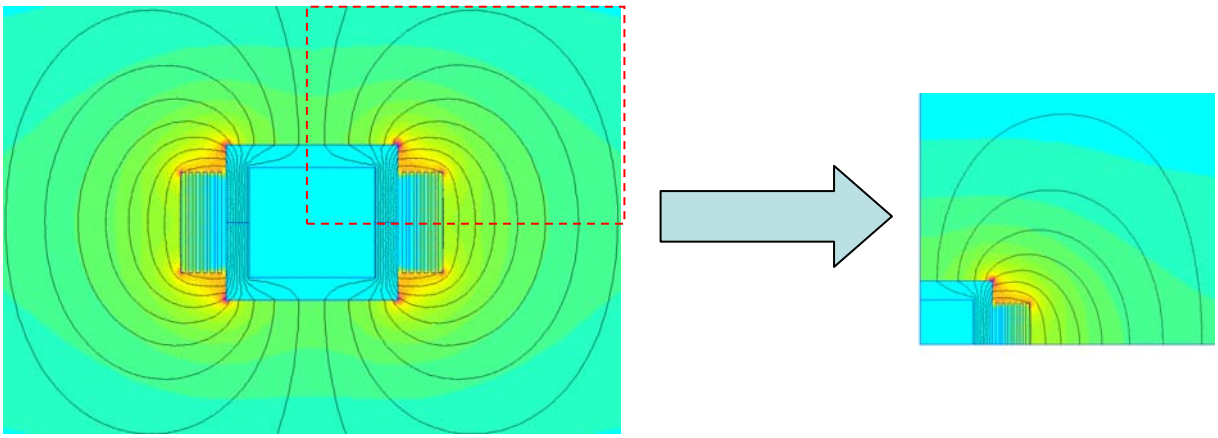


Figure IV.11: Simulation of one fourth of the total structure.

Using this strategy, simulation time is reduced to practically 1/4 of the time it takes when using the total area. However corrections must be made since 1/4 of the area has twice the real resistance of the conductor and the same leakage energy if we use the same current in the conductors.

IV.2.2.4 Simulation of Different Structures

Until now only the ICT structure shown in Figure IV.1a having conductors on the vertical position was considered. However many other structures should be optimized and also conductors on the horizontal position should be regarded. We only consider conductors in the vertical position (N_t layers of one turn per layer) or in the horizontal position (one layer with N_t turns) since the analysis presented in Chapter II showed that these two winding configurations are the ones which reduce high frequency copper losses.

Five other cases studied in the present research are exposed below in figures containing: the structure drawing, the corresponding geometrical variables, a FEM simulation graph and the values of each variable which were used to create the N-dimensional matrices. Observe that notation has changed for some geometrical parameters and that there is no need to simulate the air inside the core since the core width has little influence on the leakage inductance and AC resistance. Also variable *A* is considered always equal to 1 to simplify the analysis and simulation.

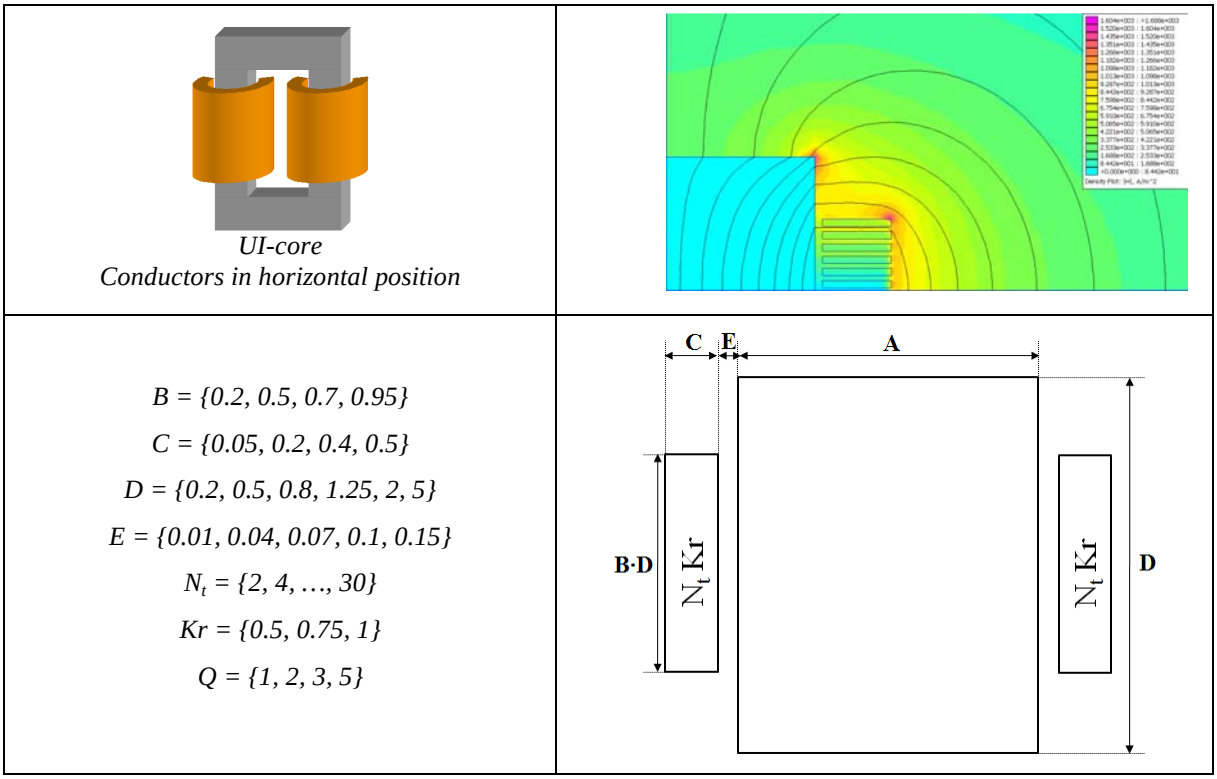
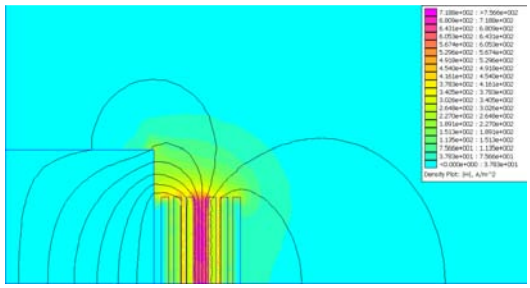
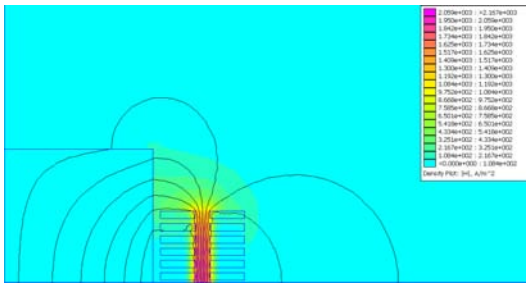


Figure IV.12: UI-core, conductors in horizontal position.



Conductors in vertical position



Conductors in horizontal position

B = {0.2, 0.5, 0.7, 0.95}
C = {0.05, 0.2, 0.4, 0.5}
D = {0.2, 0.5, 0.8, 1.25, 2, 5}
E = {0.01, 0.04, 0.07, 0.1, 0.15}
G = {0, 0.1,…, 0.9}
N_t = {2, 4, …, 30}
Kr = {0.5, 0.75, 1}
Q = {1, 2, 3, 5}

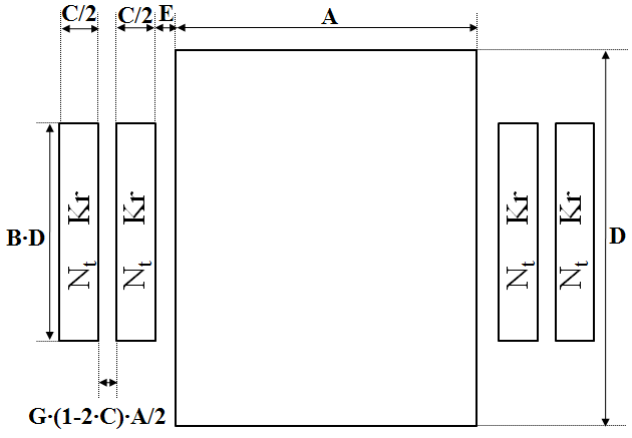
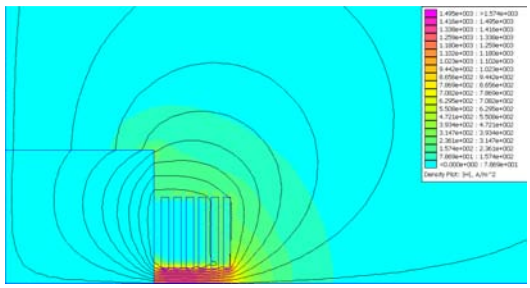
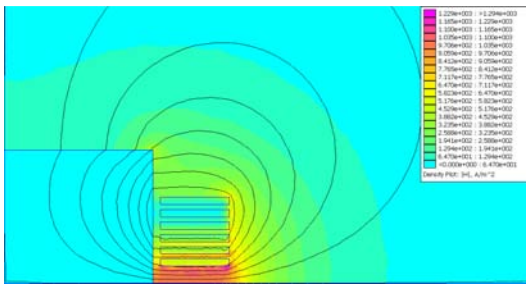


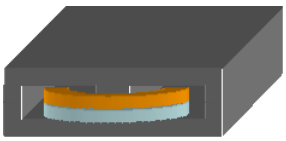
Figure IV.13: EE-core, concentric windings, conductors in horizontal and vertical positions.



Conductors in vertical position



Conductors in horizontal position



B = {0.2, 0.5, 0.7, 0.95}
C = {0.05, 0.2, 0.4, 0.5}
D = {0.2, 0.5, 0.8, 1.25, 2, 5}
E = {0.01, 0.04, 0.07, 0.1, 0.15}
G = {0, 0.1,…, 1.0}
N_t = {2, 4, …, 30}
Kr = {0.5, 0.75, 1}
Q = {1, 2, 3, 5}

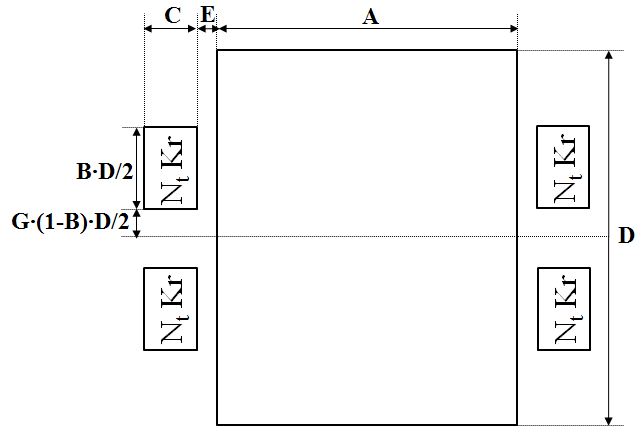


Figure IV.14: EE-core stacked windings, conductors in horizontal and vertical positions.

Some of the matrices were already created. To give an idea of the time it takes to perform all the simulations, we will take the example of the EE-core having concentric windings with conductors at horizontal position (Figure IV.13 on the right). The leakage inductance matrix has 864000 values and the AC/DC ratio matrix related to the common mode current has 3691200. Simulations took 637 hours (about 27 days) to be completed using fast computer, which results an average of 2.65 seconds per simulation. The whole simulation process takes a long time, but once it is done, optimization routines may interpolate the values. This is a very fast practice as it will be seen next.

IV.2.3 Multidimensional Interpolation

There are different methods to interpolate the values of the matrices created in the last sub-section. The most common methods are the "linear", "cubic" and "spline". All of them are included in the MATLAB function *INTERPN* [107] which is used to perform multidimensional interpolation.

In order to compare the advantages of using these matrices in an optimization process instead of inserting FEM simulation inside the optimization loop, the time consumed by FEM simulation (using software FEMM) and multidimensional interpolation methods will be compared for the case of DC leakage inductance simulation. This comparison is shown in Table IV-6, where there is also an evaluation of the maximum error observed for each type of interpolation used in software MATLAB.

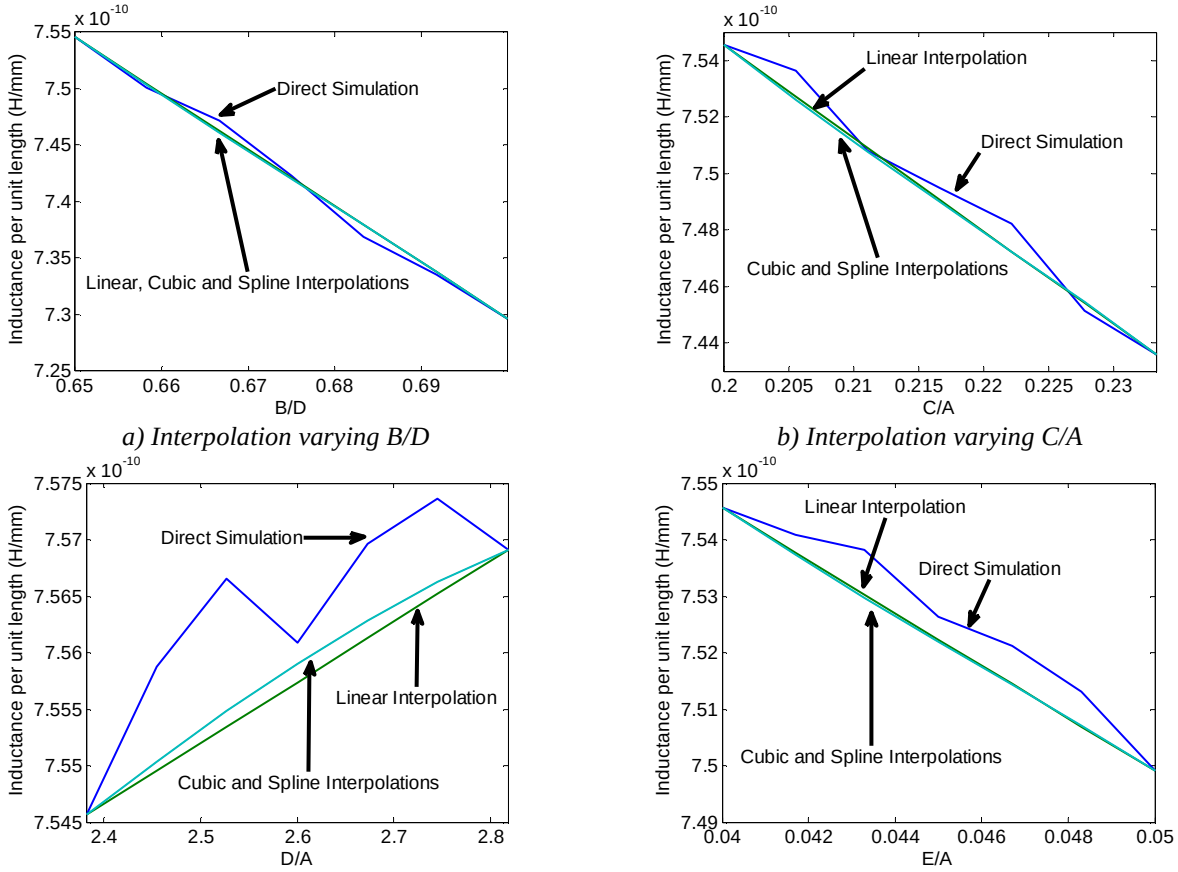
	Direct FEM Simulation	**Interpolation Method**		
		linear	**cubic**	**spline**
Time (ms)	4635	12.68	3318	3382
Max Error (%)	0	0.317	0.312	0.312

Table IV-6: Time and error comparison.

The error evaluation was performed by taking specific intervals between 2 points in each dimension and simulating 7 equally spaced points within each interval. It results in a 7x7x7x7 matrix which is to be compared to the interpolated values at the corresponding points.

Figure IV.15 shows, for one specific initial shape, the leakage inductance values obtained by different interpolation methods and by direct FEM simulation. It can be seen that usually cubic and spline methods are closer to simulated results than linear interpolation.

Concerning Table IV-6, note that the greatest maximum error exists when using linear interpolation and this error is only 0.317%. It is not so different than the maximum error obtained by cubic and spline interpolations. On the examples we considered, linear interpolation was in average 365 times faster than direct FEMM simulation. Our conclusion is that cubic and spline interpolations are excessively time-consuming and their slightly smaller error does not justify their use in an optimization routine.



a) Interpolation varying B/D

b) Interpolation varying C/A

c) Interpolation varying D/A

d) Interpolation varying E/A

Figure IV.15: Comparison between interpolation results for different methods and direct simulation at reference points (B/D=0.65, C/A=0.2, D/A=2.3818, E/A=0.04).

IV.3 Optimization Algorithms

Optimization algorithms were developed using some of the models shown in Chapter III and the approach and SOR explained in this chapter. The first algorithm which will be described is related to the design of 2-cell ICTs having the structure shown in Figure IV.1 and used in a Buck converter.

The first step is to enter all information about the optimization process: Variables, Parameters, Constraints and Objective. This is done by using an Excel file which is shown in Figure IV.16. The following explanations refer to this figure.

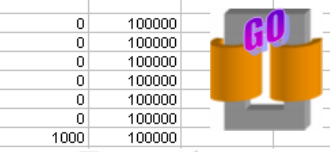
Regarding the *Optimization Variables*, the user must insert the *Initial value*, *Minimum value* and *Maximum value* of each variable. Each variable can be considered as a simple parameter (fixed value) if its corresponding checkbox at column *F* is not checked. This parameter will have the value corresponding to its "*initial value*".

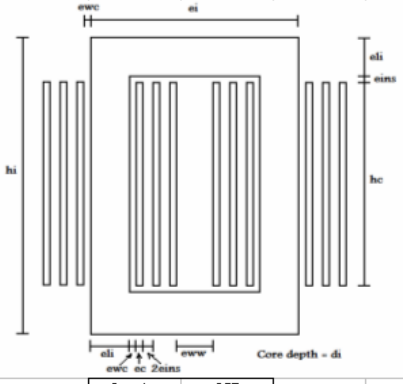
All the *Fixed Values* must be inserted. Note that core and conductor materials may be chosen from drop-down lists which are related to a workbook containing all the necessary information about these materials. Also, custom materials inserted by the user can be used.

The *Constraints* which are active must have their corresponding checkbox checked (column *F)*. These are inequality constraints and the maximum value allowed is supplied by the user.

At the end, one of the *Objectives* must be chosen from a drop-down list.

	Function	Description	Name	Initial Value	Unit	Include?	Min Value	Max Value
4	*OptimizationVariables*	Conductor width	ec	0.35	mm	Include	0	100000
5		Conductor height	hc	320.00	mm	Include	0	100000
6		Inter-winding distance	eww	64.00	mm	Include	0	100000
7		Core leg width	eli	27.00	mm	Include	0	100000
8		Core depth	di	35.00	mm	Include	0	100000
9		Number of turns	Nt	12.00		Include	0	100000
10		Switching frequency	Fs	20000	Hz	Include	1000	100000
11								
12	*Fixed Values*	Horizontal winding-core distance	ewc	0.00	mm			
13		Insulation thickness	eins	0.20	mm			
14		Input voltage	Vin	200	V			
15		Output DC current	Idcout	500	A			
16		Calculation temperature	Tc	100	°C			
17		Core material: 3C90 Philips(20-200kHz)				CUSTOM		
18		relative permeability	Mur	1.80E+03		0		
19		saturation induction	Bsat	2.50E-01	T	0.00		
20		alpha, frequency Steinmetz coeffient	alpha	1.45E+00		0.00		
21		beta, Induction Steinmetz coeffient	beta	2.75E+00		0.00		
22		Gain, Steimetz coefficient	Cm	2.65E-03		0.00		
23		Temperature Correction coefficient 0	ct0	2.45E+00		0.00		
24		Temperature Correction coefficient 1	ct1	3.10E-02		0.00		
25		Temperature Correction coefficient 2	ct2	1.65E-04		0.00		
26		Core mass density	Dmi	5.00	Kg/l			
27		Core price	Pri	1.00	$/Kg			
28		Conductor material: Copper				CUSTOM		
29		Resistivity	ro	2.26E-08	Ωm	1.85E-08		
30		Conductor mass density	Dmc	8.96	Kg/l	6.00		
31		Conductor price	Prc	10.00	$/Kg	11.00		
32		Number of harmonics calculated	Nh	200				
33		Duty Cycle	D	0.25				
34		Thermal exchange coefficient	Hexc	15.00	W/m²/°C			
35								
36	*Contraints*	Core width	ei	0.00	mm	Include		
37		Core height	hi	0.00	mm	Include		
38		Maximum output current ripple	Ioutrmax	100.00	A	Include		
39		Maximum induction in core's leg	Bmax	0.35	T	Include		
40		Maximum losses	Pmax	100.00	W	Include		
41		Maximum volume	Volmax	0.00	mm3	Include		
42		Maximum weight	Mmax	0.00	Kg	Include		
43		Maximum price	Prmax	0.00	$	Include		
44		Maximum RMS current density	Jmax	5.00	A/mm²	Include		
45		Maximum Temperature Rise	Dtmax	30.00	°C	Include		
46								
47	*Objectives*	Total Mass						





Counter	257

Figure IV.16: Excel file used to enter information about the optimization.

By clicking on *GO*, all data are sent to MATLAB and a MATLAB file containing the optimization routine is run. This routine makes use of function *FMINCON* in order to search for the minimum value of the chosen objective, taking into account the chosen inequality constraints.

Inside the main function, geometrical calculation is made to find the volume, mass, DC resistance and thermal exchange surface of the component, used to calculate the temperature.

DC flux density is established by using the DC leakage inductance found by calculating it inside the core window (equation (III-14)) and outside by using the Set of Responses explained in Sub-Section IV.2.1.

Current ripple is determined by first calculating the total AC leakage inductance. On part of this inductance is due to the part of the winding inside the core window, which is analytically calculated and modified by Dowell's equation. Outside the window we use the Set of Responses explained in Sub-Section IV.2.2.

High frequency copper losses are also predicted using the current ripple and the AC/DC resistance ratios calculated inside the core window (equation (II-5)) and outside using the Set of Responses explained in Sub-Section IV.2.2. Theory explained in III.2.1.3 is used since the high frequency current has triangular waveform.

Flux density inside the core has triangular waveform. Its peak-to-peak value is calculated and simple Steinmetz model is used to calculate core losses. In a new version of

this algorithm, model shown in equation (III-25) is used so all the materials contained in the core database may be used.

Total ICT losses are calculated by adding DC and AC copper losses to core losses. Temperature rise of the ICT is estimated using these losses, the total exchange surface and a constant and predetermined thermal exchange coefficient, as depicted in equation (III-39). Obviously, the ultra simple thermal model is the weakest point of these design routines, and might be a topic for future improvement.

After some iterations, the optimizer may converge or not and the results are sent to the same Excel file. They are presented to the user as shown in Figure IV.17. In the newer version of the optimization routine, simple drawing of the optimized ICT is made in MATLAB. This will be shown in the next section.

Geometric results			
Conductor width	ec	0.55	mm
Conductor height	hc	164.51	mm
Number of turns	Nt	2.95	
Core width	ei	53.55	mm
Core height	hi	213.62	mm
Core depth	di	114.29	mm
Core leg width	eli	24.36	mm
Inter-winding distance	eww	0.00	mm
Conductor volume	VolCond	154.39	cm3
Core volume	VolCore	1216.30	cm3
Total volume	VolTotal	1370.68	cm3
Conductor weight	MCond	**1.38**	Kg
Core weight	MCore	**6.08**	Kg
Total weight	MTotal	**7.46**	Kg
Conductor price	PrCond	13.83	$
Core price	PrCore	6.08	$
Total price	PrTotal	19.91	$
Electric results			
Switching frequency	Fs	20000	Hz
DC Resistance	Rdc	0.21	mohm
AC Resistance	Rac	0.68	mohm
DC Inductance	Ldc	2.24	uH
AC Inductance	LacNHF	1.96	uH
Output current ripple	Ioutripple	638.70	A
DC Conductor Losses	PcondDC	**13.13**	W
AC Conductor Losses	PcondNHF	**8.65**	W
Total Conductor Losses	Pcond	43.55	W
Magnetic results			
DC induction	Bdc	0.14	T
Peak-peak AC Induction	Bhf	0.23	T
Maximum induction	Bmax	0.25	T
Core Losses	Pcore	**14.17**	W
Thermal results			
Thermal exchange surface	Sexc	0.13	mm²
Temperature rise	DeltaT	**29.78**	°C
Other results			
Total Losses	PTotal	**57.72**	W
Total Efficiency	EfTotal	1.00	
Max equivalent current density	JeqrmsTotal	5.00	A/mm²

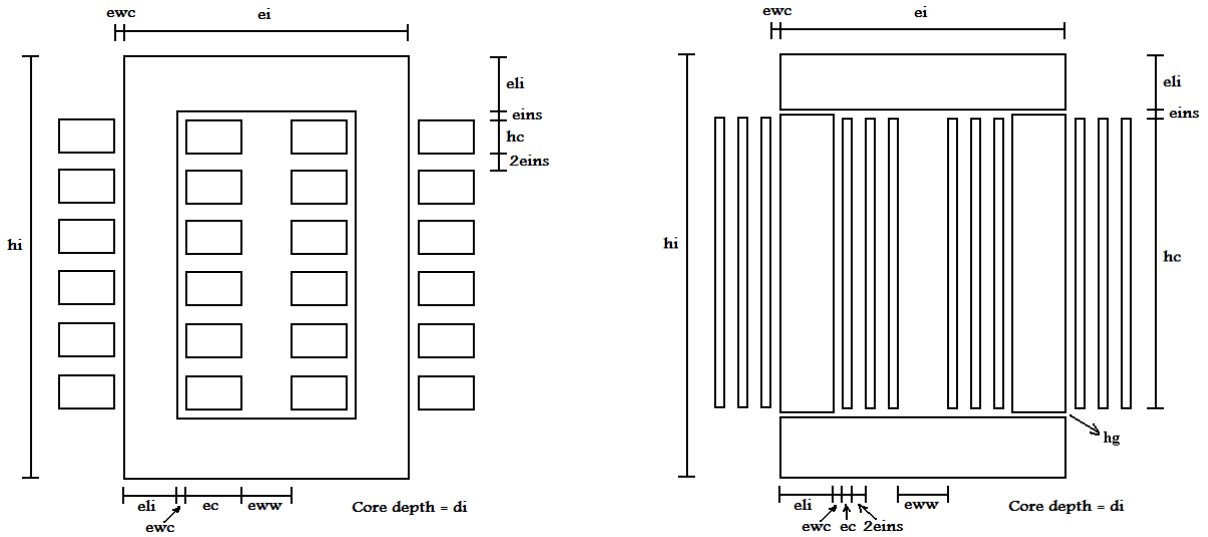
Figure IV.17: Optimization results shown in the Excel file.

IV.3.1 Other Optimization Routines

Some other routines were developed using the same approach presented before. The first one is the same 2-cell ICT having the winding using conductors in the horizontal direction. Geometrical parameters of this ICT is shown in Figure IV.18a. All the calculation is the same except to the fact that different SOR are used to calculate AC resistances and leakage inductance at high frequencies.

One algorithm was developed to optimize regular (uncoupled) inductors having the structure shown in Figure IV.18b. It is the same structure of 2-cell ICTs, but having an airgap distributed in 4 four different places. All the calculation and optimization are made directly in

Excel, thus AC resistance is not derived of SOR interpolation. Actually we could create a SOR with the values of the AC/DC resistance ratios for this case but it was not done since it would take a long time in addition to fact that uncoupled inductances is not the main subject of our study. Instead, Dowell's equations are used to calculate it although results are not so accurate. Leakage inductance SOR interpolation does not apply to regular inductors. One different optimization variable is added: airgap length (*hg*).



a) ICT having conductors at horizontal position *b) Inductor with distributed airgap*

Figure IV.18: Geometrical parameters of ICT and inductor.

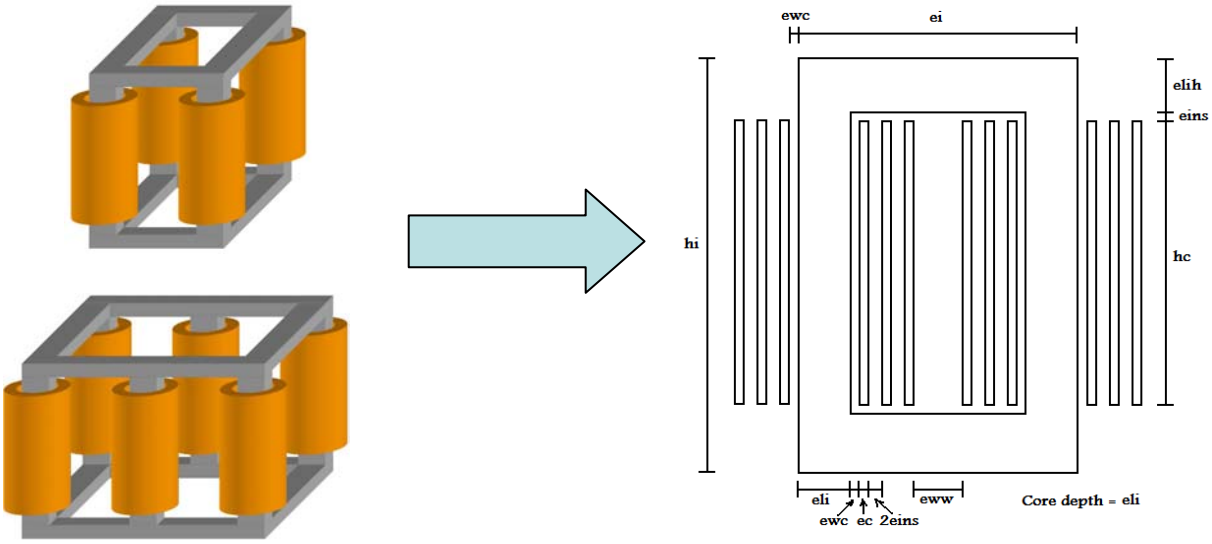
One optimization routine was developed for N-cell ICT where N = 4, 6, 8…. The topology is monolithic, double ladder, as those shown in Figure IV.19a. As seen in Section III.3.2, this topology of ICT has different flux density on the horizontal legs, when compared to the vertical wound legs. Thus the two legs may have different width and cross-section area.

However, in order to maintain the symmetry, the core section of the wound leg must be square. It means that the core depth (*di*) is equal to the core width of the wound leg (*eli*). All geometrical parameters related to two adjacent legs are shown in Figure IV.19b. Note that conductors are placed in vertical position.

The optimization routine has the same number of optimization variables when compared to the 2-cell case. However, core depth is not a variable anymore. Instead, width of the horizontal leg (*elih*) is a new variable.

All the calculation used before apply to this case except that the flux waveform in the horizontal legs must be calculated. For the moment, only the peak-to-peak value of this waveform is used in conjunction with Steinmetz model to calculate core losses. Also one extra option is given to the user in order to choose the supply sequence. Regular supply or permuted supply (as explained in Sub-Section III.3.2.1.a) may be chosen although permutation always results on smaller ICTs.

A more general optimization routine is being prepared. Calculation, data entering and displaying is made using MATLAB except for the core and conductor database which is still contained in an Excel file. This new version will optimize all types of ICTs shown above and also the ones using EE-cores (Figure III.2c and Figure III.2d). Optimization of N-cell ICTs composed of separate 2-cell will be also included.



a) Double ladder ICTs *b) Geometrical parameters*

Figure IV.19: Geometrical parameters of N-cell ICT.

A new approach to calculate flux waveforms inside each leg has also been developed with the purpose of including other topologies of N-cell ICTs such as simple ladder with guided or distributed leakage flux (Figure IV.26b and d respectively).

One of the new features of this new routine is the verification of the final AC resistance and leakage flux by FEMM simulation after the optimization result. Also, 3D drawing of the final solution is added so comparison can be visually made.

IV.4 Results

Routines developed in the last section will be used to compare designs so we can draw some conclusions about the choice of the conductor and core materials, the number of phases and switching frequency. At the end, the use of ICTs or separate inductors in interleaved converters will be discussed.

Conclusions made here are valid for the case of ICTs being used in a Buck converter with a capacitive load directly connected at the output of the ICT which means that the voltage across the ICT is imposed. Obviously conclusions may change if these ICTs are used in another converter, with another load or when there is a significant wiring inductance between the output of the ICT and the capacitive load. For example, in systems composed by more inductive loads, the output current ripple is less dependent of the ICT leakage inductance and so the constraint “Output ripple” does not influence the result.

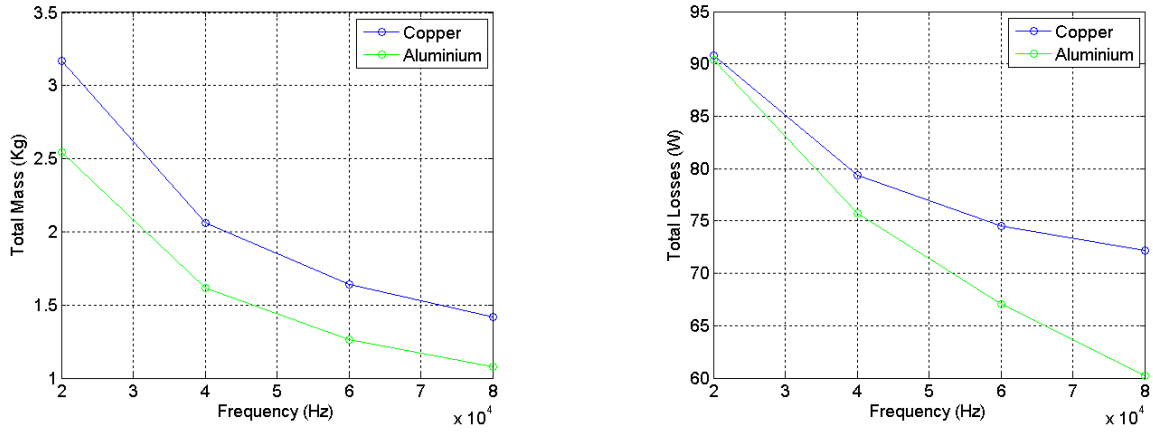
IV.4.1 Conductor Material

The first comparison is related to the material used in the conductors. It can be aluminium or copper. The topology used is the double ladder having 4 cells (Figure IV.8a) and the main parameters are shown in Table IV-7.

Parameter	Symbol	Value
Insulation thickness (mm)	*eins*	0.4
Input voltage (V)	*Vin*	200
Output current (A)	*Iout*	500
Switching frequency (kHz)	*Fs*	20 - 80
Calculation temperature (°C)	*Tc*	80
Core material		Ferrite 3C96
Thermal exchange coefficient (W/m²/°C)	*Hexc*	15
Max induction in core (T)	*Bmax*	0.38
Max total losses (W)	*Pmax*	200
Max RMS current density (A/mm²)	*Jmax*	8
Max temperature rise (°C)	*DTmax*	60

Table IV-7: Main parameters of the ICT design.

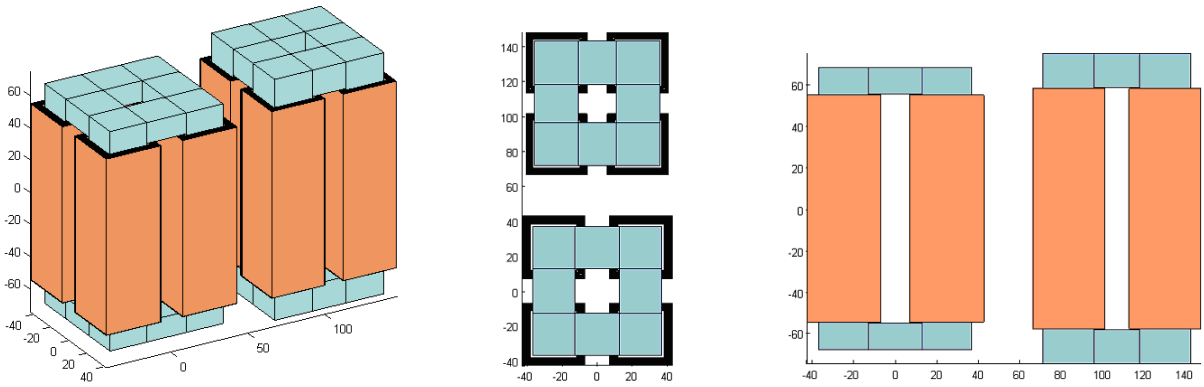
Minimizing total weight is the objective of the optimization routine, which was run for 4 different frequencies. Total mass and losses of the optimized solutions are shown in Figure IV.20. Note that ICTs made with aluminium have lower weight and losses. Although aluminium is more resistive than copper, its mass density is much lower and that is why ICTs made of aluminium are usually less heavy.



a) Total mass *b) Total losses*

Figure IV.20: Comparison of optimized ICTs with different conductor materials.

Final shape of the ICTs can be seen in Figure IV.21 and the results are shown in Table IV-8 for the case where the switching frequency is equal to 20kHz. Note that final designs are similar. The greatest difference is in the amount of conductor material. Since aluminium is much more resistive, almost the double of the material must be used to obtain the same ohmic losses in both materials, and at this point, the aluminium-based ICT is much lighter. Also, aluminium is much cheaper than copper and as a consequence, in these types of designs, it is the best choice.



a) 3D view *b) Top view* *c) Side view*

Figure IV.21: Final shape of optimized ICTs with different conductor material (scale in millimeters). Left ICT: made with aluminium. Right ICT: made with copper.

Parameter	Aluminium	Copper
Conductor weight (kg)	0.72	1.22
Conductor Volume (cm^3)	266.07	135.95
Core weight (kg)	1.83	1.95
Total weight (kg)	2.54	3.17
DC conductor losses (W)	59.66	59.43
AC conductor losses (W)	4.16	1.35
Core losses (W)	30.03	26.52
Total losses (W)	90.34	90.81
Temperature rise (°C)	60	60
Output current ripple (A)	109.49	124.40
Core width (every 2 windings)(mm)	73.77	69.11
Core height (mm)	136.36	149.84
Core horizontal leg width (mm)	13.03	16.03
Core leg width (mm)	24.07	23.86

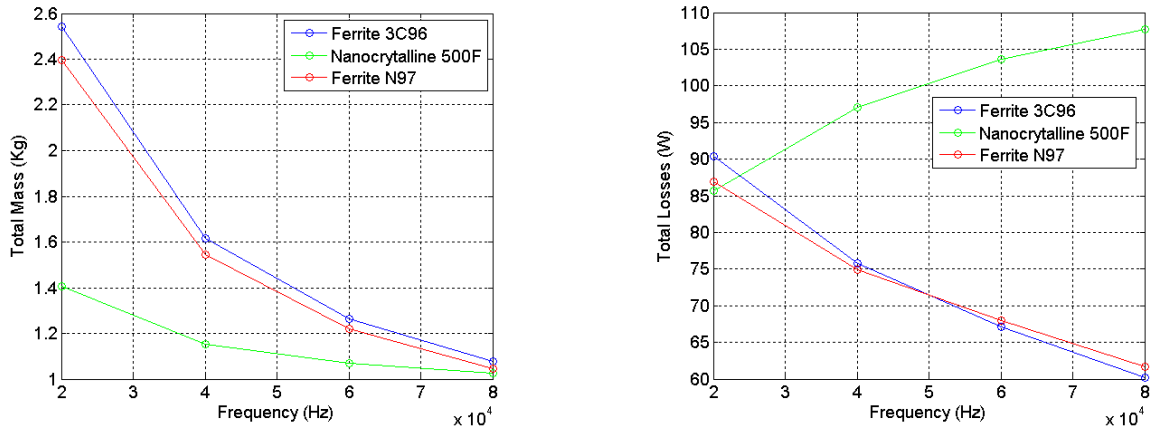
Table IV-8: Results of ICT designs with different conductor materials.

IMPORTANT CONCLUSION #1: The use aluminium is much more advantageous than copper since it results on ICTs which are less heavy and having lower cost.

IV.4.2 Core Material

Core materials having good performance at high frequency can be used in these types of ICTs. High saturation flux density associated to low core loss density is the main characteristic desired in ICT design. Three materials will be compared: Ferrite 3C96 [117], ferrite N97 [118] and nanocrystalline 500F [119]. Comparisons were made for the same ICT type and characteristics of last section. Conductor material was chosen to be aluminium and parameters are the same as in Table IV-7, except for the core material which is one of the 3 cited above. Also minimization of total weight is the objective of the optimization routine. Total mass and losses of the optimized solutions are shown in Figure IV.22.

Note that since nanocrystalline material has much higher saturation flux density, ICTs made with this material are smaller and lighter although this material has higher mass density than the others. Losses with this material are usually higher mainly because much higher flux density ripple is observed in ICTs made with this material.



a) Total mass *b) Total losses*

Figure IV.22: Comparison of optimized ICTs with different core materials.

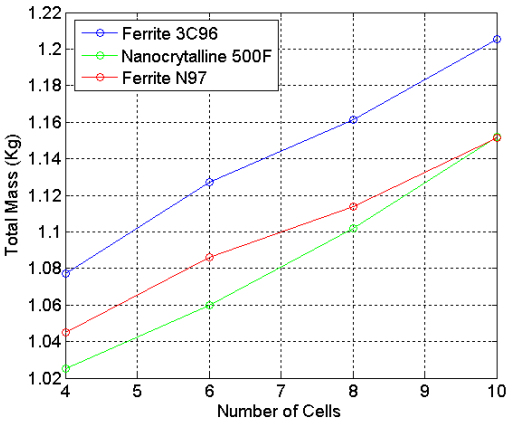
IV.4.3 Number of Cells

Comparison of the core materials was made using an ICT having 4 cells. Here we study the variation of the total mass and losses if the number of cells is increased. The same parameters and materials are used and switching frequency is fixed at 80kHz. These comparisons are shown in Figure IV.23.

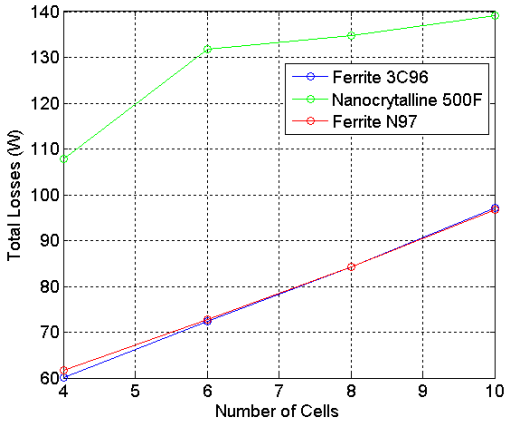
Results show that, for this specific case, the higher the number of cells in the ICT, the heavier it is. The fact that the weight increases with the number of cells is not a general result. It depends on the application and for example in the case studied in the next section 4 cells seems to be an optimum.

Also losses increase with the number of cells. It is difficult to explain why it happens since several variables and parameters play an important role in the optimization process. However we should note that the output current ripple (and consequently the ripple in each commutation cell) is reduced when the number of cells is increased, as shown in Figure IV.23c. As a consequence, the capacitor used in the output filter may be reduced if the number of cells is increased

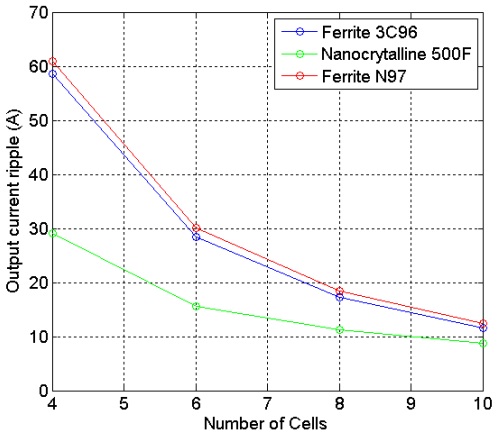
As explained in Sub-Section III.3.2.1, reduction of the flux flowing through horizontal legs may be achieved if changing the sequence of commutation. Actually, all the examples shown above were calculated using optimal permutation. The reduction on the ICT weight and losses may be verified by using the example above. Figure IV.24 compares these two options when using core made of ferrite 3C96 and switching frequency at 20kHz. Note that total mass and losses are much higher if no permutation is used.



a) Total mass

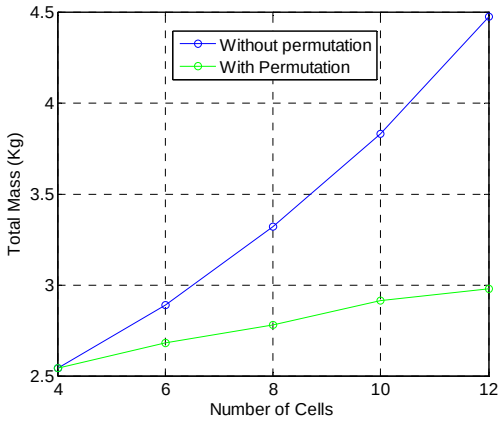


b) Total losses

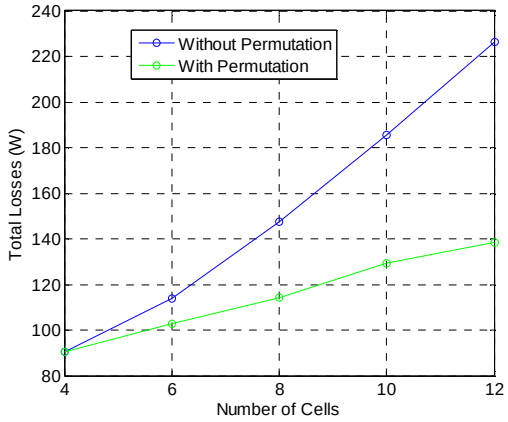


c) Output current ripple

Figure IV.23: Comparison of the number of cells in double ladder ICTs with different core material.



a) Total mass



b) Total losses

Figure IV.24: Comparison of ICT designs with and without permutation of commutation cells.

IV.4.4 ICTs or Inductors

One of the first questions which comes to mind of the designer is: Which one is better, ICTs or regular inductors?

A first element to answer this question may be seen by using Figure IV.25 where two separate inductors used in a 2-cell interleaved converter may be joined together to compose a 2-cell ICT with central leg to guide the leakage flux. By simply joining the inductors together, the current in each cell has its maximum value divided by 2 but also the frequency multiplied by 2. Usually AC resistance variation due to skin and proximity effects increases with the frequency having exponent close to 0.5. Copper losses vary with the square of the peak current. As a result it is clear that high frequency copper losses are reduced in the winding when inductors are joined together.

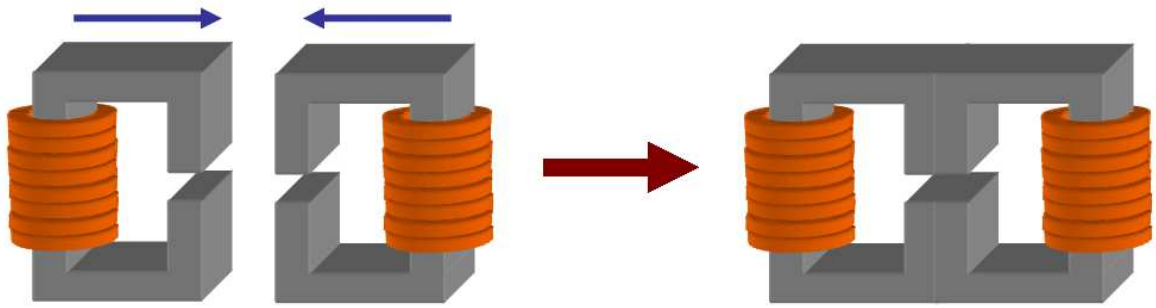


Figure IV.25: Joining two inductors to form an ICT.

The same phenomenon happens to the flux in the central leg. The maximum flux amplitude is divided by two and the frequency is multiplied by two. Regular Steinmetz models for ferrites and other materials have the flux density coefficient close to 2.5 and the frequency coefficient close to 1.5. Thus core losses in the central leg are also reduced.

Total losses are clearly reduced in an ICT having this structure and so it is reasonable to think that an ICT is usually smaller and less heavy than the equivalent inductors. This will be quantified for the examples shown above. To illustrate the use of the optimization algorithm and the difference of designs for ICTs with different number of phases, comparison between 3 ICTs and separate inductors will be presented. The ICTs are all monolithic, double ladder having 2, 4 and 6 cells.

Separate inductors have the structure presented in Figure IV.18b and they were also optimized for interleaved converters with 1, 2, 4 and 6 cells. Note that they have 2 windings which are connected in series and the airgap is distributed in 4 different places.

As an example, ICTs and separate inductors are specified to be used in the same 100kW DC/DC converter. Design is made for the worst case for each topology, which means that the duty cycle is different from each case.

The objective is to design the ICT and separate inductors having the lowest possible weight. Specifications of the design are shown in Table IV-9. Note that the maximum output current ripple is not specified since the output voltage ripple specification can be achieved by using an adequate output capacitor, which is usually much smaller than the ICTs and inductors.

Full results of the ICT optimizations are shown in Table IV-10, those related to separate inductors are shown in Table IV-11, and main results are compared in Figure IV.26. Note that, globally, ICTs are much lighter and smaller than separate inductors. For the case of 4 phases, for example, 4 separate inductors result in a magnetic component 144% heavier than

one 4-cell ICT. Also, ICTs have fewer losses than separate inductors, which is compatible with the fact that they are smaller.

The fact that ICTs are smaller and lighter than inductors agrees with conclusions made in [38]. In this article, authors optimize inductors and ICTs made with toroidal cores with different magnetic materials appropriate to each component. Inductors are made with low-loss alloy powder and ferrites (with airgap). ICTs use ferrites and nanocrystalline material. Results presented in this paper show that in all cases ICTs are smaller than inductors.

Parameter	Symbol	Value
Insulation thickness (mm)	*eins*	0.2
Input voltage (V)	*Vin*	200
Output current (A)	*Iout*	500
Switching frequency (kHz)	*Fs*	20
Calculation temperature (°C)	*Tc*	100
Core material		Ferrite 3C90
Conductor material		Copper
Thermal exchange coefficient (W/m²/°C)	*Hexc*	15
Max induction in core (T)	*Bmax*	0.25
Max total losses (W)	*Pmax*	100
Max RMS current density (A/mm²)	*Jmax*	5
Max temperature rise (°C)	*DTmax*	30

Table IV-9: Main parameters of the ICT and Inductor design.

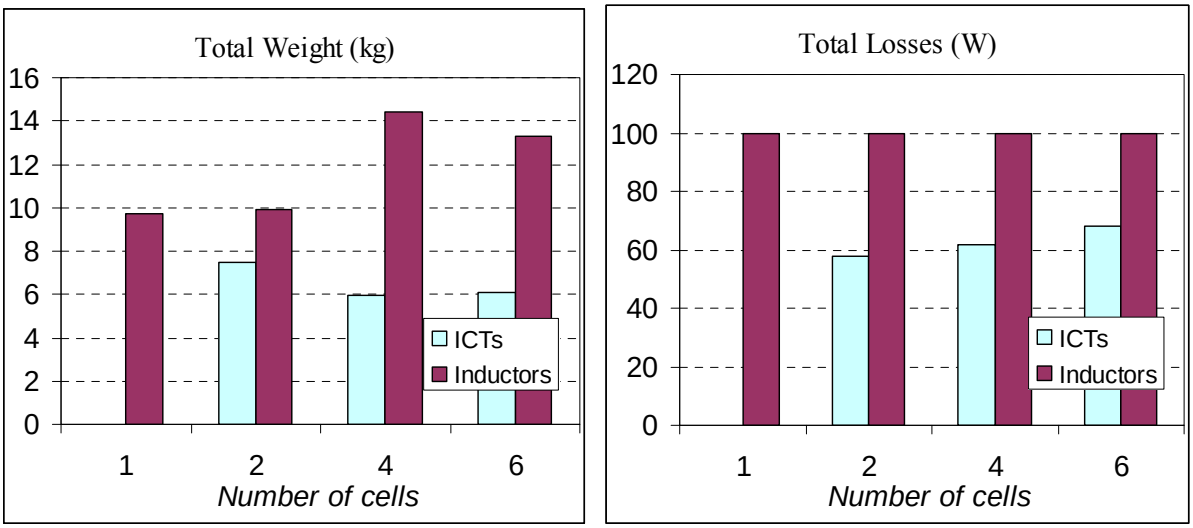


Figure IV.26: Comparison between ICTs and inductors for N-cell interleaved Buck converter.

Given that switching frequency is the same for all cases, the apparent frequency of the output current is higher for the converters with higher number of phases and also the output current ripple is smaller. As a consequence, smaller filter capacitors are necessary in these cases.

ICTs and inductors presented here have high height/width ratio. This is because these components need high conductor cross-section to allow high DC currents with ripple at high frequency (>20kHz). As a result, conductors must be high and thin.

Parameter	2 phases	4 phases	6 phases
Conductor weight (kg)	1.38	2.17	2.32
Core weight (kg)	6.08	3.75	3.79
Total weight (kg)	7.46	5.92	6.11
DC conductor losses (W)	13.13	9.63	7.09
AC conductor losses (W)	8.65	0.47	0.19
Core losses (W)	14.17	21.53	24.45
Total losses (W)	57.72	61.94	68.13
Temperature rise (°C)	29.78	30	30
Output current ripple (A)	638.70	122.84	62.82
Core width (every 2 windings)(mm)	53.55	66.82	64.48
Core height (mm)	213.62	229.39	170.45
Core depth (mm)	114.29	20.98	20.08
Core leg width (mm)	24.36	27.55	25.72

Table IV-10: Results of ICT design with different number of cells.

Parameter	1 phase	2 phases	4 phases	6 phases
Conductor weight (kg)	3.44	3.41	5.95	4.05
Core weight (kg)	6.26	6.48	8.49	9.24
Total weight (kg)	9.70	9.89	14.44	13.29
DC conductor losses (W)	55.86	53.73	52.16	53.90
AC conductor losses (W)	19.60	20.74	15.58	18.90
Core losses (W)	24.54	25.53	32.25	27.20
Total losses (W)	100	100	100	100
Temperature rise (°C)	30.00	29.56	16.98	21.84
Output current ripple (A)	660.21	331.22	162.08	93.14
Core width (mm)	94.72	61.12	56.88	57.00
Core height (mm)	693.32	350.70	326.84	143.40
Core depth (mm)	31.89	35.98	28.62	43.74
Core leg width (mm)	27.94	26.04	22.56	23.65

Table IV-11: Results of separate inductors design with different number of cells.

IV.5 Conclusions

This chapter was dedicated to the explanation of how to optimize an ICT using some of the models presented in the last chapter. Optimization methods and strategies were reviewed and the choice of the most suitable one was justified as well as the softwares to implement them. Optimization variables, parameters, constraints and objectives were selected for the case of 2-cell and N-cell ICTs.

In order to speed up the optimization process, no FEM simulation was allowed inside the optimization loop. Instead, interpolation of pre-simulated values stored in multidimensional matrices was used since this process is much faster than FEM simulation. Multidimensional matrices were generated for some topologies and they are still being generated for others. These simulations were necessary to predict the values of the DC and AC leakage inductances and AC equivalent resistances related to the common mode and differential mode currents of the part of the winding outside the core window.

With regards to FEM simulation, the influence of mesh density and simulation boundaries was investigated with the aim of finding a good trade-off between simulation time and accuracy. This is quite important when generating these multidimensional matrices since a very high number of simulations is necessary.

Optimization algorithms developed during this thesis were utilized to compare the use of different conductor and core materials. It was shown that ICTs having windings made of aluminium are usually less heavy and have lower cost, although they are bulky.

Results showed that ICTs having cores made of nanocrystalline material are smaller and less heavy than those having cores made of ferrites since the first material has higher saturation flux density. However the weight difference is significantly reduced for higher frequencies since the ferrites used in the comparison have higher performance than nanocrystalline concerning core losses at a certain frequency range.

Increasing the number of cells augments the total weight of the ICT for some cases presented in this chapter. However if the whole system composed by converter+ICT+filter (capacitor) is optimized, the conclusion may be different since the higher the number of phases, the higher the apparent output frequency and the smaller the current ripple in each cell and in the output capacitor.

Optimization results showed that ICTs are usually less heavy and produce lower losses than regular inductors if they are to be inserted in interleaved converters.

Chapter V

ICTs in Three-Phase System

V.1 Introduction

In the last chapters we saw how to design and to optimize ICTs used in some applications. In this chapter we will study the use of such components in three-phase systems and how this specific system may influence the ICT design. The impact of the choice of PWM techniques on the design of the ICT will be detailed, with a special focus on the influence of zero sequence signals which can be added to the reference signals.

Three-phase Voltage Source Inverters (VSI) are one of the most common systems found in industries. As an example, Figure V.1 shows two VSI in a typical configuration.

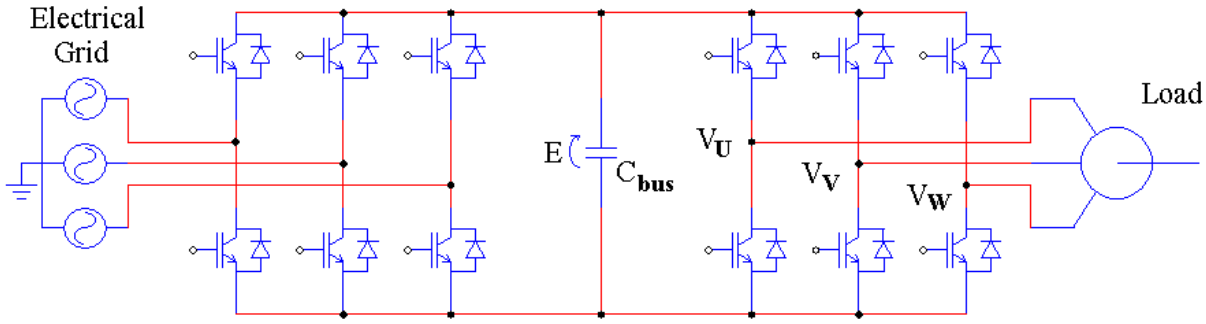
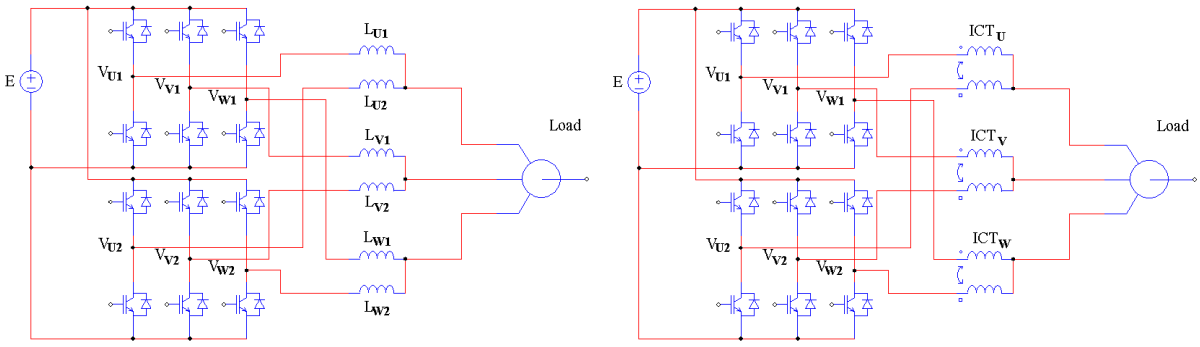


Figure V.1: Three-phase system feeding three-phase load.

When high current is needed, the parallelization of inverters may be a good option. The use of interleaving techniques offers multilevel current on the DC bus, multilevel voltage on the AC side and all resulting advantages. Initially the use of inductors was the first alternative to connect the output of the parallelized inverters, as shown in Figure V.2a. Later, coupled inductors were used [41][120][121], and like this, current stresses in the switches and in the magnetic device were reduced. Figure V.2b shows the simplest connection of coupled inductors in the system composed by two three-phase inverters.



a) With regular (uncoupled) inductors *b) With coupled inductors*

Figure V.2: Double three-phase inverter connected to three-phase load.

As far as we know, load supplied by more than two parallel three-phase inverters coupled by ICTs is not already found in industry but an example found in the literature is shown in [41] where each phase of a motor is supplied by three commutation cells connected through a three-cell coupled inductor.

Another use of coupled inductors in three-phase systems is found when the load is composed by two (or more) sub-systems, as shown in Figure V.3. These types of loads are

usually dual three-phase motors [122][123][124][125][126] and loads connected by dual three-phase transformers. The advantage of this type of load is the degree of freedom presented by the floating voltage between the two neutral points and this will be explained in details later on in this chapter.

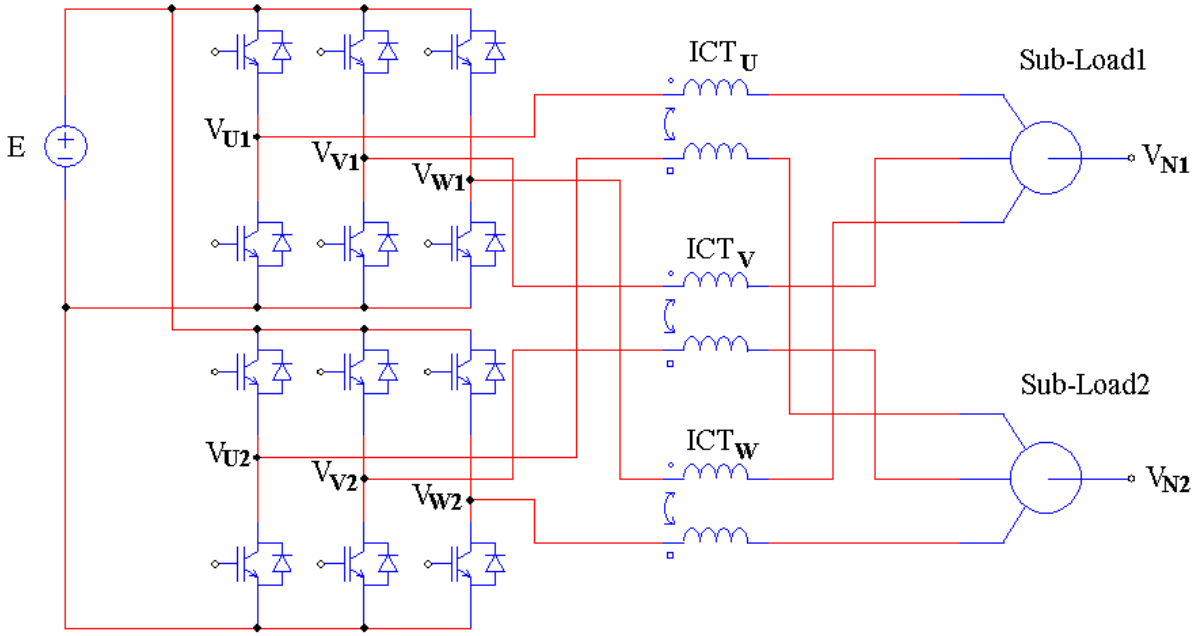


Figure V.3: Double three-phase inverter connected to double three-phase load by two-cell ICTs.

V.1.1 Modulation Methods

In relation to medium and high-voltage loads, series multilevel converters are nowadays widely used and many PWM strategies were developed in order to improve a specific characteristic of the application. These strategies may also be used in parallel multilevel converters and will therefore be reviewed here. Also we will explain the relation between modulation strategy and ICT design.

Space Vector Modulation (SVM) and carrier-based PWM are the most common modulation approaches used in the industry and in the literature. Although initially they were thought to be distinct, many authors showed their equivalence for two-level converters [127][128][129][130][131][132]. For multilevel converters the equivalence was found later by McGrath and Holmes and very good references about the subject is found in [133][134]. Since both approaches are equivalent and the carrier-based PWM is more intuitive when using zero sequence signals, the later will be used in this chapter to study the influence of the modulation to the ICT design.

V.1.2 Carrier-Based PWM Methods

There are mainly 4 methods which can be used in multilevel converters, where 3 of them may be called “Disposition Methods” which were first proposed by Carrara in [135]. The number of carriers necessary to the modulation is the number of paralleled cells (N), which is equal to the number of levels in the output voltage minus 1. Disposition methods have carriers at a frequency equal to N times the switching frequency and each carrier varies

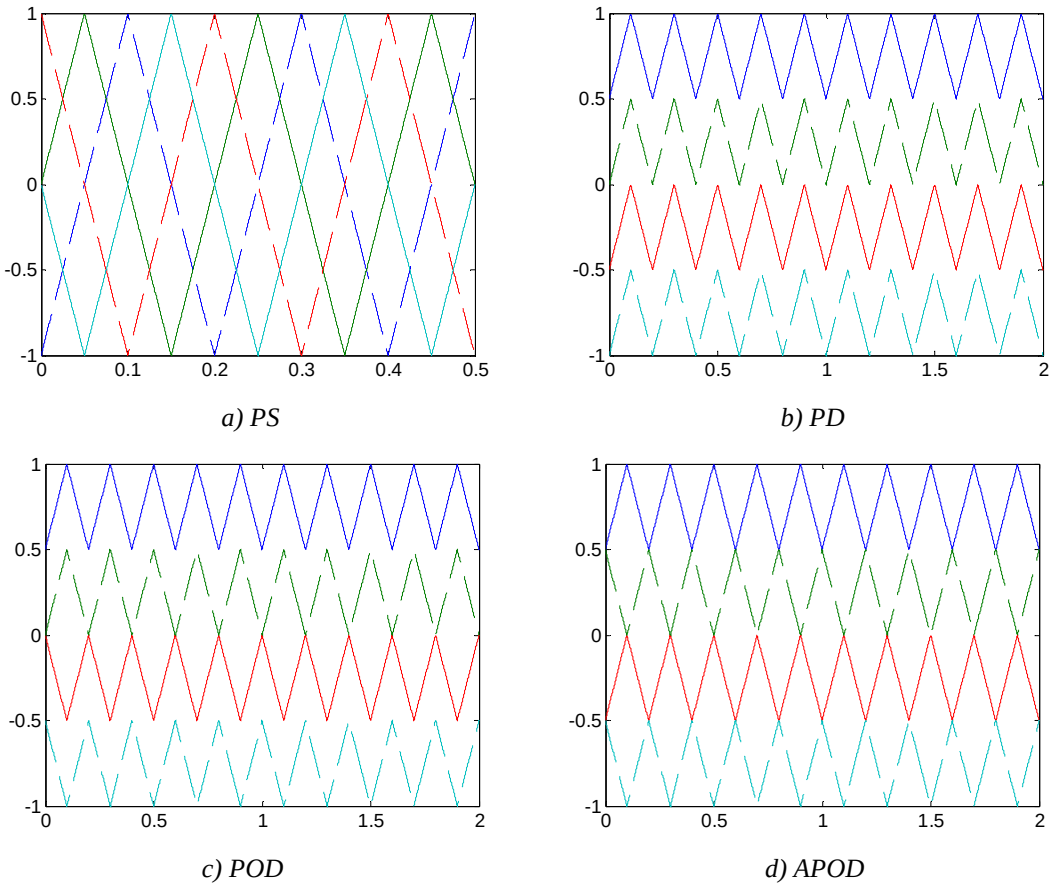
within a different range. Detailed explanation of all methods is found in [134] and they are reviewed below:

1. Phase Shift (PS): All the carriers vary from the maximum to the minimum value of the reference signal range. Each carrier has its phase shifted from $2\pi/N$ degrees from two "adjacent" carriers (Figure V.4a).

2. Phase Disposition (PD): All carriers are in phase with each other (Figure V.4b).

3. Phase Opposition Disposition (POD): All carriers above the zero line are in phase but have 180° phase difference with those below the zero line (Figure V.4c).

4. Alternative Phase Opposition Disposition (APOD): Every carrier has alternately a 180° phase difference with its neighboring carrier (Figure V.4d).



a) PS *b) PD*

c) POD *d) APOD*

Figure V.4: Different carrier-based techniques for 5-level PWM.

In general, PD method achieves higher performance than POD method when comparing the distortion on the output voltage due to the cancellation of specific harmonics [133][135][136][137]. However, in multilevel parallel converters, PD method causes higher magnetic flux inside the ICT as will be explained below.

V.1.2.1 Carrier-Based Methods Applied to Parallel Multilevel Converters

All the methods listed below may be applied to parallel converters. In order to identify which commutation cell will switch in a certain moment, a state machine may be used as it is usually done in series multilevel converters to control the voltage balance in the bus

capacitors. In parallel converters the state machine would be useful to control, for example, the flux inside the ICT.

For analysis purpose, let's take only one phase (Figure V.5) of a multilevel converter with two parallel inverters (Figure V.2b). In a system with a load with inductive characteristics, the main flux inside the ICT is due to the voltage difference (V_{X1}–V_{X2}). So it is natural to think that the state machine should choose alternately each commutation cell in order to keep the ICT magnetic flux within a certain band. Having this idea in mind, we can demonstrate that, for a 3-level converter, the PS, POD and APOD methods are equivalent, as shown graphically in Figure V.6 and that no state machine is needed. Actually, POD and APOD methods are always equivalent for 3-level converters.

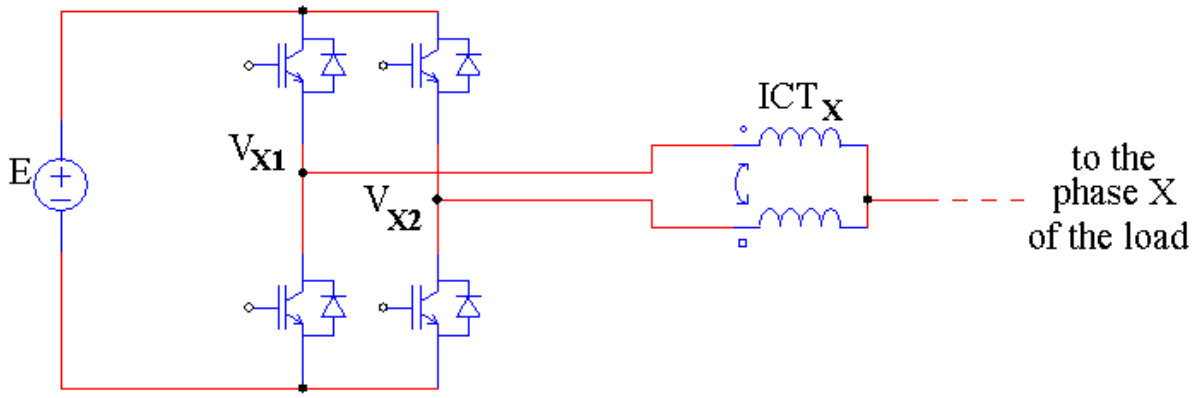
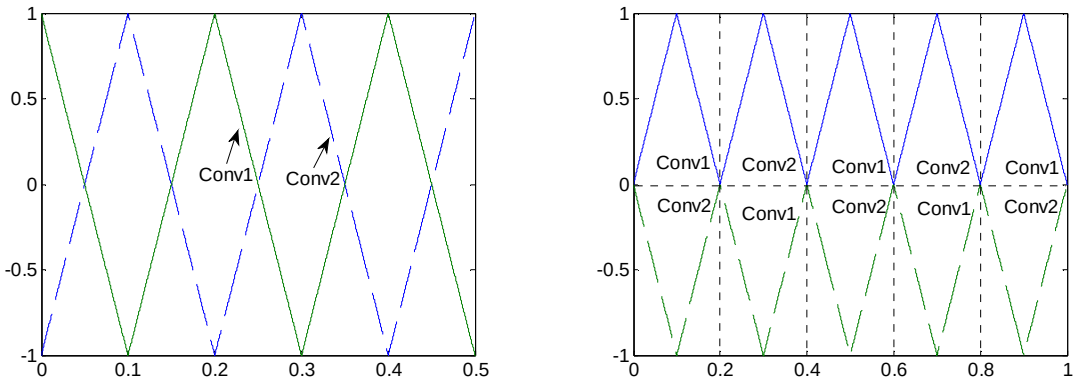


Figure V.5: One phase of the dual three-phase inverter coupled by one ICT.



a) PS *b) POD or APOD*

Figure V.6: Equivalence between PS, POD and APOD for the 3-level parallel converters.

For the PD method, a different carrier must be used to eliminate the state machine. The carriers are shown in Figure V.7. Instead, we may also use 4 carriers at the switching frequency, with 90° out of phase each. Using Figure V.8 as reference, the gate signal of commutation cell 1 comes from the comparison of reference signal (*Vref)* with carrier 1 if *Vref>0* and with carrier 3 if *Vref<0.* Correspondingly, the gate signal of commutation cell 2 comes from the comparison of reference signal with carrier 2 if *Vref>0* and with carrier 4 if *Vref<0*.

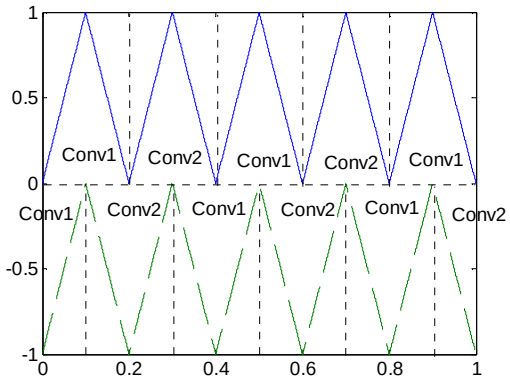
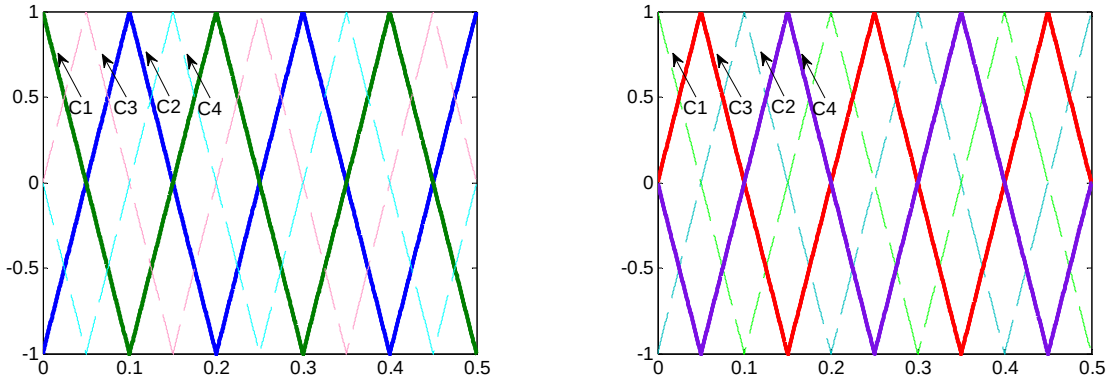


Figure V.7: Carriers for PD technique for 3-level converters.



a) if Vref>0 *b) if Vref<0*

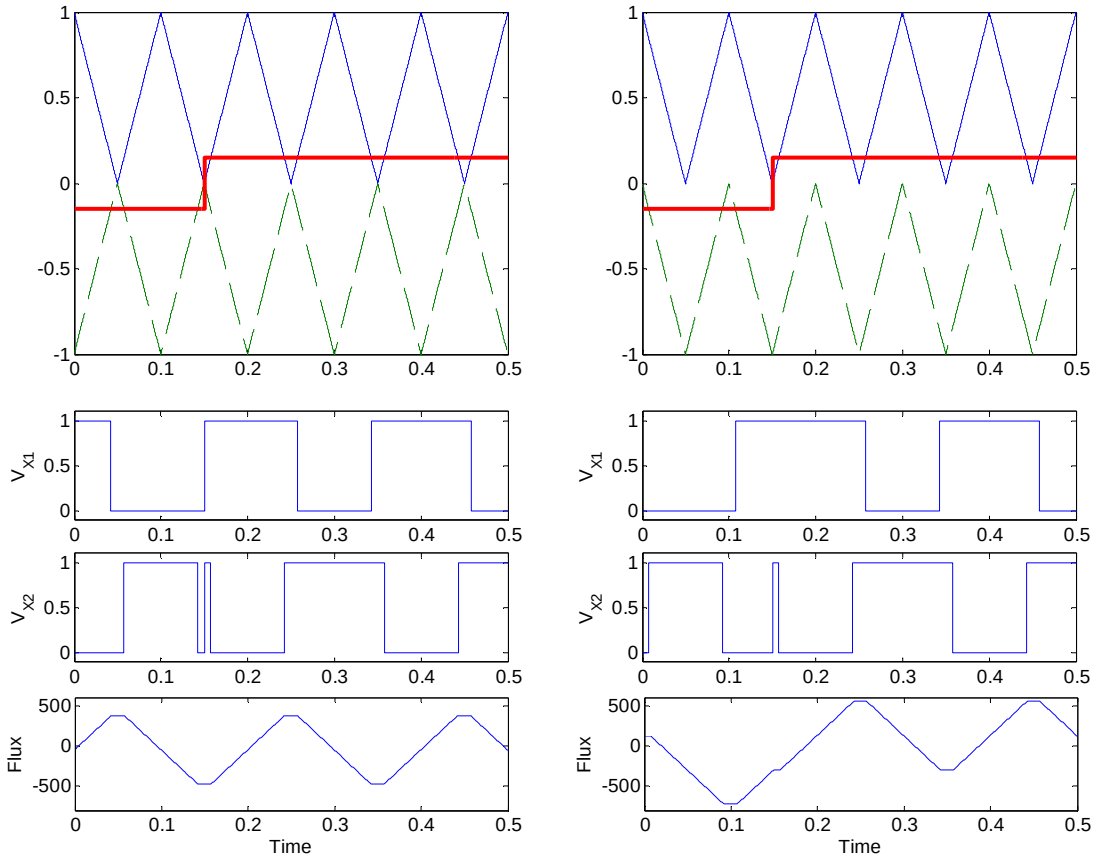
Figure V.8: Equivalence between modified PS and PD for the 3-level parallel converters.

For a system composed of N three-phase converters, if we eliminate the state machine, the POD technique is equivalent to the PS and consequently we need only to generate N carriers at the switching frequency, each one shifted from $2\pi/N$ degrees from two "adjacent" carriers. For the PD technique, we need to generate $2N$ carriers at the switching frequency, each one shifted from π/N degrees from two "adjacent" carriers.

V.1.2.1.a Flux step using PD technique

As mentioned before, PD method achieves higher performance than POD method concerning the output voltage. However it has a major disadvantage regarding the magnetic flux of ICTs used in parallel converters: "flux steps" when the reference changes the carrier to be compared to. In a 2-cell converter, it happens when the reference changes its sign.

Figure V.9 illustrates this problem, where the reference signal, the carriers, the voltage in both commutation cells and the ICT flux are shown, for both POD and PD methods. Note that when PD method is used (Figure V.9b), at the moment where the reference signal passes from positive to negative, it is not anymore compared to carrier 1 but to carrier 3 (for commutation cell 1). For commutation cell 2, it is not anymore compared to carrier 2 but to carrier 4. As a result, there is a time corresponding to a maximum of 90° (at the switching frequency) where the flux continues to grow instead of decreasing, which causes the resulting flux to vary in a different band. This band change will happen each time the reference signal crosses zero. Note that it does not happen in the POD method since there is no carrier phase changing during zero crossing of the reference signal.



a) POD *b) PD*

Figure V.9: Voltage reference, switching voltages and ICT flux for PD and POD techniques.

Depending on the difference between the reference frequency and the switching frequency, adjacent flux steps may not be complementary. It means that the flux will continue to grow. We should note that even sampling the reference will not solve the problem of flux step.

To prevent those flux steps during zero crossing when using PD method, an extra commutation may be inserted. It is out of the scope of this dissertation to explain how it can be done, but this is explained in [138].

Assumption #1: For the rest of this chapter it will be supposed that, when using PD technique, the flux step can be perfectly suppressed.

V.1.3 Zero Sequence Injection (Common Mode Offset)

In three-phase loads where the neutral point is not connected to the ground or to the middle point of the inverter's DC bus, a common mode offset may be applied to all three phases with no changing in the current at the fundamental frequency. This degree of freedom was first used in inverters in order to increase the linearity range of the output voltage [139].

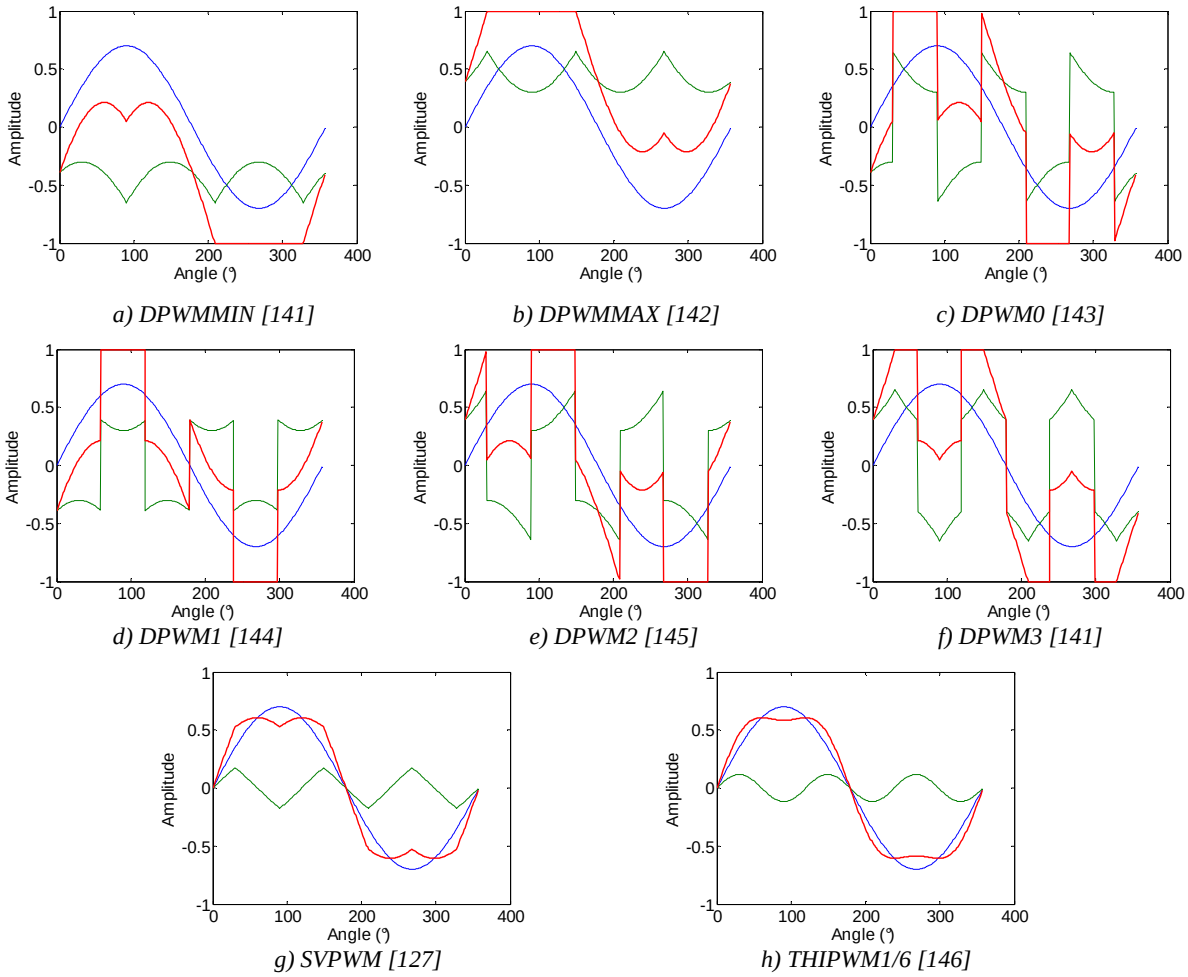
There are several different zero sequence signals described in the literature but only few of them have gained wide acceptance. Usually they are separated in Continuous PWM (CPWM) and Discontinuous PWM (DPWM). CPWM modulation waves are always strictly within the boundaries imposed by the triangular carriers while DPWM references can vary outside carrier bands resulting in output voltage clamped to the positive and/or negative DC

rail. When appropriate zero sequence is used, clamping can be obtained for one third of the time in each phase without any low frequency distortion of the output voltage.

As shown in [140], several zero sequence signals have been introduced to match the requirements corresponding to different fields of application and optimize various criteria: simplicity in the implementation, computational efficiency, high voltage linearity range, low output voltage distortion, switching losses reduction and etc. None of the zero sequence signals found in the literature addressed ICT-based converters which leads us to:

IDEA #1: Find the optimal common mode offset which reduces the magnetic flux in the ICT.

In Chapter III and Chapter IV it was seen that the design of an ICT is a tricky task and, as in any magnetic component, the smaller the flux flowing through the core, the smaller the final component. Thus finding the optimal zero sequence which reduces the magnetic flux will allow designing smaller ICTs. Obviously, the zero sequence minimizing the ICT flux may not be the best when regarding the output current ripple or the DC bus voltage ripple, and finding which zero sequence gives the best tradeoffs between DC bus filter, AC side filter and ICT itself requires application specific criteria leading to application dependant "optimal" choices. For this reason there is no universally-optimal zero sequence, but the approach used in this chapter can probably be adapted to any application.



a) DPWMMIN [141] *b) DPWMMAX [142]* *c) DPWM0 [143]*

d) DPWM1 [144] *e) DPWM2 [145]* *f) DPWM3 [141]*

g) SVPWM [127] *h) THIPWM1/6 [146]*

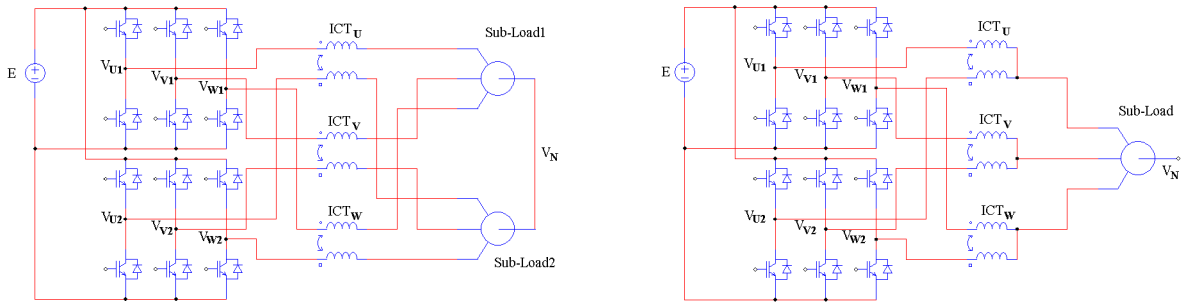
Figure V.10: Zero sequence and reference signals.

Zero sequence signals used for comparison in the next sub-chapters are shown in Figure V.10 (green lines) along with the sinusoidal reference (blue lines) and the reference after the zero sequence injection (red lines). These common zero sequences will be compared to the optimal one in terms of ICT flux.

V.2 Optimal Common Mode Offset for Flux Reduction

V.2.1 Connected Neutral Points

We will start the analysis and the search for the optimal Common Mode Offset signal (CMO) for three-phase systems with connected neutral points. This is the case of the system in Figure V.11a. In Figure V.11b there is only one three-phase load supplied by 2 inverters. The characteristic which links these two systems is the fact that the flux in an ICT only depends on the difference of voltages imposed by the commutation cells connected to it. To simplify the analysis, we will take Figure V.11b as a reference and we will suppose that these ICTs are purely inductive and their resistances are negligible, which is a good approximation for the inductances and frequencies involved in an ICT design.



a) Two sub-loads *b) One load*

Figure V.11: Different topologies equivalent to the connected neutral points topology.

The flux depends basically on the current flowing through each winding of the ICT (I_{X1} and I_{X2}, where X = U,V,W), the number of turns of each winding (N_t) and the core reluctance (*RelCore*) if we consider that the equivalent air reluctance (*RelAir*) is high when compared to the core reluctance, as shown in the equation below:

$$\phi = \frac{N_t I_{X1} - N_t I_{X2}}{RelCore} \tag{V-1}$$

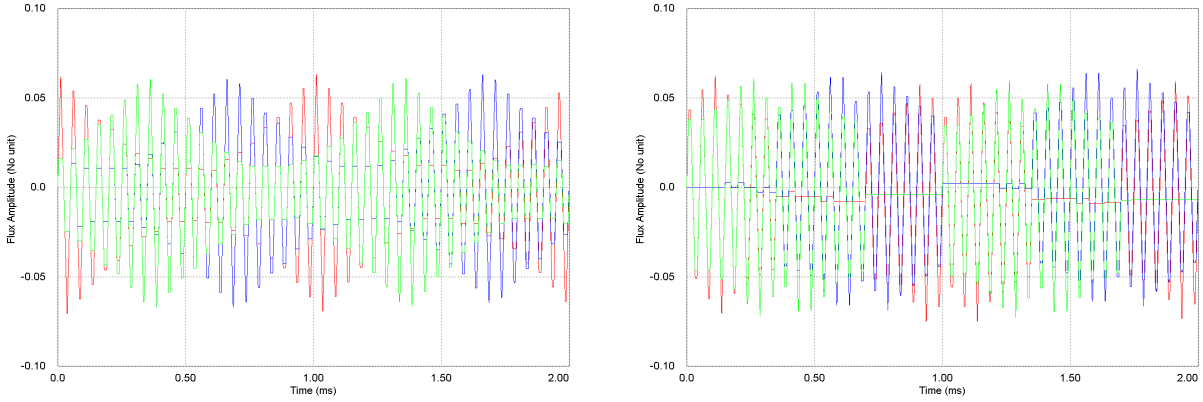
Neglecting the series resistance of the circuit, the flux will only depend on the integral of the voltage difference between each phase, and also on the mutual and self inductances of the ICT (M_{ICT} and L_{ICT} respectively), as shown in equation (V-2):

$$\phi = \frac{N_t}{RelCore} \frac{\int (V_{X1} - V_{X2})}{(L_{ICT} - M_{ICT})} \tag{V-2}$$

By this equation, wee see that comparing the impact of zero sequence signals on the ICT flux may be made by only comparing the integral of the difference of phase-neutral voltages. As an example, the fluxes in the ICTs of the 3 phases (U, V and W) are shown in Figure V.12 for the DPWM1 and Sinusoidal PWM methods, at modulation index (*Mi*) equal to 0.8, by means of a PSIM simulation and it can be seen that:

- Only 1/3 (or 120°) of the fundamental reference needs to be calculated since it is a three phase system,
- For these two strategies, the peak flux is almost the same but the RMS values are different.

Note that the flux waveforms shown in Figure V.12 are valid for one specific modulation index and such a direct comparison is meaningless. In order to compare all CMO or to find the optimal CMO, we must find the maximum peak flux over the full domain of operation (which is a key input parameter for ICT design).



a) Sinusoidal *b) DPWM1*

Figure V.12: ICT flux using DPWM1 and SPWM techniques.

To find the optimal CMO, let's analyze the behavior of the integral of the voltage difference of an ICT by sweeping the reference from its minimum value (-1) to its maximum value (+1) and calculating the maximum value (F_{max}), the minimum value (F_{min}), the maximum absolute value (F_{absmax}) and the peak-to-peak value (F_{pp}), as shown in Figure V.13. It can be seen that, for each instant, the optimal offset applied to the three phases is the one that takes away the reference of the three phases as far as possible from the value 0.

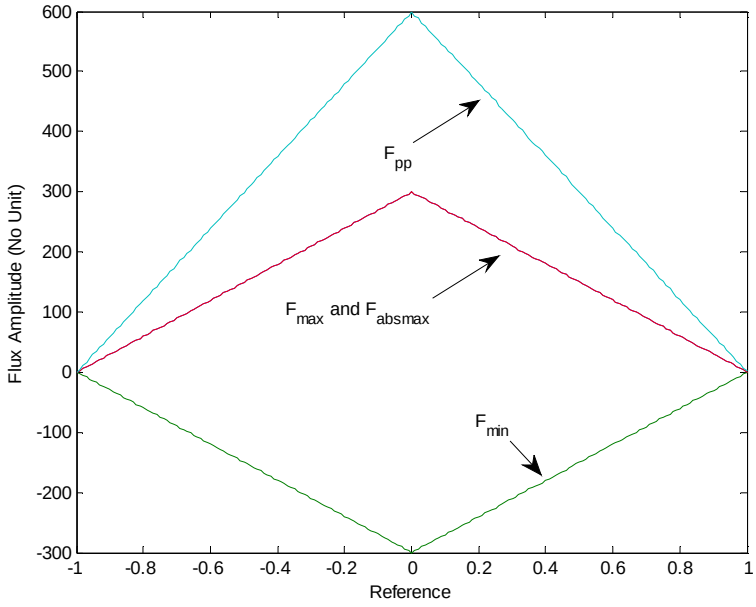


Figure V.13: ICT flux for all possible values of the reference.

The optimal CMO is easily found for low modulation indexes. For example, if modulation index is equal to 0.1, the references of the three phases will vary within -0.1 and 0.1, and as a consequence the flux oscillation will be very high for any angle of the fundamental reference signal. If we add a common mode offset which takes all three references close to -1, the flux will be minimized. For example, if all three phases have sinusoidal references, at angle 90°, phase U will have reference $v_u^* = 0.1$ and phases V and W will have reference $v_v^* = v_w^* = -0.05$. The best option is either to add an offset equal to +0.9 so that $v_u^* = 1.0$ and $v_v^* = v_w^* = 0.85$ or to add an offset equal to -0.95 so that $v_u^* = -0.85$ and $v_v^* = v_w^* = -1.0$; both options give the same minimum flux ripple. This example is shown in Figure V.14. Therefore the optimal offset for low modulation index values is

$$Offset = -1 - \min(v_u^*, v_v^*, v_w^*) \quad \text{or} \quad Offset = 1 - \max(v_u^*, v_v^*, v_w^*) \qquad \text{(V-3)}$$

Since any discrete PWM has a CMO which is a combination of the offsets of equation (V-3), any DPWM is the optimal method for low modulation indexes. An example of the waveform of two of the optimal CMOs for low modulation indexes is shown in Figure V.15 along with the references after zero sequence injection (at *Mi=0.3*).

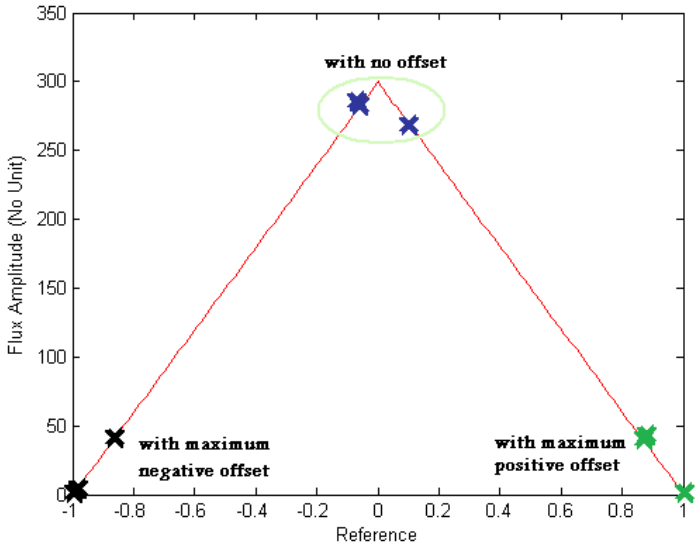
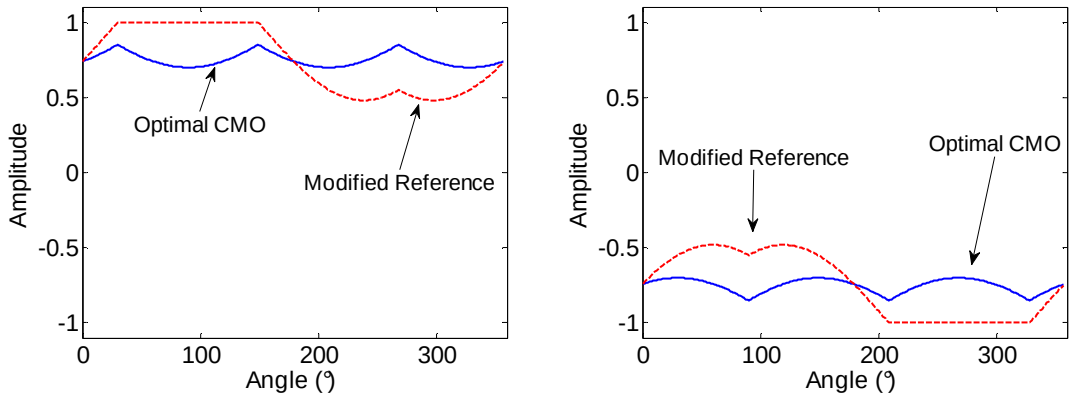


Figure V.14: Example of maximum flux oscillation with and without optimal CMO for low modulation indexes.



a) Positive optimal CMO (DPWMMAX) *b) Negative optimal CMO (DPWMMIN)*

Figure V.15: Optimal CMOs for low modulation indexes.

For high modulation indexes, the analysis is a little bit more complicated. For example, if modulation index is equal to 0.8, the references of the three phases will vary between -0.8 and 0.8, and it is not possible to find a zero sequence that gives three references with the same sign. To take the three references as far as possible from 0, a zero sequence putting the 0 in the middle of the biggest interval must be added. For example: if all three phases have sinusoidal references, at angle 80°, phase U will have reference $v_u^* = 0.7878$, phase V will have reference $v_v^* = -0.2736$ and phase W will have reference $v_w^* = -0.5142$. The best option is to bring phase U closer to 0 and phase V farther from 0 until they both have the same absolute value:

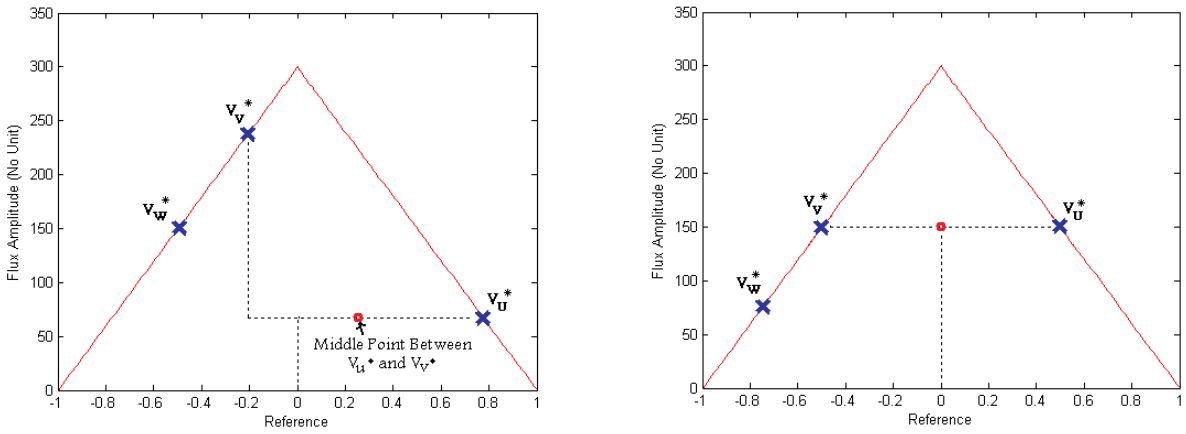
$$Offset = -\frac{v_u^* + v_v^*}{2} \quad \text{or} \quad Offset = \frac{v_w^*}{2} \tag{V-4}$$

This example is shown in Figure V.16. Generalizing for all angles and phases, the offset must be equal to half the reference which has neither the minimum nor the maximum absolute value. This can be written as follows:

$$v_0^* = v_x^* / 2 \quad \text{where}$$

$$\begin{aligned} v_x^* &= v_u^* \quad \text{if} \quad abs(v_u^*) = mid\left(abs(v_u^*), abs(v_v^*), abs(v_w^*)\right) \\ v_x^* &= v_v^* \quad \text{if} \quad abs(v_v^*) = mid\left(abs(v_u^*), abs(v_v^*), abs(v_w^*)\right) \\ v_x^* &= v_w^* \quad \text{if} \quad abs(v_w^*) = mid\left(abs(v_u^*), abs(v_v^*), abs(v_w^*)\right) \end{aligned} \tag{V-5}$$

The waveform of the optimal CMO for high modulation indexes is shown in Figure V.17 along with the references after zero order signal injection (at *Mi=0.7*).



a) Without CMO *b) With CMO*

Figure V.16: Example of maximum flux oscillation with and without optimal CMO for high modulation indexes.

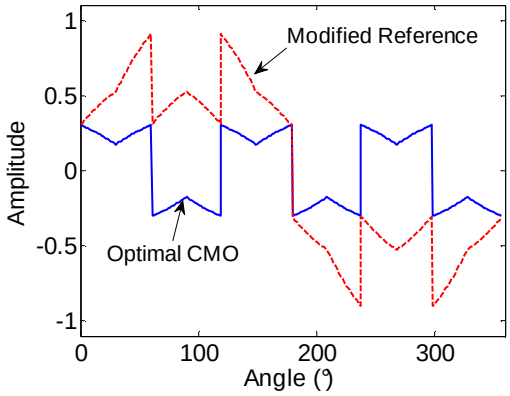
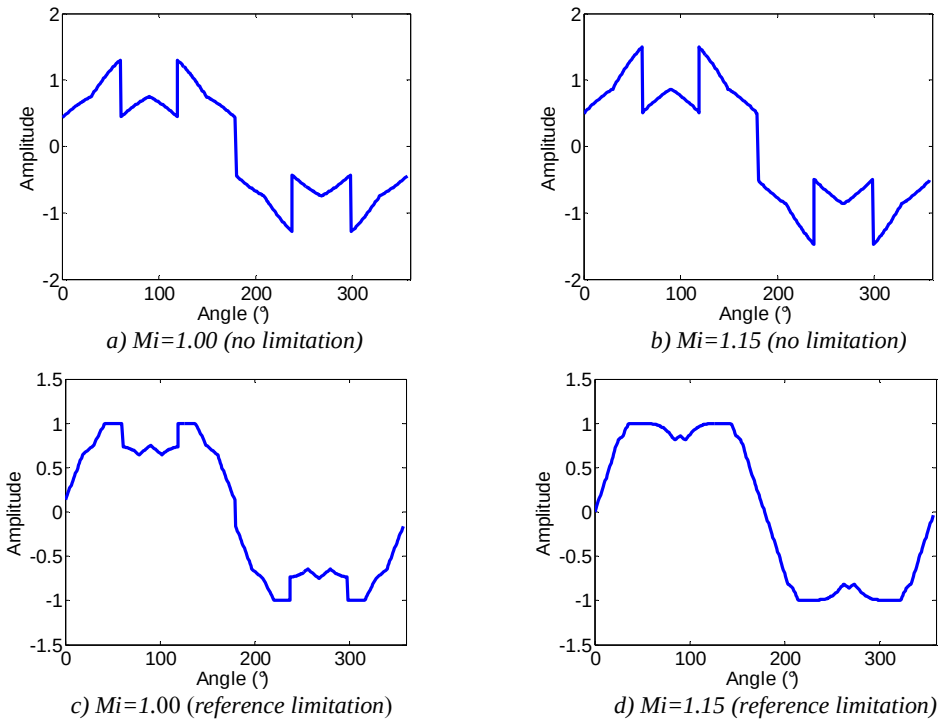


Figure V.17: Optimal CMO for high modulation indexes.

At very high modulation indexes the zero sequence given by equation (V-5) can take the references outside the [-1;+1] interval as shown in Figure V.18a and b, creating a distorted output. To solve this problem, CMO must be compensated so the reference is limited to the [-1;+1] interval as shown in Figure V.18c and d.



a) Mi=1.00 (no limitation)

b) Mi=1.15 (no limitation)

c) Mi=1.00 (reference limitation)

d) Mi=1.15 (reference limitation)

Figure V.18: Modified reference for high modulation indexes with and without CMO limitation.

This compensation is simply calculated by predicting the amount of the modified reference which exceeds 1 (or -1) for each angle. This amount is subtracted from the original CMO and, as a result, the reference is limited to +1 or -1. Thus this is still the optimal CMO with regard to the flux in the ICT, even in the overmodulation region. To illustrate the calculation of this compensation as well as the CMO, a MATLAB code is shown below. Note that modulation indexes greater than 1.15 cannot be totally compensated and distortion in the output voltage will exist, as it is well known in the literature [134].

```
If ((abs(Vu)>=abs(Vv))&&(abs(Vu)<=abs(Vw))||(abs(Vu)>=abs(Vw))&&(abs(Vu)<=abs(Vv)))
    temp = 3*abs(Vu)/2 - 1;
    Offset= Vu/2 - ((temp>0)*temp*sign(Vu));
elseif
((abs(Vv)>=abs(Vu))&&(abs(Vv)<=abs(Vw))||(abs(Vv)>=abs(Vw))&&(abs(Vv)<=abs(Vu)))
    temp = 3*abs(Vv)/2 - 1;
    Offset= Vv/2 - ((temp>0)*temp*sign(Vv));
else
    temp = 3*abs(Vw)/2 - 1;
    Offset= Vw/2 - ((temp>0)*temp*sign(Vw));
end
```

The three rules stated above must be combined to obtain an optimal behavior over the full modulation range such as illustrated in Figure V.19. Note that in this figure, curves related to modulation indexes 0.8 and 0.9 have been adapted to avoid saturation.

The exact modulation index where any discrete PWM becomes more advantageous than applying equation (V-5) will be shown later in this chapter.

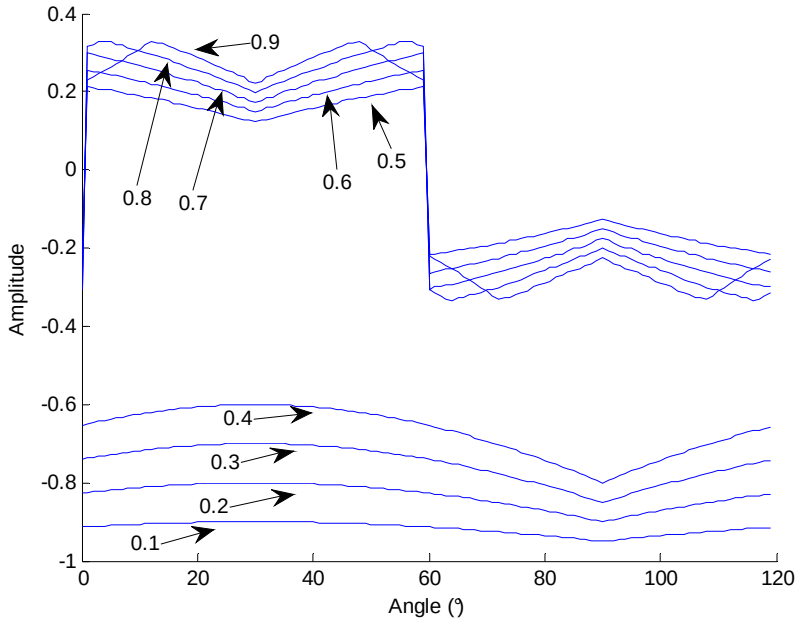


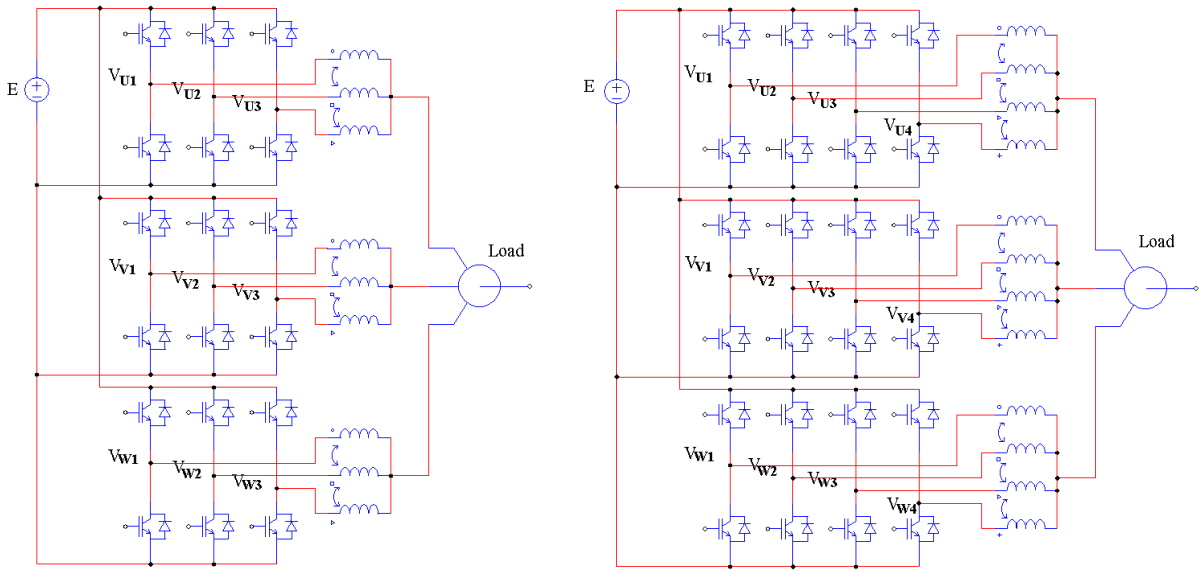
Figure V.19: Optimal CMO for all modulation indexes.

V.2.1.1 Optimal CMO for N Commutation Cells

Previously, the optimal CMO regarding the flux in the ICT was found for a three-phase system composed by only 2 parallel three-phase inverters feeding a three-phase load. It

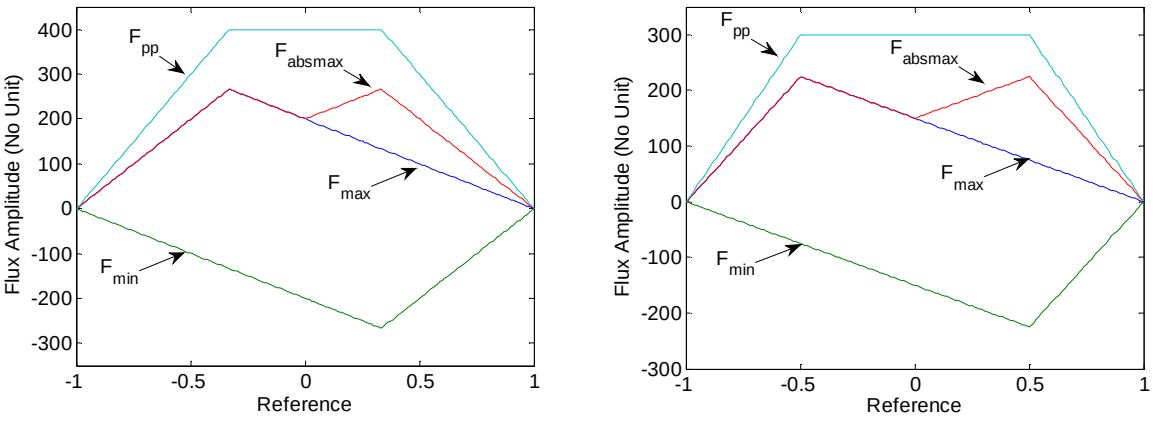
would be interesting to find the optimal CMO for systems where each phase is fed by N cells, where N is greater than 2. To find the optimal CMO we could do the same as before: analyze the behavior of the integral of the voltage difference between two cells of an ICT by sweeping the reference from its minimum value (-1) to its maximum value (+1).

In order to illustrate this method, we will apply it to two systems: one containing 3 commutation cells per phase (Figure V.20a) and the other containing 4 commutation cells per phase (Figure V.20b). The image of the calculated flux values is shown in Figure V.21 for 3 and 4 commutation cells for each phase. Note that it is different from the 2-cell case since the maximum oscillation does not occur at reference equal to 0. In fact, the maximum oscillation occurs twice in all the range, at references equal to $\pm(1-2/N)$, where N is the number of paralleled cells in each phase. The same as in the 2-cell case, for low modulation indexes, the optimal CMO is the maximum or the minimum possible offset. However, when modulation index is high, 4 solutions are possible and the analysis to find the best CMO is not simple. Instead, we may make use of massive calculation in order to find the optimal CMO.



a) 3 commutation cells per phase *b) 4 commutation cells per phase*

Figure V.20: System topologies with 3 and 4 commutation cells per phase.



a) 3 commutation cells per phase *b) 4 commutation cells per phase*

Figure V.21: Flux values for all possible reference values in 3- and 4-cell ICTs.

The idea is to add an offset to the 3 reference signals and calculate the maximum flux in the 3 ICTs for each angle in each modulation index. Only a range of 120° needs to be calculated since it is a three-phase system. The calculation of the flux is made as follows:

1. The triangular carriers are created with a certain number of points.
2. They are compared to the reference of the 3 phases summed with the offset to result on the switched voltage of each phase.
3. The average values of the switched voltages are calculated and subtracted.
4. The flux is calculated by integrating the modified switched voltage.
5. The peak values of the flux are found.

By sweeping all possible offsets it is possible to find for each angle the offset giving the lower value for the highest (among the 3 phases) peak flux, and such an optimal zero sequence can be found for each modulation index.

To precisely find the optimal CMO a great number of points in the carriers is needed as well as a great number of angles and modulation indexes. The number of offsets to be swept is probably the factor which limits the accuracy of the results presented here and using optimization routines would probably improve accuracy and reduce computational time.

The method described above was applied to find the optimal CMO for 3 and 4 commutation cells per phase and their waveforms are shown in Figure V.22 and Figure V.23, respectively. The MATLAB script used for finding the optimal CMO for 3 commutation cells is shown in the Appendix A.

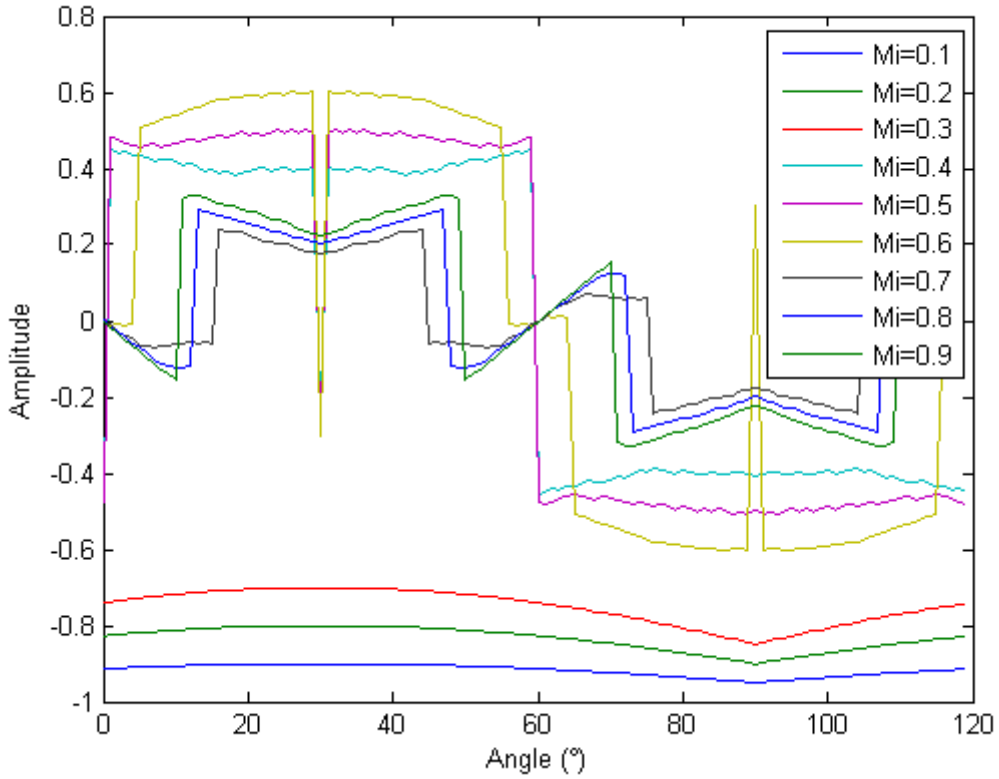


Figure V.22: Optimal CMO for 3 commutation cells per phase.

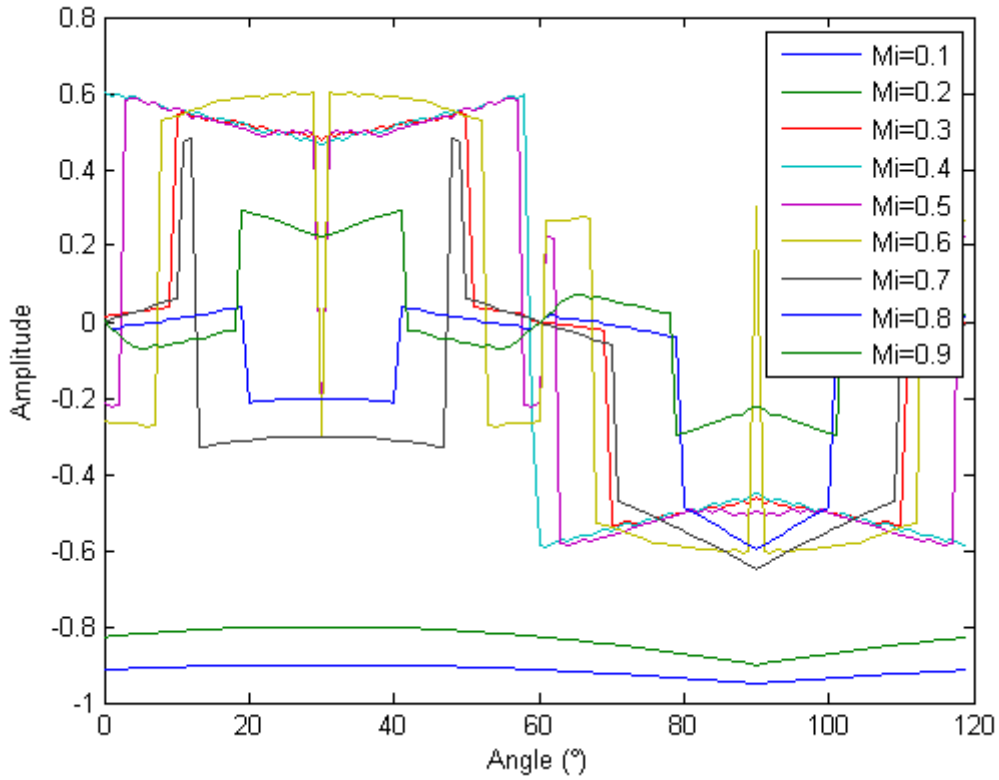


Figure V.23: Optimal CMO for 4 commutation cells per phase.

Note that, in effect, the optimal CMO is equal to the one related to the maximum (or also the minimum) possible offset for low modulation indexes, as it happens for the 2-cell case. However, for high modulation indexes the optimal offsets are different and, for the moment, no simple equation was found to represent these curves. For certain angles and some modulation indexes there are 2 offsets giving the same optimal behavior and this causes offset steps because the numerical algorithm hesitates between the two solutions.

V.2.1.2 Comparison Between Different PWM Methods in Terms of ICT Flux

With the purpose of verifying the advantage of the optimal CMO over the most common CMOs, comparison among the optimal and the ones shown in Figure V.10 will be performed.

A script using MATLAB software was written to calculate the high frequency flux for all angles of the fundamental period, and this for each PWM method applied to a system containing 2 commutation cells per phase. The highest flux ripple of each PWM method is plotted in Figure V.24 for modulation indexes ranging from 0.1 to 0.9.

As told before, the best CMO for low frequencies is any DPWM. For higher modulation indexes (approximately >0.46), applying equation (V-5) gives the lowest flux ripple. Beyond approximately 0.76, the CMO calculated using equation (V-5) must be modified to account for saturation. The resulting strategy will be called PWMBCNP and it gives the lowest maximum peak flux over the full modulation range.

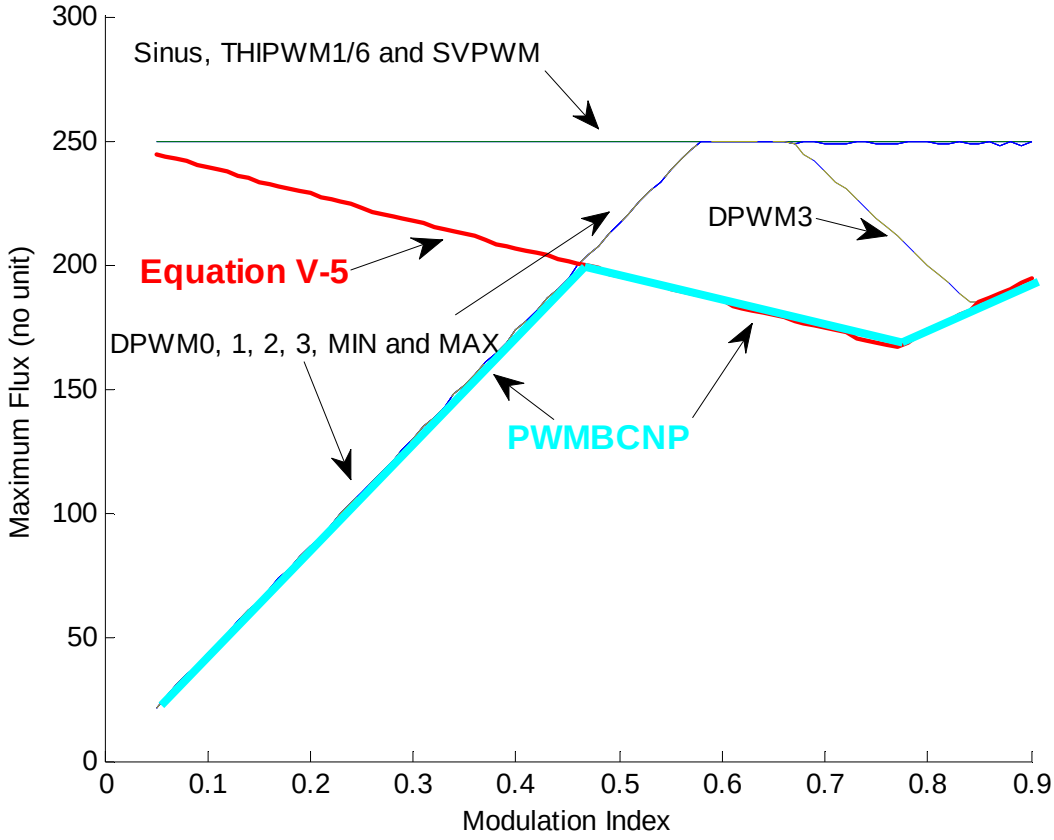


Figure V.24: Maximum flux ripple for different PWM methods.

The gain obtained by the use of this optimal PWM method, instead of any other of the common methods, may be evaluated by using Figure V.24 and the optimization algorithms presented in Chapter IV. By Figure V.24, the maximum flux ripple in the whole modulation index range using the PWMBCNP method is around 20% smaller than the one in any other method.

It should be noted that for an ICT design where the flux ripple is much higher than low frequency flux (which is usually the case for three-phase loads like motors), such a flux ripple reduction may bring a significant reduction of the size of the ICT core.

IMPORTANT CONCLUSION #1: The use of the PWMBCNP method may reduce 20% the maximum flux ripple in an ICT core.

It is important to consider that the development of PWMBCNP and Figure V.24 was based on the maximum flux ripple over one period of the fundamental waveform. As seen in Chapter III, the maximum flux ripple is not the only quantity which tells if the core will be smaller or bigger. Actually the overall flux ripple is also important since it creates core losses which have a direct influence on the core size. The CMO could thus be compared in terms of core losses. PSIM simulations have been performed to have a first insight about which CMO gives fewer ICT core losses. The results are shown in Figure V.25 for simulations using the same modulation index ($Mi = 0.7$).

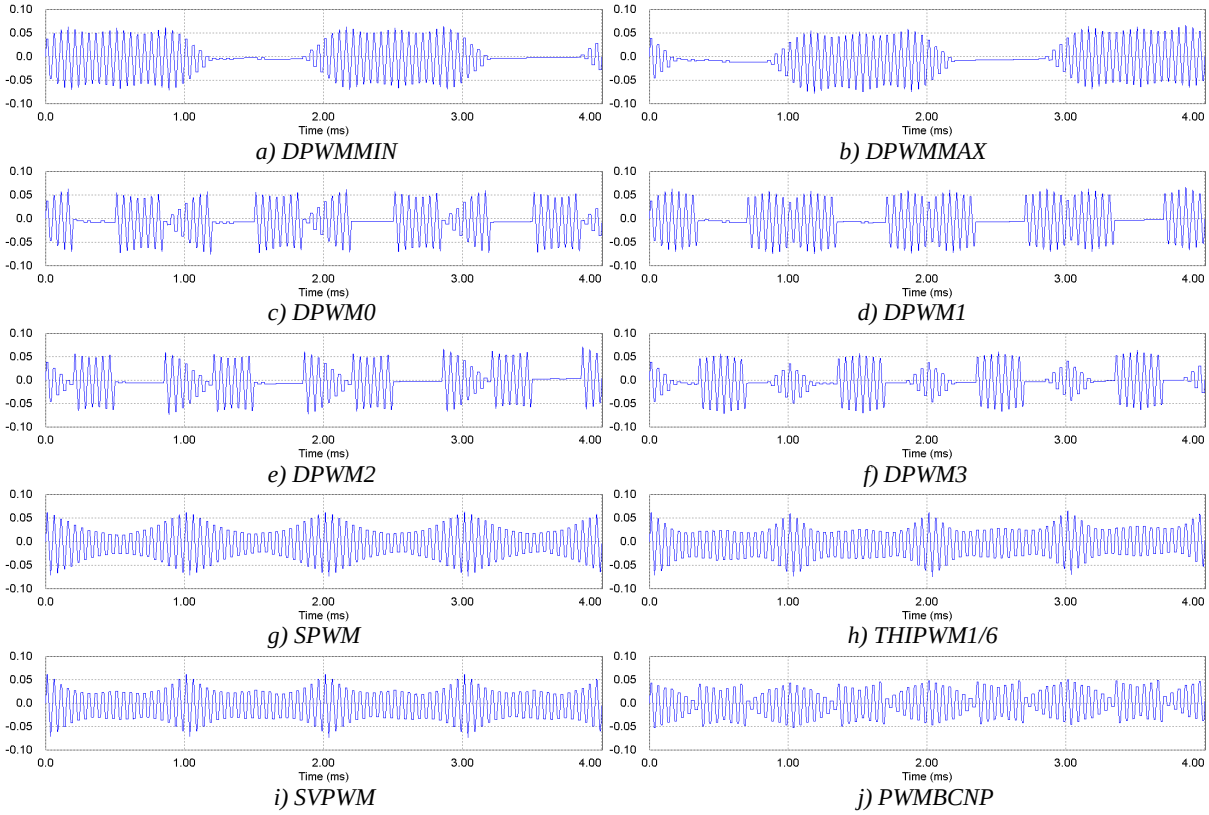


Figure V.25: ICT flux waveform for different PWM methods.

From the figure above, it can be seen that with discontinuous PWM methods there are time intervals with no flux oscillation which helps reducing core losses.

As a result of all the discussion in this section, for high modulation indexes, DPWM strategies reduce losses but PWMBCNP minimizes the peak flux; depending on the application, the best CMO choice could be any DPWM, PWMBCNP or even some CMO in between. The ideal would be to insert the optimization of the CMO inside the general algorithm of the ICT optimization. But since it seems to be an extremely hard task, the best option would be to understand the relative influence of the maximum and the overall flux ripple in the design of an ICT for a specific application in order to create a criterion to be minimized. Obviously this criterion would be based on the maximum and the overall flux ripple and the optimal CMO would be found for the minimization of this criterion.

For systems with 3 or 4 commutation cells per phase, the comparison of the maximum flux ripple for all PWM methods is shown in Figure V.26 and Figure V.27 respectively. Since we did not develop equations for the optimal CMO for 3 and 4 cells, we directly used the resulting CMOs shown in Figure V.22 and Figure V.23, which will be called, from now on, PWMBC3NP and PWMBC4NP, respectively. The resolution of these two figures is not great because the optimal CMOs were only calculated for 9 modulation indexes.

We can see that PWMBC3NP and PWMBC4NP are better than the regular PWM methods for high modulation indexes and that there is a reduction in the maximum flux ripple of approximately 15% and 14% for the 3- and 4-cell case respectively.

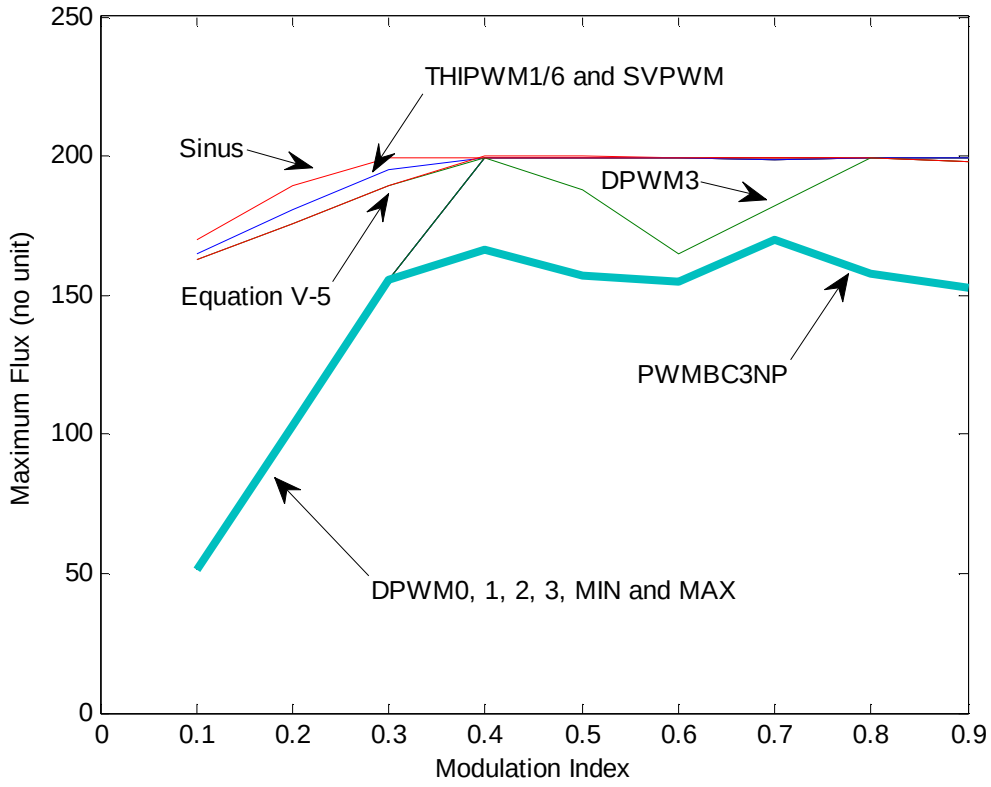


Figure V.26: Maximum flux ripple for different PWM methods for the 3-cell case.

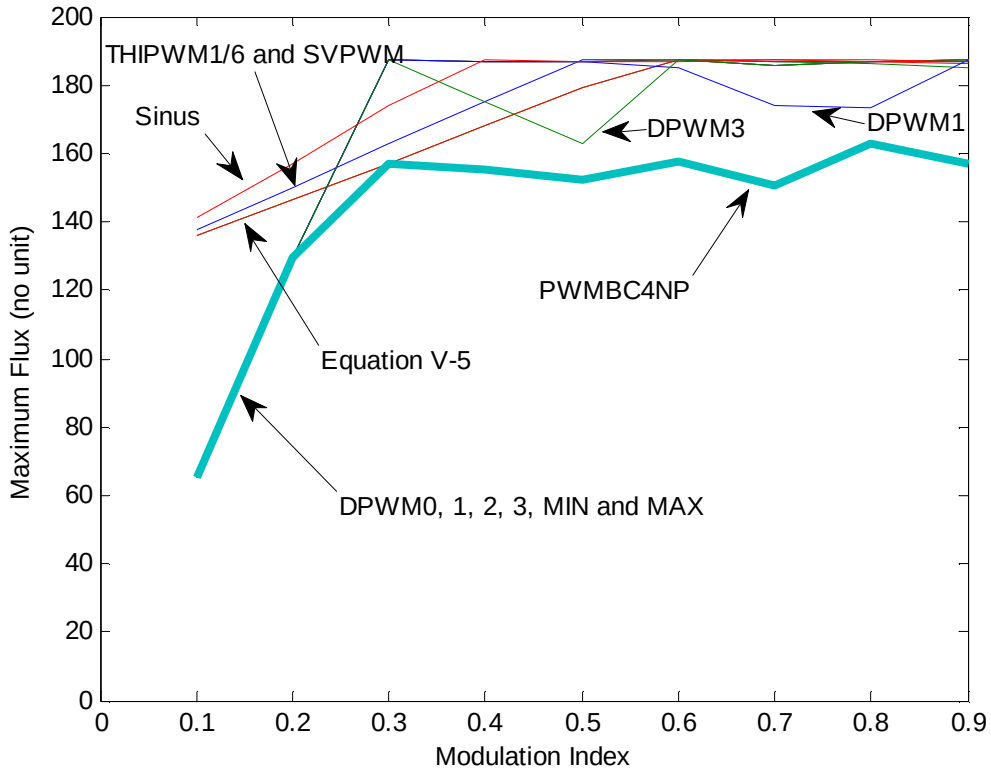


Figure V.27: Maximum flux ripple for different PWM methods for the 4-cell case.

V.2.2 Separate Neutral Point Topologies

When a three-phase load is naturally divided in 2 or more sub-loads or when designers of this load (which can be a motor or a transformer, for example) propose it this way, some advantages in the ICT design are observed.

The first one is the gain of one degree of freedom by the fact that sub-systems may have different neutral voltages and so we can use one different CMO for each sub-system at the same time. We will start by fixing the same CMO for both sub-systems and then we will show that making them different does not help on reducing the flux in an ICT.

The most noticeable advantage is the reduction on the maximum flux ripple in the ICT. This can be explained by analyzing equation (V-2). The flux oscillation is determined by the integral of the voltage difference V_{X1}-V_{X2} (where X = U,V,W). For the case of separate neutral points we will use as reference the Figure V.28 where a RLE load (such as a motor) is chosen as the reference load.

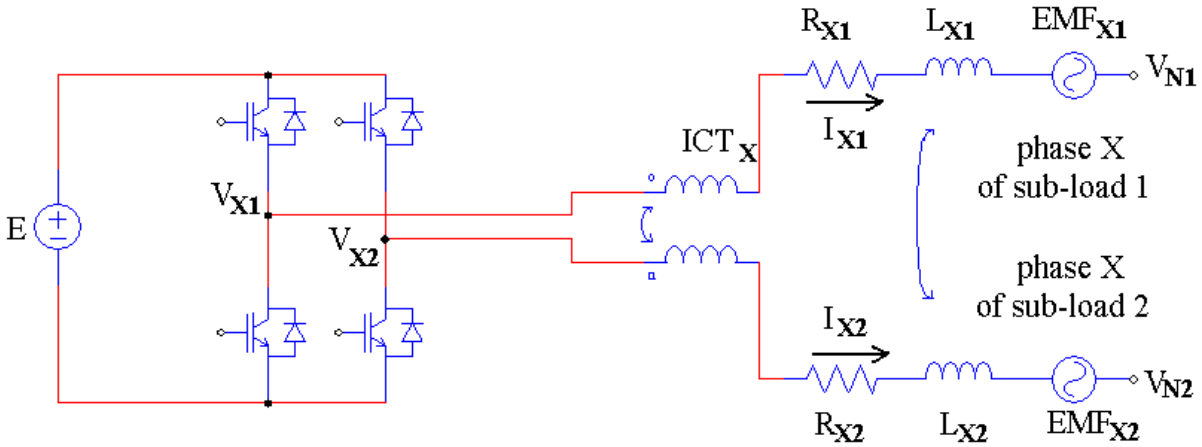


Figure V.28: One phase of the dual three-phase inverter feeding a dual three-phase load, coupled by one ICT.

As in the case of connected neutral point, the flux in the ICT depends basically on the current flowing through each winding of the ICT (I_{X1} and I_{X2}, where X = U,V,W), the number of turns of each winding (N_t) and the core reluctance (*RelCore*) if we consider that the equivalent air reluctance (*RelAir*) is high when compared to the core reluctance, as shown in the equation (V-1). Neglecting the series resistance of the ICT and of the load, the flux will only depend on the integral of the voltage difference between each phase, its corresponding neutral point and EMF, and also on the mutual and self inductances of the ICT (M_{ICT} and L_{ICT}) and the load (M and L), as shown in equation (V-6):

$$\phi = \frac{N_t}{RelCore} \frac{\int ((V_{X1} - EMF_1 - V_{N1}) - (V_{X2} - EMF_2 - V_{N2}))}{(L_{ICT} - M_{ICT}) + (L - M)} \qquad \text{(V-6)}$$

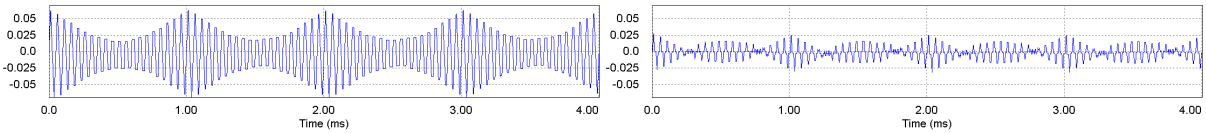
And since

$$V_{N1} = \frac{V_{U1} + V_{V1} + V_{W1}}{3} \qquad \text{and} \qquad V_{N2} = \frac{V_{U2} + V_{V2} + V_{W2}}{3} \qquad \text{(V-7)}$$

if we compare equations (V-2) and (V-6) we observe first that the total inductance when neutral points are separate is higher and thus the flux is smaller. This is not a strong argument since usually coefficient (L_{ICT} – M_{ICT}) is much greater than (L – M). The main difference comes from the fact that for the disconnected neutral point case, the flux depends not only on

the voltages of the two commutation cells connected to the ICT but also on the neutral voltages, which depend on the voltages from the other 4 commutation cells.

Figure V.29 shows a simulation using PSIM software to verify the difference between the flux in the connected neutral point and in the separate neutral point topologies using POD method (the explanation why specifying the POD method will come in the next sub-section). No CMO is injected in the reference and modulation index is equal to 0.7. In Figure V.30, a comparison between the two topologies is performed by calculating the maximum flux ripple for each modulation index also when no CMO is injected. Note that the maximum flux ripple when neutral points are not connected is much smaller than the case where the neutral points are connected, especially for low modulation indexes.



a) Connected neutral points *b) Separate neutral points*

Figure V.29: Flux waveforms of the same circuit with and without neutral point connection (Mi=0.7).

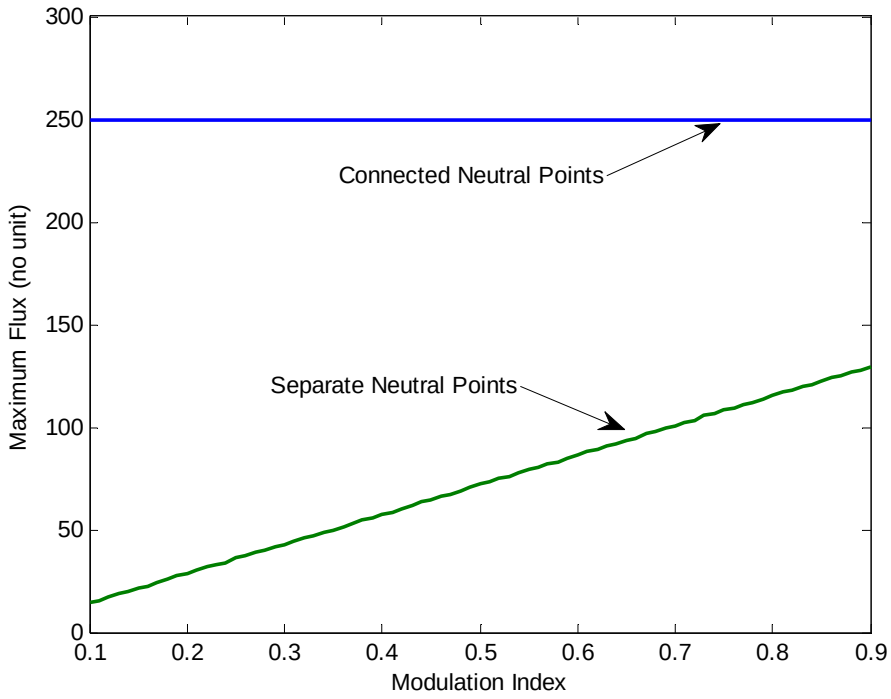


Figure V.30: Comparison of the maximum flux ripple for the same circuit with and without neutral point connection.

V.2.2.1 PD or POD?

Before trying to find the optimal CMOs for the topology with disconnected neutral points, a distinction between two cases must be made. The behavior of the flux for the POD or the PD methods is different. There were no comments about it in the past sections for the reason that the flux only depended on the voltage difference of the two cells connected to the ICT in question and these voltages are a consequence of comparison of the reference of both commutation cells to two carriers which are out of phase of 180°.

When the neutral points are disconnected, the flux in one ICT depends on the voltage in the 6 commutation cells of the converter (6 cells if we take the configuration with 2 cells

per phase as reference). In this case, one reference will be greater than 0 and the other two smaller, or vice-versa. Therefore these references will be compared to carriers which are in phase for the POD method, and 180° out of phase (at twice the switching frequency) for the PD method. The consequence on the flux can be verified in Figure V.31 where we show also the commutated voltages and phase voltages associated to both techniques (POD or PD), generated for modulation index equal to 0.5 at angle equal to 50°.

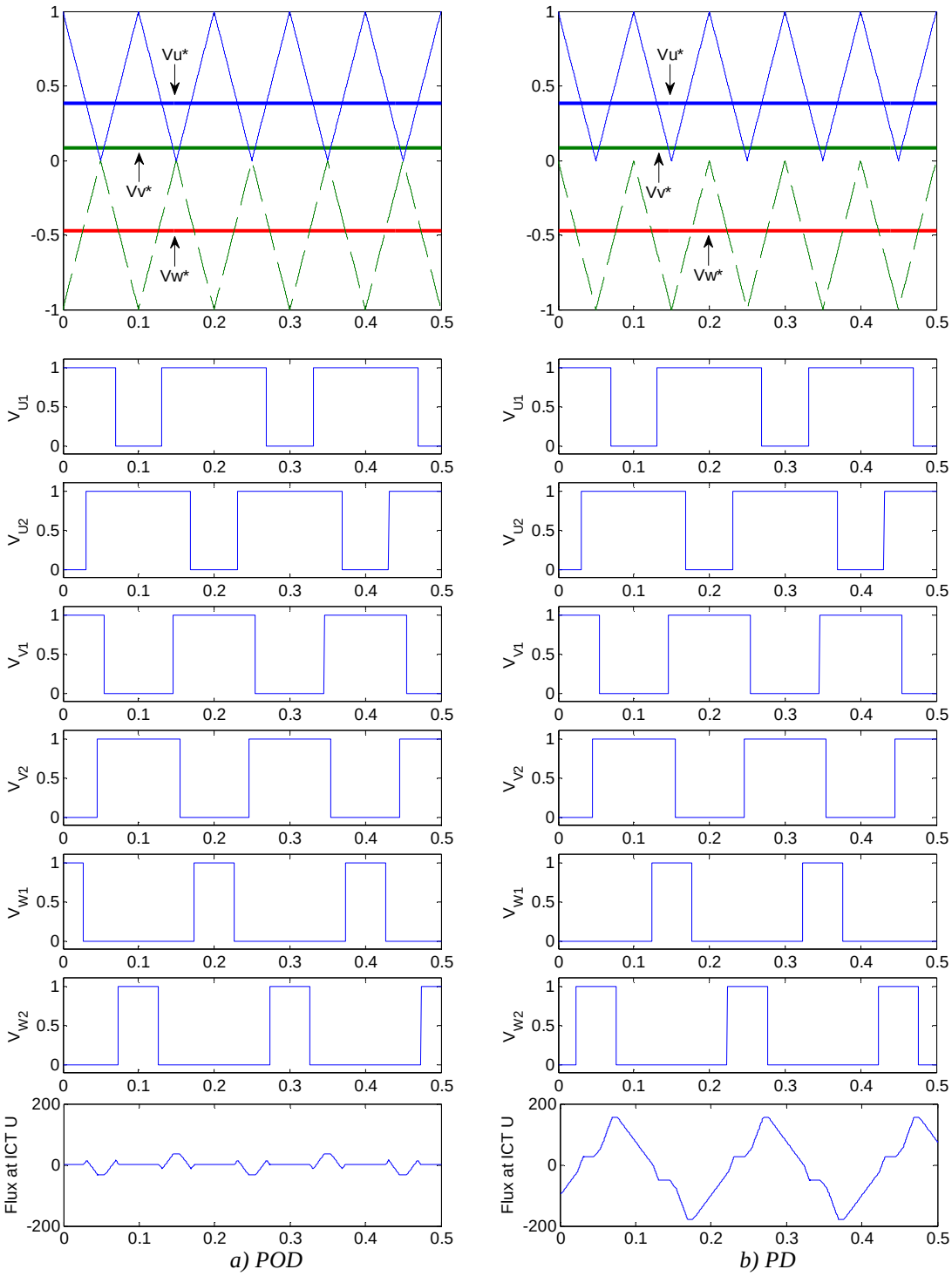


Figure V.31: Voltage reference, switching voltages and ICT flux for PD and POD techniques when Mi=0.5 and angle of the fundamental references is equal to 50°.

If we compare the flux obtained with these two methods we will see a great difference especially if there is no CMO to minimize it. Figure V.32 shows the maximum flux ripple of different modulation indexes for these two methods: red dashed lines related to PD and blue lines related to POD. Note that the flux ripple using the POD increases with the modulation index and using the PD it decreases. Also note that POD always produces less flux than PD, particularly in low modulation indexes as it is shown in Figure V.33, which presents the ratio between the flux ripple using POD and PD, for different modulation indexes. It is important to remember that this comparison is obtainable considering that the problem of "flux steps" present in the PD method is eliminated as explained in the first section of this chapter.

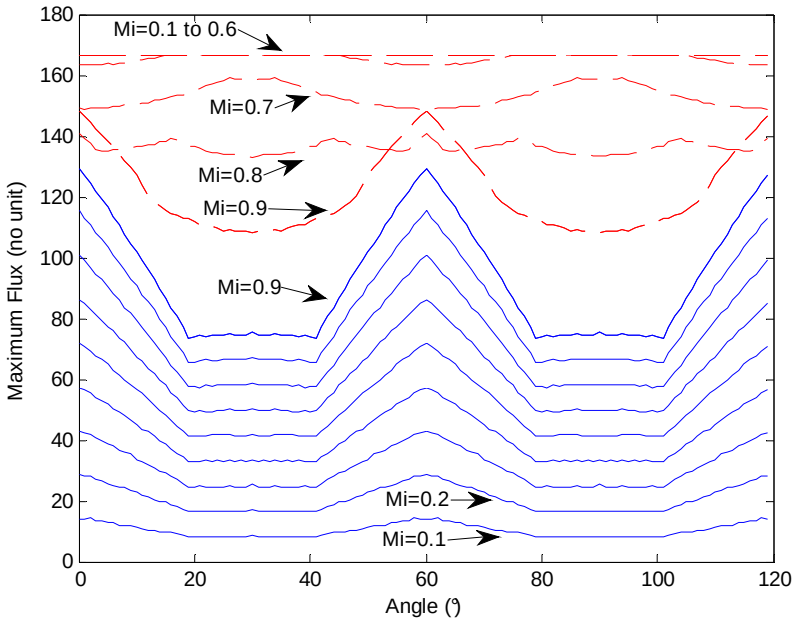


Figure V.32: Comparison of maximum flux ripples using POD (blue lines) and PD (red dashed lines) techniques.

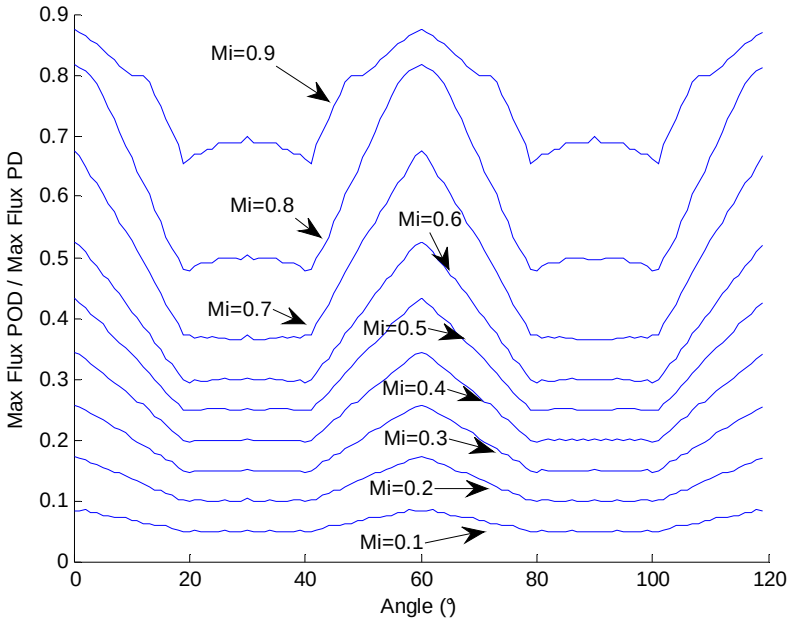


Figure V.33: Ratio between maximum flux ripples using POD and PD techniques.

Having these differences in mind, it is reasonable to conclude that there is an optimal CMO when using POD method and another when using PD method. Also each different PWM method based on the injection of CMO will have a different result if used with POD or PD methods.

V.2.2.2 Optimal CMO for 2 Commutation Cells, Using POD Technique

Using a graphical method to find the optimal CMO, as it was done for the case where the neutral points were connected, is not the best option since now the flux flowing in one ICT depends on the voltages at the output of each of the 6 commutation cells. The best way to find the optimal CMO is to use the approach explained before. By sweeping all possible offset values for each angle and each modulation index, we calculate the maximum flux ripple and we find the offset which minimizes it. Applying this idea to the present topology, the results are the curves shown in Figure V.34. Again only 120° of the fundamental period is shown since it is a three-phase system. The number of points used to calculate these curves is high and we show in Appendix B that a small number of points may lead to very different and incorrect CMOs.

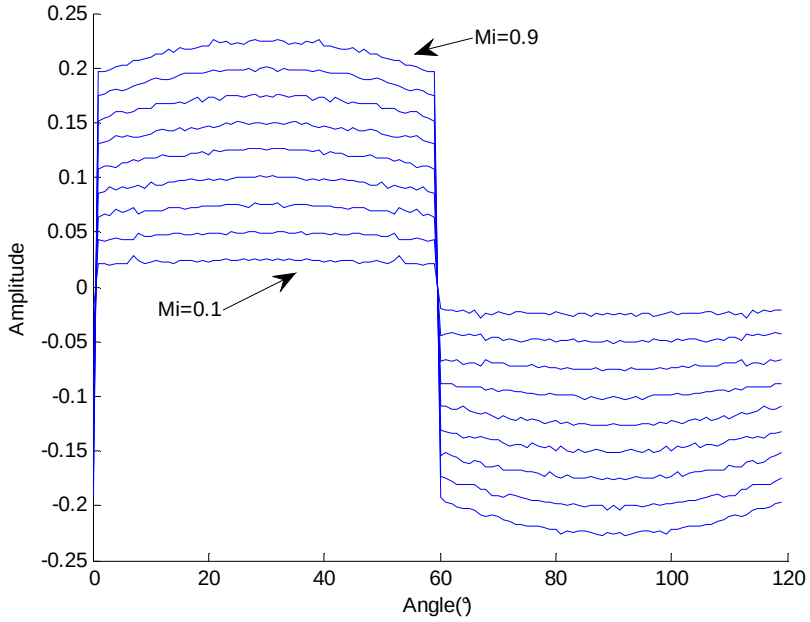


Figure V.34: Optimal CMO found by offset sweeping.

These are simple curves and it seems easy to find an equation which describes its behavior. In fact comparing the curves above with the sinusoidal references of the three phases we can find that the CMO is equal to -¼ of the reference which has the maximum absolute value. It can be described by the equation below:

$$
\begin{aligned}
&v_0^* = -v_x^*/4 && \text{where} && \\
&v_x^* = v_u^* && \text{if} && abs(v_u^*) = \max\left(abs(v_u^*), abs(v_v^*), abs(v_w^*)\right) \\
&v_x^* = v_v^* && \text{if} && abs(v_v^*) = \max\left(abs(v_u^*), abs(v_v^*), abs(v_w^*)\right) \\
&v_x^* = v_w^* && \text{if} && abs(v_w^*) = \max\left(abs(v_u^*), abs(v_v^*), abs(v_w^*)\right)
\end{aligned}
\qquad \text{(V-8)}
$$

Comparing this equation with the values obtained with the "offset sweeping" we see by Figure V.35 that they match perfectly. From now on the method using this CMO will be called PWMBC in order to simplify the text of the dissertation and an example of the reference modified by this CMO is shown in Figure V.36.

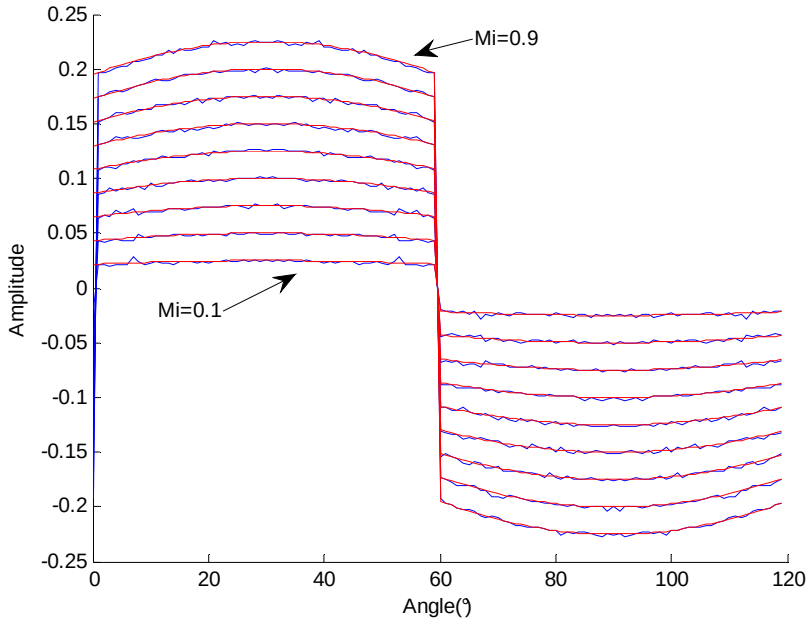


Figure V.35: Comparison between optimal CMO found by offset sweeping and by equation (V-8).

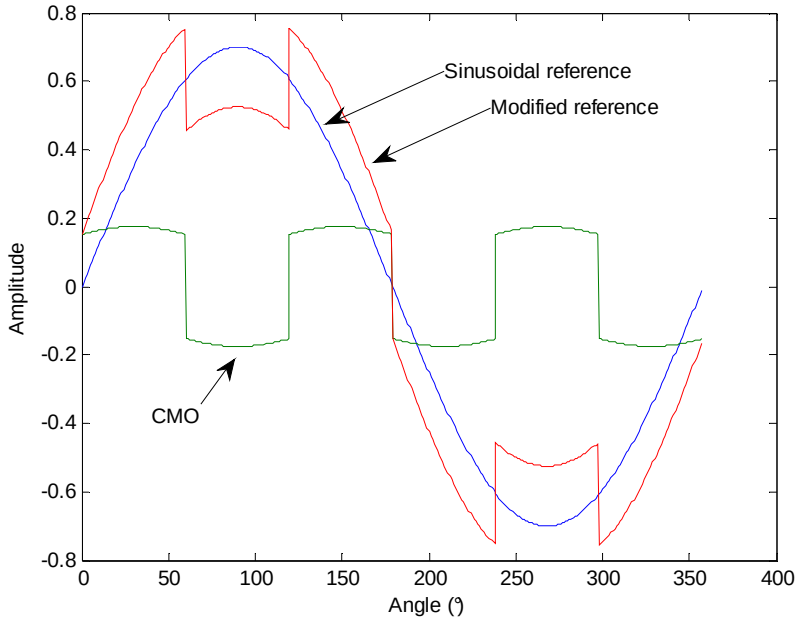


Figure V.36: Modulation waveforms of PWMBC method (Mi=0.7).

The flux reduction provided by PWMBC is shown in Figure V.37 where the red dashed lines correspond to the flux ripple after the optimal CMO injection and the blue lines stand for the flux ripple when no CMO is injected. Note the great advantage of the zero sequence signal injection: besides the fact that the maximum flux ripple is approximately 22%

smaller, the overall flux ripple (or “average flux ripple”, which can be calculated by using the area under the each curve) is even more reduced.

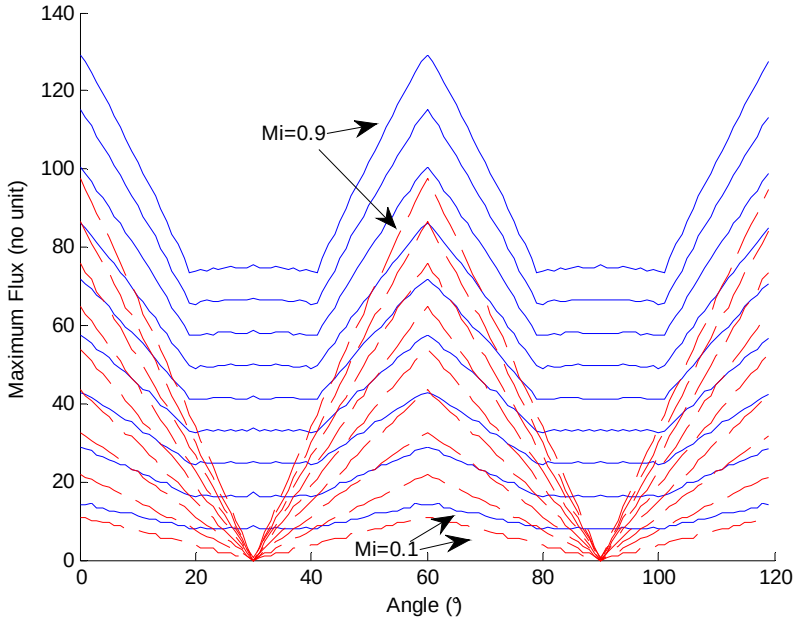


Figure V.37: Comparison of maximum flux ripples using SPWM (blue lines) and PWMBC (red dashed lines) methods and POD technique.

The same way as performed to the PWMBCNP, the PWMBC offsets must be modified in very high modulation indexes and in the overmodulation region in order to maintain the output voltages free of distortion. Figure V.38 shows the CMO for different modulation indexes in overmodulation region.

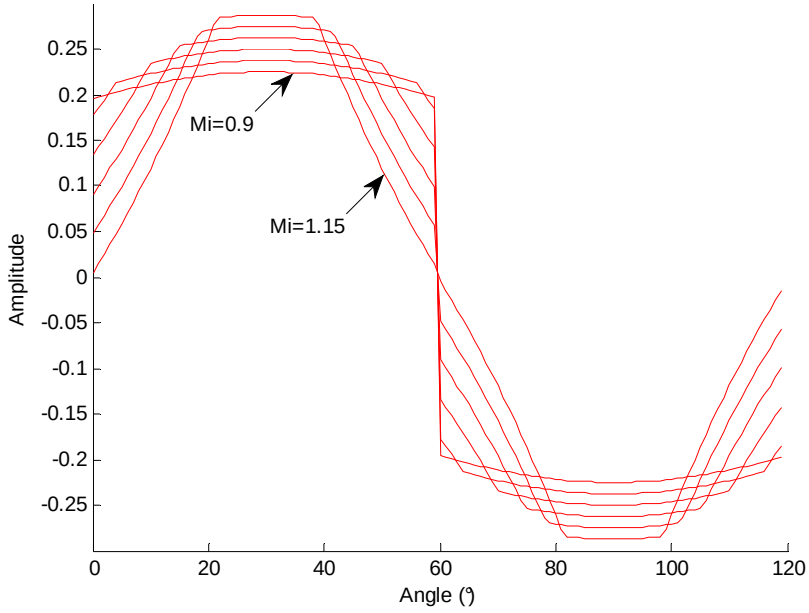


Figure V.38: PWMBC offsets in high modulation index and overmodulation regions.

This compensation is simply calculated by predicting the amount of the reference which exceeds 1 (or -1) for each angle. This amount is subtracted from the original CMO and, as a result, the reference is limited to +1 or -1. Thus this is still the optimal CMO with regard to the flux in the ICT, even in the overmodulation region. To illustrate the calculation of this compensation as well as the CMO, a MATLAB code is shown below. Note that modulation indexes greater than 1.15 cannot be totally compensated and distortion in the output voltage will exist.

```
If ((abs(Vu)>=abs(Vv))&&(abs(Vu)>=abs(Vw)))
    temp = max(abs(Vw),abs(Vv)) + abs(Vu)/4 - 1;
    Offset= -Vu/4 + ((temp>0)*temp*sign(Vu));
elseif ((abs(Vv)>=abs(Vu))&&(abs(Vv)>=abs(Vw)))
    temp = max(abs(Vu),abs(Vw)) + abs(Vv)/4 - 1;
    Offset= -Vv/4 + ((temp>0)*temp*sign(Vv));
else
    temp = max(abs(Vv),abs(Vu)) + abs(Vw)/4 - 1;
    Offset= -Vw/4 + ((temp>0)*temp*sign(Vw));
end
```

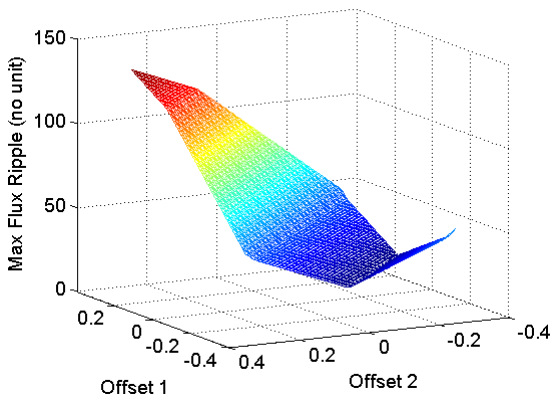
V.2.2.2.a Different offsets for different commutation cells of the same phase?

Until now we have just searched for optimal CMOs considering that the offset is the same for both converters. Given that the two sub-loads have no connection between their neutral points, it is interesting to think that we could use different offsets in each converter to further reduce the flux oscillation inside the ICT.

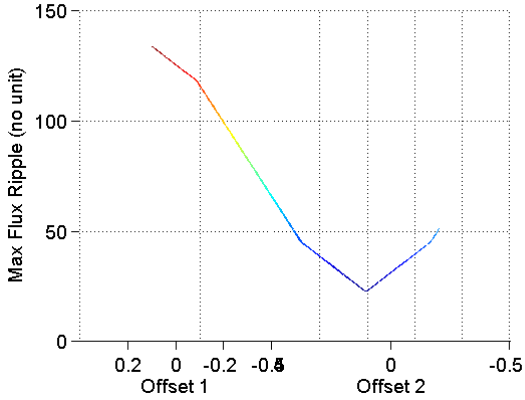
This is not true and we will explain why.

We decided to take an angle (80°) and a modulation index (*Mi*=0.6) and to plot the flux ripple for different possible offsets in converter 1 (*offset 1*) and in converter 2 (*offset 2*), without fixing a constraint that both offsets must be the same. The result is a 3D plot shown in Figure V.39a. By taking this 3D plot and showing it in the right angle (Figure V.39b) we can see that it gives the impression to be a 2D curve. It means that there is an infinity number of combinations of *offset 1* and *offset 2* resulting in a given flux ripple. Now if we take the top view of the 3D plot (Figure V.39c) we realize that if initially both offsets are the same and then we move them from this initial point by the same amount but in opposite directions, the maximum flux ripple will not change. In other words, if *offset 1* and *offset 2* are different, the flux ripple produced by them will have the same amplitude as if they were the same and having a value which is the average of their initial values.

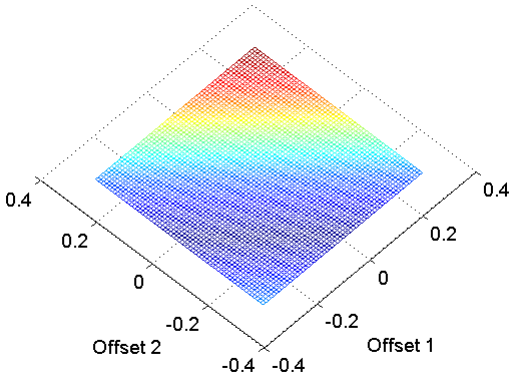
This phenomenon exists because separating the offsets from an initial common value will change the voltage in each commutation cell and in the neutral point of each sub-load in a way that the resulting flux will only change its phase, not its waveform. This can be seen in Figure V.39d where the blue lines represent the flux waveforms when *offset 1* = *x* and *offset 2* = -*x*, where *x* varies between -0.3 and +0.3 using steps equal to 0.01.



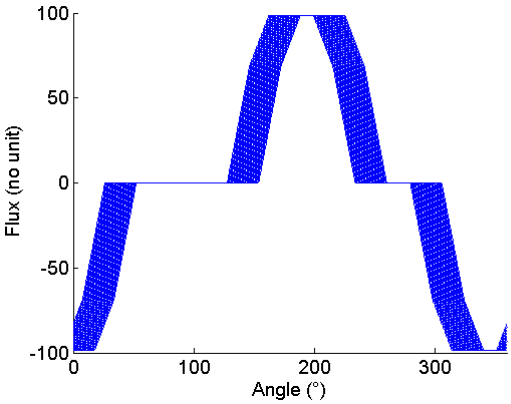
a) 3D plot



b) Right angle of figure a)



c) Top view of 3D plot



d) Flux shift with different offsets

Figure V.39: Flux behavior when different offsets are applied to the dual three-phase converters. Angle = 80°, Mi = 0.7, Offsets from -0.3 to +0.3.

IMPORTANT CONCLUSION #2: If two ICT-coupled converters connected to two sub-loads have different Common Mode Offsets CMO_1 and CMO_2, the flux ripple will be the same as if both converters had a CMO equal to $(CMO_1+CMO_2)/2$.

As a consequence of "Important Conclusion #2", if we want to control the current difference of each phase to compensate a possible low frequency imbalance, we can directly control the difference of offsets and be certain that it will not change the flux ripple.

The optimal CMOs for more than 2 sub-systems in parallel with no neutral point connection may be found by using the approach where we sweep all possible offset values for each angle and each modulation index. These CMOs have complicated waveforms and may not be described by simple equations.

V.2.2.3 Comparison Between Different PWM Methods in Terms of ICT Fluxes, Using POD Technique

As presented in the last section, in order to verify the advantage of PWMBC over the most common PWM methods a comparison among them will be performed. The high frequency flux for all angles of the fundamental period was calculated for each PWM method, applied to a system containing 2 commutation cells per phase. The highest flux ripple of each PWM method was plotted in Figure V.40, for modulation indexes ranging from 0.1 to 0.9.

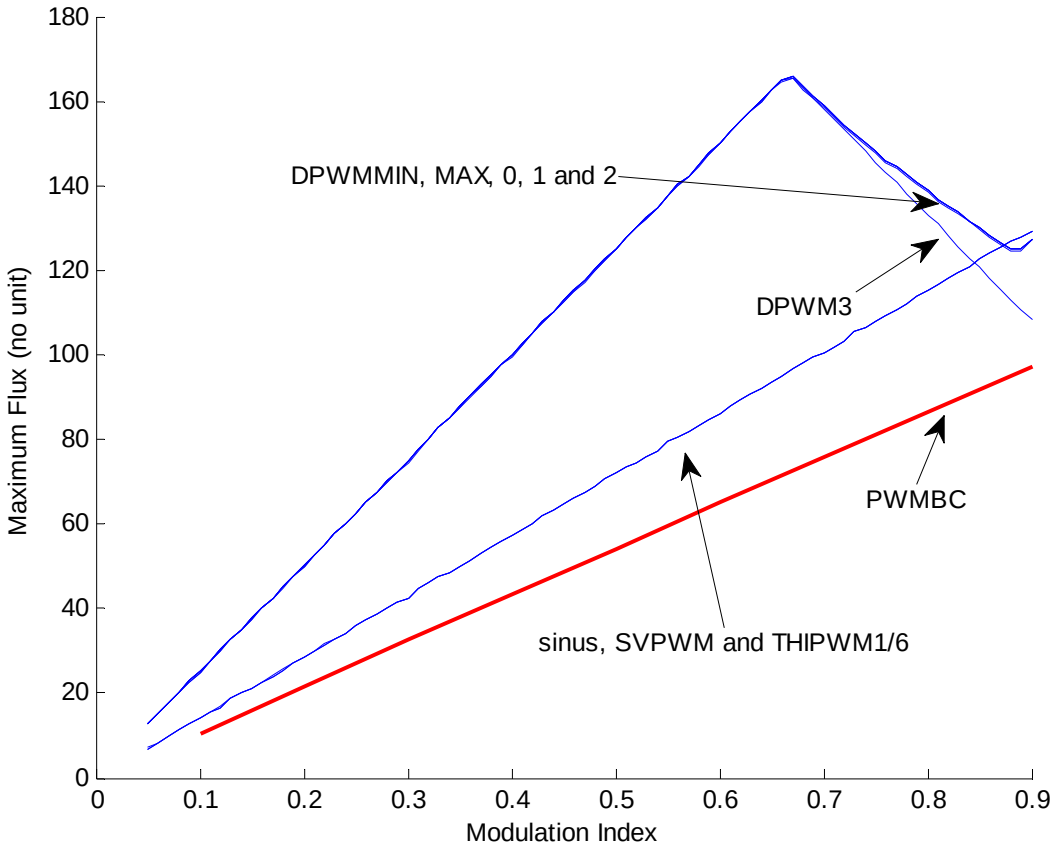


Figure V.40: Maximum flux ripple for different PWM methods.

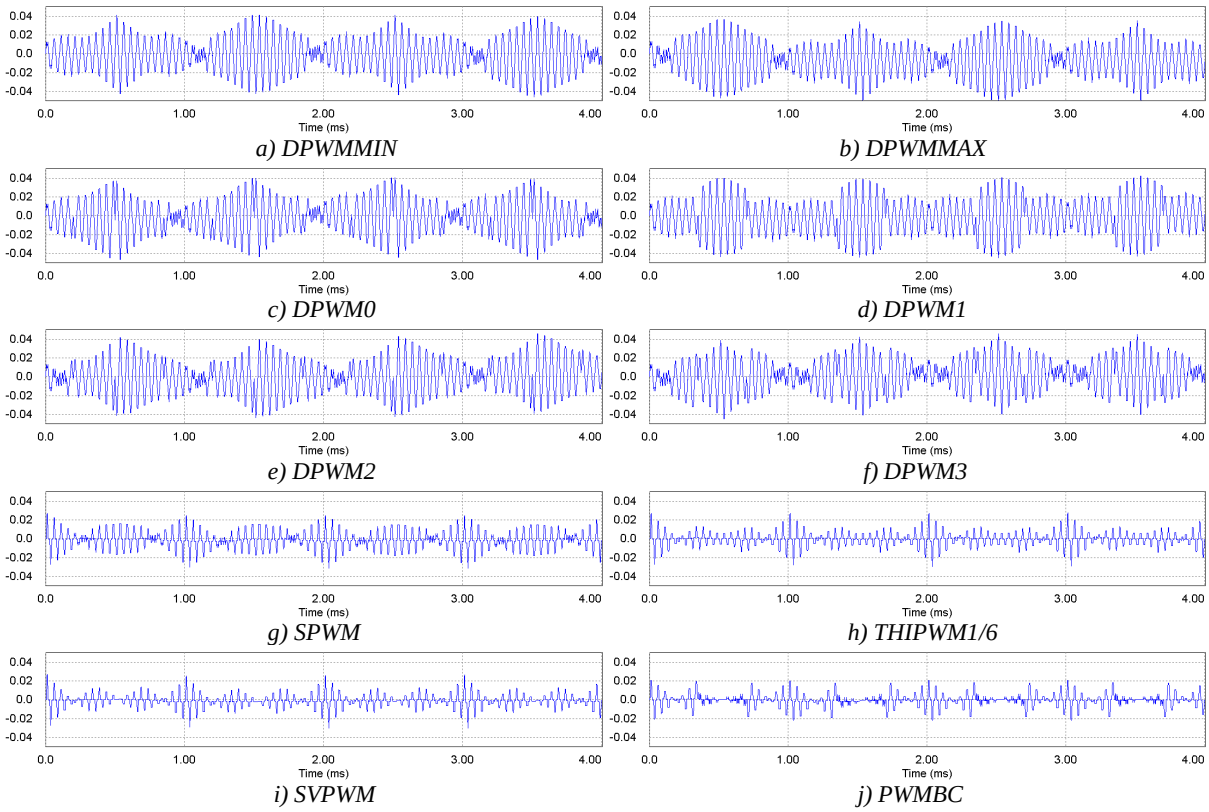
Note that PWMBC always generates less flux ripple than the other methods and that the flux reduction is approximately 22% when compared to Continuous PWM methods. It is interesting to observe that Discontinuous PWM methods produce much more flux ripple than the other methods. This is a great drawback of this type of PWM.

IMPORTANT CONCLUSION #3: The use of PWMBC method may reduce 22% the maximum flux ripple flowing through an ICT core.

PWMBC was created to minimize the maximum flux ripple in the period of the fundamental waveform. As seen in the last section, the overall flux ripple is also important in the ICT design since it engenders core losses which have a direct influence on the core size.

Simulations using PSIM were performed with the purpose of having a first insight about the flux waveform in the whole fundamental period. The results are shown in Figure V.41 for simulations using the same modulation index ($Mi = 0.7$).

Analyzing the figure above, it can be seen that continuous PWM methods behave better than discontinuous ones. Besides the fact that the maximum flux ripple is smaller using continuous PWM methods, the overall flux ripple is much smaller. Note that core losses would be much smaller with PWMBC than with any other.



a) DPWMMIN *b) DPWMMAX*

c) DPWM0 *d) DPWM1*

e) DPWM2 *f) DPWM3*

g) SPWM *h) THIPWM1/6*

i) SVPWM *j) PWMBC*

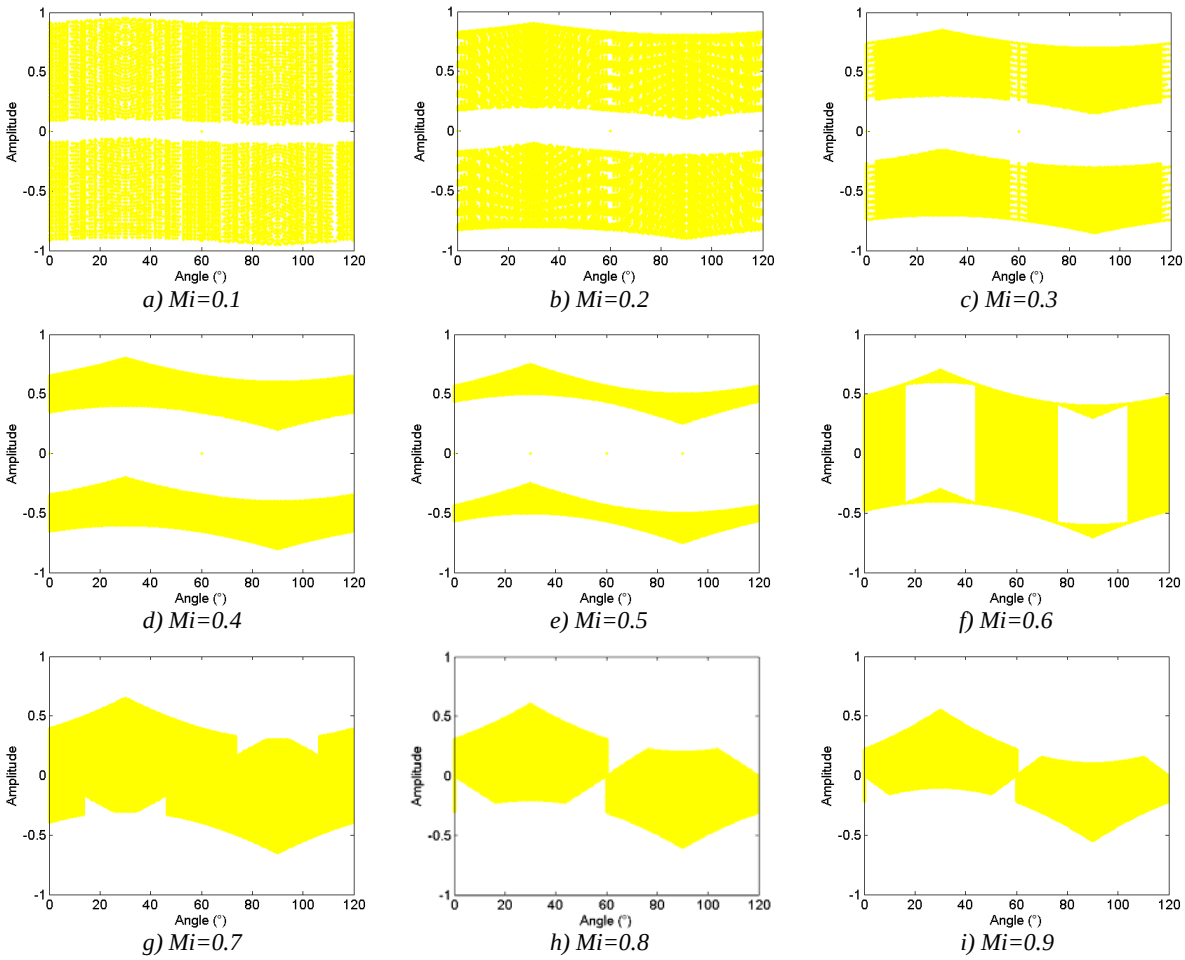
Figure V.41: ICT flux waveform for different PWM methods.

V.2.2.4 Optimal CMO for 2 Commutation Cells, Using PD Technique

Applying the idea to find the optimal CMO for the case where PD technique is used, for a given modulation index and angle, there are many different offsets which give the lowest maximum flux ripple. For this reason, a better way to find an optimal CMO is to plot all the offsets which generate a maximum flux ripple very close to the minimum numerical results. This is what it is shown in Figure V.42 where we plot using yellow circles all the offsets which generate a maximum flux ripple smaller than 1.01 times the minimum maximum flux ripple. This is done for different modulation indexes.

This figure shows that for modulation indexes lying between 0.1 and 0.6, any discontinuous PWM technique can be the optimal one. However, after Mi=0.7, the minimum and maximum offsets are not anymore the optimal ones. It means that the optimal CMO is either a specific combination of the minimum and maximum offsets, i.e. a specific discrete PWM, or a continuous PWM which crosses the zero line each 60°. Or even no offset at all!

The flux reduction provided by any discontinuous PWM (in this case DPWM3) for low modulation indexes when compared to the sinusoidal modulation is shown in Figure V.43 where the red dashed lines are the flux ripples after the CMO injection and the blue lines are the flux ripples with no CMO injected. Note that the advantage of the zero sequence signal injection only happens for low modulation indexes and that for DPWM3 the maximum flux ripple for each angle is the same as for SPWM, for Mi>0.6.



a) Mi=0.1 *b) Mi=0.2* *c) Mi=0.3*

d) Mi=0.4 *e) Mi=0.5* *f) Mi=0.6*

g) Mi=0.7 *h) Mi=0.8* *i) Mi=0.9*

Figure V.42: Offsets where the maximum flux ripple is close to the minimum numerical solution (1%).

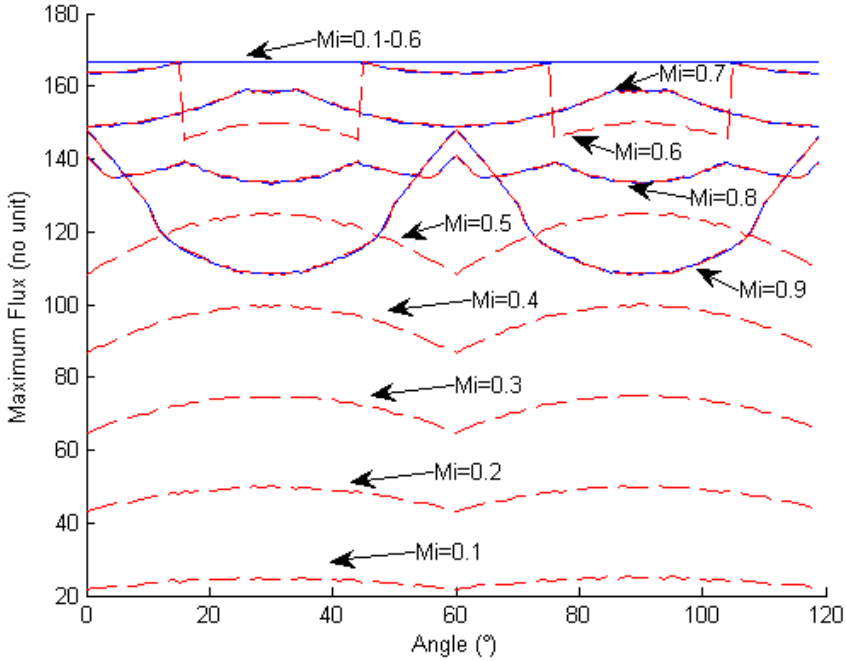


Figure V.43: Comparison of maximum flux ripples using SPWM (blue lines) and DPWM3 (red dashed lines) methods for PD technique.

V.2.2.5 Comparison Between Different PWM Methods in Terms of ICT Fluxes, Using PD Technique

The analysis presented in the last sub-section will be verified by a comparison between the most common PWM methods. The high frequency flux for all angles of the fundamental period was calculated for each PWM method applied to a system containing 2 commutation cells per phase. The highest flux ripple of each PWM method is plotted in Figure V.44, for modulation indexes ranging from 0.1 to 0.9.

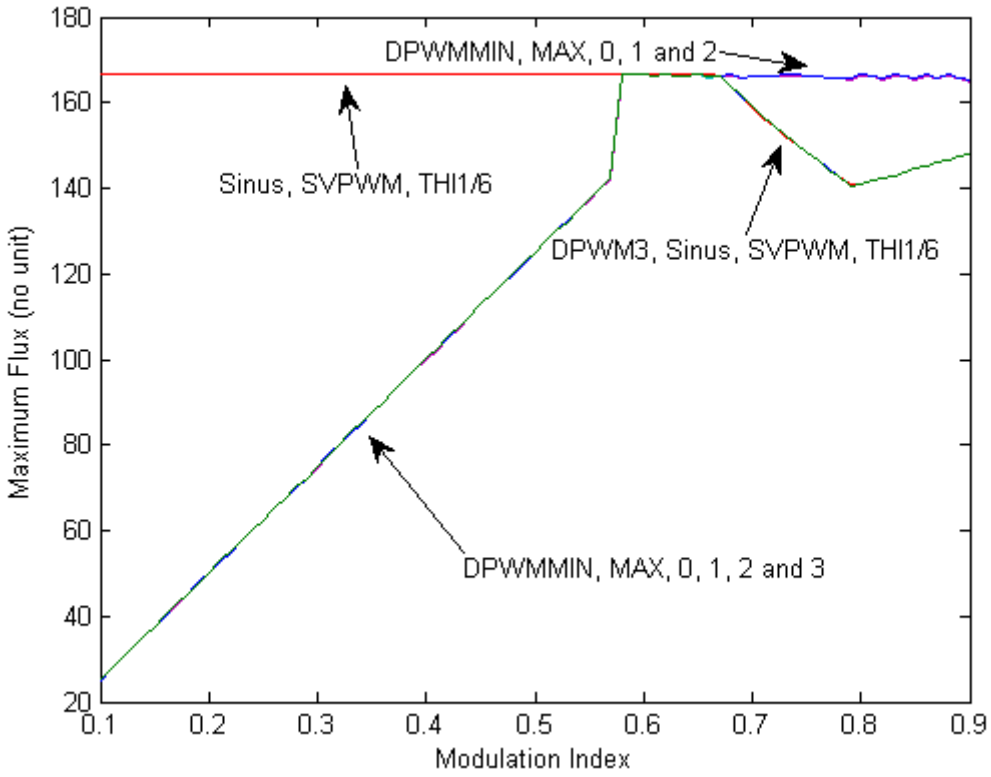


Figure V.44: Maximum flux ripple for different PWM methods.

Note that DPWM3 always generates less or equal flux ripple than the other methods. It is interesting to observe that for high modulation indexes, discrete PWM methods (excluding DPWM3) produce more flux ripple than continuous PWM methods, especially for low modulation indexes.

V.2.2.6 POD or PD When Using Optimal CMO?

After using the corresponding optimal CMO for POD and PD methods, we compare the flux issued from these two methods and we still see a great difference. Figure V.45 shows the flux ripple of different modulation indexes for these two methods: red dashed lines related to PD and blue lines related to POD. Note that POD always produces less flux than PD and the maximum flux ripple produced by POD method is 40% smaller than the one produced by PD method. Also if we compare the overall flux ripple in a fundamental period we conclude that POD method produces much less core losses than PD method. It is important to remember that this comparison is presented considering that the problem of “flux steps” present in the PD method is eliminated as explained in the first section of this chapter.

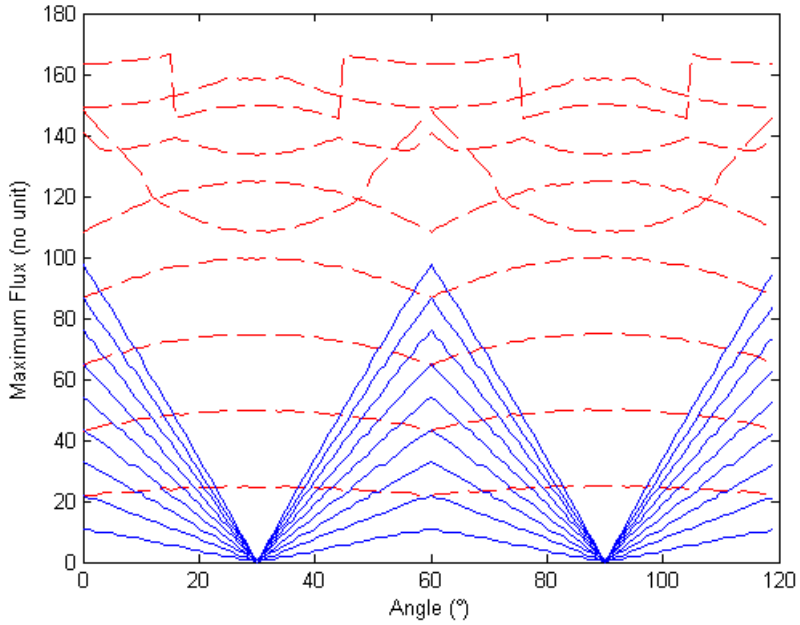


Figure V.45: Comparison of maximum flux ripples using POD (blue lines) and PD (red dashed lines) techniques, after optimal CMO.

V.3 Experimental Results

With the purpose of validating the results issued from simulations using PSIM or calculation using MATLAB, an experimental setup was developed in the laboratory. It contains 2 three-phase inverters from SEMIKRON using 1200V SEMIKRON IGBT modules (SKM50GB123D) and driver SKHI 22 as in the figure below.

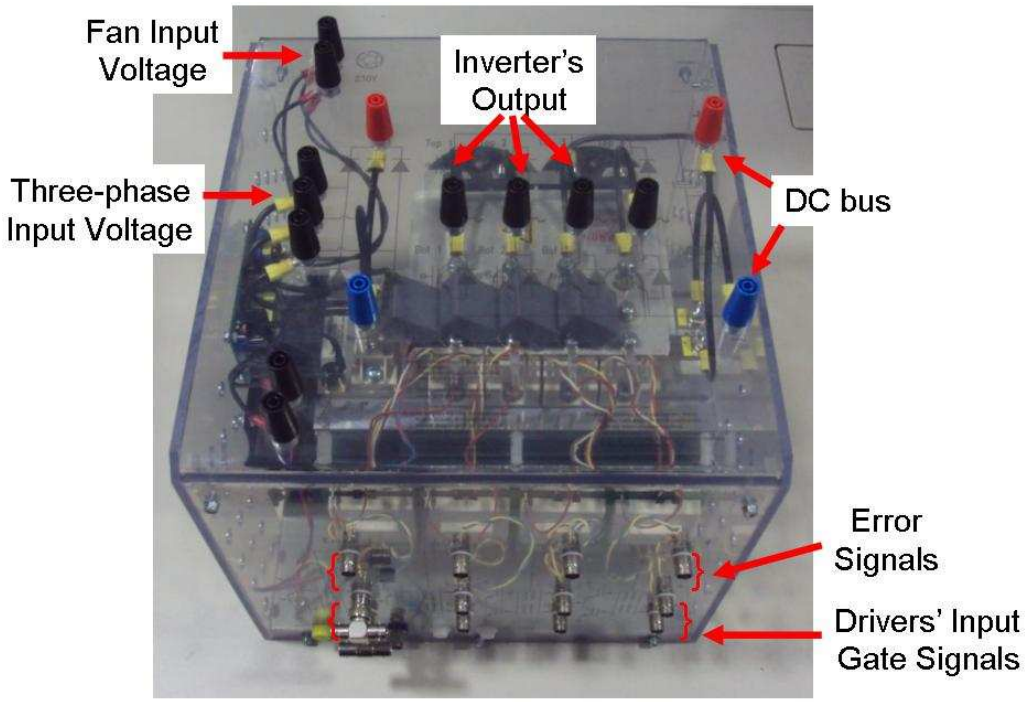


Figure V.46: Three-phase inverter used in the experimental setup (from SEMIKRON).

Each phase of each inverter is connected to a 6mH inductor designed for supporting 20Arms at 4kHz. The output of each inductor is connected to a variable three-phase resistive load.

Each inverter is controlled by a control board composed of an ALTERA ACEX 1K100 FPGA and a TMS320C6713 Texas Instruments DSP. The DSP has the function of calculating all references and control values while the FPGA generates the triangular carriers and compares them to the references values received from the DSP in order to generate the gate signals sent to both three-phase inverters. A photo of the whole experimental setup is shown in Figure V.47.

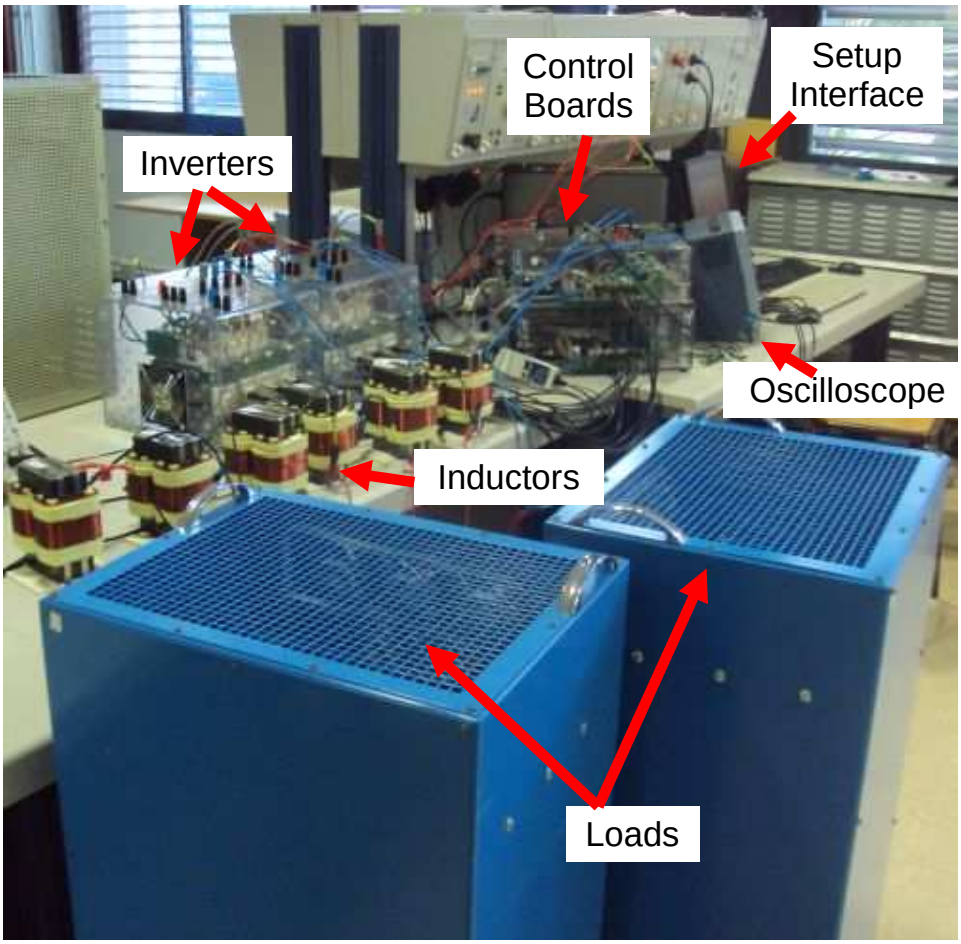


Figure V.47: Experimental setup.

The interface used for controlling the system is an Excel macro which uses the serial port of the Personal Computer to communicate with the DSP by means of RTDX protocol. It was developed so the user could easily change the following variables:

1 – The frequency of the fundamental output voltage.
2 – The gain of the closed loop proportional current controller.
3 – The PWM method, which are: SPWM, THI1/6, SVPWM, SV3PWM (for three level converters), DPWMMIN, DPWMMAX, DPWM0, DPWM1, DPWM2, DPWM3, PWMBC and PWMBCNP (this last method is equal to equation (V-5) when implemented in the experimental setup).
4 – The modulation index.

The user interface is shown in Figure V.48 where we also see some buttons to: start and stop the switching, quit the software, choose between PD or POD techniques, send variables to the controller, turn ON and OFF the closed loop control and the flux step compensation. Also we observe graphical interfaces where internal variables of the control algorithm or measured signals in the experimental setup (such as phase currents and DC bus voltage) may be plotted.

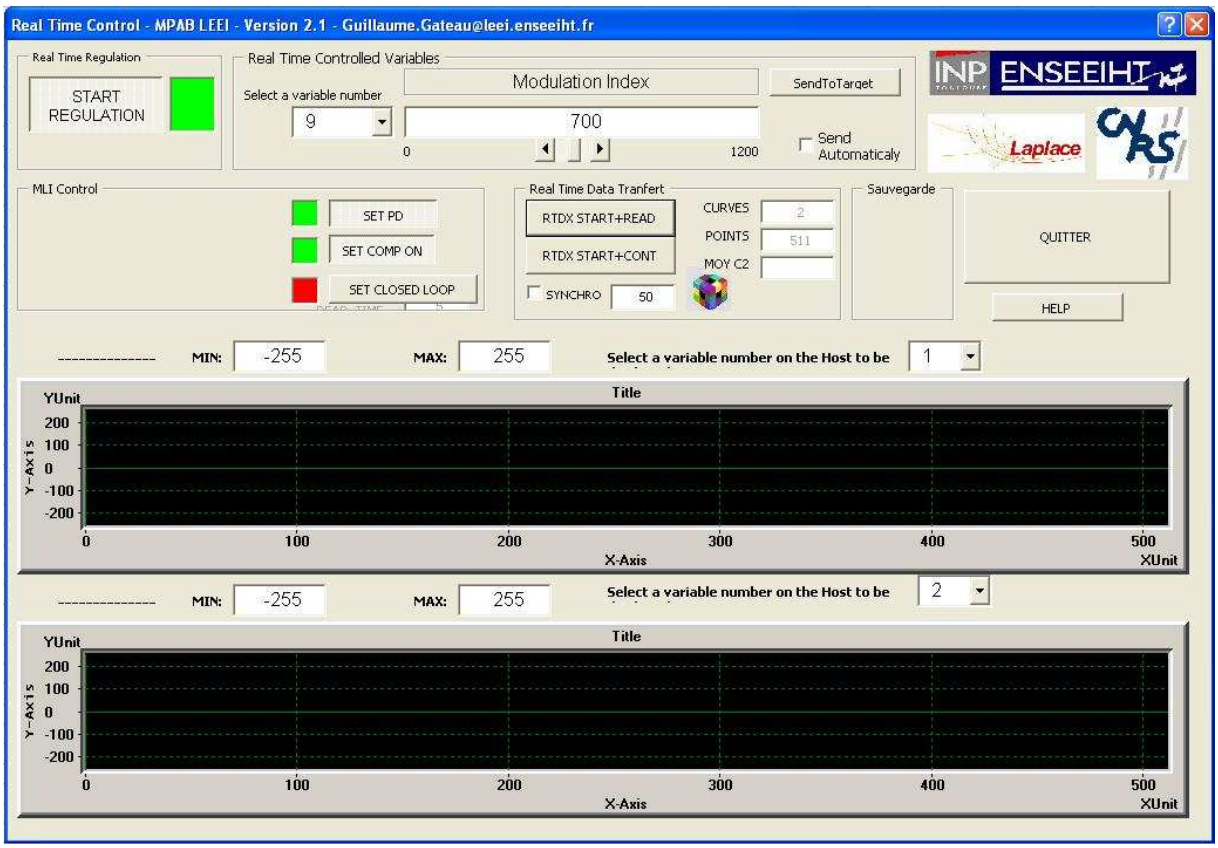


Figure V.48: User interface to control both three-phase inverters.

As told before, regular inductors were used to connect the commutation cells instead of actual coupled inductors. By equations (V-1), (V-2), (V-6) and (V-7), we can see that the flux inside the ICT is proportional to the current difference between the two commutation cells of each phase, and this is true if the mutual inductance (M_{ICT}) is high or low.

For the experimental setup constructed in the laboratory, the decision of using regular inductors was taken for the following reasons:

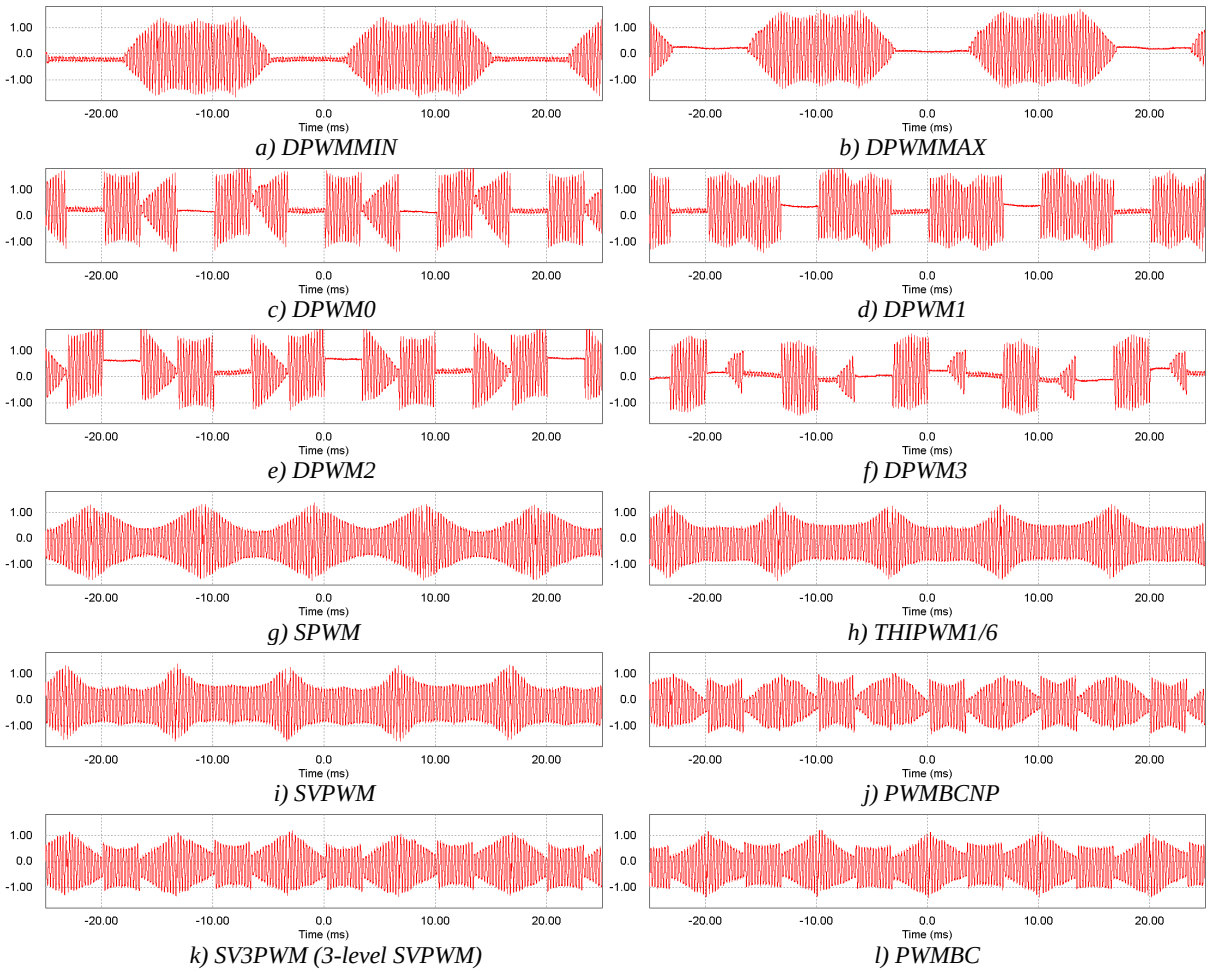
- The phenomena observed in the current difference between two commutation cells of the same phase are the same for coupled or non-coupled inductors. Only the scale of the current difference is changed.
- Regular inductors are easily found in the market and were already available in the laboratory.
- When using regular inductors, the differences in the currents are higher and thus they can be more easily measured.

V.3.1 Connected Neutral Point

For this first set of results, the two three-phase inductive-resistive loads were connected together, resulting in an equivalent single three-phase load. In order to show an image of the flux in the virtual ICT that could be inserted between two commutation cells, the currents of each commutation cell were measured by using a LECROY current probe CP030. The current difference was directly calculated in the oscilloscope LECROY Wavesurfer 424. The reference signal of phase U after the zero sequence injection along with the CMO are also measured by the use of a digital-to-analog converter. All 5 signals were acquired and saved in the hard disk of the oscilloscope in a DAT file type. The results presented in this chapter are plotted using the module SIMVIEW from software PSIM.

The acquisition was performed for each of the 12 PWM methods and for different modulation indexes (Mi = 0.1, 0.2, 0.3,…, 1.1). PD technique was used along with the compensation of flux step and closed loop for current regulation.

With the purpose of validating the experimental results, we show in Figure V.49 the acquired current differences of phase U. These were obtained by using DC bus voltage equal to approximately 150V, modulation index equal to 0.7, switching frequency equal to 4kHz, fundamental frequency 50Hz and a 5kW load.



a) DPWMMIN *b) DPWMMAX*

c) DPWM0 *d) DPWM1*

e) DPWM2 *f) DPWM3*

g) SPWM *h) THIPWM1/6*

i) SVPWM *j) PWMBCNP*

k) SV3PWM (3-level SVPWM) *l) PWMBC*

Figure V.49: Measured current differences for different methods.

If we compare the experimental waveforms of Figure V.49 with the simulation results of Figure V.25 we note that they match very well and that there is only a difference of scale which is due to the fact that they have the same modulation index but different inductances, voltages and frequencies. Also observe that PWMBCNP has the lowest maximum ripple of the current difference since it is theoretically the optimal PWM method to minimize the maximum flux ripple.

All the experimental results are presented in a concise form in Figure V.50, where the maximum current difference value is plotted for all methods and modulation indexes. Comparing this figure with Figure V.24 issued from calculation, we see that they are very similar. Furthermore it is clear that the discrete PWM methods generate less maximum flux ripple for low modulation indexes and PWMBCNP is the optimal for higher modulation indexes. Note that SV3PWM is also an interesting method for modulation indexes from 0.45 until 0.6.

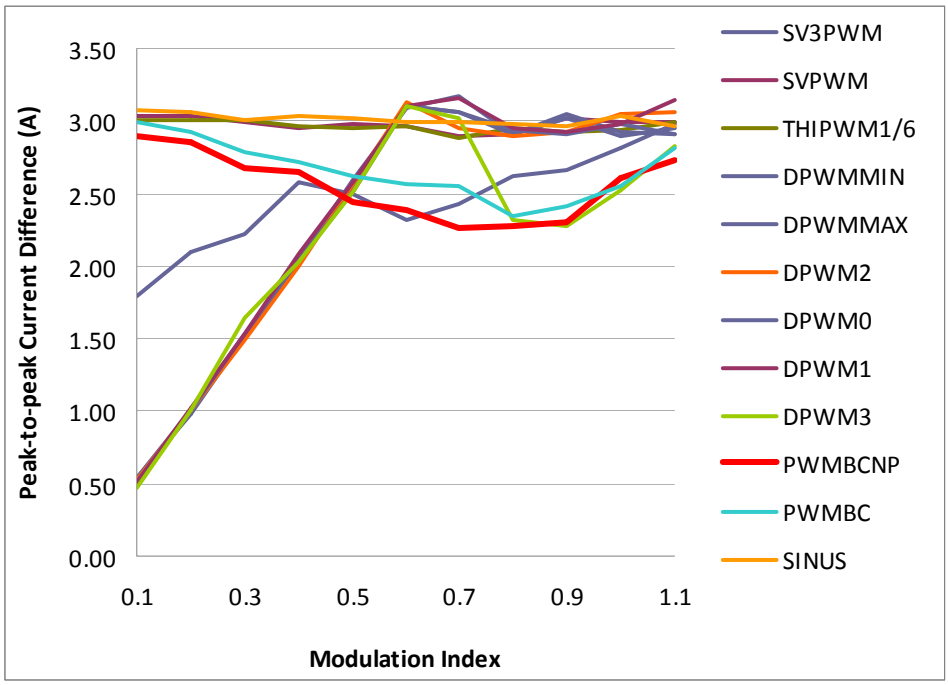
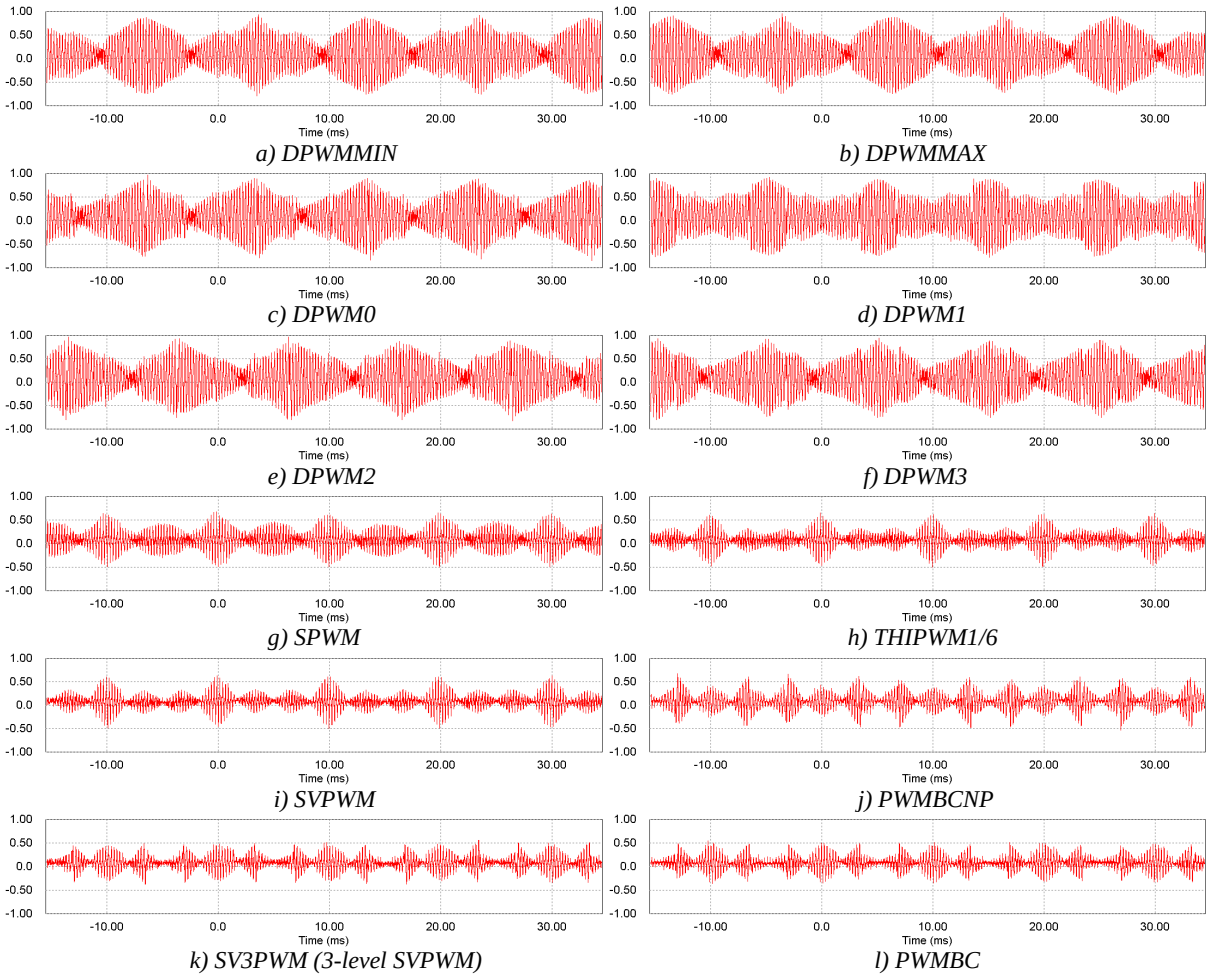


Figure V.50: Comparison of PWM methods: maximum peak-to-peak current difference obtained by experimental results.

V.3.2 Separate Neutral Point

As seen in the last sub-chapter, when the neutral points are not connected, the flux ripples are different if we use POD or PD techniques. Here we will show the results when using the POD technique. The same tools and instruments used in the last series of measurements were used in this case. Also the same signals were measured, acquired and saved in the hard disk of the oscilloscope. The acquisition was performed for each of the 12 PWM methods and for different modulation indexes (Mi = 0.1, 0.2, 0.3, … , 1.1).

In Figure V.51 the acquired current differences of phase U are shown. These were obtained by using the same conditions as before, i.e. DC bus voltage equal to approximately 150V, modulation index equal to 0.7, switching frequency equal to 4kHz, fundamental frequency 50Hz and a 4kW sub-load.



a) DPWMMIN *b) DPWMMAX*

c) DPWM0 *d) DPWM1*

e) DPWM2 *f) DPWM3*

g) SPWM *h) THIPWM1/6*

i) SVPWM *j) PWMBCNP*

k) SV3PWM (3-level SVPWM) *l) PWMBC*

Figure V.51: Measured current differences for different PWM methods.

Note that experimental results match very well the simulation results shown in Figure V.41 and also that the 3-level Space Vector PWM (SV3PWM) has similar waveform when compared to PWMBC. This is due to the similarity of their CMOs at some modulation indexes.

All the results are presented in a concise form in Figure V.52, where the maximum current difference value is plotted for all methods and modulation indexes. Comparing this figure with Figure V.40 issued from calculation, we see that they are very similar. Furthermore it is clear that the discrete PWM methods generate higher maximum flux ripple and that PWMBC is the optimal for all modulation indexes although it generates almost the same maximum flux ripple than SV3PWM, PWMBCNP and DPWM3 for some modulation indexes.

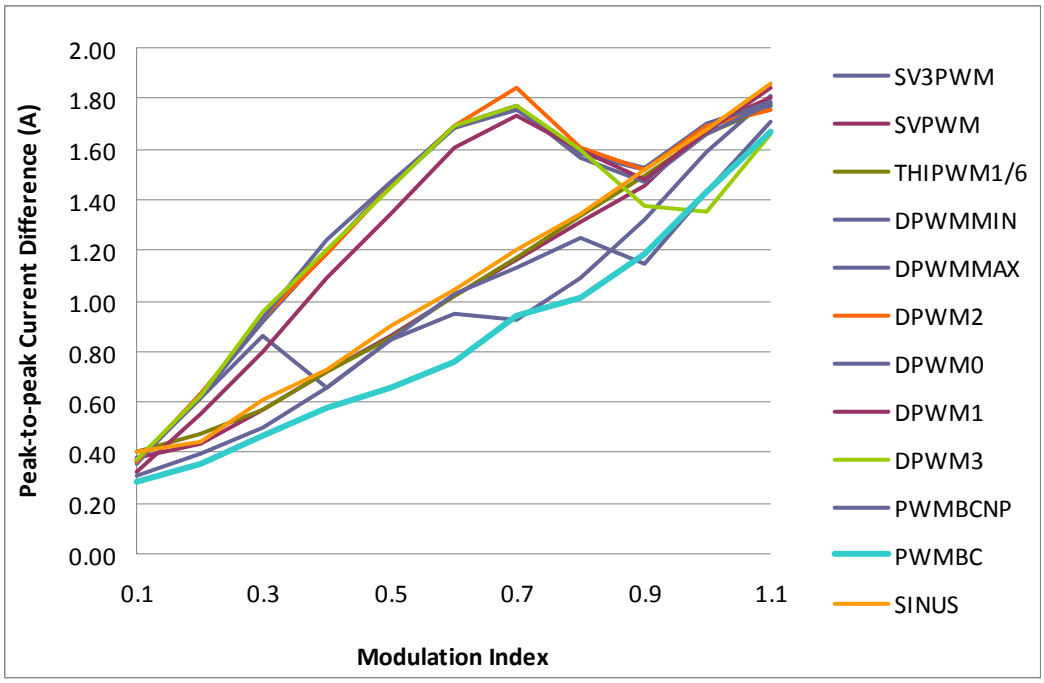


Figure V.52: Comparison of PWM methods: maximum peak-to-peak current difference obtained by experimental results.

V.4 Conclusions

In this chapter the use of ICTs in three-phase AC systems was analyzed. PWM techniques concerning carrier disposition and zero order signal injection for three-phase parallel converters were reviewed. The influence of each technique and method in the flux flowing through the ICT was explained for two different topologies: when two (or more) identical sub-loads have no electrical connection and when these sub-loads have their neutral points connected, which is the same as the case where there is only one load regarding the flux flowing through the ICT core.

For each topology and each carrier disposition technique, the optimal common mode offset added to the reference was created by means of an offset sweep and calculation of the ICT flux. These optimal CMO were created to minimize the maximum flux ripple in the ICT, which is the main magnitude which influences the core design.

As seen in Chapter III, the maximum flux ripple is not the only quantity which alters the core size. Actually the overall flux ripple is also important since it generates core losses which have a direct influence on the core size. As a result, comparisons with other methods were proposed by analyzing the temporal waveform of the flux during a fundamental period and also by calculating the maximum flux ripple.

For the case where the neutral points are connected, POD and PD techniques generate the same flux ripple, if the problem of "flux steps" is solved for the PD case. The PWMBCNP method is the one that generates the lowest maximum ripple flux and also the lowest overall ripple. For lower modulation indexes, discrete PWM methods are also interesting.

In general, separate neutral point topologies generate lower flux in the ICT than connected neutral point topologies. When neutral points are disconnected, POD and PD techniques generate different flux ripple. If PD technique is used, usually discrete PWM methods create lower flux ripple and the optimal one was found to be DPWM3. When POD

technique is used, continuous PWM methods give lower flux ripple and the optimal one was created and called PWMBC. In this topology, POD technique creates lower flux ripple than PD technique.

Most of the analysis developed in this chapter was confirmed by experimental results. Using two three-phase inverters connected to two three-phase resistive loads through inductors, the connected and disconnected neutral point cases could be verified. Experimental results match very well results issued from calculation and from simulation using PSIM.

As a result of all the discussion in this section, the optimal CMO concerning the minimization of the ICT design might not be those presented before; core losses are also a crucial design factor, and other CMO optimizing the losses or a trade-off between losses and peak flux could be investigated.

Conclusions and Future Work

The work I developed in the research group at LAPLACE has started by helping the former PhD student Valentin Costan to build a 12-cells monolithic ICT to be tested in the laboratory. At this time, the problem at stake was to understand how core losses were generated, how they were distributed in these magnetic components and how these types of losses could be reduced and the ICT efficiency be improved.

The idea of my doctoral research was to concentrate efforts on the other type of losses which are important in an ICT design: copper losses. Obviously the heart of the investigated losses was copper losses due to high frequency currents flowing through the winding of the ICTs. Low frequency copper loss calculation was considered a simple problem and no attention was given to it. However a study developed for MGEUPS revealed that low frequency copper losses may be underestimated when only the DC resistance of the winding is considered. And this is a problematic issue since low frequency copper losses are usually the most important losses of a transformer or inductor. The problem observed is the increase of winding resistance even at lower frequencies. When a foil winding is used with the purpose of reducing high frequency copper losses, the foil is generally very thin but very large. Skin effect may appear in the greater dimension of the foil and we noticed an underestimation of losses of about 13% for an inductor having 14 turns. This phenomenon is observed in foil conductors inserted in 2D/3D magnetic fields, which is the case of windings in inductors and in the part outside the core window of transformers.

A great effort was put in understanding high frequency phenomena related to copper losses. In particular, skin and proximity effects were deeply investigated making use of a simple but powerful software: Finite Element Method Magnetics (FEMM). Another software based on finite element method calculation was also used (it is called COMSOL), but the complexity of utilization and especially the calculation time turned out to be major drawbacks. COMSOL allows simulation of 3D structures which is a priori more accurate than 2D simulation. However, given that 3D simulation requires a very high number of elements, most of the simulations at higher frequencies turned out to be impractical in terms of time and memory requirements. FEMM software revealed to be a very simple and reliable tool to predict copper losses and also leakage inductances of ICTs.

Since FEMM only simulates 2D structures having sinusoidal currents, some methods had to be developed so we could accurately predict important values related to the ICT design. The first is related to the 2D nature of the simulations. Since ICTs have 3D structures, a simple approach was adopted to calculate copper losses and leakage inductance. This approach is based on the simulation of a cross-section of the ICT. Leakage inductance and AC resistance per unit length are found for the part of the winding inside and also for the part outside the core window. Then these values are multiplied by the corresponding total length of the conductors (either inside or outside the core window). Although neglecting some 3D effects, this method gave very good results.

Another method was developed to allow using FEMM even for non-sinusoidal currents. It is found in the literature that non-sinusoidal currents may be decomposed in Fourier series and the total copper losses calculated by the sum of losses related to each

harmonic. We applied this idea in the calculation of high frequency copper losses in ICTs. First we defined an equivalent AC/DC resistance ratio. This is the value which multiplied by the DC resistance and half the square value of the peak of the non-sinusoidal current, results in high frequency losses. This ratio is specific for one fundamental frequency, geometry and current waveform. The specificity of the ICT high frequency copper loss calculation lies in the fact that currents flowing in the windings may have differential and common modes. The behavior of the AC resistance is very different depending if common or differential mode current flows through the windings. Calculation of total copper losses is complicated since it is the combination of the low and high frequency currents, having a common and differential mode, for the part inside and outside the core window, calculated for each layer.

Although useful for predicting the AC resistance and leakage inductance related to 2D (and even 3D) magnetic fields, FEMM is not necessary when we deal with one-dimensional fields. And this is the case of the space inside the core window of a transformer when its height is mostly filled with conductors. High frequency resistance and leakage inductance may be analytically calculated by using different formulas. The most widely used is the one developed by Dowell in 1966. His equations were largely used in this dissertation, especially to calculate a key value: the Limit Frequency. This frequency is used to tell which is the best configuration of conductors inside a given core window, for a fixed number of turns. It was shown that only two configurations of conductors minimize copper losses in a core window with fixed dimensions: 1 – having one layer with N_t turns; 2 – having N_t layers with one turn in each. We have created tables with constant values which relate the winding area width, the current waveform, the fundamental frequency of this current and the number of turns. With a simple equation, the transformer designer may choose which of the two configurations mentioned above generates lower high frequency copper losses.

Even though copper losses in ICTs were the center of the research, we also investigated questions related to the design of these components. Combining the knowledge developed for estimating core and copper losses with simple thermal models was the approach adopted to minimize a given characteristic of the ICTs. A widely used optimization function was used to perform a single-objective optimization with several variables and constraints. Optimization algorithms were developed for some structures of 2, 4, 6, 8…. cells. Even if FEMM simulation takes much less time than 3D FEM simulation, it is sometimes impractical to insert some simulations inside the optimization loop. A solution to speed up the process is obtained by local interpolation of an N-dimensional matrix containing the pre-simulated values of the AC/DC resistance ratios and leakage inductances.

We have also studied how ICTs can be used in three-phase systems and showed that, based on the series/parallel multilevel converter duality, PWM carrier disposition techniques and zero sequence injection methods also apply to parallel interleaved converters. ICTs were considered in two different configurations: single three-phase load and double three-phase load with no neutral point connection. Analysis was made considering the flux inside the ICT core. Comparison between POD and PD strategies showed that even though PD reduces the harmonic content of the output current, it increases the ICT flux. In addition, this strategy creates “flux steps” in the core when the carrier compared with the reference is changed. These are major drawbacks to the PD strategy since bulkier ICTs must be designed to be used with this strategy.

Concerning the injection of zero sequence signals, two optimal signals were developed to minimize the ICT flux. A first PWM method named PWMBC was developed for POD strategy to be used with standard three-phase load or double star three-phase load with

connected neutral points. A second method, called PWMBCNP, was developed for POD strategy and double star three-phase load with no connection between neutral points.

All the most important PWM methods were compared to the developed methods and a reduction of roughly 20% in the maximum flux ripple was observed, both on simulation and experimentally. It is interesting to note that the approach developed to find the optimal zero sequence signals related to the ICT flux reduction could be used to find the optimal zero sequence signal related to any criteria. If the criteria is to minimize the total copper losses, or the total losses of the three-phase system, for example, different zero sequence signals will be found for each criterion.

FUTURE WORK

The ICT optimization strategy shown in this work relies on the estimation of three main quantities: core losses, copper losses and ICT temperature. We consider that studies carried out in our research group have led to accurate estimation of the two first quantities, for different ICT and converter topologies. However the thermal model is the weakest point in the optimization process. The one used to calculate the ICT temperature rise is too simple and does not precisely represent what happens with the real component. First of all, it considers a unique temperature in the whole component, which is far from reality. Then, it does not take into account forced convection. That is why more precise models [102] could be used as reference to direct the paths to where we should concentrate efforts. Actually studies about this subject have recently started to be carried out in the research group by Didier Flumian, who measures core losses by using calorimetric methods.

A more direct continuation of this work is related to the Set of Results. Some of them were already created during the PhD but they took a relatively long time to be completed since they rely on a great number of FEM simulations. Different structures should be considered such as those using toroidal cores or having an extra leg to guide the leakage flux. The structure used in the multicell ICT-coupled Flyback converter [7] has four windings in each core window. These types of multi-winding core windows are more complicate to analyze and simulate but they may also be considered.

We have compared the design of ICTs and uncoupled inductors for the same applications and we concluded that ICTs are lighter and smaller. However it would be interesting to include another “component” in this comparison: a hybrid solution composed by an ICT having very small leakage inductance in series with one or more uncoupled inductors.

One point which was not studied in this thesis is the problem related to fault tolerant converters. If a fault is detected in a commutation cell of a parallel interleaved converter, usually the faulty leg is isolated and the converter continues to work in a degraded mode. If ICTs are used to couple commutation cells, specific strategies must be developed to prevent core saturation due to the faulty leg isolation. Short-circuiting the winding connected to the faulty leg may be a solution but many other aspects must be considered.

We specifically studied the optimization of ICTs used in some converters. However the ICT resulting from the optimization algorithm does not guarantee the best performance or weight reduction of the whole system composed by the converters, ICTs, loads and eventually input and output filters. Algorithms developed during this thesis may be used in a global optimization process taking into account all the components of the whole system. Reasoning the same way, the approach used to find the optimal Common Mode Offsets to reduce the flux in ICTs inserted in three-phase systems could be inserted in a global optimization process which would find the best CMO optimizing the criteria chosen for the whole system.

The way optimization was conceived here, all relevant geometrical parameters of a magnetic core were considered as variables. Thus the resulting geometries usually did not correspond to existing commercial cores. Depending on the application, manufacturers may realize a large-scale production of a certain core resulting of an optimization process. In fact, we could also think about changing other core parameters into variables if they can influence the optimization results. For example, we could consider having the permeability as a variable. Probably the optimization of an ICT would always find the highest possible permeability for the optimal ICT. However if this approach is used in an inductor optimization, the result would not be the same. A more interesting approach might be to identify general laws describing the variation of the loss model vs the permeability.

Until now we have investigated several topologies and methods using ICTs. We have also studied phenomena related to the ICT operation and design and also how to optimize it for several cases. We believe we have acquired enough expertise about these types of components to focus on their use for dedicated applications and on the technology transfer to the industry. Through the collaboration between our research group and technology companies (CIRTEM, MGEUPS, LIEBHERR…), we see a large field of potential applications. One of them is the use of ICTs in massive series-parallel combination of individual cells related to new technologies such as supercapacitors, fuel cells, photovoltaic panels and batteries (especially Li-Ion).

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Appendix

Appendix A – MATLAB script for finding the optimal CMO

This function calculates the optimal CMO which reduces the flux in 3-cell ICTs inserted in a triple three-phase inverter connected to a three-phase load (Figure V.20a): ***FluxCalcEqualOffsetCNP3ph.m***

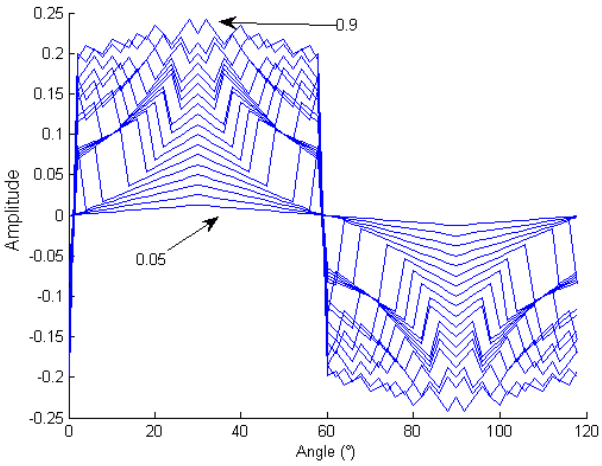
```
% Function FluxCalcEqualOffsetCNP3ph.m

% Bernardo Cougo
% Date: 29/01/10
%
% Find the best Common Mode Offsets for three-phase system containing a
% 3-cell ICT per phase

clear all

% Definitions
Nangle = 120; % Number of angles to be calculated
Nptri = 900; % Number of points of the triangular carrier
Noffset = 200; % Number of offsets used for calculation for each angle
Angle = 0:(2*pi/3)/Nangle:((2*pi/3)*(1-1/Nangle)); % Angle of the reference
in phase U of the first motor
AngleD = 0:(120)/Nangle:((120)*(1-1/Nangle)); % Angle in degrees of the
reference in phase U of the first motor
ModDep = 0.1:0.1:0.9; % Modulation Depth

% Carriers
TriangTop = 0:(1/(Nptri/2)):(1-(1/(Nptri/2)));
TriangPOD1 = circshift(TriangTop*2-1,[0 3*length(TriangTopPOD)/4]);
TriangPOD2 = circshift(TriangTop*2-1,[0 1*length(TriangTopPOD)/12]);%
Different from the 2phase case
TriangPOD3 = circshift(TriangTop*2-1,[0 5*length(TriangTopPOD)/12]);% Not
actually necessary


% Sinusoidal references
SinU = ModDep'*sin(Angle-0);
SinV = ModDep'*sin(Angle-2*pi/3);
SinW = ModDep'*sin(Angle-4*pi/3);

OffsetD1=0;
OffsetD2=0;

% Main loop
```

```
for i=1:length(ModDep)
    for j=1:length(Angle)
        % Maximum and minimum offsets for a given angle
        AlphaMax = max([SinU(i,j) SinV(i,j) SinW(i,j)]);
        AlphaMin = min([SinU(i,j) SinV(i,j) SinW(i,j)]);
        MaxDistOffset = 2 - AlphaMax + AlphaMin;
        for k=1:Noffset+1
            OffsetD1 =-1-AlphaMin + ((k-1)/Noffset)*MaxDistOffset;
            OffsetD2 = OffsetD1;

            % Switched Voltages
            U1 = (SinU(i,j)+OffsetD1) > TriangPOD1;
            V1 = (SinV(i,j)+OffsetD1) > TriangPOD1;
            W1 = (SinW(i,j)+OffsetD1) > TriangPOD1;

            U2 = (SinU(i,j)+OffsetD2) > TriangPOD2;
            V2 = (SinV(i,j)+OffsetD2) > TriangPOD2;
            W2 = (SinW(i,j)+OffsetD2) > TriangPOD2;

            % ICT Voltages
            U1U2 = U1-U2;
            V1V2 = V1-V2;
            W1W2 = W1-W2;

            % ICT Currents
            FluxU(k,:) = cumsum(U1U2)-mean(cumsum(U1U2));
            FluxV(k,:) = cumsum(V1V2)-mean(cumsum(V1V2));
            FluxW(k,:) = cumsum(W1W2)-mean(cumsum(W1W2));
        end
        % Maximum ABS value of the flux
        MaxFluxU(i,j,:) = max(abs(FluxU(:,:)),[],2);
        MaxFluxV(i,j,:) = max(abs(FluxV(:,:)),[],2);
        MaxFluxW(i,j,:) = max(abs(FluxW(:,:)),[],2);
        % Maximum of the 3 phases
        MaxFlux(i,j,:) =
max([MaxFluxU(i,j,:);MaxFluxV(i,j,:);MaxFluxW(i,j,:)]);

        % Find the offset associated to the minimum value of the maximum
ABS flux
        [kValue, kIndex] = min(MaxFlux(i,j,:));
        MinofMaxFlux(i,j) = kValue;
        OffsetforMinFlux(i,j) = -1-AlphaMin + ((kIndex-
1)/Noffset)*MaxDistOffset;
    end
end
```

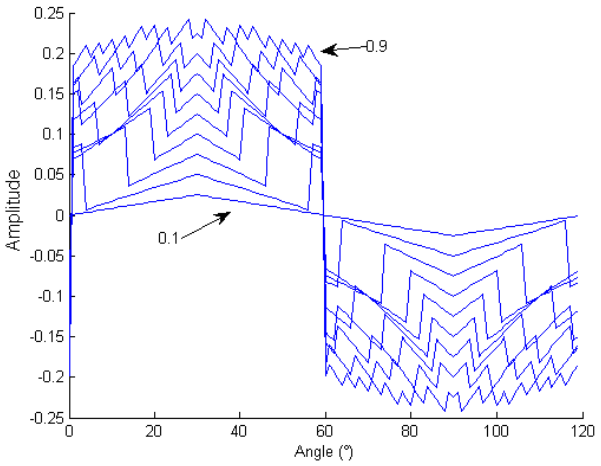
Appendix B – Number of points used to find the optimal CMO

As explained in Sub-Section V.2.1.1, the idea to find the optimal CMO is to add an offset to the 3 reference signals and calculate the maximum flux in the 3 ICTs for each angle in each modulation index. For this matter, we generate the triangular carriers having *Nptri* points. Then we create three nested loops where we sweep the modulation index, the angle and the common mode offset of the references. Inside these loops we compare the carriers with the reference plus the CMO, we find the switched voltages and then we integrate them to find the fluxes. Like this we can identify which offset gives the lowest maximum flux, for each angle and each modulation index. Gathering all offsets, we form the optimal CMO. The MATLAB script used to find these optimal CMOs was shown in Appendix A.

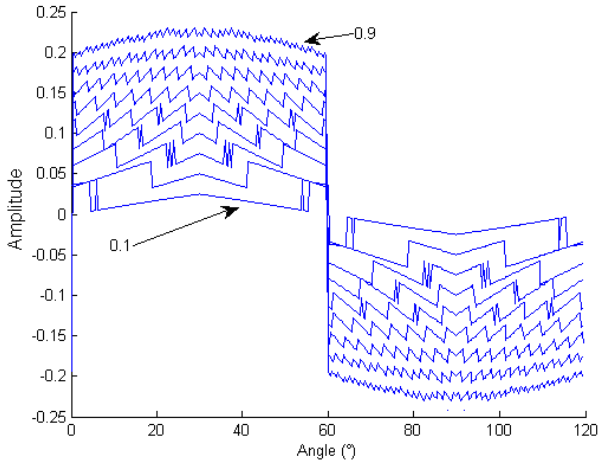
The number of angles (*Nangle*) and offsets (*Noffset*), as well as the number of points of the carriers (*Nptri*), influence very strongly the waveform of the optimal CMO. It can be seen on Figure B.1 that only with a great number of angles and offsets the optimal CMO looks like the real one described by equation (V-8).



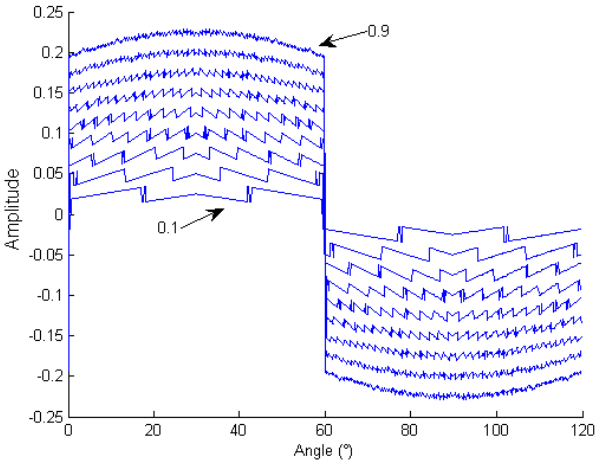
a) Nangle = 60; Noffset = 20



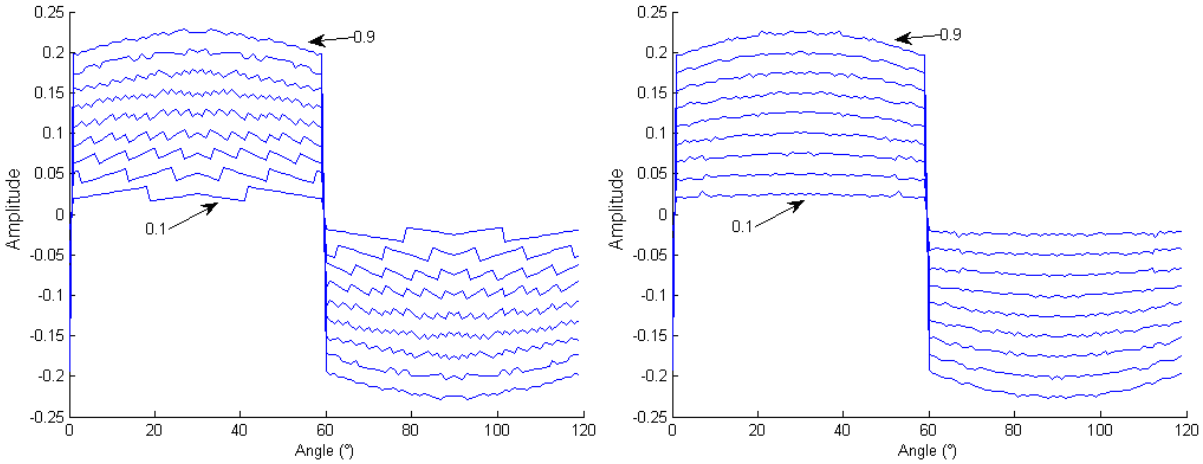
b) Nangle = 120; Noffset = 20



c) Nangle = 360; Noffset = 50



d) Nangle = 720; Noffset = 100



e) Nangle = 120; Noffset = 100 *f) Nangle = 120; Noffset = 1000*

Figure B.1: Optimal CMO for different number of angles and offsets.

Appendix C – Calculating AC resistances for different current modes

The aim of this part is to show that it is possible to calculate total copper losses in a 2-winding transformer or ICT by calculating the differential and common mode currents.

For a 2-cell ICT having currents I_1 and I_2, as shown in Figure C.1, we may define the differential mode current (I_{DM}) and the common mode current (I_{CM}) as:

$$I_{DM} = \frac{I_1 - I_2}{2} \quad \text{and} \quad I_{CM} = I_1 + I_2 \tag{C-1}$$

and, inversely:

$$I_1 = \frac{I_{CM}}{2} + I_{DM} \quad \text{and} \quad I_1 = \frac{I_{CM}}{2} - I_{DM} \tag{C-2}$$

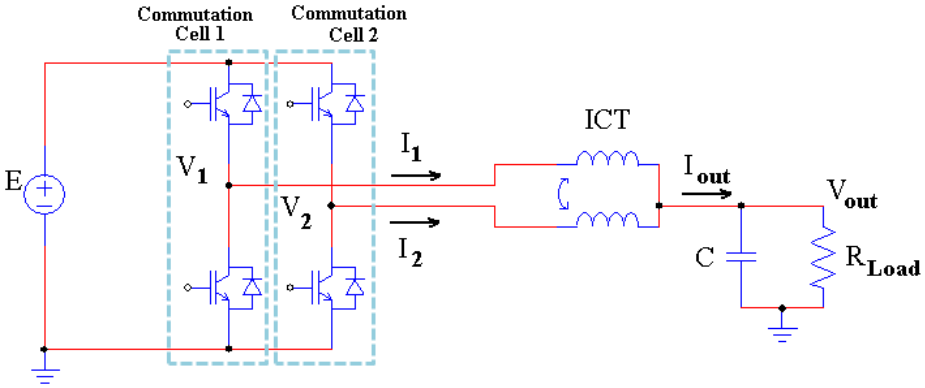


Figure C.1: Two-cell intercell transformer used in an interleaved converter.

First we will analyze total copper losses for DC or low frequency currents, where no skin and proximity effects are observed. Later high frequency currents will be considered.

DC or Low Frequency Currents

Total copper losses may be calculated as

$$P_{cuLF} = R_1 . I_1^{\,2} + R_2 . I_2^{\,2} \tag{C-3}$$

If we use C-2 in C-3, we have

$$P_{cuLF} = R_1 . (\frac{I_{CM}}{2} + I_{DM})^2 + R_2 . (\frac{I_{CM}}{2} - I_{DM})^2$$

$$P_{cuLF} = (R_1 + R_2) . I_{DM}^{\,2} + (R_1 + R_2) . I_{CM}^{\,2} / 4 + (R_1 - R_2) . (I_{CM} . I_{DM}) \tag{C-4}$$

By equation (C-4) we see that we may calculate low frequency copper losses using separate differential and common mode currents only if:

- these two modes have different frequencies or;
- the resistances of the two windings are identical, which is the case of an ICT.

High Frequency Currents

When high frequency currents flow through the ICT, there will be a different current distribution inside the conductors of both windings if there is a differential mode current. Currents I_1 and I_2 may be decomposed in common and differential modes and all the flux in the system (including conductors, core and air) will be the sum of the fluxes generated by the differential and the common mode currents, given that it is a linear system. Thus, the current distribution inside the conductors will be sum of the current distribution related to both fluxes. As a result, the total high frequency copper losses may be calculated as:

$$P_{cuHF} = R_1.I_1{}^2 + R_2.I_2{}^2 = R_1.\left(\int_s J_1 dA\right)^2 + R_2.\left(\int_s J_2 dA\right)^2 \tag{C-5}$$

Decomposing in both common and differential mode current densities:

$$P_{cuHF} = R_1.\left(\int_s \left(\frac{J_{CM}}{2} + J_{DM}\right) dA\right)^2 + R_2.\left(\int_s \left(\frac{J_{CM}}{2} - J_{DM}\right) dA\right)^2$$

$$P_{cuHF} = R_1.\left[\left(\int_s \frac{J_{CM}}{2} dA\right)^2 + \left(\int_s J_{DM}\, dA\right)^2 + 2.\left(\int_s \frac{J_{CM}}{2} dA\right).\left(\int_s J_{DM}\, dA\right)\right] + \tag{C-6}$$

$$+ R_2.\left[\left(\int_s \frac{J_{CM}}{2} dA\right)^2 + \left(\int_s J_{DM}\, dA\right)^2 - 2.\left(\int_s \frac{J_{CM}}{2} dA\right).\left(\int_s J_{DM}\, dA\right)\right]$$

Since the current distributions may be interpreted as different AC resistances, we may write:

$$R_{CM1} = R_1.\left(\int_s \frac{J_{CM}}{2} dA \Big/ I_{CM}\right)^2 \quad \text{and} \quad R_{CM2} = R_2.\left(\int_s \frac{J_{CM}}{2} dA \Big/ I_{CM}\right)^2$$

$$R_{DM1} = R_1.\left(\int_s J_{DM}\, dA \Big/ I_{DM}\right)^2 \quad \text{and} \quad R_{DM2} = R_2.\left(\int_s J_{DM}\, dA \Big/ I_{DM}\right)^2 \tag{C-7}$$

Substituting C-7 into C-6, we have:

$$P_{cuHF} = (R_{DM1} + R_{DM2}).I_{DM}{}^2 + (R_{CM1} + R_{CM2}).{I_{CM}}^2/4 +$$

$$+ (R_1 - R_2).\left[\left(\int_s J_{CM}\, dA\right).\left(\int_s J_{DM}\, dA\right)\right] \tag{C-8}$$

By equation (C-8) we see that we may calculate high frequency copper losses using separate differential and common mode currents only if:

- these two modes have different frequencies or;
- the resistances of the two windings are identical.

If the resistances of both windings are identical, which is generally the case in an ICT, equation (C-8) may be simplified:

$$P_{cuHF} = R_{DM} . I_{DM}^{\ 2} + R_{CM} . I_{CM}^{\ 2} / 4 \qquad \text{(C-9)}$$

Equations (C-4) and (C-9) are very similar and we note that the main difference when calculating low or high frequency copper losses is the fact that we have different resistances related to the differential and common mode when the frequency is high, which is not the case for lower frequencies.

A simple example will be given to illustrate this phenomenon. Let us consider a core window comprising two windings, each one having only one turn. In the winding on the left we have a sinusoidal current of amplitude 1A. In the winding on the right we have a sinusoidal current of amplitude 3A but flowing in opposite direction. Thus, we have:

$$I_{DM} = \frac{3-1}{2} = 1A \qquad \text{and} \qquad I_{CM} = 3+1 = 4A \qquad \text{(C-10)}$$

We have performed a 2D FEM simulation of this transformer with both currents I_1 and I_2, but also with the differential and common mode currents, at a frequency of 10kHz. The absolute values of the current density for all these cases are shown in Figure C.2. Below each winding we show its corresponding copper losses, calculated by the software. Note that total copper losses related to the currents I_1 and I_2 (shown on the transformer on the top) is equal to the sum of the copper losses related to the common and differential mode currents. These results validate equation (C-9).

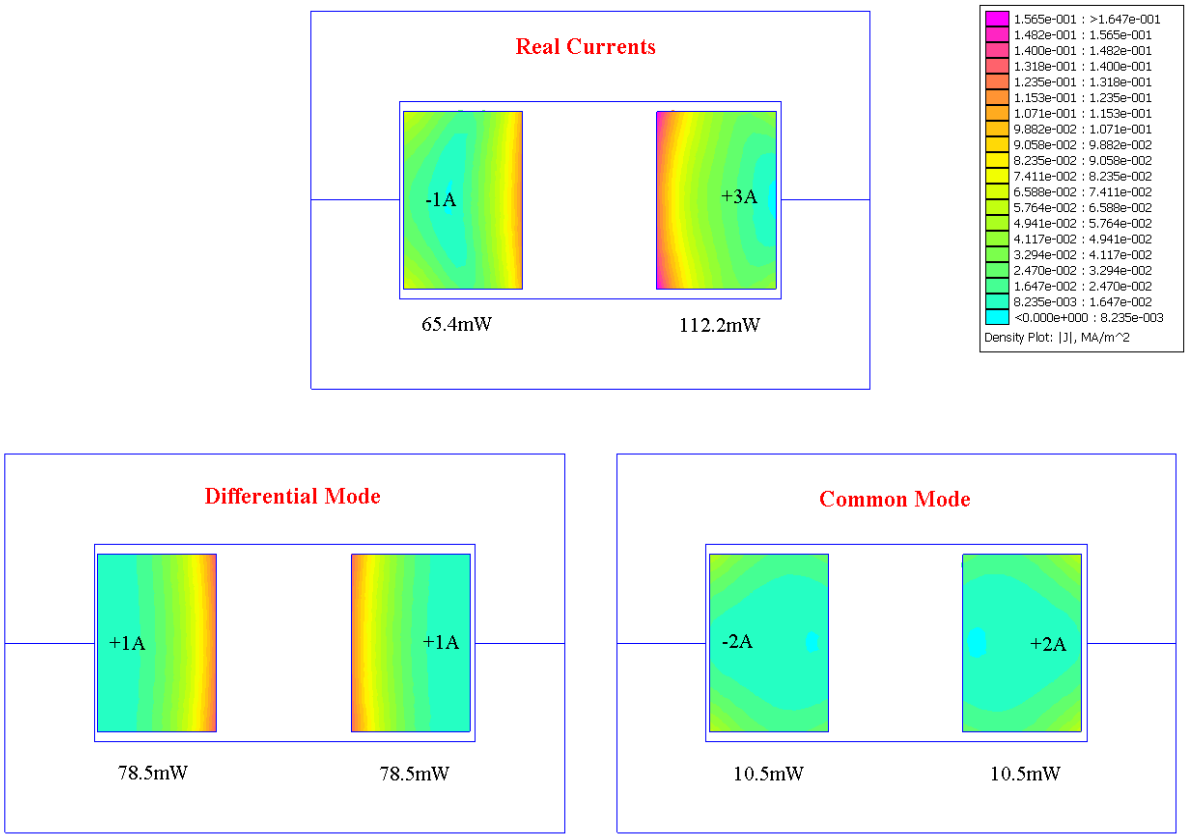


Figure C.2: Current distribution of transformer with real currents and also with corresponding differential and common mode currents.