Regulation of power amplifiers under VSWR conditions in CMOS 65nm for 60GHz applications

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Regulation of power amplifiers under VSWR conditions in CMOS 65nm for 60GHz WLAN applications

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General introduction

Since several tens of years and the invention of walkie-talkie (during World-War-II), radio-frequency transceivers are implemented in more and more portable applications. As soon as they become mobile, wireless communicating objects can be placed in a large variety of environments, with some being really inhospitable.

From the mobile phone left in a jeans' pocket with a bunch of keys, to the smartphone laying on a metal table, the mobile terminals are very often in obstructed environment far from the ideal free-space behavior.

Moreover, the size of the mobile terminals being more and more reduced, EM obstacles can be located in the very close vicinity of the antenna. It results in some interaction with the antenna which cannot be easily anticipated by EM simulations. The recent issue encountered by Apple on the 4th generation of its iPhone is a good illustration. The quality of the radio link can be drastically decreased simply by handling the phone in a given position.

This is a serious issue when considering the end user application. But the interaction between an antenna and its environment also generate a huge issue when considering the electrical effects at the transceiver level.

The wave propagation theory explains that an antenna is a transducer, which can convert an electrical signal into electro-magnetic waves. But the antenna also performs the reverse conversion, and hopefully; the electro-magnetic waves in the close vicinity of the antenna are converted into electrical signals. It results that when an incident wave, generated by an antenna, is reflected on an EM obstacle, a reflected wave is created, which is converted back into the device as an electrical wave. The incident and reflected waves add up into a standing wave, which creates dangerous overvoltage. The EM perturbing elements located in the close vicinity of an antenna can be detected electrically by an antenna impedance mismatch.

To overcome this issue, RF terminals have to integrate a feedback loop, which detects abnormal situation and protects the internal elements or optimize the performance of the terminals. A lot of academic and industrial work has been done so far on power regulated PAs in the frequency range below 10GHz, most of them implying analog regulation loops.

The goal of this thesis is to propose detection and power regulation solutions for millimeter wave PAs, and more particularly operating in the WLAN 60GHz band.

The first chapter presents the context of the study. After having introduced the IEEE 802.15.3c specifications, the current context on millimeter-wave transmitters is presented. The antenna impedance variation with environmental conditions is then detailed through a theoretical approach and through VSWR measurements performed at 60GHz. This chapter ends up with an overview of the architecture to be implemented and the associated system specifications.

The second chapter introduces the power detection circuit, which is able to work as antenna impedance mismatch sensor. This circuit uses a capacitive coupler and a power detector which both are highly detailed in this chapter. This chapter also presents the first circuit implementation of this thesis and the measurement results.

The third chapter presents a novel architecture of Logarithmic Analog-to-Digital Converter. This architecture is used to volt-linearize and digitize the signal coming from the power detection circuit. The system can then use the antenna impedance mismatch information in a digital feedback loop.

The fourth chapter introduces the novel concept of power detection, power regulation and power protection loops proposed in this thesis for mmW PAs. System study aspects are presented and finally completed by measurement results.

Finally, the fifth chapter introduces an alternative project, which uses the system architecture developed in this thesis to test the analog / mmW / digital co-simulation capabilities of Advanced Design System from Agilent Technologies.

The manuscript ends up with conclusions on the implemented solutions and perspectives for future research.

Chapter I. Context of the study

Chapter introduction

This first chapter presents the general context of this study.

The WirelessHD specification is first investigated. The targeted applications of this high data rate short range standard are mainly for HDMI cable replacement. High data rates, up to 3Gbps, can be obtained by increasing the bandwidth. WirelessHD standard uses the 7GHz wide frequency band between 57 and 64GHz.

However, millimeter-wave (mmW) frequencies are quite difficult to reach with low-cost technologies such as CMOS. The transmitters and power amplifiers working in the mmW frequency band are then presented. CMOS technology is particularly investigated as it is the most appropriate technology to address the rising mass-market of the WirelessHD specification (low-cost, high integration capabilities…).

One remaining limitation of mmW CMOS PAs is the reliability. Reliability issue can notably result from impedance mismatch situations between the PA and the Antenna. Perturbing elements located in the close vicinity of the antenna actually generates such impedance mismatch, which induces standing waves between the PA and the antenna. Those standing waves can damage or seriously degrades the performance of the power amplifier. The creation of standing waves and their effects on the power amplifier are hence investigated in this chapter.

This chapter ends up with a proposition of regulated PA architecture, which could overcome the reliability limitation of CMOS PAs. Using several integrated power detectors between the PA and the antenna could actually detect an impedance mismatch situation. The information could then be threated by a digital regulation loop, which could acts on the gain of the power amplifier.

Chapter outline

I.1. Building a WLAN-WPAN system at 60GHz

This section starts with a brief introduction and a small overview of the applications targeted by the emerging WLAN-WPAN systems at 60GHz. The new IEEE 802.15.3c and Wireless-HD standards have hence been specified (or are still on-going) by competent organizations, working at millimeter-wave frequencies. The advantages of working at millimeter-wave frequencies are then described before presenting some characteristics of those two new standards.

I.1.1. Introduction and targeted applications

Since the invention of the bipolar transistor (Nov. 17 1947) by John Bardeen, Walter Brattain and William Shockley [**1**], consumer usage has been profoundly changed. This results in a considerable growth of the number of electronics devices used in every home and more recently by every individual person. From radio broadcasting, television, High-Fidelity (Hi-Fi) equipment in the 1960s to computers in the 1990s, mobile phone at the end of the 1990s, Internet revolution in 2000, and since 2000, Mp3 players, GPS, tablet-PC… the new systems are adopted faster and faster by people at large letting manufacturers innovate permanently in order to satisfy the needs of their consumers.

Moreover, in all consumer electronics fields, the quality has increased considerably such as in broadcasting television systems [**1**]. At its invention just before World War II (WWII), broadcasting was in black and white and the screen resolution was very low (less than 405 lines). Those experimental systems have been standardized after WWII with 625 lines and 25 frames per second in the majority of countries in the world and with 819 lines in France (standardized by the Mitterand decree in November 1948). The color broadcast has been introduced in North America by the second version of the standard NTSC (National Television System Committee) adopted in 1953; there were 525 lines and 30 frames/s at this time. In France, the resolution was lowered to 625 lines when adding the color by adopting the standard SECAM IIIB in June 1967. At the end of the 20^{th} century, the television became digital: United States and Canada adopted the standard developed by the Advanced Television Systems Committee (ATSC) and the rest of the world adopted the Digital Video Broadcast - Terrestrial (DVB-T). Nowadays the television becomes High Definition with a screen resolution up to 1920x1080pixels. Although every citizen is not equipped in HDTV yet, manufacturers are already interested by higher definition video standards such as WQXGA which displays images of 2560x1600pixels. Furthermore, each pixel is coded by a higher number of bits in order to increase the color depths. The refreshment frequency is also increased for video fluidity.

By increasing the quality of our video display equipment, we have also increased the capacity of our storing devices such as Blue-Ray Digital Versatile Disks (Blue-Ray-DVD) in multimedia equipment and hard disks in the computing field. However, the link quality between those equipment has to be increased in the same way in order to benefit of the better quality of each device. It is similar in computing field, a better processor will be useful only if its peripheral devices (Human Interface Devices, Flash memory, hard disk, video display…) could emphasize it with a sufficient quality and if data links could manage data flows fast enough. And the quality of links is critical in every field of consumer electronics. Moreover, consumers want their devices to communicate with each other: the mobile phone should be able to connect the laptop to Internet (i.e. to the World…), the TV screen should be able to display images from the camera, the video camera, the computer, the Blue-Ray DVD drive… and to connect the 5.1 (or 7.1, or 9.2 …) sound system, the ADSL box…

Researchers and industrials from IEEE task group 802.15.3c target the definition of a new wireless communication standard that could provide very high data rates (up to 3Gb/s) while insuring the compatibility between many different systems. Applications mainly target high speed data transfer and High Definition (HD) video streaming (Audio & Video transfer) [**2**] [**3**].

File transfer occurs in both office and home environments but it can be divided in 2 classes: low and high data rate. The lower class corresponds to local small file transfer like printing or small document transfer, and light internet access (email, web, chat). The higher class corresponds to local file transfer for bulky music and video like from photo/video camera, photo/video cell phone or mp3

player to computer, and Internet bulky music and video downloading (from legal downloading sites, Video On Demand). The targeted range is between 1 and 10m.

HD video streaming occurs in conference environment when one or several laptop (-s) want to display a presentation on TV or video-projector. In home environment, video streaming stands for displaying on HDTV or projector uncompressed video coming from fixed devices (power-line operated devices) like Blue-Ray DVD player or game console and from mobile devices (battery operated devices) like photo/video camera, multimedia mobile player… The targeted range is between 0.5 and 3m.

More concretely, Figure I-1 illustrates the targeted applications. The first one concerns cable replacement and can be applied to High-Definition-Multimedia-Interface (HDMI) or Serial-Advanced-Technology-Attachment (SATA). Then Sync & Go applications permit to quickly synchronize two mobile devices together or one mobile device with a computer. A Giga-Bit-Per-Second (Gbps) Wireless link can also be used as a high data rate Wireless-Local-Area-Network (WLAN) and works similarly to WiFi. Finally, some Ad-Hoc networks can be implemented using this wireless link and connect together several computers or connect one computer to its peripheral devices (screen, external hard-drive, printer…), or one audio-video receiver to the screen or projector and to the speakers.

Figure I-1 Targeted applications of the new IEEE 802.15.3c standard

Other applications are targeted too: multimedia kiosk and Short Range High Speed Backhaul. In Multimedia kiosk application, several consumers could download audio and video files from a public kiosk (range less than 5m) in urban environment on their cell phone, mp3 player or other mobile device. Short Range High Speed Backhaul stands for connecting 2 distant points that could be in a corridor (20-30m long) or outdoor between 2 buildings (200-300m distant) where it seems difficult to establish a wired connection. The link should be able to provide Gigabit Ethernet on a fixed installation with highly directive antennas (high gain). It can be notice that wireless Backhaul can also use classical Mobile-phone and WiFi standards (see Annex A) or some other standards working between 71 to 76GHz, 81 to 86GHz or 92 to 95GHz. However, some solutions have already been implemented at 60GHz [**4**].

Potential commercial implementations are very large, from mobile devices such as mobile phone, mp3 player, photo/video camera, laptop… to fixed devices (power-line operated) such as HD-TV, DVD player, video projector, computer…

Those applications are usually split between three categories of networks. The Wireless Personal Area Network (WPAN) is a short range standard, less than 10m, with quite low data rates. The Wireless Local Area Network (WLAN) is a moderate range standard, between 10m and some hundreds of meters, with a good data rate like 54Mb/s for WiFi. Finally, Fixed Local Area Network Extension (FLANE) in the range of 10 to 800m with Light-of-Sight (LOS) conditions between the emitter and the receptor corresponds to Backhaul in extension of a private LAN.

Figure I-2 illustrates the different categories of networks with respect to the distance range of the communications. The FLANE is similar to a Wireless Metropolitan Area Network (WMAN). The Wireless Wide Area Network (WWAN) covers a larger area than the WMAN, with more than 10km range communications. However, the new Multi Gigabit Wireless Standard (MGWS) does not target to establish so long distance wireless link. The targeted MGWS is called WPAN-WLAN system as it should provide the data rate of WLAN in the range of WPAN.

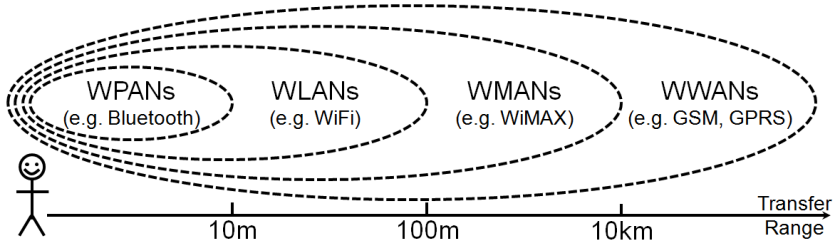


Figure I-2 WPAN, WLAN, WMAN, and WWAN definition with respect to the transfer range

Figure I-3 presents a comparison between the different High Data Rate (HDR) wireless standards. The IEEE 802.15.3c and Wireless-HD (WiHD, see section I.1.3 for more details) are compared to some proprietary systems (Amimon and Celeno, both working in the 5GHz unlicensed band) and the 802.11 systems (WiFi a, b, g, n and its evolutions ac working at 5GHz and ad working at 60GHz) with respect to the communication range and the data rate. This figure also makes the link between the HDR standards and the different applications presented above. Some comparison elements with the other wired and wireless standards can also be found in Annex A.

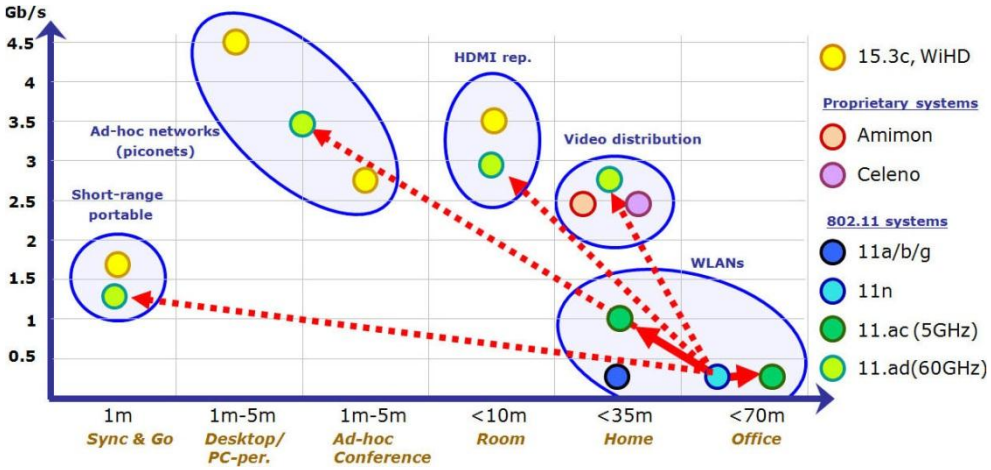


Figure I-3 High Data Rate (HDR) standards with respect to the communication range and the data rate

I.1.2. Millimeter-Wave frequencies

i. A worldwide unlicensed frequency band

Millimeter-wave frequencies present some advantages for previously detailed applications. First of all, this frequency band is unlicensed in many countries, which naturally makes it a good candidate for a new communication standard. In the United-States [**5**] as in Canada [**6**], the frequency band between 57 and 64GHz is actually free with only some constraints on the radiated power density at 3m (9µW/cm² mean and 16µW/cm² at peak level). In Korea [**7**], the same frequency band is free as well, but the power at the antenna connector should not exceed 10dBm (10mW). Australia [**8**] has the same power exigency of 10dBm at the antenna connector, but the allowed frequency bandwidth is reduced to 3.5GHz: from 59.4GHz to 62.9GHz. However Australian Communications and Media Authority (ACMA) is looking forward to go by the international specifications by fixing a departure [**9**] for indoor WPAN applications that allows the use of the frequency band from 57 to 66GHz with a maximum power of 13dBm at the antenna connector and an Equivalent Isotropically Radiated Power (EIRP) of 20W. The frequency band is also different in Japan [**10**] from 59 to 66GHz. The adjacent band from 54.25 to 59GHz cannot be used as it is already licensed in Japan. Japan regulates also the antenna gain that should be less than 47dBi. In Europe at last [**11**], although the actual available frequency band reaches from 59 to 62GHz, the European Telecommunications Standards Institute (ETSI) is looking forward the possibility to extend this unlicensed frequency band from 57 to 66GHz.

Figure I-4 shows graphically the worldwide availability of the 60GHz frequency bands discussed above.

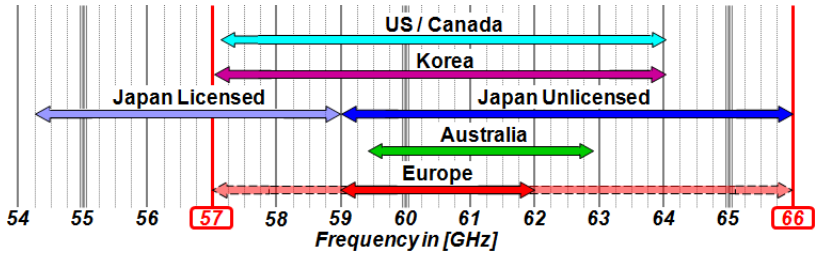


Figure I-4 Worldwide availability of a 60GHz frequency band

It follows that in most countries in the world there is a 7GHz wide frequency band from 57 to 64GHz that could be used for MGWS (highlighted in Figure I-4). This frequency band can then be divided in several channels (4 channels of 1.25GHz as an example) that every country could allow or not the use of one or another channel to conform to its own frequency band availability, as it is the case also for WiFi.

ii. A short range link

This available frequency band is located in the frequencies called millimetric as the associated wavelength is in the order of some millimeters (5mm at 60GHz). At those frequencies, waves are rapidly attenuated in the terrestrial atmosphere, given the O_2 presence. This is a major drawback for long range links (several kilometers) but a real advantage for short range applications (less than 10m). Waves at those frequencies being actually shortly attenuated, they do not propagate out of the room or the building, increasing considerably the security of the wireless systems. Furthermore, many similar networks can coexist on a restricted area as interferences between those different networks are highly reduced thanks to the high level of attenuation.

To estimate this attenuation, we simply use the Friis formula of the equation (I.1):

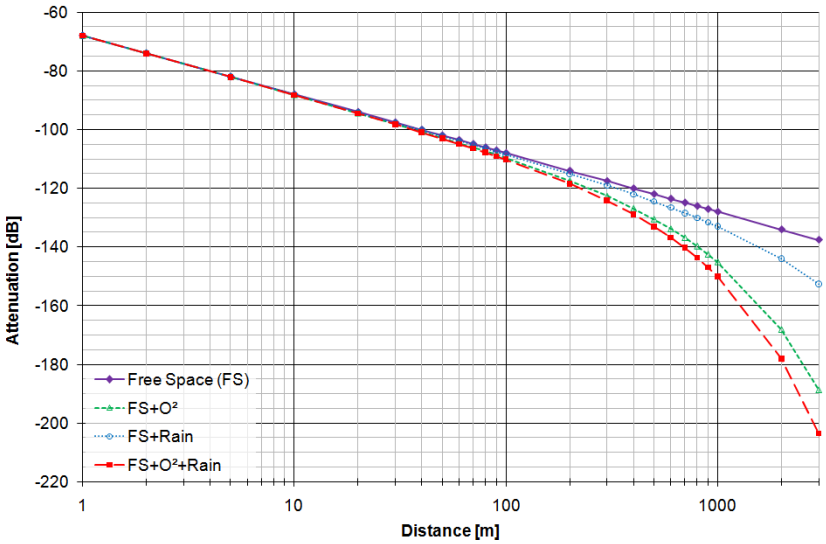
$$\frac{P_{RX}}{P_{TX}} = G_{ANT_{TX}}.G_{ANT_{RX}}.\left(\frac{\lambda}{4\pi.D_{TX-RX}}\right)^2 \qquad \text{(I.1)}$$

Where P_{RX} and P_{TX} represent the power at the reception and at the emission, $G_{ANT_{RX}}$ and $G_{ANT_{TX}}$ stand for the gains of reception and emission antennas, D_{TX-RX} is the distance between those two antennas and λ is the wavelength of the transmitted signal.

The lower the wavelength is – that means the higher the frequency is –, the higher is the attenuation. Thus, at 60GHz, the attenuation due to the free space wave propagation stands to 88dB for a 10m range and to 108dB for a 100m range. The signal is attenuated so rapidly that is becomes impossible to extract it frocm the noise. Even for short ranges, the receiver sensitivity will be a key parameter to obtain a sufficient Signal to Noise Ratio (SNR) to correctly detect the useful signal.

In addition to this high attenuation due to the wave propagation in free space, it should be noticed that this frequency band from 55 to 65GHz matches with a range where the oxygen absorption is high [**12**], in the order of 16dB/km. This is insignificant in comparison with the 88dB for 10m of free space propagation, but it should be taken into consideration for ranges of several hundred meters. In the same way, the rain could generate an additional attenuation from 5dB/km to several tens of dB/km depending on the rainfall strength.

The sum of all those attenuations, illustrated in Figure I-5, reinforces the idea that it is very difficult to establish long range links at millimeter-wave frequencies. On the other hand, the use of millimeter-wave frequencies for indoor and short range (less than 10m) applications is highly attractive for the security of networks as for the geographical density of frequency re-use.



FS: Free space propagation; O²: Oxygen attenuation; Rain: rain attenuation (-5dB/km when it rains 10mm/h)
Figure I-5 Attenuations of a 60GHz signal versus the distance between the emitter and the receiver

To compensate those attenuations for outdoor or middle range (from 10 to 100m) applications such as backhaul, the directivity of the antenna could be increased. By using a very directive 47dBi antenna (Japan specifications) both at the emission and the reception, a gain of 94dB could be added to the link budget as it is shown by the Friis Formula.

iii. Smart components

Finally, frequencies being high, corresponding wavelengths are relatively low: 5mm at 60GHz (in free space). Therefore propagation elements like quarter wave lines or antennas have a reasonable size (in the order of several millimeters) and, as a consequence are directly integrable on silicon. This easiness of integration allows a financial gain in the production stage but the low size of propagation elements generate also an additional cost in the design stage as electromagnetic effects of each interconnection have to be taken into account.

I.1.3. The IEEE 802.15.3c & WirelessHD standards

Task Group 3c (TG3c) was formed in March 2005 by the IEEE Standards Association to supply a millimeter-wave alternative PHY of the IEEE 802.15.3-2003 (see Annex A). It aims to write a WPAN standard that could provide data rates higher than one Gb/s. Although this Task Group is still working, a first draft of this new standard IEEE 802.15.3c with the main orientations is already available [**13**].

Before the publication of any IEEE specification, an industrial consortium, the WirelessHD Special Interest Group (SIG) was formed in 2006 including ten leading consumer electronics manufacturers [**14**]: Broadcom, Intel, LG Electronics, Panasonic, Philips Electronics, NEC, Samsung Electronics, SiBEAM, Sony and Toshiba. In January 2008, this SIG finalized the WirelessHD 1.0 standard [**15**], which aims to be a wireless HDMI specification, thus focusing on the audio and video applications. It allows transmission of uncompressed HD video and audio from a consumer equipment to a HD display through a very high speed wireless connection up to 4Gb/s. The core technology promotes a theoretical 25Gb/s data rate, which allows scalability to future HD Audio/Video formats such as the integration of the 3rd dimension in videos.

A second industrial consortium, the WiGig Alliance for Wireless Gigabit Alliance has proposed its own standard in December 2009 [**16**]. This organization includes 15 technology leaders: Atheros Communications, NEC, Broadcom, Nokia, Dell, NVIDIA, Intel, Panasonic, LG Electronics, Samsung Electronics, Marvell International, Toshiba, MediaTek, Wilocity and Microsoft. Some companies are also part of this consortium only working as contributors such as NXP, STMicroelectronics and Texas

Instruments. The specification proposed by the WiGig Alliance is quite similar to the one proposed by the WirelessHD SIG and reaches 6.9Gbps data rate.

Finally, a second public standardization organization, ECMA international, has also proposed a multi-gigabit-per-second wireless standard, called ECMA-387, in December 2008 [**17**]. Here again, the standard is quite similar to the WirelessHD one.

The specifications which will be detailed in this section are extracted from the WirelessHD 1.0 standard [**15**] as it was finalized before the other ones. However, Task Group IEEE 802.15.3c is working on the compatibility with the WirelessHD specification. The two other standards introduced here should also be compliant with the WirelessHD specification.

The WirelessHD 1.0 specification incorporates the PHY and MAC layers, and also error protection, framing and timing control techniques in order to guarantee a sufficient consumer Quality-of-Service (QoS) for Audio and Video applications. Antenna beam steaming/forming will allow adaptively control of signal radiation angle to build a new transmission path with reflections when the Line-of-Sight (LOS) direct communication could not be established.

i. Frequency band & channels organization

First of all, the frequency band was chosen between 59 and 66GHz, thus providing 7GHz bandwidth. The use of an additional band between 57 and 59GHz should be allowed too. This 9GHz bandwidth is then divided in at least 4 channels that should be able to provide up to 2.5Gb/s each as depicted in Figure I-6. But those 4 channels could be reorganized in several smaller channels each providing a lower data rate to match the need of the application.

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (MHz)	Roll-Off Factor
A1	57.240	58.320	59.400	1728	0.25
A2	59.400	60.480	61.560	1728	0.25
A3	61.560	62.640	63.720	1728	0.25
A4	63.720	64.800	65.880	1728	0.25

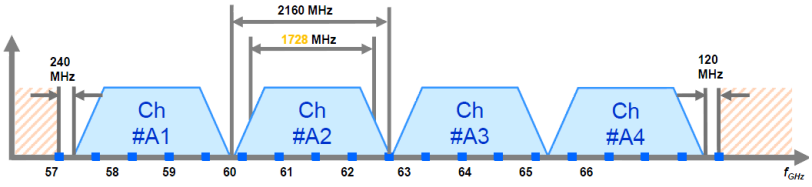


Figure I-6 Channel organization of the 57-66GHz Band [18**]**

ii. Modulation

WirelessHD uses Orthogonal Frequency Division Multiplexing (OFDM) coding technique with 512 subcarriers and Quadrature Phase-Shift-Keying (QPSK) or 16 Quadrature Amplitude Modulation (QAM) modulations depending of the requested data rate.

In OFDM [**1**], a large number of closely-spaced orthogonal subcarriers are used to carry data. The data is divided into several parallel data streams, one for each subcarrier. Hence OFDM spreads the high data rate requested by the application into several lower data rate channels working each at its own subcarrier frequency. Then, each subcarrier is modulated with a conventional modulation scheme – such as PSK or QAM – at a low symbol rate.

In OFDM, the sub-carrier frequencies are chosen so that the subcarriers are orthogonal to each other, which means that the peak of one subcarrier occurs when other subcarriers are at zero as illustrated in Figure I-7. Hence the cross-talk between the sub-channels is eliminated and inter-carrier guard bands are not required.

Mathematically, the orthogonality requires that the subcarrier spacing Δf is a multiple of the inverse useful symbol duration T_U as written in the equation (I.2) where k is an integer (typically equal to 1).

$$\Delta f = k/T_U \tag{I.2}$$

Therefore, with N subcarriers, the total signal bandwidth B will be N times the subcarrier spacing Δf.

$$B = N.\Delta f \tag{I.3}$$

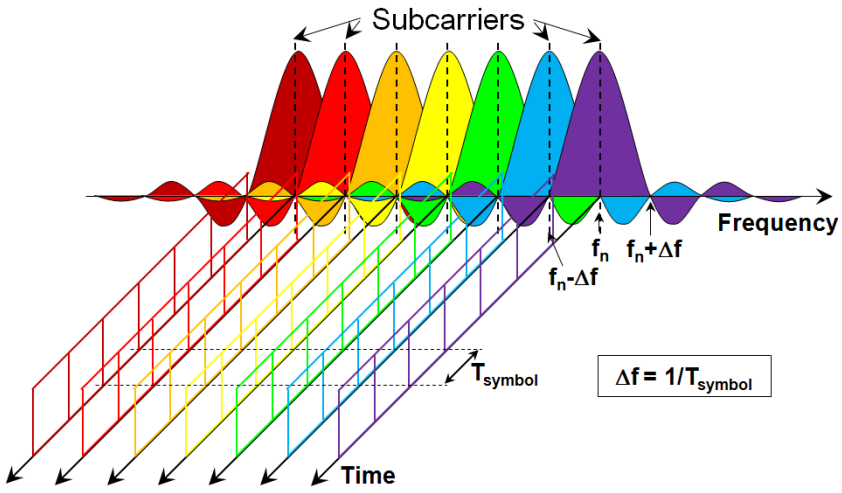


Figure I-7 OFDM principle based on several orthogonal subcarriers

OFDM has been chosen for WirelessHD standard because of its robustness against narrow-band co-channel interference and against inter-symbol interference and fading caused by multipath propagation. Moreover OFDM can also easily adapt to severe channel conditions and present a very high spectral efficiency. The main limitation of OFDM is the high Peak-to-Average-Power Ratio (PAPR) induced – as the phases of the subcarriers are independent, they will often combine constructively – which requests the implementation of very linear transmitter circuitry, and thus complicates the design of the power amplifier.

iii. Spectral mask and power levels

The transmitter output signal should conform to the spectral mask represented in Figure I-8 (relative power levels and frequency).

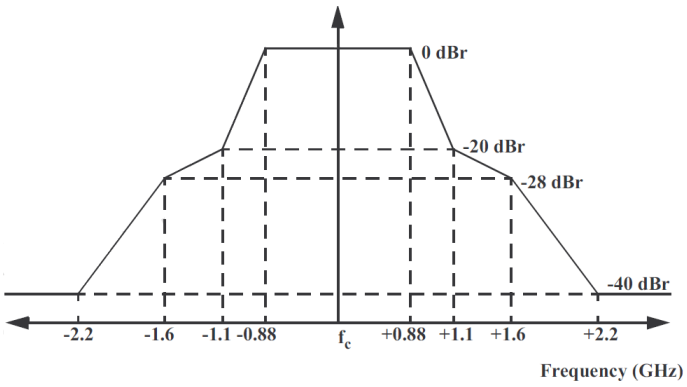


Figure I-8 Transmitter spectral mask for one high rate channel

The typical RF power at the antenna connector is fixed to 10dBm (10mW) and antenna gain should not exceed 10dBi (50° angular aperture). The resulting radiation level (EIRP) should not exceed 20dBm which is lower than the maximum allowed EIRP fixed at 40dBm.

However, the 10dBm RF power at the antenna connector does not include the around 9dB PAPR induced by the OFDM modulation. This results in a much more difficult constraint as the transmitter should be able to generate 19dBm RF output power at the antenna connector while it is still working in a linear mode.

I.2. mmW transmitters in Silicon technology

I.2.1. Transmitter architectures

Although signal generation can differ with the chosen modulation and with the architecture, Radio-Frequency transmitters always integrate a power amplifier (PA) and an antenna. The baseband signal (usually digital in actual systems) can actually be up-converted to RF by different architectures: homodyne (direct conversion), heterodyne (one or two-step conversion using an intermediate frequency), or some alternative architecture such as all-digital transmitter for software defined radio [**19**]. However in classical architectures, the up-conversion (or down-conversion in a receiver) is done by a mixer.

But the power at the mixer output does not achieve the specifications in almost all the cases. The signal should be amplified by a Power Amplifier to reach the requirements of the targeted standard. However, PAs are not ideal components and have many parasitic non-linear effects (see Annex C), which should sometimes be compensated by adding a filter just before the antenna. However, for mmW applications, the harmonic frequencies ($2.f_0$, $3.f_0$ …) are very far from the center frequency f_0 and are naturally filtered by the passive devices connected to the RF path such as the transmission lines, the pad, the wire-bonds or even the antenna itself. Hence the harmonic filter is not needed for mmW frequencies. Thereby, PAs are generally the last component before the antenna.

Figure I-9 shows the architecture of RF transmitter last stages. The power amplifier can be divided in 3 blocks as the active module (with power transistors) has to be impedance matched at its input and output. Here we have considered that the modulation and the up-conversion were integrated in the RF signal generation module and it is not really useful to be detailed in this work.

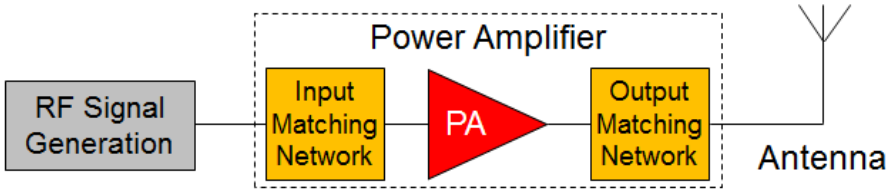


Figure I-9 Power Amplifier and Antenna can be found in all RF transmitters

As explained in section I.1.2, millimeter waves are quickly attenuated and the losses due to the wave propagation in the air have to be compensated. To compensate those losses due to the wave propagation in the air, the first idea would consist in increasing the gain of the PA resulting in a higher output power at the antenna connector. But technology considerations often limit the use of this technique. The second method, which is also often used, consists in increasing the directivity of antennas as, except in specific broadcast applications, a transmitter has to communicate in only one direction, the one of the receptor; all the power emitted in other directions being useless. It is also possible to combine those two techniques, thus creating a transmitter with reasonable output power levels and connecting an antenna with also reasonable directivity.

High directivity antennas can be realized with horn wave-guides. But such antennas cannot be integrated in a chip unlike patch antennas which are much easier to integrate. However to increase the directivity of a patch antenna, several patch elements have to be integrated in an array with specific phase on each element to ensure a good combination of the electromagnetic waves in the air.

Having several small antennas organized into an array, each antenna can be driven independently from the others. This is called beam-forming. Several antennas emit the same input signal with specific phase and amplitude deviations for each antenna [**20**]. Due to the difficulty of changing the phase and amplitude of a high power signal, several RF-chains are used to perform beam-forming, one per antenna. This technique permits to reduce the constraints in terms of saturated and 1dB compression output power and in terms of gain on the PAs. An evolution of such beam-

forming technique, called beam-steering, consists of implementing phase and amplitude elements on each chain that can be tuned. Constructive and destructive interferences of the emitted signals result in a preferred radiation directivity of the antenna array, thus resulting in a beam of the antenna that can be directed to follow the receiver. However this last technique is difficult to implement with sufficient precision and sufficient efficiency in terms of power consumption at mmW frequencies and its circuit implementation is currently still in study in many research teams.

The wave combination in the air proposed by the beam-forming technique can also be realized in the circuit just before the antenna. A transformer can actually be used to connect the output of several PAs to a single antenna. The interest here is also to reduce the constraints on each elementary PA. See section C.3 in Annex C for more details.

A state-of-the-art on mmW transmitters can be found in Annex B.

I.2.2. Power Amplifier

The Power Amplifier is a critical block in a transmitter chain as it is often the last one before the antenna. Some generalities on PAs can be found in Annex C. A brief state-of-the-art of mmW PAs and a practical example with the pre-PA that is used in this PhD work are detailed hereafter.

i. State of the art of mmW PA

Table I-1 (see the next page) summarizes the main characteristics of the mmW PAs in GaAs, InP, SiGe and CMOS technologies published over the last 15 years.

However performing some measurements at those very high frequencies is not an easy task and it is often difficult to obtain directly the desired characteristics without any measurement artifact. De-embedding techniques are hence widely used to be able to deduce the desired characteristics from the measurement results. Moreover we have also used some de-embedding techniques in this PhD work to extract the significant results from the measurements as it is presented in Annex G.

As a consequence, the validity of those results should hence be balanced with the measurement conditions and with the de-embedding techniques. So we advise the readers to keep a critical eye on the values collected in the literature and summarized in this table.

Moreover those published results do not integrate every characteristic that could be requested by an industrial company before integrating a power amplifier in an end-user product. As an example, the reliability performance (with respect to ESD, impedance mismatch, or in terms of device lifetime…) is not considered here which is critical for the semiconductor provider that needs to guarantee a certain product quality to his customers.

Power Amplifiers at millimeter-Wave frequencies where first designed in III-V technologies such as GaAs or InP. The first publications of 60GHz PA in III-V technologies actually date from the mid-1990's. During 10 years, only III-V technologies were used for mmW PAs as such frequencies were exclusively used for military and spatial applications. However, in mid-2000's low-cost technologies were requested by the emergence of mass market applications. Between 2004 and 2007 most of the mmW PA publications concern BiCMOS SiGe technologies. When mmW PAs in SiGe technologies became competitive, the focus has migrated progressively to CMOS technologies. Since 2007, most of the publications effectively concern CMOS technologies.

Figure I-10 (on the page 27) shows the evolution of the ITRS Figure-Of-Merit (FOM) [**21**] with respect to the publication date for the different technologies. The FOM is calculated using the formula (I.4), where P_{sat} is the saturated power in [W], *Gain* is the linear gain [unit less], *PAE* is the power added efficiency in [%] and *f* is the frequency in [GHz].

$$FOM_{PA} = P_{sat}.Gain.PAE.f^2 \quad \text{(I.4)}$$

	Tech. [µm]	Freq. [GHz]	Bandwidth [GHz]		Mode	Nb. Stg.	Arch.	Comb.	P_{sat} [dBm]	G_{sat} [dB]	P_{1dB} [dBm]	G_{max} [dB]	PAE peak [%]	P_{DC} [mW]	Size [mm²]	FOM	Reference
GaAs pHEMT	0.1	60	-	-	s	2	-	2x	24.3	9.4	24	12	24	-	5.46	3 686	S.-W. Chen [22]
		60	55	64	b	2	-	-	9.5	3	7.5	12.8	-	-	7.56	-	M. Han [23]
		62.5	-	-	b	2	-	-	27.5	9.8	25	13	21	-	10.4	9 204	O. S. A. Tang [24]
		62.5	-	-	s	2	-	-	24.7	9.7	23	13.5	26	-	7	6 710	O. S. A. Tang [24]
	0.15	60	45	65	s	3	CS	-	12.5	8	9	18	-	-	6	-	C. Kärnfelt [25]
		60	48	55	s	3	CS	-	> 16	< 12	14	15.5	-	-	3	-	M. Käirkkainen [26]
		60	50	65	s	3	CS	-	16	7.5	15	12	6.23	525	4.5	142	M. Varonen [27]
		60	55	64	s	3	CS	2x	15	12	12	16	-	-	2.18	-	Y. Mimino [28]
		60	59	64	s	2	-	-	25	11	23	18	27	-	10.66	19 394	R. Lai [29]
		60	57	63	s	3	CS	2x	19	10	17	13.4	7.33	975	4.5	459	M. Varonen [30]
		60	-	-	s	1	CS	-	16	5	15	8	-	-	2	-	M. Abbasi [31]
		60	-	-	s	2	CS	-	16	11.5	15	15	-	-	2.5	-	M. Abbasi [31]
InP HEMT	0.1	60	50	65	s	1	-	-	23.5	7.5	23	10.5	43	-	3	3 888	W. M. T. Kong [32]
	0.12	60	56	63	s	1	-	-	24	7.1	22	10	43	-	2.85	3 888	A. O. S. Tang [33]
	0.15	62	59	64	s	2	-	-	30	15	29	20	21	-	-	80 724	Y.C. Chen [34]
		95	82	98	s	2	-	-	26.3	8.9	24	12	20	-	3.55	12 203	D. L. Ingram [35]
SiGe	0.12	61.5	-	-	d	2	CE	-	16.2	2	11.2	10.8	4.3	375	1.68	82	B. A. Floyd [36]
		77	75	80	s	2	Casc +CE	-	14.4	10	12	19	15.7	161	-	2 036	S. T. Nicolson [37]
		77	65	80	s	4	CE	2x	17.5	12	14.5	17	12.8	405	0.6075	2 139	A. Komijani [38]
	0.13	58	-	-	s	-	-	-	11.5	1	-	4.2	20.9	-	-	26	A. Valdes-Garcia [39]
		60	58	65	d	1	Casc	-	20	4.5	13.1	18	12.7	240	0.975	2 885	U. R. Pfeiffer [40]
		61.5	59	64	d	1	Casc	-	17	-	10.5	15	10	288	-	599	S. K. Reynolds [41]
		61.5	-	-	d	1	Casc	-	14	2.5	8.5	12	4.2	264	0.625	63	U. R. Pfeiffer [42]
		77	-	-	d	2	CE	-	12.5	4.5	11.6	6.1	3.5	325	1.575	15	U. R. Pfeiffer [43]
		85	73	97	s	8	Casc	4x	21	5	-	8	3.4	-	2.4	195	E. Afshari [44]
		60	59	64	d	1	Casc	4x	23	13	21.5	22	6.3	1200	3.42	7 172	U. R. Pfeiffer [45]
	0.18	60	-	-	b	3	CE	-	15.8	-	11.2	11.5	16.8	281	0.9	325	C. Wang [46]
	0.2	77	-	-	d	1	Casc	-	18.5	-	-	-	5.4	-	-	-	H. Li [47]
CMOS	0.065	60	45	65	s	3	CS	-	7	4	1.5	13	2.42	124.8	0.609	8.71	M. Varonen [48]
		60	57	65	s	2	CS	-	13	3	8.9	8	11	64.8	0.288	49.85	S. Aloui [49]
		60	57	65	d	3	CS	-	11.5	3	2.5	15.8	11	43.5	0.0533	212.66	W. L. Chan [50]
		60	55	65	d	2	CS	4x	17.9	6.8	15.4	18.8	11.7	460	0.825	1970.1	J.-W. Lai [51]
		60	53	68	b	2	Casc	8x	18.1	8	11.5	15.5	3.6	1504	0.462	296.9	B. Martineau [52]
		62	55	65	s	1	CS	-	9	-	6	4.5	9	27.6	0.27	7.31	A. Valdes-Garcia [53]
	0.09	60	52	65	s	3	CS	-	9.3	0	6.4	5.2	7.4	39.75	0.1505	7.51	T. Yao [54]
		60	43	65	d	2	CS	-	12.3	2.5	9	5.5	8.8	-	0.2508	19.09	D. Chowdhury [55]
		60	-	-	s	4	CS	2x	10.6	0.5	8.2	8.3	2.35	228.6	0.975	6.57	T. Suzuki [56]
		60	60	64	s	3	CS	2x	11	9	10	14.3	8.2	150	0.18	100.03	M. Tanomura [57]
		60	57	65	d	4	CS	-	12	11	10.2	15	14.0	84	0.15	252.60	T. LaRocca [58]
		60	52	64	s	2	CS	2x	11.6	1.5	10.1	8.2	11.5	81	1.0292	39.54	M. Bohsali [59]
		60	57	65	s	4	CS	2x	12	7	8.2	20	9.0	146	0.649	513.51	D. Dawn [60]
		60	55	71	s	3	Casc	4x	14.5	14	10.5	26	10.2	286	0.64	4120.1	Y.-N. Jen [61]
		60	58	66	s	4	CS	4x	20	12	18	20.6	14.2	-	1.7575	5869.4	C. Y. Law [62]
		61	57	65	s	2	Casc +CS	-	8.4	8	5.1	17	5.8	54	-	74.83	S. Pinel [63]
		62	60	65	s	2	CS	-	-	-	4	12.2	24	10.4	0.4826	-	B. Heydari [64]
		70	0	70	s	2	CS+ Casc	-	10	-	10	7	6.14	122	0.72	15.08	M.-D. Tsai [65]
		77	65.7	83.2	s	4	CS	2x	6.3	2	4.7	8.5	1.71	142.2	0.975	3.06	T. Suzuki [56]
	0.13	60	51	65	s	3	Casc	-	-	-	2	12	2.70	54	1.3	-	C. H. Doan [66]
		60	55.5	62.2	s	5	Casc	-	7.8	2.5	7	13.5	3.00	-	1.8	14.57	B. Wicks [67]
	0.065 SOI	60	50	66	s	2	Casc	-	10.5	3	7.1	14	22.3	22	0.5734	226.26	A. Siligaris [68]

s=single-ended | b=balanced | d=differential | CS=common source | CE=common emmiter | Casc=cascode

Table I-1 State-of-the-art of mmW PA

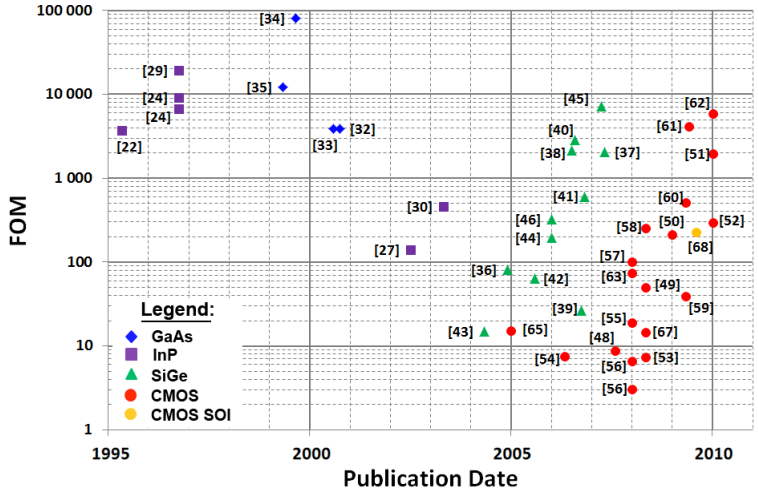


Figure I-10 FOM of mmW PA with respect to the publication date

PAs in SiGe and CMOS technologies both present a global growth of their performances. However the FOM of III-V technologies PAs are still difficult to reach with low-cost technologies.

On another side, the FOM defined in the equation (I.4) does not integrate any notion of linearity and bandwidth which are two key characteristics of PAs for WirelessHD applications as explained in section I.1.3. A PA with a lower FOM but with a good linearity – i.e. a high 1dB compression point – and no ripple on the full 57-66GHz frequency band will be preferred in the design of a full WirelessHD transmitter.

ii. Pre-Power Amplifier used in this PhD work

The power amplifier used for this PhD work (notably in Chapter IV) is a simplified version of the power amplifier proposed by Baudouin Martineau in [**52**] as it integrates only one differential signal path and hence does not integrate any power combiner. This PA has also been designed by Baudouin Martineau – and was hence directly available in our Design Team from STMicroelectronics – in order to work as a driver to the complete power amplifier exposed in [**52**], thus working as a Pre-Power Amplifier (PPA).

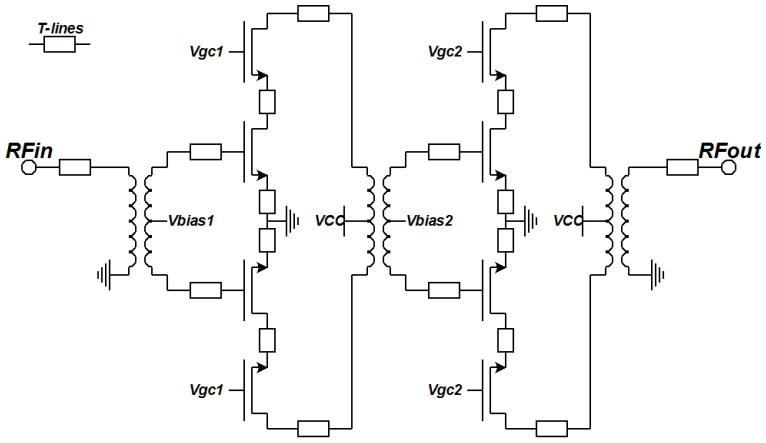
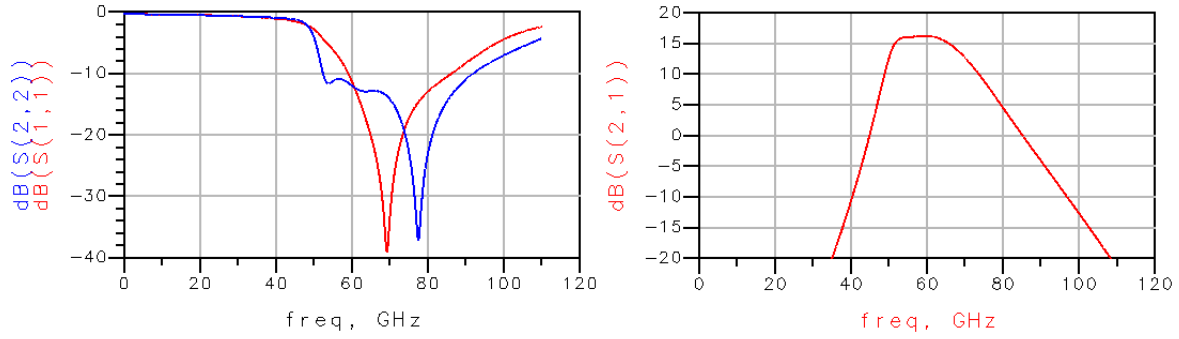


Figure I-11 Schematic of the PPA used in this PhD work

This solution has been chosen as this PPA exhibits a sufficient output power level to be used in a VSWR regulation loop while minimizing the cost in terms of design time and complexity. Moreover, when this solution has been chosen in mid-2009, both PPA and PA were not measured yet. Hence the PPA introduced a much lower risk level compared to the complete PA as there is a lower number of transformers with unknown electro-magnetic coupling effects between those transformers.

Figure I-11 shows the schematic of the designed PPA where the rectangles represent the transmission lines. The PPA is based on a balanced structure with two stage cascode topology. The cascode topology has been chosen for reliability considerations (see section I.3.3) and to ensure a sufficient output voltage swing which means a high output power level. The inter-stage matching and the input and output single-ended to differential conversion are made using small transformers used as baluns. This solution has been proposed by the University of California in Berkeley in [**55**] as an effective way to perform the impedance transformation and the differential to single-ended conversion simultaneously.

Figure I-12 shows the simulated S-parameters of this PPA. The input and output matching parameters, respectively S_{11} and S_{22} are well matched to 50Ω – matching parameter lower than -10dB – on a wide bandwidth from 60GHz up to 88GHz, limited by the input S_{11}. The transmission parameter S_{21}, represented on the diagram b., presents also a wide bandwidth from 52GHz up to 64GHz where the PPA gain is around 16.4dB with very low ripple over the full bandwidth.



a. **b.**

Figure I-12 Simulated S_{11} and S_{22} matching (a.) and S_{21} transmission (b.) S-parameters of the PPA

Figure I-13 shows the result of a harmonic balance simulation with a 60GHz sinewave signal applied at the PPA input.

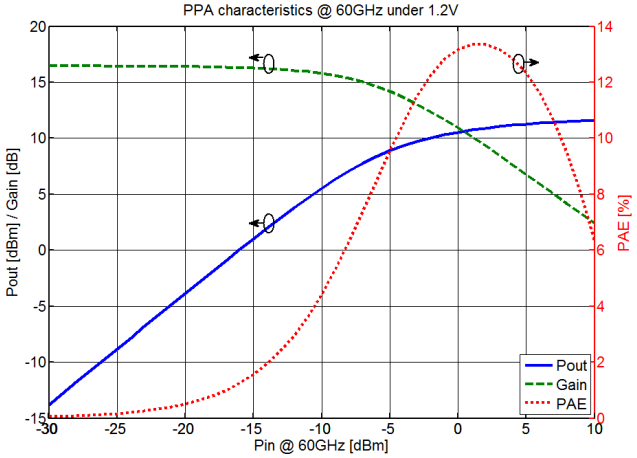


Figure I-13 Output power, Gain and PAE characteristics of the 60GHz PPA with respect to the input power

The PPA exhibits hence a 16.4dB small signal gain, a 1dB compression point output power P_{-1dB} of 6.5dBm, a 12dBm saturated output power (but with only 3dB gain), and a 13.2% maximum *PAE*. It can be noted that the P_{-1dB} is very far from the 19dBm linear output power required by the Wireless HD standard (see section I.1.3.iii). However this amplifier integrates only one signal path with no power combining technique, reason why it is called pre-power amplifier. This consideration being made, this PPA exhibits good characteristics which are comparable to the state-of-the-art of CMOS power amplifiers (see section I.2.2.i).

During all those simulations, the PPA consumes around 80mW DC power under a 1.2V supply voltage which is the standard supply voltage in 65nm CMOS technology using low V_t transistors. The active area is 0.045mm².

I.3. Antenna impedance variation with environmental conditions

I.3.1. Introduction to standing wave formation

A Matlab model has been developed in order to illustrate the progressives and standing waves concepts. Hence we consider a transmission-line with a given length called L and a given propagation constant β. At the input of this T-line is applied a sine wave signal V_{in} with an amplitude *amp*, a frequency f_0 and a phase φ_0:

$$V_{in} = amp.\sin\left(2\pi f_0.t + \varphi_0\right) \tag{I.5}$$

This sine wave signal will propagate along the T-line which presents an attenuation constant α (some details on transmission line theory can be found in Annex E). The incident wave $V_i(x,t)$ defined at time t and on point x of the T-line will hence be given by the equation (I.6).

$$V_i\left(x,t\right) = amp.\exp\left(\alpha.x\right).\sin\left(2\pi f_0.t - \frac{2\pi}{\lambda_0}.x + \varphi_0\right) \tag{I.6}$$

At the end of this T-line (where $x = L$) is placed an electrical load defined by its impedance Z_L. If this load impedance Z_L is different from the reference impedance of the T-line Z_0 (see Annex E), the reflection coefficient Γ_L defined in the equation (I.7) will be non-zero ranging from -1 to +1 in extreme conditions when Z_L is equal to 0 (short) or +∞ (open) respectively.

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{I.7}$$

The incident wave $V_i(x,t)$ defined in the equation (I.6) will be reflected on this load with the reflection coefficient Γ_L defined in the equation (I.7), thus creating a reflected wave $V_r(x,t)$ that is given by the equation (I.8).

$$V_r\left(x,t\right) = \left|\Gamma_L\right|.amp.\exp\left(\alpha.\left(x-2L\right)\right).\sin\left(2\pi f_0.t + \frac{2\pi}{\lambda_0}.\left(x-2L\right) + \varphi_0 - \varphi_{\Gamma_L}\right) \tag{I.8}$$

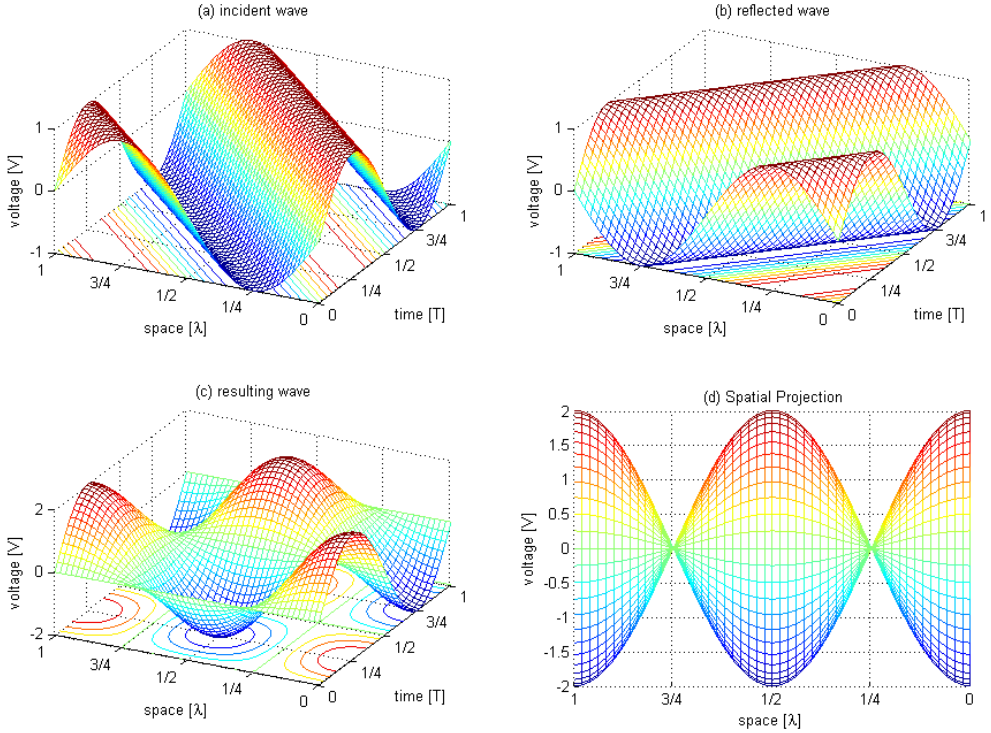
The incident and the reflected waves both propagate along the same T-line. The resulting voltage $V(x,t)$ at point x of the T-line and for time t is hence the sum of the incident and the reflected voltages as written in the equation (I.9).

$$V\left(x,t\right) = V_i\left(x,t\right) + V_r\left(x,t\right) \tag{I.9}$$

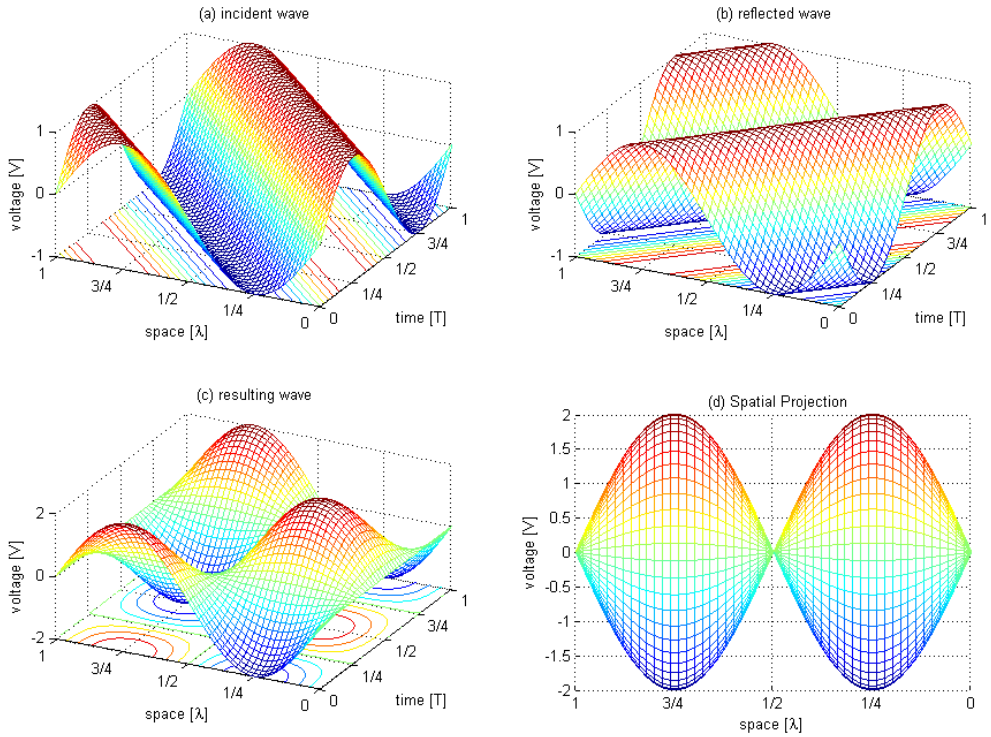
However those two waves propagate in opposite directions to each other and interfere together. At this point, it is much easier to make some mathematical simplifications to be able to calculate those interferences. The T-line will hence be considered ideal – the attenuation coefficient α will be set to zero – and the input sine wave signal will have a 0° phase φ_0. Those two simplifications being made, the voltage $V(x,t)$ is a combination of a progressive wave (the second part of the equation, highlighted in green) and of a standing wave as the time (highlighted in red) and the space (highlighted in blue) components are no more linked together in the first part of the equation (I.10).

$$V\left(x,t\right) = \begin{pmatrix} 2.\left|\Gamma_L\right|.amp.\sin\left(2\pi f_0.t - \frac{2\pi}{\lambda_0}.L - \frac{\varphi_{\Gamma_L}}{2}\right).\cos\left(-\frac{2\pi}{\lambda_0}.x + \frac{2\pi}{\lambda_0}.L + \frac{\varphi_{\Gamma_L}}{2}\right) \\ +\left(1-\left|\Gamma_L\right|\right).amp.\sin\left(2\pi f_0.t - \frac{2\pi}{\lambda_0}.x\right) \end{pmatrix} \tag{I.10}$$

Figure I-14 and Figure I-15 illustrate the wave propagation on an ideal T-line of λ length terminated at its extremity ($x=\lambda$) by an open circuit ($Z_L=+\infty$; $\Gamma_L=+1$) and a short circuit ($Z_L=0$; $\Gamma_L=-1$) respectively. The source impedance is fixed to $Z_0=50\Omega$. For each configuration, the incident wave (a.), the reflected wave (b.), the sum of both waves (c.) and its spatial projection (d.) have been plotted.



Incident (a) and reflected (b) progressive waves, the resulting standing wave (c) and its spatial projection (d)
Figure I-14 Creation of standing waves for a reflection coefficient of +1

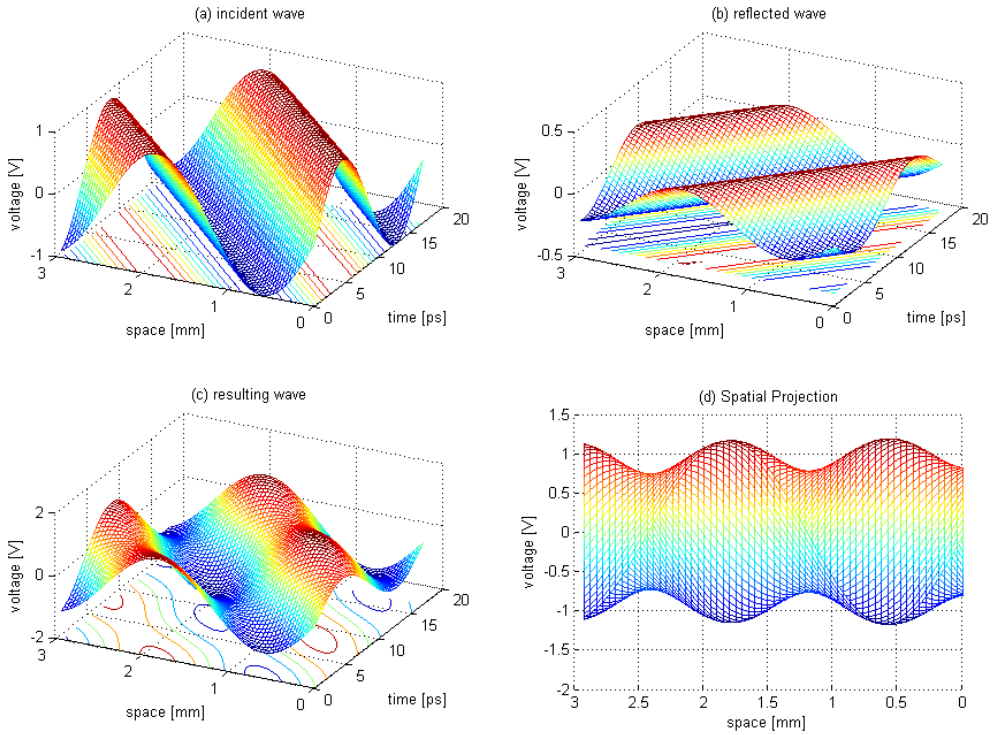


Incident (a) and reflected (b) progressive waves, the resulting standing wave (c) and its spatial projection (d)
Figure I-15 Creation of standing waves for a reflection coefficient of -1

In the two extreme conditions open and short, no progressive wave result from the sum of the incident and the reflected wave. As can be seen on the diagrams d. of Figure I-14 and Figure I-15, the time evolution of the global voltage does actually not propagate along the T-line but simply results in a local oscillation of the voltage. This is called a standing wave. The points were no oscillation occurs are called the nodes of the standing wave and the points were the oscillation is maximal are called resonant points.

However, the location of the resonant points and of the nodes of the standing wave are opposite between the two configurations. This is mathematically expressed by an opposite phase $\varphi_{\Gamma L}$ of the reflection coefficient Γ_L.

Now let us consider a non-extreme condition when Γ_L is equal to *0.2+0.1*j*, and a more realistic case of a 2.9mm length T-line (*1.2*λ* at 60GHz in silicon dioxide) which present 1.2dB/mm attenuation coefficient α for a 60GHz 1V amplitude sinewave signal. The Matlab simulation results have been plotted in Figure I-16 in the same disposition that for the previous simulations.



Incident (a) and reflected (b) progressive waves, the resulting standing wave (c) and its spatial projection (d)
Figure I-16 Creation of standing waves for Γ=0.2+j*0.1 and 1.2dB/mm attenuation coefficient on the T-line

In this ordinary case, the resulting wave is composed of a standing wave component as described previously and a progressive wave component (which is the part really emitted by the antenna in a practical case). The amplitude of the resulting progressive wave can be calculated on the diagram d. of Figure I-16 as the maximum amplitude of the global wave when located in a node of the standing wave – i.e. where the standing wave contribution is null.

The Voltage Standing Wave Ratio is then defined as the ratio of the standing wave to the progressive wave, i.e. the ratio of the maximum voltage to the minimum voltage. This ratio is also commonly calculated using the reflection coefficient Γ_L as written in the equation (I.11).

$$VSWR = \frac{\max\left(V\left(x,t\right)\right)}{\min\left(V\left(x,t\right)\right)} = \frac{1+\left|\Gamma_L\right|}{1-\left|\Gamma_L\right|} \tag{I.11}$$

I.3.2. 60GHz VSWR measurements

i. Link between electro-magnetic obstacles and antenna impedance variation

In the previous section we have consider an electrical load Z_L at the end of the T-line. This load impedance was introduced in the theoretical approach to represent the impedance of the antenna in a real transmitter. In practice, the incident signal is generated by a PA and propagates through a transmission line before reaching the antenna.

Moreover an antenna is a transducer that converts an electrical signal into an electro-magnetic wave – or inversely – and the antenna impedance is a direct function of its topology. Adding some parasitic elements in the field of an antenna will hence cause a variation of the antenna impedance.

Figure I-17 illustrates this phenomenon: an incident signal V_i (in blue) generated by the PA propagates through the T-line to the antenna where it is converted into an electro-magnetic wave (also in blue); this wave is reflected on the electro-magnetic obstacle thus creating a reflected wave (in red) which is converted by the antenna into a reflected signal V_r (also in red). The resulting electro-magnetic wave (in green) is the sum of the incident and the reflected waves. The same operation occurs in the electrical domain on the T-line, the resulting signal (not represented) is the sum of the incident V_i and the reflected V_r signals. This electrical phenomenon is the consequence of the variation of the antenna impedance as explained in the previous section.

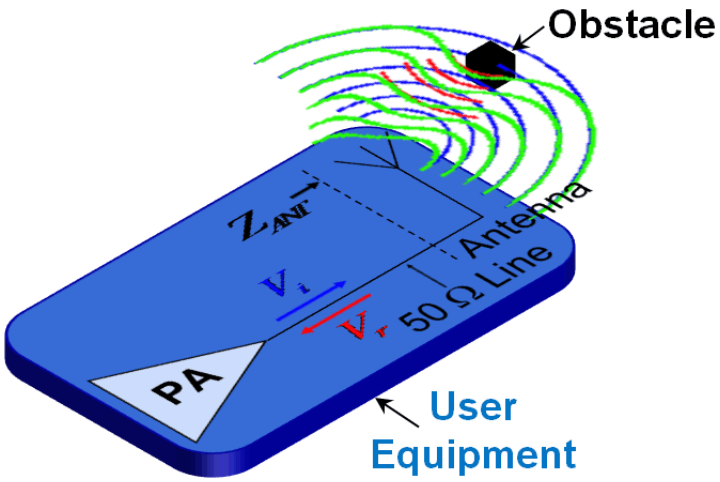


Figure I-17 Link between electro-magnetic obstacles and antenna impedance variation

The link between EM obstacle and antenna impedance variation being established, it would be of great interest now to quantify this phenomenon. Unfortunately, at mmW frequencies, the literature looks very poor on the subject. The only publication we have found [**69**] explores the effect of a human body on the impedance of a horn antenna for GSM applications at 450 and 900MHz.

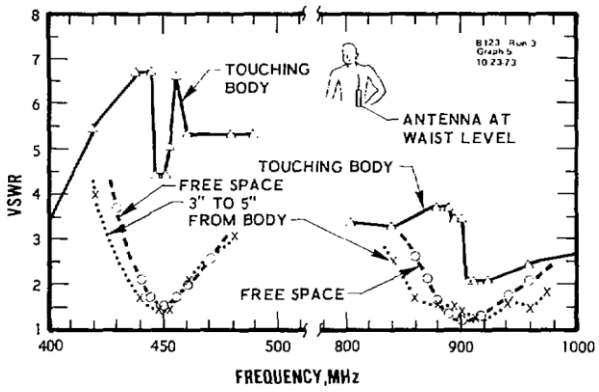


Figure I-18 Link between electro-magnetic obstacles and antenna impedance variation [69**]**

Figure I-18 illustrates the measurement results they have obtained. In the 450MHz band, a human body touching the antenna can generate a VSWR of up to 7:1 while it is only 4:1 around 900MHz. A VSWR of 7:1 means that, considering purely real impedance, the antenna impedance varies between 7 and 350Ω while it should be 50Ω. However the 60GHz band is very far from the quite low frequencies studied in this publication and the effects of EM obstacles should be very different.

ii. Measurement protocol

We have hence conducted our own measurement campaign at the IEMN laboratory in January 2007 in order to quantify the effects of EM obstacles on the antenna impedance at mmW frequencies. For these measurements, an antenna is directly connected to a network analyzer which measures the reflection coefficient (S_{11} parameter) while a metal plane or a human hand is placed at a certain distance *d* in front of the antenna in its main radiation direction. This experimental assembly is illustrated in Figure I-19.

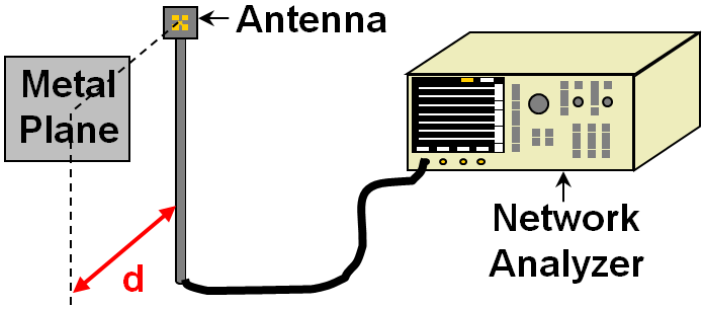


Figure I-19 Experimental assembling for antenna impedance mismatch measurements

First of all, the network analyzer is calibrated on the 55-65GHz frequency band to be automatically de-embedded during the measurements. This is necessary not to integrate any unwanted effect generated by the network analyzer.

The second step of the procedure is to measure the reflection coefficient of the antenna when placed in the free space, without any perturbation. This will generate the reference with respect to which should be compared all the future measurements in obstructed space. By this way, the antenna impedance will not be taken into consideration but the antenna impedance variation will.

The third step consists of adding a metal plane (M.P.) in front of the antenna and measuring the reflection coefficient while varying the distance *d* between the metal plane and the antenna. This corresponds to obstructed vicinity for the antenna. The measured reflection coefficient should be observed with respect to the reference obtained previously in free space conditions.

The last step is to measure the reflection coefficient when touching the antenna with a human hand. As introduced in section I.1.2.ii, the di-hydrogen monoxide molecule presents a high attenuation coefficient at 60GHz [**12**], in the range of its value at 2.4GHz (used by microwave oven). And yet water makes up 55% to 78% of the human body [**1**]. The human body is hence a very good EM obstacle at mmW frequencies. Moreover, a user terminal in the mobile applications of the Wireless HD specifications [**15**] will have to work in close vicinity of the human body.

This measurement procedure is repeated for several mmW antennas. First a horn antenna is tested. Horn antennas are usually more directive than the others as a full 3D structure guides the waves in the desired direction. However this kind of antenna cannot be easily integrated in a chip. Patch antennas, on the other hand, are much easier to integrate in a chip but they present a lower directivity than horn antennas. Hence patch antennas are also tested following the procedure detailed above.

Now patch antennas are constituted by an array of elementary patch elements. The directivity of the antenna array depends of the number of elements used in each direction (*x* and *y* while the antenna main beam will be in the direction *z*). 4-elements (2x2) and 16-elements (4x4) patch antennas have been tested in the same conditions as the horn antenna.

Moreover, patch antennas can generate waves with a linear polarization or with a circular polarization depending of their topology – in fact, depending on the way the different elements are connecter together. In linear polarization, the electric field vector and the magnetic field vector are both confined in their own plane along the direction of propagation $\vec{k}$, as can be seen in Figure I-20.a. In circular polarization, the tip of the electric field vector and the tip of the magnetic field vector, at a fixed point in space, both describe a circle as time progresses [**1**], as can be seen in Figure I-20.b. Both linear and circular polarizations are tested on each of the 4-elements and 16-elements patch antennas.

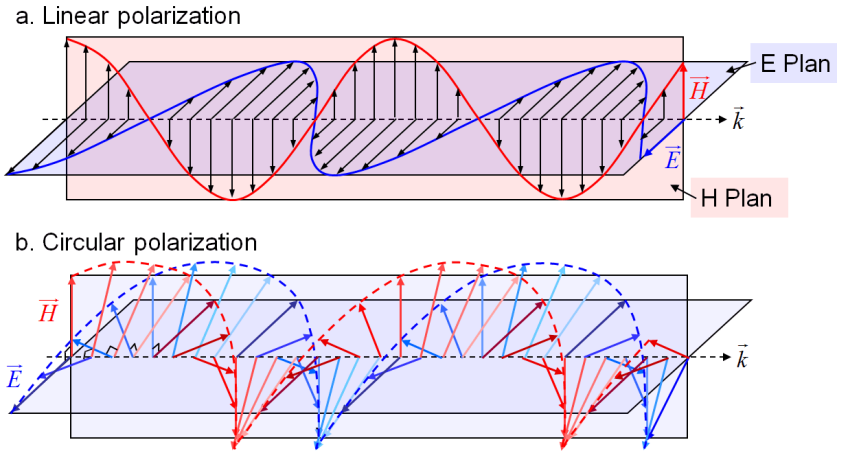


Figure I-20 Linear (a.) and circular (b.) polarization of electromagnetic waves

Figure I-21 shows the photographs of the horn antenna and of the 16-elements linear polarization patch antenna.

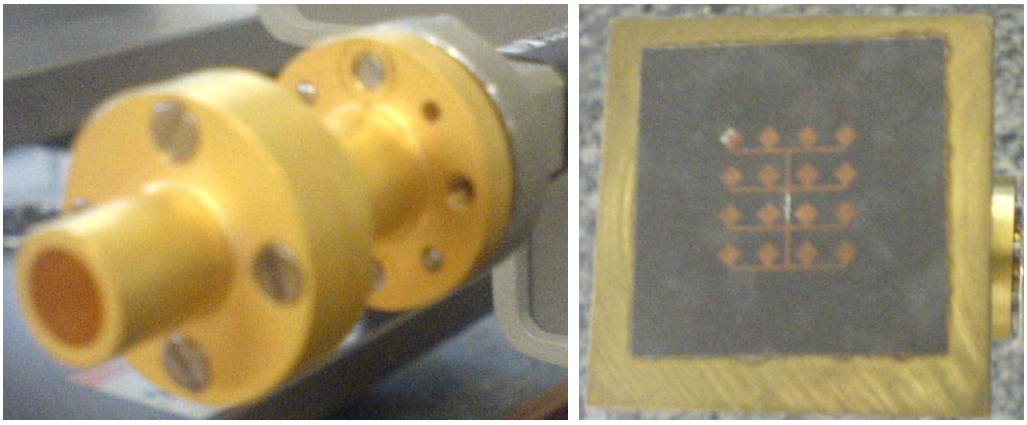


Figure I-21 Horn (left) and Patch (right) antennas

iii. Measurements results

Before beginning the measurement procedure detailed above, we have verify that what we called "free space" could be used as the reference for the other measurements. We have hence measured the reflection coefficient S_{11} of the horn antenna placed in an anechoic chamber (designed for mmW frequencies) and the same antenna placed in the air without any obstacle around (at more than 1m around), what we have called "free space". The incident power from the network analyzer has been set to 0dBm. Figure I-22 shows the measurement results. The magnitude of the antenna S_{11} presents similar results in the two environmental conditions; the anechoic chamber just generates a little less ripple than the "free space". The use of an anechoic chamber is hence not necessary and the following measurements have been performed directly in the lab. This highly simplifies the measurement procedure.

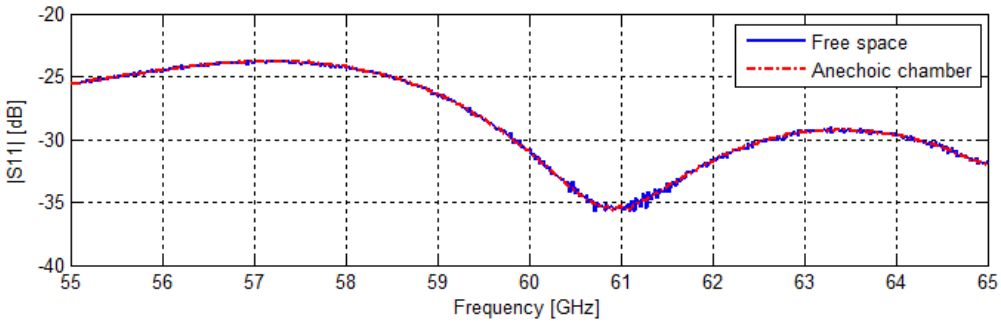
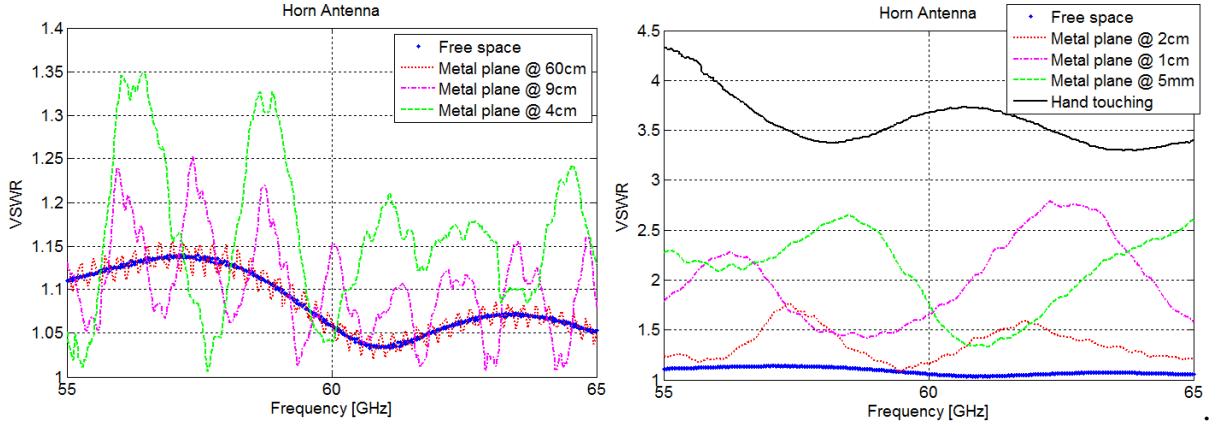


Figure I-22 Free space vs. anechoic chamber reflection coefficient of the horn antenna

Figure I-23.a and b. show the influence in terms of VSWR of a metal plane placed in the far field (more than 4cm) and in the near field (less than 2cm) respectively of the horn antenna. In the far field, the VSWR stays below 1.35:1 but the ripple around the free space value progressively increases while the distance to the EM obstacle decreases. In the near field, the VSWR continues to increase and reaches 3:1 when the obstacle is located at 5mm from the antenna. Figure I-23.b also shows the VSWR of up to 4.5:1 when touching the antenna with the hand.



a. Far field **b. Near field**

Figure I-23 VSWR of the horn antenna with EM obstacle

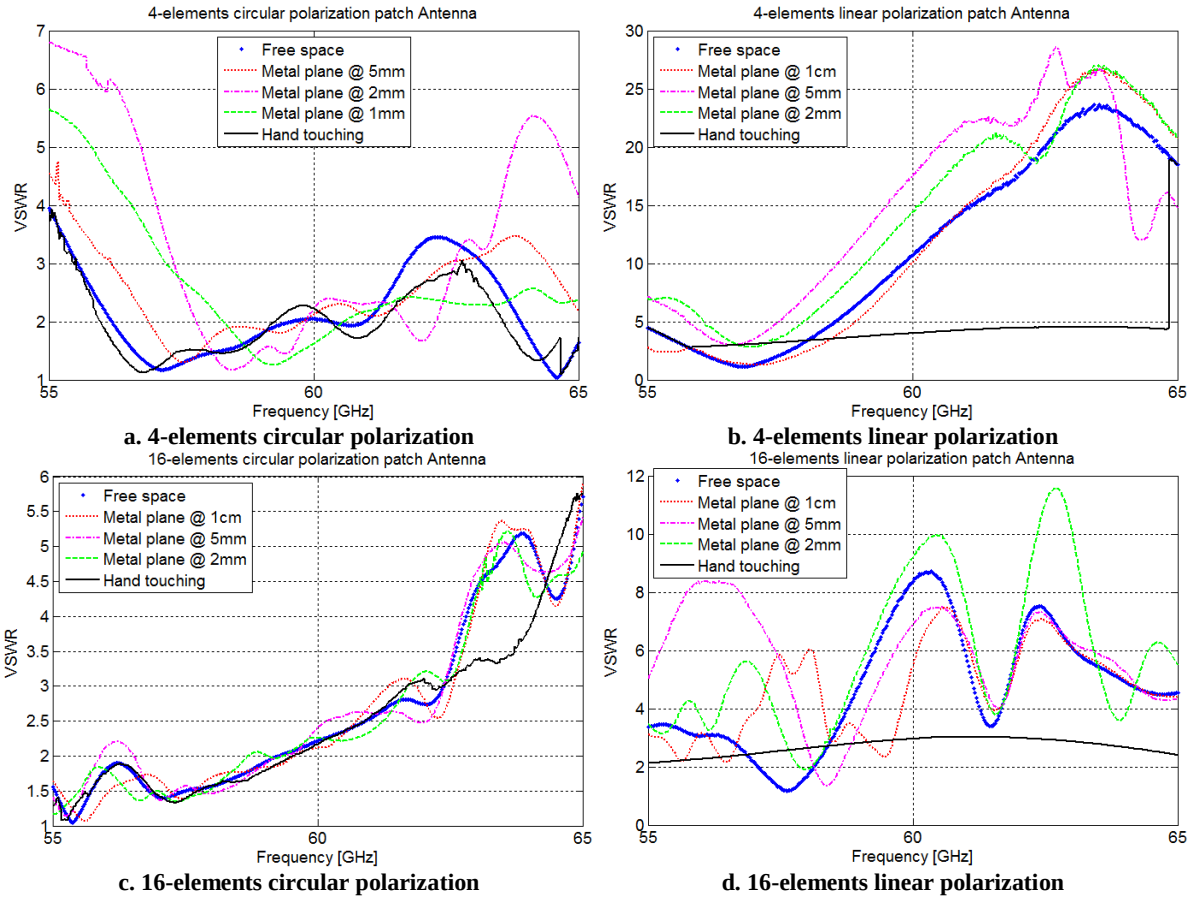
Figure I-24 a, b, c and d show the measurement results in terms of VSWR for the 4-elements circular polarization, 4-elements linear polarization, 16-elements circular polarization and 16-elements linear polarization patch antennas respectively. The first observation is that the studied patch antennas have globally a smaller bandwidth than the horn antenna. The free space response of the different antennas actually present a minimum – close to 1:1 VSWR, which correspond to the best matching to the network analyzer characteristic impedance 50Ω – at 57GHz, 57GHz, 55.5GHz, 57.5GHz (called resonance frequencies) respectively with levels higher than 2:1 VSWR at less than 1GHz from the resonance frequency. This is particularly true for the two linear polarization patch antennas. The horn antenna, in revenge, presents a very flat VSWR level on the full 55-65GHz frequency band.

The 4-elements circular polarization patch antenna shows a progressive detuning with an increase of the resonance frequency when the metal plane is approached to the antenna. However at 57GHz, the original resonance frequency, the VSWR grows up to 5:1. A hand touching the antenna seems to have very low influence on this antenna.

The 4-elements linear polarization patch antenna does not present any detuning due to obstructed vicinity. However at 57GHz, the resonance frequency, the VSWR also grows up to a 3:1 ratio. The hand touching the antenna generates a flat VSWR response which is difficult to interpret as it could be more a consequence of a short cut between some elements of the patch antenna rather than the effects of an electromagnetic obstacle.

The 16-elements circular polarization patch antenna seems to be perturbed neither by the metal plane placed in front of it whatever is the distance between the antenna and the metal plane, neither by the hand touching it.

The 16-elements linear polarization patch antenna presents a growth up to 6:1 VSWR at 57.5GHz, the resonance frequency, when approaching the metal plane to the antenna. The hand touching the antenna presents a flat VSWR response as for the 4-elements linear polarization patch antenna.



a. 4-elements circular polarization **b. 4-elements linear polarization**

c. 16-elements circular polarization **d. 16-elements linear polarization**

Figure I-24 VSWR of the four different patch antennas with EM obstacle

This study on the effect of the environment on the antenna impedance at 60GHz has not the pretention of being exhaustive as it has not been developed by specialist of antennas and electromagnetic wave propagation. The measurement conditions may hence not be perfectly appropriated to those kinds of measurements.

Moreover all those measurements have been performed with antennas and equipment which were available in the laboratory. State-of-the-art components could generate different results. However those measurements give a good idea of the range.

The most significant results of those measurements are the increase of the resonance frequency (detuning) and the increase of the VSWR at the original resonance frequency observed for the 4-elements circular polarization patch antenna. In extreme conditions, with a metal plane placed at 2mm in from of the antenna, the VSWR can reach 5:1 or 6:1.

I.3.3. Effects on Power Amplifiers

Impedance mismatch at PA output stage can result in two effects: over-voltage and over-current. Over-current can generate some electro-migration phenomenon in the access metals [**1**] which can be avoided upstream of the chip fabrication by carefully respecting the minimal metal line width and via number that correspond to the maximal current levels that can occur in the circuit following the rules given in the targeted technology design rules manual [**70**]. Moreover the effects of over-current on CMOS components themselves are very limited as the capabilities of MOS devices in terms of current are very high. Over-current can hence not be considered as a really severe effect of impedance mismatch in MOS technologies.

Over-voltages in revenge can generate several physical phenomenon that can have irreversible consequences on MOS devices. First of all, over-voltage can overcome the maximum capability of MOS transistors and hence produce oxide breakdown or simply generate excessive wear-out that progressively degrades the gate oxide which is usually referred as Time Dependent Dielectric Breakdown (TDDB). Then, with lower voltage levels, Hot-Carriers-Injections (HCI) phenomenon can occur.

At moderate over-voltage levels, the transistors in the output stage will be pushed in triode region. The PA will hence not stay linear causing a degradation of the link quality of the wireless system. However this phenomenon has no durable effect on the transistors and will hence not be detailed here.

i. Time Dependant Dielectric Breakdown (TDDB)

Over-voltages can occur between the gate and the channel – i.e. at the terminals of the gate oxide. A high electric field across the gate insulator could induce soft and hard breakdown of the transistor. The difference between soft and hard breakdown mechanisms is difficult to establish clearly [**71**]. However the dielectric breakdown of the oxide layer in a MOS structure can be defined as a local increase of the system's conductance. This change can be abrupt or gradual depending fundamentally on the oxide thickness, device area and stress condition [**72**]. This is this abrupt or gradual change that will be named respectively hard and soft oxide breakdown. In soft breakdown situation, the transistor is still functional but the threshold voltage and the mobility are degraded. Figure I-25 shows the happening of two soft breakdowns (SBD) and one hard breakdown (HBD) by the observation of the gate voltage of a NMOS transistor during a constant-current stress. Each jump in this characteristic is associated with the opening of a new breakdown spot across the oxide layer.

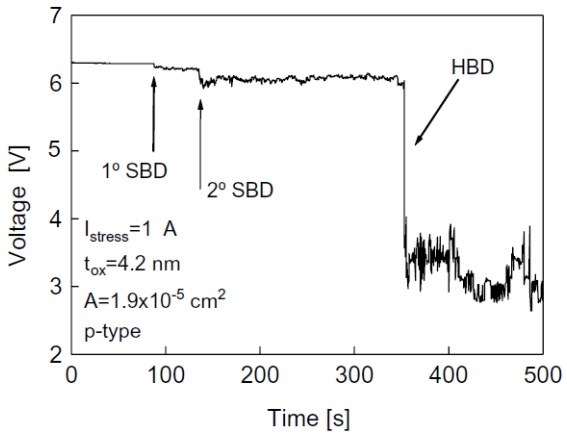


Figure I-25 Evolution of the gate voltage during a constant current stress test during which several breakdown events are detected as abrupt voltage drops

As other features of the device are scaled down, the oxide thickness must be reduced. Oxides become more vulnerable to the voltages fed into the device as they get thinner. An oxide layer can break down instantaneously at 8-11MV per cm of thickness, which means 0.08-0.11V per angstrom of thickness [**73**]. The oxide layer being only 18 angstroms for standard V_T in our targeted 65nm CMOS technology [**70**], the resulting critical voltage level applied across the oxide layer is around 1.44-1.98V in this first coarse study.

The oxide breakdown considered in this study [**73**] includes several physical effects, the most critical in our application being the Time-Dependent Dielectric Breakdown (TDDB) which corresponds to a wear-out breakdown. However it is much easier to explain the phenomenon considering oxide rupture due to Electro-Static Discharge (ESD) events.

At the physical level, a high voltage being applied across the oxide layer causes a weak spot within it to exhibit dielectric breakdown and allow current to flow. This current flow, which is

basically due to loss of dielectric isolation at that spot, causes localized heating, which induces the flow of a larger current. A vicious cycle of increasing current flow and localized heating ensues, eventually causing a meltdown of the silicon, dielectric, and other materials at the hot spot. This meltdown creates a short circuit between the layers supposedly isolated by the oxide.

In contrary to the ESD effect which involves very high voltage levels, TDDB can occur under normal bias with reasonable voltage levels. TDDB is primarily due to the presence of weak spots, or dielectric defects within the oxide layer arising from its non-ideal processing.

Some studies have shown that SiO_2 TDDB is a charge injection mechanism, the process of which may be divided into 2 stages – the build-up stage and the runaway stage [**73**]. During the build-up stage, charges invariably get trapped in various parts of the oxide as current flows in the oxide. The trapped charges increase in number with time, forming high electric fields. During the runaway stage, the sum of the electric field built up by charge injection and the electric fields applied to the device exceeds the dielectric breakdown threshold in some of the weakest points of the dielectric. These points start conducting large currents that further heat up the dielectric, which further increases the current flow. This positive feedback loop eventually results in electrical and thermal runaway, destroying the oxide in the end.

The presence of defects in the dielectric greatly reduces the time needed for the transition from the build-up to the runaway stage. These defects actually have the effect of thinning down the oxide where they are located, since they are occupying space that should have been occupied by the dielectric. The effective electric field is higher in these thinned-out areas compared to defect-free areas for any given voltage. This is why it takes a lower voltage and shorter time to break down the dielectric at its defect points.

The DRM [**70**] of the STMicroelectronics 65nm CMOS technology gives maximum voltage guidelines that protect against TDDB. To determine this maximum DC voltages that can be sustained by the circuitry while meeting any given reliability goal, the total on-silicon gate oxide area A_{ox} for all NMOS and PMOS devices, the product lifetime L expressed in hours, and the failure rate F (per 10,000) must be used following the equation (I.12).

$$V_{\max}\left(A_{ox},T_j,L,F\right)=V_0\left(A_{ref},T_j,L_{ref},F_{ref}\right)-m.\log\left(\frac{A_{ox}}{A_{ref}}\right)-n.\log\left(\frac{L}{L_{ref}}\right)+p.\log\left(\frac{F}{F_{ref}}\right) \quad \text{(I.12)}$$

In this equation, V_0 is the reference V_{max} for this technology considering an on-silicon reference area A_{ref}, a reference product lifetime L_{ref} and a reference failure rate F_{ref}. T_j is the junction temperature and m, n and p are empirical constants. The DRM also gives the reference maximum gate voltage V_0 for a 10^6µm² reference area A_{ref}, a 11.4 years product lifetime L_{ref} and a 10 per 10,000 failure rate F_{ref} for a low power LP process NMOS device from 1.71V for a 45°C junction temperature T_j down to 1.54V for a 150°C T_j. PMOS devices with similar parameters exhibit lower V_0 from 1.66V at 45°C T_j down to 1.37V at 150°C T_j.

ii. Hot-Carrier-Injection (HCI)

The hot-carrier-injection effect has to be introduced here in order to explain the progressive deterioration of PA characteristics due to the antenna impedance mismatch. The aim of this explanation in this design & system level PhD thesis is simply to present an overview of this complex physical phenomenon in order to understand its consequences on the PA design.

The term “hot-carriers” refers to either holes or electrons that have gained sufficient kinetic energy after being accelerated by a strong electric field to overcome a potential barrier necessary to break an interface state [**1**]. Because of their high kinetic energy, hot carriers can get injected and trapped in areas of the device where they shouldn't be, forming a space charge that causes the device to degrade or become unstable. Injected carriers which are not trapped become gate current, while carriers flowing into the substrate are detected as substrate current.

In MOS devices, the carrier is injected from the conducting channel in the silicon substrate to the gate dielectric in silicon dioxide (SiO_2). To become "hot" and enter the conduction band of SiO_2, an electron must gain a kinetic energy of 3.3 eV. For holes, the valence band offset in this case dictates they must have a kinetic energy of 4.6 eV.

There are four commonly encountered hot carrier injection mechanisms [**74**]: the drain avalanche hot carrier (DAHC) injection; the channel hot electron (CHE) injection; the substrate hot electron (SHE) injection; and the secondary generated hot electron (SGHE) injection.

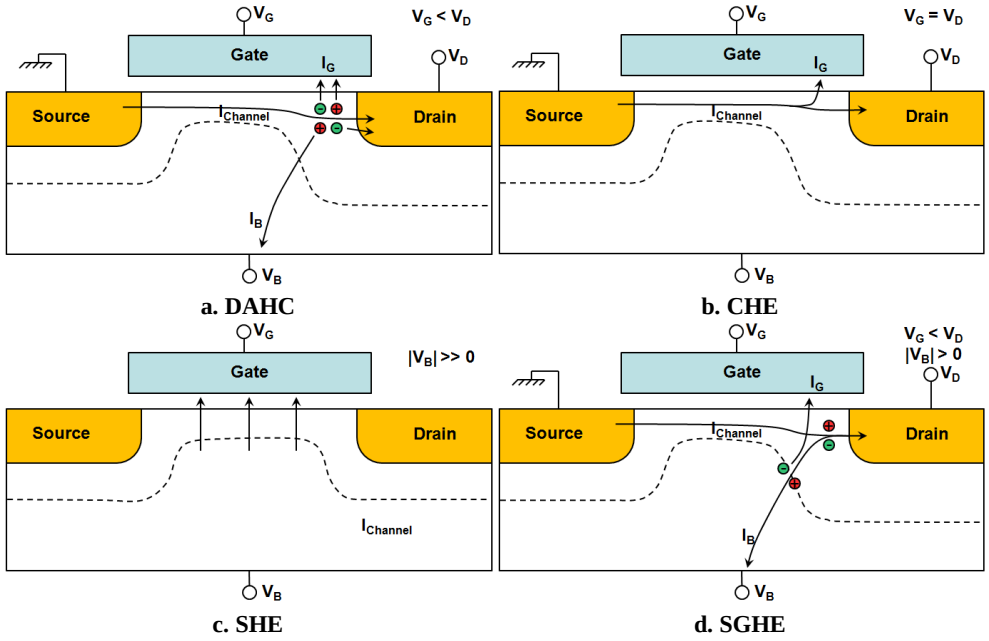


Figure I-26 Hot-carrier injection mechanisms

The drain avalanche hot carrier (DAHC) injection, illustrated in Figure I-26.a, occurs when a high voltage applied at the drain under non-saturated conditions ($V_D > V_G$) results in very high electric fields near the drain, which accelerate channel carriers into the drain's depletion region. The acceleration of the channel carriers causes them to collide with Si lattice atoms, creating dislodged electron-hole (e-h) pairs in the process. Some of those displaced e-h pairs gain enough energy to overcome the electric potential barrier between the silicon substrate and the gate oxide. Under the influence of drain-to-gate field, they get injected into the gate oxide layer where they are sometimes trapped. The hot-carriers trapped at the Si-SiO_2 interface or within the oxide itself form a space charge that increases over time as more charges are trapped.

These trapped charges shift some of the characteristics of the device, such as its threshold voltage V_{th} and its conveyed conductance g_m. Furthermore, the injected carriers that do not get trapped in the gate oxide become gate current and the holes from the e-h pairs generated by impact ionization flow back to the substrate and become substrate current. The DAHC injection is said to produce the worst device degradation in sub-micron CMOS technologies.

The channel hot electron (CHE) injection, illustrated in Figure I-26.b, occurs when both the drain voltage V_D and the gate voltage V_G are significantly higher than the source voltage V_S ($V_D \approx V_G >> V_S$). Because of the high gate voltage, channel carriers – flowing from the source to the drain – are sometimes driven towards the gate oxide even before they reach the drain.

The substrate hot electron (SHE) injection, illustrated in Figure I-26.c, occurs when the substrate bias is very far from the gate voltage ($|V_B| >> 0$). Under this condition, carriers (e or h) are driven by the substrate-to-gate field from the substrate to the Si-SiO_2 interface and some carriers get injected into the gate oxide.

The secondary generated hot electron (SGHE) injection, illustrated in Figure I-26.d, occurs under conditions similar to DAHC ($V_D>V_G$), thus also resulting in impact ionization near the drain. However, in SGHE, the additional substrate's back bias results in a field that tends to drive the hot carriers generated by the secondary carriers – that was likewise created by an earlier incident of impact ionization – toward the surface region, where they further gain kinetic energy to overcome the surface energy barrier.

Hot carrier effects are aggravated in advanced sub-micron CMOS technologies as the operating voltages are not decreased proportionally to the device dimensions, resulting in higher electric fields internal to the device [**74**]. And the higher the electric fields are, the higher the probability of hot-carriers-injection is.

The presence of mobile carriers in the oxides triggers numerous physical damage processes that can drastically change the device characteristics over prolonged periods. The accumulation of damage can eventually cause the circuit to fail as key parameters such as threshold voltage shift due to such damage.

The Negative Bias-Temperature Instability (NBTI) is the physical degradation mechanism that occurs for stressed PMOS transistors. The phenomenon is the equivalent in PMOS to the HCI phenomenon in NMOS. However this effect is not detailed here as linear power amplifiers do not use any PMOS transistors connected to the RF output.

iii. Effects of hot-carrier-injection on CMOS RF amplifiers

Figure I-27 shows the progressive degradation of the main characteristics (threshold voltage V_t, carrier mobility U, transconductance gm, drain current i_d, cut-off frequency f_t and gate capacity C_g) of a nMOSFET under HCI stress [**75**]. In this study, the transistor is a 0.16µm nMOSFET with 50µm channel width and 24 angstroms oxide thickness. The HCI stress condition is $V_{gs}=V_{ds}=2.6V$ and the measured condition is $V_{gs}=0.85V$ and $V_{ds}=1.5V$.

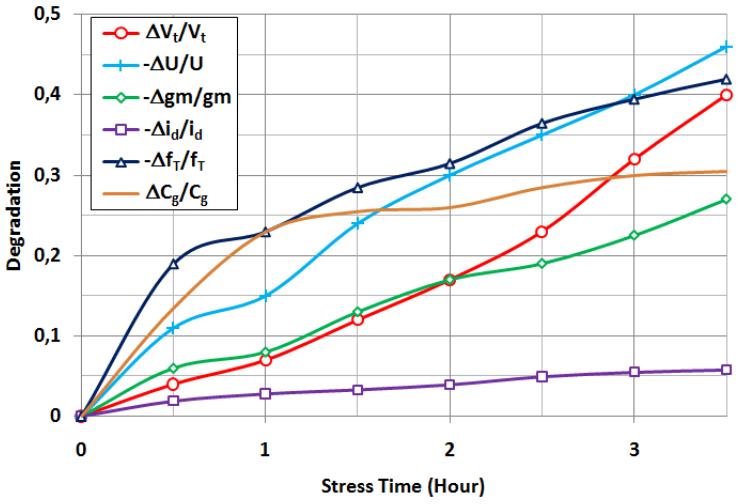


Figure I-27 nMOSFET characteristics degradation under HCI stress

Every parameter is impacted by the HCI stress and suffers from an increase – or a decrease if there is a minus sign in the legend – in the range of 25% to 50% after 3 hours and a half of stress exposition, except the drain current which presents a decrease of about 5% after 3 hours.

Although those extreme stress conditions are very rarely happening during 3 hours without any interruption, this cumulated exposition level can occur during the lifetime of the device. Some aging models are hence developed to characterize the time a semiconductor would be stressed at a given level during its entire life. This can be traduced in terms of lifetime which corresponds to the time

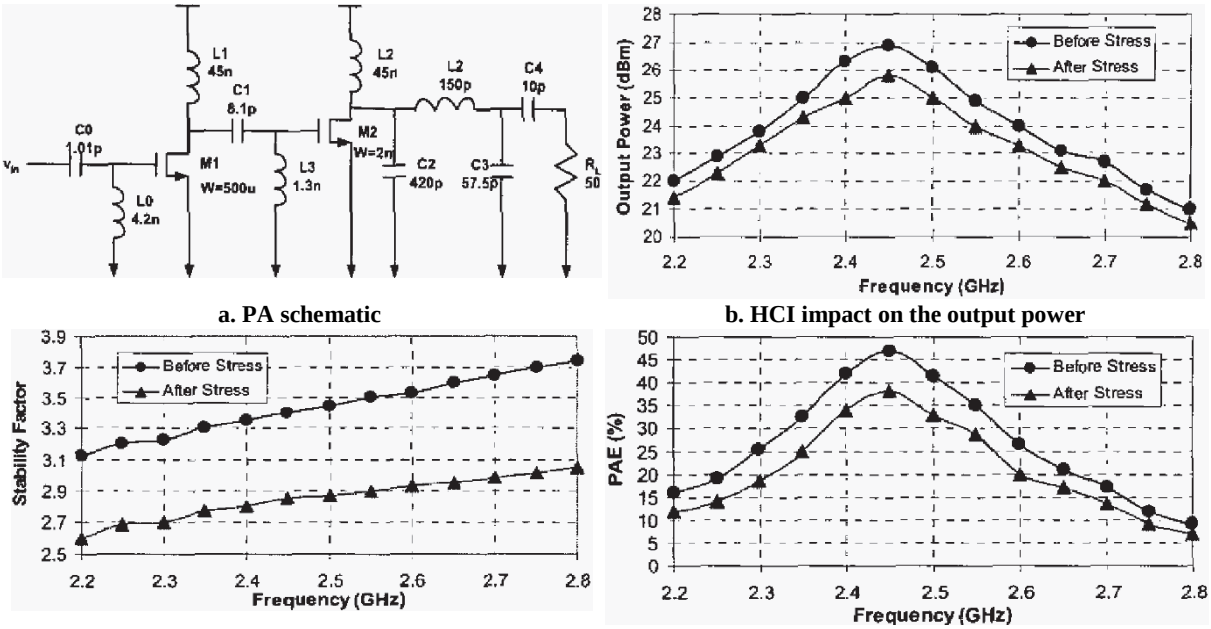
during which the component's characteristics stay better than a certain percentile of its initial characteristics (which means a certain percentile of degradation) [**76**] [**77**].

STMicroelectronics proposed the following general rule to approximate the degradation of device characteristics in the 65nm CMOS technology design rule manual [**70**]:

$$ttf = A.\left(\frac{\Delta}{10\%}\right)^{1/n}.L^{m}.\exp\left(B.\left[\frac{1}{Vds}-\frac{1}{Vd0}\right]\right) \quad \text{(I.13)}$$

where Δ represents the percentage degradation of an electrical parameter (*gm*, V_t…), *L* is the drawn channel length, *Vds* is the drain to source bias, and *Vd0* is typically *VDD+10%* (*VDD* is the nominal supply voltage). *A*, *B*, *n* and *m* are constants determined empirically and detailed in the DRM [**70**]. Considering the voltages *Vds* and *Vd0* expressed in volts and the dimension *L* in microns, the resulting time-to-failure *ttf* is given in years.

[**78**] presents the impact of HCI on a Class AB power amplifier designed for Bluetooth applications at 2.45GHz. The schematic of this PA is illustrated in Figure I-28.a.



a. PA schematic

b. HCI impact on the output power

c. HCI impact on the stability factor

d. HCI impact on the PAE

Figure I-28 Hot-carrier injection effect on an RF power amplifier

The simulated output power, shown in Figure I-28.b, presents a 1.2dB degradation after being stressed – following an aging model not detailed in the publication. In the same conditions, the PAE, shown in Figure I-28.d, decreases from 46% down to 38%. Those PA characteristics degradations also come with a decrease of the stability factor, shown in Figure I-28.c.

To conclude, to ensure a given performance of the RF PA during a given lifetime, the DC and RF voltages must be examined. RF lifetime must be evaluated considering the application and the modulation scheme used. In any case, the cascode topology can be a good candidate to improve reliability at design level [**52**] as the voltage swing on each transistor is reduced, thus reducing the risk of over-voltages.

However the aging model used to ensure a given reliability of the PA does not directly take into consideration the high voltage levels induced by VSWR caused by antenna propagation environment disturbance. Integration of a protection loop on the power stage is hence necessary in order to prevent progressive degradation of the PA performances or simply to prevent PA breakdown.

I.4. Regulation of the antenna VSWR in a 60GHz power amplifier

As introduced along the previous sections of this chapter, a new standard has been written for mass-market applications, which allows transferring audio and video, but also data, by a multi-gigabit per second wireless connection using millimeter-wave frequencies (section I.1). Several transmitters that partially respect this Wireless-HD standard have already been built in III-V technologies but also in silicone technologies (section I.2 and Annex B). However using silicon technologies and specially CMOS technologies presents some limitations. The power amplifiers are actually more sensitive to the antenna impedance mismatch that can be generated by obstructed propagating environment (section I.3).

The aim of this PhD work is hence to design a digital regulation loop for WLAN 60GHz power amplifiers in order to protect and optimize their performance in case of antenna impedance mismatch caused by environmental wave propagation disturbances.

This section first presents the system architecture that has to be implemented, then introduces the concept of power detector used as a VSWR sensor, and finally details the system requirements.

I.4.1. System architecture

Figure I-29 shows a general view of the proposed architecture to detect and regulate the VSWR generated by the antenna environment. A VSWR detector is integrated between the power amplifier and the antenna in order to sense the antenna impedance variations and to give this information to the regulation system. This information is then translated in the digital domain and processed by the digital feedback/decision loop that establishes the necessary compensation that should be applied on the power amplifier and on the matching network to regulate the antenna impedance mismatch.

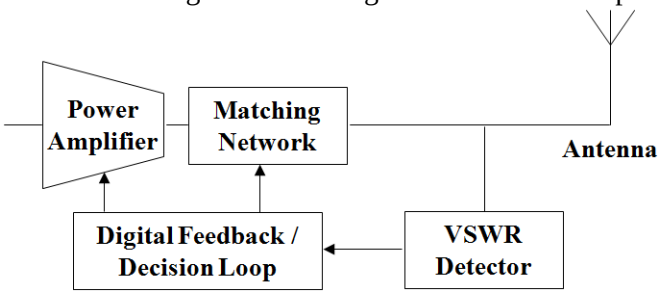


Figure I-29 General architecture of the Antenna VSWR regulated Power Amplifier

The decision loop will be implemented in the digital domain in order to have sufficient computing capability to elaborate a complete regulation strategy. The decision should actually be taken with respect to the information given by the VSWR sensor, but also with respect to some information as the desired power level at the antenna connector that could be given by the digital signal processor (DSP) that generates the baseband signal. Moreover, this regulated system is targeted to be implemented in a standard digital 65nm CMOS process from STMicroelectronics, which presents a huge integration capacity for digital operations.

The architecture presented in Figure I-29 is very general and can be implemented in many different ways as it will be detailed in Chapter IV. Considering actually only the sensor of this regulation loop, several solutions can meet the desired function and generate information that corresponds to the VSWR or the impedance mismatch. As an example, the impedance mismatch can be deduced from power level information simply by doing a comparison between the power that really flows between the PA and the antenna and the power that should theoretically flow at this place if the antenna would present the ideal 50Ω impedance. A power detector can hence act as the VSWR detector as it will be detailed here after.

I.4.2. Integrated power detectors

i. Sensing the power rather than the impedance

The first step to protect Power Amplifiers from the phenomenon presented in section I.3.3 is to detect the antenna impedance mismatch. The measurements of the antenna impedance presented in section I.3.2 have been performed with the help of an external network-analyzer that generates an incident test wave before sensing the reflected wave. This measurement method is well appropriate to sense the impedance of an antenna in a laboratory environment but cannot be integrated in-situ to realize a VSWR regulated power amplifier.

In such an application, the antenna impedance is very difficult to sense as this measure should be performed in-situ, continuously when the transmitter emits some RF power, and without any use of any perturbing test signal. Rather than sensing the impedance, one would prefer sensing the power that flows from the PA to the antenna. By doing a small comparison between the measured power and the power level that should theoretically be observed at the PA output if the antenna had presented a perfect 50Ω impedance, one can actually deduce the impedance mismatch and appropriately regulate the system.

Moreover, sensing directly the power can be difficult and designers would prefer to deduce the power information from a current or from a voltage measure which both are much easier to implement. The power is actually directly proportional to the voltage squared; the ratio between the power and the voltage squared being the reference impedance Z_0 as written in the equation (I.14) deduced from well-known Joule's and Ohm's laws.

$$P = V.I = \frac{V^2}{Z_0} = Z_0.I^2 \tag{I.14}$$

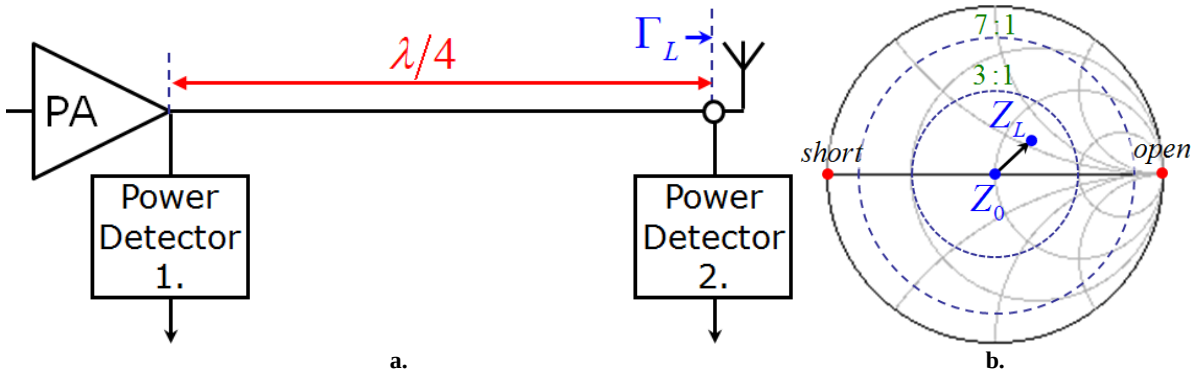
In sub-micron CMOS technology, the main limitation is the low breakdown voltage [**79**]. Thus, using a CMOS technology, the output voltage is the parameter to be detected. Hence the power information is deduced from the voltage information simply by squaring the voltage. The techniques to perform this operation are detailed in Chapter II.

ii. The need of two power detectors

As introduced in section I.3.1, the antenna impedance mismatch generates a standing wave that is characterized by resonance points and nodes where the amplitude of the standing wave is maximal and minimal respectively. Placing a unique power sensor could hence generate an error as it can be located either at a resonance point, at a node, or in an intermediate position. The measured power would hence be different from the true power flowing in the line as one could not determine if the measured power corresponds only to a progressive wave – that we want to measure – or to a combination of the progressive wave and the standing wave.

At this time, the theoretical approach introduced in section I.3.1 can be developed still using Matlab. Considering a 60GHz sinewave incident voltage progressive wave V_i with 1V amplitude and 0° phase applied at one end of a λ/4 length T-line of Z_0 characteristic impedance, a reflected voltage progressive wave V_r will appear in the T-line depending of the load impedance Z_L located at the other end of the T-line. Those two waves will combine together thus forming one progressive wave and one standing wave as explained in section I.3.1.

In the present study, we consider two power detectors located in phase opposition which means the two detectors are located at both ends of the *λ/4* length T-line as shown in Figure I-30.a. By convention the detector on the PA side is called detector number 1 and the detector on the antenna side is called detector number 2 thus following the natural space propagation of the useful incident progressive wave.



a. b.

Figure I-30 Location of the two power detectors (a.); Smith chart described by the antenna impedance (b.)

Moreover in the present study, the load impedance Z_L covers all the possible values in magnitude and in phase. This means the reflection coefficient Γ_L covers all the values of magnitude lower than 1 and of phase include between 0 and 360°. This reflection coefficient variation corresponds to the whole Smith chart which is a well-known diagram used by radio-communication engineers for solving problems with transmission lines and matching circuits. The Smith chart is plotted on the complex reflection coefficient plane in two dimensions [**1**] and is constituted by a certain number of constant resistance (real part) and constant reactance (imaginary part) load impedance Z_L lines as shown in Figure I-30.b. The Smith chart is hence a graphical representation of the conversion between the load impedance and the reflection coefficient Γ_L following the equation (I.7). The VSWR can also be represented on the Smith chart by circles centered on the origin ($\Gamma_L=0$ or the equivalent in terms of impedance $Z_L=Z_0$) as following the equation (I.11), the VSWR only depends of the magnitude of the reflection coefficient Γ_L. Two circles have been represented in Figure I-30.b that correspond to 3:1 VSWR for the dotted line and to 7:1 VSWR for the dashed line.

By the way, the incident and reflected waves are combined together and form a single voltage at each time, for each location of the T-line and for each value of the T-line load impedance. This voltage is then squared and divided by the reference 50Ω impedance Z_0 thus resulting in a power information still for each (time, space, impedance) trinomial. This instantaneous power information is averaged on a full time period and considered at the two detector locations (at λ/4 from the antenna and at the antenna connector). This operation generates the averaged power defined for the two detectors and for each value of antenna impedance.

The result of this theoretical approach is plotted in Figure I-31. The diagrams a. and b. represent on a Smith chart the averaged power detected by each of the two power detectors with respect to the load impedance presented at the end of the T-line. Those two diagrams are symmetrical with respect to the imaginary reflection coefficient Γ_L axis (the vertical one). The maximum of the first detector, obtained for a short circuit, corresponds to the minimum of the second detector; and a minimum of the first detector, obtained for an open circuit, corresponds to the maximum of the second detector.

Each value of the antenna impedance – i.e. each point of the Smith chart – generates hence two complementary values on the two power detectors. Those two values can be combined together by simple average and difference mathematical operations to generate data which are more significant and which can be much easier used by the regulation loop. The average of the two detected powers is actually proportional to the magnitude of the reflection coefficient Γ_L as shown in Figure I-31.c. On the other hand, the difference between the two detected powers is proportional to the real part of the reflection coefficient Γ_L as shown in Figure I-31.d. Knowing its magnitude and its real part, the reflection coefficient can be determined with only an uncertainty on the sign of its imaginary part.

However it has to be noticed that the theoretical output power level at the antenna connector has to be known in order to determine the reflection coefficient of the antenna. Otherwise knowing the reflection coefficient is necessary to determine the true power level at the antenna connector.

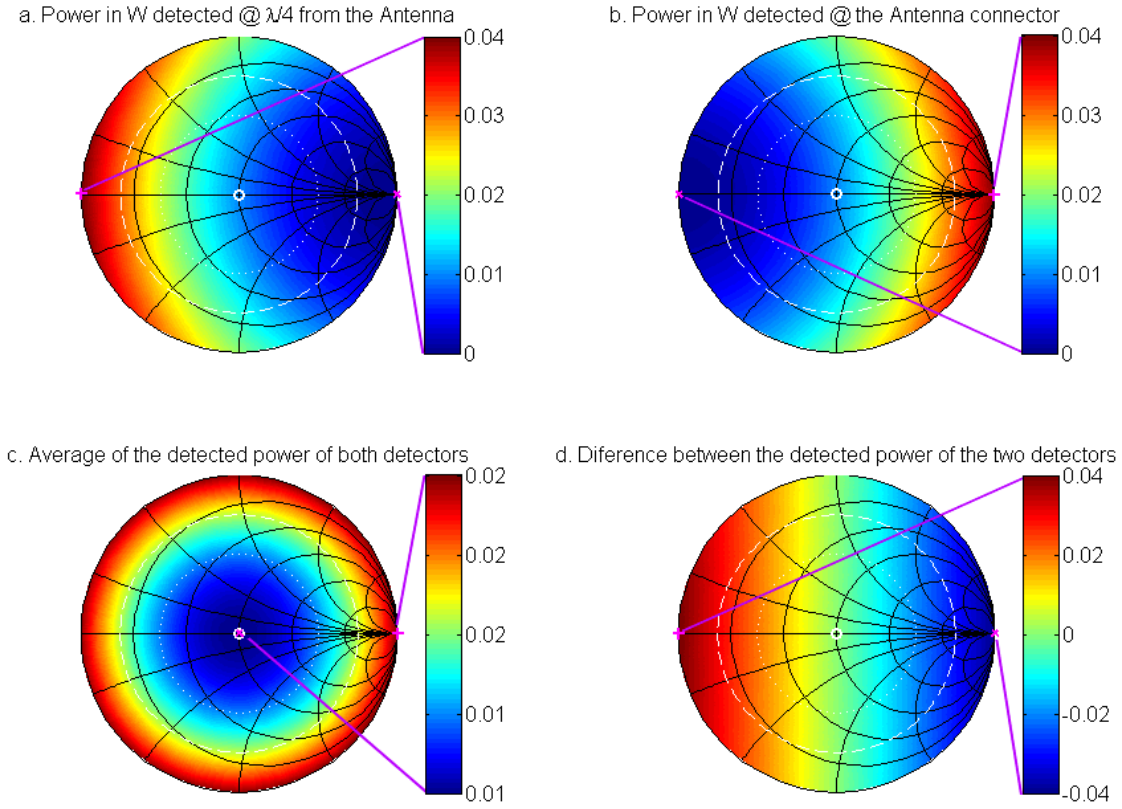


Figure I-31 Theoretical load-pull simulation of two detectors sensing the power in a λ/4 T-line

iii. Frequency and pad capacitance limitations

The previous study has been performed for a 60GHz sinewave signal. However the Wireless HD standard defines a useful frequency bandwidth between 55GHz and 65GHz (see section I.1.3.i). The λ/4 distance between the two power detectors which was calculated for a 60GHz signal is hence no more equal to λ/4 for a 55GHz signal or for a 65GHz signal. The amplitude limitation – equivalent to the error between the 55GHz and the 60GHz signals – is given by a simple calculus on the space component of the standing wave expressed at the equation (I.10), considering the detector at the axis origin (x=0) and no phase shift induced by the load impedance. This calculus is presented at the equation (I.15) and highlights the high 13.05% error level induced by the λ/4 difference between the center frequency at 60GHz and the actual frequency of 55GHz. Following the cosine function, a 65GHz signal would generate the same error level but with the opposite sign.

$$Error_{55GHz} = \cos\left(\frac{2\pi}{\lambda_{55GHz}}.\frac{\lambda_{60GHz}}{4}\right) = \cos\left(\frac{\pi}{2}.\frac{55GHz}{60GHz}\right) \approx 13.05\% \qquad \text{(I.15)}$$

Figure I-32 shows the simulation results obtained with a 55GHz sinewave signal applied at the input of the λ/4 T-line designed for 60GHz signals. The diagram a. presents the power detected on the first detector located at λ/4 from the antenna connector, and can hence be compared to the one of Figure I-31.a. It appears the diagram obtained for a 55GHz signal (Figure I-32.a) is the image of the diagram obtained for a 60GHz signal (Figure I-31.a) subjected to a certain rotation on the Smith chart. This rotation is directly induced by the fact that the detector is not located at λ/4 for a 55GHz signal but for a 60GHz signal. The frequency does not affect the second detector which hence still corresponds to Figure I-31.b.

Let us now consider the average power on both detectors which is shown in Figure I-32.b (to be compared with Figure I-31.c). The iso-value circles are no more centered on the origin of the Smith chart thus generating a huge difficulty to interpret the detected power in terms of reflection coefficient magnitude.

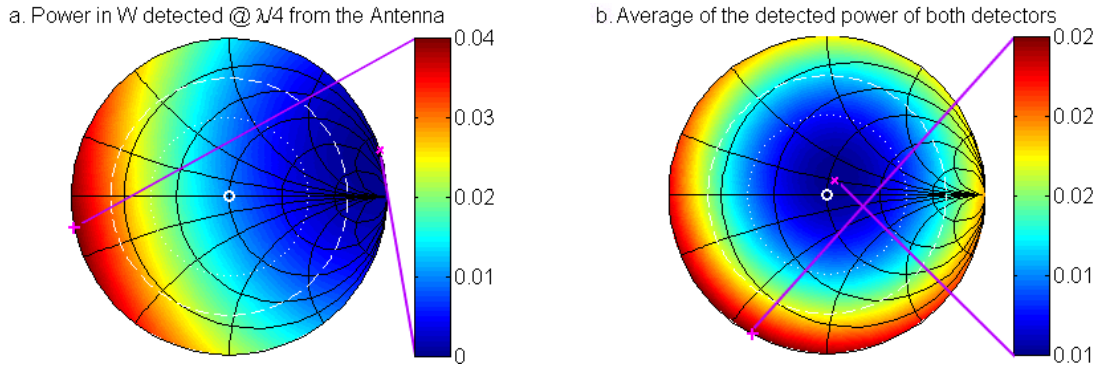


Figure I-32 Power in the T-line for the first detector (a.) and average of both power (b.) considering a 55GHz signal

Moreover, only sinewave signals have been considered here. But the targeted modulation for the Wireless HD standard is a complex OFDM as described in section I.1.3.ii. This should results in more complex diagrams difficult to interpret correctly.

Another limitation occurs when considering a more realistic situation where the antenna does not ideally match to 50Ω but is connected to the power amplifier through a pad that presents a small 30fF capacitance in parallel which is lower than the actual value in 65nm CMOS technology. Figure I-33 shows the theoretical simulation results including this additional pad capacitance in parallel to the load impedance. The diagram disposition is similar to the one of Figure I-31.

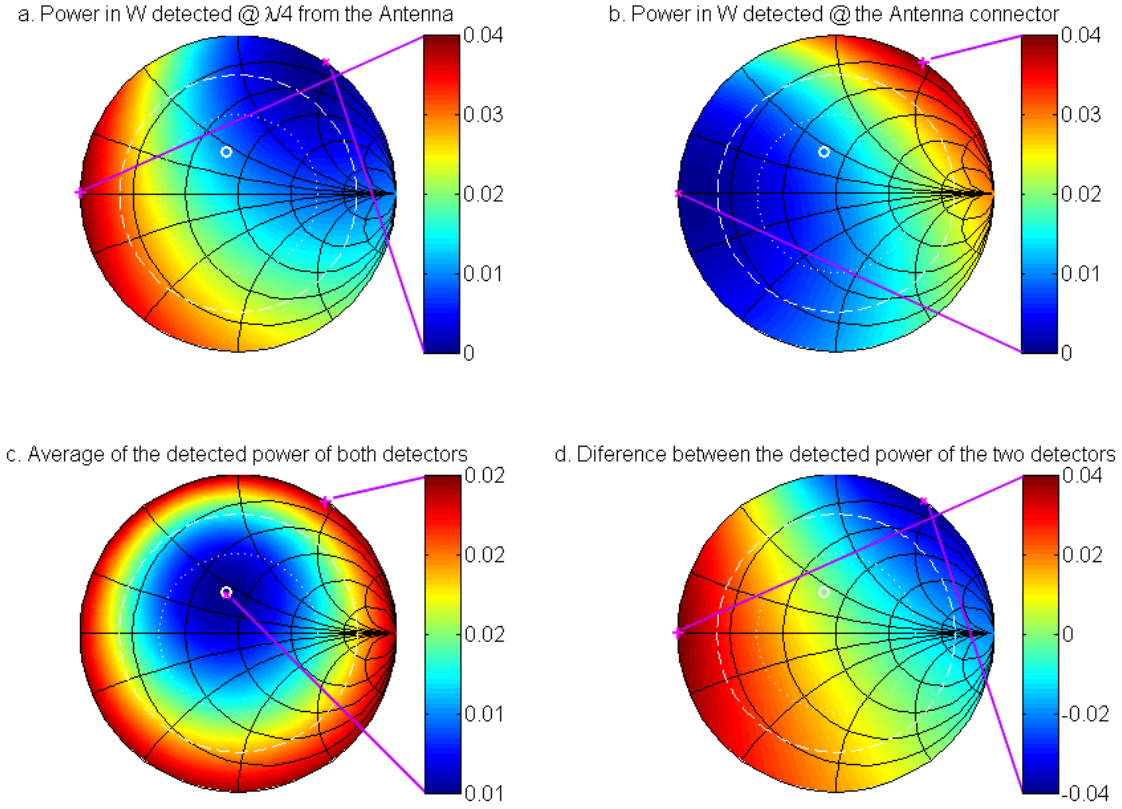


Figure I-33 Theoretical simulation including an additional 30fF capacitance in parallel to the load impedance

Both detected power diagrams (a. and b.) have suffered from a certain rotation but also from a certain offset as the diagram centers are moved as can be seen by observing the maximum and minimum locations (respectively the "+" and the "x" in magenta) in Figure I-33. In fact, the additional parallel capacitance has to be compensated on the load impedance to match the 50Ω characteristic impedance of the T-line. The load impedance that does not generate any standing wave is hence given

by the conjugate complex of the capacitive impedance in parallel of the targeted 50Ω load impedance as written in the equation (I.16). This particular point is represented by the small white circle in Figure I-33.

$$\left(Z_L\right)_{\text{no standing wave}} = Z_0 \,//\left(\frac{1}{j.C.\omega}\right)^* = \frac{-Z_0 \big/ j.C.\omega}{Z_0 - 1 \big/ j.C.\omega} \tag{I.16}$$

The computation on the two detected powers suffers from the same transformation as can be seen on the diagrams c. and d. of Figure I-33. Building a regulation loop on this information becomes hence very difficult. To conclude on this phenomenon, the theoretical approach developed in section I.4.2.ii can be quite difficult to implement in a circuit as every parasitic capacitive or inductive effect on the transmission line has to be taken into consideration as it will impacts the global load impedance seen by the T-line.

I.4.3. System requirements

Considering the measurements of section I.3.2, we have decided for this study to fix the following system requirements. First, the system should be able to protect itself from up to 7:1 VSWR which correspond to extreme conditions where an obstacle is placed at less than 1cm just in front of the antenna. Secondly, the system should be able to regulate itself from up to 3:1 VSWR which correspond to a situation that can occur routinely. The end-user actually wants his Wireless-HD equipment to works fine even if its environment is quite reasonably perturbed. Those two limits, 3:1 and 7:1 VSWR, correspond to the white dotted and dashed circles respectively on the diagrams of Figure I-31 and of Figure I-33.

The maximum VSWR to be detected being fixed to 7:1, once can calculate the minimal detection range required on the power detectors. The first step is to convert the VSWR in terms of load impedance. As written in the equation (I.17), 7:1 VSWR corresponds to an impedance ratio of 7 between the load impedance Z_L and the reference impedance Z_0 or inversely.

$$7:1 VSWR \Rightarrow \left|Z_L\right| = 7.\left|Z_0\right| \; or \; \left|Z_0\right| = 7.\left|Z_L\right| \tag{I.17}$$

This impedance ratio can then be expressed in terms of power ratio considering the power detection technique introduced in section I.4.2.i based on the voltage squared. The detected power P_{Z_0} considering a Z_0 load impedance and the true power level P_{Z_L} flowing in the real Z_L load impedance are linked together by the impedance ratio as detailed in the equation (I.18).

$$\frac{P_{Z_0}}{P_{Z_L}} = \frac{V_{peak}{}^2 \big/ \left(2.Z_0\right)}{V_{peak}{}^2 \big/ \left(2.Z_L\right)} = \frac{Z_L}{Z_0} \tag{I.18}$$

Finally expressed on a logarithmic scale (the power are hence expressed in dB), the power ratio becomes a difference between the two power P_{Z_0} and P_{Z_L} equals to the impedance ratio expressed on a logarithmic scale as written in the equation (I.19).

$$\left(P_{Z_0}\right)_{dB} = \left(P_{Z_L}\right)_{dB} - 20.\log\left(Z_L/Z_0\right) \tag{I.19}$$

A 7:1 VSWR antenna impedance mismatch is hence requesting a 16.9dB linear detection range, for a constant PA output power level. This output power level can then vary in a certain range given by the standards specification in order to reduce the power consumption when the receiver and the transmitter are very closed together thus resulting in a very advantageous situation. The power detector used in this regulation system has hence to provide a high detection range to fulfill the requirements in terms of VSWR effect and in terms of transmitter output power capability.

Chapter conclusion

This first chapter has presented the global context of this PhD study.

First of all, the need for a new high data rate low distance wireless communication standard has been presented through an introduction on the possible applications. Some characteristics of the Wireless-HD, this new wireless standard have then been listed after having exposed the many advantages of the unlicensed 60GHz frequency band.

In a second time, we have focused on the transmitter architectures that could fulfill the Wireless-HD requirements. Still focusing on a specific RF block included in all transmitters, we have presented the power amplifier which is one of the most difficult blocks to design at those millimeter-wave frequencies in CMOS technologies. After having overviewed the millimeter-wave PAs state-of-the-art, we have presented the PPA used in our system (detailed in Chapter IV). This CMOS65 PPA exhibits a 6.5dBm output power at the 1dB compression gain, a 16.4dB gain and a 13.2% maximum PAE.

The antenna impedance variations resulting of obstructed wave propagation environment and their impacts on the power amplifiers have then been investigated. A theoretical approach of the formation of the standing waves has hence been developed as an introduction to this phenomenon. Some antenna impedance mismatch measurements at 60GHz have then been presented in order to quantify the VSWR that can really be observed in millimeter-wave circuits. The dramatic consequences of such VSWR on the power amplifiers have been listed with a necessary study of the physical phenomenon that occurs in MOS devices.

Finally, we have introduced the architecture of a regulated system that could protect the power amplifier from the damages caused by an antenna impedance mismatch induced by an obstructed wave propagation environment. The theoretical approach previously introduced has also been completed to come to the conclusion that simple power detectors could be used as the VSWR detector but with some limitations still remaining. Some system requirements have finally been fixed. The system should hence be able to protect itself from a 7:1 VSWR and to regulate up to 3:1 VSWR.

The second chapter details the power detector that has been designed to perform the VSWR detection. The third chapter presents the Analog-to-Digital Converter with logarithmic characteristic which is used to convert the analog signal from the VSWR detector to the digital domain. The fourth chapter investigates the implementation of a VSWR regulated power amplifier at the system level.

Chapter references

[1] Wikipedia, The free encyclopedia. [Online]. http://en.wikipedia.org

[2] A. Seyedi, "Draft tg3c system requirements," Project IEEE P802.15 15-05-0353-08-003c, Dec. 2006. [Online]. http://www.ieee802.org/15/pub

[3] A. Sadri, "802.15.3c Usage model document (UMD), Draft," Project IEEE P802.15 15-06-0055-15-003c, Jan. 2007. [Online]. http://www.ieee802.org/15/pub

[4] (2010, Apr.) Rowe Network, 60GHz Backhaul products. [Online]. http://www.rowewireless.com/xcart/home.php?cat=311

[5] Federal Communications Commission, "CFR Title 47 Part 15.255 - Operation within the band 57–64 GHz.," United States Legislative Document, Dec. 2005. [Online]. http://www.access.gpo.gov

[6] "RSS-210 - Low-power Licence-exempt Radiocommunication Devices (All Frequency Bands): Category I Equipment," Canadian Legislative Document, Sep. 2005. [Online]. http://strategis.ic.gc.ca/epic/internet/insmt-gst.nsf/en/sf01320e.html

[7] Electronics and Telecommunications Research Institute (ETRI), "Notice of Korean 60 GHz Unlicensed Band Allocation," Project IEEE P802.15 15-06-0330-00-003c, Jul. 2006. [Online]. http://www.ieee802.org/15/pub/

[8] Australian Communications and Media Authority, "Radiocommunications (Low Interference Potential Devices) Class Licence 2000," Australian Legislative Document, Jul. 2006. [Online]. http://www.comlaw.gov.au/ComLaw/Legislation/

[9] Australian Communications and Media Authority, "Proposed Variation to the Radiocommunications (Low Interference Potential Devices) Class Licence 2000 and Revocation of the Radiocommunications (Infrared Devices) Class Licence 2002," Australian Legislative Document, Aug. 2008. [Online]. http://www.comlaw.gov.au/ComLaw/Legislation/

[10] Association of Radio Industries and Businesses (ARIB), "Wireless Local Area Networks and Fixed Wireless Access," Japanese Legislation Document, May 2004. [Online]. http://www.ece.utexas.edu/~wireless/General/60ghz.php

[11] European Radiocommunications Office, "The European Table of Frequency Allocations and Utilisations covering the Frequency range 9 kHz to 275 GHz," European Legislative Document, May 2004. [Online]. http://www.ero.dk/doc98/official/pdf/Rep025.pdf

[12] M. Marcus and B. Pattan, "Millimeter Wave Propagation; Spectrum Management Implications," *IEEE Microwave Magazine*, Jun. 2005.

[13] "WGMGWS(07)05 - Preliminary Draft ECC Report on MGWS-rev6Feb2007," Feb. 2007.

[14] (2009, Jan.) Wireless HD Consortium. [Online]. http://www.wirelesshd.org

[15] Wireless HD Consortium, "Wireless HD specification, revision 1.0," Jan. 2008.

[16] (2010, Apr.) WiGig, Wireless Gigabit Alliance. [Online]. http://wirelessgigabitalliance.org

[17] (2010, Apr.) ECMA Internationnal, Standard ECMA-387. [Online]. http://www.ecma-international.org/publications/standards/Ecma-387.htm

[18] H. Harada and I. Lakkis, "Merged proposal: New PHY Layer and Enhancement of MAC for mmWave System Proposal," Project IEEE P802.15 15-07-0934-01-003c, Nov. 2007. [Online]. http://www.ieee802.org/15/pub/

[19] A. Frappé, "All-digital RF signal generation using DS modulation for mobile communication terminals," Ph.D. Thesis, Université des Sciences et Techniques de Lille, Lille, France, Dec. 2007.

[20] C. H. Doan, S. Emami, D. A. Sobel, A. M. Niknejad, and R. W. Brodersen, "Design Considerations for 60 GHz CMOS Radios," *IEEE Communications Magazine*, vol. 42, no. 12, pp. 132-140, Dec. 2004.

[21] (2010, Feb.) Iternational Technology Roadmap for Semiconductors (ITRS). [Online]. http://www.itrs.net

[22] S. W. Chen, P. M. Smith, S. M. J. Liu, W. F. Kopp, and T. J. Rogers, "A 60-GHz High Efficiency Monolithic Power Amplifier Using 0.1-µm PHEMT's," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 6, pp. 201-203, Jun. 1995.

[23] M. Han, et al., "V-Band CPW Balanced Medium Power Amplifier for 60 GHz Wireless LAN application," in *IEEE 13th Asia-Pacific Microwave Conference (APMC) Proceedings*, vol. 2, Suzhou, China, Dec. 2005.

[24] O. S. A. Tang, et al., "A 560 mW, 21% Power-Added Efficiency V-band MMIC Power Amplifier," in *IEEE*

18th Annual Gallium Arsenide Integrated Circuit (GaAs IC 1996) Symposium, Technical Digest, Orlando, FL, USA, Nov. 1996, pp. 115-118.

[25] C. Kärnfelt, P. Hallbjörner, H. Zirath, and A. Alping, "High Gain Active Microstrip Antenna for 60-GHz WLAN-WPAN Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 6, pp. 2593-2603, Jun. 2006.

[26] M. Käirkkainen, M. Varonen, J. Riska, P. Kangaslahti, and V. Porra, "A Set of Integrated Circuits for 60 GHz Radio Front-End," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, vol. 2, Seattle, WA, USA, Jun. 2002, pp. 1273-1276.

[27] M. Varonen, M. Käirkkainen, J. Riska, P. Kangaslahti, and V. Porra, "Power Amplifiers for 60 GHz WLAN Applications," in *IEEE Radio and Wireless Conference (RAWCON 2002)*, Boston, MA, USA, Aug. 2002, pp. 245-248.

[28] Y. Mimino, et al., "A 60 GHz millimeter-wave MMIC chipset for broadband wireless access system front-end," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, vol. 3, Seattle, WA, USA, Jun. 2002, pp. 1721-1724.

[29] R. Lai, et al., "A high efficiency 0.15 µm 2-mil thick InGaAs/AlGaAs/GaAs V-band power HEMT MMIC," in *IEEE 18th Annual Gallium Arsenide Integrated Circuit (GaAs IC 1996) Symposium, Technical Digest*, Orlando, FL, USA, Nov. 1996, pp. 225-227.

[30] M. Varonen, M. Käirkkainen, P. Kangaslahti, and V. Porra, "Integrated Power Amplifier for 60 GHz Wireless Applications," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, vol. 2, Philadelphia, PA, USA, Jun. 2003, pp. 915-918.

[31] M. Abbasi, H. Zirath, and I. Angelov, "Q-, V-, and W-Band Power Amplifiers Utilizing Coupled Lines for Impedance Matching," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, Atlanta, GA, USA, Jun. 2008, pp. 863-866.

[32] W. M. T. Kong, et al., "Very high efficiency V-band power InP HEMT MMICs," *IEEE Electron Device Letters*, vol. 21, no. 11, pp. 521-523, Nov. 2000.

[33] A. O. S. Tang, et al., "Design and Fabrication of a Wideband 56- to 63-GHz Monolithic Power Amplifier With Very High Power-Added Efficiency," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1298-1306, Sep. 2000.

[34] Y. C. Chen, et al., "A Single Chip 1-W InP HEMT V-Band Module," in *IEEE 21st Annual Gallium Arsenide Integrated Circuit (GaAs IC 1999) Symposium*, Monterey, CA, USA, Oct. 1999, pp. 149-152.

[35] D. L. Ingram, et al., "A 427 mW, 20% Compact W-Band InP HEMT MMIC Power Amplifier," in *IEEE Radio Frequency Integrated Circuits (RFIC 1999) Symposium, Digest of Papers*, Anaheim, CA, USA, Jun. 1999, pp. 95-98.

[36] B. A. Floyd, et al., "SiGe Bipolar Transceiver Circuits Operating at 60 GHz," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 156-167, Jan. 2005.

[37] S. T. Nicolson, et al., "A Low-Voltage 77-GHz Automotive Radar Chipset," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, Honolulu, HI, USA, Jun. 2007, pp. 487-490.

[38] A. Komijani and A. Hajimiri, "A Wideband 77 GHz, 17.5 dBm Fully Integrated Power Amplifier in Silicon," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1749-1756, Aug. 2006.

[39] A. Valdes-Garcia, S. Reynolds, and U. R. Pfeiffer, "A 60GHz Class-E power amplifier in SiGe," in *IEEE Asian Solid-State Circuits Conference (ASSCC 2006)*, Piscataway, NJ, USA, Nov. 2006, pp. 199-202.

[40] U. R. Pfeiffer, "A 20dBm Fully-Integrated 60GHz SiGe Power Amplifier with Automatic Level Control," in *IEEE Proceedings of the 32nd European Solid-State Circuits Conference (ESSCIRC 2006)*, Montreux, Switzerland, Sep. 2006, pp. 356-359.

[41] S. K. Reynolds, et al., "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2820-2831, Dec. 2006.

[42] U. R. Pfeiffer, D. Goren, B. A. Floyd, and S. K. Reynolds, "SiGe Transformer Matched Power Amplifier for Operation at Millimeter-Wave Frequencies," in *IEEE Proceedings of the 31st European Solid-State Circuits Conference (ESSCIRC 2005)*, Grenoble, France, Sep. 2005, pp. 141-144.

[43] U. R. Pfeiffer, S. K. Reynolds, and B. A. Floyd, "A 77 GHz SiGe Power Amplifier for Potential Applications in Automotive Radar Systems," in *IEEE Radio Frequency Integrated Circuits (RFIC 2004) Symposium*, Fort Worth, TX, USA, Jun. 2004, pp. 91-94.

[44] E. Afshari, H. Bhat, X. Li, and A. Hajimiri, "Electrical Funnel: A Broadband Signal Combining Method," in *IEEE International Solid-State Circuits Conference (ISSCC 2006), Digest of Technical Papers*, San Francisco, CA, USA, Feb. 2006, pp. 751-760.

[45] U. R. Pfeiffer and D. Goren, "A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 857-865, May 2007.

[46] C. Wang, et al., "A 60 GHz Transmitter with Integrated Antenna in 0.18 um SiGe BiCMOS Technology," in *IEEE International Solid-State Circuits Conference (ISSCC 2006), Digest of Technical Papers*, vol. 10.4, San Francisco, CA, USA, 2006.

[47] H. Li, H. M. Rein, T. Suttorp, and J. Böck, "Fully Integrated SiGe VCOs With Powerful Output Buffer For 77 GHz Automotive Radar Systems And Applications Around 100 GHz," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1650-1658, Oct. 2004.

[48] M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, "Millimeter-Wave Amplifiers in 65-nm CMOS," in *IEEE Proceedings of the 33rd European Solid-State Circuits Conference (ESSCIRC 2007)*, Munich, Germany, Sep. 2007, pp. 280-283.

[49] S. Aloui, E. Kerhervé, D. Belot, and R. Plana, "A 60GHz, 13dBm Fully Integrated 65nm RF-CMOS Power Amplifier," in *Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference (NEWCAS-TAISA 2008)*, Montréal, Canada, Jun. 2008, pp. 93-96.

[50] W. L. Chan, J. R. Long, M. Spirito, and J. J. Pekarik, "A 60GHz-band 1V 11.5dBm power amplifier with 11% PAE in 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2009), Digest of Technical Papers*, vol. 22.4, San Francisco, CA, USA, Feb. 2009, pp. 380-381.

[51] J. W. Lai and A. Valdes-Garcia, "A 1V 17.9dBm 60GHz power amplifier in standard 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2010), Digest of Technical Papers*, vol. 23.6, San Francisco, CA, USA, Feb. 2010, pp. 424-425.

[52] B. Martineau, V. Knopik, A. Siligaris, F. Gianasello, and D. Belot, "A 53-to-68GHz 18dBm power amplifier with an 8-way combiner in standard 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2010), Digest of Technical Papers*, vol. 23.8, San Francisco, CA, USA, Feb. 2010, pp. 428-429.

[53] A. Valdes-Garcia, S. Reynolds, and J. O. Plouchart, "60 GHz Transmitter Circuits in 65nm CMOS," in *IEEE Radio Frequency Integrated Circuits (RFIC 2008) Symposium*, Atlanta, GA, USA, Jun. 2008, pp. 641-644.

[54] T. Yao, M. Gordon, K. Yau, M. T. Yang, and S. P. Voinigescu, "60-GHz PA and LNA in 90-nm RF-CMOS," in *IEEE Radio Frequency Integrated Circuits (RFIC 2006) Symposium*, San Francisco, CA, USA, Jun. 2006, pp. 147-150.

[55] D. Chowdhury, P. Reynaert, and A. M. Niknejad, "A 60-GHz 1-Volt +12.3dBm Transformer-Coupled Wideband Power Amplifier in 90nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, vol. 31.2, San Francisco, CA, USA, Feb. 2008.

[56] T. Suzuki, Y. Kawano, M. Sato, T. Hirose, and K. Joshin, "60GHz and 77GHz Power Amplifiers in Standard 90nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, vol. 31.3, San Francisco, CA, USA, Feb. 2008.

[57] M. Tanomura, et al., "TX and RX Front-Ends for 60GHz Band in 90nm Standard Bulk CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, vol. 31.1, San Francisco, CA, USA, Feb. 2008.

[58] T. LaRocca and M. C. F. Chang, "60GHz CMOS Differential and Transformer-Coupled Power Amplifier for Compact Design," in *IEEE Radio Frequency Integrated Circuits (RFIC 2008) Symposium*, Atlanta, GA, USA, Jun. 2008, pp. 65-68.

[59] M. Bohsali and A. M. Niknejad, "Current combining 60GHz CMOS power amplifiers," in *IEEE Radio Frequency Integrated Circuits (RFIC 2009) Symposium*, Boston, MA, USA, Jun. 2009, pp. 31-34.

[60] D. Dawn, et al., "60GHz CMOS power amplifier with 20-dB-gain and 12dBm Psat," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, Boston, MA, USA, Jun. 2009, pp. 537-540.

[61] Y. N. Jen, J. H. Tsai, T. W. Huang, and H. Wang, "Design and analysis of a 55-71-GHz compact and broadband distributed active transformer power amplifier in 90-nm CMOS Process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 7, pp. 1637-1646, Jul. 2009.

[62] C. Y. Law and A. V. Pham, "A high-gain 60GHz power amplifier with 20dBm output power in 90nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2010), Digest of Technical Papers*, vol. 23.7, San Francisco, CA, USA, Feb. 2010, pp. 426-427.

[63] S. Pinel, et al., "A 90nm CMOS 60GHz Radio," in *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, vol. 6.8, San Francisco, CA, USA, 2008.

[64] B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad, "Low-Power mm-Wave Components up to 104GHz in 90nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*, vol. 10.7, San Francisco, CA, USA, Feb. 2007, pp. 200-203.

[65] M. D. Tsai, H. Wang, and J. F. Kuan, "A 70GHz Cascaded Multi-Stage Distributed Amplifier in 90nm CMOS Technology," in *IEEE International Solid-State Circuits Conference (ISSCC 2005), Digest of Technical Papers*, vol. 21.7, San Francisco, CA, USA, Feb. 2005.

[66] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-Wave CMOS Design," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 144-155, Jan. 2005.

[67] B. Wicks, E. Skafidas, and R. Evans, "A 60-GHz Fully-Integrated Doherty Power Amplifier Based on 0.13-µm CMOS Process," in *IEEE Radio Frequency Integrated Circuits (RFIC 2008) Symposium*, Atlanta, GA, USA, Jun. 2008, pp. 69-72.

[68] A. Siligaris, et al., "A 60GHz power amplifier with 14.5dBm saturation power and 25% peak PAE in CMOS 65nm SOI," in *IEEE Proceedings of the 35th European Solid-State Circuits Conference (ESSCIRC 2009)*, Athens, Greece, Sep. 2009, pp. 168-171.

[69] H. E. King and J. L. Wong, "Effects of a Human Body on a Dipole Antenna at 450 and 900 MHz," *IEEE Transactions on Antennas and Propagation*, pp. 376-379, May 1977.

[70] "CMOS 065 Design Rule Manual 65nm Bulk CMOS Process," STMicroelectronics Design Rule Manual 7683821 revision E, Oct. 2006.

[71] P. Roussel, R. Degraeve, G. Van den bosch, B. Kaczer, and G. Groeseneken, "Accurate and robust noise-based trigger algorithm for soft breakdown detection in ultra thin oxides," in *IEEE Proceedings of the 39th Annual International Reliability Physics Symposium (IRPS)*, Orlando, USA, FL, May 2001, pp. 386-392.

[72] E. Miranda and J. Suné, "Electron transport through broken down ultra-thin SiO2 layers in MOS devices," *Microelectronics Reliability*, vol. 44, no. 1, pp. 1-23, Jan. 2004.

[73] (2010, Apr.) Silicon Far-East. [Online]. http://www.siliconfareast.com/oxidebreakdown.htm

[74] (2010, Apr.) Silicon Far-East. [Online]. http://www.siliconfareast.com/hotcarriers.htm

[75] E. Xiao, J. S. Yuann, and H. Yang, "CMOS RF and DC reliability subject to hot carrier stress and oxide soft breakdown," *IEEE Transactions on Device and Materials Reliability*, vol. 4, no. 1, pp. 92-98, Mar. 2004.

[76] M. Ruberto, et al., "Consideration of age degradation in the RF performance of CMOS radio chips for high volume manufacturing," in *IEEE Radio Frequency Integrated Circuits (RFIC 2005) Symposium*, Long Beach, CA, USA, Jun. 2005, pp. 549-552.

[77] G. Groeseneken, R. Degraeve, B. Kaczer, and P. Roussel, "Recent trends in reliability assessment of advanced CMOS technologies," in *IEEE Proceedings of the International Conference on Microelectronic Test Structures (ICMTS)*, vol. 18, Leuven, Belgium, Apr. 2005, pp. 81-88.

[78] E. Xiao, "Hot carrier effect on CMOS RF amplifiers," in *IEEE 43rd Annual International Reliability Physics Symposium (IRPS)*, San Jose, CA, USA, Apr. 2005, pp. 680-681.

[79] A. Scuderi, L. La Paglia, F. Carrara, and G. Palmisano, "A VSWR-Protected Silicon Bipolar RF Power Amplifier With Soft-Slope Power Control," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 611-621, Mar. 2005.

Chapter II. A 60GHz 65nm CMOS power detector

Chapter introduction

This second chapter presents a 60GHz 65nm CMOS power detector that has been implemented to detect the VSWR induced by obstructed antenna close vicinity. Power detectors are often divided in two different modules following Figure II-1: the power detector itself and the power coupler. The power detector is the active part that realizes the conversion between a current or voltage into power information. The power coupler realizes the interface with the direct RF path (from the PA to the Antenna).

Before presenting the chosen solution, the circuit design and the simulation results, a state-of-the-art is given considering separately the power detector and the power coupler. The circuit design implementation for testability is then presented as some additional components have to be integrated to be able to measure the power detector circuit. Load-pull measurement results are finally given to characterize the designed power detector circuit and to verify its ability to detect antenna VSWR.

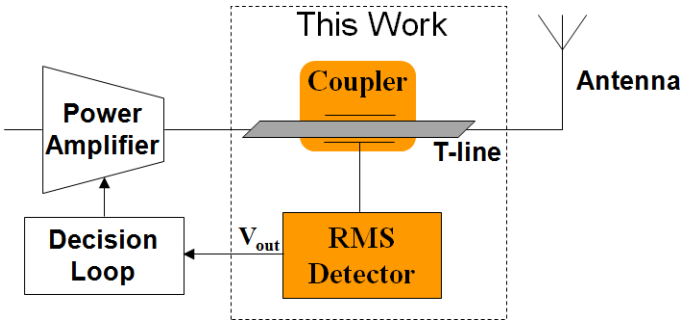


Figure II-1 Integration of a coupler and a RMS detector

Chapter outline

II.1. State of the art

The state-of-the-art presented hereafter is divided in two parts as power detection techniques are often requested two distinguished modules which realize each a specific function as illustrated in Figure II-1. The power detector first is the active part of the circuit that translates a voltage or current into power information. The power coupler then which most of the time only includes passive components is used to interface the power detector module with the RF chain. Its specific function is to take a sample or weighed copy of the RF signal and send it to the power detector while having minimum impact on the RF signal flowing in the direct path (from the PA to the antenna).

Both modules are then being studied separately.

II.1.1. Power detector

RMS power detectors are used to obtain power information. That means to square and low-pass filter a voltage or current information or simply root mean square power information if it is possible. As it has been introduced in section I.3.3, the most critical impacts of antenna VSWR on CMOS power amplifiers imply high voltage levels. We have actually chosen to measure the power as the square of the voltage rather than working on the current. Several techniques have already been imagined and implemented to realize the square of the voltage function.

The purpose of the following paragraphs is not to present every techniques that have been used for measuring the power in instrumentation equipment (see [1]) but we present hereafter a non-exhaustive state of the art of power measurement techniques actually used in integrated circuits.

i. Thermal detectors

One of the most usual technique to measure an RMS power value is to convert this power into the temperature domain and measure the temperature variation, as shown in Figure II-2. This is called a thermal detector. In practice, the incident power is dissipated into a resistor that creates a temperature growth in the near surrounding area of the resistor. By measuring this temperature growth we obtain the desired power information. The RMS function is automatically realized by the thermal capacity of the thermal cavity. The temperature varies progressively in the thermal cavity and does not follow the RF signal itself but its envelope.

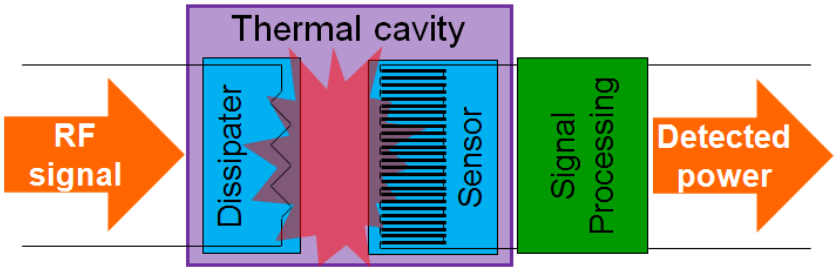
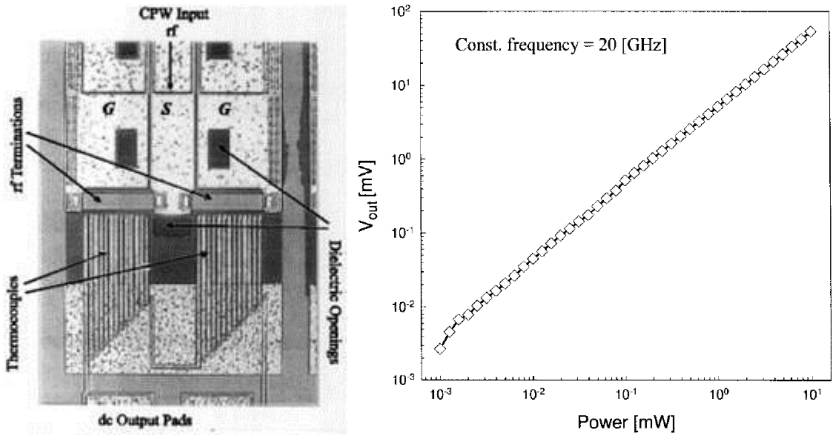


Figure II-2 Principle of a thermal power detector

There are two ways of sensing the temperature growth: using a thermistor and using a thermocouple [1] [2]. A thermistor converts the temperature variation into a resistance variation that has to be processed to obtain the desired information in the form of a voltage or current. A thermocouple is a junction between two different metals that produces a voltage related to a temperature [1]. We often use several thermocouples in series in order to increase the voltage variation.

[3] presents the realization of such thermal detector in a commercial CMOS process using micromachining techniques in order to realize the thermocouples that sense the temperature elevation. This detector is able to sense the RMS power from -30dBm up to 10dBm in the frequency range from 50MHz up to 20GHz with linearity better than ±0.16%. The die photograph of this realization is presented in Figure II-3.a and the output voltage versus the incident power is plotted in Figure II-3.b.



a. Die photograph **b. Output voltage versus incident power**

Figure II-3 Thermal detector in commercial CMOS process using micromachining techniques

Thermocouple based thermal detectors present a higher dynamic range than thermistor ones while being less sensitive to the ambient temperature evolution. Nevertheless, both thermal detectors need to be calibrated and present a long data acquisition time – 1ms for thermocouple and tens to hundreds of milliseconds for thermistor – due to the thermal conversion [2]. In both cases the power to be measured is consumed in a resistor creating a highly invasive sensor.

ii. Approximation of exponential characteristic

A power detector can also use the square law approximation of the diode exponential characteristic. A P-N junction – i.e. a diode – or a metal / semiconductor contact – found in schottky diodes – actually follows the exponential characteristic of the equation (II.1) where I_D is the diode current, V_D the voltage across the diode, I_S the reverse bias saturation current, V_t the thermal voltage, and n the ideality factor.

$$I_D = I_S\left(\exp\left(\frac{V_D}{nV_t}\right)-1\right) \tag{II.1}$$

Considering the Taylor series development of the exponential function near *0*, the equation (II.1) becomes:

$$I_D = I_S\left(\frac{(V_D/nV_t)}{1!}+\frac{(V_D/nV_t)^2}{2!}+\frac{(V_D/nV_t)^3}{3!}+\ldots\right) \tag{II.2}$$

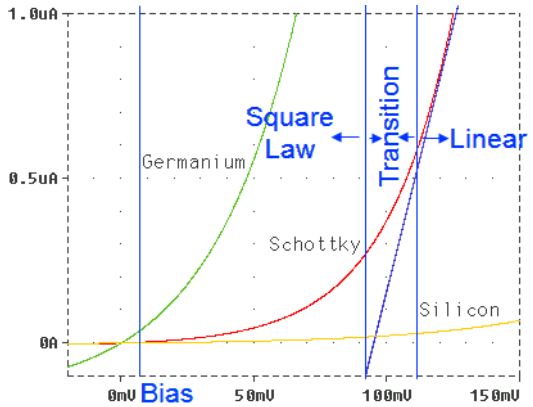


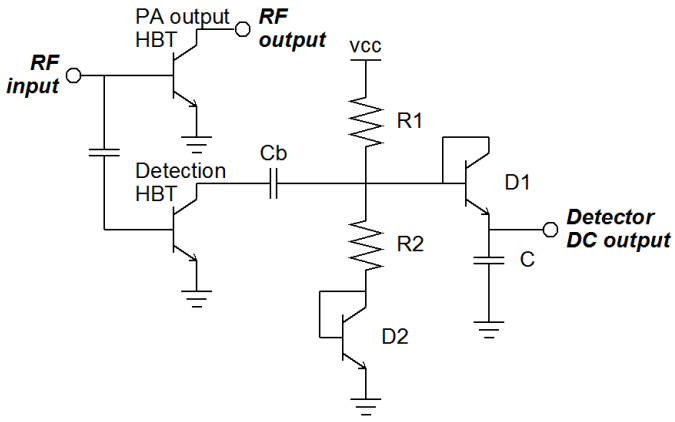
Figure II-4 Silicon (yellow), Schottky (red) and Germanium (green) diodes characteristics

For small signals, only the second order term is significant and the diode works in its square law region. In this case, the diode current is proportional to the voltage across the diode squared. Then a

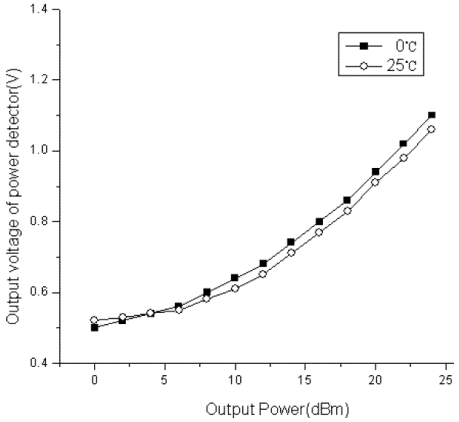
simple low-pass filter realizes the RMS function. When the voltage grows up, the diode detector is no longer in its square law region. After a transition region, the characteristic becomes linear and the device can be used as a peak detector. Figure II-4 depicts the characteristics of silicon, germanium and schottky diodes and the three different regions of exponential approximation. Schottky diodes are often used as their thermal voltage is lower than the one of silicon but schottky diodes are unavailable in many advanced processes.

Diode detectors are widely used in instrumentation equipment as a complement of thermal detectors [1]. However, diode detectors have also been implemented in silicon in order to target radio frequency telecommunication applications.

[4] presents a diode detector in SiGe HBT technology for TD-SCDMA application (3rd generation cellular standard). Figure II-5 illustrates this implementation with the schematic (a.) and the simulated voltage as a function of power characteristic (b.). The simulation shows a linear detection region from 15dBm up to 24dBm limited by the test setup. But the detector is sensitive to the temperature as it can be seen in Figure II-5.b and as it was predicted by the thermal voltage V_t – equal to kT/q – dependence in the equation (II.2).



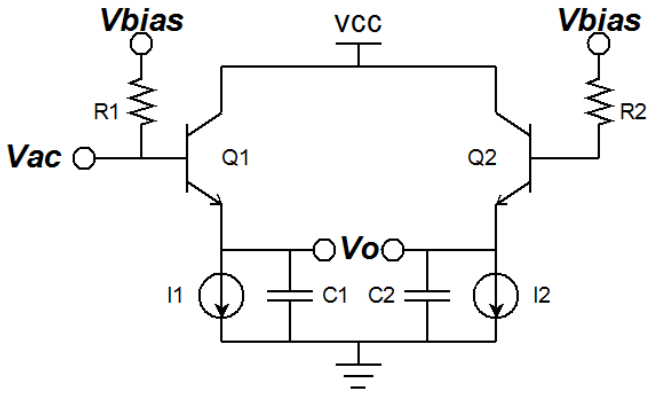
a. Detector schematic



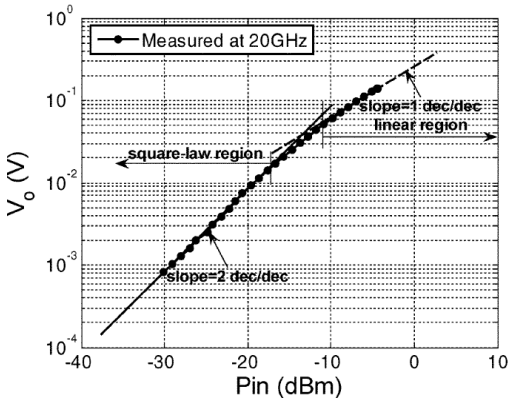
b. Simulated detector output voltage versus PA output power for two temperature conditions

Figure II-5 Diode detector SiGe implementation

The bipolar transistor has also an exponential characteristic when working in its active direct region, which can also be exploited to build an RMS detector. Meyer structure [5], which was initially used for peak power detection when the characteristic is linear, can actually also realize RMS power detection if the signal is small enough to stay in the region where a square law is a good approximation of the exponential function as explained in [6].



a. Detector schematic



b. Measured transfer characteristic

Figure II-6 Meyer's detector

Figure II-6.a presents the schematic of Meyer's detector. This structure needs a common biasing voltage V_{bias} on both transistors base, a single RF input voltage V_{ac} and provides the output voltage V_o across both transistor emitter. After several approximations detailed in [6], this output voltage is linearly proportional to the sum of the squares of all harmonics' amplitudes as can be seen in the equation (II.3).

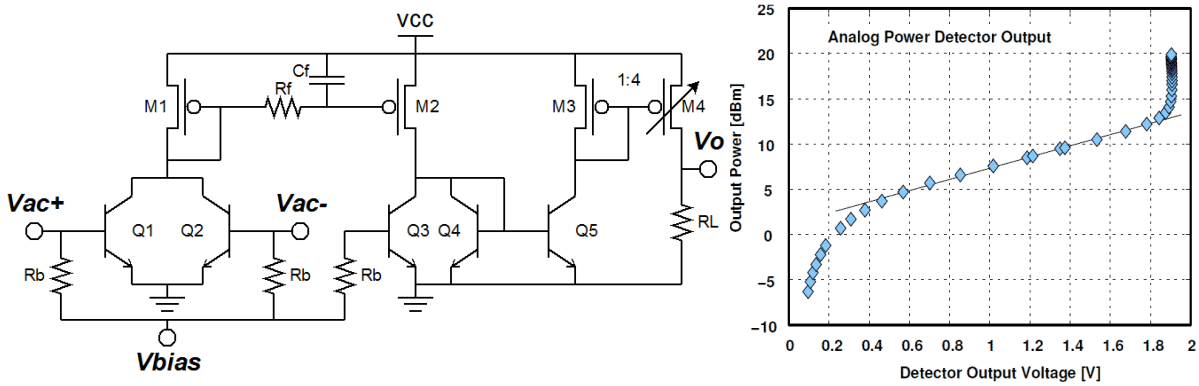
$$Vo \cong \frac{1}{4.V_t} \sum_{i=1}^{N} \left(Vac_i^{\,2} \right) \tag{II.3}$$

This peak/RMS power detector was fabricated using the IBM7WL BiCMOS process. The measured transfer characteristic – output voltage V_o vs. input power P_{in} – is presented in Figure II-6.b for a 20GHz sine wave input signal. The square law region is limited to 20dB dynamic range. The detector becomes linear for high input power.

This structure has been modified in [7] by adding a resistive link between the RF input signal V_{ac} and the base of the Q2 transistor in order to decrease the size of the transition region. In this solution implemented in IBM6HP BiCMOS process, the detector follows a square law on 30dB dynamic range for a 5GHz sine wave input signal.

Also based on the square law approximation of bipolar transistor exponential characteristic, [8] presents a differential RMS power detector. The schematic is shown in Figure II-7.a. Transistors Q1 and Q2 are biased in a class-B regime where each collector current is exponential with respect to the ratio Base-Emitter voltage V_{BE} on the thermal voltage V_t. The exponential function can be approximated by a polynomial function as in the equation (II.2) where V_D will be replaced by V_{BE}. The combination of both transistor currents will remove all odd-order components and double all even-order components. As a first order, the sum of the collector currents is proportional to the squared input voltage. By developing the cosines function squared, the resulting sum of both collector currents (equation (II.4)) is proportional to a DC component and a $2.f_0$ component that is low pass filtered by R_f and C_f. After amplification the resulting output voltage V_o is a DC component proportional to the input signal amplitude V_{ac} squared.

$$I_{CQ1+CQ2} \propto \left(\frac{V_{BE}}{V_t} \right)^2 = \left(\frac{V_{ac} \cos(i\omega_0 t)}{V_t} \right)^2 = \left(\frac{V_{ac}}{V_t} \right)^2 \cdot \left(\frac{1+\cos(2i\omega_0 t)}{2} \right) \tag{II.4}$$



a. Detector schematic **b. Measured transfer characteristic**

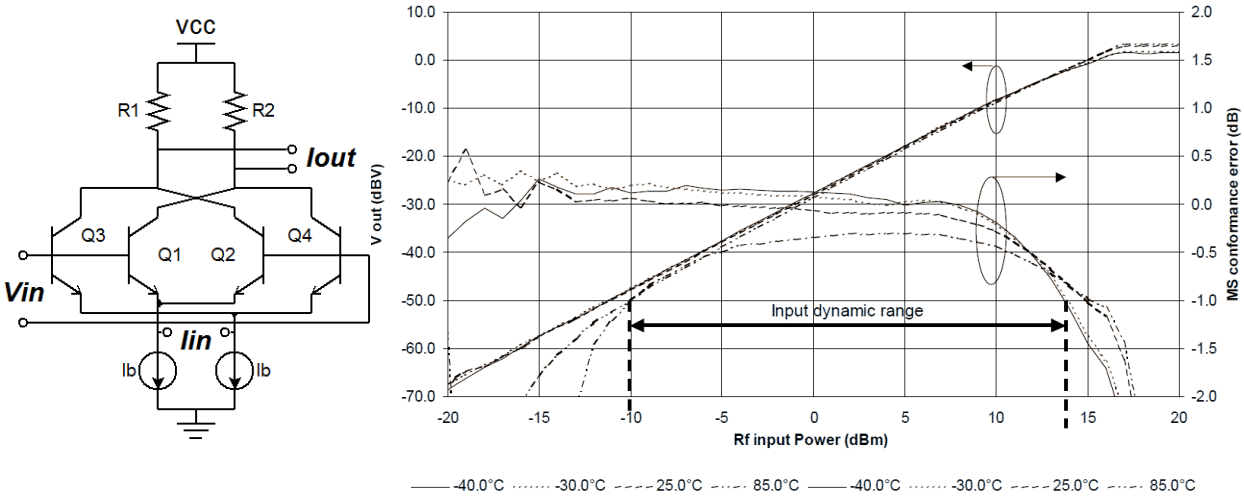
Figure II-7 Pfeiffer detector

This detector was implemented coupled to a PA and was fabricated in a 0.13µm SiGe BiCMOS process technology from IBM. Figure II-7.b presents the measured detector output voltage versus PA output power characteristic. For a 60GHz sine wave input signal, the detector response is linear from 4 up to 12.5dBm. The RC network was designed with a cut-off frequency of 13.8MHz that means that this detector could follow a 13.8MHz envelope evolution of a 60GHz sine wave signal.

To conclude on this kind of detector, the square law approximation of an exponential semiconductor characteristic (diode or bipolar transistor) is a high frequency and low cost solution. However this approximation is possible only on a reduced region that limits the dynamic range. Moreover the temperature dependence is very high, which is a major drawback.

iii. Analog signal processing

The square law can also be realized by an analog signal processor. The most famous one is the Gilbert multiplier cell. The square law function is actually just the multiplication of a signal by itself. The application of this technique for power detection has been patented in 2001 [9] with some extra improvement techniques. Figure II-8.a shows the Gilbert detector schematic.



a. Detector schematic **b. Measured transfer characteristics**

Figure II-8 Gilbert cell multiplier

[10] presents a 0.35µm BiCMOS process implementation for WCDMA applications at 2GHz. In this implementation, the power detector includes also a chopper in order to eliminate the multiplier offset. By performing the multiplication operation at an intermediate frequency (the chopper frequency), the DC multiplier offset does not affect the result. The measured detection characteristic is shown in Figure II-8. The linear detection range is 20dB with less than 1dB error over the temperature range from -40°C to +85°C.

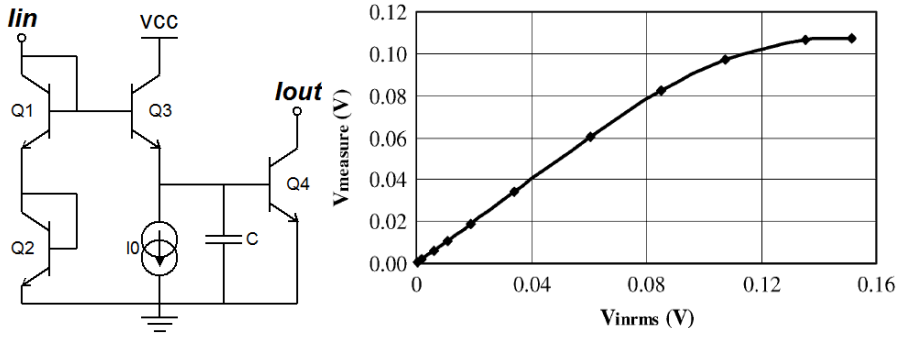
Another analog signal processing for RMS power detection is based on the translinear principle [11] that can be used to realize a current square divider. Voltage-to-current (V-I) and current-to-voltage (I-V) converters are integrated at the input and output of this current square divider to form a translinear detector. The principle of operation of translinear detectors actually is that an AC input voltage is converted to a current signal (V-I converter), squared by a current square divider circuit, converted to a voltage (I-V converter) and then low-pass filtered to produce a DC output voltage proportional to the power of the input signal. Figure II-9.a presents the schematic of the square divider, the translinear cell. For ideal transistors (infinite β), the input and output currents I_{in} and I_{out} are linked together with $\dot{I}_{out}$ the derivative of I_{out} by the relation (II.5) where I_0 is the bias current and V_t the thermal voltage.

$$I_{in}^{\,2} = I_0 . I_{out} + C.V_t . \dot{I}_{out} \tag{II.5}$$

Solving (II.5), the output current is proportional to the time-averaged (function $\langle\ \rangle$) input current squared, that means to the mean-square of the input signal (equation (II.6)).

$$I_{out} = \frac{I_{in}^{\,2}/I_O}{1 + s.C.V_t/I_O} = \left\langle \frac{I_{in}^{\,2}}{I_O} \right\rangle \tag{II.6}$$

This principle has been implemented in [12] and fabricated in the IBM 6HP BiCMOS process. A bias circuit and input and output interfaces were added to the simple translinear circuit represented in Figure II-9.a. In this implementation, a square-root function was done off-chip resulting in a voltage-voltage characteristic (not power-voltage). This characteristic is shown in Figure II-9.b for a 1GHz RF input signal.



a. Detector schematic **b. Measured transfer characteristic**

Figure II-9 Translinear Detector

To conclude on analog signal processing detectors we can notice the good accuracy (error less than 1%) of this low cost solution. However the complexity of the circuits limits the bandwidth to 1 or 2GHz.

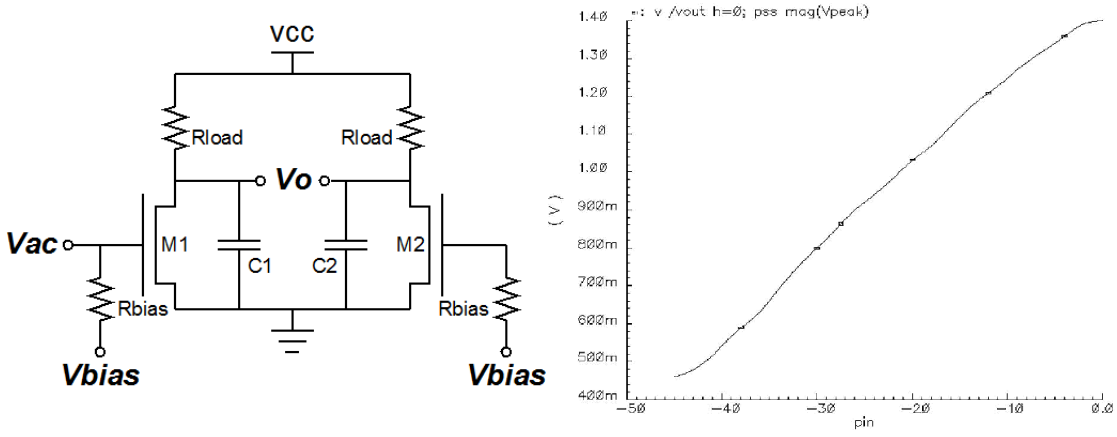
iv. MOS naturally square law detectors

Previous detectors use thermal effects, square law approximation of an exponential characteristics or complex analog signal processing. However the easiest way to realize the desired function is simply to use the MOS naturally square law characteristics when biased in saturation. Saturated MOS characteristics – drain-source current I_{DS} versus gate-source voltage V_{GS} – actually is a square law as it can be noticed in the equation (II.7) where every notation has its usual meaning.

$$I_{DS} = \frac{K.W}{2.L}.\left(V_{GS} - V_t\right)^2.\left(1+\lambda.V_{DS}\right) \qquad \text{(II.7)}$$

[13] presents a MOS implementation of the Meyer detector (see section II.1.1.ii). The schematic is shown in Figure II-10.a and the simulation results on the IBM BiCMOS6HP process in Figure II-10.b. Considering a sine wave signal ($V_{ac} = |V_{ac}|.\cos(\omega.t)$) applied to this detector input, the drain-source current of *M1* & *M2* follows the equation (II.7) and after being low-pass filtered by *C1* and *C2*, the differential output voltage V_0 is proportional to the input signal amplitude V_{ac} squared (equation (II.8)).

$$V_0 = \frac{K}{4}.\frac{W}{L}.R_{load}.V_{ac}^{\ 2} \qquad \text{(II.8)}$$



a. Detector schematic **b. Simulated transfer characteristic**

Figure II-10 MOS Meyer detector

A chopper modulator (working at 500kHz) and a progressive compression logarithmic amplifier were added to the detector resulting in a linear output voltage versus input power expressed in [dBm]. This detector achieves 45dB dynamic range with bandwidth up to 6GHz.

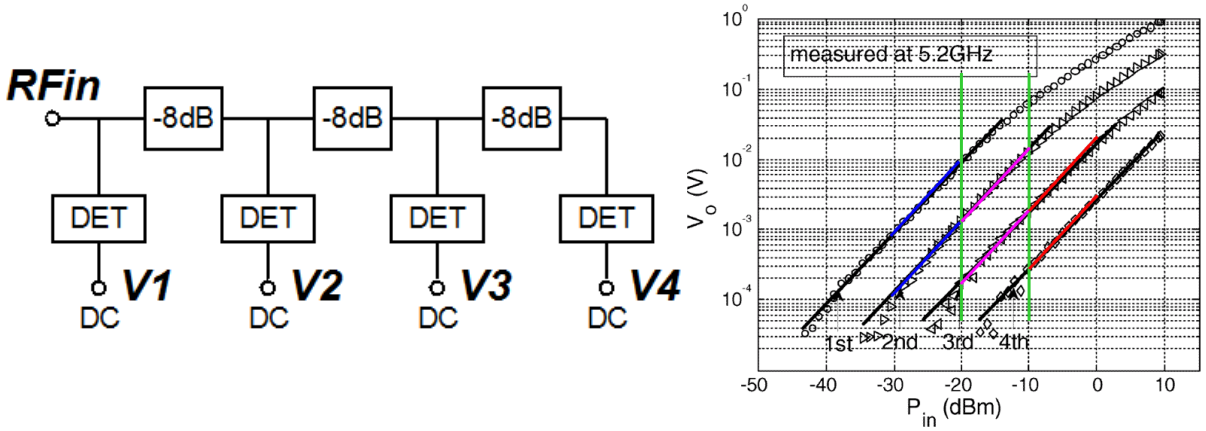
Saturated MOS is a very powerful technique to realize a square law that can be applied to RMS power detectors. The simplicity of this solution actually makes it very low cost – furthermore it is CMOS technology – and low power (17mW for this implementation). Moreover it achieves a high dynamic range and a high bandwidth.

v. Increasing the dynamic range of a detector

The dynamic range limitation can be overcome by building a ladder of detectors and attenuators as presented in Figure II-11.a. This technique is conceptually very easy but practically it results in a huge cost in term of complexity, size and consumption. This technique has been implemented in [6].

Several Meyer detectors (see section II.1.1.ii) were associated together in a ladder topology with 8dB attenuators. The appropriate detector output – the one which is in its linear running region – is selected by the computation of all detector outputs. By comparing the ratio of consecutive detector output voltage (eg. V_2/V_1 or V_3/V_2), the appropriate detector output is indicated by the ratio that best approximates the attenuator gain.

This implementation results are shown in Figure II-11.b where the color code illustrates the detector selection principle. The 20dB square law dynamic range of a single detector is extended up to 40dB with 4 detectors.



a. Circuit synoptic **b. Measured transfer characteristics**

Figure II-11 Dynamic range increasing technique

Despite its already presented drawbacks, this technique permits a high dynamic range improvement. Including it in this state-of-the-art was a way to put into perspective the dynamic range limitation of certain detection techniques presented previously. The dynamic range could be increased in most of those situations.

vi. Discussion

Table II-1 summarizes the different advantages and drawbacks of the power detection techniques previously presented.

	Dynamic Range	Accuracy	Bandwidth	Complexity	Integration
Thermal detector	+	++	++	--	--
Approx. of exponential behavior	--	-	++	+	+/-
Analog signal processing	+	++	--	-	+
MOS square law detector	++	+	+	+	++

Table II-1 Comparison of the different power detection techniques

II.1.2. Power coupler

The detector module being yet presented, we can now study the different solutions to connect this detector module to the transmitter chain with minimum impact on the RF signal.

Connecting directly the power detector cell to the power amplifier output would highly influence the signal on the direct path, thus resulting in a deterioration of the transmitter performances while sensing the wrong power level on the detector. A power coupler is hence needed to realize the interface between the power detector and the rest of the circuit (see Figure II-1).

Furthermore, the integration of a power coupler adds an attenuation coefficient that generally could be adjusted by the design parameters. This attenuation coefficient can be tuned to match the detector input signal to the detector square law working region and optimize the full power detector dynamic range.

i. Direct connection, no coupler integrated

Although many power regulation loops do not integrate any power coupler before the power detector, this simplified scheme illustrated in Figure II-12 needs a particularly high impedance detector input not to deteriorate the signal to be measured. That is often the case when using diode detectors as in [14] and in [15].

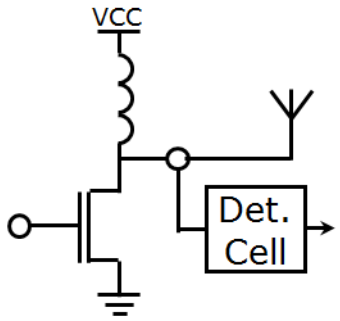


Figure II-12 Direct connection of the power detector to the direct path

Some regulation loop integrates very simple passive networks to realize this interface resulting in a high impedance detector input. In [16] a simple resistive link is implemented. In [17] resistors are coupled with capacitors to realize a less invasive power detection solution as can be seen in Figure II-13.

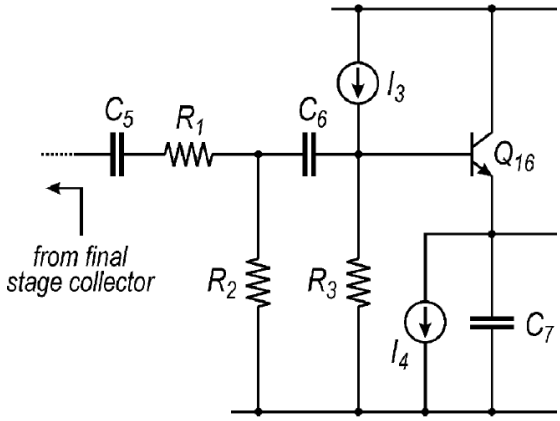


Figure II-13 R-C passive network connection between the envelope detector and the direct path

ii. Parallelization of the power transistor

Even using diode detectors, it could be preferred to implement a separate signal path just for the detection. As an example in [4], a transistor is integrated in addition to the main path of the power amplifier to realize the interface between the detector and the direct signal path as can be seen in Figure II-14.

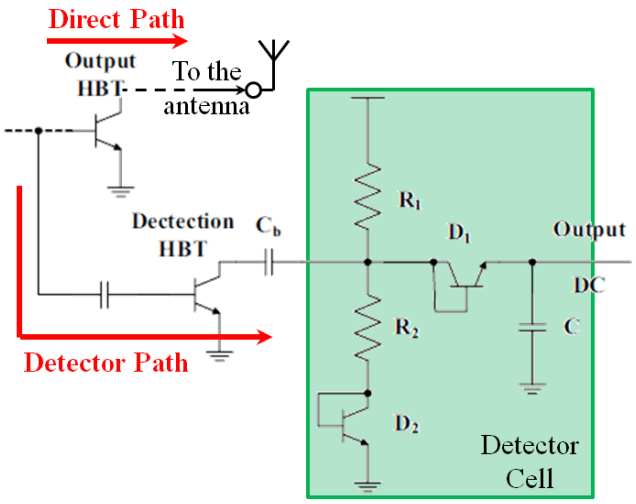


Figure II-14 Parallelization of the power transistor

This solution seems to present very low influence of the detector on the rest of the circuit, but as this power detector is not connected to the PA output it will not be sensitive to the PA output impedance mismatch. So this solution is not suitable for our application.

iii. Directional coupler

Another way to connect a power detector to an RF transmitter chain is to use a directional coupler. This kind of detector is composed of 2 transmission lines of λ/4 length (so it depends of the application frequency) that are coupled electromagnetically. Figure II-15 presents the connection in an RF chain of a directional coupler. Port 1, called input port, is connected to the PA output. Port 2, called transmitted port, is connected to the antenna. Port 3, called coupled port, is connected to the power detector. Port 4, called isolated port, is connected to a 50Ω reference impedance. The advantage of this technique is that the wave flowing from the coupled port is an image of only the incident wave that flows into port 1.

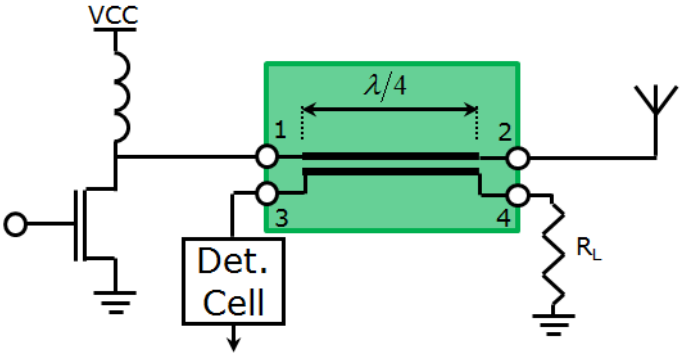


Figure II-15 Directional coupler connection

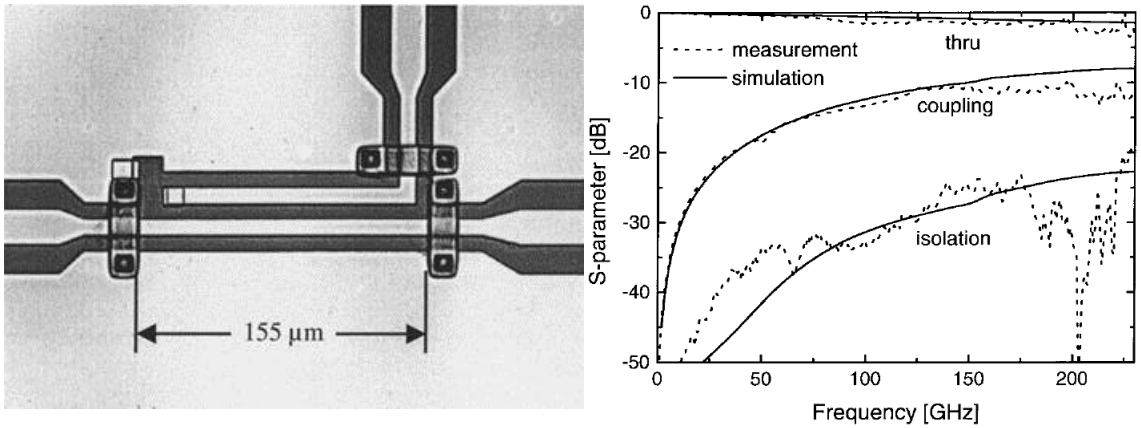
Several definitions are needed as they are commonly used to characterize those devices. The coupling factor *CF*, the isolation *Is*, the insertion loss *IL* and the directivity *Di* are derived as detailed in equations (II.9) from the waves *P1*, *P2*, *P3* and *P4* that flow respectively in the ports 1, 2, 3 and 4 described in Figure II-15.

$$CF = -10.\log\left(\frac{P3}{P1}\right) \qquad Is = -10.\log\left(\frac{P4}{P1}\right)$$
$$IL = -10.\log\left(1-\frac{P3}{P1}\right) \qquad Di = -10.\log\left(\frac{P4}{P3}\right) \tag{II.9}$$

For an ideal directional coupler, those parameters should tend to the infinity except the insertion loss that should tend to 0. The coupling factor, the isolation and the directivity are linked together by the relation (II.10).

$$Di = Is - CF \tag{II.10}$$

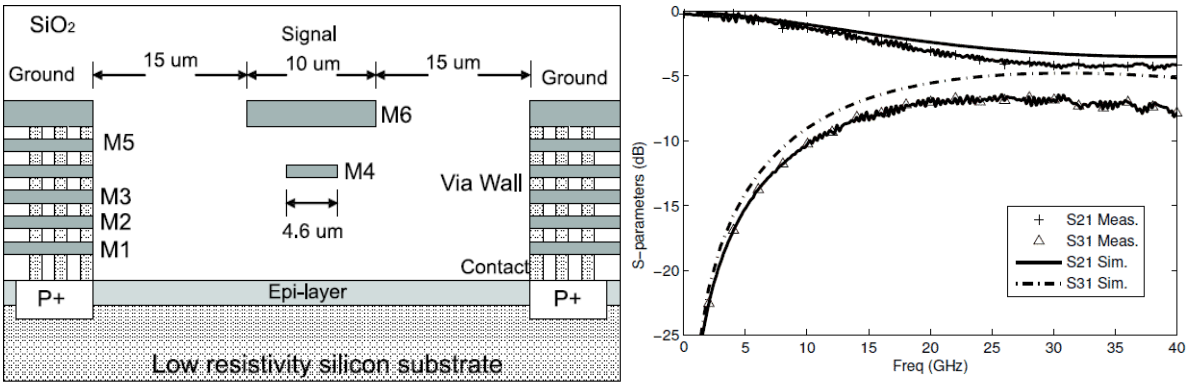
[18] presents the integration of a 180GHz directional coupler in GaAs technology. The coupler is represented in Figure II-16.a and has a 155µm length. The simulated and measured results are compared in Figure II-16.b. This coupler shows a -11dB coupling factor up to 180GHz, a -24dB isolation that can be traduced by a -13dB directivity (equation (II.10)), while the insertion loss stay behind -3dB.



a. **b.**

Figure II-16 Integrated directional coupler on a GaAs substrate running at 180GHz

Directional couplers can also be implemented in CMOS technology. [19] presents a 10-40GHz directional coupler fabricated in a 0.18µm commercial CMOS process from National Semiconductor. Figure II-17.a shows the cross section of this coplanar coupler where the direct path is in the upper metal (M6) and the coupled line is in metal 4. Those two lines are coupled along 934µm.



a. **b.**

Figure II-17 Integrated 10-40GHz directional coupler on a 0.18µm CMOS process

The simulated and measured S-parameters are compared in Figure II-17.b. This directional coupler presents -7 to -10dB coupling factor and more than 10dB directivity within 10-40GHz. However the -5dB insertion loss are too high for a practical integration of such coupler in an RF transmitter. Particularly in our case at 60GHz, this high loss located between the PA and the antenna is not acceptable and cannot be compensated by the CMOS PA in order to reach the high output power which is required by the standard [20]. Furthermore, directional couplers need λ/4 length coupling lines; and even for a frequency as high as 60GHz, this constitutes a major integration limitation. So, we cannot use such directional coupler solution.

iv. Capacitive coupler

Capacitive couplers use capacitors to collect a part of the energy from a transmission line (T-line) to the detector. In practice, a little metal rectangle is inserted under the T-line that creates two capacitors: one with respect to the line and the second to the grounded substrate. That results in a capacitive divider. Professor Pfeiffer has used this kind of couplers in [8]. The 3D structure integrated in the backend of the IBM SiGe process is depicted in Figure II-18.

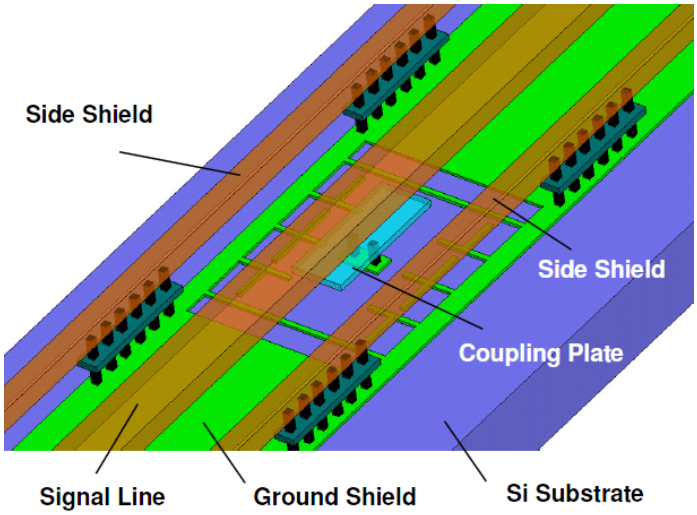


Figure II-18 Capacitive coupler using silicon backend process

The coupler voltage attenuation coefficient is given by the capacitors ratio of the divider and can be tuned by adjusting the distance of the coupling plate metal from the T-line – i.e. by choosing the metal level that best fits the desired attenuation coefficient. This value can also be tuned by adjusting the size of the coupling plate. However it is needed to perform Electro-Magnetic simulations on this kind of structure in order to tune the coupler parameters to obtain the desired voltage attenuation coefficient as it will be detailed in the next section.

In [8], the structure of the Grounded Coplanar Waveguide (G-CPW) T-line has been modified in the coupler region in order to keep constant the propagation impedance on the T-line. As a consequence, this capacitive coupler has a negligible effect on the direct path. Furthermore, the transmission line is not an additional component as it is needed to connect the power amplifier output to the antenna input. So this coupler has a high integration capability.

v. Discussion

Table II-2 summarizes the advantages and drawbacks of the power coupler techniques previously presented. The capacitive coupler represents a very attractive solution that we have chosen to implement. This implementation will be discussed in the next section.

	Impact on direct path	**Integration**	**Accuracy**
Direct connection	--	++	+
Parallelization	++	-	-
Directional coupler	--	--	+
Capacitive coupler	+	++	+

Table II-2 Comparison of the different power coupler techniques

II.2. Chosen solution and Circuit Design

The following section details the chosen solution in our design for the power detector and the power coupler.

II.2.1. Power detector

For the RMS power detector, we have chosen the concept of the differential structure proposed by U. Pfeiffer in [8] (see section II.1.1.ii) with the advantage of the naturally square law of MOS transistor in saturation (see section II.1.1.iv). This solution should permit us to obtain a high dynamic range with a high frequency differential input signal.

i. Schematic

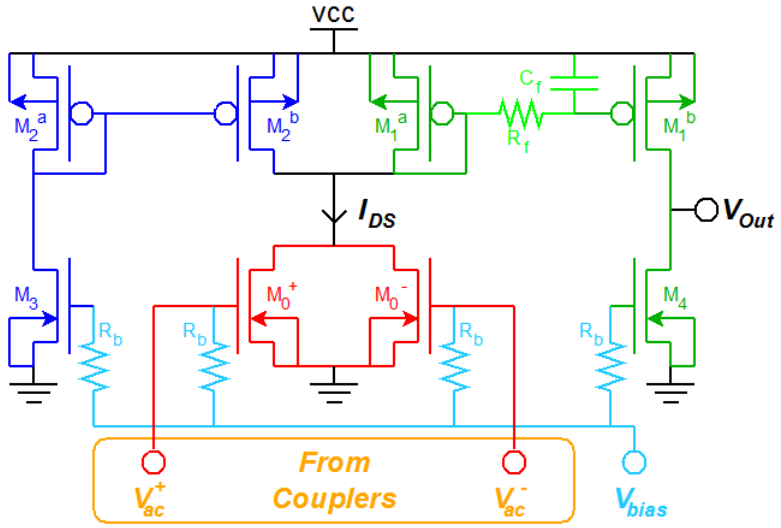


Figure II-19 Designed detector schematic

The schematic of the proposed RMS power detector is presented in Figure II-19. This detector is composed of a detector cell, a biasing cell, an amplifier and an RC filter. The detector cell – in red in Figure II-19 – contains the 2 N-MOS transistors M_0^+ and M_0^-. Working in saturation, each drain current I_{DS}^+ and I_{DS}^- follows the square law characteristic of the equation (II.11) where each notation has its usual meaning.

$$I_{DS}^{\pm} = \frac{K.W}{2.L}.\left(V_{GS}^{\pm} - V_t\right)^2.\left(1+\lambda.V_{DS}^{\pm}\right) \quad \text{(II.11)}$$

By applying on both MOS gate a differential sine-wave signal (see equation (II.12)) of V_{ac} amplitude and ω_0 pulsation in addition to the biasing voltage V_{bias} forced by the resistors R_b – in light blue in Figure II-19 – the resulting sum I_{DS} (see Figure II-19) of both drain-source currents is proportional to a biasing component plus the differential input voltage squared (equation (II.13)).

$$V_{GS}^{\pm} = V_{bias} \pm V_{ac}.\cos\left(\omega_0.t\right) \quad \text{(II.12)}$$

$$I_{DS} = \frac{K.W}{2.L}.\left(1+\lambda.V_{DS}\right).\left(2.\left(V_{bias} - V_t\right)^2 + 2.\left(V_{ac}.\cos\left(\omega_0.t\right)\right)^2\right) \quad \text{(II.13)}$$

Developing the cosine squared of the equation (II.13) gives the equation (II.14).

$$I_{DS} = \frac{K.W}{2.L}.\left(1+\lambda.V_{DS}\right)\left(2.\left(V_{bias} - V_t\right)^2 + V_{ac}{}^2 + Vac^2.\cos\left(2.\omega_0.t\right)\right) \quad \text{(II.14)}$$

In this equation, the current I_{DS} is proportional to the sum of a biasing component $(V_{bias} - V_t)^2$, noted I_{bias} here after, a DC component $V_{ac}{}^2$, noted I_{useful} here after, and an RF component $V_{ac}{}^2.\cos(2.\omega_0.t)$ at twice the input signal frequency. This RF component is highly attenuated thanks to the low-pass filter composed by the resistance R_f and the capacity C_f – in light green in Figure II-19. The cutoff frequency of this filter will be noted f_c.

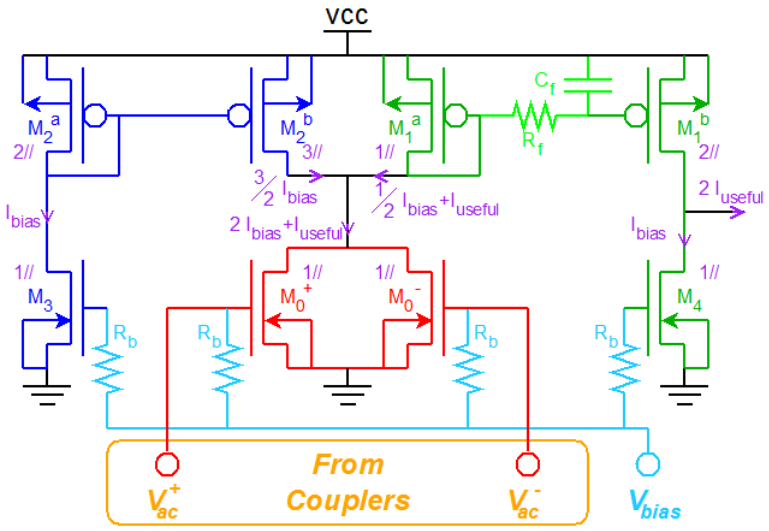


Figure II-20 Designed detector schematic with current repartition

Figure II-20 details the current dispatching through the blue and the green branches of the circuit. The blue branch – composed by the PMOS current mirror $M_2{}^a$ and $M_2{}^b$ and by the NMOS M_3 – is used to bias the detector cell $M_0{}^+$ and $M_0{}^-$ (in red on the figure). Thanks to the 3 for 2 PMOS mirror ratio the biasing current I_{bias} flowing in the branch $M_2{}^a$ M_3 is amplified to $3/2.I_{bias}$ that composed the major part of the $2.I_{bias}$ flowing in the detector cell. The remaining $1/2.I_{bias}$ is used to bias the amplifier cell in green in Figure II-20 – composed by the PMOS current mirror $M_1{}^a$ and $M_1{}^b$ and the NMOS M_4. The 2 for 1 mirror ratio amplifies the useful current I_{useful} – i.e. the DC component of I_{DS} in the equation (II.14) – and the $1/2.I_{bias}$ component which then flows in the NMOS M_4.

The resulting output current $2.I_{useful}$ is directly proportional to the differential input voltage amplitude squared $V_{ac}{}^2$. Hence this circuit realizes the desired function: RMS power detection.

The design uses standard transistors from 65nm CMOS process, either standard or low V_t flavor, but with no specific analog process option. As this circuit should detect 60GHz sine-wave input signal considering our Wireless-HD application, the length L of transistors $M_0{}^+$ and $M_0{}^-$ was minimized to 60nm. Using a capacitive coupler as it will be explained in section II.2.2, the $V_{ac}{}^+$ and $V_{ac}{}^-$ input parasitic capacitance should be minimized in order to have reduced influence on this coupler. The width W of $M_0{}^+$ and $M_0{}^-$ has been also minimized to 120nm. For a good biasing current matching between the 3 branches of the circuit, transistors M_3 and M_4 have the same sizes as $M_0{}^+$ and $M_0{}^-$.

Considering PMOS transistors now, for a good current repartition $M_2{}^a$, $M_2{}^b$, $M_1{}^a$ and $M_1{}^b$ should have the same sizes. Their size L and W should be large enough to realize a good copy of the current, but should also stay reasonable for implementation considerations. Those two parameters were also minimized in the first chip implementation – settled to 60nm and 120nm as NMOS L and W – resulting in a quite bad current copy as it will be detailed in the first chip measurement analysis, in section II.4. This error has been corrected in the second chip implementation where L and W were fixed respectively to 1µm and 2µm.

The RC filter cutoff frequency f_c should be carefully chosen in order to have enough RF signal attenuation first, but also because this cutoff frequency will fix the dynamic range of the detector by fixing the noise floor. A last consideration for the design of this RC network is the chip

implementation as capacitors are with inductors the most size consuming components in silicon integration.

ii. Noise study

The dynamic range of the detector is limited at low power levels by the noise floor. The Signal-to-Noise Ratio (SNR) should actually always be kept higher than 1 (or 0dB) in order to be able to separate the signal information from the noise. We can calculate this SNR by considering only the noise coming from the detector cell, the transistors M_0^+ & M_0^- – which are the only ones that work at 60GHz.

This SNR has been computed in Matlab starting from the characteristic $I_{DS}=f(V_{GS})$ of the desired NMOS transistors obtained by a DC simulation with Cadence (Spectre simulation using DK BSIM4 models). The waveforms of the current output signal I_{DS}^+ and I_{DS}^- of transistors M_0^+ and M_0^- are computed by applying a 60GHz sine-wave voltage on the gate of each MOS transistor (see the equations (II.12)).

In the same time can be calculated the noise current spectral density *Snid* (expressed in [A²/Hz]) of MOS transistors in saturation (equation (II.15) where each notation has its usual meaning). The transconductance *gm* is derived from the initial MOS transistor characteristic as in the equation (II.16).

$$Snid = \frac{8}{3}.KT.gm \tag{II.15}$$

$$gm = \frac{\Delta I_{DS}}{\Delta V_{GS}} \tag{II.16}$$

Considering a white noise, which is low-pass filtered in a first order RC network (R_f and C_f in Figure II-19) with a cutoff frequency f_c, the noise bandwidth is generally considered equal to $\pi/2.f_c$. The SNR is hence given by the equation (II.17), where the notation $\overline{I_{DS}}$ stands for the time average of the signal current I_{DS} (which means that the biasing component is not taken into consideration here), and $\overline{Snid}$ for the noise current spectral density *Snid*.

$$SNR = \frac{\left(\overline{I_{DS}}\right)^2}{\overline{Snid}.\frac{\pi}{2}.fc} \tag{II.17}$$

However, this demonstration assumes a first order low-pass filter and the MOS transistors have to stay in their saturation regime.

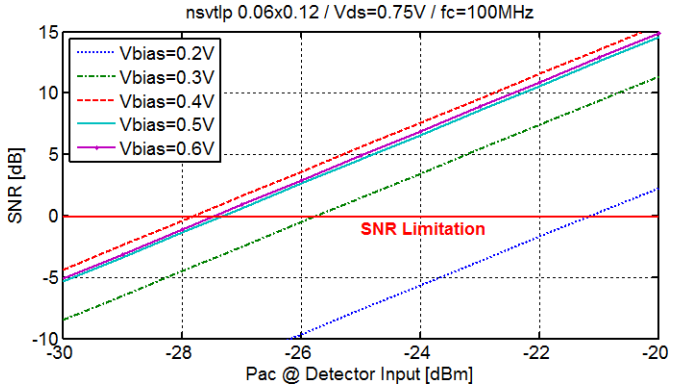


Figure II-21 Noise simulation: *SNR* versus detector input power P_{ac} for several biasing voltages

We can now compare the SNR – and the induced dynamic range – for several biasing voltage from 0.2V up to 0.6V. For this simulation we have decided to fix the cutoff frequency to 100MHz. We have also considered a constant V_{DS} of 0.75V on the detector cell – we have verified that the voltage

V_{DS} does not affect significantly the SNR – which is composed of transistor nsvtlp of size 0.06 per 0.12 µm². Figure II-21 presents the results of this simulation where the coupler attenuation coefficient is not taken into consideration resulting in an offset of the dynamic range that could be quite high depending on the coupler voltage attenuation coefficient squared (see section II.2.2.vi). The SNR presents an optimum for a biasing voltage of 0.4V. This method can be used to determine the best biasing voltage that should be applied to the detector cell to maximize the dynamic range.

In the same way, we can fix the biasing voltage to 0.4V and the detector input power P_{ac} to 0dBm, and simulate the influence of the transistor width W on the SNR. The cutoff frequency f_c is still fixed to 100MHz. We can see in Figure II-22 that the SNR is directly proportional to the transistor width and double (+3dB in log scale) with the transistor width. This result could be predicted easily as the signal I_{DS} being directly proportional to W (equation (II.11)) is squared in the SNR expression (equation (II.17)). On the other hand, the noise current spectral density, being also directly proportional to W through the transconductance gm (equation (II.15)), only contributes with a power one to the SNR. The resulting SNR expression is hence directly proportional to the transistor width W.

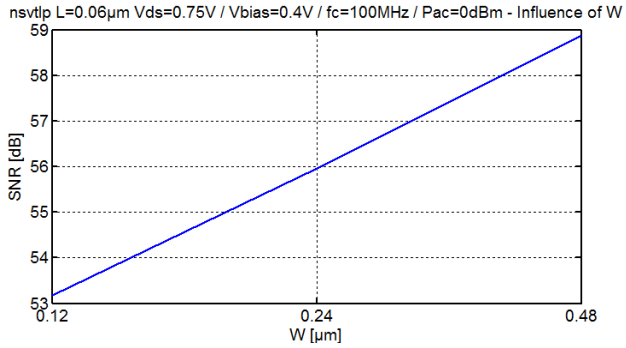


Figure II-22 Noise simulation: SNR versus detection transistor width

Although increasing the transistor width W could increase the SNR – so the dynamic range of the detector – we have chosen to keep this parameter to 0.12µm in order to minimize the detector input capacitance as explained in the previous section.

Another parameter which has an important effect on the SNR is the cutoff frequency f_c of the low-pass filter. The equation (II.17) actually predicts that the SNR should be inversely proportional to the cutoff frequency. The simulation is fully compliant with this prediction as it can be seen in Figure II-23, the SNR is inversely proportional to the cutoff frequency f_c (-10dB/dec ramp).

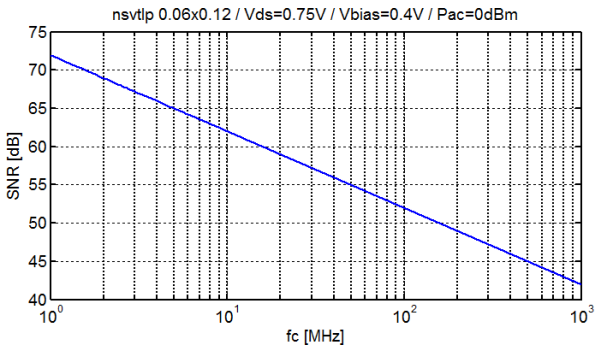


Figure II-23 Noise simulation: SNR versus 1st order low-pass filter cutoff frequency f_c

In conclusion, the cutoff frequency of the 1st order low-pass filter will highly affect the dynamic range of the detector. The lower is this frequency the higher is the dynamic range. However it is quite difficult to integrate high value capacitors in silicon and the detector dynamic response is derived from the desired application: the cutoff frequency f_c should be higher than the desired regulation loop speed. In our case we have chosen to fix this cutoff frequency to 100MHz which corresponds to an interesting regulation speed even if the implemented regulation loop is very slower (see Chapter IV).

iii. Current-voltage conversion

The power detector presented in this section has a current output as can be seen in Figure II-20. Furthermore the current level is very low, in the range of 0.1µA which is very difficult to sense. So a current-voltage converter is integrated at the output of the detector cell. This converter is also used to amplify the useful signal and output a voltage that is possible to sense with commonly used measurement equipment.

Figure II-24 shows the schematic of the current-to-voltage converter. It is composed of two similar cells, each being built on a CMOS inverter with a resistive feedback (trans-impedance amplifier).

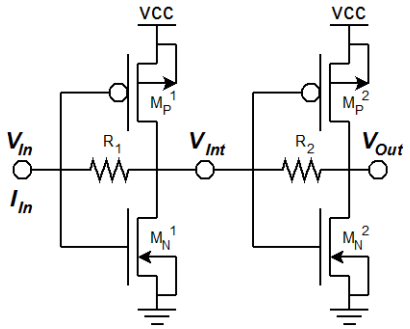


Figure II-24 Current-to-Voltage Converter schematic

The resistances and the MOS transistors have been sized to maximize the output voltage variation when charged by a 50Ω load while keeping a linear input current to output voltage transfer function. This results in a 0.1 x 3µm² (*L* x *W*) NMOS M_N^1 and a 0.1 x 10µm² PMOS M_P^1 on the first stage with a 10.24kΩ feedback resistance R_1. The second stage has 4 parallel 0.06 x 250µm² NMOS M_N^2 (split into 50 fingers), 4 parallel 0.06 x 250µm² PMOS M_P^2 (also split into 50 fingers) and a 10.24kΩ feedback resistance R_2.

iv. Simulation results

The simulation results presented here integrate the power detector and the current-to-voltage converter (also called buffer). No coupler is integrated yet, still resulting in an offset of the dynamic range of the detector cell with respect to the one of the full power detector.

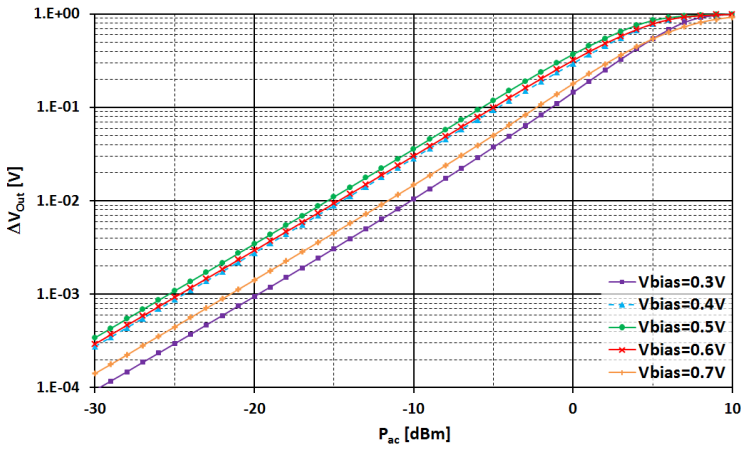


Figure II-25 Detector and buffer characteristic for various biasing voltages with svtlp transistors (1st circuit)

Figure II-25 shows the buffered output voltage variation ΔV_{out} versus the detector input power P_{ac} (calculated as the detector input voltage squared on a 50Ω load) for different biasing voltages V_{bias}. The characteristic has been simulated with an input power from -30dBm to +10dBm as at the lower limit the output voltage variation (between 0.1 and 1mV) is estimated to be very close to the noise level and at the upper limit both the detector and the buffer become saturated.

The extreme values 0.3V and 0.7V of V_{bias} generate a much lower output voltage variation which is also not linear versus the input power. The best characteristic – linear response and high output voltage variation – is founded for a V_{bias} around 0.5V. This conclusion is very close to the 0.4V optimized V_{bias} obtained in the noise study of section II.2.1.ii.

Figure II-26 shows the results obtained for the same circuit schematic (detector and buffer) placed in the same simulation conditions but using lvtlp MOS transistors rather than svtlp. The simulation in this case shows that the biasing voltage should be a little lower than previously as the optimized V_{bias} is between 0.4 and 0.5V – the two curves are confused. Here again the extreme case of 0.7V on V_{bias} generates a lower and a nonlinear voltage variation.

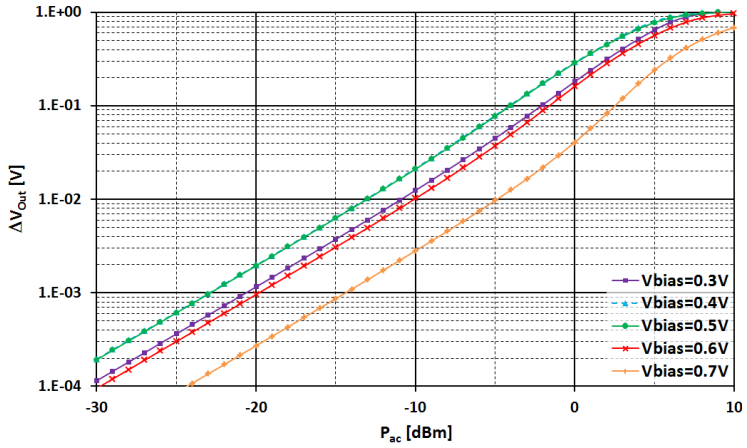


Figure II-26 Detector and buffer characteristic for various biasing voltages with lvtlp transistors (2nd circuit)

II.2.2. Power coupler

In order to predict coupler performances, Electro-Magnetic simulations have been performed. During this Ph.D. we have used both Ansoft HFSS [21] and Agilent Momentum [22] tools. All the presented simulations in this section II.2.2 have been performed with Ansoft HFSS [21]. Post Layout Simulations have then been realized with Agilent Momentum [22] with similar results. However in the two cases we have had to simplify the process backend as it will be presented now.

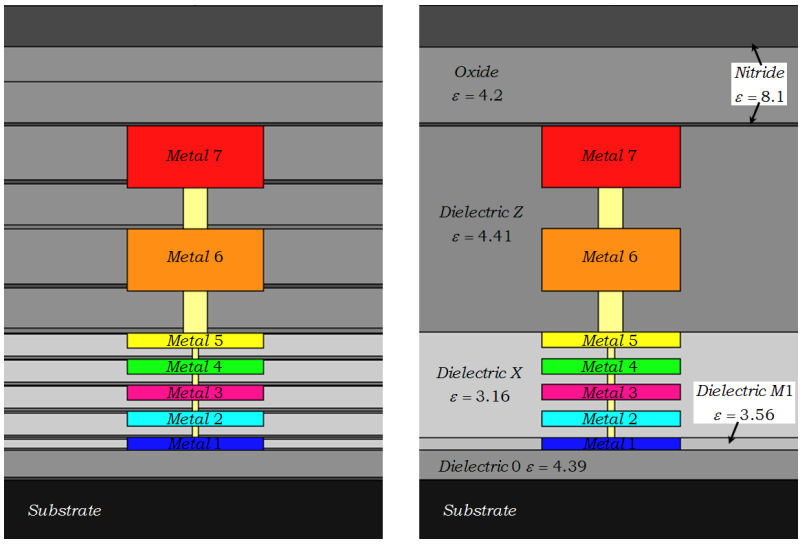
i. Modeling the backend of the 65nm CMOS process from STMicroelectronics

Electro-Magnetic simulators still present some issues in simulating complicated structures as our capacitive coupler designed in a deep submicron process backend of line (BEOL), such as CMOS 65nm from STMicroelectronics. This means some simplifications are needed to perform those simulations on a reasonable computer configuration and in a reasonable simulation time (less than 10 hours). The 3D structure of the coupler is actually simplified, especially the small elements like Vias. But the process backend includes also very thin layers of dielectric that imply very long simulation times. Here again we need some simplifications [23] [24].

Instead of considering each dielectric layers, we consider a single dielectric with equivalent characteristics. The equivalent relative permittivity ε_{req} is calculated using the equation (II.18) where n is the layer index, h_n the thickness of the nth layer and ε_n the relative permittivity of the nth layer [25].

$$\varepsilon_{req} = \left(\sqrt{\varepsilon_n} + \frac{h_{n-1}}{h_{n-1} + h_n} \left(\sqrt{\varepsilon_{n-1}} - \sqrt{\varepsilon_n} \right) \right)^2 \qquad \text{(II.18)}$$

Those simplifications can reduce significantly the complexity of the structure and so the simulation time. However all those simplifications need to be carefully studied in order to keep a structure as close as possible from the real circuit implementation. The difficulty is that each 3D structure will needs its own simplifications as each 3D structure will not excite the same electromagnetic modes.



a. Initial BEOL from the DRM **b. Simplified BEOL for simulation**

Figure II-27 Simplification of the 65nm CMOS process from STMicroelectronics for EM simulation

Figure II-27 shows the simplification we have chosen to make on the 65nm CMOS process from STMicroelectronics for our capacitive coupler. On the left is the initial cross section defined in the DRM [26], and on the right is the simplified cross section which was used in simulations.

ii. T-line structure

Considering the conclusions of the comparison between the different T-line structures which is presented in Annex E section E.1.2, the structure we have chosen to implement is based on the Grounded-CoPlanar Waveguide (G-CPW) of Figure E-1.c.

More precisely, we have used the upper metal layer, M7 in our targeted 65nm CMOS 7 metal layers BEOL, for the signal conductor and the M1 and M2 layers for the ground plane – M1 is a thin metal that is not well suited for ground planes. This way, we maximize the distance between the conductor and the ground plane for the microstrip propagation mode.

Moreover, to respect the density rules imposed by our DRM [26], the two coplanar ground planes have to be stacked on each metal layer. The resulting structure is presented in Figure II-28 where the oxide layers simplifications presented at Figure II-27 are taken into account. The distance between the 2 ground walls (equal to $2*gw+2*g+w$) will be imposed by the respect of the density rules on the metal layers 3 to 6.

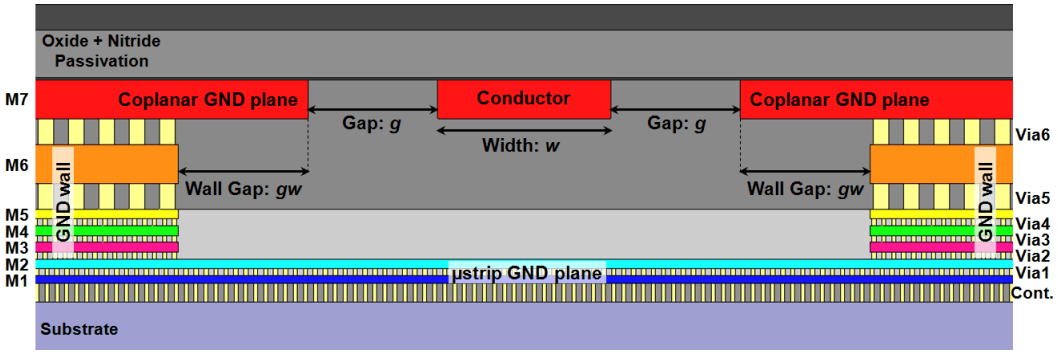


Figure II-28 Cross section of the designed G-CPW

Rather than using a plain metal ground plane below the T-line as in microstrip lines, it has been chosen to concentrate the return current loop into the coplanar ground walls. Metal beams hence replaces the plain metal ground plane of the microstrip mode in order still to ensure a perfect matching (symmetrical repartition) of the reference voltage of the two ground walls as it will be visible on the 3D view of Figure II-29.

For a given structure, we can vary several parameters. The width *W* of the T-line has to be tuned to obtain the desired characteristic impedance Z_c and attenuation constant. However this parameter has also a high impact on the size of the full propagation element. But reducing the *W* will also reduce the maximum current that can flow in the conductor line due to electro-migration issues (these should be respected with respect to the values given in the DRM [26] and for the highest operation voltage).

The best results were found for a T-line width *W* of 8µm, 8µm gap on each side, fully stacked ground walls – no wall gap *gw* in Figure II-28 – and a density of 20% on the ground plane under the T-line. This means the ground beams that connect the 2 ground walls are 2µm large and spaced with a pitch of 10µm. The designed structure is presented in Figure II-29 including via simplifications for the EM simulation (3D view from Ansoft HFSS).

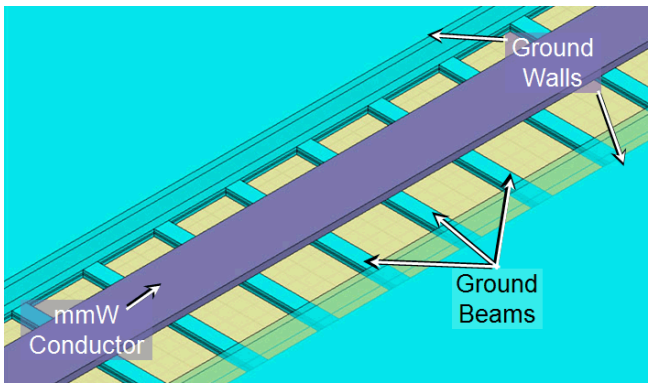
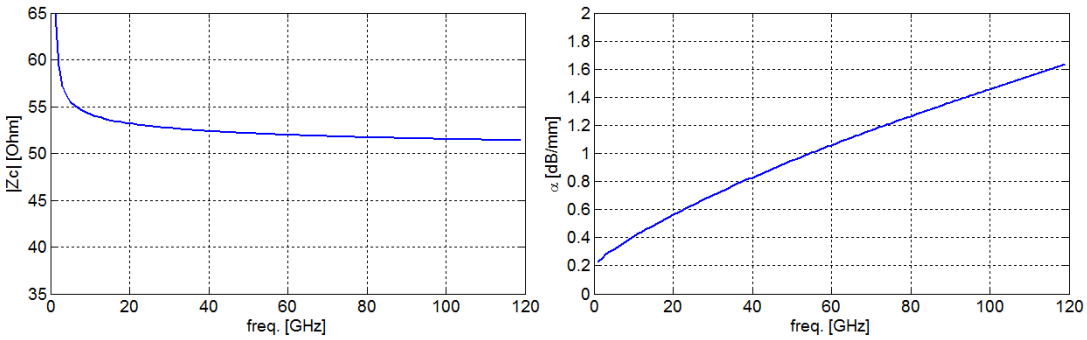


Figure II-29 Designed G-CPW (3D view from Ansoft HFSS)

The simulated (with Ansoft HFSS [21]) characteristic impedance Z_c and attenuation coefficient α of the designed T-line are represented in Figure II-30 (see Annex E for details on the way to obtain those T-line parameters). The characteristic impedance is around 52Ω at 60GHz while the attenuation coefficient is less than 1.1dB/mm at 60GHz.



a. Characteristic impedance **b. Attenuation constant**

Figure II-30 Main characteristics of the designed G-CPW (Ansoft HFSS simulation)

iii. Modeling the T-line

The EM simulations being made in the frequency domain, the resulting S-parameters or the extracted T-line characteristics are also defined in the frequency domain and it is often necessary to build an equivalent electrical circuit of the propagation elements in order to integrate it in circuit simulations performed in the time domain. By using an equivalent circuit, time domain simulations actually overcome the use of complex inverse Fast Fourier Transform (i-FFT) algorithms. This means the equivalent circuit saves a lot of computing time, but also it reduces drastically the unpresision introduced by the i-FFT algorithm as discussed in section E.2.1 of Annex E.

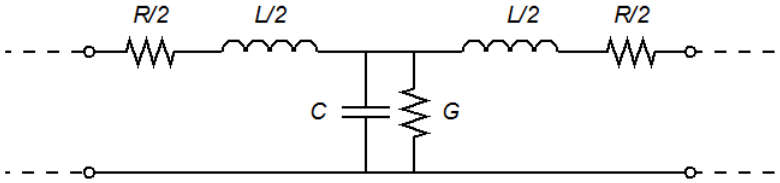
T-line modelization is a well-known technique for RF and mmW designers and will hence not be explained here. However, some details on this technique can be found in Annex E.

The designed T-line is divided into a multitude of section. Each section is considered to be equivalent to the the symmetrical RLCG circuit of Figure II-31.a (see section E.2.3). Distributed *r*, *l*, *c*

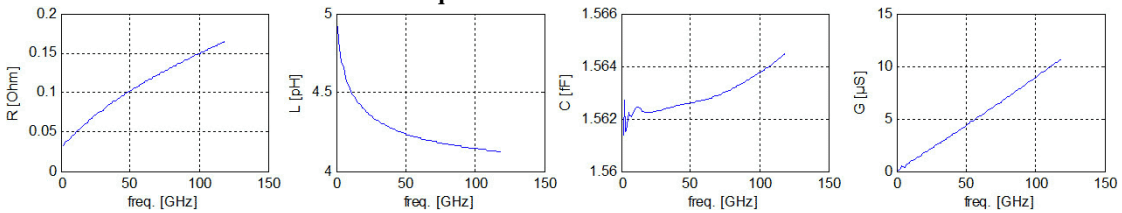
and *g* parameters – corresponding to a division of the T-line into an infinite number of sections – are extracted from the simulated S-parameters and are given at the frequency of 60GHz by the system (II.19).

$$\begin{cases} r = 11.25[\Omega/mm] & c = 156[fF/mm] \\ l = 421[pH/mm] & g = 0.522[mS/mm] \end{cases} \quad \text{(II.19)}$$

Dividing the T-line in 19 sections of 10µm length each (corresponding to one ground beam per section), we can calculate the values of the lumped symmetrical RLCG model. Their frequency dependence is plotted in Figure II-31.b while the values at 60GHz are just the ones given by the system (II.19) divided by a factor one hundred (*1/100* x [*Ω/mm*] = [*Ω/10µm*] and so on for the other parameters).



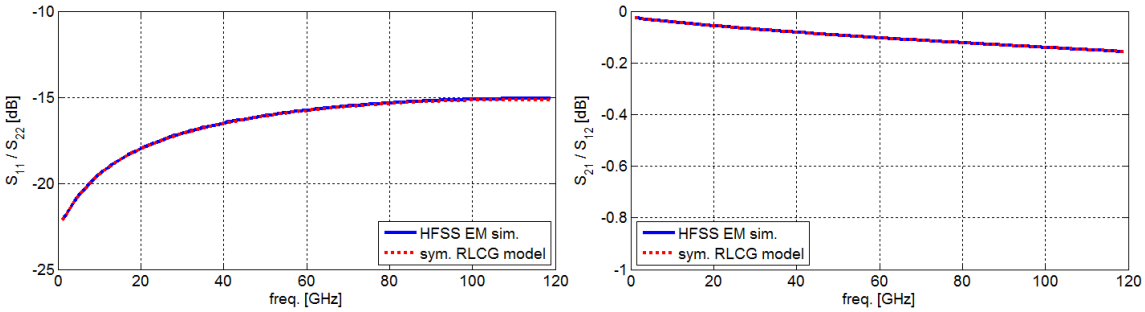
a. Electrical equivalent model for each T-line section



b. Extraxted values for each 10µm length section

Figure II-31 Symmetrical lumped RLCG model

We can now verify our model by doing a simple S-parameters simulation of the passive network obtained and compare with the S-parameter obtained by the HFSS electro-magnetic simulation. This verification is performed using Agilent ADS [27]. The reflection parameters S_{11} and S_{22} are plotted in Figure II-32.a and the transmission parameters S_{12} and S_{21} are plotted in Figure II-32.b. In this case, the model fits very well to the simulation.



a. Reflection S_{11} and S_{22} parameters **b. Transmission S_{21} and S_{12} parameters**

Figure II-32 Comparison between the EM simulation and the symmetrical RLCG model

iv. Structure of the 3D capacitive coupler

The difficulty concerning the capacitive coupler lies in the coupled port mismatch with respect to the usual 50Ω. Furthermore, the parameter we want to adjust is the voltage attenuation – the power detector presented in section II.2.1 needs a voltage input rather than a power one. These are two major constraints for the designer as the simulation results cannot be directly interpreted. Hence the optimization of the coupler performances has to be realized by a loop on the three steps: first the Electro-Magnetic simulation (presented in this section), then the modeling with lumped components (presented in section II.2.2.v), and finally the transient simulation (presented in section II.2.2.vi)

First of all, Figure II-33 shows a 3D view of the designed coupler. As it has already been presented in section II.1.2.iv, a small metal rectangle has been inserted inside the Grounded-Coplanar WaveGuide that has been studied previously. The coupling plane is 8µm large and 7µm long in the 6th metal layer that results in two capacitors, one with respect to the mmW conductor in the 7th metal layer and the other with respect to the ground (beams, walls and substrate). The voltage which is sensed on the coupling rectangle is then transferred to the power detector input through the vias and through the coupler output (1µm large) which is designed in the 2nd metal layer. This coupler output being very close to the ground reference (substrate), it has a very high influence on the capacitors ratio i.e. on the coupler voltage attenuation.

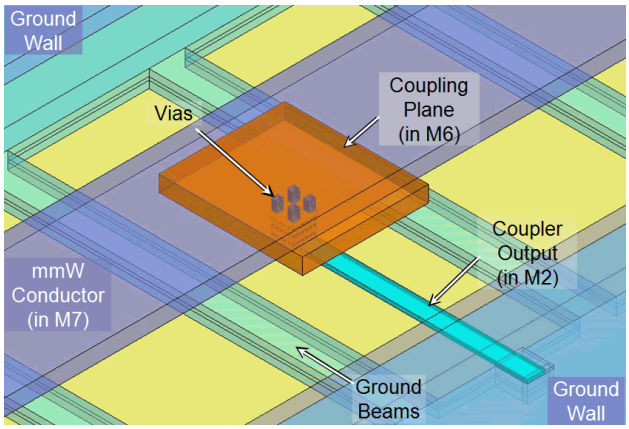


Figure II-33 Designed capacitive coupler (3D view from Ansoft HFSS)

In our solution, the coupling area is very small. Hence the coupling plane has a negligible effect on the transmission line and there is no need for an inductive compensation as in Pfeiffer's solution [8] (see section II.1.2.iv). The electromagnetic simulation results can be seen at Figure II-35 that makes a comparison with the S-parameters of the equivalent model discussed in the next session.

v. Modeling the capacitive coupler

In [8], the capacitive coupler region is modeled using a very simple L-C structure. This model does not include any resistive component. Furthermore, the connection path between the capacitive plane and the detector input is not taken into consideration. This model seems insufficient for us and we have developed our own model of the capacitive coupler region. In practice, we have modeled every contribution that could be shown on the 3D structure of Figure II-33.

First the direct RF path between ports 1 and 2 is still a transmission line. So it will be modeled by an RLCG network as explained in section II.2.2.iii. However, the specificity of this coupler is that the structure is perfectly symmetrical. This symmetry should appear in the equivalent model. Each component has hence been split in two equal parts. The values of the series components (the resistor and the inductance) are divided by two while the values of the parallel components (the capacitor and the admittance) are doubled, thus resulting in the same global values.

In the second time we have considered the capacitive divider induced by the introduction of the coupled plane. Its contribution has naturally been modeled by two capacitors in series. But an admittance has also been inserted in parallel of each capacitor to model the resistivity of the dielectrics. The coupled signal then encountered the vias before being transferred to the detector as can be seen in Figure II-33. The stacked metal and vias can be modeled by a resistance and an inductance in series.

Finally, the connection between the coupler and the detector implemented in the 2nd metal layer as can be seen in Figure II-33 acts as a small propagation line. This contribution is modeled using the methodology explained in Annex E. The propagation length being small in respect to the guided wave length, the structure is divided in only one section where the capacitance and the admittance contributions are divided in two for symmetrical reasons by the same way that for the RF T-line in the 7th metal layer.

The resulting model of the coupler region (10µm length on the RF T-line) is shown in Figure II-34. Each physical contribution has been taken into account, from the RF T-line in M7 (in light-blue) to the T-line in M1 (in purple) through the capacitive divider (in light-red) and the vias (in light-green).

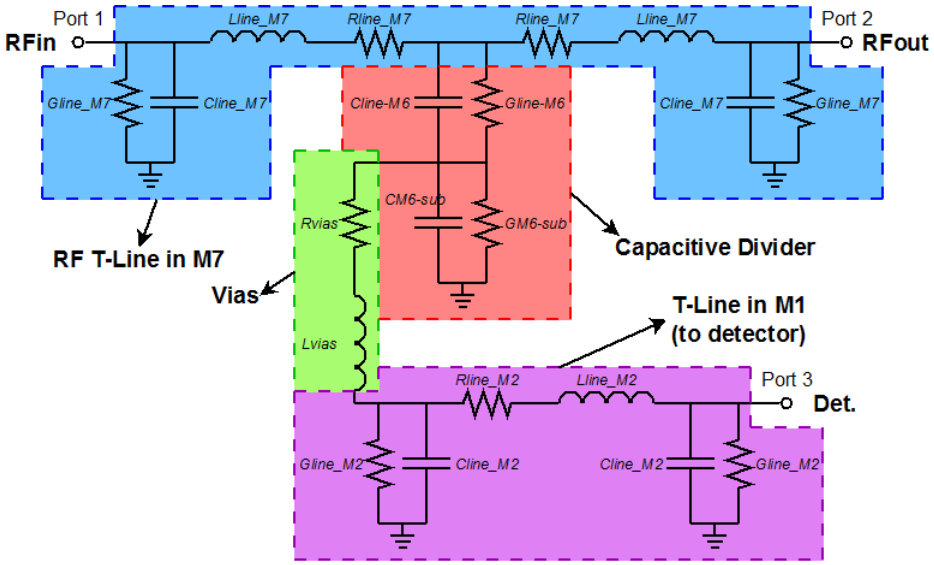
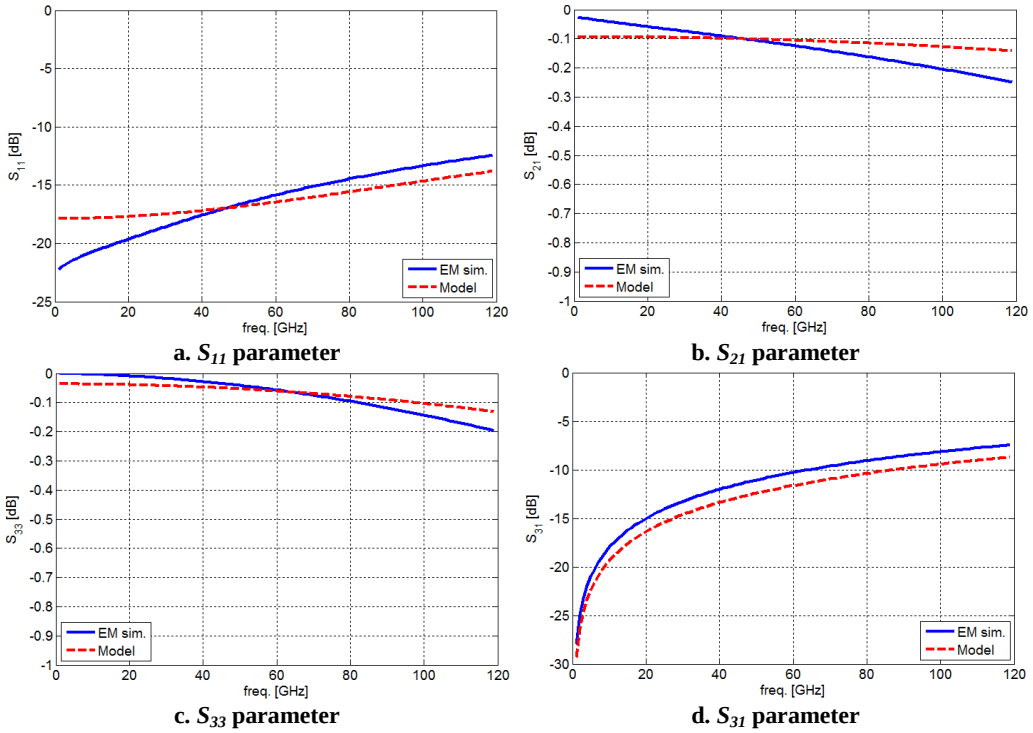


Figure II-34 Equivalent circuit of the capacitive coupler region which was used in the time domain simulation

The value of each component of Figure II-34 is indicated on the equation (II.20) for 60GHz frequency.

$$\begin{cases} R_{line\,M7}=0.1125[\Omega] & G_{line-M6}=5[\mu S] & & R_{line\,M2}=1.8[\Omega] \\ L_{line\,M7}=4.21[pH] & C_{line-M6}=3.69[fF] & R_{vias}=0.3[\Omega] & L_{line\,M2}=5[pH] \\ C_{line\,M7}=0.96[fF] & C_{M6-sub}=0.6[fF] & L_{vias}=0.1[pH] & C_{line\,M2}=0.5[fF] \\ G_{line\,M7}=5.22[\mu S] & G_{M6-sub}=5[\mu S] & & G_{line\,M2}=37[\mu S] \end{cases} \quad \text{(II.20)}$$



a. S_{11} parameter **b. S_{21} parameter**

c. S_{33} parameter **d. S_{31} parameter**

Figure II-35 Comparison between the EM simulation (HFSS) and the RLCG model

Figure II-35 shows the S-parameters comparison between the electro-magnetic simulation (plain lines) and the equivalent model of Figure II-34 (dashed lines). This comparison is made using Agilent ADS software [27]. The values presented in the equation (II.20) were optimized to obtain the best fit to the EM simulation results simultaneously on the S_{11}, S_{21}, S_{33} and S_{31} parameters at 60GHz. In the implemented model, those values have no frequency dependence.

Figure II-35.c highlights the mismatch on the 3rd port, the coupled output noted *Det.* on the Figure II-34. This port is actually not designed to match with the 50Ω characteristic impedance of the S-parameters, but to be a high-Z that well connects to the detector cell input.

vi. Transient simulations

The capacitive coupler equivalent circuit can now be simulated in the time domain. A transient analysis of the schematic shown in Figure II-36 has been performed using Agilent ADS software [27]. The coupler model of Figure II-34 has been integrated between two T-line RLCG model each composed by 9 sections. In this simulation, the 3rd port of the coupler has been charged by the detector cell input impedance, a 200Ω resistance in series with a 1.87fF capacity. This capacity is in the same range that the ones integrated in the coupler model (see Figure II-34 and equation (II.20)) and hence has a very high influence on the attenuation voltage.

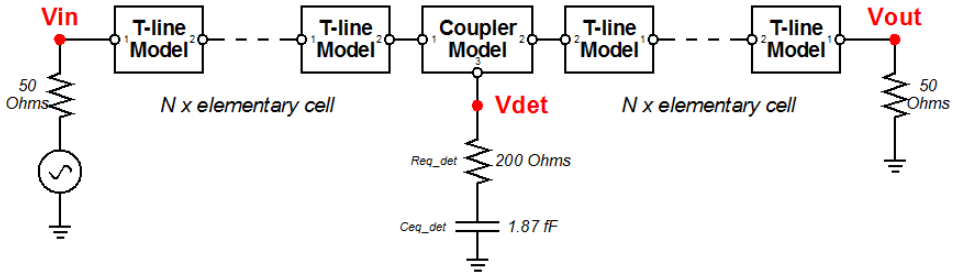


Figure II-36 Schematic of the transient analysis of the coupler model

The results of the transient simulation are given by the wave forms of Figure II-37. The ratio between the voltage transferred to the detector V_{det} and the input voltage V_{in} gives the voltage attenuation coefficient of the structure.

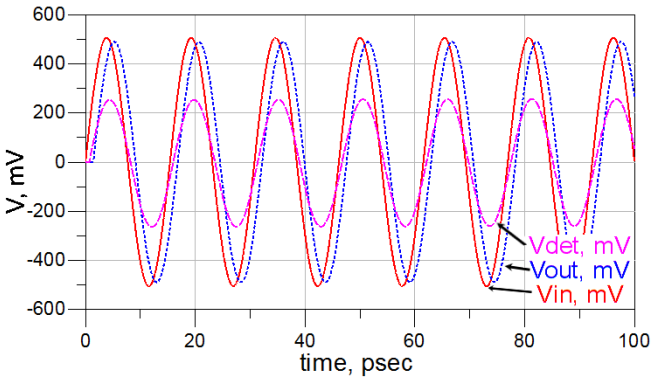


Figure II-37 Input, output and detector voltages resulting from the transient analysis of the Figure II-36's schematic

In our case, the optimization procedure has permitted to obtain a 0.54 voltage attenuation coefficient. Speaking now in terms of power, the voltage is squared and the power attenuation coefficient is 0.297 or -5.3dB on a more significant scale. This power attenuation coefficient is different than the -10dB of the S_{31} parameter (see Figure II-35.d) as it does not correspond to the real power ratio between the coupler output and input; but it corresponds to the significant coefficient of the power coupler that should be taken into consideration on the system level. The detector cell input voltage was also expressed in terms of power – noted P_{ac} – in section II.2.1.

II.3. Circuit physical implementation for testability

The power detector and power coupler presented in the previous section have been implemented on a test chip in order to verify the functionality of the power detector before using it in a regulation loop (see Chapter IV). The circuit realization should hence validate the electromagnetic simulations of the capacitive coupler (section II.2.2) and prove that the power detector circuit effectively works at 60GHz as seen in the simulations of section II.2.1.

However some precautions have to be taken in order to be able to test the circuit and some adjacent components have to be implemented together with the power detector and the power coupler which are the "useful" part of the final circuit. Some de-embedding structures have also to be implemented in addition to the final circuit to be able to deduce the desired characteristics on the useful part of the circuit from the full circuit measurements. Those elements are detailed in Annex F while the most critical things are discussed in this section.

II.3.1. Circuit synoptic

Figure II-38 shows the synoptic of this circuit implementation. The differential detector is integrated between the two couplers. Each coupler is integrated inside a coplanar wave-guide (CPW) transmission line (T-line). A buffer is necessary to amplify and convert the detector output current into a voltage that can be sensed by measurement equipment with 50Ω input impedance as introduced in section II.2.1.iii.

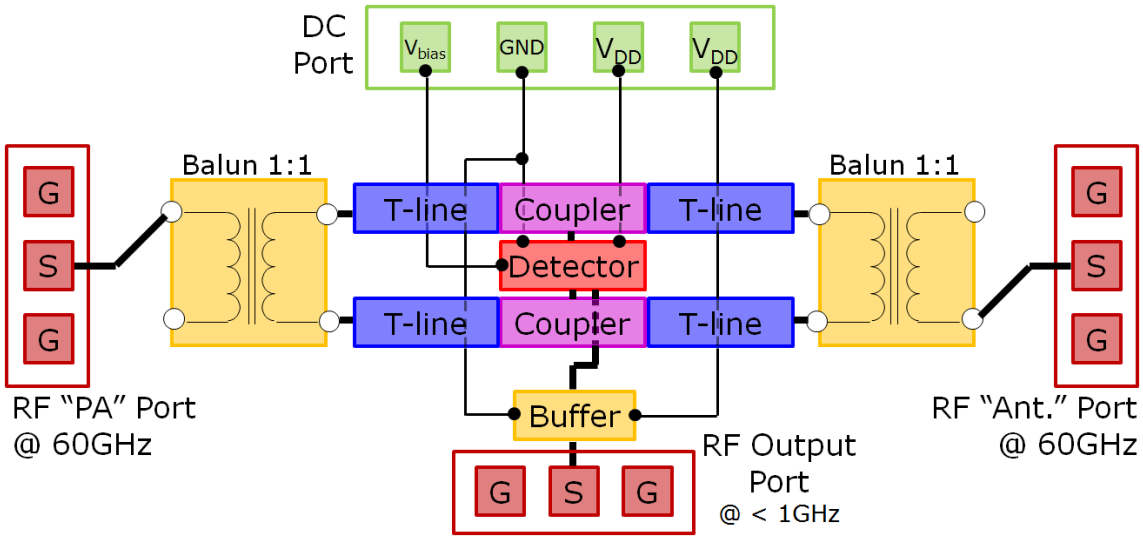


Figure II-38 Power detection circuit synoptic

Differential probes and measurement equipment working properly at 60GHz were not available in our laboratories at the date of this circuit implementation. Hence differential to single-ended baluns were integrated to connect the differential T-line – composed of two single-ended lines – to the measurement equipment.

II.3.2. Circuit implementation

i. Power couplers & power detector

The main part of the chip is composed of the power detector and the two power couplers. Each component has been studied in detail in sections II.2.1 and II.2.2. They are not going to be presented here again. However the co-integration of those three blocks together is specific and needs some explanations.

The connections between the coupled port of the capacitive couplers and the detector, called V_{ac}^{+} and V_{ac}^{-}, work at 60GHz. So the length of those two paths should be minimized in order to minimize the influence on the mmW signals (see section II.2.2.v). Hence, the detector should be the nearest as possible of the two couplers. Furthermore, the architecture is differential. This means the length of the two paths V_{ac}^{+} and V_{ac}^{-} should be equal. So the detector should be integrated between the two couplers.

The detector has hence been designed to respect those considerations and has been integrated inside the ground wall between the two transmission lines which integrate the capacitive couplers. In this way the constraining CMOS 65nm technology design rules [26] are precisely respected.

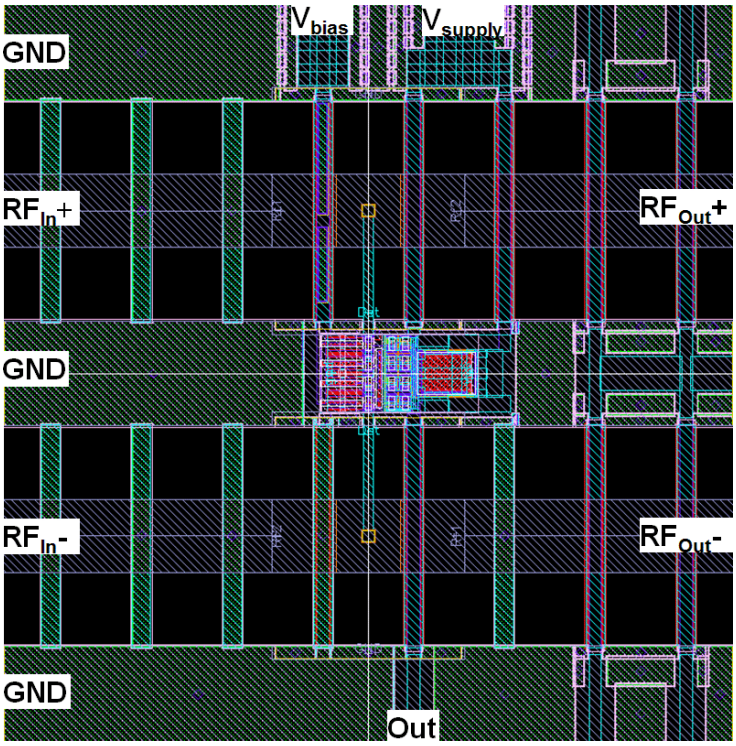


Figure II-39 Power couplers and detector layout

Figure II-39 shows the resulting layout of the power detector integrated between the two capacitive couplers. The total surface of this "useful circuit" is 80x80µm². The entire additional surface used by this circuit is requested by the measurement setup.

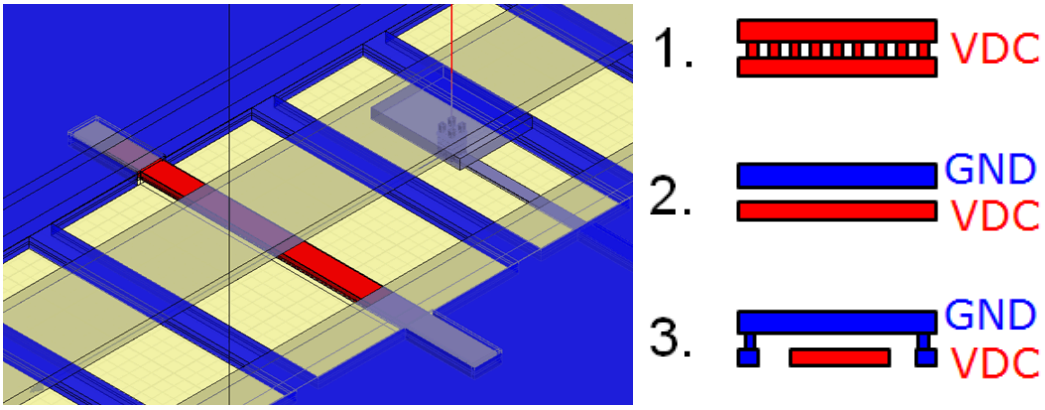
ii. DC connections under the T-line

The supply and biasing voltages and the output current of the detector cell have to be connected respectively by two pads and by the buffer. Those DC (or low frequency) connections should hence pass through the T-lines as can be seen in Figure II-39. A special care has hence been applied during the design of those DC and low-frequency connections.

The structure of the transmission line is detailed in section II.2.2.ii. The coplanar waveguide is composed of a signal path in the thick 7th metal layer, and two ground walls which are connected together by regularly spaced ground beams in the 1st and the 2nd metal layer. Adding some piece of metal to transfer the supply and the biasing voltages from the pads to the detector circuit would affect the wave propagation in the T-line. The only possibility not to deteriorate the characteristics of the T-line is to integrate those DC connections inside the ground beams. In this way the DC signal (or low-frequency) flowing in a beam of the T-line structure is seen as a ground by the RF or mmW signal that flows in the T-line. Hence the T-line structure is not affected by the change in the use of the beam.

Figure II-40.a shows a 3D view of the T-line when one ground beam (in red on the figure) is used to transfer a DC signal. The beam which is used for this specific function can be very closed to the capacitive coupler, as can be seen in Figure II-40.a.

The DC signals that need to be transferred into the beams are a supply voltage and a biasing voltage that have to be purely continuous. So the influence of the mmW signal flowing into the T-line on those DC voltages has to be minimized. Three beam structures have been studied. The first solution is to use the same beam structure that is used for ground connections which is composed by the 1st and the 2nd metal layers connected together by vias. The second solution is to disconnect the two metal layers and use only the lower one for the DC voltage path. The upper metal layer is connected to the ground working as an electro-magnetic screen between the DC path and the T-line signal path. The third solution is to cover each side of the DC path by a ground EM screen. The substrate can also be connected to the ground forming a kind of pipe for the DC signal. Figure II-40.b shows the beam profile of those 3 studied solutions.



a. 3D view from Ansoft HFSS **b. 3 possible profiles**

Figure II-40 DC connection under the T-line

S-parameters simulations were performed using Ansoft HFSS software considering four 50Ω ports (the capacitive coupler represented in Figure II-40.a was not considered during this simulation). The 60GHz signal attenuation between the T-line path and the beam DC voltage path was found to be -35.4dB for the 1st structure, -50.5dB for the 2nd and -76.5dB for the 3rd one.

The 3rd solution clearly appears to be the best one considering only this criterion. However, working with a constant 2µm beam width in the two lower metal layers, the DC signal path section (metal height x line width) is highly reduced in the 3rd solution with respect to the 1st solution as highlights Figure II-40.b. Considering the 24µm length of the beam – which is the distance between the two ground walls – the resistance of the beam is hence equal to 0.68Ω in the 1st structure, 1.98Ω in the 2nd one and 3.55Ω in the 3rd one. All those results are summarized in Table II-3 where CO stands for the contact layer (between the 1st metal layer and the substrate), M1 and M2 respectively for the 1st and the 2nd metal layers, and Via1 for the via connection between those two metal layers.

		Metal width in [µm]							max. I_{dc}	DC line resistance	Coupling @ 60GHz
		CO	M1		Via1		M2				
		GND	GND	VDC	GND	VDC	GND	VDC	[mA]	[Ω]	[dB]
Str. Nb.	1	-	-	2	-	2	-	2	9,64	0,68	-35,4
	2	-	-	2	-	-	2	-	4,3	1,98	-50,46
	3	0,5	0,5	1	0,5	-	2	-	2,13	3,55	-76,48

Table II-3 Summary of the simulation results of a DC connection under the T-line

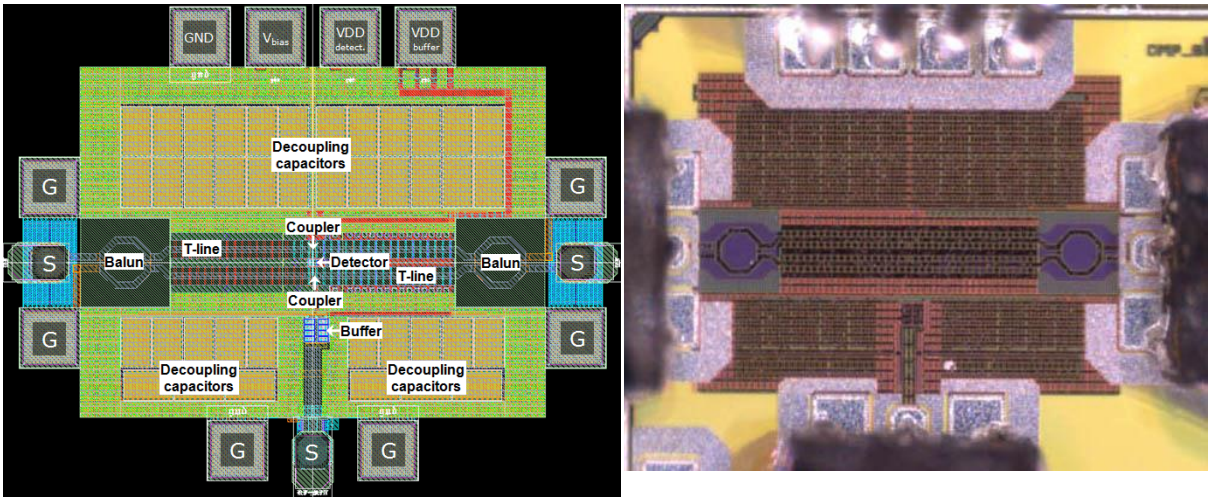
In this test chip implementation, we have chosen to optimize the quality of the DC links by minimizing the coupling factor with respect to the mmW T-line. We have hence implemented the 3rd solution. The high level of resistance issue has been overcome by increasing the number of parallel beams used for each DC link.

iii. Pads

The chip has two mmW ports on the east and west sides (for 60GHz signals), one RF port on the south side (for the buffer output), and a DC port on the north side. This ports distribution, illustrated in Figure II-38, is set to be compliant with measurement benches. The mmW and RF ports are designed for ground-signal-ground probes (GSG) with a 100µm pitch. The DC port is composed of 4 pads designed for a DC probing rake with a 100µm out pitch. The DC pads are attributed, from the left to the right, to the detector biasing voltage, the ground, the detector supply voltage and the buffer supply voltage. The two supply voltages have been separated to be able to sense the power consumption separately on the power detector and on the buffer.

II.3.3. Full circuit physical implementation

All the individual blocks presented previously in this section and in Annex F have been integrated in the final circuit following the synoptic of Figure II-38. Figure II-41 shows respectively the layout view and the die photograph of this circuit. The circuit including pads occupies 0.54mm² while the core area including the power detector and couplers is only 80x80µm².



a. Layout **b. Die photograph**

Figure II-41 Implemented power detection circuit

This circuit has been integrated in a complete chip called PowDet60G with some de-embedding structures and some back-up solutions in case of a dysfunction or a design error on the main circuit. A single-ended version – which is balun-free – of this power detector circuit has notably been implemented. This complete PowDet60G chip is detailed in Annex F.

II.4. Measurement results

This circuit has been measured in three different phases. First, the passive devices have been characterized in terms of S-parameters thanks to a network analyzer. In a second time, the detector has been characterized considering a linear power sweep in the transmission line and constant load impedance. Finally, load pull measurements have been carried on in order to verify the ability of the detector to effectively detect the antenna impedance variation. All those measurements have been performed at both the IEMN and IMS laboratories, except the high power levels of the power sweep and the load pull measurements that have been performed respectively at IEMN and IMS.

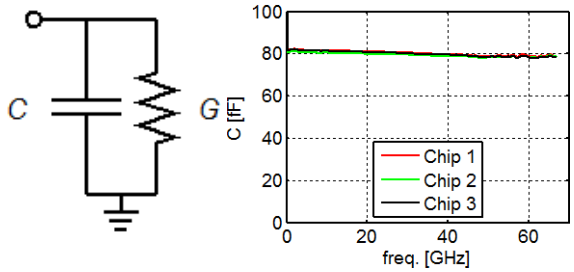
II.4.1. S-parameters

i. Parasitic pad capacitance and balun resonance

The small signal characteristics of passive devices are obtained by performing S-parameters measurements using a network analyzer. The network analyzer has been beforehand calibrated to generate S-parameters de-embedded in the plane of the probes which means that every parasitic effect of the measurement equipment including the cables, the probes, and the VNA itself are taken into account.

However, the additional components integrated to ensure the testability of the chip – such as the pads and the baluns (see Annex F) – are still considered in those measurement results while they are not taken into account in the simulation results as those components are not part of the useful circuit. Their effects have hence been characterized to be able to de-embed the measurement results in order to obtain the characteristic of the useful part of the circuit independently of the measurement environment. Details on this characterization can be found in Annex G with some explanations on the de-embedding techniques.

The effects of the pads can be modeled by a capacitor in parallel with a resistance following the circuit of Figure II-42.a. The value of the capacitor which is extracted from the measurements (see Annex G for details) in around 80fF from DC up to 67GHz as can be seen in Figure II-42.b.



a. Pad model **b. Extracted pad capacitance**

Figure II-42 Pad capacitance effect

This capacitance effect can be easily de-embedded (see Annex G). However this de-embedding generates some erroneous results if the pad capacitance starts to resonates with some inductive components. This is notably the case in our circuit when considering the pad-balun association. The measurement of the single-ended balun de-embedding structure (see Figure F-7 in Annex F) illustrates this phenomenon. Figure II-43 shows the S_{11} and S_{21} parameters that are directly extracted from the measurements and that are de-embedded using two different techniques (see Annex G for details).

Although the two de-embedding techniques generate same range results below 45GHz, the difference becomes very high above 45GHz meaning the de-embedding is not valid anymore. The measured structure actually resonates at around 40GHz.

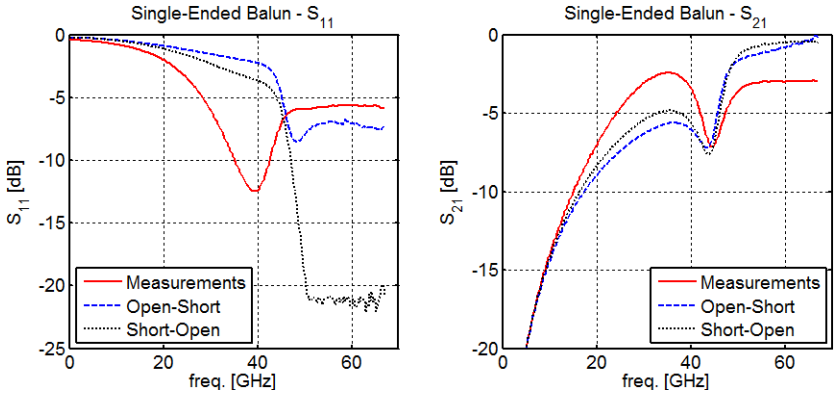


Figure II-43 Single-Ended Balun S_{11} and S_{21} parameters; measured and de-embedded results

The same resonance phenomenon can be observed on the differential balun de-embedding structure (see Figure F-8 in Annex F). Figure II-44 shows the measured and de-embedded results (Open-Short). This differential balun structure, which is close to the power detector circuit, resonates between 40 and 45GHz.

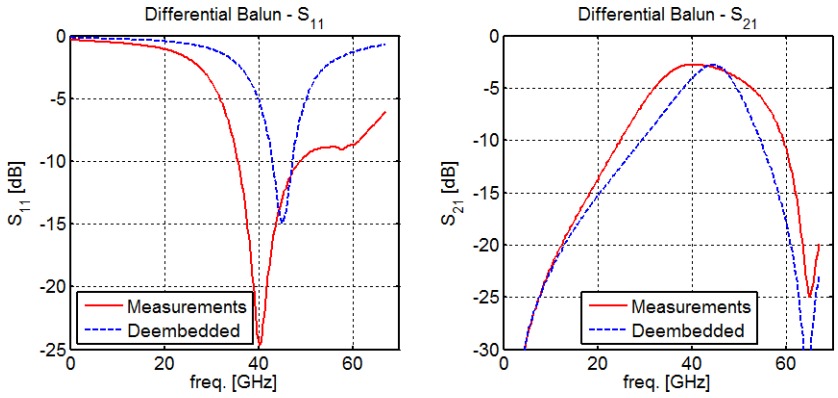


Figure II-44 Differential Balun S_{11} and S_{21} parameters; measurements and open-short de-embedded results

This resonance has not been predicted by the simulations as the pad capacitance has not been evaluated and hence not been taken into consideration. The full power detector of Figure II-41 will hence be very difficult to characterize at 60GHz due to this resonance between the balun and the pad. However, a backup single-ended structure that does not integrate any balun has also been implemented in this chip (section F.2.4 of Annex F). This structure should not present too much loss at 60GHz.

It can be noticed that the Open-Short de-embedding structure being much closer to the physical circuit configuration, this technique will be preferred in the following measurements analysis.

ii. Differential T-line including the detector

The differential detector, presented in Figure II-41, is then characterized. This structure integrates a balun at both ends of the transmission line and hence presents a resonance frequency around 40GHz that corresponds to the balun inductance resonance with the pad capacitance as introduced previously and validated below by the retro-simulations (sub-section iv).

Figure II-45 shows the measured and open-short de-embedded S_{11} and S_{21} parameters obtained for this structure. The structure effectively resonates at 38GHz and presents -3.7dB insertion loss at this frequency while the insertion loss reaches -15.8dB at 60GHz when considering the full circuit not de-embedded.

Those measurement results have been compared with the measurements results of the structure f. of Figure F-6 (Annex F) where no power coupler is integrated beneath the transmission line. Those two structures present so-closed S-parameters results that we have decided not to include it in this thesis. This confirms the power coupler has a negligible effect on the transmission line.

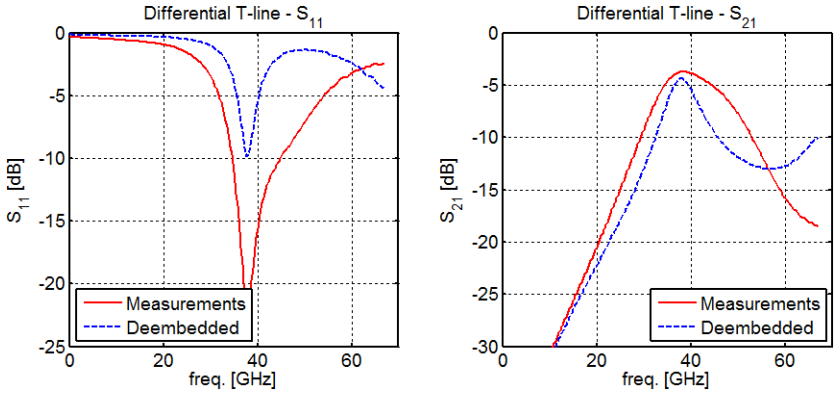


Figure II-45 Differential T-line S_{11} and S_{21} parameters; measurements and open-short de-embedded results

iii. Single-Ended T-line including the detector

The single-ended version of the power detector (structure b. of Figure F-6, Annex F) is measured in order to characterize the transmission line without any perturbing element such as the baluns. This structure integrates a power coupler which has no effect on the T-line as explained above.

Figure II-46 shows the measurements and the open-short de-embedded results of the single-ended detector structure, focusing on the S_{11} and on the S_{21} parameters. The open-short de-embedding of this structure has not been performed using the open and short structures previously used for the balun as those structures integrate some accesses that are not included in this structure.

The open has been obtained here by a small computing of the one-port S-parameter measurement result of the pad alone (see Annex G) in order to obtain a two-port network that integrates an open circuit between two pads. The short has been obtained by a theoretical approach. The pad has actually been modeled by a parallel 80fF capacitor (extracted value from the measurements) and a serial 0.05Ω resistive 23pH inductance (theoretical values of metal resistance and inductance given by the DRM [26]). A short circuit has been integrated between two pad models and simulated as a two-port network using Agilent ADS tools, thus giving the S-parameters of the short structure used for de-embedding.

This de-embedding technique correctly removes the low-pass filter effect created by the pad capacitance as can be seen on the S_{21} characteristics in Figure II-46. The de-embedded structure is well matched to 50Ω as can be seen on the S_{11} diagram and presents about 0.8dB insertion loss at 60GHz.

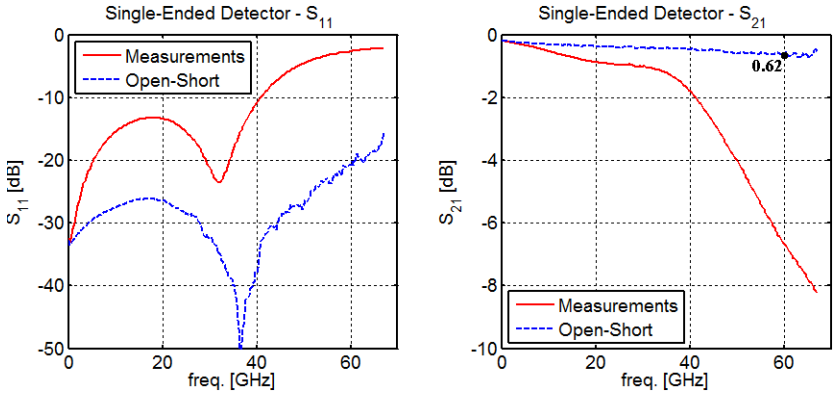


Figure II-46 Single-ended Detector S_{11} and S_{21} parameters; measurements and open-short de-embedded results

The T-line characteristics are then extracted from those de-embedded results following the equations detailed in Annex G and taking into consideration the 640µm length of the implemented transmission line. Figure II-47 shows the propagation constant α and the characteristic impedance of the measured T-line. Those two characteristics extracted from the measurement results are very close to the values obtained by simulation. This validates the different simplifications performed in order to simplify the electro-magnetic simulations (see section II.2.2.i).

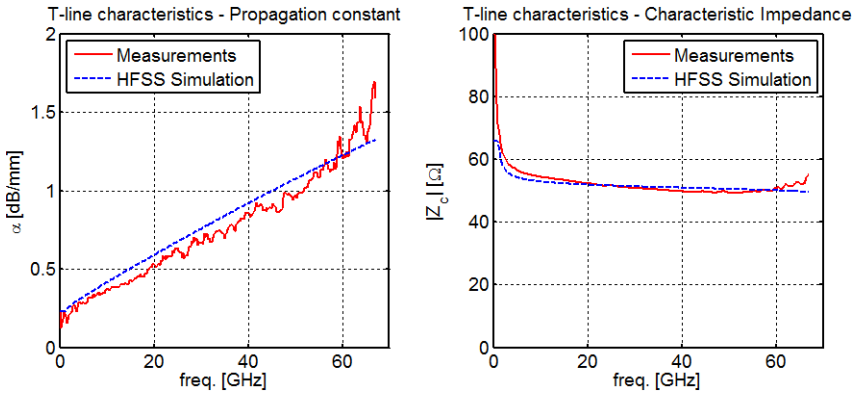


Figure II-47 Single-ended T-line: extracted T-line characteristics

The designed Grounded-Coplanar Waveguide Line (GCPW) is well matched to 50Ω and presents 1.2dB/mm attenuation at 60GHz.

iv. Retro-simulations

Some retro-simulations have been performed in order to verify the origin of the resonance frequency around 40GHz. For those retro-simulations, we have used the S-parameters resulting from electromagnetic simulations (mainly performed with Ansoft HFSS) of the different parts of the circuit (balun, T-line and coupler). The measured S-parameters of the pad have also been used and added on both side in front of the simulated circuit. The circuit has hence been considered as a combination of 2 and 4-port networks (see Annex D) and simulated using Agilent ADS S-parameters simulator.

Figure II-48 shows the cascading of pad, T-line and coupler that has been considered for the retro-simulation of the single-ended T-line circuit.

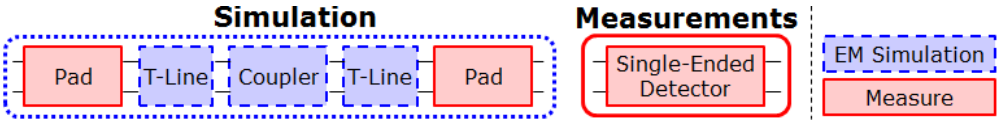


Figure II-48 Retro-simulation configuration for the single-ended T-line circuit

Figure II-49 shows a comparison on the S_{11} and S_{21} parameters between the measurements (plain line) and the retro-simulation (dashed line) results. The measurements results are very close to the retro-simulation results, especially for the S_{21} parameter. Hence, adding the pad capacitance effect to the T-line and coupler chain effectively creates a low-pass filter with a cut-off frequency at about 40GHz.

The small remaining difference between the measurements and the retro-simulation results, especially on the S_{11} curves, is probably induced by the transitions between the pads and the T-line that have not been considered in the retro-simulation.

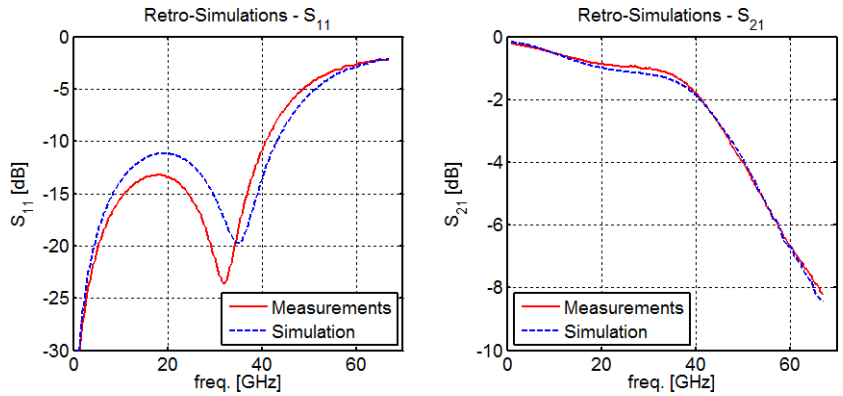


Figure II-49 Comparison between the measurements and the retro-simulation for the single-ended T-line circuit

Similar retro-simulations have been performed for the differential power detector circuit. Figure II-50 shows the different configurations that have been simulated. The first one simply includes the pads, the baluns, the couplers and some T-line elements. The second configuration includes some transition elements between the baluns and the T-lines in addition to the previous configuration. Those two retro-simulation configurations are compared with the measurement results of the differential T-line circuit.

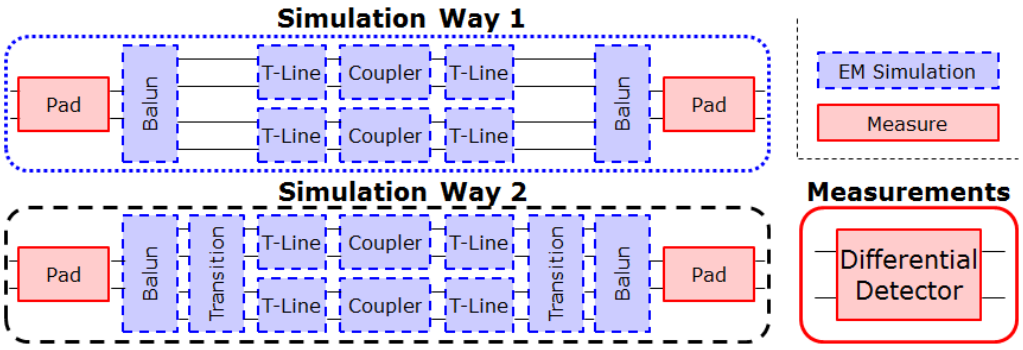


Figure II-50 Two different retro-simulation configurations for the differential T-line circuit

Figure II-51 shows a comparison on S_{11} and S_{21} parameters between the measurements results (plain line) and the two retro-simulation configurations (respectively dotted and dashed lines).

The first observation that has to be made is that the three curves have globally the same shape. As for the retro-simulation of the single-ended T-line circuit, the pad is here effectively the perturbing element that has not been taken into consideration in the simulations during the design phase. Simply adding the effect of the pad actually corrects the shape of the S_{11} and S_{21} curves obtained in simulation.

Now focusing on the difference between the two retro-simulation configurations, it can be noticed that the frequency resonance decreases when considering the transition elements, thus reaching the value obtained in measurements. The transmission elements that are not all taken into account in those simulations (such as between the pads and the baluns) should hence explain the small remaining difference with respect to the measurements.

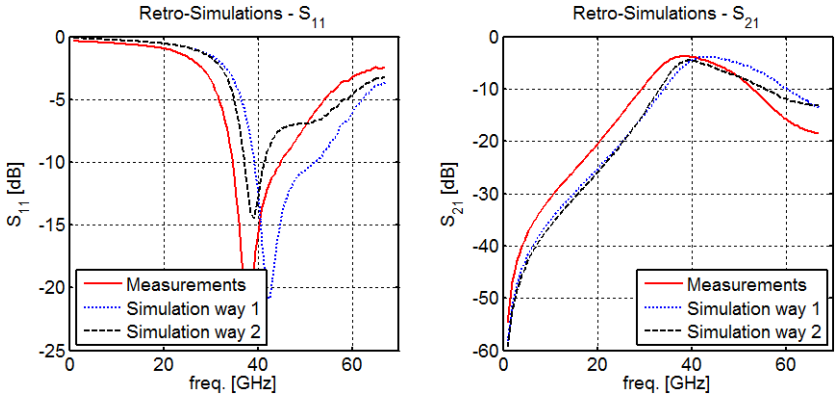


Figure II-51 Comparison between the measurements and the two retro-simulations for the differential T-line circuit

II.4.2. Input power sweep

The two power detector circuits (differential and single-ended) have then been characterized in terms of detection range. In order to characterize the detector behavior, power sweeps on the transmission line have been applied at several mmW frequencies. However a careful de-embedding procedure that will be detailed first has been used on the raw measurement data in order to present the measured detector output voltage with respect to the actual power in a vertical plane on the top of the coupler metal square.

i. Experimental protocol

A 60GHz programmable signal generator (PSG) has been connected at the mmW input of the circuit while the mmW output has been loaded by a 50Ω impedance. The DC power is provided by a voltage generator that automatically collects the consumed current. The supply power is then sent to the device under test via an adequate 4-pins probe. Finally, the detector output voltage is probed on the 4th circuit port and plotted on an oscilloscope. This measurement configuration is illustrated in Figure II-52.

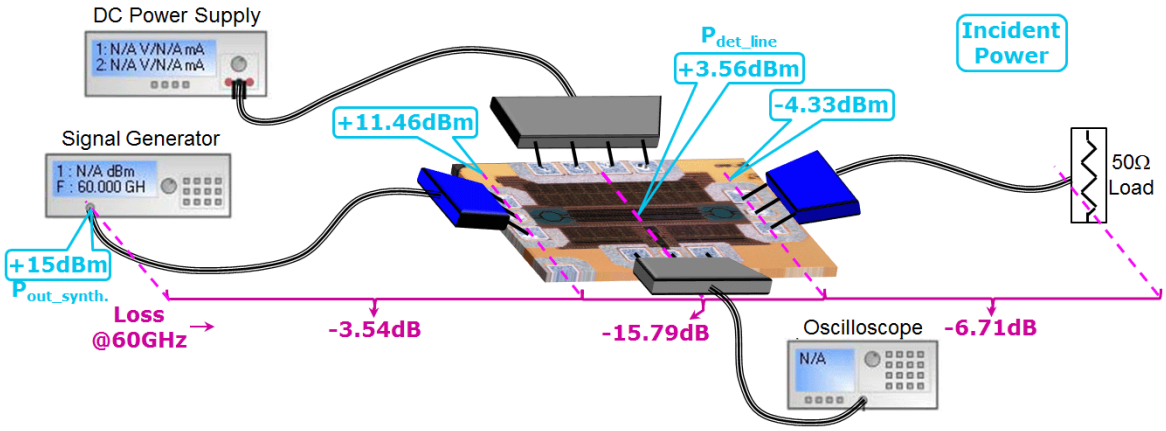


Figure II-52 Differential detector: power measurements test bench

Considering the insertion losses of the cables and probes and of the DUT itself, the power delivered in the T-line in a vertical plane on the top of the coupler metal square, noted P_{det_line}, can be evaluated from the synthesizer output power P_{out_synth} following the equation (II.21) for the differential power detector circuit.

$$P_{\det\_line} = P_{out\_synth} - 11.43dB \qquad \text{(II.21)}$$

Although this de-embedding operation is detailed in Annex G, the different insertion loss contributions have been reported on the bottom of Figure II-52 while an example of power level at different locations of the measurement configuration have been reported on the top of the same figure (the circled values). Considering a +15dBm generated signal at 60GHz, the power level that would be observed by the power coupler on the circuit is only +3.56dBm.

The same de-embedding operation is performed on the single-ended power detector circuit. However the small-signal S_{21} parameter value being quite lower than previously, the resulting power level seen by the power coupler is much higher.

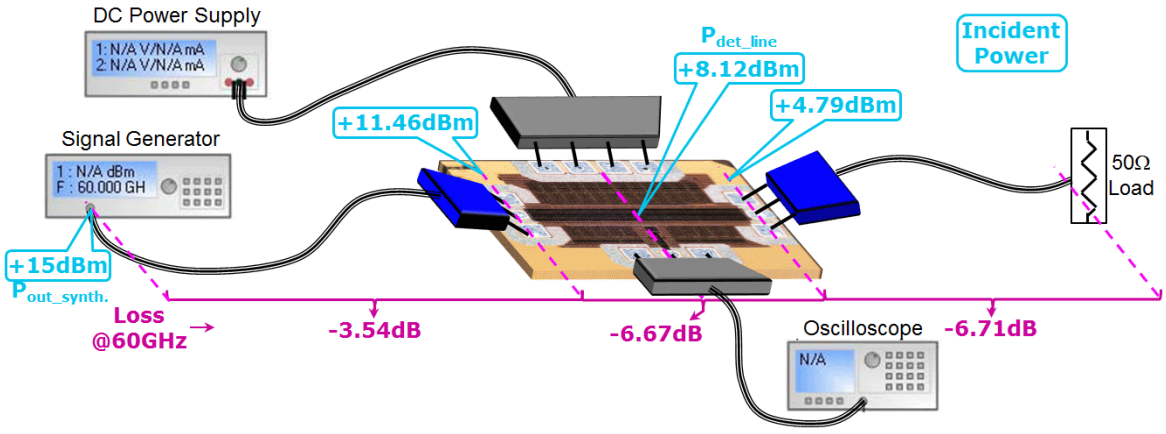


Figure II-53 Single-ended detector: power measurements test bench

Still considering a +15dBm generated signal at 60GHz, the power level that would be observed by the power coupler is +8.125dBm this time, which can be synthetized into the equation (II.21). The new values corresponding to the single-ended circuit are reported in Figure II-53.

$$P_{\det\_line} = P_{out\_synth} - 6.87dB \quad \text{(II.22)}$$

Moreover, the generated power that is indicated on the signal generator is not regulated in real-time inside the equipment and the true generated power that is effectively send to the circuit is quite different to the power level that is displayed on the generator. Those insertion losses are negligible for low power levels but reach -0.84dB for the maximal displayed PSG output power of +15dBm (see Annex G). They have hence been taken into consideration in the following measurements results.

ii. Differential power detector

A power sweep has been applied on the differential power detector circuit (see Figure II-41). Two different chips have been measured in two different biasing conditions. First the supply voltage is fixed to the nominal value of 1.2V and the bias voltage V_{bias} to 666mV, which corresponds to the simulated conditions. Then the supply voltage is increased to 1.3V and the bias voltage is decreased to 500mV. Figure II-54 shows the de-embedded measurement results.

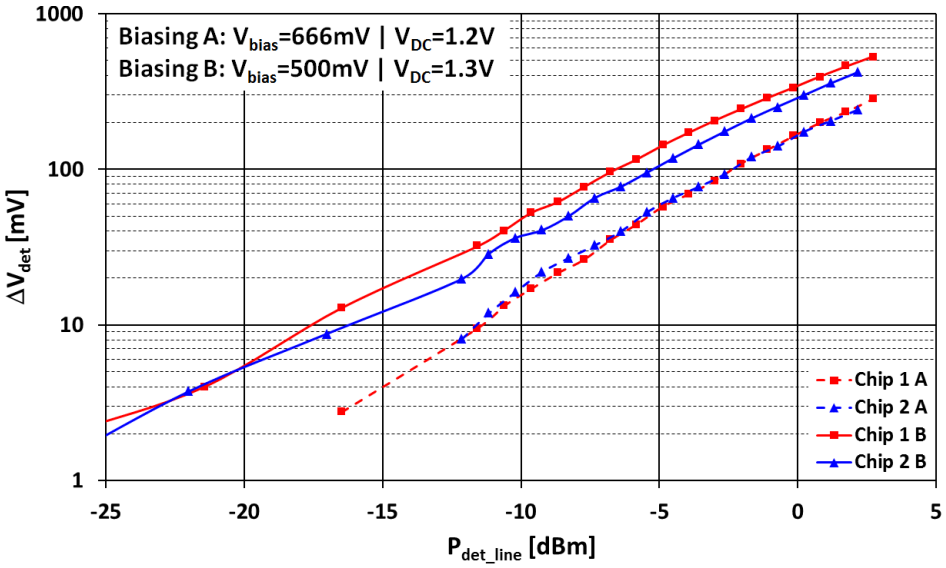


Figure II-54 Measured characteristic of the differential power detector circuit (de-embedded results)

The differential power detector circuit provides more than 25dB linear detection range, the measurements being limited by the equipment capability. The biasing conditions generate an offset between the characteristics and can be used to tune the detection range of the circuit to the desired power level range.

Some additional measurements have been carried out to increase the power level at the input of the power coupler. For those measurements, the PSG has been replaced by a GUN diode connected to a tunable attenuator that both have been characterized using an external bolometer. This new test configuration provides 4dB more gain, thus reaching +6.32dBm power level in the vertical plane of the coupler.

A complete power sweep has been performed from -20dBm up to +6.32dBm in order to correlate the measurement results to the results obtained using the PSG. This correlation is very satisfying as can be seen in Figure II-55. Moreover, the power detector effectively continues to present an almost linear characteristic; but the global shape of the curve is not purely linear and presents a progressive bending that can correspond to the buffer response which is not fully linear (see section II.2.1.iv).

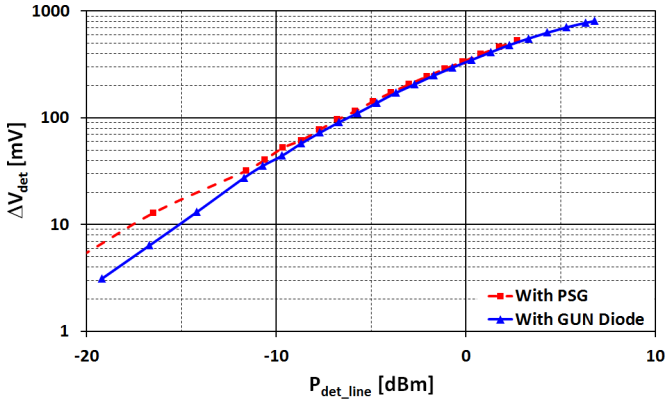


Figure II-55 Differential power detector: power characteristic for high power levels

Electrical tests as those presented in Figure II-54 have been carried out for T-line input signals in the frequency range from 30GHz up to 65GHz with 5GHz steps, and similar voltage detection capability has been observed. Those measurement results are reported in Figure II-56 for reference only.

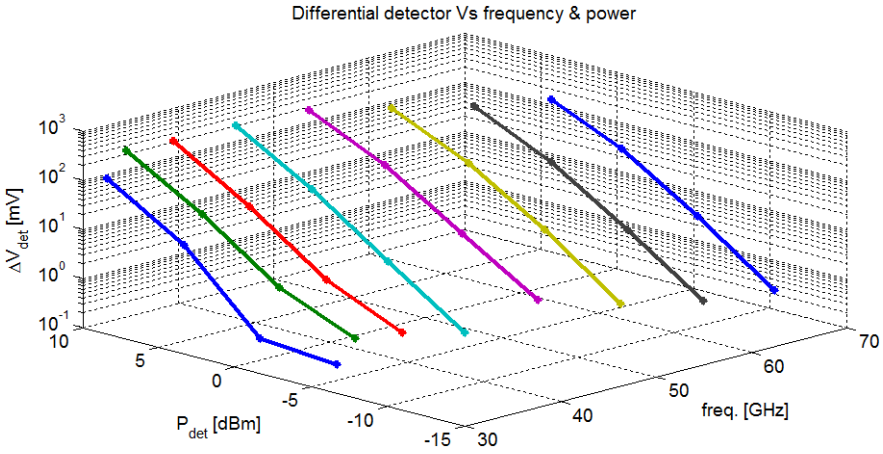


Figure II-56 Differential power detector: power characteristic for different frequencies

The circuit consumes less than 35mA including the output buffer and less than 55µA without the output buffer, both considering a 1.2V supply.

iii. Single-ended power detector

The same measurements have been performed on the single-ended power detector (structure b. of the Figure F-6 in Annex F). Two chips have also been tested in the two same biasing conditions. Figure II-57 (next page) shows the results of those measurements.

The linear detection range for the single-ended detector is higher than 20dB, and here again, the maximum available power level is limited by the test equipment.

The higher power level at the detector input compensates the lower gain of the detector that should be observed between the differential and the single-ended versions of the power detector. However, for both differential and single-ended detectors, it is very complicated to compare the measurement results with the simulations as the power level at the input of the coupler cannot be directly measured.

Nevertheless, it appears that the measurement results (summarized in Table II-5) are a little better than the simulations had predicted for both differential and single-ended configurations. This can be explained, as introduced in section G.3.3 of Annex G, by the consideration that has been made

for de-embedding the measurement results that the detected power was only composed of the incident power coming from the PSG. It appears hence that some wave reflections on the baluns and pads increased the detected power, thus artificially increasing the performance of the detector circuit. However this hypothesis cannot be verified as the true power level at the coupler input cannot be determined precisely.

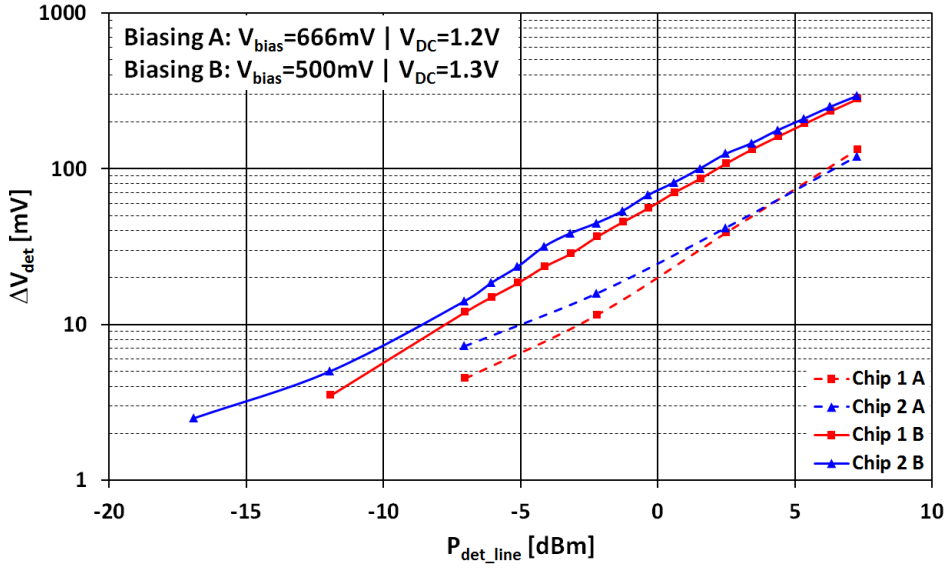


Figure II-57 Measured characteristic of the single-ended power detector circuit (de-embedded results)

II.4.3. Load-pull measurements

Finally, source and load pull measurements have been carried out on the circuit and will be presented first by detailing the experimental protocol, then by presenting the detector characteristic with respect to the load impedance applied at the circuit output, and finally by showing the optimized power transfer at both input and output of the circuit using the source and load pull tuners.

i. Experimental protocol

All the load-pull measurements presented in this thesis have been carried out in the IMS laboratory using Focus Microwaves equipment. This test bed is composed as detailed in [28] and illustrated in Figure II-58 (where the isolator and attenuator are not represented). The references and specifications of the equipment are listed in Table II-4. The different equipment are connected through GPIB to a controlling computer that automatically de-embeds – after a calibration procedure – the power levels to display the DUT input power P_{in_DUT} and the DUT output power P_{out_DUT}.

Function	Equipment reference	Specifications
Sinusoidal signal generator	Agilent PNA E8361A	10MHz-67GHz
Input power amplifier	SP6010-30-20W	37dB Gain, 17dBm OCP1
Coupler	CL3-12-R1000	10dB
Isolator	FBI-12-RSES0	
Source and load-pull tuners	Focus iCCMT-75500	Freq. 55-90GHz
Variable attenuator	LSA-12-5000	From 0 to -25dB gain
Power meter	HP EPM-441A & EPM-437A With Agilent V8486A probes	Range: -30 / +20dBm Freq. 50-75GHz
DC power supply	HP E8631A	
Multimeter	HP 34401A	

Table II-4 Refereces and specifications of the load-pull measurement equipment

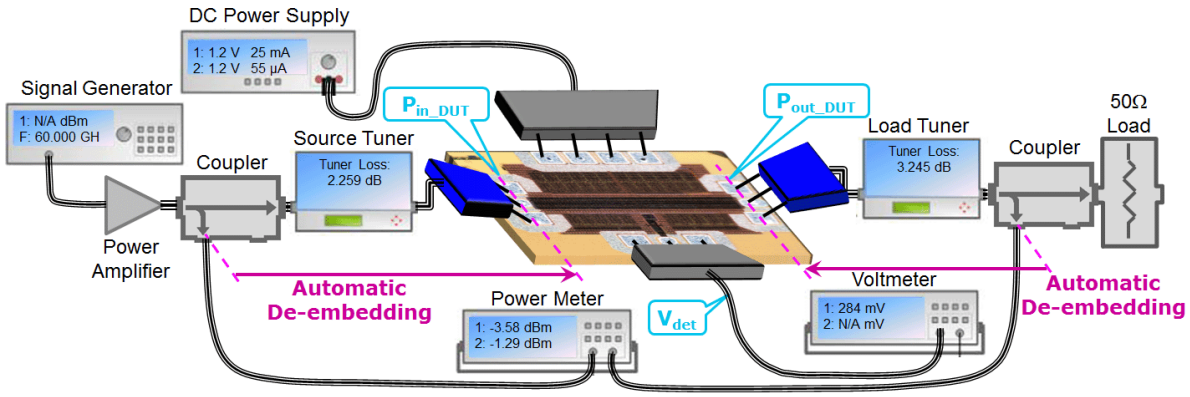


Figure II-58 Load-pull measurements simplified test bench

As can be seen on the synoptic of Figure II-58, three parameters are measured simultaneously which are the DUT input and output power levels, respectively P_{in_DUT} and P_{out_DUT}, and the detector output voltage V_{det}. However, the P_{in_DUT} is regulated by the controlling computer to present an almost constant power level at the input of the DUT and hence characterize the DUT independently of the applied source and load impedances. This parameter will hence not be considered directly but will be computed with the P_{out_DUT} following the equation (II.23) to build the gain which is more suitable to characterize our DUT. We have hence two ways to characterize our device which are first to calculate the gain of the DUT and then to measure the detector output voltage V_{det}.

$$Gain = P_{out\_DUT} - P_{in\_DUT} \tag{II.23}$$

Due to some difficulties to establish a correct contact between the probes and the pads during the measurement of the differential power detector circuit, only the single-ended detector results are going to be presented here.

ii. Load-pull measurements results

The first tests that have been performed are typical load-pull measurements. The source tuner is fixed and presents a constant 50Ω source impedance. The load impedance is progressively tuned to cover a certain portion of the Smith chart which is unfortunately limited to about 3:1 VSWR by the measurement equipment (such as cable losses, maximum linear range of the power source and the amplifier …). In our implementation, tuning the load impedance is equivalent to create an antenna impedance variation at the end of the transmission line within which the power level is measured by our detector.

Figure II-59 shows the circuit's gain with respect to the complex impedance variation at the T-line output on the single-ended test chip. Those results have been obtained for a 60GHz sine-wave input signal with about -2.5dBm power level at the input of the DUT (P_{in_DUT}). The DUT gain varies from about -10dB up to -3.7dB following the color code defined on the right of the figure which is linked on the diagram to the minimum and maximum values obtained for 0.43 reflection coefficient magnitude and respectively -90° and +90° reflection coefficient angle. The maximum gain is hence obtained for a mostly inductive load impedance that corrects the capacitive effect of the pad.

For a 50Ω load impedance – at the center of the abacus – the gain measured in this experimental configuration fits to the -6.5dB S_{21} parameter measured previously at 60GHz during the small-signal circuit characterization (see section II.4.1.iii). Still having only passive components on the RF path, the small signal S_{21} parameter is once again equal to the large signal gain what is verified here by the experimentation.

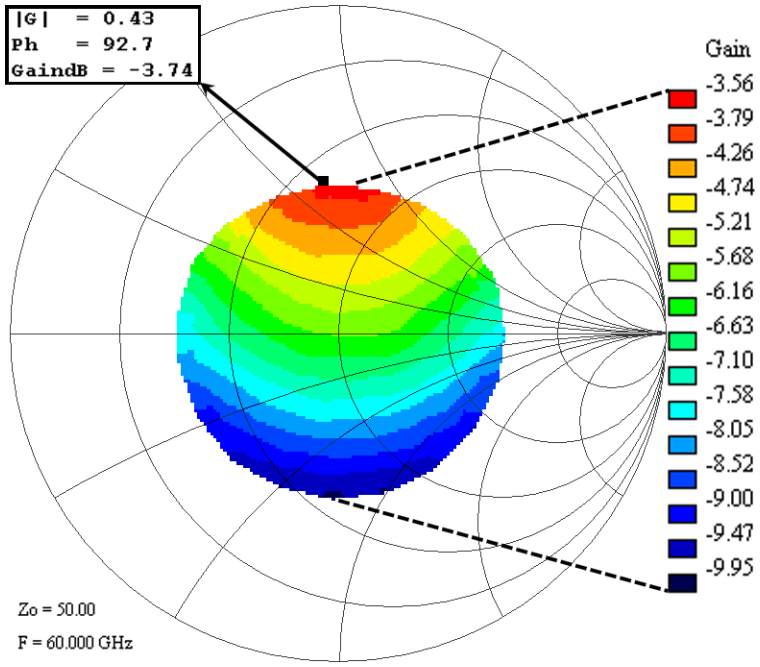


Figure II-59 Single-Ended detector gain with respect to the load impedance (Load-pull measurements)

Keeping the same measurement configuration illustrated in Figure II-58, the gain which was the observed parameter in the previous experiment is now replaced by the detector output voltage. Figure II-60 shows the detector output voltage with respect to the complex impedance variation at the T-line output on the single-ended test-chip. This voltage varies from 0.31V up to 0.41V following the color code specified on the right of the figure (the number of displayed digit was erroneously trunked by the controlling software but can easily be interpolated) and reported on the diagram itself. The minimum and the maximum voltages have been measured for 0.45 reflection coefficient magnitude and for respectively 30° and 140° reflection coefficient angles. Both correspond to an inductive impedance what is concordant to the previous measurement results as the pad capacitance has to be compensated before performing a load pull directly at the T-line output.

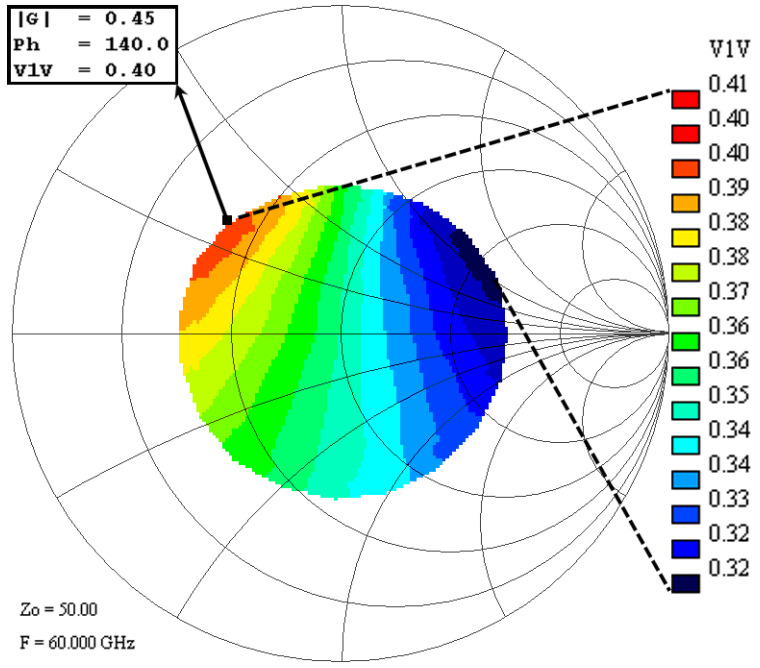


Figure II-60 Single-Ended detector output voltage with respect to the load impedance (Load-pull measurements)

We can hence get rid of this pad effect and consider now the detector voltage distribution with respect to the load antenna while keeping in mind that the maximum gain was obtained previously for a 0.43 magnitude and 90° angle reflection coefficient.

First this real-time experimentation demonstrates the ability of the implemented circuit to reveal at least 3:1 VSWR impedance variation on the T-line load which is our targeted application.

Then this detector output variation can be correlated to the standing wave formation introduced in sections I.3.1 and I.4.2.ii. For 50Ω load impedance, no or few standing wave is actually created and the observed voltage is in the middle of its dynamic range. But when the magnitude of the reflection coefficient Γ increases, a standing wave appears in the T-line and the power level measured by the detector – so the detector output voltage – increases or decreases depending of the phase of the reflection coefficient. The measured diagram of Figure II-60 is hence similar to the diagrams obtained in theoretical simulations and presented in Figure I-31, the impedance offset to the inductive zone being still considered.

iii. Source and load-pull optimization

We have then performed a source pull measurement, still working on the single-ended detector circuit. The source tuner being now fixed to the best impedance that compensates the capacitance effect of the input pad, which is mostly inductive, a classical load pull measurement is performed. Figure II-61 shows the new gain diagram obtained for the optimized source impedance.

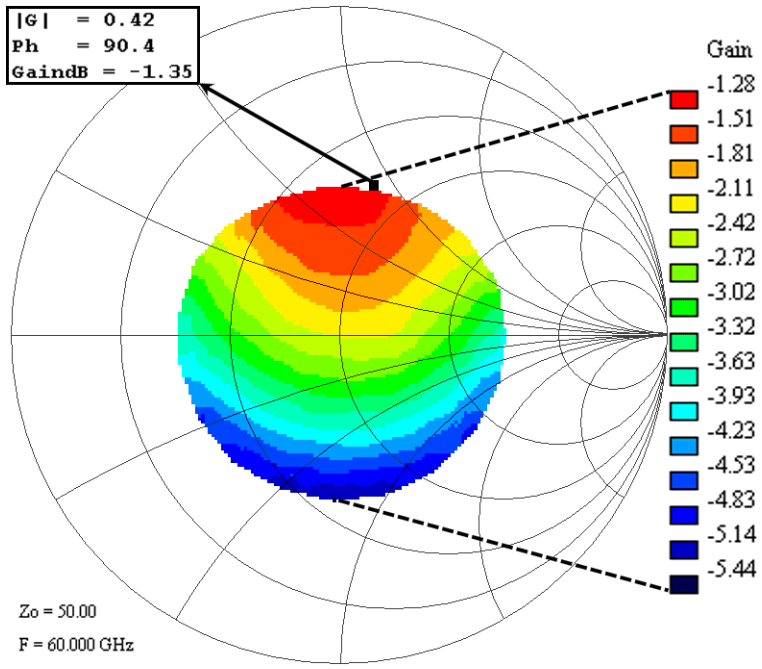
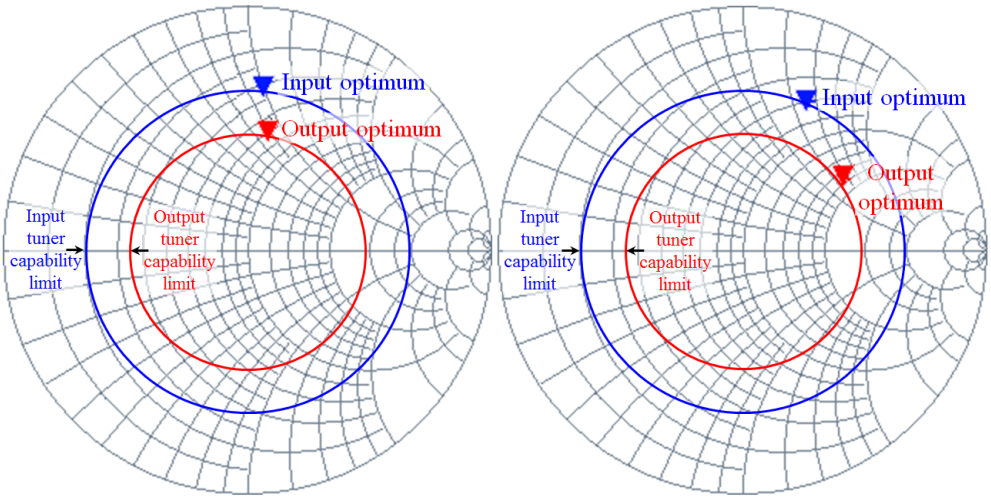


Figure II-61 Single-Ended detector gain with respect to the load impedance with optimized source impedance

The gain now reaches -1.35dB and is still obtained for inductive load impedance that compensates the output pad. However this maximum gain is still observed for the limit of capability of the load tuner, meaning that a better result could have been observed if the measurement equipment could have presented a much higher reflection coefficient magnitude. This equipment capability limit is illustrated by the two circles in Figure II-62.a, the smallest corresponding to the load tuner capability and the largest one to the source tuner capability.

This experimentation has been repeated with another chip and a better situation has been found, the gain reaching -1.07dB for 0.626 magnitude and 84.1° angle of input reflection coefficient and 0.458 magnitude and 79.3° angle of output reflection coefficient. Those specific source and load impedance are illustrated by the two triangles in Figure II-62.a.



a. Single-Ended detector **b. Differential detector**

Figure II-62 Optimized source and load impedances for the two power detector circuits

Similar measurements have been performed on the differential detector circuit. The maximum gain that has been observed is -9.51dB which has to be compared to the -15.8dB small signal S_{21} parameter measured at 60GHz with 50Ω at both input and output of the circuit (see section II.4.1.iii).

This smallest losses situation has been obtained when the source impedance was tuned to 0.629 magnitude and 65.5° angle of reflection coefficient Γ and the load impedance to 0.491 magnitude and 33.2° angle of reflection coefficient. Those two characteristic points are illustrated by the two triangles of Figure II-62.b.

Chapter conclusion

This chapter has presented a 60GHz 65nm CMOS power detector. This power detector circuit includes two main modules: the power detector itself, and the power coupler. The power detector is the active part that translates a voltage or current into power information while the power coupler realizes the interface between the detector and the RF chain (PA-Antenna).

After having detailed the state-of-the-art on those two modules, the chosen solution has been presented. The RMS power detector is based on the differential structure proposed by U. Pfeiffer in [8] (BiCMOS implementation) while taking advantage of the naturally square law of MOS transistor in saturation. This power detector is connected to an RF chain through a capacitive coupler integrated inside a grounded-coplanar-waveguide (GCPW). This coupler has been simulated using Electro-Magnetic simulators and an equivalent lumped model has been built in order to perform transient simulations including this power coupler.

The circuit physical implementation has then been introduced. Some adjacent components have been integrated in addition to the power coupler and power detector in order to be able to measure the circuit. This is notably the case of the baluns and the buffer. Some de-embedding structures have also been implemented to be able to deduce the desired characteristics on the useful part of the circuit from the full circuit measurements. A single-ended structure has also been integrated to work as a backup solution if some problems would have occurred on the differential structure.

Finally, the power detector circuit has been measured in three different phases. The first one corresponds to the small-signal S-parameters characterization of the different passive structures. The second phase consists of measuring the power detector answer to a power sweep in the transmission line while maintaining constant load impedance on the RF chain. The last phase is to perform a load-pull measurement and measure the detector output voltage while keeping a constant input power level but while varying the load impedance.

Table II-5 establishes a comparison between this work and the state-of-the-art for 60GHz implementations. By using MOS transistors in saturation rather than square law approximation of bipolar exponential characteristic, the presented detector shows a much larger detection range. With a larger than 16.9dB detection range, our detector is able to detect a 7:1 VSWR. The ability to detect up to 3:1 VSWR has been verified through load-pull measurements.

60GHz Power Detector	**This Work**	**U. Pfeiffer** [8]
Process	65nm CMOS	0.13µm SiGe BiCMOS
Output Signal Bandpass	0-100MHz	0-13.8MHz
Linear Detection Range	25dB	8.5dB
Minimal Detected Power	-25dBm	4dBm

Table II-5 Comparison with state-of-the-art

However this detector output voltage has now to be used in a regulation loop in order to compensate the measured antenna impedance mismatch. But before being implemented in a regulation loop (see Chapter IV), the detector output voltage has to be digitized through a Logarithmic Analog-to-Digital Converter (LADC) in order to obtain a digital signal that linearly corresponds to the measured power level expressed on a logarithmic scale – i.e. in [dBm].

Chapter references

[1] "Agilent Fundamentals of RF and Microwave Power Measurements," Agilent Technologies, Application Note AN 64-1C, April 2001.

[2] A. S. Brush, "Measurement of Microwave Power - A review of techniques used for measurement of high-frequency RF power," *IEEE Instrumentation & Measurement Magazine*, vol. 19, no. 2, pp. 20-25, April 2007.

[3] V. Milanovic, M. Gaitan, E. D. Bowen, N. H. Tea, and M. E. Zaghloul, "Thermoelectric Power Sensor for Microwave Applications by Commercial CMOS Fabrication," *IEEE Electron Device Letters*, vol. 18, no. 9, pp. 450-452, September 1997.

[4] Q. Z. Hu, Z. H. Liu, L. Yan, and W. Zhou, "A SiGe Power Amplifier with Power Detector and VSWR Protection for TD-SCDMA Application," in *IEEE Proceedings of the International Conference on Mixed Design of Integrated Circuits and System (MIXDES 2006)*, Gdynia, Poland, June 2006, pp. 214-217.

[5] R. G. Meyer, "Low-power Monolithic RF Peak Power Detector Analysis," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 1, pp. 65-67, January 1995.

[6] T. Zhang, W. R. Eisenstadt, R. M. Fox, and Q. Yin, "Bipolar Microwave RMS Power Detectors," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 2188-2192, September 2006.

[7] T. Zhang, W. R. Eisenstadt, and R. M. Fox, "A Novel 5 GHz RF Power Detector," in *IEEE International Symposium on Circuits and Systems (ISCAS 2004) Proceedings*, vol. 1, Vancouver, Canada, May 2004, pp. 897-900.

[8] U. R. Pfeiffer and D. Goren, "A 20dBm Fully-Integrated 60GHz SiGe Power Amplifier with Automatic Level Control," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp. 1455-1463, July 2007.

[9] B. Gilbert, "RMS-to-DC converter with balanced multi-tanh triplet squaring cells," 6,204,719, March 2001.

[10] M. Kouwenhoven and A. van Staveren, "A 2 GHz Mean-Square Power Detector with Integrated Offset Chopper," in *IEEE International Solid-State Circuits Conference (ISSCC 2005), Digest of Technical Papers*, vol. 1, San Francisco, CA, USA, February 2005, pp. 124-126.

[11] J. Mulder, W. A. Serdijn, A. C. van der Woerd, and A. H. M. van Roermund, "Dynamic translinear circuits-an overview," in *Proceedings of the 2nd IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design*, Baveno, Italy, September 1997, pp. 65-72.

[12] Q. Yin, W. R. Eisenstadt, R. M. Fox, and T. Zhang, "A Translinear RMS Detector for Embedded Test of RF ICs," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 5, pp. 1708-1714, October 2005.

[13] Y. Zhou and M. Chia Yan Wah, "A Wide Band CMOS RF Power Detector," in *IEEE International Symposium on Circuits and Systems (ISCAS 2006) Proceedings*, Kos, Greece, May 2006, pp. 4228-4231.

[14] A. van Bezooijen, R. Mahmoudi, and A. H. M. van Roermund, "Adaptive Methods to Preserve Power Amplifier Linearity Under Antenna Mismatch Conditions," *IEEE Transactions on Circuits and Systems I (TCAS I), Regular Papers*, vol. 52, no. 10, pp. 2101-2108, October 2005.

[15] A. Scuderi, L. La Paglia, F. Carrara, and G. Palmisano, "A High Performance RF Power Amplifier with Protection against Load Mismatches," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, vol. 2, Philadelphia, PA, USA, June 2003, pp. 699-702.

[16] F. Carrara, C. D. Presti, A. Scuderi, C. Santagati, and G. Palmisano, "A 3W 55% PAE CMOS PA with Closed-Loop 20:1 VSWR Protection," in *IEEE International Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*, vol. 4.2, San Francisco, CA, USA, February 2007, pp. 80-82.

[17] A. Scuderi, L. La Paglia, F. Carrara, and G. Palmisano, "A VSWR-Protected Silicon Bipolar RF Power Amplifier With Soft-Slope Power Control," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 611-621, March 2005.

[18] O. Wohlgemunth et al., "Integrated Directional Coupler for 90 and 180 GHz," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 8, pp. 308-310, August 1999.

[19] Y. Zhu and H. Wu, "A 10-40GHz 7dB Directional Coupler in Digital CMOS Technology," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, San Francisco, CA, USA, June 2006, pp. 1551-1554.

[20] Wireless HD Consortium, "Wireless HD specification, revision 1.0," January 2008.

[21] Ansoft. (2010, August) HFSS 3D Full-wave Electromagnetic Field Simulation. [Online]. http://www.ansoft.com/products/hf/hfss/

[22] Agilent Technologies. (2010, August) Momentum 3D Planar EM Simulator. [Online].

http://www.agilent.com/find/eesof-momentum

[23] N. Seller, "Contribution à l'Étude, au Développement et à la Réalisation d'Oscillateurs à Commandes Numériques en Technologie Silicium CMOS Avancée," Université Bordeaux 1, Bordeaux, France, Ph.D. Thesis.

[24] B. Martineau, "Potentialités de la technologie CMOS 65nm SOI pour des applications sans fils en bande millimétrique," Université des Sciences et Techniques de Lille, Lille, France, Ph.D. Thesis May 2008.

[25] A. Siligaris, C. Mounet, B. Reig, and P. Vincent, "CPW and discontinuities modeling for circuit design up to 110 GHz in SOI CMOS technology," in *IEEE Radio Frequency Integrated Circuits (RFIC 2007) Symposium*, Honolulu, HI, USA, June 2007, pp. 295-298.

[26] "CMOS 065 Design Rule Manual 65nm Bulk CMOS Process," STMicroelectronics, Design Rule Manual 7683821 revision E, October 2006. **RESTRICTED ACCESS**

[27] Agilent Technologies. (2010, August) Advanced Design System (ADS). [Online]. www.agilent.com/find/eesof-ads

[28] Magali de Matos, Eric Kerhervé, Hervé Lapuyade, Jean Baptiste Bégueret, and Yann Deval. (2009) Centre National pour la Formation en Microélectronique. [Online]. http://www.cnfm.fr/VersionFrancaise/animations/JP/Matos.pdf

Chapter III. Logarithmic Analog-to-Digital Converter

Chapter introduction

Analog-to-Digital Converters (ADC) are used to digitize an analog signal. Most of the time, the ADC has a linear behavior and directly associates an output code to the analog signal applied on its input. However, if the ADC analog input signal does not correspond to the physical quantity to be digitized through a linear behavior, the generated digital code would not linearly correspond to the physical quantity.

This is actually the case when considering the power level to be measured in the proposed VSWR regulation loop. The information to be digitized being the detected power level expressed on a logarithmic scale (in [dBm]), the analog signal coming from the power detector has an exponential behavior with respect to the physical quantity to be digitized. This exponential behavior has to be compensated using a logarithmic-behavior device in order to keep a constant digitization step along the full scale of the physical quantity.

This chapter presents the innovative architecture of a Logarithmic Analog-to-Digital Converter (LADC) that has been proposed and implemented during this Ph.D. thesis. This architecture advantageously uses the intermediate signals generated by a progressive compression logarithmic amplifier, which are regularly spaced with respect to the input signal expressed on a logarithmic scale, to perform a first step of digitization. This coarse conversion being made, a second digitization step could be performed by choosing and digitizing the intermediate signal that is linear with respect to the input signal expressed on a logarithmic scale. The coarse and the fine codes resulting from those two conversion steps are merged into a single code, which is linear with respect to the analog input signal expressed on a logarithmic scale.

Chapter outline

III.1. Needs for logarithmic ADC & existing solutions

III.1.1. Needs

The usual need for analog-to-digital converters (ADC) is to digitize an analog signal in order to be able to compute the information in the digital domain with a signal processor. The analog signal to be digitized is often the output of a transducer and hence represents a physical quantity (electrical, thermal…). Figure III-1 shows the synoptic of a physical quantity digitization.

Figure III-1 Digitization of a physical quantity

However the transducer often generates an analog signal that represents the physical quantity to be measured through an exponential law. In the context of this thesis, the power detector (detailed in the previous chapter) generates a voltage variation that is proportional to the power level expressed on a linear scale. But, the regulation loop working on the power level expressed in dBm, the power detector can be seen as a transducer that generates a voltage variation with respect to the power level expressed in dBm through an exponential law.

The difficulty now is to digitize this analog signal that represents a physical quantity through an exponential law. Using a classical linear ADC, a variation of one Least Significant Bit (LSB) does actually not represent the same range of the physical quantity when being situated at the lower or at the higher end of the digital code. This is illustrated in Figure III-2. The exponential curve on the right corresponds to the conversion of the physical quantity into the analog voltage made by the transducer. The linear stairs on the left corresponds to the digitization of the analog voltage and has been reported on the exponential law on the right to represent directly the digitization of the physical quantity. On this figure is also highlighted the physical quantity that is represented by one LSB at both the lower and the higher ends of the digital code. In this example, one LSB represents about 14% of the physical quantity scale when considering the digital code "0001", and represents only 2% when considering the digital code "1110".

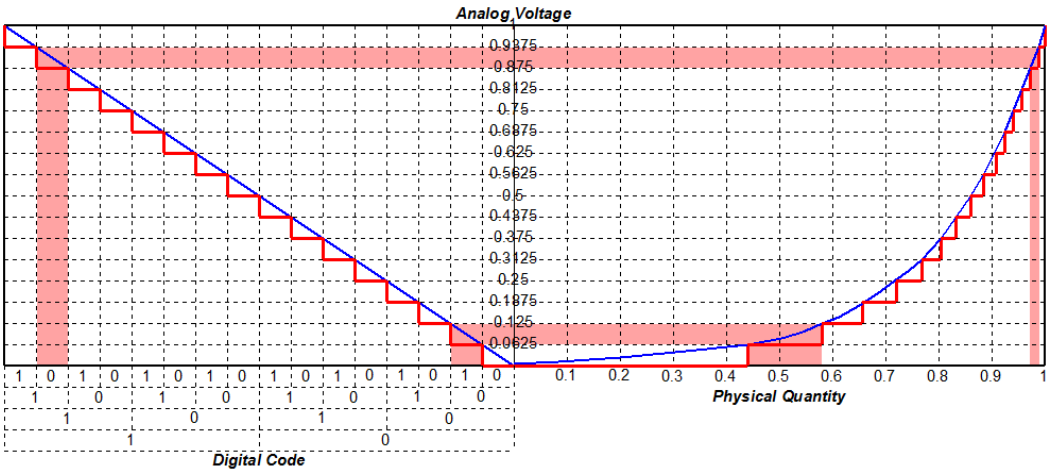


Figure III-2 Digitization through a linear ADC of a physical quantity sensed through an exponential law

Using a linear ADC would result in a very good precision at the higher end of the transducer scale which is much better than the requested one, but it would also result in a very poor precision at the lower end of the transducer scale which, this time, is insufficient with respect to the requested precision.

A better solution would be to implement a logarithmic analog-to-digital converter (LADC) that could compensate the exponential law of the transducer. Such an ideal LADC is illustrated in

Figure III-3. Using an ADC that includes a logarithmic function, the variation of one LSB does not correspond anymore to a constant variation of the analog voltage (logarithmic curve on the left), but combined to the exponential characteristic of the transducer, this now corresponds to a constant variation of the physical quantity. The new digitization function is reported on the right curve and is now an irregular stairs or more exactly (and also more poetically) an exponential stairs.

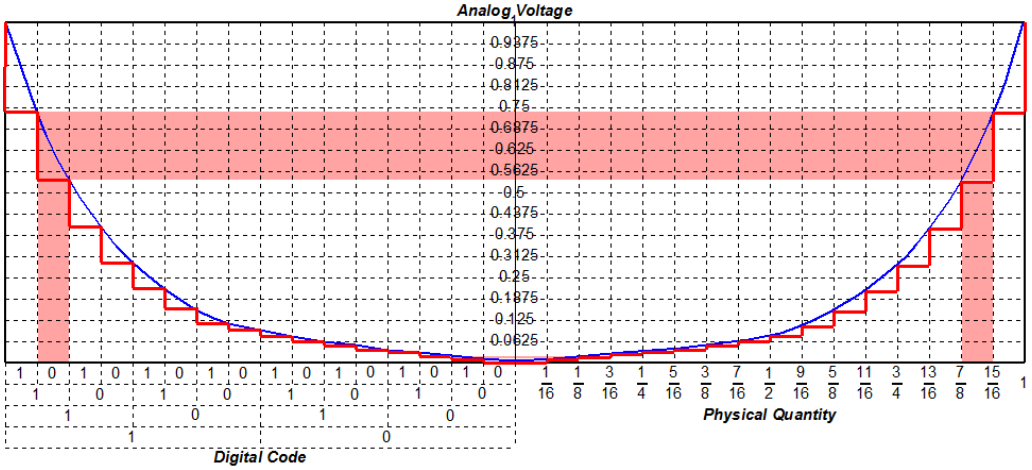


Figure III-3 Digitization through a logarithmic ADC of a physical quantity sensed through an exponential law

III.1.2. State-of-the-art

LADCs have been designed since the early 1970's. S. Cantarano and G.V. Pallottino have hence classified in three categories the different techniques already developed or imagined in 1973 [1]. The first one uses a linear ADC, the logarithmic conversion being performed previously in the analog domain. However, the logarithmic conversion can also be performed in the digital domain after having digitized the input signal through a linear ADC. This is the second category of LADC. Finally, the ADC can directly perform the logarithmic conversion simultaneously with the analog-to-digital conversion. Those three different categories are illustrated in Figure III-4.

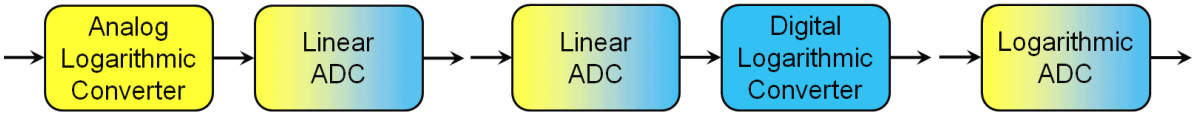


Figure III-4 Three different ways to realize a LADC

Focusing on the first LADC class (Figure III-4.a), the analog logarithmic converter is usually based on logarithmic amplifiers when the input and output variables are voltages or currents. This is notably the case when using an exponential behavior component in a feedback loop (see section III.1.2.v) or when using progressive compression logarithmic amplifier (see section III.1.2.vi). But some other techniques use frequencies, the duration of time intervals or some other physical variables.

i. Logarithmic converters using alternative physical variables

Considering a discharging RC network, the voltage across the capacitor is actually described by an exponential law following the equation (III.1).

$$V = V_0.\exp\left(-t/RC\right) \tag{III.1}$$

This voltage can be fed to a window comparator as can be seen in the schematic of Figure III-5 proposed in [2], with the reference levels V_{ref} and V_{in}. The resulting pulse width T at the window comparator output is hence given by the equation (III.2).

$$T = RC.\left|\ln\left(V_{in}/V_{ref}\right)\right| \tag{III.2}$$

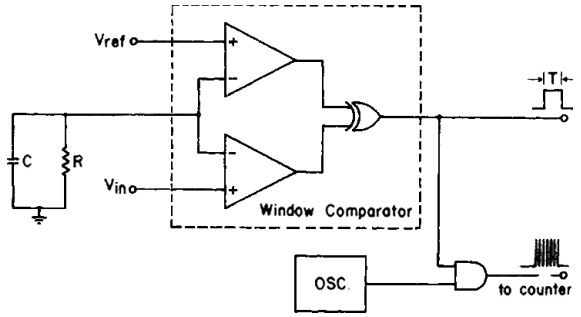


Figure III-5 Logarithmic converter using a discharging RC network

A simple combination through an AND logic gate with a digital clock signal converts the resulting pulse width in a certain number of much smaller pulses with a constant width that have to be counted in order to obtain a digital quantity corresponding to the logarithm of the input voltage V_{in}. Although this implementation is much closer to the third class of LADC (Figure III-4.c) rather than the first one as the ADC cannot be separated from the logarithmic converter, it illustrates the principle of some alternative techniques that uses the duration of time intervals or some other physical variables.

ii. Digital logarithmic converters

Let us now focus on the second category of LADCs that uses a logarithmic converter in the digital domain following the linear ADC (Figure III-4.b). In general, a floating point rather than a true logarithmic representation is used [1], where *F* denotes the current number of bits of the fraction (mantissa), E the current number of bits of the exponent. There are several different methods for the floating point representation of a number but the widely used one is the true floating point where the number N is given by the expression (III.3).

$$N = F.2^{E} \tag{III.3}$$

Figure III-6 illustrates the synoptic of a sequential floating-point converter, which is the simplest and the most widely used method to compress digital information into a floating-point representation.

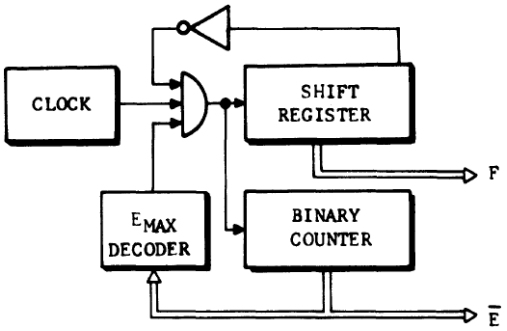


Figure III-6 Synoptic of a sequential Floating-Point converter

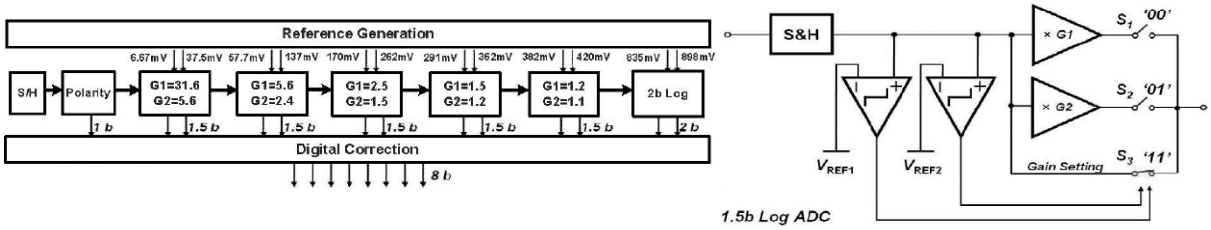
Since the logarithmic conversion is realized with digital techniques on quantized information all the problems of accuracy are now to be considered with reference to the ADC that must accept a wide input dynamic range. This is the reason why such digital solution cannot be implemented regarding our application where the covered dynamic range should be very wide. However many different implementations of floating-point converters are presented in [1] that can be of special interest for applications requesting modest dynamic range.

The two following techniques correspond to LADCs of the third category that directly perform the logarithmic conversion simultaneously to the analog-to-digital conversion (Figure III-4.c).

iii. Logarithmic pipeline ADC

An 8-bit logarithmic pipeline ADC is proposed in [3] that pipelines 5 stages of 1.5-bit sub-ADCs, much like a linear pipeline ADC, followed by one 2-bit logarithmic flash ADC as can be seen on the architecture of Figure III-7.a. However, instead of a 3-level multiplying DAC (MDAC), one of three gain settings is selected, by switching in different values for the feedback capacitor across an operational amplifier, depending on the sub-ADC decision as shown in Figure III-7.b. The 1.5 bit-per-stage architecture is built with a certain overlap between the different stages. This redundancy relaxes the requirements on comparator accuracy and reference voltage accuracy.

It has to be noticed that the logarithmic function needs a different set of reference voltages and gains on each stage (see Figure III-7.a). The major interest of [3] actually lies in the rescale of the dynamic range between the different stages. This is also one major drawback for this solution as creating many amplifiers with different gains induces a high cost in terms of complexity which reduces the flexibility of the implemented solution. Moreover the accuracy of several gain steps is often difficult to be reached.



a. Architecture of the logarithmic amplifier **b. Architecture of a pipeline stage**

Figure III-7 Implementation of a switched capacitor logarithmic pipeline ADC

However, this architecture has been implemented in 0.18µm CMOS process. The logarithmic pipeline ADC exhibits 22MS/s conversion rate and 80dB dynamic range while consuming 2.54mW from a 1.62V supply and occupying 0.56mm² considering only the active part.

iv. Logarithmic sigma-delta converters

Sigma-Delta modulators are known as high performance analog-to-digital converters. It is hence natural that some people would have tried to expand the dynamic range of such sigma-delta (Σ–Δ) ADCs by integrating a logarithmic conversion. Σ–Δ modulators are actually often used in audio and radio applications for the measurement of electrical magnitudes expressed in logarithmic units (dB) such as the power level.

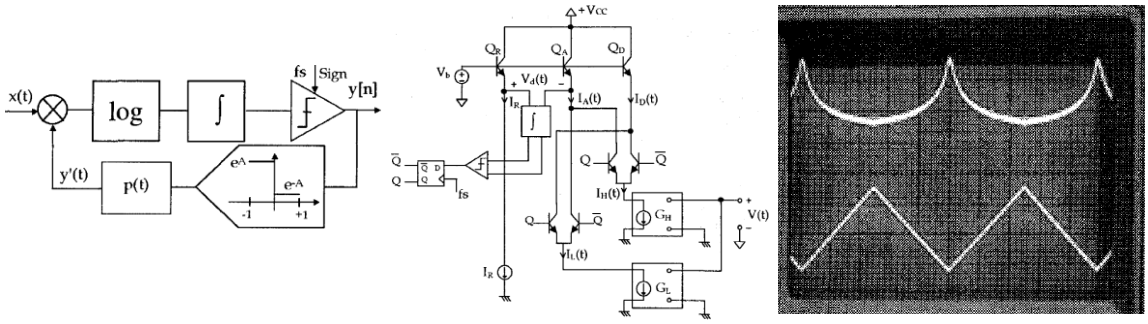
L. Hernandez proposes in [4] a single bit implementation of a logarithmic Σ–Δ described by the synoptic of Figure III-8.a. Figure III-8.b is a simplified circuit diagram of the implemented Σ–Δ modulator where *x(t)* from the synoptic is replaced by *V(t)* and *y(n)* by *Q(n)*. The trans-conductance amplifiers G_L and G_H set the feedback gain described in the synoptic following the equation (III.4).

$$e^{A} = G_H \Big/ \sqrt{G_H.G_L} \quad \& \quad e^{-A} = G_L \Big/ \sqrt{G_H.G_L} \tag{III.4}$$

The voltage $V_d(t)$ just before the integrator hence follows the expression (III.5) where V_L and V_H stand respectively for the lower and the higher levels reached by the time-varying input voltage *V(t)*.

$$\frac{V_d(t)}{KTe} = \ln\left(\frac{V(t)}{\sqrt{V_H.V_L}}\right) + \ln\left(\frac{G_H.Q + G_L.\overline{Q}}{\sqrt{G_H.G_L}}\right) \tag{III.5}$$

Figure III-8.c displays a time domain measurement of the test circuit using a sampling frequency of 5MHz. A triangular waveform of 2kHz was used as input signal *V(t)* and is shown in the lower trace. The upper trace (inverted) represents the digital output of the modulator when reconstructed by a low-pass analog filter. It may be seen that the reconstructed output reproduces a waveform close to the logarithm of the input signal.



a. Synoptic of the modulator **b. Simplified circuit diagram** **c. Time domain waveforms**

Figure III-8 Implementation of a 1-bit sigma-delta logarithmic ADC

Let us now come back to the first class of LADC (Figure III-4.a) and detail the known techniques to realize the logarithmic converter in the analog domain.

v. Using an exponential device in a loop-back

Logarithmic circuits of various types can be realized by using physical devices whose characteristics are inherently logarithmic, such as the PN junctions [1]. Figure III-9 shows the most used scheme of such logarithmic amplifiers. A diode which has naturally an exponential characteristic is integrated in the feedback circuit of an operational amplifier. The diode is often replaced by a transistor in the so called "transdiode" connection. The resulting output voltage V_{out} is hence logarithmically dependent on the input voltage V_{in} as it follows the equation (III.6) where each term has its usual meaning or is directly defined in Figure III-9.

$$V_{out} = V_{ref} - V_t . \ln\left(\frac{V_{in} - V_{ref}}{R.I_S} - 1\right) \tag{III.6}$$

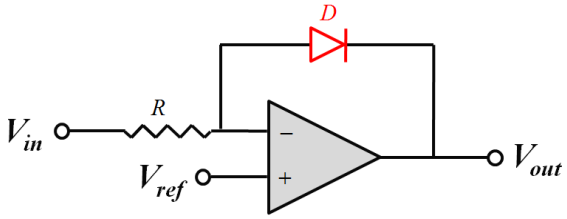
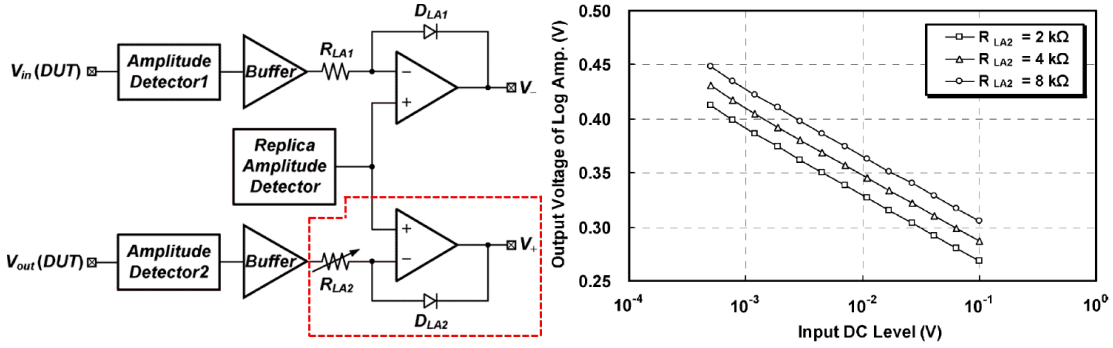


Figure III-9 Logarithmic converter using a feedback loop including an exponential law component

Such a feedback loop including an exponential device to realize a logarithmic amplifier has been implemented in [5] to be used with some amplitude detectors as can be seen in Figure III-10.a. This is hence very close to our application. In this study, the input resistance R_{LA2} can be digitally tuned to adapt the output voltage of the logarithmic amplifier to the desired voltage range.



a. Schematic **b. Simulated transfer function**

Figure III-10 Implementation of a feedback loop including an exponential device

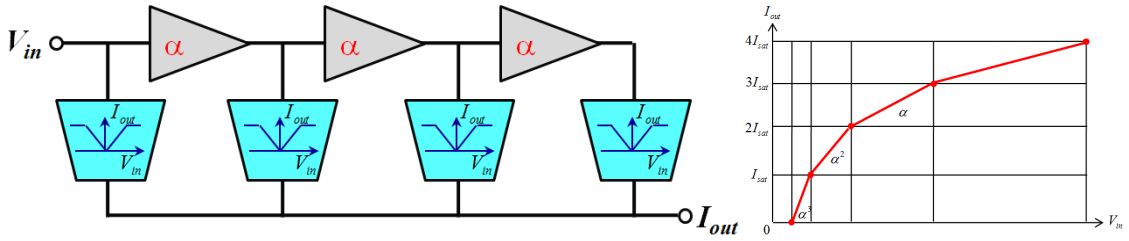
The full Built-In-Self-Test circuit has been implemented in 0.18µm CMOS process and exhibits 30dB dynamic range over the full 1-10GHz operating frequency band while consuming only 7.2mW under a single 1.8V power supply voltage and occupying only 0.042mm².

The simulated transfer function of the logarithmic amplifier circuit – highlighted in Figure III-10.a – (the detectors and buffers are not integrated) is shown in Figure III-10.b for three different values of R_{LA2}. The dynamic range obtained for this logarithmic amplifier is limited to about 2.3 decades which is insufficient for our application.

Based on a feedback loop, the circuit should actually ensure a certain stability margin that reduces the dynamic range. Moreover this kind of logarithmic amplifier has also to deal with the high V_t of the diode or transistor integrated in the feedback loop, and the temperature has also a high influence on the amplifier characteristic.

vi. Progressive compression logarithmic amplifier

Another solution to realize a logarithmic converter in the analog domain is to approximate the logarithmic function with a series of contiguous segments generated by a cascade of non-linear amplifier cells [6]. This technique is called progression compression as it uses a cascade of amplifiers that progressively compress the signal. Considering the synoptic of such logarithmic amplifier illustrated in Figure III-11.a which is composed of a cascade of α gain amplifiers and voltage-to-current rectifiers, the resulting $I_{out}=f(V_{in})$ transfer function is an approximation of the logarithmic function as can be seen in Figure III-11.b.

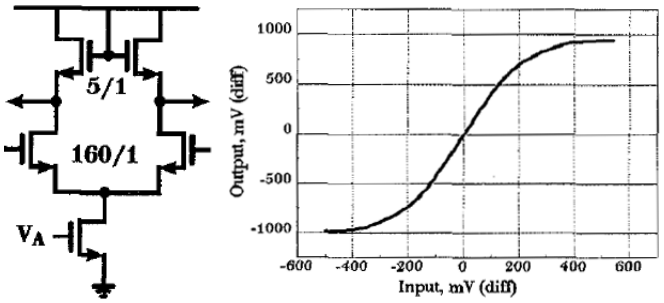


a. Synoptic **b. Transfer function**

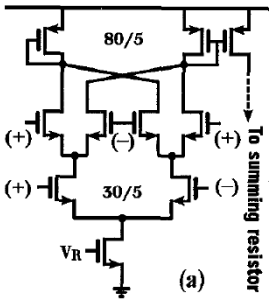
Figure III-11 Theory on progressive compression logarithmic amplifier

When the smallest range rectifier reaches its saturation range, its output current is actually almost constant and the just higher range rectifier takes the relay as this one is still in its linear working range. The gain of the global amplifier hence changes from an α^N slope to an α^{N-1} slope. Integrating a certain number of amplifier-rectifier sections hence progressively approximates the desired logarithmic characteristic.

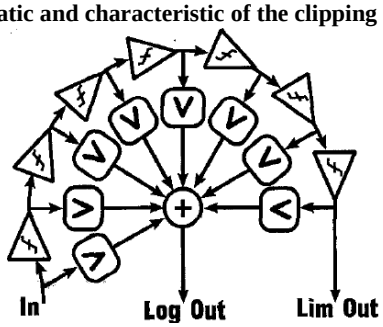
[7] presents an early implementation in 1995 of such progressive compression logarithmic amplifier which integrates 7-stages of 12dB gain clipping amplifiers and 8 rectifiers along the cascade. Figure III-12.c shows the synoptic of this implementation. The schematic of the rectifier is presented in Figure III-12.b. Figure III-12.a shows the schematic and characteristic of one clipping amplifier. Figure III-12.d shows the measurement results of the full logarithmic amplifier performed at 0, 27 and 85°C. This 1µm CMOS process implementation consumes 2W under 2.7V power supply voltage. However the logarithmic amplifier exhibits more than 80dB dynamic range with 5MHz bandwidth.



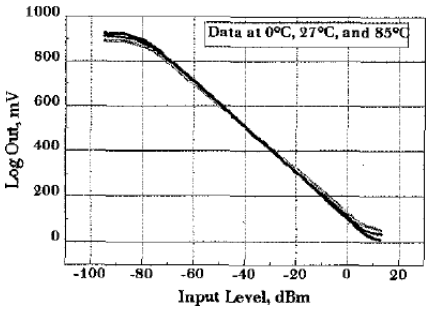
a. Schematic and characteristic of the clipping amplifier



b. Schematic of the rectifier



c. Synoptic of the logarithmic amplifier

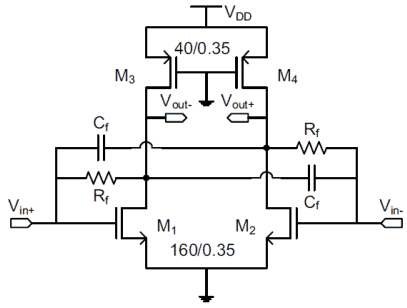


d. Measured characteristic

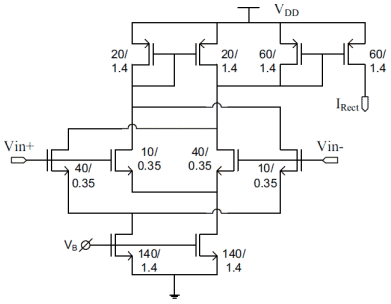
Figure III-12 Implementation of a progressive compression logarithmic amplifier

A more recent implementation in 0.35µm CMOS process has been presented in 2008 in [8]. The synoptic of the logarithmic amplifier, illustrated in Figure III-13, and the schematic of both the clipping amplifier and the rectifiers, illustrated in Figure III-13.a and Figure III-13.b respectively, are almost similar to the implementation detailed previously. But this time, the logarithmic amplifier integrates 8-stages of 6dB gain clipping amplifiers and 9 rectifiers.

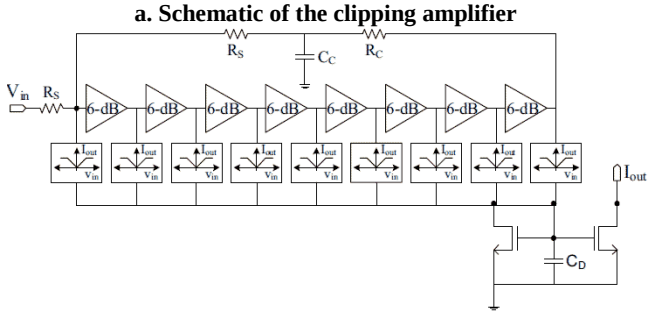
Figure III-13.d shows the input-output characteristic of the logarithmic amplifier which has been measured at the input frequency of 2.4GHz. The resulting characteristic is almost exponential as the circuit is used as an RF signal level detector and not directly as a logarithmic amplifier. The logarithmic amplifier exhibits 56dB gain with 2.5GHz bandwidth while consuming only 184mW under a single 2.5V power supply voltage. The total die area is 330x575µm².



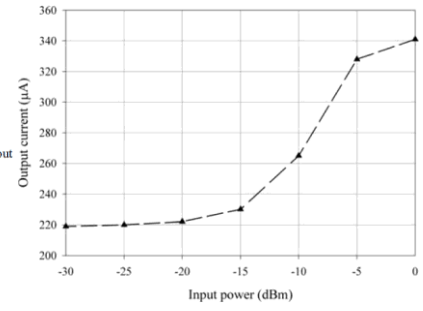
a. Schematic of the clipping amplifier



b. Schematic of the rectifier



c. Synoptic of the logarithmic amplifier



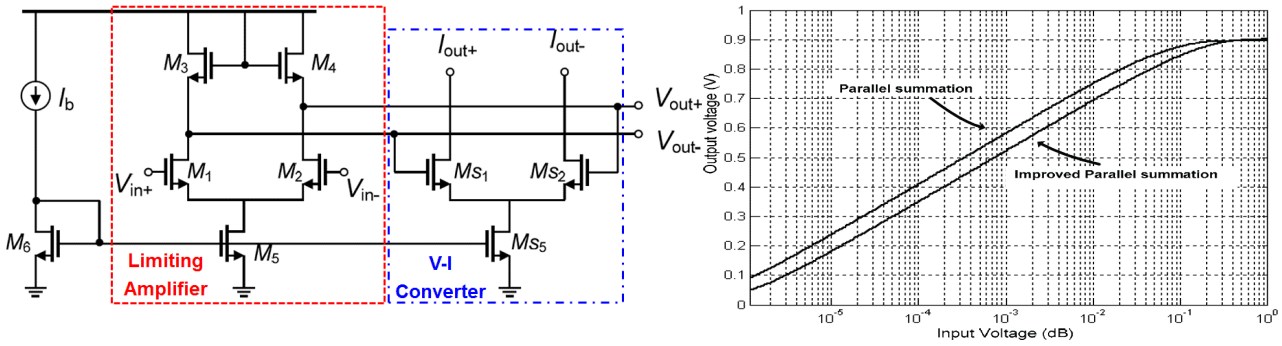
d. Measured characteristic

Figure III-13 Implementation of a progressive compression logarithmic amplifier

Some other implementations of progressive compression logarithmic amplifier can also be found in the literature [9][10][11] that are not detailed here as they differ from the two implementations presented above in the circuit implementation.

On the other hand, the principle implemented in [12] is quite different as it corresponds to the 2nd version of progressive compression logarithmic amplifiers introduced in [6]. The rectifier is actually directly integrated in the amplifier and the amplifier output voltage has then just to be converted into current through a trans-conductance in order to be summed with the other currents of the amplifier cascade.

The schematic of each stage, illustrated in Figure III-14.a, is hence much simpler than for the previous implementations. Using only 8 transistors per stage, the number of stages can be increased while keeping a very small occupied area and very low power consumption. The implementation presented in [12] integrates 12 amplifier cells.



a. Schematic of the clipping amplifier and the V-I converter **b. Simulated characteristics**

Figure III-14 Implementation of a simple progressive compression logarithmic amplifier

The output currents of all stages are then summed and converted into a differential voltage that is represented in Figure III-14.b. This logarithmic amplifier exhibits hence about 5 decades dynamic range and 50MHz bandwidth.

Analog Devices has also worked on progressive compression logarithmic amplifiers [13] and sells some commercial products. The AD8307 [6] exhibits 92dB dynamic range and 500MHz bandwidth with ±1dB linearity while consuming only 20mW under 2.7V power supply voltage. The AD8319 [14] exhibits a lower 45dB dynamic range but a much wider bandwidth from 1MHz up to 8GHz while consuming 66mW under 3V power supply voltage.

Concluding that the implementation presented in [12] and illustrated in Figure III-14 of a progressive compression logarithmic amplifier is very attractive due to its simplicity and its flexibility, we have decided to integrate a linear ADC inside this architecture, thus converting the logarithmic amplifier into a LADC of the third category (see Figure III-4.c). This innovating solution being inexistent in the literature as has been seen in this section, we have patented this work. The next section exposes this proposed innovating solution.

III.2. Proposed innovating solution

III.2.1. Observations on a progressive compression logarithmic amplifier

The proposed innovating solution is based on a classical progressive compression logarithmic amplifier (PCLA). As described above in the state-of-the-art, one of the PCLA architecture integrates a cascade of limiting amplifiers that progressively compresses the dynamic range, and some voltage-to-current converters that convert the intermediate voltages (the output of each amplifier stage) in currents that are summed to form the output of the PCLA [6].

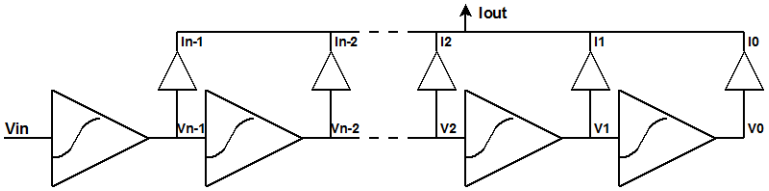


Figure III-15 Block diagram of a known progressive compression logarithmic amplifier

At this time, some very interesting observations can be made on the shape of the intermediate voltages at the output of each amplifier stage. Figure III-16 shows the theoretical intermediate voltages from V_{n-1} at the first stage output down to V_0 at the last stage output with respect to the input voltage V_{in} of the PCLA expressed on a logarithmic scale.

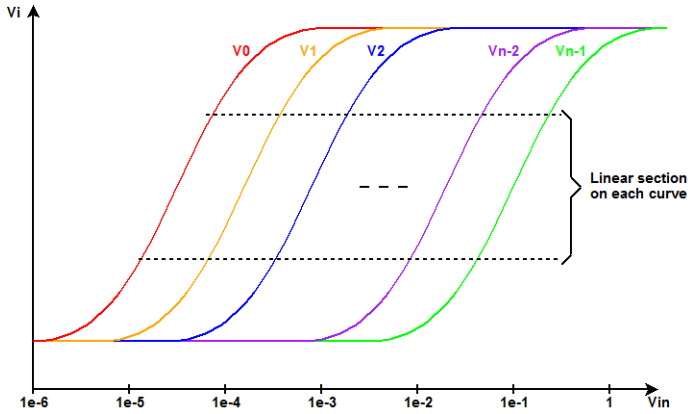


Figure III-16 Theoretical output voltage of each stage

First, all those voltage curves have the same shape which is only subject to a regular translation along the V_{in} axis expressed on a logarithmic scale. All the amplifier stages being identical, they actually have the same input-output characteristic. This corresponds to a geometrical progression which is naturally translated into a linear progression on a logarithmic scale.

This is much easier to understand focusing on the linear regime of the amplifier stages. When all the amplifiers work in their linear region, the Nth stage output voltage, noted V_0, will be α^N dependent to V_{in} while the N-1th stage output voltage, noted V_1, will be α^{N-1} dependent to V_{in}, and so-on. V_0 is hence an image of V_1 through a factor α the linear gain of the Nth amplifier stage. The product being equivalent to an addition in the logarithmic domain, the V_0 curve is hence a translation of the V_1 curve along the V_{in} axis expressed on a logarithmic scale. Those linear ranges of each intermediate voltage correspond to the lower part of the characteristics of Figure III-16 – under the lowest dotted line – where the curves are almost exponential as V_{in} is expressed on a logarithmic scale. The same translation occurs for the other parts of the curves, notably for the saturation region above the highest dotted line of Figure III-16.

The second observation concerns the intermediate range of each intermediate voltage when the amplifier stage is no more linear but is not already in deep saturation. This intermediate range corresponds to the region between the two dotted lines in Figure III-16. In this intermediate range, all the voltage curves are almost linear with respect to the input voltage expressed on a logarithmic scale. Moreover, the different intermediate voltage curves being only subjected to a regular translation along the V_{in} axis expressed on a logarithmic scale, this linear range is common to all the intermediate voltages as can be seen in Figure III-16.

III.2.2. Coarse conversion

The first observation is used to realize a coarse analog-to digital conversion. The intermediate voltages curves, being regularly spaced along the V_{in} axis expressed on a logarithmic scale, actually determine the intermediate voltage which is in its linear region would give an indication on the range of V_{in}. A simple comparison of all those intermediate voltages with a common reference voltage V_{ref} can give us this indication in the form of a digital output with a thermometer code representation.

Considering an Nth stages PCLA, *N-1* comparators are hence integrated following the architecture of Figure III-17 and compare the intermediate voltages from V_{N-1} down to V_1 with a common reference voltage V_{ref}. A comparison of the last intermediate voltage V_0 is not necessary if the fine analog-to-digital conversion described here after is also implemented as it would give some redundant information.

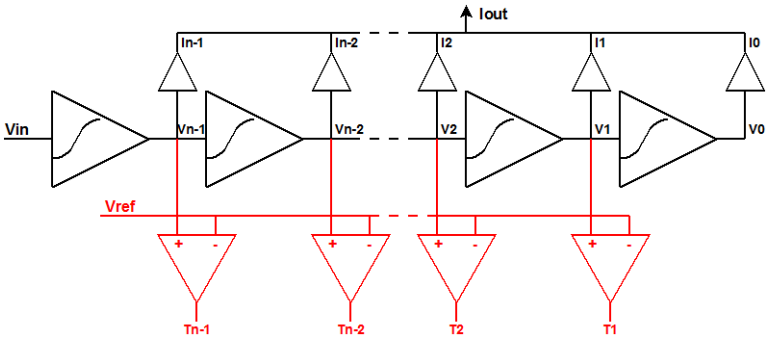


Figure III-17 Block diagram of first stage coarse conversion

Figure III-18 shows the comparison of the intermediate voltages with a common reference voltage V_{ref} and the thermometer code resulting from this coarse conversion.

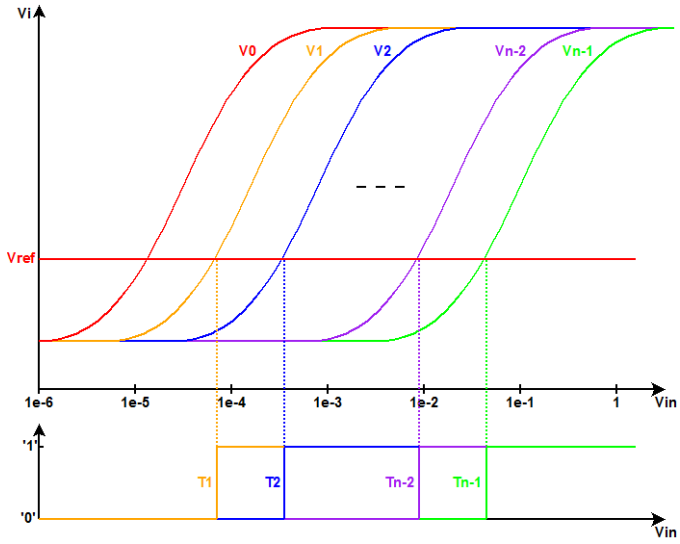


Figure III-18 Theoretical intermediate voltages and thermometer code resulting from the coarse conversion

The digital output code is qualified as "thermometer code" as a given value is coded by a succession of zeros and a succession of ones, the information lying in the location of the change between the succession of zeros and the succession of ones; hence working similarly to the mercury progression in a thermometer. This thermometer code digital output can quite easily be converted into a classical binary digital code and form the coarse bits of the logarithmic analog-to-digital converter. An example of such thermometer to binary code converter is given in section III.3.2.iv. *N-1* comparators generate a thermometer output code on *N-1* bits, noted T_1 up to T_{N-1}, which are converted into $\sqrt{N}$ bits expressed on a classical binary code.

III.2.3. Fine conversion

However, $\sqrt{N}$ bits can be insufficient to quantify the input voltage V_{in} and a fine conversion can be implemented using the second observation of section III.2.1 in order to increase the precision of the digital output code. Observing that the intermediate voltage curves of Figure III-16 all have a linear section with respect to the input voltage when expressed on a logarithmic scale, the intermediate voltages can actually be directly digitized through a classical linear ADC on their linear section. The precision of the LADC can hence be increased with few extra cost by simply adding a linear ADC. But the input of this so called "fine ADC" needs first to be shaped.

An analog multiplexer hence selects the intermediate voltage V_i which is in its linear section and will be digitized by the fine ADC. This selection is made depending directly of the thermometer code output of the coarse converter and following the rule: the signal *Vi* is selected if and only if there is a difference between the bits T_i and T_{i+1}. On the extremities, the signal V_0 is logically selected if all the thermometer code bits are equal to zero; and the signal V_{n-1} is selected if all the thermometer code bits are equal to one. Those rules are summarized in the expression (III.7).

$$\begin{cases} Mux\_Out = Vi \text{ if and only if: } \forall i \in [1; N-2], T_i \neq T_{i+1} \\ Mux\_Out = V_0 \text{ if and only if: } \forall i \in [0; N-1], T_i = 0 \\ Mux\_Out = V_{N-1} \text{ if and only if: } \forall i \in [0; N-1], T_i = 1 \end{cases} \quad \text{(III.7)}$$

Figure III-19 illustrates in broad outline the resulting PCLA including the coarse converter and the analog multiplexer. The analog multiplexer hence needs the different intermediate voltages V_{N-1} down to V_0 and the thermometer code bits T_{N-1} down to T_1 to output a voltage *Mux_Out* that is linear by sections with respect to the input voltage V_{in} expressed on a logarithmic scale. The shape of this multiplexer output voltage is shown in Figure III-20.

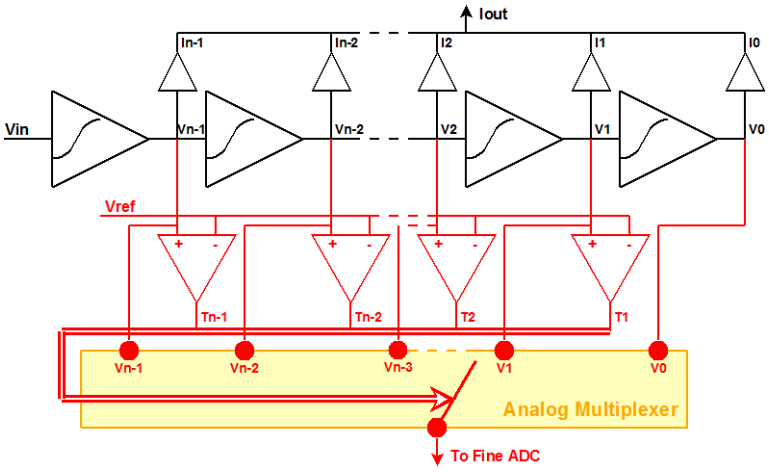


Figure III-19 Block diagram of the first conversion stage and the analog multiplexer

At this point, it is important to discuss how the level of the reference voltage generating a *Mux_Out* signal that is effectively linear by sections can be determined. To obtain a linear by section

multiplexer output signal, the reference voltage V_{ref} should actually respect the two following rules for each intermediate voltage V_i: first, V_i is linear when $V_i=V_{ref}$ – i.e. when V_i is selected – and then, V_i is still linear when $V_{i+1}=V_{ref}$ – i.e. when V_{i+1} is just selected instead of V_i. Those two rules have been applied for the V_{N-2} intermediate voltage in Figure III-20.

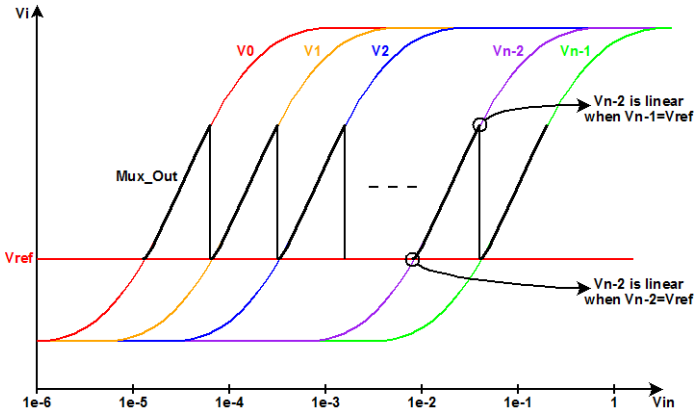


Figure III-20 Theoretical intermediate voltages and analog multiplexer output

The multiplexer output signal *Mux_Out* being now linear by sections with respect to the input voltage V_{in} when expressed on a logarithmic scale, it can be digitized thanks to a classical linear ADC. This linear ADC can be of any type the application requests from flash to sigma-delta or other pipeline ADC. Figure III-21 shows in light blue the fine analog-to-digital conversion that is performed on the *Mux_Out* signal. Considering a $\sqrt{M}$ bits fine ADC, the linear section of *Mux_Out* is divided in *M* steps (*M-1* reference voltages $V_{ref\ I}$ if considering a flash ADC), but different values of the input voltage V_{in} will generate the same fine bits code as can be seen in Figure III-21.

The fine bits are only meaningful when they are correlated to the coarse bits as one digital code on the fine bits is generates on different linear sections of *Mux_Out* and hence corresponds to different values of the input voltage V_{in}. The $\sqrt{N}$ bits of the coarse conversion are placed in front of those $\sqrt{M}$ bits of the fine conversion to form a $\sqrt{N}+\sqrt{M}$ bits digital word corresponding to the LADC output. By this way, the precision of the LADC can be increased by increasing the precision of the linear fine ADC while keeping the coarse ADC as it is. On the other hand, the fine conversion can be removed if the application does not need more precision than the $\sqrt{N}$ bits of the coarse conversion.

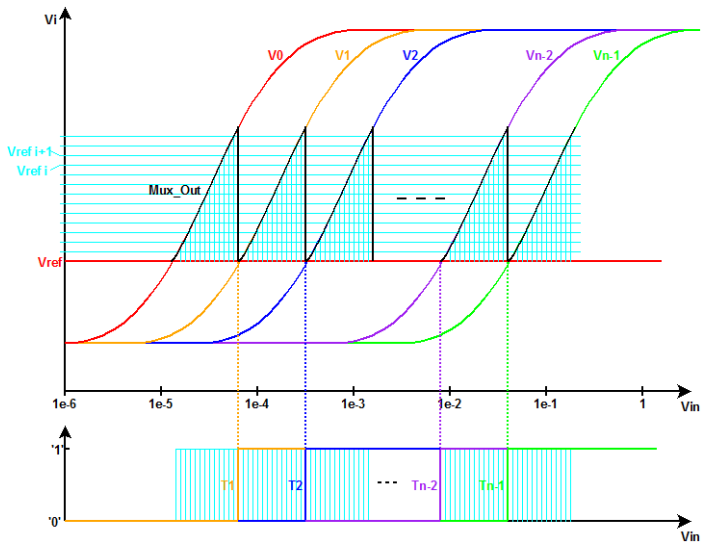


Figure III-21 Theoretical intermediate voltages with both coarse and fine conversion

III.2.4. Calibration considerations

i. Linearity limitation

This logarithmic analog-to-digital conversion being made in two steps, the fine bits and the coarse bits have to be well correlated in order to minimize the conversion error. The linearity of the LADC actually depends on the correlation between the coarse bits and the fine bits, which is directly impacted by the accuracy of the comparators. A small error in the coarse conversion will imply an error on the selected segment; hence the output of the analog multiplexer *Mux_Out* will exceed the range (overflow or underflow) of the fine ADC. Figure III-22 illustrates this phenomenon.

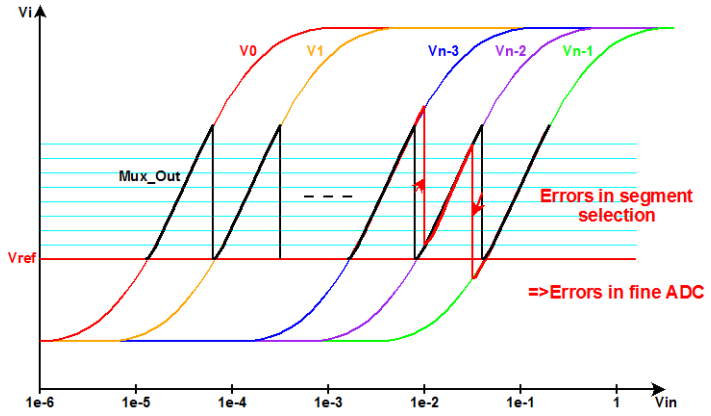
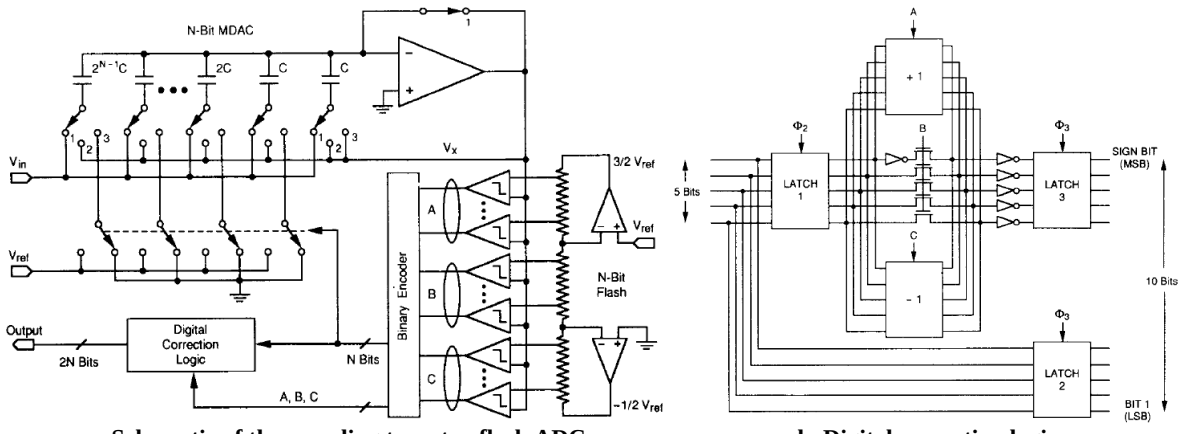


Figure III-22 Linearity error mechanism induced by a comparator error in the coarse conversion

ii. Existing solution

The innovating solution proposed above is fully compatible with the known techniques of ADC linearity increasing and ADC calibration. [15] presents a linearity correction technique to be implemented with a recycling two-step flash ADC. The proposed solution is to increase the range of the flash ADC by integrating additional comparison levels at both the lower and the higher conversion range which generates respectively the C and the A group of thermometer code bits as shown on the schematic of Figure III-23.a. The B group of thermometer code bits corresponds to the dynamic range of the ideal linear flash ADC.

A digital correction logic, shown in Figure III-23.b, then computes the resulting bits of the recycling two-step ADC by adding or subtracting one to the Most Significant Bits (MSB) depending of the result of the fine conversion, thus correcting the linearity error made during coarse conversion.



a. Schematic of the recycling two-step flash ADC **b. Digital correction logic**

Figure III-23 Known technique that increases the linearity of an ADC

iii. Implementation in our LADC

This known technique can be applied to our innovating LADC. To ensure a proper coverage of the LADC full scale, the solution actually consists of increasing the range of the fine ADC to create an overlap between the higher end of one linear section and the lower end of the next linear section. This is illustrated in Figure III-24 where the multiplexer output signal *Mux_Out* can be coded by the fine ADC even if an error occurs during coarse conversion.

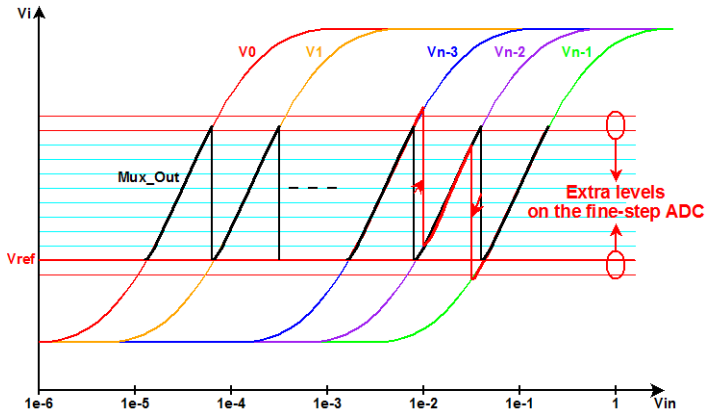


Figure III-24 Adding some extra levels on the fine ADC

However those additional fine steps generate additional fine bits while the LADC digital output word should still be coded on $\sqrt{N}+\sqrt{M}$ bits with a continuous linear code – i.e. all the values of the digital code should be obtained and should correspond to a constant portion of the input voltage V_{in} when expressed on a logarithmic scale. The digital correction logic is hence not so simple as the one of Figure III-23.b [15]. In our implementation, a calibration procedure has to be developed.

iv. Calibration procedure

The calibration procedure necessitates a calibration phase during which the characteristic of the LADC is observed. An analog monotonic ramp is hence applied at the input of the LADC while the digital LADC output is stored in a table. The input ramp can be linear with respect to the time but this would result in an exponential spreading over the time of the digital output, the ADC being logarithmic. A continuous time step at the output can be obtained by applying an exponential ramp at the input. By the way, the input ramp can have any shape as long as it is monotonic.

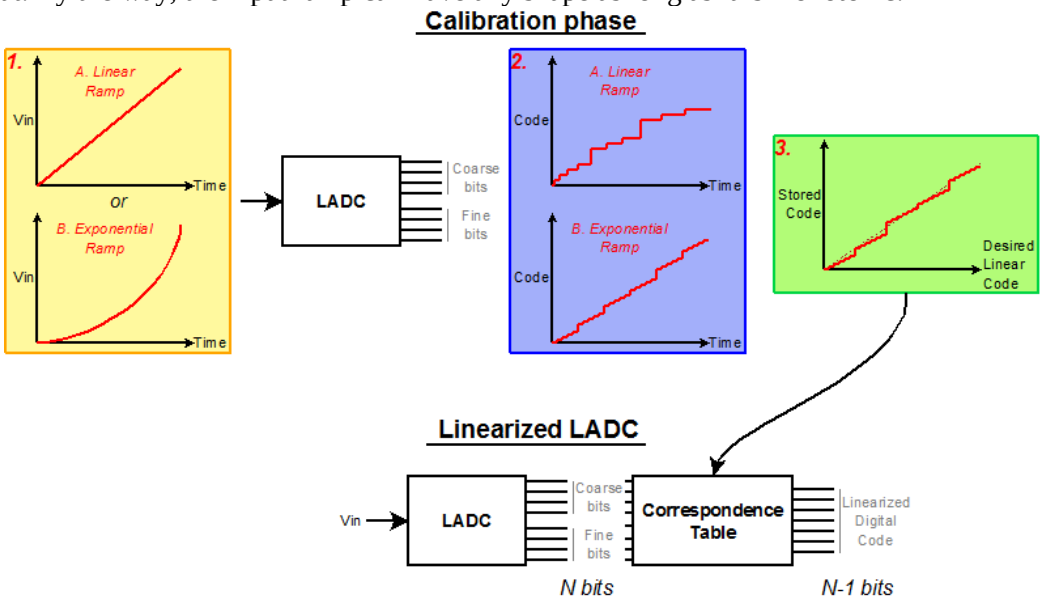


Figure III-25 Calibration procedure to linearize the LADC

Figure III-25 illustrates this calibration phase for the two cases of a linear and an exponential ramp with respect to the time applied at the input of the LADC (1.); the resulting output digital code is hence obtained with respect to the time (2.). This allows creating a correspondence table (3.) between the measured code and the desired value of this output code. This correspondence table is then directly used to linearize the output of the LADC as can be seen in Figure III-25.

Figure III-26 illustrates the correspondence table that could be obtained for a 4 bits coarse converter and a 3.5 bits fine converter which should be linearized to form a 7 bits linear LADC. This correspondence table can be implemented into a memory that would output the value stored in the location that is addressed by the combination of the coarse and fine bits of the LADC.

The highlighted values of the table form a continuous linear digital code. The values that are not highlighted (i.e. on white background) are extrapolated from the other values in order to form a meaningful output code if inadvertently the corresponding coarse and fine codes would have appeared. This table is illustrated in terms of analog multiplexer output *Mux_Out* with respect to the input voltage V_{in} at the bottom of Figure III-26.

Fine bits (LSBs)		Coarse bits (MSBs)															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0	0000		0000110	0001110	0011000	0011110	0100110	0101111	0110110	0111110	1000110	1001110	1010110	1100000	1100111	1101110	1110110
1	0001		0000111	0001111	0011001	0011111	0100111	0110000	0110111	0111111	1000111	1001111	1010111	1100001	1101000	1101111	1110111
2	0010	0000000	0001000	0010000	0011010	0100000	0101000	0110001	0111000	1000000	1001000	1010000	1011000	1100010	1101001	1110000	1111000
3	0011	0000001	0001001	0010001	0011011	0100001	0101001	0110010	0111001	1000001	1001001	1010001	1011001	1100011	1101010	1110001	1111001
4	0100	0000010	0001010	0010010	0011100	0100010	0101010	0110011	0111010	1000010	1001010	1010010	1011010	1100100	1101011	1110010	1111010
5	0101	0000011	0001011	0010011	0011101	0100011	0101011	0110100	0111011	1000011	1001011	1010011	1011011	1100101	1101100	1110011	1111011
6	0110	0000100	0001100	0010100	0011110	0100100	0101100	0110101	0111100	1000100	1001100	1010100	1011100	1100110	1101101	1110100	1111100
7	0111	0000101	0001101	0010101	0011111	0100101	0101101	0110110	0111101	1000101	1001101	1010101	1011101	1100111	1101110	1110101	1111101
8	1000	0000110	0001110	0010110	0100000	0100110	0101110	0110111	0111110	1000110	1001110	1010110	1011110	1101000	1101111	1110110	1111110
9	1001	0000111	0001111	0010111	0100001	0100111	0101111	0111000	0111111	1000111	1001111	1010111	1011111	1101001	1110000	1110111	1111111
10	1010	0001000	0010000	0011000	0100010	0101000	0110000	0111001	1000000	1001000	1010000	1011000	1100000	1101010	1110001	1111000	
11	1011	0001001	0010001	0011001	0100011	0101001	0110001	0111010	1000001	1001001	1010001	1011001	1100001	1101011	1110010	1111001	

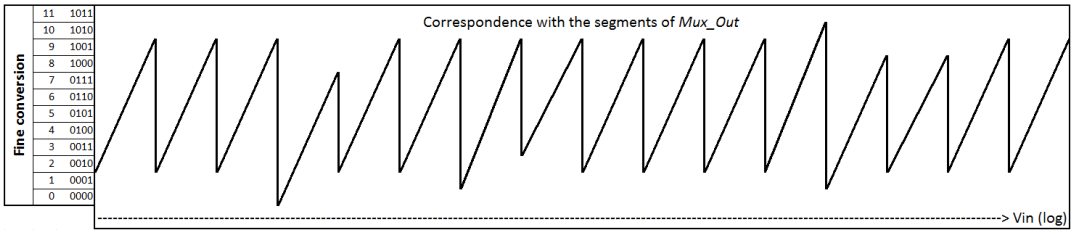


Figure III-26 Correspondence table for the LADC linearization

v. Improved calibration procedure

The table presented at Figure III-26 stores a 7 bits code for each combination of the 2^4 coarse and $2^{3.5}$ fine codes. This corresponds to a 7 bits code for each of the 192 possible output code from the LADC. This is not necessarily a problem for such small LADC but this can become problematic for a LADC with a wider dynamic range. Moreover this solution is not really efficient as in each column of the table – i.e. for each coarse code – the progression of the stored values is linear and can hence be linked to the value of the fine bits.

The solution we proposed here to improve the efficiency of the linearization table is to store only the values of the first line of the correspondence table which means to store only one value for each of the coarse code. This works as a pre-distortion of the LADC output code. The fine bits are now directly added to the 7 bits output of the table which is addressed with the coarse bits, thus forming the continuous linear code at the linearized LADC output as can be seen in Figure III-27.

As an example, the coarse code ‘0110’ (6 in decimal) generates the code ‘0101111’ at the output of the table that is directly added to the fine code, ‘0001’ as an example, to form the linearized output code ‘0110000’ on 7 bits which is effectively the value stored in the initial large calibration table of Figure III-26.

However, the first cell of the table can be inexistent as the combination of the value ‘0’ on both the coarse and the fine bits would never happen. This is notably the case in the large table of Figure III-26 where this cell is empty. A sign bit should hence be added in front of the 7 bits data stored in the improved correspondence table to be able to store a negative value that would generate

the appropriate positive output code – thanks to an overflow – after the fine bits being added. This sign bit can hence be removed after the addition as can be seen in Figure III-27.

This improved method hence stores only 16 values on 8 bits rather than 192 values on 7 bits in the initial configuration.

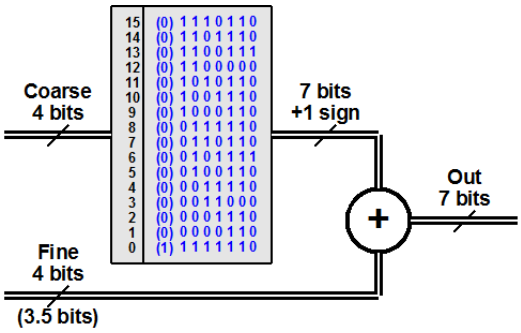


Figure III-27 Improved correspondence table and associated digital logic for the LADC linearization

The improved correspondence table is obtained by counting the number of changes on the fine code while applying a monotonic voltage ramp at the input of the LADC. The value stored in the table is then obtained by subtracting the fine code to the counter value at each change on the coarse code.

III.2.5. Advantages of this innovating solution

The innovating technique presented here has several advantages with respect to the known logarithmic analog-to-digital converters detailed in section III.1.2.

First, this solution ensures a large dynamic range as it is directly dependent to the architecture of the progressive compression logarithmic amplifier (PCLA) integrated in the LADC. The dynamic range of this LADC is actually linked to the number of concatenated amplifiers forming the PCLA and to their individual gains. The dynamic range of the LADC could hence be increased for a constant gain of each amplification stage by increasing the number of concatenated amplifiers, the number of coarse output bits being increased at the same time.

On the other hand, for a constant number of amplifiers, the dynamic range of the LADC can be increased by increasing the gain of each amplification stage. But in this case, if the LADC includes a fine converter, the PCLA architecture should still respect the rule introduced at Figure III-20 meaning that each intermediate voltage V_i should be linear both when $V_i=V_{ref}$ and when $V_{i+1}=V_{ref}$.

The proposed innovating solution is hence very flexible as the dynamic range can be increased by several ways. Moreover, the resolution of the LADC can also be increased by several ways. As introduced above, the resolution of the LADC actually depends on the resolution of the coarse converter, which means the gain and the number of amplification stages. But the resolution of the LADC also depends on the resolution of the fine converter.

The fine converter is a classical linear ADC that is independent to the rest of the LADC and can hence ensure the requested resolution. Inversely, if the application does not require a huge precision level, the fine converter can be totally removed thus simplifying drastically the LADC implementation. This LADC can hence be qualified as very flexible with regard to the existing solutions.

The presented LADC ensures the same performance in terms of frequency bandwidth as the integrated PCLA. This LADC is also compatible with known techniques for linearity improvement as presented in section III.2.4 and the calibration can be automatized and implemented in-situ.

Finally, the implementation of this innovating LADC which is detailed in section III.3 occupies a really reduced 0.02mm² size when implemented in CMOS 65nm process while keeping a reasonable consumption under a standard 1.2V low supply voltage.

III.3. Circuit physical implementation

The innovating LADC architecture has been implemented in CMOS 65nm process from STMicroelectronics to be integrated just after the power detector presented in Chapter II, thus giving the digitized power level expressed in dBm. The following section discusses this circuit physical implementation and presents some simulation results.

III.3.1. Implementation overview

Figure III-28 shows the block diagram of the implemented LADC which can be decomposed in several blocks. First the progressive compression logarithmic amplifier (PCLA) integrates 16 amplifier and voltage-to-current converter stages. This PCLA hence generates 16 intermediate voltages from V_{15} down to V_0, in addition to the analog current output I_{out}. Although this analog current output is not necessary for the LADC, it has been kept to be compared to the digital output, thus verifying the effective characteristic of the digitization part.

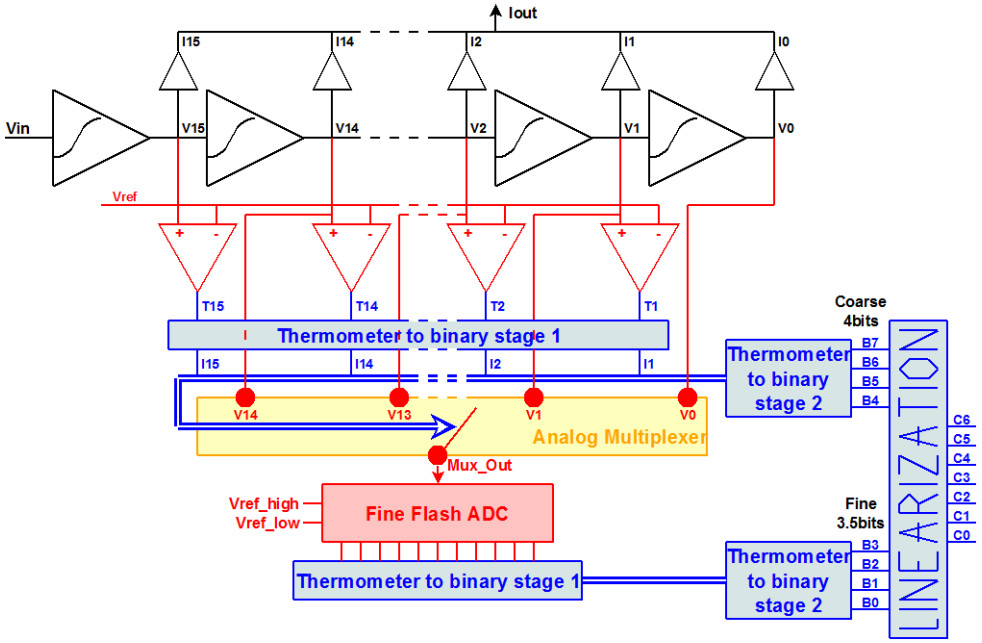


Figure III-28 Overview of the implemented LADC

The intermediate voltages are then compared to a common reference voltage V_{ref}. This corresponds to the coarse analog-to-digital conversion (also called coarse ADC here after). The resulting coarse thermometer code on the 15 digital signals from T_{15} down to T_1 is converted into a classical binary code on 4 digital signals from B_7 down to B_4. This conversion is realized in two phases and hence uses an intermediate digital code on 15 digital signals from I_{15} down to I_1. This intermediate digital code is advantageously used to control the analog multiplexer as can be seen in Figure III-28.

The analog multiplexer then selects the intermediate voltage V_i that is currently linear with respect to the input voltage V_{in} expressed on a logarithmic scale. This selection uses the intermediate digital code previously mentioned and outputs an analog voltage *Mux_Out* which is linear by section with respect to V_{in} expressed on a logarithmic scale.

This multiplexer output voltage is digitized thanks to a classical linear flash ADC. *Mux_Out* is hence simultaneously compared to 10 reference voltages equally distributed between V_{ref_low} and V_{ref_high} and is also compared to V_{ref_high} itself, thus resulting in 11 digital output signals which are also coded on a thermometer scale. The resulting thermometer code is converted into a classical binary code on 3.5 bits (12 possible values) – corresponding to the digital signals B_3 down to B_0 – similarly to the previous thermometer to binary conversion.

Finally, the 8 output digital signals from B_7 down to B_0 are computed in a digital correction logic block to form a continuous linear code on 7 bits from C_6 down to C_0. This correction logic block, called "Linearization" in Figure III-28, has not been integrated on silicon but can be integrated easily in a Field Programmable Gate Array (FPGA) as it is purely digital and the correspondence table can be re-programmed at any time.

III.3.2. Design considerations

i. Progressive compression logarithmic amplifier

The PCLA integrates 16 "compression amplifier" stages, each stage being composed of an amplifier and a voltage-to current converter. The schematic of one compression stage is shown in Figure III-29 and is very close to the solution proposed in [12] (see Figure III-14.a).

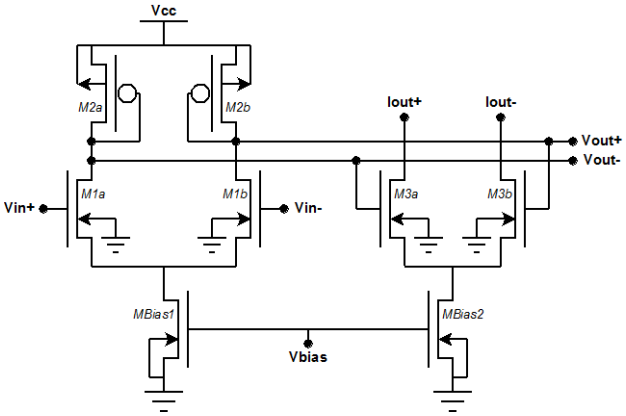


Figure III-29 Schematic of each amplification stage integrated in the PCLA

This compression stage has been designed in CMOS 65nm process from STMicroelectronics using low V_t and low power transistors in RF configuration (lvtlp_rf) in order to be fully compatible with the power amplifier already designed (see section I.2.2.ii) and hence minimize the need for process options. Table III-1 summaries the size of the different transistors used in each compression stage. The width of the transistors M3a and M3b being half the width of the transistors M1a and M1b, the current flowing in the V-to-I converter has also been reduced by half thanks to a reduction of the number of biasing transistors. MBias2 is hence composed of one 1x1 µm² unity biasing transistor while MBias1 includes 2 parallel unity biasing transistors.

Given in µm	**M1a / M1b**	**M2a / M2b**	**M3a / M3b**	**MBias1 / MBias2**
W	5	1	0.5	1
L	5.8	0.4	0.4	1

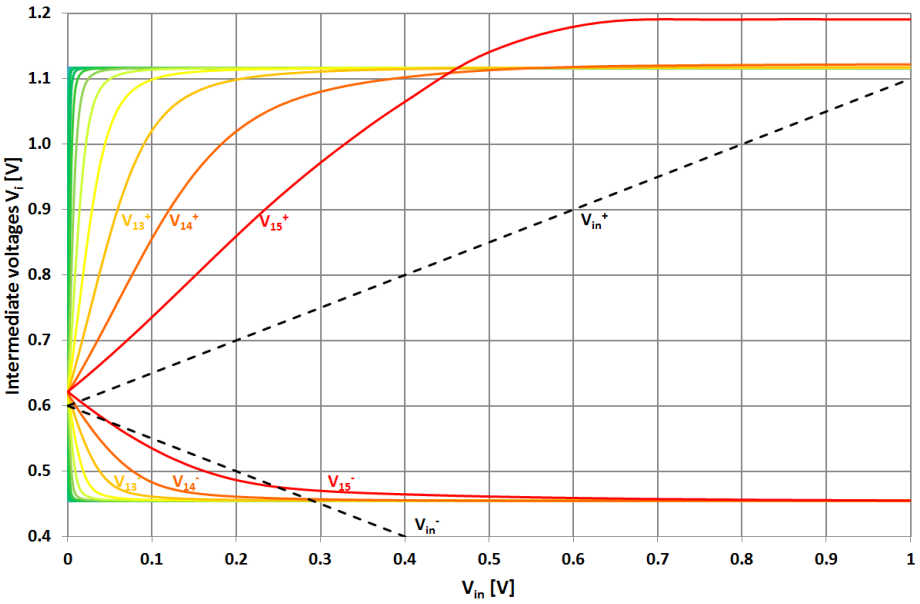
Table III-1 Size of the MOS transistors used in the amplifier and V-to-I converter

As can be seen in Figure III-29, the implemented structure is fully differential which helps in a cascade of amplifiers to overcome the limitations caused by DC offsets on the intermediate voltages. This structure has been simulated considering a 420mV biasing voltage V_{bias}, a 1.2V power supply voltage and a differential input voltage equally split on the negative V_{in}^- and positive V_{in}^+ branches centered on 600mV operating point.

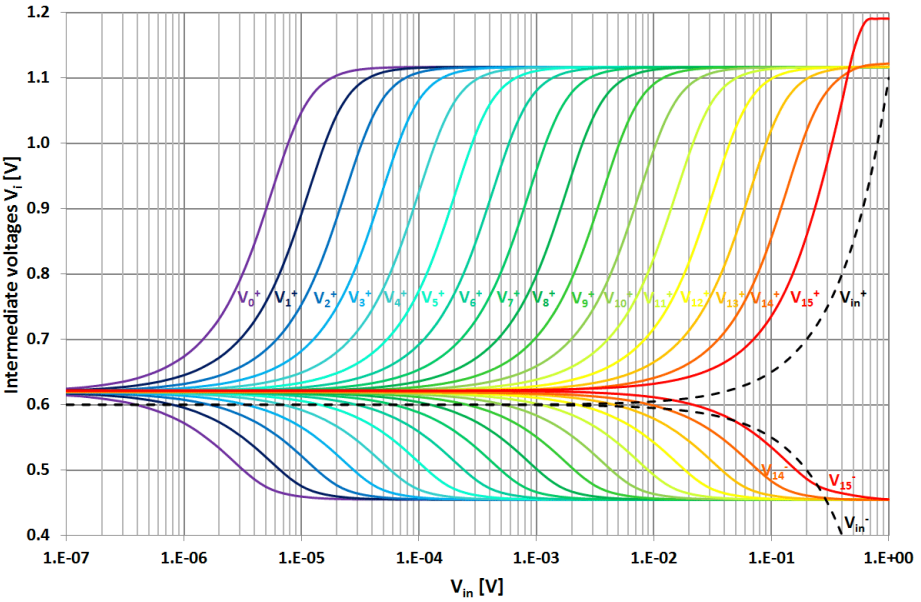
Figure III-30 shows both the positive and the negative intermediate voltages respectively V_i^+ and V_i^- with respect to the differential input voltage V_{in}. On the diagram a. the input voltage is represented on a linear scale while on the diagram b. V_{in} is expressed on a logarithmic scale. The simulated gain of an elementary stage is about 2.06. This can be easily observed on the linear scale of Figure III-30.a where the intermediate voltages are progressively compressed each time on a smaller portion of the V_{in} scale. As a consequence, the output voltages from the 8th up to the 16th stages – respectively V_8^+ and V_8^- down to V_0^+ and V_0^- – are too much compressed on the vertical axis to be

observed on this linear diagram as the corresponding linear gain with respect to the input voltage varies respectively from 320 up to 102790. However, the same intermediate voltages are equally distributed along the V_{in} axis expressed on a logarithmic scale (Figure III-30.b). The linear gain hence effectively corresponds to an offset on a logarithmic scale as introduced in section III.2.1.

The compression of the differential signal V_i is not equally dispatches on the positive V_i^+ and the negative V_i^- branches. The major part of the differential variation actually always occurs on the positive branch as can be seen on the two diagrams of Figure III-30. For this reason it has been decided to perform the different analog-to-digital conversions on the positive intermediate voltages only. The V_i^+ voltages are actually ideally distributed along the V_{in} axis and integrate a wide linear range. Moreover, it is much easier to compare a single-ended signal rather than a differential one.



a. On a linear scale



b. On a logarithmic scale

Figure III-30 Intermediate voltages at the output of each compression stage

The last observation that can be made on those diagrams is the difference of saturation of the first stage with respect to the following stages. The positive output of the first stage V_{15}^+ is actually controlled by the negative input of this first stage V_{in}^-. This negative input varying in a larger range than the other negative intermediate voltages V_i^-, the saturation level of the first stage positive voltage is different than for the other positive intermediate voltages V_i^+. Moreover, there is a difference in the

DC operating point between the input and the output voltages of the first amplifier stage, which also contributes to the difference of shape between the first and the following compression stage outputs.

Finally, the shape of the first stage positive output voltage V_{15}^{+} does not provide a true linear range with respect to the input voltage expressed on a logarithmic scale (Figure III-30.b). It has hence been decided not to implement the selection of this intermediate voltage in the analog multiplexer, not to convert an erroneous curve in the fine ADC, as can be observed in Figure III-28.

Figure III-31 shows the layout of one compression stage. The 9 MOS transistors of the compression stage are integrated in a 21x7µm² rectangle that perfectly imbricates with the identical adjacent compression stages to form the 16 stages PCLA which occupies only 21x117µm².

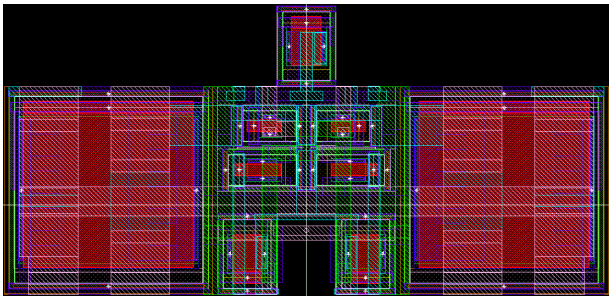


Figure III-31 Layout of one compression stage integrated in the PCLA

ii. Comparator

The implemented LADC widely uses comparators to digitize the analog signals. First the intermediate voltages are compared to a common reference voltage to form the coarse conversion. Then the analog multiplexer output voltage *Mux_Out* is compared to a set of reference voltages in a flash ADC that performs the fine conversion. All the comparators integrated in this LADC are strictly identical and are composed of four different stages following the schematic of Figure III-32.

First, two identical analog amplifiers increase the difference between the two voltages to be compared. Then, the comparator strictly speaking converts the analog voltage difference into a logical '0', meaning the input voltage (V_{in}^{+}) is lower than the reference one (V_{in}^{-}), or a logical '1', meaning the input voltage (V_{in}^{+}) is higher than the reference one (V_{in}^{-}). Finally, a digital latch stage outputs a constant '0' or '1' logical level valuable on the full clock period, the output of the previous stage generating a valuable data only when the clock *CLK* is low – i.e. when $\overline{CLK}$ is high.

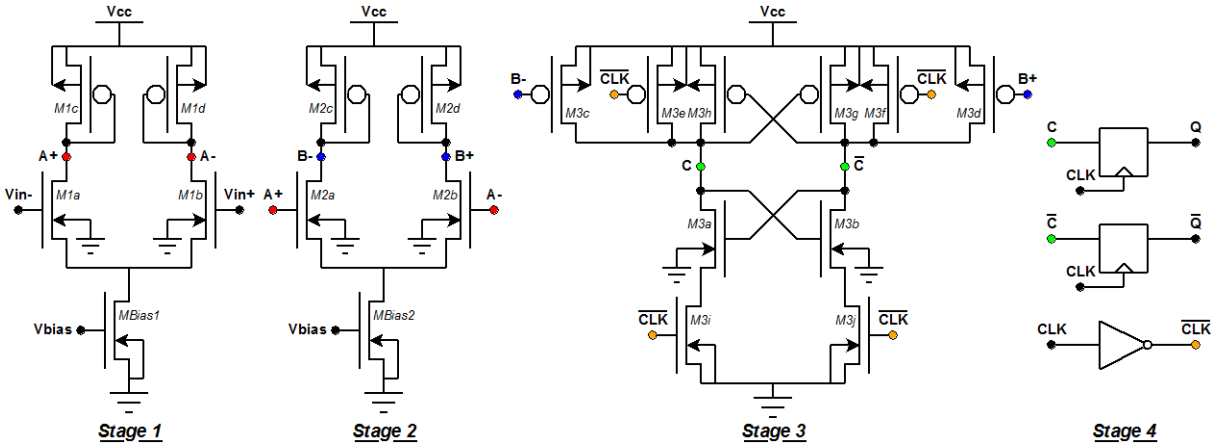


Figure III-32 Schematic of the comparator widely used in the LADC

Here again, only low threshold voltage low power and RF structure (lvtlp_rf) MOS transistors have been used. The different widths and lengths as well as the number of parallel transistors are summarized in Table III-2. It can be noticed that the two first stages are exactly identical. There are also only two different sizes (L & W) of transistors which highly simplifies the layout.

Given in µm	**M1a / M1b M2a / M2b**	**M1c / M1d M2c / M2d**	**MBias1 MBias2**	**M3a / M3b**	**M3c / M3d M3e / M3f M3g / M3h**	**M3i / M3j**
W	1	1	0.5	0.5	0.5	0.5
L	0.5	0.5	0.28	0.28	0.28	0.28
Nb of // MOS	2	1	2	4	2	1

Table III-2 Size of the MOS transistors used in the comparator

The comparator has been simulated with transient ADS simulator – as the comparator needs to be clocked – under RF Design Environment (RFDE). The clock frequency has been fixed to 5MHz. The reference voltage (on V_{in}^-) has been fixed to 1V which is the most difficult voltage level that has to be compared in the fine converter (the closest one to the supply voltage). The input voltage to be compared (on V_{in}^+) follows a succession of 4 different values [-200mV, +5mV, +200mV, -5mV] with respect to the 1V reference voltage, each value being applied during 2.5µs. Such configuration is often used in ADC simulations as it highlights the memory effect of the comparators when changing from a deep difference between the inputs to a light opposite difference. Moreover, considering the 200mV linear variation of V_i^+ and the 4bit fine ADC, 5mV is lower than one LSB. Figure III-33 shows the two input voltages on the left vertical axis and the digital output *Q* on the right vertical axis.

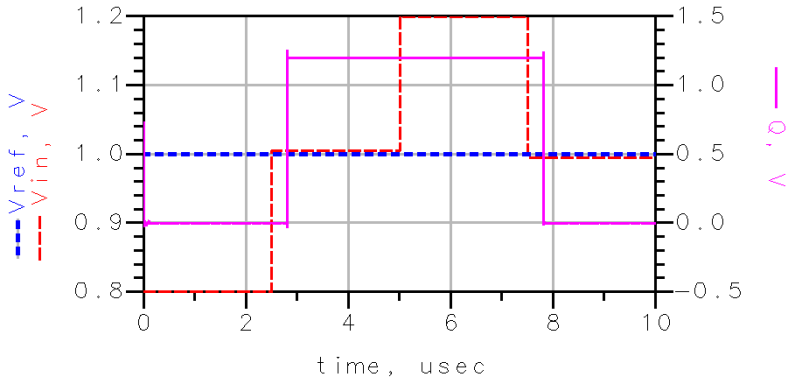
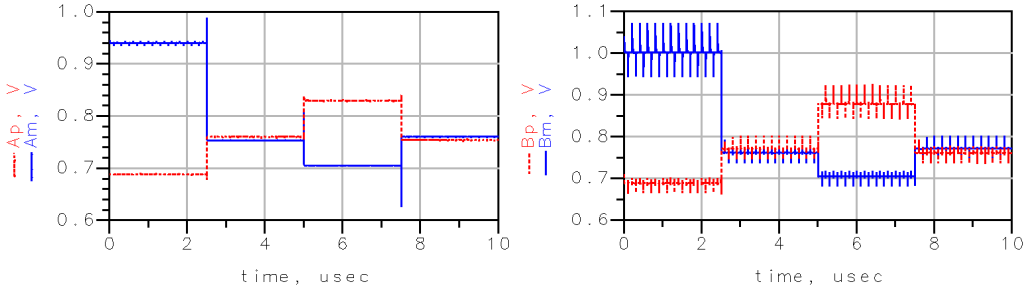


Figure III-33 Simulated digital output of the comparator with respect to the analog input signals

This simulation shows the comparator is able to detect either a +5mV and a -5mV voltage difference between its inputs without any memory effect. The time required before the comparator outputs the good value is directly dependent on the clock frequency. The clock has also a huge effect on the analog signals that are generated by the two amplifier stage in front of the comparator stage. Figure III-34 a. and b. actually show the differential output voltages respectively from the first and the second amplifier stages that can be observed in the simulation conditions presented above. One can notice the output voltages from the second stage are very disturbed by the clock edges as the third stage that is clocked loads the second stage. The clock influence is much lower on the output voltages from the first stage which is not directly loaded by clocked signals. This is why two amplifier stages have been implemented in this comparator. By this way the input voltage is not much affected by the clock signal which is very important in this LADC implementation as the intermediate voltages are directly connected to *Mux_Out* and are hence connected to several comparators in parallel.



a. First stage output **b. Second stage output**

Figure III-34 Simulated analog outputs of the two first stages of the comparator

As introduced previously, the regularity in the sizes of the transistors allows a very compact layout. The layout of the comparator is presented in Figure III-35 and occupies 26.6x7µm². In fact, the height of the comparator has been matched with the high of one compression stage (see above) to minimize the length of the connections for the intermediate voltages V_i between the PCLA and the coarse converter.

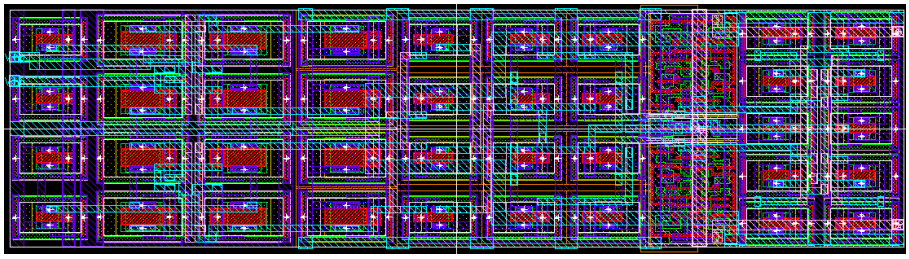
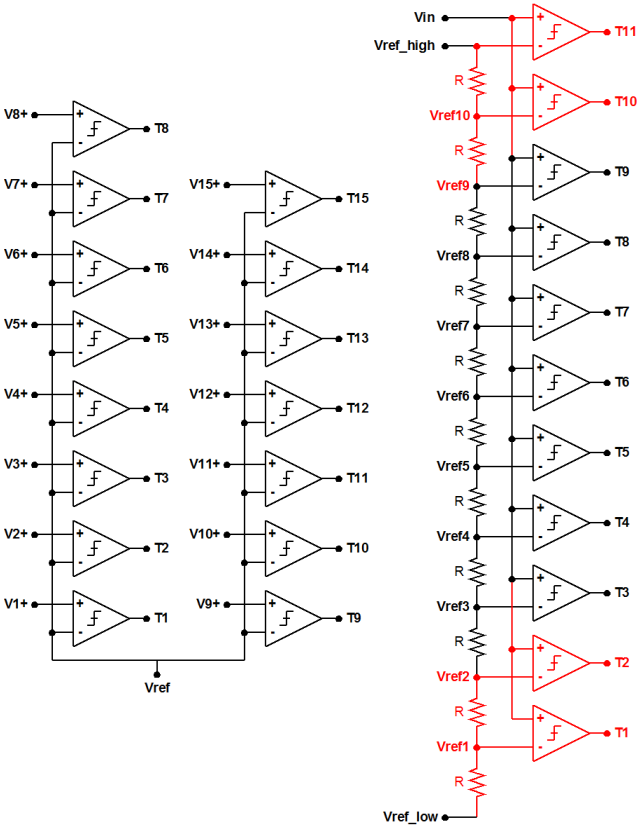


Figure III-35 Layout of one comparator integrated both in the coarse and in the fine converters

iii. Coarse and fine converters

The comparator presented above is used as an elementary block in both the coarse and the fine converters. The coarse converter hence integrates 15 comparators to generate the 15 thermometer coded digital outputs that correspond to 4bits in classical binary representation. All the comparators have a common reference voltage V_{ref} connected on their negative input while the positive inputs are connected to the different intermediate voltages from V_{15}^{+} down to V_1^{+} as can be seen in Figure III-36.a.

The configuration is a little different for the fine converter as it is a classical flash ADC. The positive inputs of the comparators are, this time, all connected together to the input voltage V_{in} to be converted which is the analog multiplexer output *Mux_Out* in practice. The negative inputs of the comparators are connected to a set of reference voltages from V_{ref1} up to V_{ref10} generated by a resistive network (each resistance is 10kΩ) between two external reference voltages V_{ref_low} and V_{ref_high} as can be seen in Figure III-36.b.



a. For the coarse 4bits **b. For the fine 3.5bits**

Figure III-36 Implementation of the coarse and fine converters

The fine converter integrates 11 comparators. 7 of them (3bits) are distributed along the theoretical linear segment of *Mux_Out* which should be obtained if all components are ideal. The four remaining comparators (corresponding to the '.5' indication when speaking of the 3.5bits fine converter), two above and two under the previous series of 7 comparators, which are highlighted in Figure III-36.b, create an overlap between the range of two successive segments in order to be able to linearize the LADC after a calibration phase (see section III.2.4).

The power supply network and the biasing circuitry are not represented in Figure III-36 a. and b., but obviously all the supply voltages are connected together to 1.2V and all the biasing voltages are also connected together and tied to an external 420mV reference voltage.

Both coarse and fine converters being an assembly of identical comparators (layout in Figure III-35), the area is proportional to the number of comparators which are integrated. The coarse converter occupies hence 27x113µm² while the fine flash ADC occupies 28x78µm², the 1µm additional width corresponding to the resistive network.

iv. Thermometer to binary code converters

The digital outputs from the coarse and the fine converters detailed above are generated as thermometer codes that have to be converted into classical binary codes to form the digital output of the LADC. The two thermometer to binary code conversions are similar and use the principle exposed in [16] of a two steps conversion. The first step that has been implemented is similar to the pre-encoder developed in [16]. It converts the thermometer code where the value is given by the number of thermometer bits T_i settled at '1' into an intermediate code where only one intermediate bit I_i is settled to '1' and the value is given by the location of this unique '1' among the bus of intermediate bits from I_1 up to I_{15}. This intermediate code is then converted into the classical binary code. The implementation of this second step conversion is quite different from [16] as it is performed with logical gates rather than directly at the transistor level.

State	Thermometer Code															Intermediate Code															Binary Code			
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}	B_7	B_6	B_5	B_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0
5	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1
6	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
7	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0
9	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1
10	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0
11	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1
12	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0
13	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Table III-3 Thermometer to 4bits binary code conversion table

The truth table of this two-step conversion is presented in Table III-3 for the 4bits of the coarse conversion. The 15 thermometer bits from T_1 up to T_{15} are first converted into 15 intermediate bits from I_1 up to I_{15} following the rule given in equation (III.8).

$$\forall i \in [2;15], I_i = T_{i-1}.\overline{T_i} \;;\; I_1 = \overline{T_1}.\overline{T_2} \tag{III.8}$$

Those 15 intermediate bits are then converted into 4 binary bits from B_4 up to B_7 that form the 4 most significant bits (MSB) of the LADC output following the equation (III.9).

$$\begin{cases} \overline{B_4} = (I_1 + I_3 + I_5 + I_7) + (I_9 + I_{11} + I_{13} + I_{15}) \\ \overline{B_5} = (I_1 + I_2 + I_5 + I_6) + (I_9 + I_{10} + I_{13} + I_{14}) \\ \overline{B_6} = (I_1 + I_2 + I_3 + I_4) + (I_9 + I_{10} + I_{11} + I_{12}) \\ \overline{B_7} = (I_1 + I_2 + I_3 + I_4) + (I_5 + I_6 + I_7 + I_8) \end{cases} \tag{III.9}$$

State	Thermometer Code											Intermediate Code												Binary Code			
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0
3	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1
4	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
5	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
6	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0
7	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1
8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
9	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1
10	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0
11	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Table III-4 Thermometer to 3.5bits binary code conversion table

Table III-4 presents the truth table of the two step thermometer to binary code conversion for the 3.5bits of the fine ADC. The conversion rules are similar to the ones given previously for the 4bits of the coarse conversion.

The two steps for this thermometer to binary code conversion have been implemented using standard cell logic gates in our targeted CMOS 65nm technology. Figure III-37 shows the implementation of those two thermometer-to-binary code conversions.

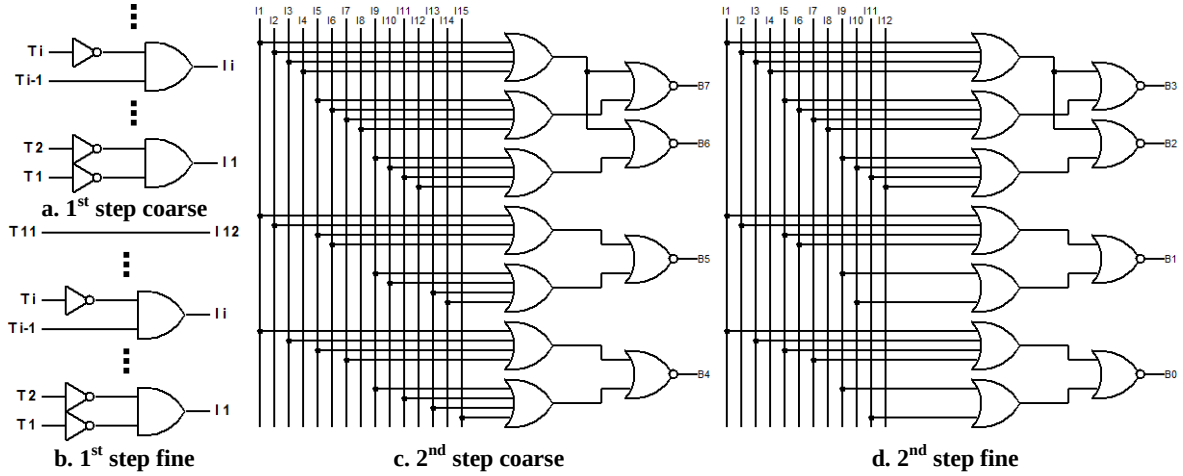


Figure III-37 Implementation of the two steps of the thermometer to binary conversion

v. Analog multiplexer

The analog multiplexer uses the intermediate bits from I_1 up to I_{15} generated by the first step of the coarse thermometer to binary code converter to select the intermediate voltage from V_0^+ up to V_{14}^+ generated by the PCLA which is in its linear range with respect to the LADC input voltage expressed on a logarithmic scale. The selected intermediate voltage is then directly used as the input voltage of the fine ADC as can be seen in Figure III-28.

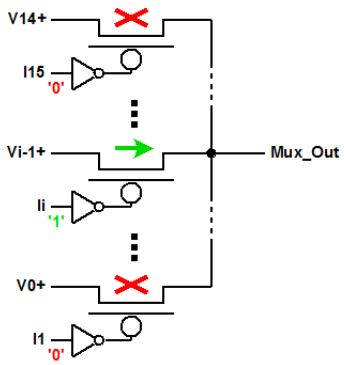


Figure III-38 Schematic of the analog multiplexer

This analog multiplexer has been implemented very simply following the schematic of Figure III-38 using NOT logical gate and 8.02x0.2µm² (*W*x*L*) with 4 fingers plvtlp_rf PMOS transistors. As introduced in the previous subsection, at any time only one intermediate bit I_i is 'on', the other being 'off' which means only one PMOS transistor is open. *Mux_Out* is hence connected to only one intermediate voltage V_i^+ at a given instant.

Mux_Out being directly connected to a given intermediate voltage V_i^+ and to the fine ADC input, this intermediate voltage is loaded by the comparators that form the fine ADC. Changing the selected intermediate voltage generates hence a high current consumption peak on the two intermediate voltages concerned. This current consumption peak affects the result of the coarse conversion which means the intermediate voltage to be selected. An instable loop can hence be formed around the coarse converter and the analog multiplexer.

A series of laches clocked at a lower frequency (1MHz as an example) has hence been integrated between the intermediate bits generated by the first step thermometer to binary code conversion and the same intermediate bits used in the analog multiplexer. By adding a delay in the loop, the two concerned intermediate voltages have now enough time to overcome the load impedance change and the associated peak current consumptions before the intermediate voltage selection being re-evaluated. The intermediate voltage selection loop is hence stabilized.

In practice, there is no necessity to implement a second clock signal. The need is only to integrate a delay between the coarse conversion and the segment selection, and eventually to lower down the frequency of the full LADC. However, having an independent clock signal for the segment selection can be useful in the first circuit implementation of this innovating LADC architecture.

vi. Physical implementation of the full LADC

The layout of the full LADC occupies only 82x120µm² and is presented in Figure III-39. On this figure can be recognized from top to bottom: first, the PCLA composed by 16 compression stages; then comes the coarse converter composed by the series of 16 comparators; the analog multiplexer then comes just after the first step of thermometer to binary code converter for the 4bits coarse conversion outputs as the analog multiplexer uses the intermediate bits of the thermometer to binary conversion; and finally the fine ADC composed of 12 comparators lies at the bottom. The other thermometer to binary code converters are integrated on the left bottom of the figure with a series of latches that synchronize the 8 output bits of the LADC.

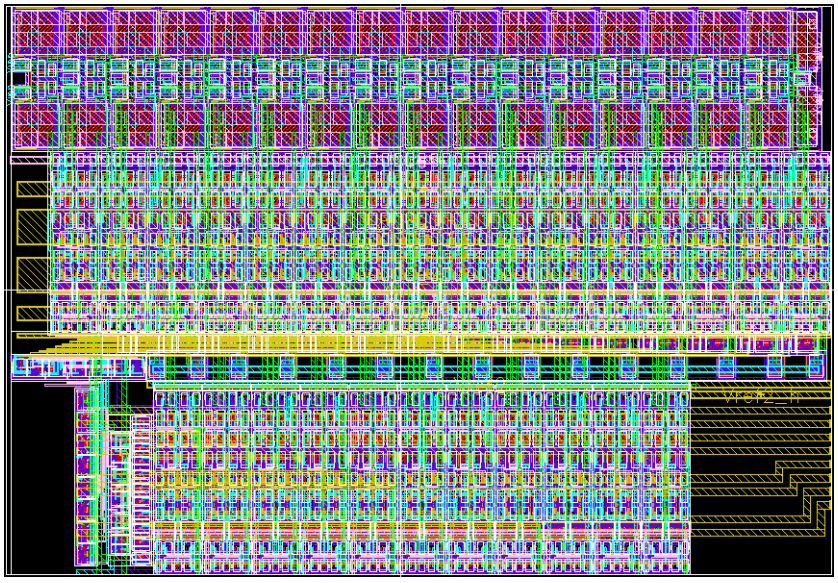


Figure III-39 Layout of the full LADC

in Figure III-39, the differential input voltage is located on the top left corner and the digital output is located on the bottom left corner and are redirected by M5 connections (in yellow) to the bottom right corner. The analog output from the PCLA is located on the top right corner.

III.3.3. Transient simulations

i. Simulation conditions

The designed LADC has been simulated with transient ADS simulator (under RFDE) as the comparators need a clock signal in the time domain to work. The input voltage V_{in}^- has been fixed to 700mV as a reference, while V_{in}^+ follows a decreasing exponential law (using VtExp device from adsLib with 0V V_{low}, 600mV V_{high}, 0s *Delay1*, 100ns *Tau1*, 1µs *Delay2* and 22µs *Tau2*). Although a constant V_{in}^- increases the asymmetry in the dispatching of the differential intermediate voltages V_i between the positive V_i^+ and the negative V_i^- branches, this approximately corresponds to the use of case of this LADC where the LADC is used to digitize the voltage difference between an active RMS power detector and an identical second one used as reference (see the configuration of Figure IV-10).

The biasing voltage which is common to the PCLA and all the comparators has been fixed to 420.8mV by a very simple polarization circuit composed of a 16kΩ resistance in series with a NMOS diode connected transistor (in practice, 8 parallel 1x1µm² nlvtlp_rf transistors) between the 1.2V supply voltage and the ground.

The reference voltages have been fixed to 800mV for the coarse converter reference voltage V_{ref1}, and to 764mV and 1.005V for respectively the low (V_{ref2_l}) and the high (V_{ref2_h}) reference voltages of the fine flash ADC. V_{ref2_l} and V_{ref2_h} are calculated to match the 2nd fine flash reference voltage (V_{ref2} in Figure III-36.b) to the reference voltage of the coarse converter V_{ref1} and the 10th reference voltage (V_{ref10} of the fine converter) to the ideal highest level of *Mux_Out* considering a fully linear LADC. This hence results in additional levels in the fine flash converter which are used to calibrate the LADC as detailed in III.2.4.

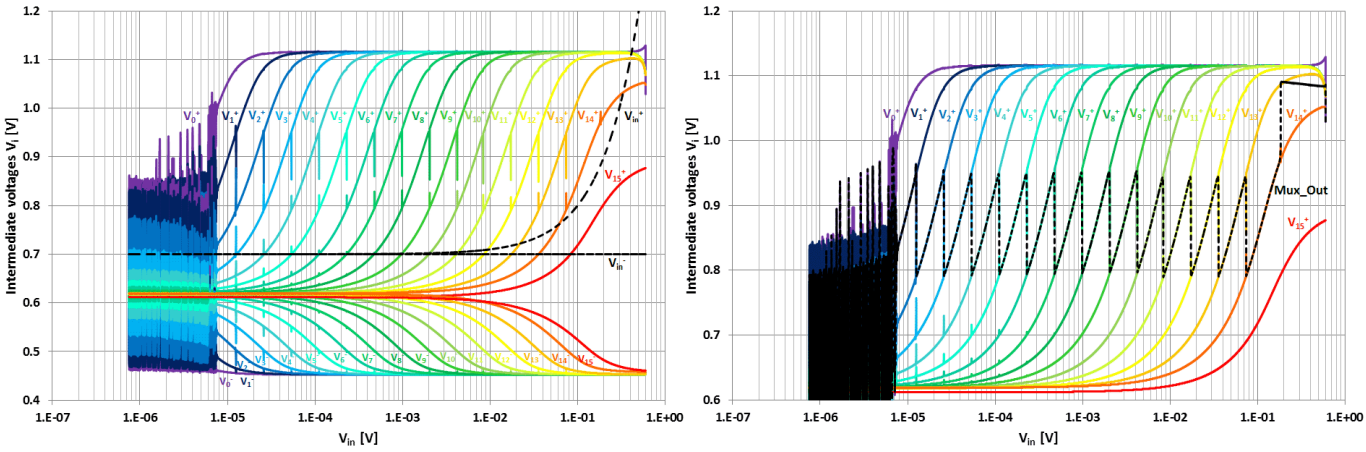
The LADC is synchronized by two different clock signals. The high speed clock *CLK_h* is used by all the comparators and has been fixed to 8MHz in this transient simulation. The low speed clock *CLK_l* is used by a series of latches on the digital inputs of the analog multiplexer to stabilize the intermediate voltage selection (see section III.3.2.v) and also by a series of latches on the 8 digital output bits from D_0 up to D_7 to form a synchronous digital output.

The transient simulation has been performed on 300µs which is relatively long for a transient simulation with 8MHz maximum clock frequency. But this simulation time corresponds to less than 2 cycles of *CLK_l* for each digital output code when considering the 7.5 bits of the digital output with a 1MHz *CLK_l* frequency. However this simulation needs about 5 hours of computation on a 4 cores CPU and 8Go RAM memory redhat40 Sun station as 455000 time steps have been calculated for the 3677 transistors defined with BSIM4 model.

All the following curves have been represented with respect to the differential input voltage V_{in} expressed on a logarithmic scale rather than with respect to the time as it is much easier to understand the functioning of the LADC in a DC simulation point of view rather than directly in transient analysis. The transient analysis is only chosen for the comparators to work properly.

ii. Analog intermediate voltages

The positive and negative input voltages, respectively V_{in}^+ and V_{in}^-, have been represented in Figure III-40.a with all the positive and negative intermediate voltages of the PCLA from V_0^+ and V_0^- up to V_{15}^+ and V_{15}^-. As introduced in section III.3.2.i, the negative intermediate voltages have a much lower variation that the positive intermediate voltages and can hence not be considered during the suite of the analysis. However, once can notice the about 100mV difference between the input voltages and the intermediate voltages at the operating point ($V_{in}=0$) which highly affects the output not only of the first stage of voltage compression in the PCLA, but also the second stage. This effect has already been discussed in section III.3.2.i but with reduced impacts as the voltage difference was smaller than in this simulation (see Figure III-30.b).



a. Intermediate voltages V_i^+ and V_i^- **b. Intermediate voltages and analog multiplexer output**

Figure III-40 LADC analog internal signals obtained by transient simulation

All the intermediate voltages suffer from some glitches in their linear working range (with respect to V_{in} on a logarithmic scale) specially the intermediate voltages of the latest PCLA stages. Moreover, those glitches become so high when V_{in} is lower than 8µV that the intermediate voltages does no more result from a regular offset on the V_{in} axis expressed on a logarithmic scale. Those glitches actually result from the intermediate voltage selection in the analog multiplexer as can be seen in Figure III-40.b where the multiplexer output voltage *Mux_Out* has been represented simultaneously with the positive intermediate voltages. The location of the glitches effectively well correlates to the discontinuities of *Mux_Out*.

A solution would be to slow down the low speed clock frequency *CLK_l* in order to increase the available time for the intermediate voltages to reach their final value after a change in the selection of the intermediate voltage used for the fine converter. This should effectively increase the stability of the intermediate voltage selection as explained in the section III.3.2.v. This solution has been verified with conclusive results on a reduced simulation time. However reducing the frequency of *CLK_l* would require a much longer simulation time to be able to obtain all the possible digital output code which would drastically increase the time required to perform the full simulation. This solution has hence not been implemented in the actual simulation. However some better performance can be expected during the measurements with a much lower frequency of *CLK_l*.

iii. Digital output signals

Figure III-41.a shows the digital output bits from D_0 up to D_7 (D_0 up to D_3 from the fine converter and D_4 up to D_7 from the coarse converter). Those individual bits have been computed to form a unique digital output code ranging from 0 up to 256 (8bits) which is illustrated in Figure III-41.c. A linear tendency curve has also been represented to verify the linearity of the conversion (still with V_{in} on a logarithmic scale). The digital code changes most of the time by small steps of one LSB, but also by large steps at each new intermediate voltage selection with some codes that never occur. The fine converter being a 3.5bits ADC, the 4bits fine digital output codes from "1100" up to "1111" actually never appears, which results also in some missing codes at the global LADC output.

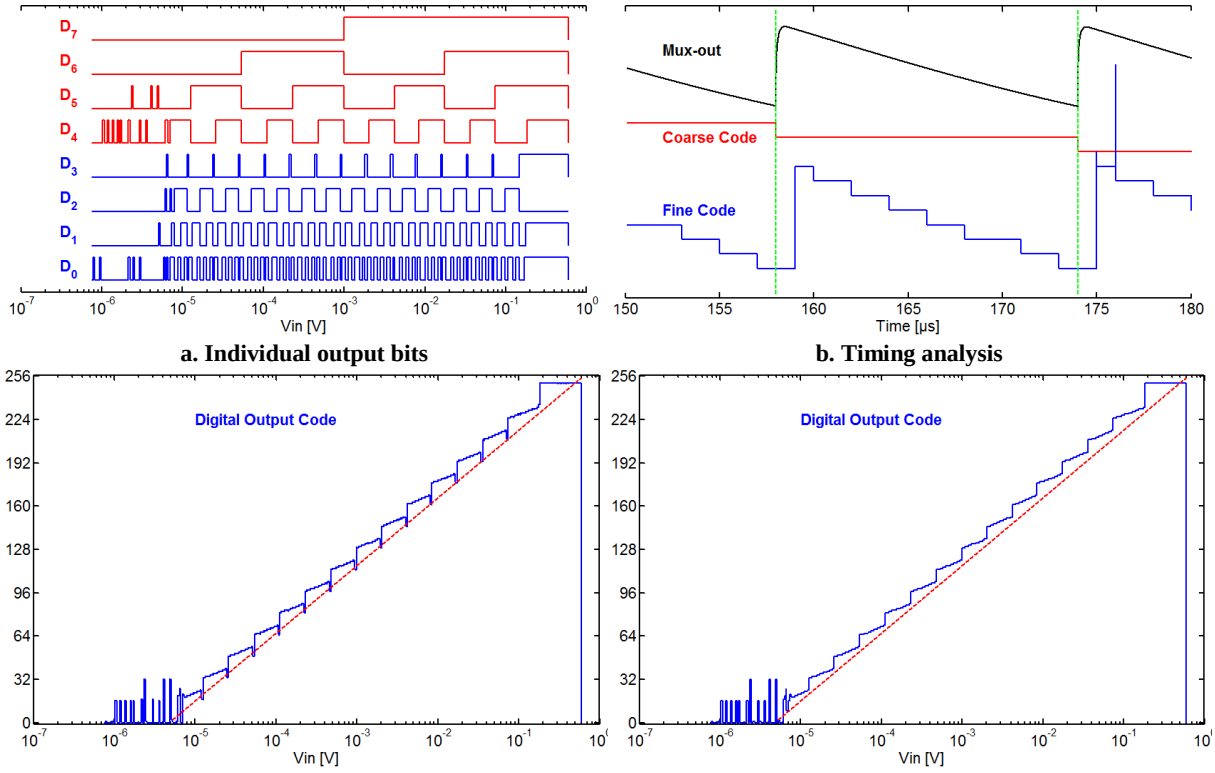
Those curves have to be balanced with the quick evolution of the input voltage and with the restricted number of cycles of *CLK_l* for each output digital code which can create some unexpected values as the input voltage can have changed between the evaluation by the coarse converter – i.e. the intermediate voltage selection – and the evaluation by the fine converter.

Moreover, when considering the fine and the coarse codes – computed respectively from D_0 up to D_3 and from D_4 up to D_7 – in the time domain simultaneously with the multiplexer output voltage *Mux_Out* (see Figure III-41.b), one can observe the synchronization between the coarse and the fine bits is not perfect. When the coarse code changes, the multiplexer output voltage is actually connected to a different intermediate voltage V_i (new selection). This selection change is not performed instantaneously as *Mux_Out* is charged by the fine converter which means by a capacitive load. *Mux_Out* hence progressively charges the capacity formed by the fine converter before reaching its

new intermediate voltage V_i level. When *Mux_Out* is digitized through the fine converter on a rising edge of *CLK_l*, *Mux_Out* is not yet charged to its new value resulting in an erroneous fine code or more exactly a fine code which does not corresponds to the actual value of the coarse code.

A simple latch operation needs hence to be applied on the coarse code to correct this issue. This latch additional step has not been integrated in-situ and has hence to be realized outside the chip directly on the LADC 7.5bits output code formed by the bits from D_0 up to D_7. When applying this additional latch on the coarse code, the unexpected values that were observed on the digital output code at each coarse code change (see Figure III-41.c) are removed. The corrected digital output code, represented in Figure III-41.d, is now perfectly linear with respect to the LADC input voltage expressed on a logarithmic scale.

A careful study – which is not detailed here – on the fine code (from D_0 up to D_3) can show that the additional comparison levels integrated at both ends of the fine converter range to be able to calibrate the LADC are effectively useful. The codes "0000", "0001", "1010" and "1011", which correspond to those additional steps outside the ideal range, are actually generated by the fine converter.



a. Individual output bits **b. Timing analysis**

c. Digital output code **d. Corrected digital output code**

Figure III-41 LADC digital outputs obtained by transient simulation

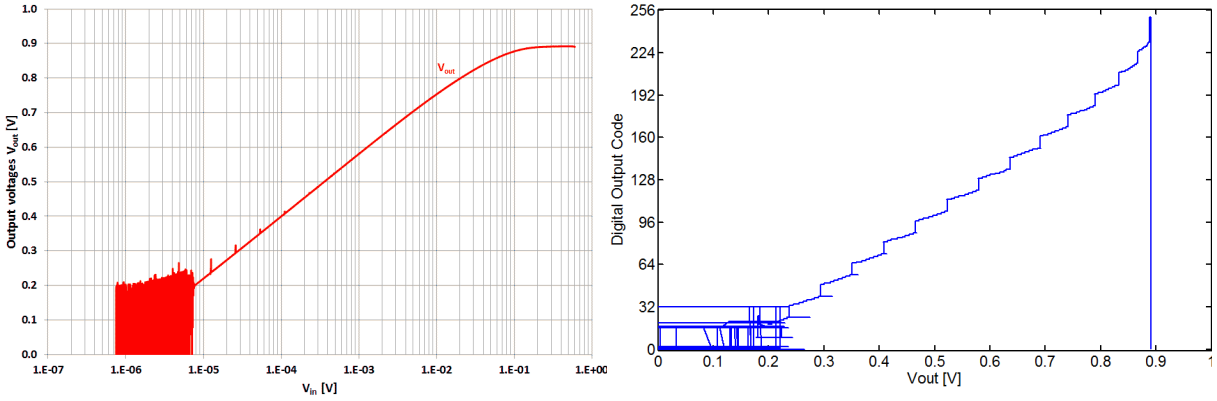
iv. Analog output voltage

Figure III-42.a shows the analog output voltage V_{out} of the LADC (the output of the PCLA) with respect to the input voltage V_{in} of the LADC expressed on a logarithmic scale. For V_{in} under 8µV, V_{out} also suffers from the instability generated by the intermediate voltage selection. However the V_{out} Vs. $log(V_{in})$ characteristic is still linear on about 4 decades which should be sufficient for our application.

Moreover, this analog output voltage V_{out} is quite interesting to be kept in addition to the digital output code as it gives information which can be used to verify the digitization operation in the LADC. Figure III-42.b actually shows the digital output code with respect to the analog output voltage. The instability introduced above also creates some errors under the value 32 of the digital output code which should not be considered. However, this curve shows the digitization operation regardless of the input voltage which may not be accessible in a fully integrated chip (see Chapter II).

But this characteristic is not fully linear especially for the upper range of the dynamic range. The digital code actually reaches more values for high levels of the output voltage that for low levels

of the output voltage. This can be explained by the fact that V_{out} is converted from the sum I_{out} of all the individual output currents of the different compression stages. This current-to-voltage conversion is performed thanks to an active network which saturates for high levels of the output voltage. This V-to-I converter is hence less linear than our digitization architecture.



a. Analog output voltage Vs. input voltage **b. Digital output code Vs. analog output voltage**

Figure III-42 Analog output voltage obtained by transient simulation

III.3.4. Frequency and noise limitations

i. Frequency considerations

An AC simulation is performed on the PCLA integrated in the LADC in order to determine the bandwidth of the analog part of this LADC. A 700mV DC voltage is applied on the PCLA negative input and a 1V amplitude AC signal is applied on the PCLA positive with respect to the negative input, thus resulting in a single-ended excitation, which is much closer to the configuration in which is used this PCLA (see Figure IV-10.a in section IV.2.1.ii). Figure III-43 shows the resulting positive intermediate voltages V_i^+, at the output of the different compression stages.

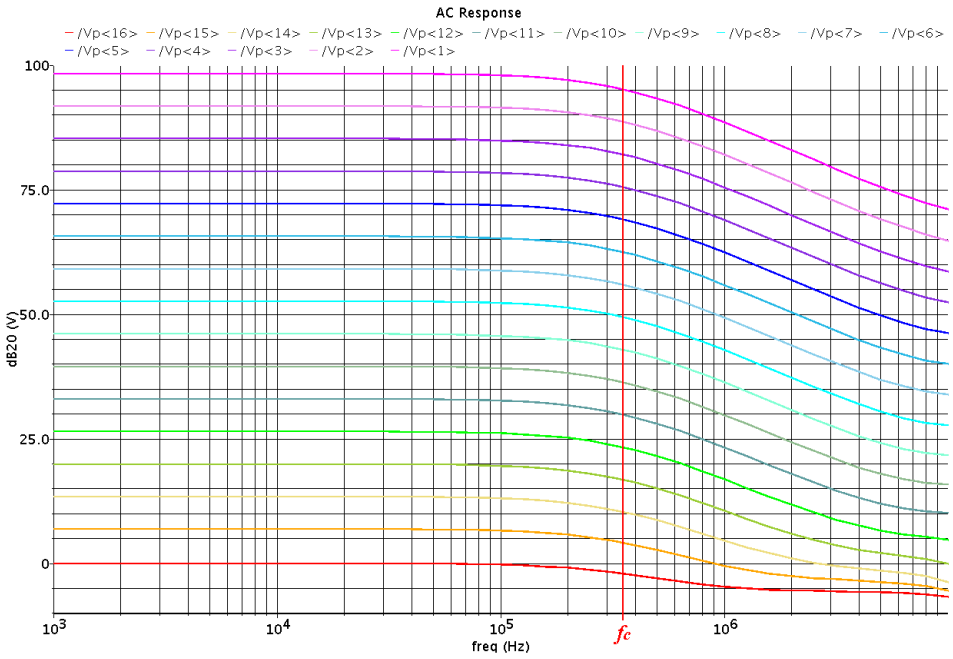


Figure III-43 AC simulation of the PCLA – intermediate voltages V_i

As can be seen on this figure, the first compression stage presents a unity voltage gain (0dBv) whereas the 15 following compression stages exhibit a voltage gain of 2 (6dBv). This difference actually results from the single-ended to differential conversion which is performed by this first compression stage. This first stage hence exhibits the same voltage gain that the 15 following stages.

To conclude on this AC simulation, one can calculate the cutoff frequency of the PCLA. The 16 compression stages being identical, they all exhibit the same bandwidth which is found to be 340kHz. This is also the bandwidth of the complete PCLA.

ii. Noise considerations

The same configuration with a DC voltage on the PCLA negative input and an AC voltage on the PCLA positive input is used to perform a noise simulation. Figure III-44 shows the resulting noise spectral density (given in [V²/Hz]) of V_0^+, the positive output of the last compression stage of the PCLA (see Figure III-28 and Figure III-30).

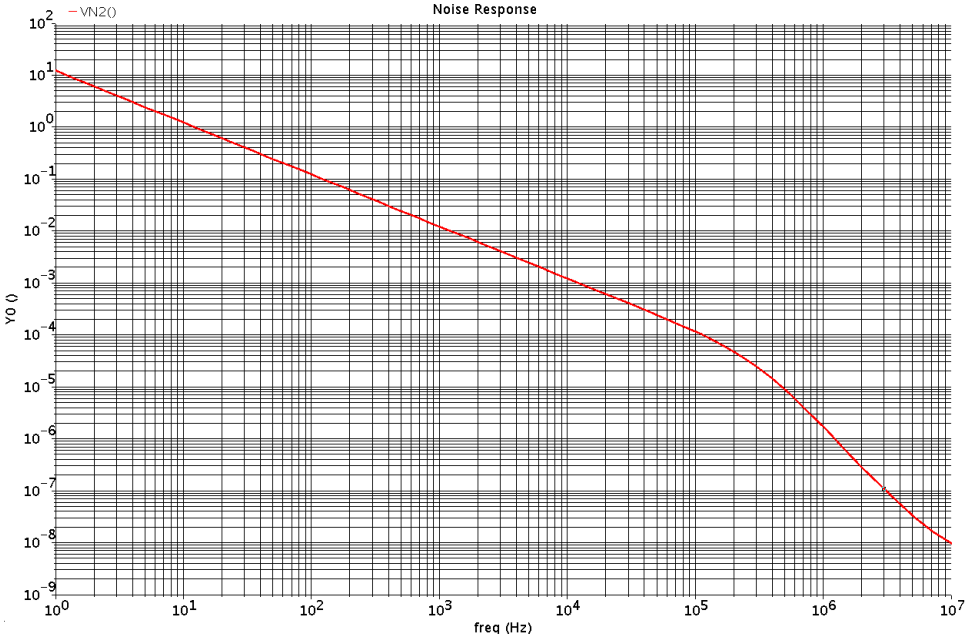


Figure III-44 Noise simulation of the PCLA – noise spectral density (in V²/Hz) of the PCLA output V_1

The noise at the output of the PCLA is hence mostly composed of *1/f* noise. This *1/f* noise is then attenuated at frequencies higher than the 340kHz cutoff frequency of the PCLA. However there is still 1.75e-6 V²/Hz output noise at 1MHz.

One can calculate the total noise level $VN_{RMS\ @\ the\ output}$ in [V] simply by integrating the noise spectral density on the appropriated bandwidth. Considering the frequency band from 1Hz up to 340kHz, one actually obtains 12.46V of $VN_{RMS\ @\ the\ output}$.

This noise level can then be referred to the PCLA input simply by dividing by the gain of the full amplifier chain, which is 82 508 in our case. The noise level referred on the PCLA input considering the frequency band from 1Hz up to 340kHz, $VN_{RMS\ @\ the\ input}$ is hence 151µV.

This reduces the dynamic range of the PCLA, which means the LADC dynamic range, to almost 3 decades, which has to be compared to the initial 5 decades obtained in the transient simulations (see Figure III-42).

Chapter conclusion

This chapter has presented a novel architecture of Logarithmic Analog-to-Digital Converter (LADC), which has been patented in the early 2010 [**17**]. This architecture takes advantage of the specificities of the intermediate signals generated by a Progressive Compression Logarithmic Amplifier (PCLA).

The intermediate signals characteristics are actually regularly spaced along the PCLA input signal expressed on a logarithmic scale. This first specificity is used to perform a first step of digitization, which is a coarse conversion.

Then the intermediate signals characteristics, with respect to the PCLA input signal still expressed on a logarithmic scale, all present the same shape, which integrates a linear zone. This second specificity is used to perform a second step of digitization. After a selection of the intermediate signal which is effectively in its linear zone, a classical linear flash ADC performs the fine conversion.

This architecture could certainly be improved with the help of specialists in the ADC design. Adding a track-and-hold circuit on the input signal, as an example, could stabilize the signal to be digitized. In the same way, buffering the intermediate signals with simple follower OPAs could isolate the clocked comparators, integrated in the two coarse and fine digitization stages, from the analog PCLA, and so improve both the performance of the PCLA and of the digitization stages. Moreover, the global performance of this LADC could probably be improved too by a more careful design of the different parts.

However, this novel architecture of LADC still presents several advantages, which can be summarized in one word: flexibility. The dynamic range can actually be modified by increasing the gain of each elementary compression stage, or by adding or removing compression stages in the PCLA. This second solution also modifies the resolution of the LADC as it modifies the number of comparator integrated in the coarse converter. The resolution of the complete LADC can also be increased simply by increasing the resolution of the classical linear fine converter. For certain applications which do not require too much resolution, this fine ADC can also be wholly removed.

In practice, this LADC architecture has been implemented in 65nm CMOS process from STMicroelectronics with 16 compression stages, which means 4bits of coarse conversion, and a 3.5bits fine flash ADC. This implementation hence generates 7bits, the lost 0.5bit being used to correlate the 3.5bits coming from the fine ADC with the 4bits coming from the coarse conversion following a known linearization technique.

Simulation results shows that the LADC exhibits more than 4.5 decades of linear dynamic range; which are reduced to 3 decades considering the noise generated by the PCLA.

To conclude, this LADC has been integrated twice in the circuit PADet60G, which aims to regulate the gain of a PPA depending on the antenna impedance mismatch (see Chapter IV). Some measurement results can be found in section IV.4.3.

Chapter references

[1] S. Cantarano and G. V. Pallottino, "Logarithmic Analog-to-Digital Converters: A Survey," *IEEE Transactions on Instrumentation and Measurement*, vol. 22, no. 3, pp. 201-213, Sep. 1973.

[2] S. Ben-Yaakov and J. Chen, "An RC Logarithmic Converter-Digitizer," *IEEE Transactions on Instrumentation and Measurement*, vol. 27, no. 1, pp. 24-26, Mar. 1978.

[3] J. Lee, et al., "A 2.5mW 80dB DR 36dB SNDR 22MS/s Logarithmilc Pipeline ADC," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, Kyoto, Japan, Jun. 2007, pp. 194-195.

[4] L. Hemandez and S. Paton, "A continuous-time noise-shaping modulator for logarithmic AD conversion," in *IEEE International Symposium on Circuits and Systems (ISCAS 1999) Proceedings*, vol. 2, Orlando, FL, USA, May 1999, pp. 364-367.

[5] Y. C. Huang, H. H. Hsieh, and L. H. Lu, "A Build-in Self-Test Technique for RF Low-Noise Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1035-1042, May 2008.

[6] "Low Cost, DC to 500MHz, 92dB Logarithmic Amplifier," Analog Devices Datasheet AD8307, Jul. 2008.

[7] S. Khorram, A. Rofougaran, and A. A. Abidi, "A CMOS Limiting Amplifier and Signal-Strength Indicator," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, Kyoto, Japan, Jun. 1995, pp. 95-96.

[8] S. Wongnamkam, A. Thanachayanont, and M. Krairiksh, "A 2.4GHz 43dB CMOS Logarithmic Amplifier for RF Signal Level Detection," in *IEEE 5th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, vol. 2, Krabi, Thailand, May 2008, pp. 725-728.

[9] C. C. Lin, K. H. Huang, and C. K. Wang, "A 15mW 280MHz 80dB Gain CMOS Limiting/Logarithmic Amplifier With Active Cascode Gain-Enhancement," in *IEEE Proceedings of the 28th European Solid-State Circuits Conference (ESSCIRC 2002)*, Florence, Italy, Sep. 2002, pp. 311-314.

[10] K. A. Townsend, J. W. Haslett, and J. Nielsen, "A CMOS Integrated Power Detector for UWB," in *IEEE International Symposium on Circuits and Systems (ISCAS 2007)*, New Orleans, LA, USA, May 2007, pp. 3039-3042.

[11] C. D. Holdenried, J. W. Haslett, J. G. Mc Rory, R. D. Beards, and A. J. Bergsma, "A DC-4-GHz true logarithmic amplifier: theory and implementation," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 10, pp. 1290-1299, Oct. 2002.

[12] M. Shaterian, A. Abrishamifar, and H. Shamsi, "A programmable true piecewise approximation logarithmic amplifier," in *IEEE International Conference on Microelectronics (ICM)*, Marrakech, Morocco, 2009, pp. 90-93.

[13] E. Nash, "Logarithmic Amplifiers Explained," Analog Devices Ask the Applications Engineer Analog Dialog 33-3, no. 28, 1999. [Online]. http://www.analog.com

[14] "1MHz to 10GHz, 45dB Log Detector/Controller," Analog Devices Datasheet AD8319, Apr. 2008.

[15] B. S. Song, S. H. Lee, and M. F. Tompsett, "A 10-b 15-MHz CMOS Recycling Two-Step A/D Converter," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1328-1338, Dec. 1990.

[16] J. Choudhury, C. Cavanaugh, and G. Seetharaman, "An Efficient Encoding Scheme for Ultra-Fast Flash ADC," in *IEEE Topical Conference on Wireless Communication Technology*, Honolulu, HI, USA, 2003, pp. 38-39.

[17] J. Gorisse, A. Cathelin, A. Kaiser, and E. Kerhervé, "Progressive Compression Logarithmic Analog-to-Digital Converter," French Patent UNKNOWN, On-going (2010).

Chapter IV. VSWR Regulation

Chapter introduction

Chapter I has presented the general context of this thesis and has introduced the system specifications. The system should actually be able to protect the power amplifier up to 7:1 VSWR and should be able to regulate and optimize the PA performance up to 3:1 VSWR.

A power detection circuit has then been presented in Chapter II to work as the antenna impedance sensor. A first circuit implementation has been realized in 65nm CMOS process from STMicroelectronics, which exhibits 25dB linear detection range. Load-pull measurements have also proved that the circuit was able to detect up to 3:1 VSWR, limited by the measurement equipment.

Chapter III has then exposed a novel architecture of Logarithmic Analog-to-Digital Converter, which can be used to linearize and digitize the analog signal generated by the power detector circuit.

The present chapter now explores the system in its wholeness, which aims to regulate a power amplifier against antenna impedance mismatches. After a brief state-of-the-art on the different existing solution to regulate the impedance mismatch, a novel architecture is proposed. This architecture uses notably two power detection circuits such as the one presented in Chapter II, and two LADCs such as the one presented in Chapter III, to implement two feedback loops, one for the PA protection, the other for the PA regulation, in order to fulfill the requirements introduced in Chapter I.

The proposed architecture is implemented in 65nm CMOS process from STMicroelectronics in a circuit called PADet60G. This circuit implementation is discussed in this chapter before showing some open-loop simulation results. Measurement results on this circuit are then presented. Finally, this chapter discusses of the VSWR regulation concept and presents the algorithm which has to be integrated in the feedback decision block.

Chapter outline

IV.1. Regulation architecture

IV.1.1. State of the art

i. Overview

Although it is a major issue to protect power amplifiers from antenna impedance mismatch, very few of solution have been made. And this is more obvious yet that the frequency of the application is high. We have actually not found in the literature any protection loop for applications working at millimeter-wave frequencies. However some solutions have been developed for RF applications such as the cellular phones. We will hence present here some of those solutions, but we must keep in mind that the working frequencies are not in the same range as our targeted applications which means some solutions cannot be implemented while some others can be more easily integrated at mmW frequencies.

In 2005, Van Bezooijen from Philips Semiconductors has built a brief state-of-the-art in [1]. He has notably proposed a classification of the different regulation loops depending on the location of the action of the feedback loop. By generalizing this classification we can establish that the feedback loop can act either on the driver stages, or on the power stages of the PA, or finally on the impedance matching network. Those different classes can be combined to form a more powerful VSWR regulated transmitter. But actually such combinations have not been reported in the literature as it is sufficiently difficult to implement one or the other solution separately.

Figure IV-1 shows those three different possibilities. The location of the sensor in the RF chain as the way it is built (see Chapter II) does not really import here. This classification has been made as the different classes imply different concepts which are now going to be detailed.

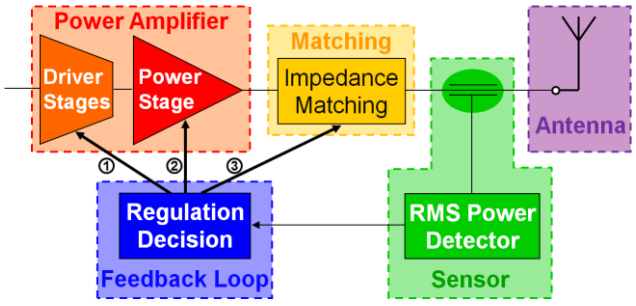


Figure IV-1 Classification of the feedback loops depending on the location the loop acts

ii. Regulation on the driver amplifier

The first category is the easiest one to implement. Acting on the driver stages consists in practice of limiting the signal strength at the input of the power stage. The PA input power being limited, so would be the output power too. And a much lower output power would cause much lower effect even with a high level of VSWR.

This regulation loop can be made in close cooperation with the baseband DSP. By the way, the user (the program of the user equipment) could know the transmission has been perturbed by antenna impedance mismatch and could react in function. However, its reaction possibilities are very low as it can only try to emit with a lower output power which means the receiver would not necessary be able to sense the signal, or it can also wait for a better antenna impedance condition which means the wireless link is broken for an undefined time.

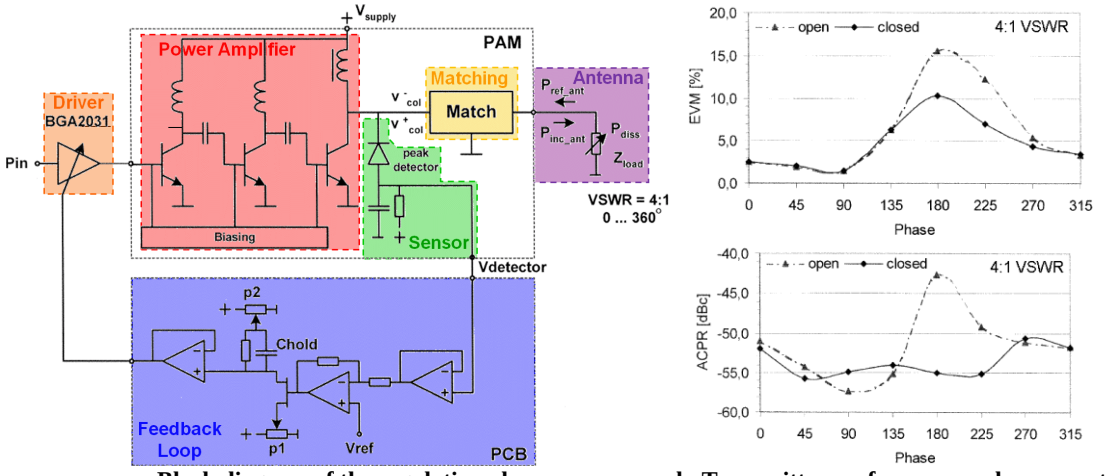
However Scuderi has demonstrated in [2] that this solution is very efficient as a protection loop. He has actually integrated a feedback loop that acts on a VGA upstream from the PA and its driver amplifier. This feedback loop is built on a very simple level comparator between the detected voltage at the power transistor collector and a tunable threshold voltage (the block diagram is very close to the one of Figure IV-2.a). The regulated system, designed in 0.8µm bipolar process (HSB3 from

STMicroelectronics) for 1.8GHz DCS-PCS applications, exhibits a good protection for up to 20:1 VSWR for all mismatch phases while the PA without protection is damaged by less than 8:1 VSWR.

Such protection loop has also been implemented by the same designer team from STMicroelectronics and the Università di Catania (Italia) with a more complex circuitry in 2005 [3]. However the measurement procedure was a little bit different. The load mismatch was actually settled to 10:1 VSWR (tested for all the phases) and the supply voltage was progressively increased. The PA with VSWR protection is not damage with a supply voltage up to 5.1V while the PA without VSWR protection was damaged with a supply voltage higher than 3.9V. The ruggedness of the PA was hence considerably improved.

Finally, in 2007, this PA protection technique has been implemented on a 0.25µm CMOS PA (BiCMOS process), still by the same designer team [4]. This time, the feedback loop uses also the gate voltage of the power transistor in addition to the drain voltage. PAs without protection cannot sustain a 10:1 VSWR when operating at 2V. In contrast, protected PAs revealed no failure after a VSWR test as severe as 20:1 (any phase angle) under the same supply voltage.

This solution is hence very efficient as a protection loop. But it can also be used to improve the PA linearity as reducing its output power (through its input power) would avoid PA saturation. Such PA linearity improvement technique has been implemented in 2004 by Van Bezooijen from Philips Semiconductors [5][1] for EDGE applications. Figure IV-2.a shows the block diagram of the implemented solution. When an overvoltage is detected on the collector of the power transistor, the gain of the driver is lowered. This hence avoids power stage saturation and improves the PA linearity. Figure IV-2.b shows the transmitter performance enhancement (EVM and ACPR) with respect to the phase of the impedance mismatch for 4:1 VSWR both in open loop and in closed loop. An EVM improvement of 5% and an ACPR improvement of 10dB have been obtained at 28.5dBm output power and 4:1 VSWR.



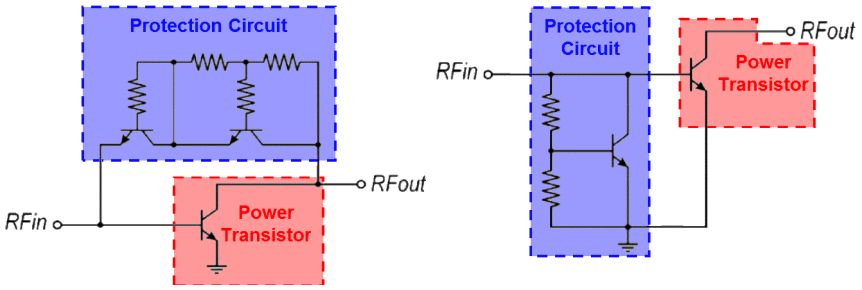
a. Block diagram of the regulatioon loop **b. Transmitter performance enhancement**

Figure IV-2 Regulation on the driver stage [5]

iii. Regulation on the power stage

When considering now a regulation loop acting on the power stage, the strategy is most of the time to modify the gain of the power amplifier, which is very similar to the previous regulation category. But when acting on the power stage, its output impedance will be modified. By reducing the biasing current flowing in the power transistor, the trans-conductance presented to the load is actually modified. Here again the impedance mismatch is not corrected, but contrarily to regulation loops on the driver stages, the impedance mismatch is modified.

Some very simple analog protection circuits have been reported in the literature [6][7]. The first one, illustrated in Figure IV-3.a, is based on collector voltage clamping [6]. By detecting an overvoltage on the power transistor collector, the biasing voltage on the power stage base is automatically reduced, thus avoiding the breakdown. The second protection loop, illustrated in Figure IV-3.b, is based on base voltage clamping [7]. An overvoltage detected on the base of the power transistor is directly corrected at the same location.



a. Collector voltage clamping [6] **b. Base voltage clamping [7]**

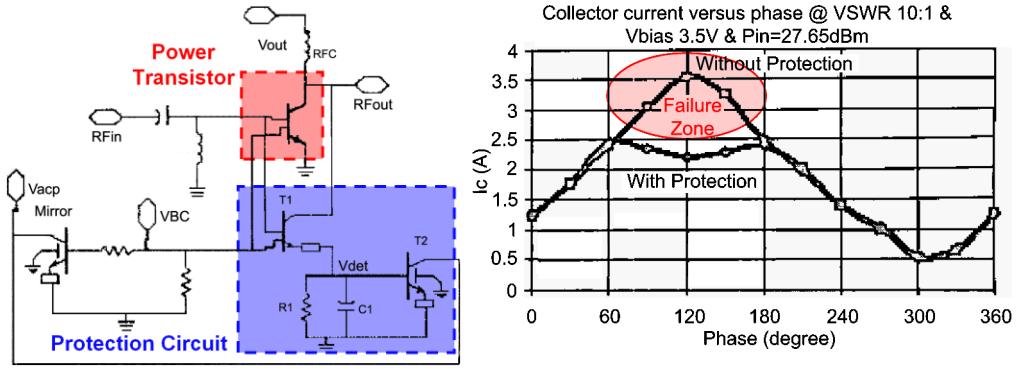
Figure IV-3 Two simple analog protection loops acting on the power stage

More recently, Zimmermann has presented in [8] a protection loop which is a little bit more complex. The detected voltage is actually compared to a voltage reference before the protection being activated and the gain of the PA being lowered. This protection loop has been implemented in a CMOS PA working at 1.9GHz for DECT applications. The PA topology is very close to our own PA topology (see section I.2.2.ii).

Such simple analog protection loop can also be implemented for HBT transistors where the breakdown generally comes from overcurrent rather than from overvoltage. Karoui from Freescale Semiconductors and LAAS-CNRS has hence proposed a protection loop against overcurrent flowing in HBT power transistors for GSM applications [9].

Figure IV-4.a shows the schematic of the implemented solution. The collector current that flows in the power transistor is sensed by the transistor T_1. This current is converted into a voltage V_{det} thanks to R_1 and low-pass filtered by C_1. When V_{det} exceeds the turn on voltage of the GaAs HBT T_2 (1.3V), the power stage biasing current is decreased (feedback on the current mirror of the PA biasing circuit) which means the gain of the amplifier is decreased.

Ruggedness tests have carried out under GSM conditions. The PA has been pushed into saturation. A 10:1 VSWR has been applied on the PA output while the phase has been progressively tuned over the entire 360°. The test has been repeated for supply voltage from 3.5V up to 5.5V. Without protection circuit the PA failed at supply voltages of 4.5V and 5.5V. With protection circuit, the collector current of the PA does not exceed 2.5A (the current threshold) and the PA revealed no damage with a supply voltage up to 5.5V for all load phase angles. Figure IV-4.b shows the collector current with respect to the load phase for a 3.5V supply voltage for both the initial PA and the protected PA.



a. Schematic of the regulatioon loop **b. PA performance enhancement**

Figure IV-4 Current regulation on the power stage [9]

Another solution to build a feedback loop that acts on the power stages is to control the supply voltage of the power transistor. This solution has been proposed and evaluated by simulations in [1] but has not been implemented to our knowledge. Figure IV-5 shows the block diagram of such feedback loop acting on the power amplifier supply voltage.

Two opposite strategies can be adopted depending if the PA should be protected from overvoltage or linearized to avoid saturation. Considering the first solution, when an overvoltage is detected on the collector of the power transistor, the supply voltage should be lowered to lower the voltage swing on the collector of the power transistor, thus avoiding PA breakdown.

In opposition, considering a linearization loop now, when the collector voltage reaches a given threshold close to the supply voltage, this means the PA will enter in its saturation regime. The supply voltage should hence be increased in order to increase the collector voltage swing range and thus to avoid waveform distortion. By the way, the power amplifier could exhibit better linearity performances but with an extra cost of efficiency. Moreover, the design difficulty is to build a good DC/DC converter which can exhibit very short time response.

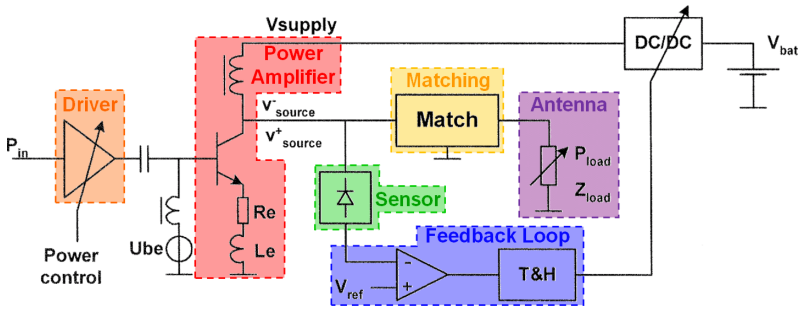
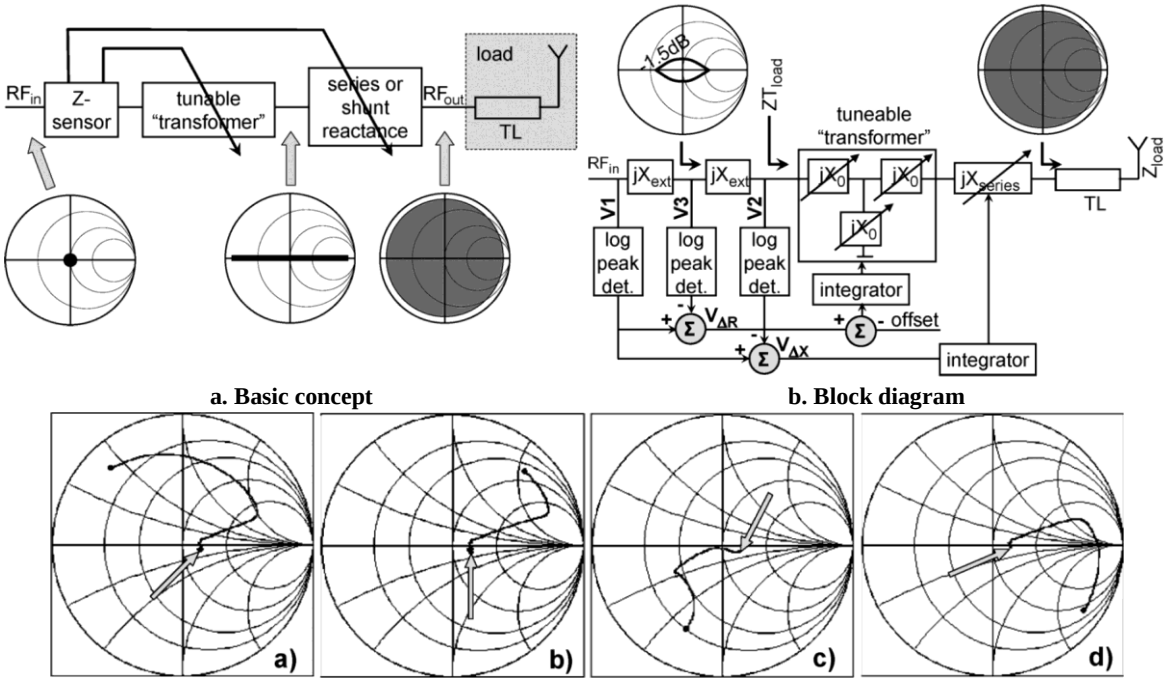


Figure IV-5 Block diagram of a regulation on the DC/DC converter of the power stage[1]

iv. Regulation on the matching network

The last category of VSWR regulation loop introduced in [1] aims to directly correct the impedance mismatch by acting on the matching network between the PA and the antenna. This technique should exhibits better results than the two previous ones as the power amplifier is always loaded by a constant load impedance. However regulating an impedance matching network is more complicated than simply tuning the gain of a driver amplifier. This technique has hence been explored only recently by university research teams only.



a. Basic concept **b. Block diagram**

c. Measurement results for 4 different initial load impedances (the arrow shows the impedance after regulation)

Figure IV-6 Regulation on the impedance matching network [10]

Firrao from the University of Twente has proposed such matching network regulation for GSM 900MHz applications [10]. The concept of the automatic antenna tuning system is shown in

Figure IV-6.a. Tuning is done in two steps: first the imaginary part of the load impedance is tuned to (almost) zero using a series (or shunt) reactance, then the resulting real part is transformed to the target real value (i.e. 50Ω) with a tunable "transformer". The tuning is performed automatically using the impedance sensor at the input of this matching network, where the impedance is always tuned to 50Ω.

This impedance sensor uses 3 detectors as, conceptually, three properties must be measured: the voltage magnitude, the current magnitude and the phase. In practice, the impedance can be determined thanks to two reactances and three peaks detectors to detect the (low frequency) amplitude of RF signals. The block diagram of this implementation is shown in Figure IV-6.b. The sensor system generates two outputs by comparing the 3 detectors output voltages: V_{DX} and V_{DR} indicate respectively the imaginary part and the real part of the tuned antenna impedance.

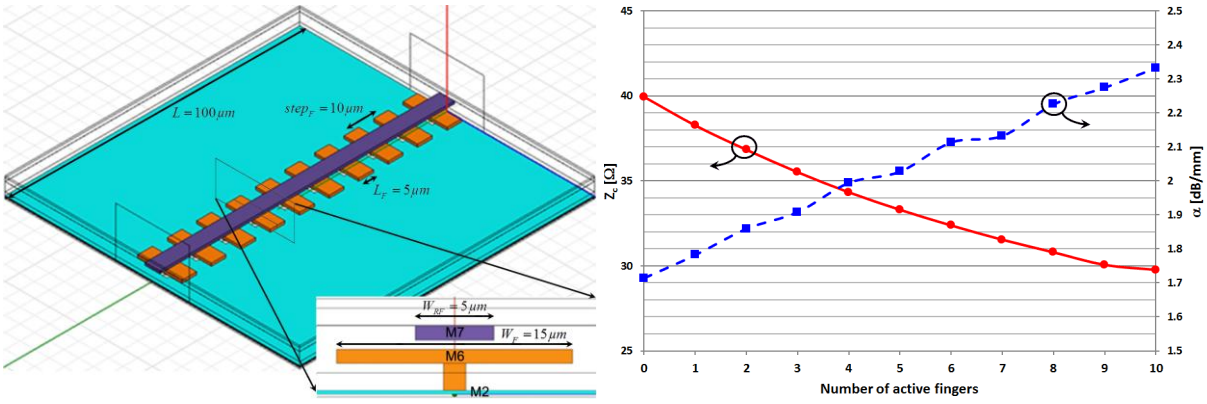
This automatic antenna tuning system has been implemented, but not integrated in a die yet. The sensor system has actually been implemented on PCB using SMD components and a Maury tuner was used to emulate the total impedance of the tunable matching network and antenna. The control algorithm that drives the Maury tuner has been implemented in a PC.

However this is a first step toward an integrated VSWR regulated PA. Moreover this implementation allows verifying the concept of regulation on the impedance matching network. And the system effectively corrects the load impedance by reaching about 50Ω whatever the initial impedance is as can be seen in Figure IV-6.c (the arrow shows the impedance after regulation).

IV.1.2. Proposed solutions

i. Difficulties of tuning a matching network

Directly correcting the antenna impedance inside the impedance matching network seems to be the best solution as no impedance mismatch would result between the PA and the antenna. To go further on this technique, we have evaluated the capability of tuning the impedance matching network for mmW applications. As the wavelength becomes smaller enough to be integrated on silicon, at millimeter-Wave frequencies the matching network are mostly implemented using transmission lines rather than lumped components. We have hence performed some electromagnetic simulations on a coplanar T-line – composed of a ribbon in the 7th metal layer and a ground plane in the 2nd metal layer (see section II.2.2.i for details on the 65nm CMOS technology) – under which some regularly spaced fingers – in the 6th metal layer – have been integrated. Figure IV-7.a shows a 3D view of the structure (from Ansoft HFSS [**11**]).



a. 3D view of the simulated structure **b. EM simulation results**

Figure IV-7 Impedance adaptation inside a µ-strip transmission line

The 10 fingers are progressively connected to the ground (the repartition of the active fingers is optimized) what increases the capacity between the ribbon and the ground. Figure IV-7.b shows the characteristic impedance and the propagation constant of the T-line with respect to the number of active fingers. The characteristic impedance can be tuned from 40Ω down to 30Ω. This is hence an interesting solution but the variation range of the impedance seems to be too low with respect to the 7:1 VSWR or even to the 3:1 VSWR that are targeted for the PA protection or regulation (see section I.4.3). This solution has hence not been chosen.

ii. Implemented solution

The solution that is proposed implements two regulation loops both acting on the power amplifier gain. The first one works as a protection loop. The PA is actually switched "on" or "off" depending on the power level that is detected as close as possible to the PA power transistor. If this power level exceeds a given threshold voltage, an overvoltage state – i.e. a critical situation – is declared and the PA has to be protected by a drastically decrease of its gain. The PA being turned "off", no (or very few) power is sent to the antenna and the impedance mismatch has hence no dangerous influence on the PA. This protection loop has to work fast enough to efficiently protect the PA against VSWR situations. Moreover, this protection loop should be able to protect the PA for an antenna impedance mismatch up to 7:1 VSWR as it has been specified in section I.4.3.

The second regulation loop is more complex. The aim of this regulation loop is to optimize the performances of the PA whatever the antenna impedance is. This loop has hence first to detect the antenna impedance. In practice, this can be implemented by using two power detectors as explained in section I.4.2.ii. The two power detector outputs have then to be analyzed and threated to determine the gain value that has to be applied on the PA to optimize its performances regarding the antenna impedance.

This function is complex to implement in the analog domain as it needs high computing capabilities. Moreover, performing this decision function in the analog domain cannot provide the same ease of reconfiguration that in the digital domain. It has hence been decided that this decision function should be implemented in the digital domain. This implies to implement both Analog-to-Digital Conversion (ADC) on the input signals (detector output voltages) and Digital-to-Analog Conversion (DAC) on the output signal (PA gain control). Following the system requirements introduced in section I.4.3, this regulation loop should be able to compensate up to 3:1 VSWR.

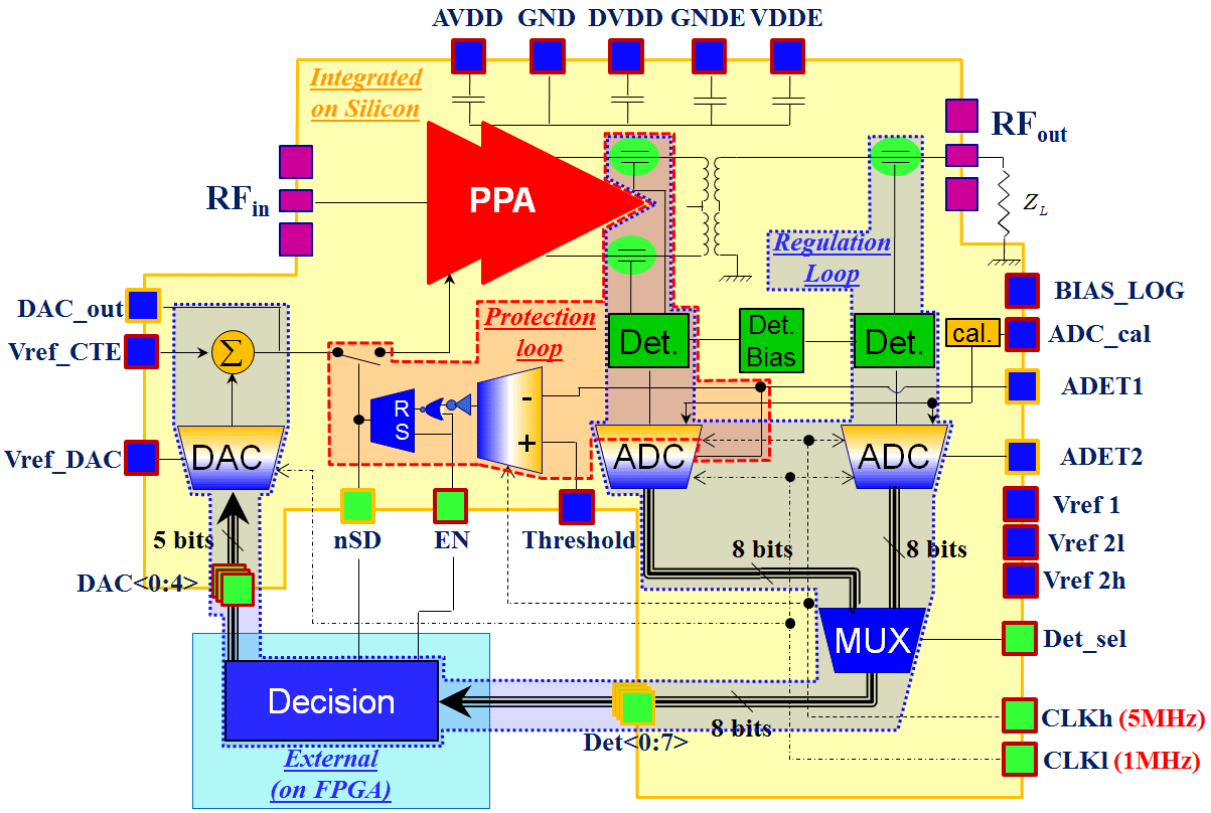


Figure IV-8 Block diagram of the implemented solution

Figure IV-8 shows the block diagram of the proposed solution, which integrates the two feedback loops previously introduced: the protection loop and the regulation loop. Additional information, which concerns the circuit implementation, is also reported on this figure and is explained in section IV.2.

IV.2. Circuit design and implementation for testability

The architecture proposed in the previous section seems to improve the reliability of the mmW power amplifier. But it is currently only theoretical concepts that are not proved yet. A circuit implementation is actually requested to demonstrate the functionality of the VSWR-regulation.

The circuit implementation, which is presented in this section, is based on the block diagram of Figure IV-8. As it can be seen on this figure, the protection loop is fully integrated in the circuit. But the digital decision block of the regulation loop is implemented externally to the circuit. It is actually more interesting to implement this decision block in a Field-Programmable Gate Array (FPGA) device rather than inside the circuit as the need is for a programmable device, which could test different decision schemes.

The use of already designed blocks has been preferred for design time consideration. The power amplifier, the power detectors and the logarithmic Analog-to-Digital Converter actually come from some previous works, which are detailed in the previous chapters of this thesis. Some further information is given hereafter.

However, several blocks, such as the power couplers and the Digital-to-Analog Converter, have to be modified and request some design efforts in order to be integrated in this demonstrator circuit. Those blocks are presented in section IV.2.2.

IV.2.1. Add-ons on already presented blocks

i. Power amplifier

The power amplifier used in this circuit implementation has been designed by Baudouin Martineau from STMicroelectronics. This is actually a pre-power amplifier (PPA) as it provides a high gain (16dB) but with a reduced output power (6.5dBm OCP1) at 60GHz, which is insufficient to respect the Wireless-HD specification. This PPA is actually presented in section I.2.2.ii. The schematic and the simulation results can be found in Figure I-11, Figure I-12 and Figure I-13.

Figure IV-9 shows the layout of this PPA, which has been initially provided by Baudouin Martineau. The two cascode stages can be easily identified as well as the three matching baluns (input, inter-stage and output matching networks). Input and output GSG mmW pads, designed for direct probing, are also integrated, which makes this PA ready for fabrication. The total layout, expecting the DC supply and biasing pads, is about 640x350µm².

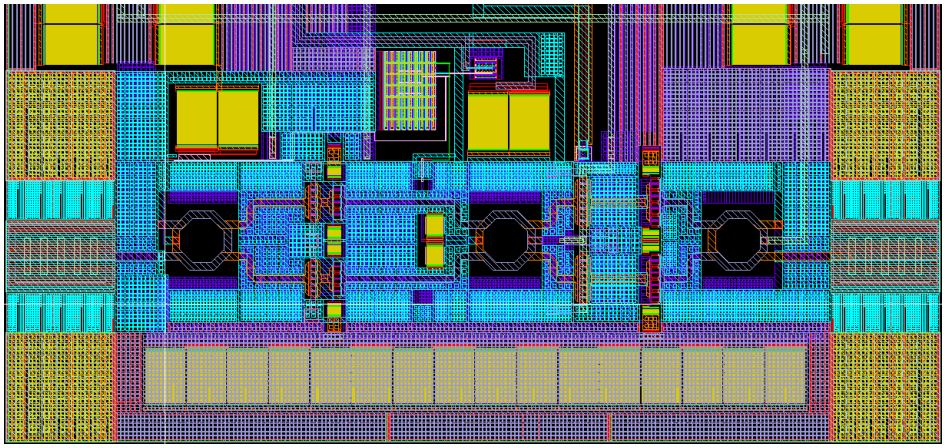


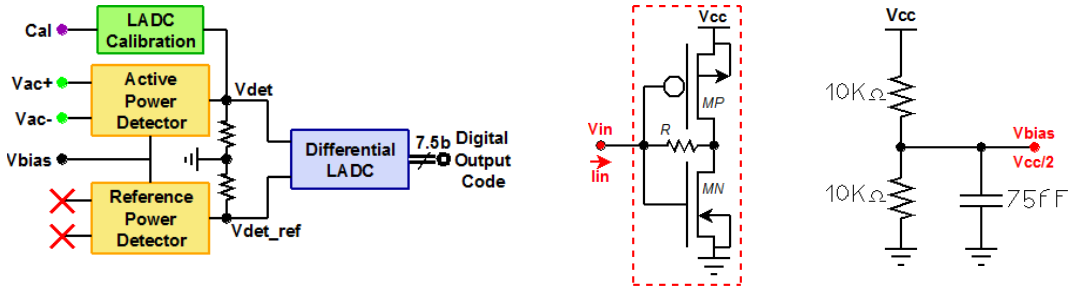
Figure IV-9 Layout of the initial PPA

The layout of this PPA, which has been proved to work fine thanks to a first fabrication and measurement procedure in the early 2010, has been kept unchanged. The following blocks, which need to be added for our peculiar application of VSWR-regulation, are hence integrated inside this layout with a minimum impact on it.

ii. Power detectors

The power detectors are coming from the first circuit implementation presented in Chapter II. This power detector has been proved to provide 25dB dynamic range at 60GHz and to be able to detect up to 3:1 VSWR, this value being limited by the measurement equipment. However some minor modifications are integrated in this second circuit implementation. The size of the current mirror MOS transistors is actually increased to 1x2µm² in order to increase the quality of the current copy. Standard V_t (svt) transistors are also replaced by low V_t (lvt) transistors in order to be fully compatible with the process options used by the PPA. This modification is presented in section II.2.1.iv to have very few influence on the power detector functioning.

The information laying in the variation of the output voltage rather than in the output voltage itself (see section II.2.1 and section II.4.2), the implementation configuration is modified to obtain the information as a differential voltage. A second identical power detector, which is not connected to any RF signal, is actually added to work as a reference. This reference detector gives the reference voltage level, which corresponds to the output voltage level of the active detector when no RF is applied on its inputs. This resulting differential architecture is illustrated in Figure IV-10.a. The differential architecture should also overcome the dependence to the process, voltage and thermal (PVT) variations.



a. Architecture with a reference detector **b. I-V converter schematic** **c. Bias voltage generation**

Figure IV-10 Architecture including two power detectors and adjacent circuits

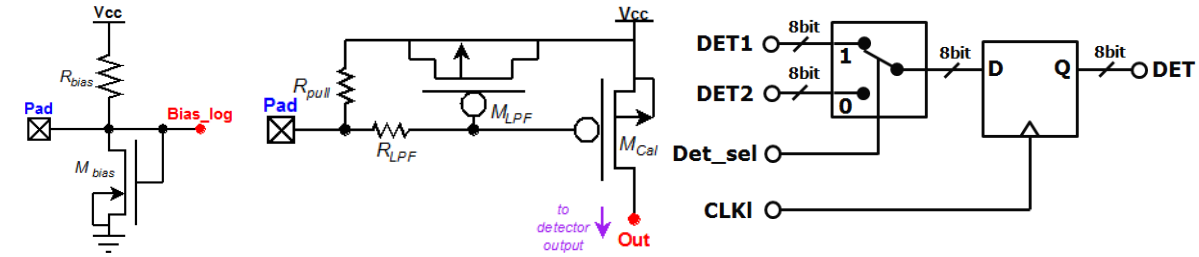
The first circuit implementation used a buffer to convert the power detector current output into a voltage that could be sensed by 50Ω measurement equipment (see section II.2.1.iii). This second circuit implementation does not need to ensure the compatibility to 50Ω equipment as the power detector output is directly digitized thanks to the differential LADC (Figure IV-10.a), which provides high-impedance inputs. The buffer is hence replaced by an active charge, shown in Figure IV-10.b, which converts the detector output current into a voltage. This active charge is actually composed of the 1st stage of the initial buffer. The MP transistor sizes 10x0.1µm² (in 10 fingers). The MN transistor sizes 3x0.1µm² (in 3 fingers). The resistance is tuned to be 10kΩ.

Finally, the bias voltage requested by the active and the reference power detectors is generated internally to the circuit thanks to the simple voltage divider schematic of Figure IV-10.c. The biasing voltage seems to have reduced influence while it stays close to half of the supply voltage as can be seen in Figure II-26 in section II.2.1.iv. It is actually not necessary to add a pad for this biasing voltage.

iii. Logarithmic Analog-to-Digital Converter

The two Analog-to-Digital Converters (ADC), which are mentioned on the block diagram of Figure IV-8, have to deal with the exponential behavior of the differential voltage coming from the power detectors. The power detector actually has a linear characteristic with respect to the power level expressed on a linear scale; but the regulation loop needs to control the power level at the PA output expressed on a logarithmic scale. As a consequence, a logarithmic behavior has to be integrated just before (or within) the ADC in order to compensate the exponential characteristic previously mentioned.

A novel architecture of Logarithmic Analog-to-Digital Converter (LADC) has been proposed, which is presented in Chapter III. The circuit implementation of this LADC is discussed in section III.3. However this LADC is integrated with three adjacent circuits presented hereafter.



a. Bias voltage generation **b. Calibration circuit** **c. Structure of the digital output multiplexer**

Figure IV-11 LADC adjacent circuits

First, the biasing voltage requested by the two LADCs is generated internally to the circuit thanks to the use of the small circuit of Figure IV-11.a. As can be seen on this figure, the biasing voltage *Bias_log* is generated thanks to the resistance R_{bias} (16kΩ) and the transistor M_{bias} (8 devices in parallel, each being 1x1µm² nlvtlp_rf). But *Bias_log* can also be imposed from the outside of the circuit thanks to the dedicated pad. The internal biasing circuit then does not have any effect on *Bias_log*.

Then, a calibration circuit, shown in Figure IV-11.b is integrated. As explained in section III.2.4, the LADC actually needs to be calibrated. Two conversion stages being integrated in the LADC, the resulting coarse and fine bits have to be correlated together in order to form a regular and monotonous output code. A calibration circuit is hence added in parallel to the active power detector on the positive input of the LADC, thus following the architecture of Figure IV-10.a. A PMOS M_{cal}, similar to the PMOS integrated on the output stage of the power detector (2 devices in parallel, 1x2µm² plvtlp_rf), is controlled thanks to a dedicated pad. The voltage applied on this dedicated pad is low-pass filtered by R_{LPF} (17.26kΩ) and M_{LPF} (4 parallel devices, 1x2µm² plvtlp_rf) and converted by M_{cal} into a current, which is added to the power detector output current. A 10kΩ pull-up resistance R_{pull} disables this calibration circuit when no voltage is applied on the dedicated pad.

Finally, a synchronous multiplexer, illustrated in Figure IV-11.c, is used in order to reduce the number of I/Os requested by the two LADCs, each generating an 8bit digital output. Using one extra I/O, Det_sel, the multiplexer reduces from 16 (8 for DET1 and 8 for DET2) to 9 (8 for DET and 1 for Det_sel) I/O pads to integrate in the circuit. However, this multiplexer also reduces the speed of the regulation loop. The two detected power levels (from the two active power detectors) are actually requested by the digital decision block before it can determine the appropriate gain to be applied on the PA in order to compensate the impedance mismatch.

IV.2.2. Adjacent circuits

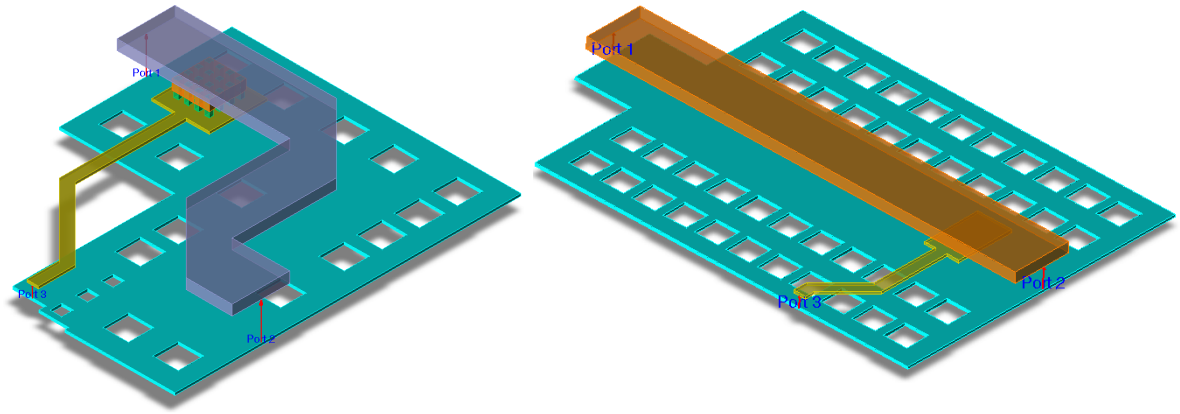
i. Power couplers

The capacitive coupler presented in section II.2.2 shows good measurement results (see section II.4.1). This capacitive coupler actually provides about 0.3 voltage attenuation coefficient while having negligible effect on the direct path (from the PA to the antenna).

However, this capacitive coupler is designed to be integrated inside a Grounded CoPlanar Waveguide (G-CPW) transmission line. The actual PPA (see section IV.2.1.i) uses microstrip (µ-strip) transmission lines. The structure of the power coupler needs hence to be adjusted to the new transmission line structure in order to be integrated in the PPA layout with minimal modification on the PPA output matching network.

As can be seen in Figure IV-8, there are 3 power couplers requested in this VSWR-regulated architecture, which, in practice, creates 2 power sensors. The first sensor is located as close as possible to the drains of the PPA power transistors in order to sense overvoltage and avoid PA breakdown. Integrated before the differential-to-single-ended balun, this sensor is composed of two symmetrical power couplers, referred hereafter as the first couplers, to work on a differential signal. The first coupler is studied hereafter in single-ended mode.

The second sensor is composed of only one power coupler, called second coupler, and is located as close as possible to the mmW GSG pad in order to directly sense the power sent to the antenna.



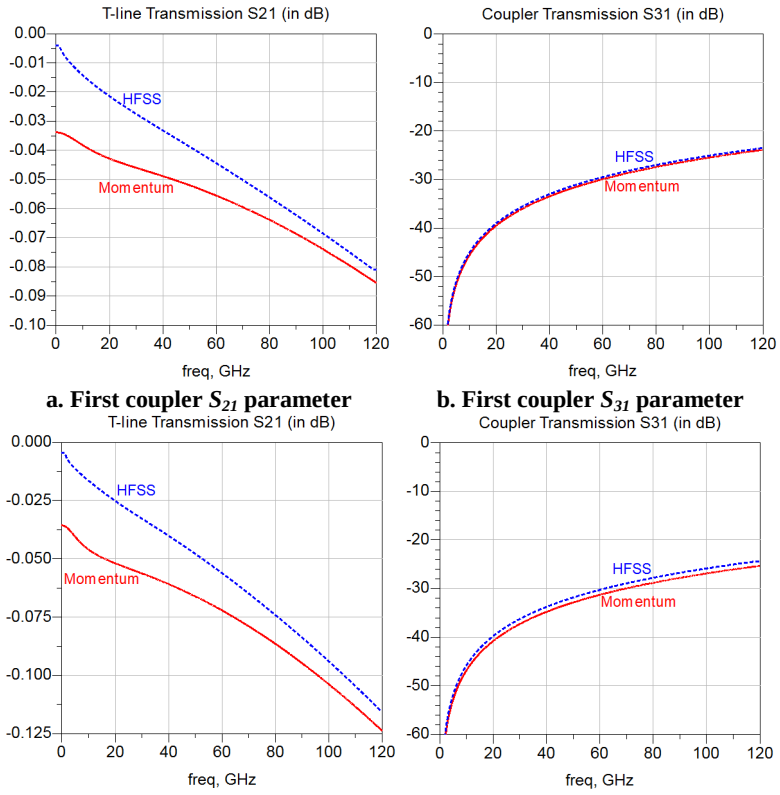
a. First power coupler **b. Second power coupler**

Figure IV-12 3D-view from Agilent Momentum [12] of the two power couplers

The first coupler is integrated inside a µ-strip T-line composed of a ribbon in the 7th metal layer and a ground plane in the 2nd metal layer. The metal element that probes the signal is a combination of a 5x5µm² rectangle in the 5th metal layer and of a 3x3µm² rectangle in the 6th metal layer.

The second coupler is integrated inside a µ-strip line composed of a ribbon in the 6th metal layer and a ground plane in the 2nd metal layer. A 5x3µm² rectangle in the 5th metal layer is integrated to form the two capacitors.

Those two couplers are perfectly integrated inside the transmission lines of the PPA output matching network. Figure IV-12 shows a 3D view from Agilent Momentum [**12**] of the two power couplers. The coupler output path in the 5th metal layer is simulated simultaneously to the rest of the structure for both power couplers as it increases the capacity with respect to the ground, and hence reduces the voltage attenuation coefficient.



a. First coupler S_{21} parameter **b. First coupler S_{31} parameter**

c. Second coupler S_{21} parameter **d. Second coupler S_{31} parameter**

Figure IV-13 Simulation results for the two new power coupler structures

Figure IV-13 a. and b. show respectively the S_{21} parameter (transmission on the direct path) and the S_{31} parameter (transmission through the coupler) for the first power coupler. These are electromagnetic simulation results obtained by HFSS from Ansoft [**11**] and by Momentum from Agilent Technologies [**12**]. Considering the reduced scale of the first diagram, one can conclude that the two EM simulators generate similar results. The very low level of S_{31} at 60GHz, about -30dB, means the power coupler has negligible impact on the direct path as a very reduced part of the incident power is sent to the coupled port. Moreover those S-parameters are obtained for a 50Ω load impedance on the coupled port, which is far from the reality where the power detector presents a high input impedance.

Similar curves, shown in Figure IV-13 c. and d., have been obtained for the second coupler. Here again, the two EM simulators provide perfectly fitted results. To conclude, both couplers present between 0.3 and 0.4 voltage attenuation coefficient and has been tuned not to saturate the power detectors even in case of severe antenna impedance mismatch with high output power involved.

ii. Digital-to-Analog Converter & PPA gain control

A Digital-to-Analog Converter (DAC) is used as the actuator of the regulation loop to tune the gain of the PA when an impedance mismatch occurs at the PA output. The designed DAC can generate 32 linearly spaced output levels thus resulting in a 5bit DAC.

Initially, the PPA designed by Baudouin Martineau already integrates a 5bit DAC to control the gain. This initial DAC is built on a very classical architecture where the different binary bits from B_0 up to B_4 directly control a series of different weighted transistors – through the number of devices mounted in parallel. The least significant bit (LSB) B_0 actually controls only one transistor while the next bit B_1 controls 2 transistors in parallel and so on up to the most significant bit (MSB) B_4 which controls 16 parallel transistors. This configuration is very efficient in terms of design and physical implementation.

However when changing from the command "01111" to the command "10000" as an example – which corresponds to a change of only one LSB – all the transistors are commuted simultaneously as the 15 "LSB transistors" (1 for B_0, 2 for B_1, 4 for B_2 and 8 for B_3) are turn 'off' while the 16 "MSB transistors" (16 for B_4) are turn 'on'. This creates high current peaks in the different branches and the DAC output current suffers from some glitches and some unexpected transitional values before reaching its stable final value. This is not necessary a problem when considering a system which should only be tunable very rarely. But this is a major drawback when considering a system which is permanently regulated as the targeted one of Figure IV-8.

The DAC presented hereafter resolves this limitation by activating each elementary transistor individually thanks to the use of an intermediate thermometer code. The input binary code from B_0 up to B_4 is actually converted into a thermometer code from T_0 up to T_{30} and each thermometer bit T_i is connected to only one transistor, or more exactly one branch of the current mirror. In this way, a variation of one LSB implies only one transistor (transistor branch) commutation which reduces drastically the amplitude of the glitches.

This modification apart, the structure of the current mirrors is very close to the one of the initial DAC. A degenerated cascoded current mirror has been implemented, which increases the quality of the current copy. Each current branch is actually composed of two MOS transistors in series with one 2kΩ resistor. The ratio of some current mirror needs to be adjusted in order to generate a LSB at about 1µA while keeping an input reference current in a reasonable range (high enough to minimize the impact of the noise, small enough not to increase too much the consumption of the circuit) at about 12µA. This is simply realized by changing the weight of the current branches.

Figure IV-14 shows the schematic of the designed 5bit DAC which includes 3 levels of current mirrors. The first one uses NMOS transistors with a 10/6 current ratio between the output I_0 and the input I_{in}. The second one uses PMOS transistors with a 1/4 ratio but generates 4 different equally weighted outputs from I_1 up to I_4. Each of those four currents is then copied in 8 identical branches, which can be activated thanks to individual switches. This last stage converts the digital thermometer code from T_0 up to T_{30} into a certain number of active current that are finally summed to form the

output current of the DAC I_{out}. This 3rd current mirror uses NMOS transistors with 1/5 current ratio. Some capacitors have also been integrated in this last current mirror to protect the reference voltages of the transistor commutation which also reduces the emergence of glitches.

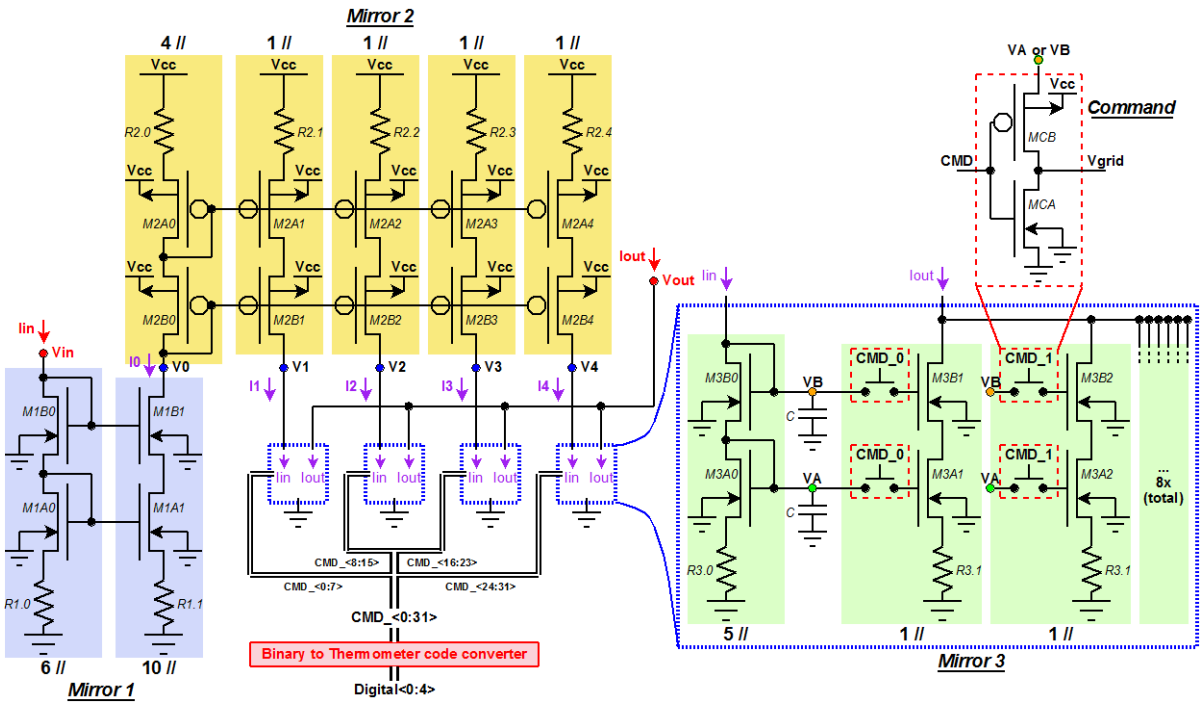


Figure IV-14 Schematic of the 5bits DAC

The different size and values of the transistors and resistors used in this DAC are summarized in Table IV-1.

	Mirror 1		Mirror 2		Mirror 3		Command
	M1A0 M1B0 R1.0	M1A1 M1B1 R1.1	M2A0 M2B0 R2.0	M2A (1:4) M2B (1:4) R2. (1:4)	M3A0 M3B0 R3.0	M3A (1:8) M3B (1:8) R3. (1:8)	MCA MCB
Nb of // dev.	6	10	4	1	5	1	1
W	2µm	2µm	2µm	2µm	1µm	1µm	5µm
L	2µm	2µm	2µm	2µm	1µm	1µm	0.1µm
R	2kΩ	2kΩ	2kΩ	2kΩ	2kΩ	2kΩ	

Table IV-1 Size of the transistors and resistors used in the 5bit DAC

Figure IV-15 shows the layout of this 5bit DAC which occupies only 60x93µm².

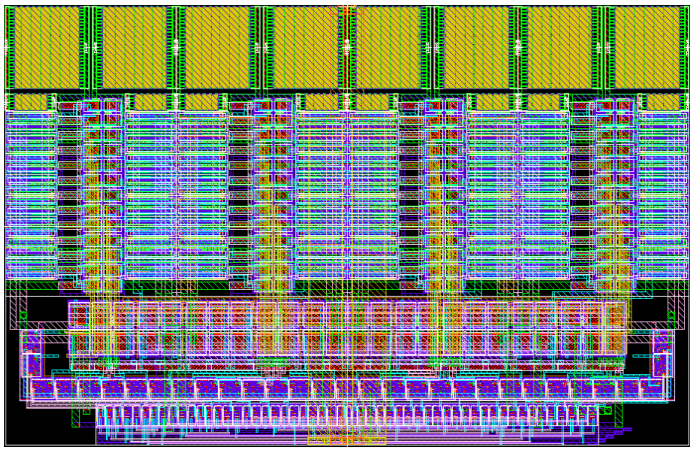
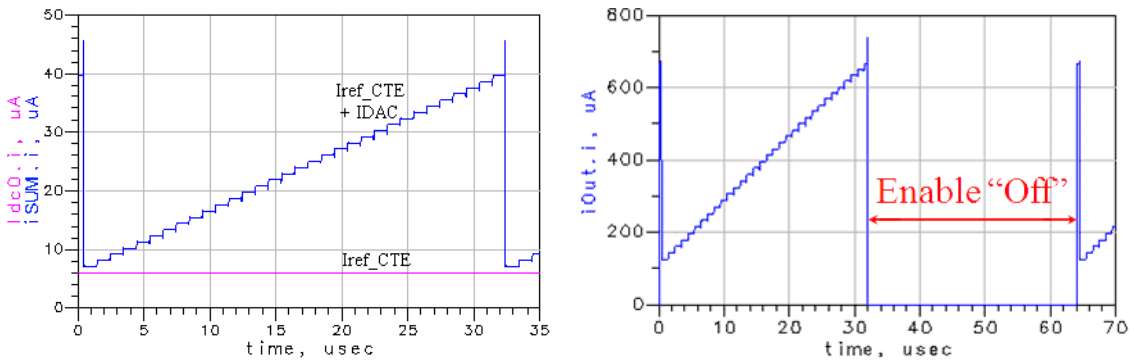


Figure IV-15 Layout of the 5bits DAC

In addition to this DAC, an analog control of the gain of the PPA is implemented following the architecture of Figure IV-8. This analog input, called V_{ref_CTE}, allows the addition of a certain level of biasing current to the DAC output in order to adjust the range of variation of the gain control. This also makes an additional tunable parameter, which can be used as a backup solution to overcome a dysfunction of the DAC. The resulting current, which is the addition of the DAC and the constant (CTE) components is shown in Figure IV-16.a. This current is amplified by a factor 19 thanks to another current mirror, which creates the biasing currents of the two PPA stages, as can be seen in Figure IV-16.b. This current mirror integrates a switch, which is controlled by the protection loop, which can be used to turn "off" the PPA.



a. DAC output current summed to the analog Iref_CTE **b. PPA biasing current**

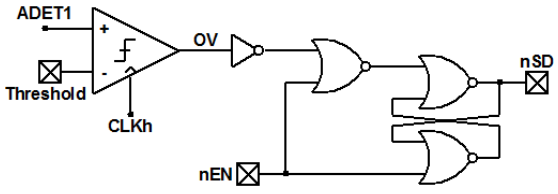
Figure IV-16 Transient simulation results of the PPA gain control

iii. Protection loop implementation

The PPA gain control, presented above, can be deactivated by the protection loop. In practice, the detector output is compared to a threshold voltage (eternally tunable). This indicates if an overvoltage situation (OV) is detected. A simple digital circuit, based on an R-S latch, then determines if the PPA should be shuttled down (signal nSD). Figure IV-17.a shows the schematic of this protection loop.

When an overvoltage situation is detected (OV='1') and the protection loop is activated (nEN='0'), the protection loop shuts down the PPA (nSD='0'). The PPA stays shuttled down while the protection loop is not re-armed by an external decision (nEN='1'). The decision to shut down the PPA can be deactivated thanks to the enable signal nEN (nEN='1'). The functioning of the protection loop is summarized in the truth table of Figure IV-17.b.

The initial comparison, which should detect an overvoltage situation, uses the signal ADET1 coming from the analog output of the logarithmic amplifier (integrated in the LADC). This signal is not critical and can be loaded by the clocked comparator, contrarily to the signal coming from the power coupler (signal V_{ac}) and to the signal coming from the detector (signal V_{det}). However, the protection loop effectively uses the power level detected as close as possible to the drain of the power transistors integrated in the PPA, to determine if the power amplifier is in a critical overvoltage situation.



nEN	OV	nSD	Comment
0	0	nSD	Memory state
0	1	0	Shut down due to overvoltage
1	0	1	No overvoltage detection
1	1	1	/ PPA forced to be active

a. Schematic **b. Truth table**

Figure IV-17 Protection loop decision circuit

IV.2.3. Full circuit physical implementation

All the blocks presented above are integrated in a unique circuit called PADet60G following the block diagram of Figure IV-8. The die photograph of the circuit PADet60G is shown in Figure IV-18 where the different pads are also defined. As can be seen on the left part of the circuit, the layout of the PPA has been kept unchanged to minimize the impact on the PPA characteristics.

The circuit is pad-limited and occupies 640x2300µm² while the active part only occupies 640x400µm², the additional space being used to integrate some decoupling capacitors.

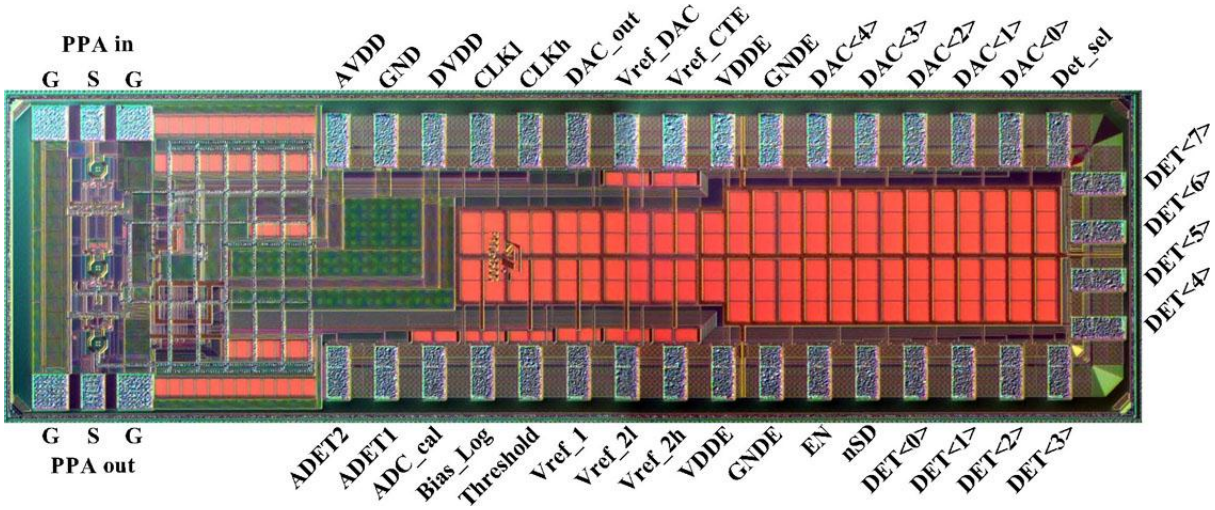


Figure IV-18 Die photograph of the circuit PADet60G

The circuit integrates too many IOs that have to be probed simultaneously during the measurement phase. Only the mmW pads are actually being probed. All the DC and low-frequency IOs are going to be wirebonded on a PCB board (see section IV.4.1.i). To facilitate the wirebonding process, the 36 concerned IOs are integrated in a pad ring using standard cells from the IO library of the STMicroelectronics 65nm CMOS technology. All those IOs hence integrate an ESD protection circuit. The digital IOs also integrate some buffer and some pull-up or pull-down options. Table IV-2 gives the definition of the different IOs with the typical value to be applied on.

Name	I/O	A/D	Pull	Function	Typ	Unit
DC Supplies						
AVDD	I	A	-	Analog supply voltage	1.2	[V]
DVDD	I	A	-	Digital supply voltage	1.2	[V]
GND	I	A	-	General Ground	0	[V]
VDDE	I	A	-	I/O supply voltage	1.2	[V]
GNDE	I	A	-	I/O ground (internally connected to GND)	0	[V]
PPA Dedicated						
RFin	I	mmW	-	mmW PPA input (GSG for probing)	60	[GHz]
RFout	O	mmW	-	mmW PPA output (GSG for probing)		
Log. ADC Dedicated						
BIAS_LOG	I	A	-	Voltage biasing for the Logarithmic Amplifier	0.42	[V]
Vref1	I	A	-	Reference voltage for coarse flash ADC	0.8	[V]
Vref2l	I	A	-	Negative reference voltage for fine flash ADC	0.764	[V]
Vref2h	I	A	-	Positive reference voltage for fine flash ADC	1.005	[V]
CLKh	I	D	Down	High frequency clock for ADC	5	[MHz]
CLKl	I	D	Down	Low frequency clock for ADC	1	[MHz]
ADC_cal	I	A	-	LADC calibration input		
Det_sel	I	D	Down	Selection bit for Det1 or Det2		
ADET1	O	A	-	Analog output detector 1		
ADET2	O	A	-	Analog output detector 2		
Det<0:7>	O	D	-	Digital output detector		
DAC & Protection Loop Dedicated						
Vref_DAC	I	A	-	Reference for DAC	0.83	[V]
Vref_CTE	I	A	-	Reference for current control	0.6	[V]
DAC_out	O	A	-	Output voltage for DAC in-situ test		[V]
DAC<0:4>	I	D	Up	Digital input for DAC	1	[MHz]
Threshold	I	A	-	Threshold voltage for the protection loop	1.15	[V]
EN	I	D	Up	Enable/Reset for the protection loop		
nSD	O	D	-	non Shut Down for the protection loop		

Table IV-2 IO definition for the circuit PADet60G

IV.3. Analog open-loop simulations

IV.3.1. Simulation configuration

The circuit PADet60G integrates simultaneously RF/mmW elements, data converters and a digital decision block. The simulation of those elements together cannot be performed in a simple simulation. RF/mmW elements actually need to be simulated in the frequency domain (60GHz signals would induce a very fine time step with respect to the digital phenomenon at about 1MHz, which means a very large number of computing points). Data converters actually need to be simulated in the time domain. This means that to simulate the complete system, one has to build a co-simulation with mmW elements simulated using the envelope simulator, data converters using the transient simulator, and the digital decision block using a behavioral simulator. Such co-simulation can currently be implemented using Agilent Technologies software (see Chapter V). However the integrated regulation loop highly complicate the co-simulation and it is very difficult to obtain valid results.

Nevertheless, some open-loop simulations have been carried on in order to verify that the system could properly work. The simulation configuration, shown in Figure IV-19, only integrates the mmW and analog blocks of the complete circuit, which are the PPA, the power couplers and power detectors, and the logarithmic amplifiers integrated inside the two LADCs. Then Harmonic Balanced (HB) simulations with 1 tone at 60GHz can be performed using Agilent RFDE tools [**13**].

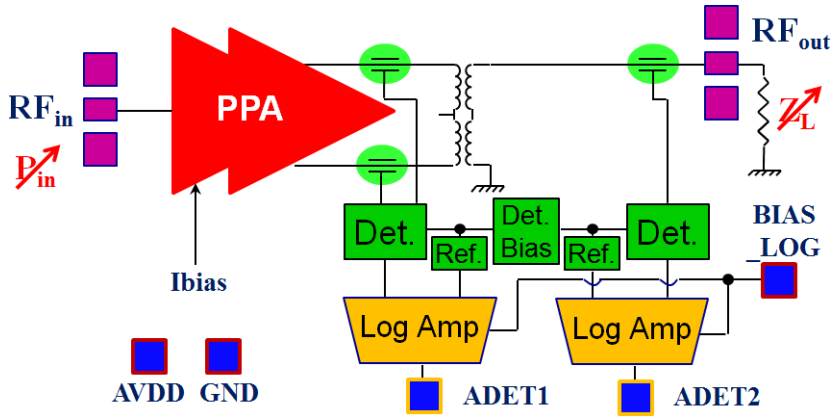


Figure IV-19 Analog open-loop simulation configuration

Two different procedures are used. First, a power sweep is applied on the PPA input in order to characterize the PPA with the power detectors. Then, the PPA load-impedance Z_L is tuned to progressively cover the full Smith chart resulting in a load-pull simulation. This last configuration is equivalent to an antenna impedance mismatch at the PPA output. According to the theoretical simulations in section I.4.2.ii, the power detectors should sense this impedance mismatch.

IV.3.2. Power sweep simulations

A power sweep in applied on the 60GHz sinewave signal at the input of the PPA. Figure IV-20.a shows the simulation results of the variation of the output voltage for the two power detectors (the differential input of the logarithmic amplifier). The curves are linear up to a certain power level, around -5dBm of P_{in}, where saturation can be observed. This saturation can also be observed on the output power curve (scale on the right axis), meaning the power detector is still linear with respect to its input, which is the power flowing in the transmission-line at the PPA output.

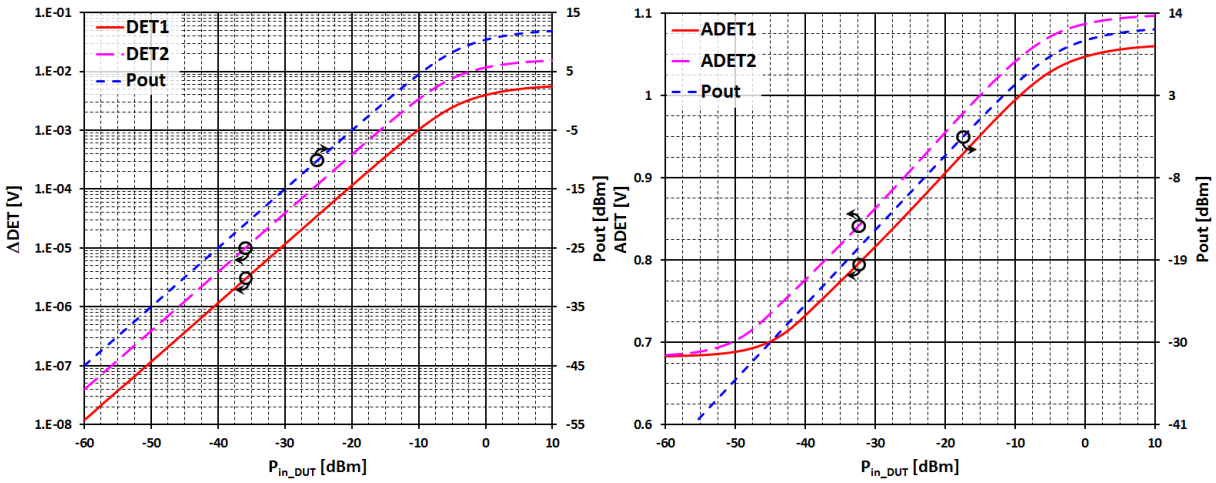
Figure IV-20.b shows the signals ADET1 and ADET2 (see Figure IV-19), the analog outputs of the logarithmic amplifier at the output of the two power detectors. Similarly to the detector output voltage variation, the two logarithmic amplifier outputs are also linear on a large dynamic range from less than -45dBm up to -5dBm of P_{in}.

One can observe that this linear regime stands for a linear scale on the vertical axis with respect to the input power expressed in dB. This is not the case when considering the detector output voltage variation (see Figure IV-20.a). The logarithmic amplifier effectively converts its differential input voltage DET1 and DET_ref1 into the signal ADET1 through a logarithmic characteristic.

The saturation regime observed on both ADET1 and ADET2 curves corresponds to the saturation of the PPA output power P_{out} (expressed in [dBm] on the right axis). This means that the logarithmic amplifier is still linear up to the saturation of the output power.

Finally the almost constant offset between ADET1 and ADET2 can be explained considering the following arguments. The first detector being differential, its characteristic should be increased by a factor 2 (3dB with respect to Pin) with respect to the single-ended second detector. But the second detector being located after the differential to single-ended converter balun, the voltage to be detected is twice – the balun losses apart – the voltage detected by each differential input of the first detector. The two effects should cancel each other out.

The only difference remaining is the voltage attenuation ratio of the two couplers. The first coupler actually presents a 0.19 voltage attenuation ratio while the second coupler presents a 0.37 voltage attenuation ratio. There is hence a 2 factor between the characteristics of the two couplers. This results in a 3dB offset (with respect to P_{in}) between the two detector outputs DET1 and DET2 (Figure IV-20.a) and between the two logarithmic amplifier outputs ADET1 and ADET2 (Figure IV-20.b).



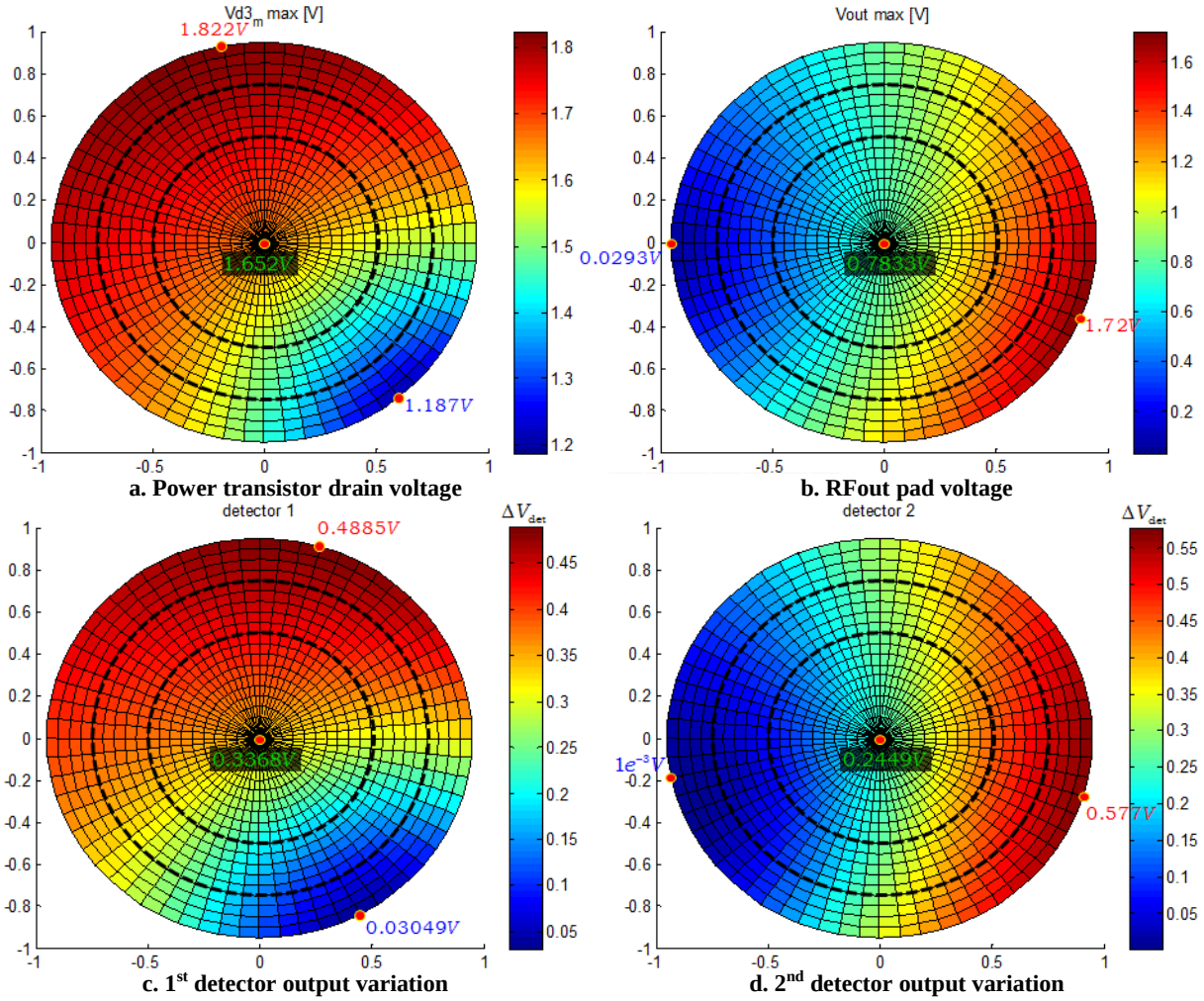
a. Detector output voltage variation **b. Logarithmic amplifier outputs**

Figure IV-20 Simulation results, detector output variation versus input power sweep

IV.3.3. Load-pull simulations

Load-pull simulations are then performed. A harmonic balance simulation (1 tone at 60GHz) is hence computed for each value of the PPA load impedance. The amplitude of the reflection coefficient |Γ| ranges from 0 up to 19/20 (equivalent to 39:1 VSWR) with 20 steps; and the phase of the reflection coefficient arg(Γ) ranges from 0 up to 2π with 64 steps. The simulation results are then computed using Matlab to generate the diagrams of Figure IV-21, which are equivalent to Smith charts (the Smith chart is a |Γ| / arg(Γ) representation), the usual Smith chart curves being removed for readability. The 3:1 and 7:1 VSWR contours are reported on each diagram and correspond to the two black dashed circles. The minimum, the maximum, as well as the 50Ω values are also reported on each diagram.

Note: Those simulation results correspond to an early version of the PPA, where the first capacitive coupler exhibits a 0.3 voltage attenuation ratio and the second capacitive coupler exhibits a 0.2 voltage attenuation ratio. More precisely, the µ-strip lines are not implemented in the same metal layers that in the circuit implementation; but their lengths and shapes have been kept unchanged. As a consequence, the diagrams presented hereafter are more qualitative rather than quantitative.



a. Power transistor drain voltage **b. RFout pad voltage**

c. 1st detector output variation **d. 2nd detector output variation**

Figure IV-21 Load-pull simulation results

The first observation is that the two detectors (diagrams c. and d.) effectively sense the antenna impedance mismatch. The distance between the two detectors is almost $\lambda/8$ – the length of the balun is difficult to evaluate. This explains the difference with respect to the theoretical simulations presented in section I.4.2. One can hence observe an almost $\pi/2$ rotation between the diagrams of the two detectors, which is more interesting for the regulation algorithm (see section IV.5).

The diagrams a. and b. show respectively the voltage level at the power transistor drain and at the RF_{out} pad, where the load impedance is tuned. Those power transistor drain voltage reaches the critical level of 1.8V for certain values of the load impedance. This is where the protection loop should be useful. The information given by the first detector (diagram c.) well fits the information requested by the protection loop (diagram a.). This means the protection loop can be implemented simply by integrating a comparator between the 1st detector output voltage and a given threshold.

Note finally that there is a small phase offset between the diagrams c. and a. and between the diagrams d. and b. This phase offset results from the real location of the capacitive couplers with respect to the power transistor drain and to the RF_{out} pad. The first coupler is actually located 15µm far from the power transistor drain and the second coupler is actually located 10µm far from the RF_{out} pad.

IV.4. Measurement results

IV.4.1. Measurement configuration and procedure

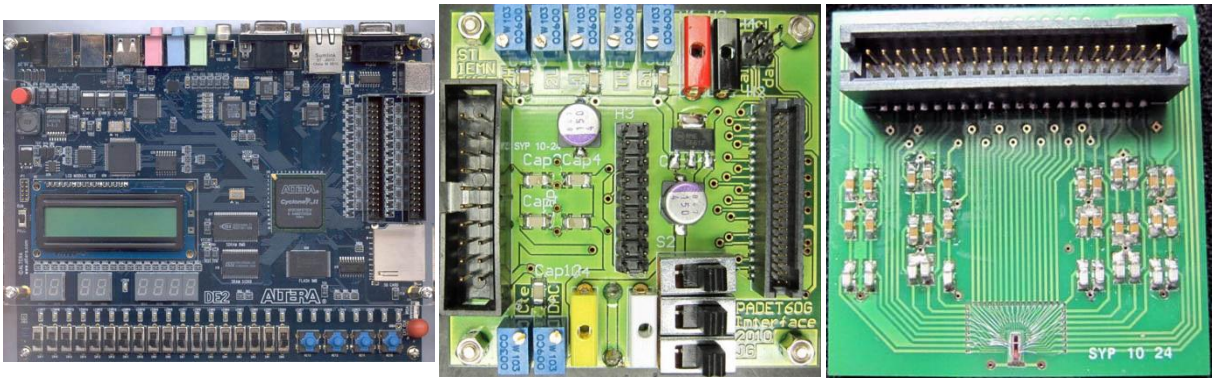
i. Test boards

Integrating too many I/Os to be directly probed (see Table IV-2), the circuit PADet60G is reported and wire-bonded on the Chip Board, shown in Figure IV-22.c. This 34x34mm² PCB board has been designed to be compliant to the requirements of the probing station in IMS laboratory (3D size and totally flat bottom face to be sucked on the chuck of the probing station). The PPA input and output pads are hence kept accessible and can easily be driven through the mmW GSG probes. The board integrates a complete decoupling strategy for the different supply and reference voltages, thus using 3 capacitors of different values (100nF, 4.7nF and 10pF) for each voltage.

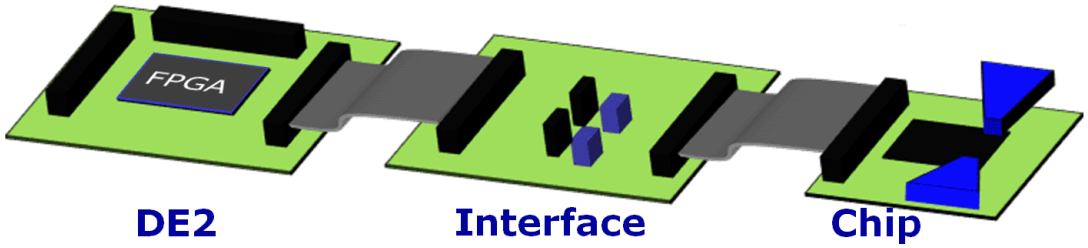
This Chip Board is connected to the Interface Board, shown in Figure IV-22.b, through a 1meter long 40 connectors ribbon cable from Samtec (2 rows of 20 positions; cable reference: SFSD-20-30-G-40.00-D-NUS; board connector reference: TFM-120-12-L-D) following the assembly of Figure IV-22.d. The Interface Board generates the different supply and reference voltages requested by the circuit PADet60G. This drastically reduces the need for laboratory equipment as only one 2.8V supply is requested to generate AVDD, DVDD, VDDE, Vref1, Vref2l, Vref2h, BIAS_LOG, Threshold, Vref_CTE, and Vref_DAC (see Figure IV-8 and Table IV-2 for IO definitions).

The Interface Board also integrates some buffer (ref: SN74AVC20T245) on the digital signals to convert the 3.3V LVCMOS logic used by the FPGA into the 1.2V LVCMOS logic used by the DUT circuit.

This Interface Board is hence connected to the Altera DE2 board, shown in Figure IV-22.a, through a 1meter 20 connectors ribbon cable (standard ribbon cable with 0.05inch pitch and usual header connectors) following the assembly of Figure IV-22.d. This Altera DE2 board integrates a Cyclone II FPGA, which is used to implement the digital decision block of Figure IV-8.



a. Altera DE2 board **b. Interface board** **c. Chip board**



d. Test boards assembly

Figure IV-22 Test boards

The test boards assembly presented above is used in two different measurement environments, which are presented hereafter, depending of the element to be characterized.

ii. Equipment in STMicroelectronics environment

First, both characterizations of the DAC (section IV.4.2) and of the LADC (section IV.4.3) are performed in STMicroelectronics environment. Those characterizations do not require any probe station as the inputs and outputs of the DAC and LADC are available through the Interface Board. Only DC and low-frequency signals are involved in those measurements.

Table IV-3 lists the laboratory equipment that is used in this environment. Only one external supply voltage source (at 2.8V) is used as the requested supply voltages are then generated on the interface board (see section IV.4.1.i) to appropriately supply the circuit.

A precision supply voltage source, the Keithley 2602A, is used to characterize the LADC. As a logarithmic function is integrated in this ADC, the dynamic range of its analog input actually ranges from 1µV up to 1V (6 decades). In addition to this DC characterization, a voltage ramp is also applied at the input of the LADC. This ramp is generated by the Agilent 33250A waveform generator.

The DAC block needs a digital ramp on its input to generate the corresponding analog voltage. This digital ramp can be generated either by the FPGA (see section IV.4.1.i) or by a data generator, the Tektronix DG2020A with the appropriate P3420 pods.

Finally, all the measurements are obtained with the Tektronix MSO 4104 oscilloscope. This oscilloscope has 4 analog inputs and 16 digital inputs working hence as a kind of logic analyzer. This function is very useful to characterize data converters as both input and output characteristics can be obtained and displayed synchronously.

Function	Equipment reference
DC power supply	Toellner TOE 8732
Precision DC power supply	Keithley 2602A
Waveform generator	Agilent 33250A
Data generator	Tektronix DG2020A with 2 P3420 pods
Oscilloscope	Tektronix MSO 4104

Table IV-3 Measurement equipment in STMicroelectronics environment

iii. Equipment in IMS environment

In a second time, the circuit PADet60G has to be characterized with the appropriate mmW signals. The Chip Board is then loaded on the probing station and two mmW GSG probes from Cascade are connected to the input and the output of the PPA integrated in the circuit PADet60G. This enables the characterization of the circuit in terms of power sweep (section IV.4.4) and in terms of load-pull measurements (section IV.4.5). This is referred hereafter as the IMS environment.

Table IV-4 lists the laboratory equipment that is used in this environment. The Sinusoidal Signal Generator, the input power amplifier, the coupler, the isolator, the source and load-pull tuners, the variable attenuator and the power meters with their power sensors are all part of the load-pull bed designed by Focus for the IMS laboratory [**14**], which is already presented in section II.4.3 for the load-pull characterization of the circuit PowDet60G. The DC power supply and the multimeter are optional equipment of this measurement bed.

Function	Equipment reference
Sinusoidal Signal Generator	Agilent PNA E8361A
Input power amplifier	SP6010-30-20W
Coupler	CL3-12-R1000
Isolator	FBI-12-RSES0
Source and load-pull tuners	Focus iCCMT-75500
Variable attenuator	LSA-12-5000
Power meter + Power sensor	HP EPM-441A & EPM-437A + Agilent V8486A
DC power supply	HP E3631A
Multimeter	HP 34401A

Table IV-4 Mesurement equipment in IMS environment

Figure IV-23 shows the synoptic of the IMS environment. As previously explained, the mmW input and output ports of the PPA are both probed and connected to source and load impedance tuners. The analog supply and reference voltages are generated by the Interface Board from an external 2.8V power supply. In the different measurements performed using the IMS environment (sections IV.4.4 and IV.4.5), the supply voltages AVDD and VDDE are settled to 1.4V (maximum voltage allowed by the IO pads) in order to increase the gain and the output power of the PPA. The digital signals (both up and down links) are treated by the FPGA DE2 board following the test board assembly introduced in section IV.4.1.i.

Finally, the 2 analog outputs ADET1 and ADET2 are probed on the Interface Board and measured by 2 voltmeters (multimeters). Those 2 multimeters, as well as the 60GHz signal generator, the 2 power meters and the source and load tuners are connected together through GPIB (General Purpose Interface Bus) and controlled by Focus software on a computer. The GPIB connections are not reported in Figure IV-23. This test bed can performed either power sweep measurements or source or load-pull measurements.

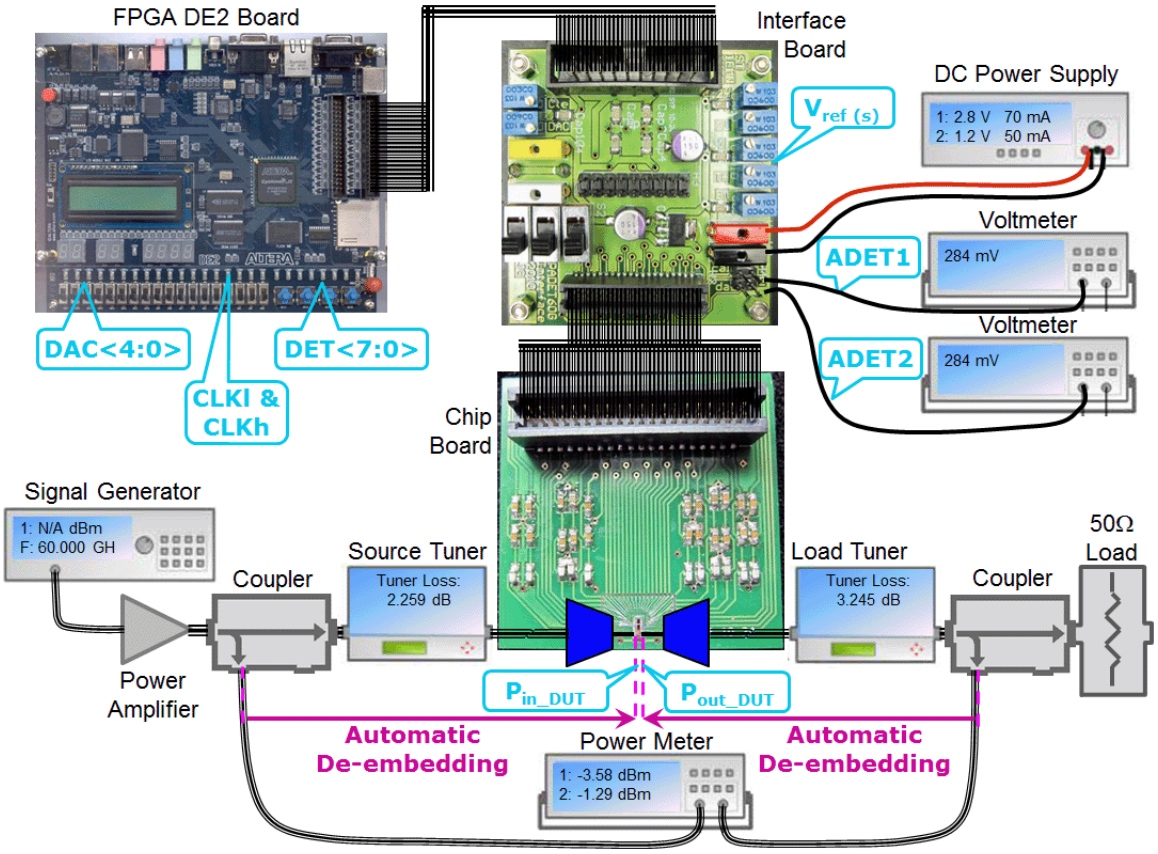


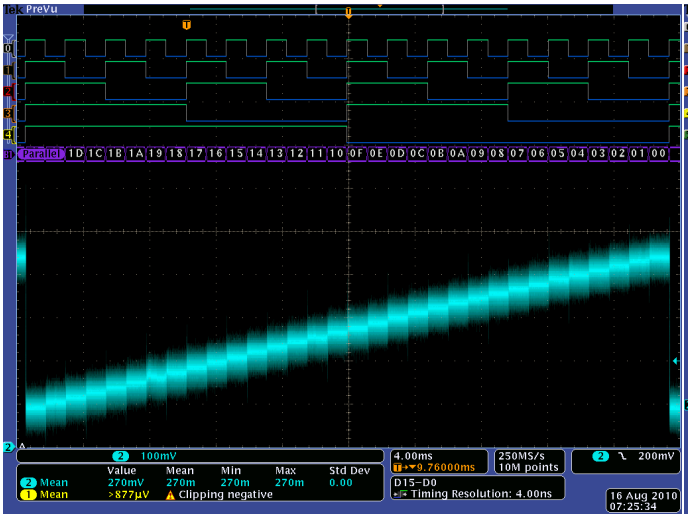
Figure IV-23 Synoptic of the IMS environment

IV.4.2. DAC measurements

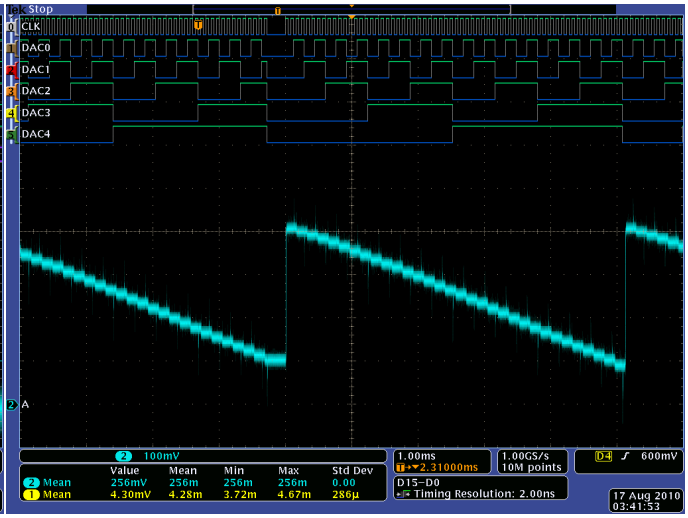
i. Digital control of the analog DAC output

The Digital-to-Analog Converter block is characterized in two different ways, both using the STMicroelectronics environment. First, a digital ramp is generated by the FPGA on the DE2 board. The FPGA also generates the clock signal CLKl at a frequency around 0.84MHz (27MHz on-board quartz frequency divided by 2^5). The data changing frequency is around 0.824kHz (27MHz divided by 2^15). Figure IV-24.a shows the measurement results obtained with this test setup. The digital signals generated by the FPGA are displayed on the top of the diagram with the combination of the 5 bits into hexadecimal data. The DAC analog output voltage is plotted on the bottom of the diagram.

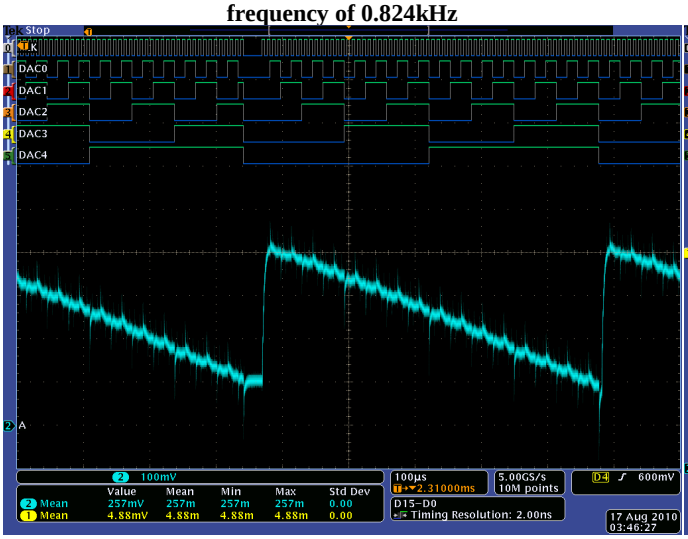
Despite a high level of noise on the analog output voltage, the DAC seems to work fine and provides 32 stairs corresponding to the 5bit digital ramp at the input of the circuit. A second setup is then settled up in order to obtain better results with a lower level of noise.



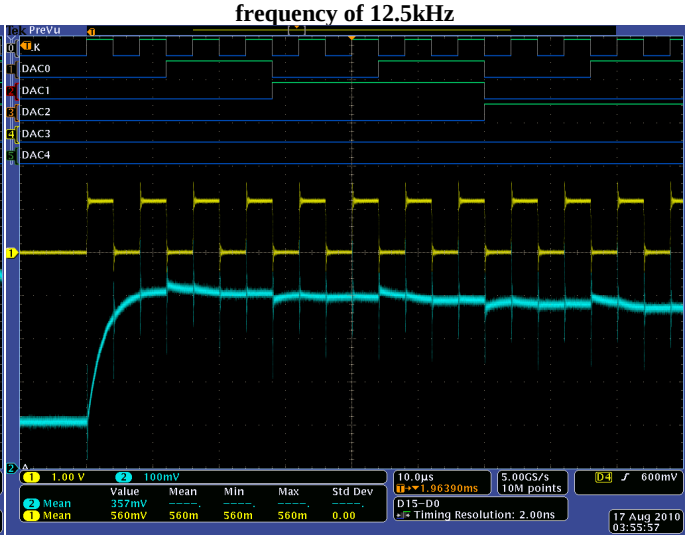
a. Digital ramp generated by the FPGA board with a Data frequency of 0.824kHz



b. Digital ramp generated by the data generator with a Clock frequency of 12.5kHz



c. Digital ramp generated by the data generator with a Clock frequency of 125kHz



d. Digital ramp generated by the data generator with a Clock frequency of 125kHz – Clock & ADC output signals

Figure IV-24 DAC measurement results

In a second time, the FPGA is replaced by the digital data generator. This equipment generates a counter on 7bits. The LSB of this counter is used as the clock signal (CLKl on PADet60G) while the 5 MSBs are used as the DAC input data. In this way, the data changing frequency is 4 times lower than the clock frequency. Two clock frequencies are tested: 12.5kHz (which corresponds to a 3.125kHz data changing frequency), and 125kHz (31.25kHz data changing frequency).

Figure IV-24 .b and c. shows the measurement results respectively for the 12.5kHz and 125kHz digital ramps. The Digital inputs with the clock are displayed on the top of the diagram while the analog output voltage still lies on the bottom. Figure IV-24.d corresponds to a zoom on the beginning of the 125Khz digital ramp. The additional yellow curve in the middle of the diagram corresponds to the clock signal probed in the analog domain.

Working with the laboratory equipment generates a lower noise level on the analog DAC output voltage as can be seen by comparing Figure IV-24.a and Figure IV-24.b. This could be explained partially by the bad ground connection between the FPGA and the circuit. The buffer integrated on the Interface Board could also generate some noise on the different supply voltages. This buffer being not supplied when the FPGA board is disconnected, the use of the laboratory equipment could actually generate a lower noise level. Finally the measure itself could perturb the DAC output.

One solution to enhance the characterization of this DAC is to replace the laboratory DC supplies by battery supplies, which is often less dependent from external disturbances. However a digital ramp would still be required on the DAC input, which would still be generated by mains supplied equipment. Moreover the analog output signal would also still be measured by the oscilloscope, which is mains supplied. This test has hence not been implemented

Concerning now the working frequency, 125kHz clock frequency and 31.25kHz data changing frequency seems to be the maximum working frequency for the DAC (see Figure IV-24.c and Figure IV-24.d). Note that the clock frequency is not the limiting parameter. A 824kHz clock frequency is actually applied when working with the FPGA (Figure IV-24.a). The data changing frequency is hence the main limiting parameter. This 31.25kHz limitation is much lower than the 1MHz observed during the simulations. This could be explained by the many parasitic capacitances added by the measurement configuration (test boards and test equipment). Those parasitic capacitances are actually not in the same range that the capacitors integrated in the circuit and could explain this high difference in terms of working frequency.

ii. Analog control of the analog DAC output

As can be seen in Figure IV-8, the PPA gain control – signal named $DAC_{\_out}$ – can also be controlled by the analog input V_{ref_CTE}. Figure IV-25 shows the characteristic of this analog function. The measured data have been obtained by storing the average of the $DAC_{\_out}$ signal (function Mean on the oscilloscope) for an input voltage V_{ref_CTE} ranging from 0 up to 1.2V. The simulated curve is also reported in Figure IV-25. Despite a high offset between the simulated and measured results characteristics which results from different digital codes applied on the DAC input (DAC "off" in measurements and "on" in simulations), the shape of the two curves is identical meaning this analog control is fully operational. The PA gain could hence be controlled through this analog input in addition to the DAC.

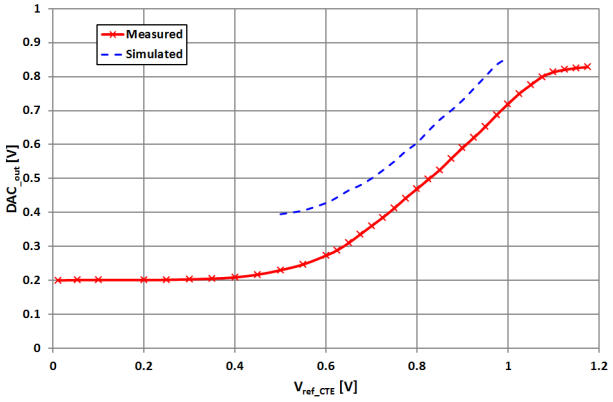


Figure IV-25 Analog control of the DAC output

The Digital-to-Analog-Converter is hence fully operational and shows measurement results very close to simulation results over all the 32 digitally controlled stairs. The analog way for controlling the PA gain has also successfully been tested.

IV.4.3. LADC measurements

Still using the STMicroelectronics environment, the Logarithmic Analog-to-Digital Converter (LADC) is characterized. The main issue here is that the inputs of the LADC, which are the detector and reference detector output voltages (see Figure IV-10.a), are not directly accessible from the outside of the circuit (otherwise the additional pads would have highly degrade those signals). As explained in section IV.2.1.iii, a calibration input has been implemented. This ADC_cal input is used in the following measurements and two different ways are used to control it.

First, a DC voltage, coming from a precision DC power supply, the Keithley 2602A, is applied on ADC_cal. Each time a valid digital code (stable value) is observed on the LADC output, the voltage level applied on ADC_cal is stored in a table. This table is then plotted, which gives the red curve, referred as "Keithley", in Figure IV-27. The same curve is reported on both graphs a. and b. to work as a reference.

Considering the high level of noise, already evocated in the previous measurements, the LADC generates a very few number of valid codes, 20 in practice, very far from the theoretical 180 (2^7.5) different codes. More precisely, valid codes are obtained for higher than 10mV steps of ADC_cal while the LADC requires some 1µV precision to be fully characterized.

In a second time, the Keithley DC power supply is replaced by a waveform generator, the Agilent 33250A. A voltage ramp – from 0V up to 1V at a frequency of 1Hz - is applied on ADC_cal. The oscilloscope is used to measure simultaneously the analog input signal ADC_cal (CH3), the analog output signal ADET2 (CH2) and the 8bit digital output DET (digital signals 15 down to 8). The FPGA generates the two clock signals CLKh (at 6.25MHz) and CLKl (at 1MHz), as well as the selector DET_sel between the two LADC outputs. CLKh, CLKl and DET_sel are also displayed on the oscilloscope (digital signal 0, 1 and 7 respectively).

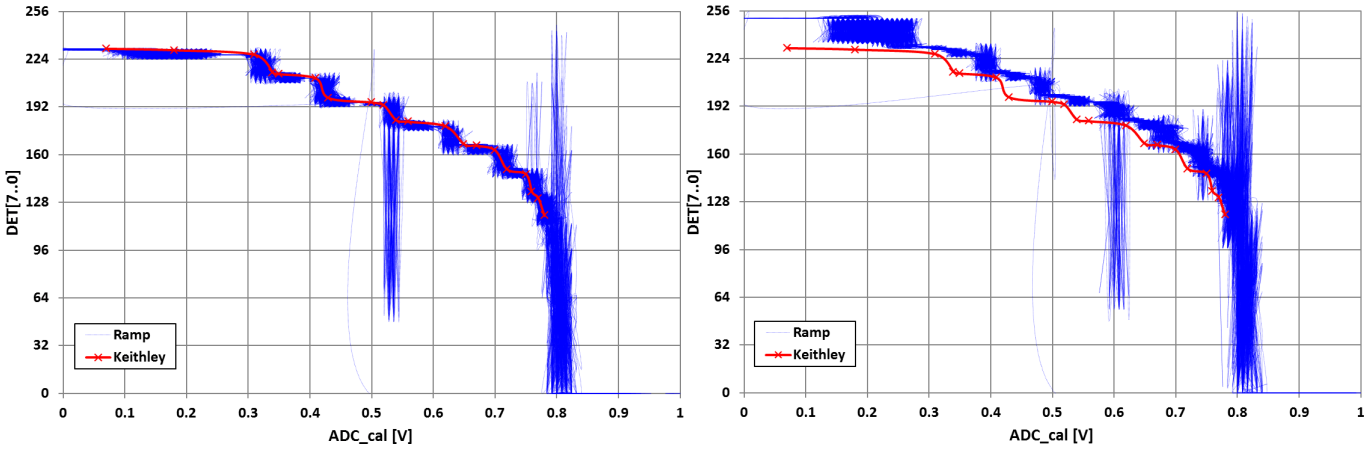
a. First set of reference voltages **b. Second set of reference voltages**

Figure IV-26 LADC measurement results, oscilloscope snapshots

Figure IV-26.a presents a snapshot of the oscilloscope screen where all the previously introduced signals are displayed. This measure has been obtained for a first set of reference voltages (V_{ref1}, V_{ref2l} and V_{ref2h}) and presents some wide regions where the variation of the analog input voltage does not correspond to any variation of the digital output signals. A second set of reference voltages, corresponding to the simulated configuration which is given in Table IV-2, is also tested and gives the measurement results of Figure IV-26.b.

The two sets of reference voltages provide both interesting results as the digital output code seems to be logarithmically dependent on the time, which means logarithmically dependent on the analog input voltage ADC_cal. However, a high level of noise is still present both on the analog voltages and on the digital signals.

The data presented on the two oscilloscope snapshots of Figure IV-26 are exported and computed using Excel. The digital 8 bits from DET7 down to DET0 can be seen as a single code ranging from 0 up to 255 (=2^8-1) and displayed as a function of the analog input voltage ADC_cal. Figure IV-27.a and Figure IV-27.b show those two curves, referred as "ramp" (dotted blue curves), simultaneously with the characteristic observed in the first experiment with the Keithley supply and the first set of reference voltages (plain red curve).



a. First set of reference voltages for both curves

b. Second set of reference voltages for the curve "ramp" and First set of reference voltages for the curve "Keithley"

Figure IV-27 LADC measurement results, graphical views

The first observation that can be made is that the curves obtained with the first measurement configuration (red curve) and with the second measurement configuration (dotted blue curve) fit very well together (Figure IV-27.a). The 2nd configuration simply integrates a higher noise level than the 1st configuration as all the transient states are considered here.

A second observation is that the 2nd set of reference voltages (Figure IV-27.a) generates some digital codes that are not obtained in the 1st set (Figure IV-27.a). This is notably the case of the codes values between 230 and 250. This conforms to the simulations: the desired conversion range can be obtained by adjusting properly the different reference voltages, such as in a classical ADC.

Finally, it can be noticed that all those curves clearly shows the logarithmic characteristic of the LADC. This proves qualitatively the functionality of this innovating Logarithmic-ADC solution. However the noise limitation is too important to be able to quantify the characteristic of the LADC at low input levels.

Those measurements results have been obtained only for one of the two integrated LADCs. The analog output of the second LADC actually seems to be pushed to the supply voltage.

IV.4.4. Power sweep measurements

The following measurements are performed using the IMS environment. The supply voltage of the analog part of the circuit (AVDD and VDDE) is increased to 1.4V. This voltage level cannot be further increased as the pads integrate overvoltage protection (clamping diodes), which limits the supply voltage to about 1.4V. Two different chips are tested, each being wirebonded on a Chip Board.

i. PPA output power and gain measurement results

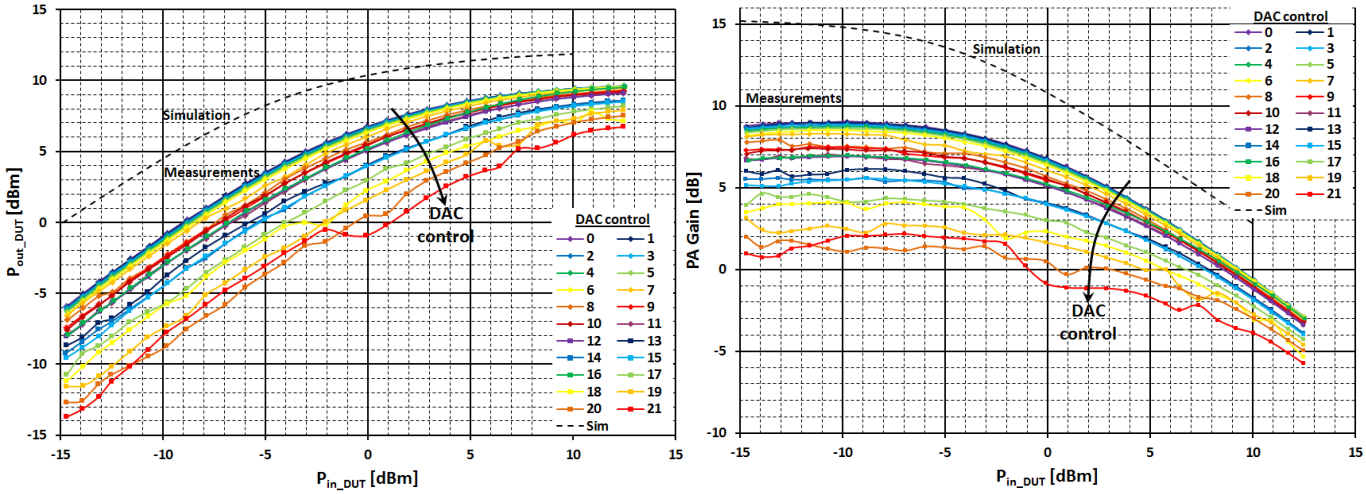
The first power sweep measurements aim to verify the good working of the PPA. The output power P_{out_DUT} and the gain *Gain* are hence measured for a power sweep on the PPA input. The gain being controlled by the digital code at the input of the DAC, different codes are tested from 0 (the highest gain, see section IV.4.2.i) to 31 (the lowest gain). Note that the high values of the digital code are sometimes not tested as the corresponding gain would be too low, which results in some difficulties to obtain power levels in the range of the power meters (see Figure IV-23).

Figure IV-28 shows the measurement results obtained for the first chip. The diagram a. corresponds to the PPA output power, the diagram b. to the power gain. The simulation results (under 1.2V supply) are reported on those diagrams (dashed lines).

For the lowest DAC code, the 1st chip exhibits 9.6dBm saturation output power P_{sat}, 5dBm output power at the 1dB compression point *OCP1*, and 9.05dB power gain. Those values have to be compared with the 11.9dBm P_{sat}, 6.5dBm *OCP1* and 15.36dB power gain obtained in simulation (under 1.2V supply voltage). Previous measurements performed by Baudouin Martineau shows 13dBm P_{sat}, 8dBm *OCP1* and 15dB power gain at 60GHz under 1.8V supply voltage (in this implementation, the DC pads are not limited by clamping circuit).

Concerning the power gain, the measurement result is much lower than the simulation result. However the 9.05dB measured here under 1.4V is coherent to the 15dB measured under 1.8V, especially considering the cascode topology of the PPA. A high supply voltage is actually required to ensure a sufficient drain-source voltage swing on both cascoded transistors. The same reason explains the difference in terms of P_{sat} and *OCP1*. Those PPA measurement results are hence coherent to the previous measurements performed by Baudouin Martineau under 1.8V supply voltage.

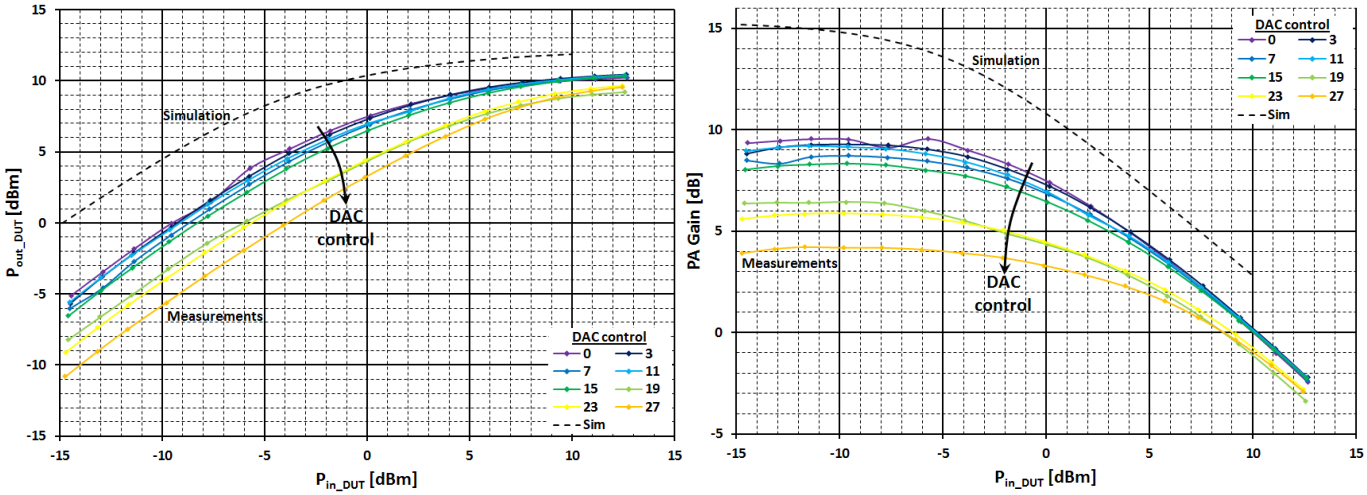
Those measurements also show that the DAC input code effectively controls the gain of the PPA. The PPA gain can actually be lower down from 9dB down to 1dB simply by increasing the DAC code from 0 up to 20.



a. PPA output power **b. PPA gain**

Figure IV-28 Measurements at 60GHz on the 1st chip – P_{out} and Gain for different DAC control codes

Similar results are obtained with the 2nd chip as can be seen in Figure IV-29. This 2nd chip exhibits 10.44dBm P_{sat}, 5.6dBm *OCP1* and 9.5dB power gain. Here again the DAC code effectively controls the PPA gain.



a. PPA output power **b. PPA gain**

Figure IV-29 Measurements at 60GHz on the 2nd chip – P_{out} and Gain for different DAC control codes

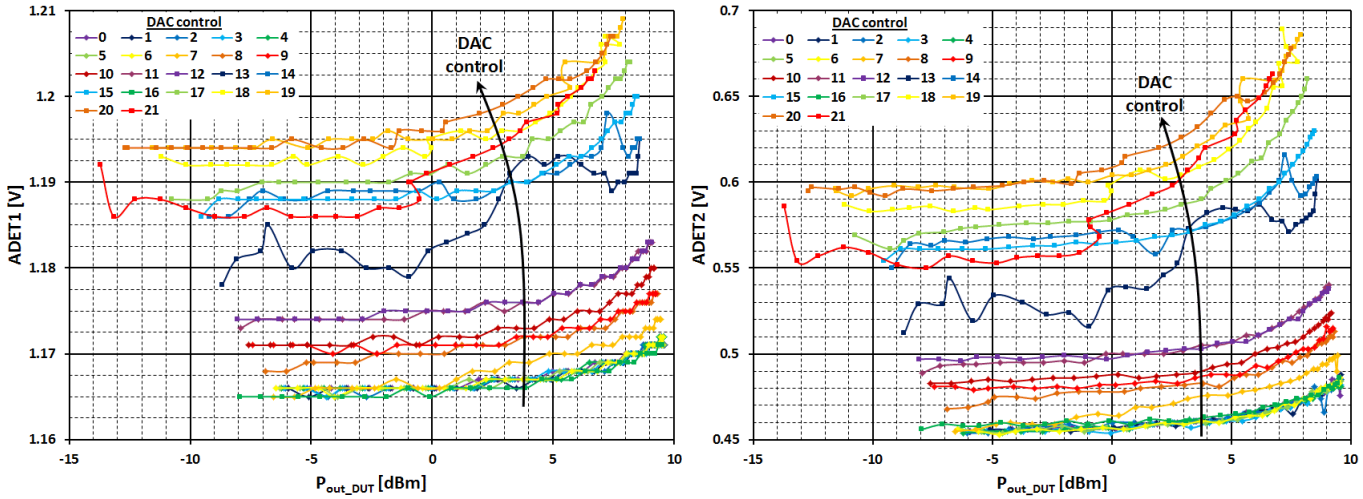
ii. Detectors analog output voltage measurement results

The analog output voltages coming from the two detectors (LADC analog output), the signals ADET1 and ADET2, can then be measured and plotted with respect to P_{out_DUT}. Considering the signals ADET1 and ADET2 with respect to the PPA output power gives the characteristic of the power detectors with the logarithmic amplifier (referred as PCLA hereafter, which stands for Progressive Compression Logarithmic Amplifier) regardless of the PPA characteristic.

Figure IV-30 and Figure IV-31 show those two signals (ADET1 on the diagram a. and ADET2 on the diagram b.) respectively for the 1st and the 2nd chips. Considering the 1st chip, ADET1 and ADET2 are monotonously dependent on the DAC code. This is not so clear on the 2nd chip. In practice, the different measurements of the 1st chip are all performed with the same laying of the 2 mmW probes. Several probe laying are involved for the 2nd chip measurements, the DAC codes 0, 3 and 7 being performed with a first laying, the codes 11, 15 and 19 with a second laying, and the codes 23 and 27 with a third laying. One can observe that each time the probes are laid down on the circuit, the signals ADET1 and ADET2 are lowered down (see Figure IV-31).

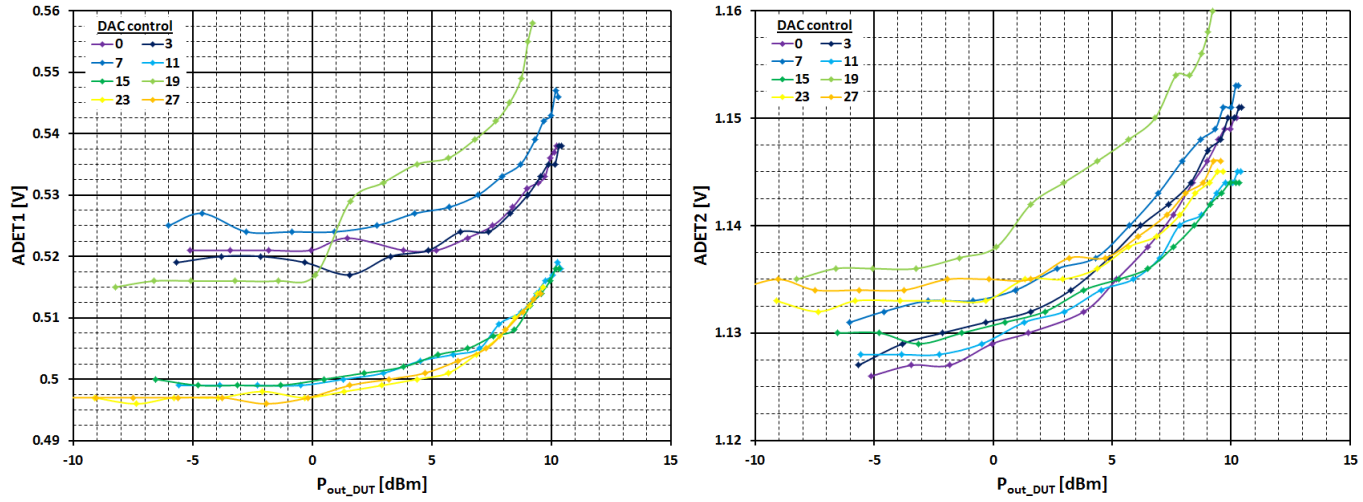
To be more precise on this issue, the connection between the GSG probes and the circuit pads is difficult to be kept with sufficient quality. The probes being directly connected to the tuners through solid waveguides, every little mechanical oscillation on the impedance tuner or some other measurement equipment is actually directly passed on the extremity of the probes, which progressively degrades the quality of the contact. This effect cannot be detected easily during the measurement as long as one parameter vary.

The consequence here is that the different ADET1 characteristics (Figure IV-30.a) progressively increase with the DAC codes for the 1st chip. But theoretically those curves should be merged in a single characteristic. The same effect is observed on ADET2 (Figure IV-30.b). One can conclude that the signals ADET1 and ADET2 seem to be more dependent on the quality of the mmW pad contacts than on the power level itself.



a. ADET1 b. ADET2

Figure IV-30 Measurements at 60GHz on the 1st chip – ADET signals for different DAC control codes



a. ADET1 b. ADET2

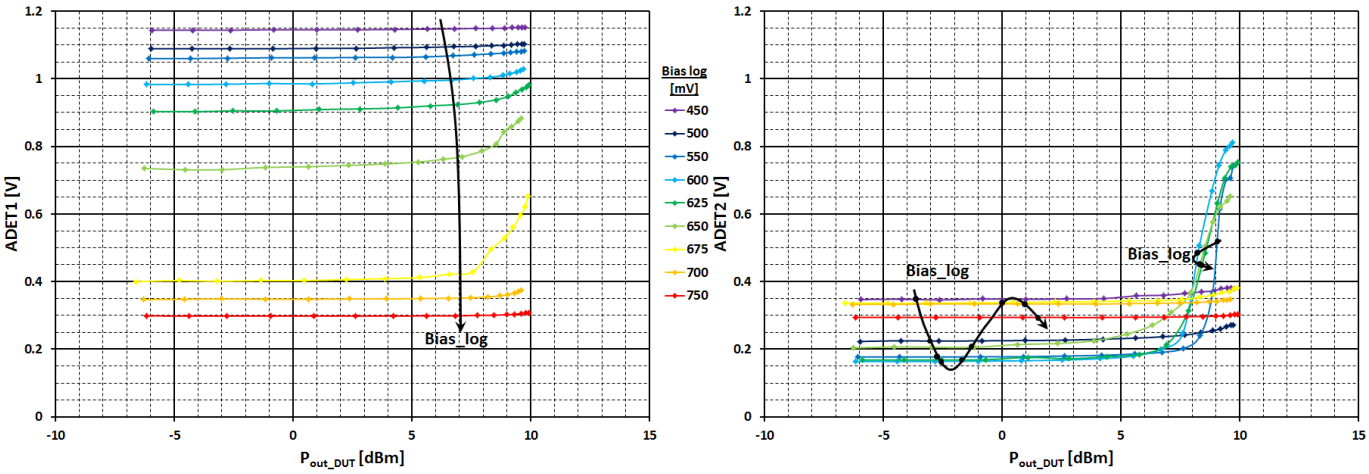
Figure IV-31 Measurements at 60GHz on the 2nd chip – ADET signals for different DAC control codes

Both PCLA are biased by the same *Bias_log* voltage (applied on the pad BIAS_LOG) fixed to 440mV. However their outputs exhibit different behaviors. Considering the 1st chip, when the signal ADET1 presents a very low variation (some 15mV) around a high 1.18V level, the signal ADET2 presents a much larger dependence on P_{out_DUT} (some 75mV) around a much lower 0.5V level. This difference of behavior is inverted considering the 2nd chip.

As a conclusion, there must be a dysfunction in the circuit. This dysfunction should more probably result from a mismatch between the differential input of the PCLA rather than from a design error such as an open of short circuit. The next question is logically: which of the two ADET signals is correct for each test chip? This question can be answered by the study of the influence of *Bias_log* through the measurement results first, then through some retro-simulations.

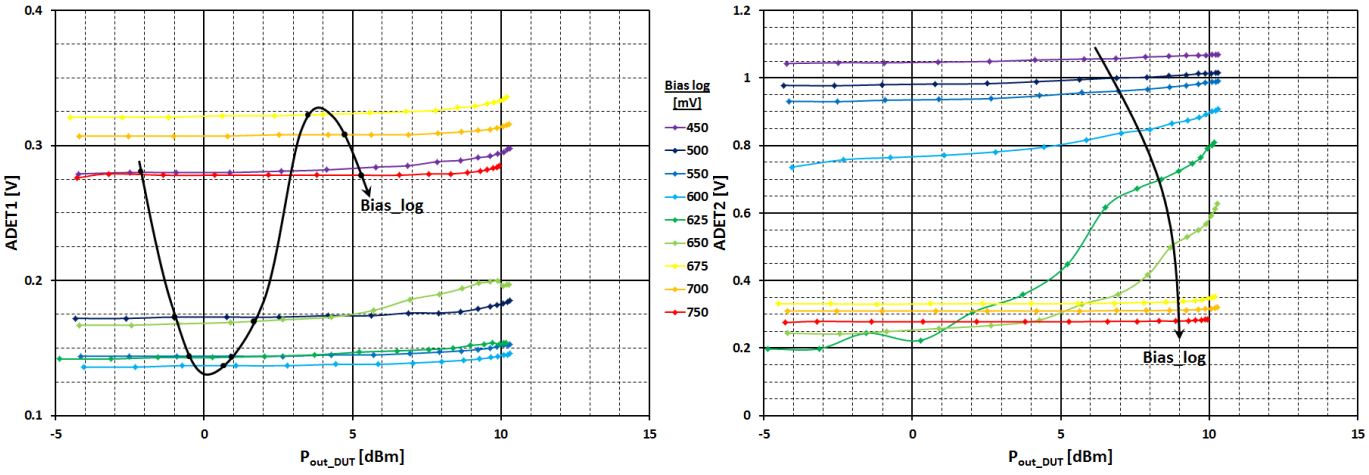
iii. Influence of Bias_log

The DAC code is now fixed to 0 (the highest PPA gain). ADET1 and ADET2 are measured still with respect to P_{out_DUT}, but for different values of *Bias_log* from 450mV up to 750mV. Figure IV-32 and Figure IV-33 show the measurement results for respectively the 1st and the 2nd chips.



a. ADET1 **b. ADET2**

Figure IV-32 Measurements at 60GHz on the 1st chip – ADET vs. P_{out_DUT} for different Bias_log



a. ADET1 **b. ADET2**

Figure IV-33 Measurements at 60GHz on the 2st chip – ADET vs. P_{out_DUT} for different Bias_log

The first observation is that the measurement results obtained previously for 440mV on *Bias_log* are fully coherent with the actual results. For 440mV on *Bias_log*, ADET1 on the 1st chip effectively stay around 1.15V when ADET stay around 0.35V with a larger variation with respect to P_{out_DUT}. Furthermore, this is also inverted on the 2nd chip.

Let us then consider the actual measurement results of Figure IV-32 and Figure IV-33. ADET1 on the 1st chip (Figure IV-32.a) and ADET2 on the 2nd chip (Figure IV-33.b) exhibit a monotonous

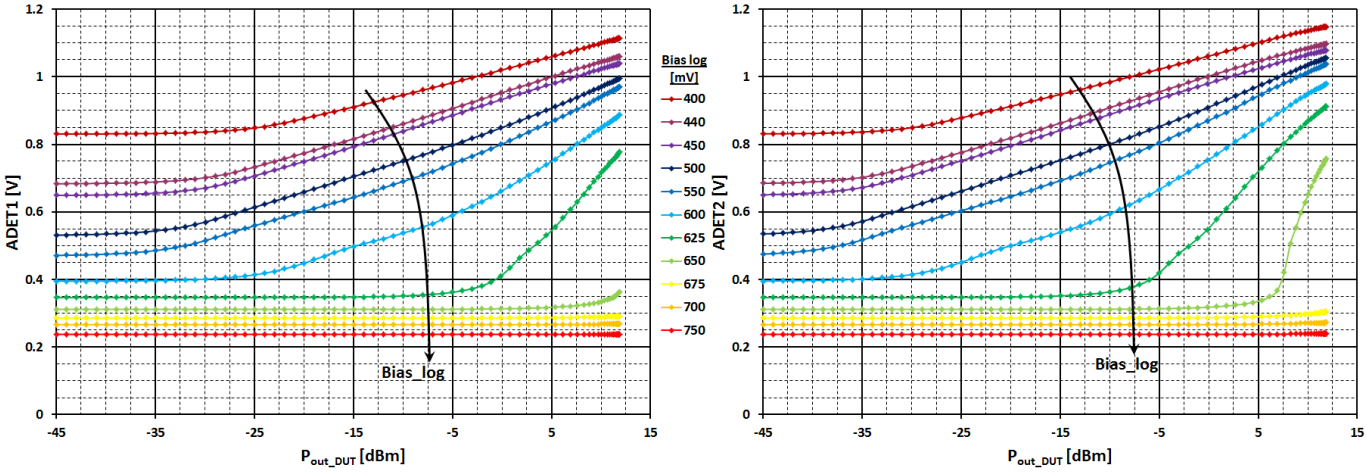
dependence on *Bias_log*. In opposition, ADET2 on the 1st chip (Figure IV-32.b) and ADET1 on the 2nd chip (Figure IV-33.a) show a more complex dependence on *Bias_log*. Moreover, those signals stay in a reduce range between 0.1V and 0.4V, whereas the two first characteristics (ADET1 on the 1st chip and ADET2 on the 2nd chip) vary from 0.2V up to 1.2V depending on *Bias_log*. Some retro-simulations are then required to determine the theoretical *Bias_log* dependence.

iv. Retro-simulations

Some retro-simulations are carried on considering the same schematic that for the initial simulation on the PPA with the power detectors and the associated PCLAs (see Figure IV-19 in section IV.3). Similarly to the measurement presented above, the level of *Bias_log* is progressively tuned from 400mV up to 750mV. Note that the supply voltage in those retro-simulations is fixed to 1.2V, less than the 1.4V applied in the measurements.

The retro-simulation results are shown in Figure IV-34. In those simulations, the best characteristic is obtained for 440mV on *Bias_log* as both ADET1 and ADET2 exhibit more than 20dB linear dynamic range, limited by the PPA output power.

Then, increasing *Bias_log* monotonously decreases the two signals ADET1 and ADET2. This is hence similar to the measurements results on ADET1 for the 1st chip and ADET2 for the 2nd chip. However the simulation results then presents a linear dependence on P_{out_DUT}, which is not so important in the measurements.



a. ADET1 **b. ADET2**

Figure IV-34 Retro-simulation – ADET vs. P_{out_DUT} for different Bias_log

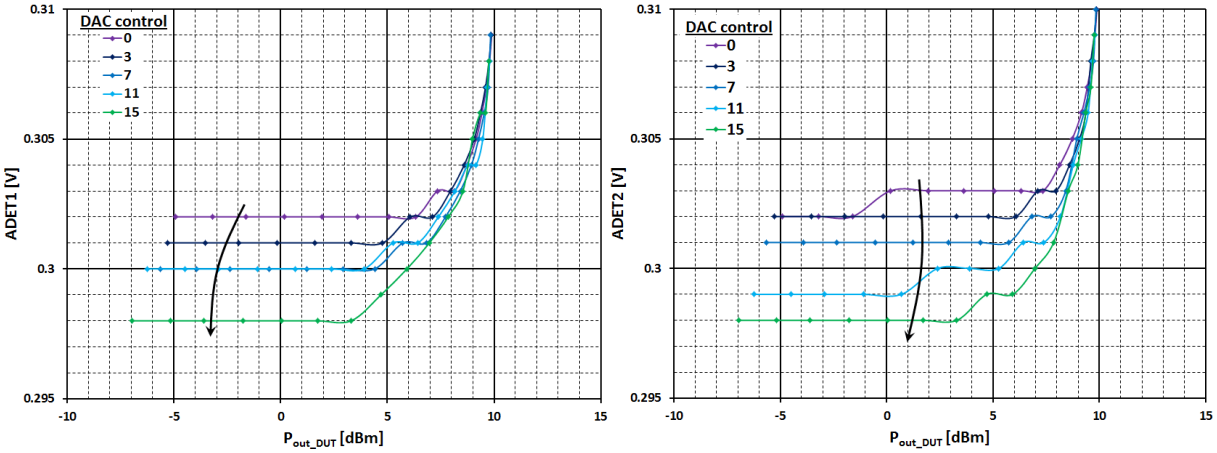
Let us come back to the theory of the PCLA and the influence of *Bias_log* in order to explain the shape of the curves of Figure IV-34. *Bias_log* is actually directly linked to the gain of each elementary compression amplifier integrated in the PCLA. Up to a certain point (550mV on *Bias_log*), a higher gain on the elementary amplifiers increases the dynamic range of the PCLA but reduces its linearity. Moreover, each elementary compression amplifier being biased with a higher current, the sum of all those contributions is also higher. This results in a higher potential difference between the two terminals of the summing resistance – i.e. a decrease of the DC value of ADET1 and ADET2 (see sections III.1.2.vi and III.3.2.i).

To conclude, those retro-simulations put into evidence that this is ADET2 on the 1st chip (Figure IV-32.b) and ADET1 on the 2nd chip (Figure IV-33.a) that suffer from a dysfunction. ADET1 on the 1st chip (Figure IV-32.a) and ADET2 on the 2nd chip (Figure IV-33.b) exhibit normal characteristics.

v. Conclusion for Bias_log

Bias_log is now tuned to obtain a linear variation on the signals ADET1 and ADET2 with respect to P_{out_DUT} before performing load-pull measurements. Figure IV-35 shows ADET1 and ADET2 versus P_{out_DUT} for the 2nd chip and a 710mV *Bias_log* and for 5 different DAC codes.

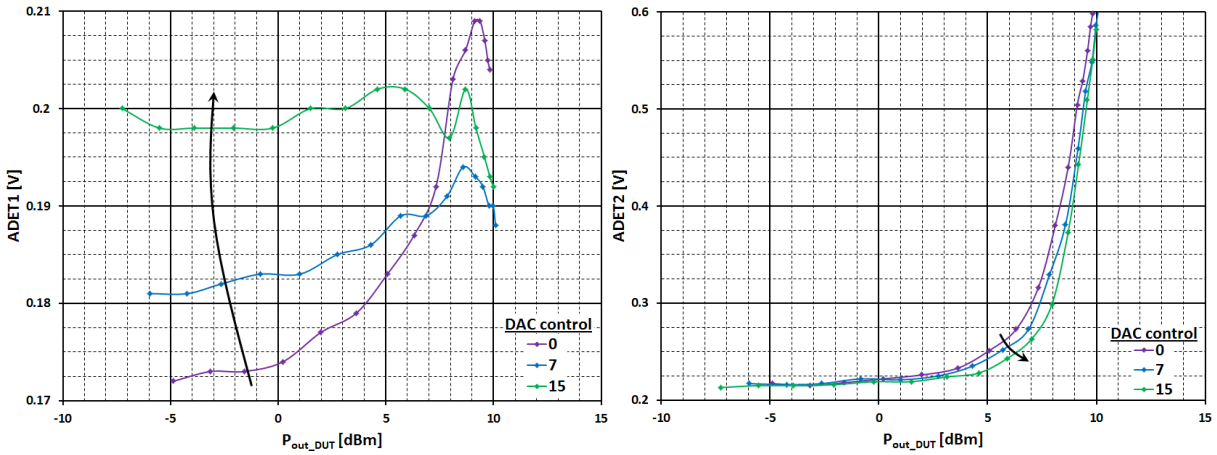
ADET1 and ADET2 exhibit similar characteristics with the same DC level and with a quite linear variation for P_{out_DUT} higher than 7dBm. Moreover this variation does not depend on the DAC code. However the dynamic range of this variation is reduced to about 10mV, which is in the range of the precision of the measure. Performing load-pull measurements with this level on *Bias_log* would then give very weak results.



a. ADET1 **b. ADET2**

Figure IV-35 Measurements at 60GHz on the 2nd chip with 710mV Bias_log

Bias_log is hence lowered down to 670mV. Figure IV-36 shows the measurement results. This level of *Bias_log* optimizes the characteristic ADET2 vs. P_{out_DUT} in terms of dynamic range and linearity. ADET2 actually provides almost 350mV linear variation which is much easier to sense with the multimeters. With the same biasing configuration, ADET1 provides 40mV of variation for the DAC code 0, which should be enough to be sensed by the multimeters.



a. ADET1 **b. ADET2**

Figure IV-36 Measurements at 60GHz on the 2nd chip with 670mV Bias_log

To conclude on those power sweep measurements, this is very difficult to analyze the issue on ADET2 for the 1st chip and on ADET1 for the 2nd chip. The input signals of the PCLA are actually not accessible from the outside of the chip, which gives very few information on the location of the issue. This could actually come from a mismatch between the active detector and the reference detector outputs (see Figure IV-10.a). But this could also come from a dysfunction inside the PCLA.

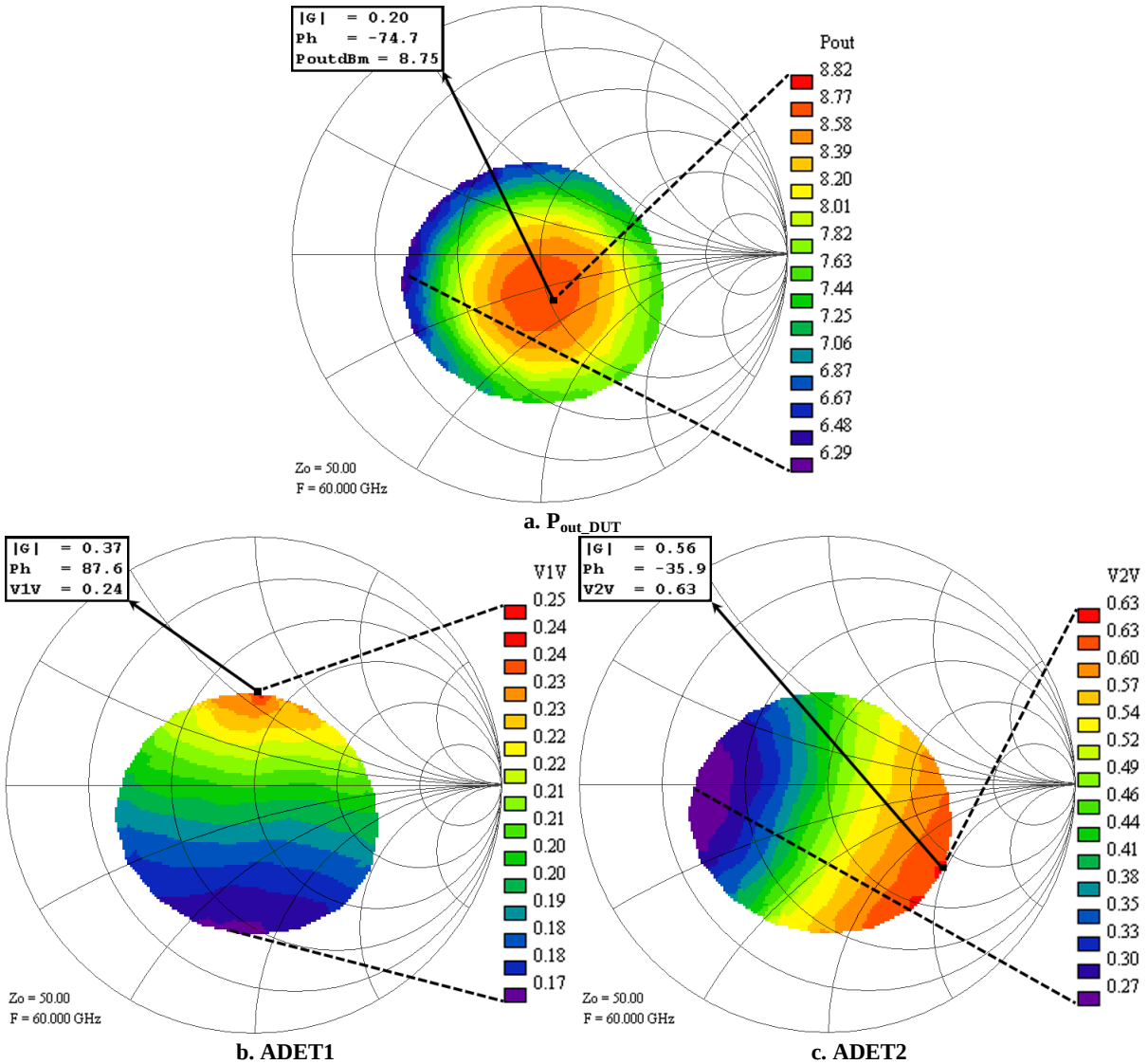
However, by carefully adjusting *Bias_log*, one can obtain usable characteristics on ADET1 and ADET2, which enables the load-pull measurements presented hereafter.

IV.4.5. Load-pull measurements

Load-pull measurements are performed using the IMS environment. The DUT input power P_{in_DUT} is fixed to a constant power (regulated by the software) and the impedance of the load tuned is progressively tuned in order to cover the maximum portion of the Smith chart. The DUT output power P_{out_DUT} and the two voltages ADET1 and ADET2 are then measured and displayed on a Smith chart. The following measurements are all performed on the 2nd chip under a 670mV *Bias_log*.

i. 2nd chip at 60GHz

The first measurements are performed with a 60GHz sinewave input signal with 2.5dBm input power. This is hence large signal measurements and the PPA is close to the saturation as 8.68dBm P_{out_DUT} and 6.15dB gain are measured at 50Ω. Figure IV-37 a., b. and c. show a Smith chart representation of the results respectively for the PPA output power and for ADET1 and ADET2.



a. P_{out_DUT}

b. ADET1 **c. ADET2**

Figure IV-37 Load-pull measurements on the 2nd chip with 670mV Bias_log and with 60GHz sinewave excitation

The maximum power level is obtained for a reflection coefficient Γ of 0.2 amplitude and 75° phase, which is quite close to the desired PPA 50Ω output impedance. The PPA is hence well matched to 50Ω on its output. However, the PPA working in open-loop, P_{out_DUT} varies from 6.29dBm up to 8.8dBm depending on the load impedance.

Considering now ADET1 and ADET2, one can deduce that the two detectors are well able to detect the load impedance mismatch. ADET1 actually varies from 0.17V up to 0.24V. Its minimum

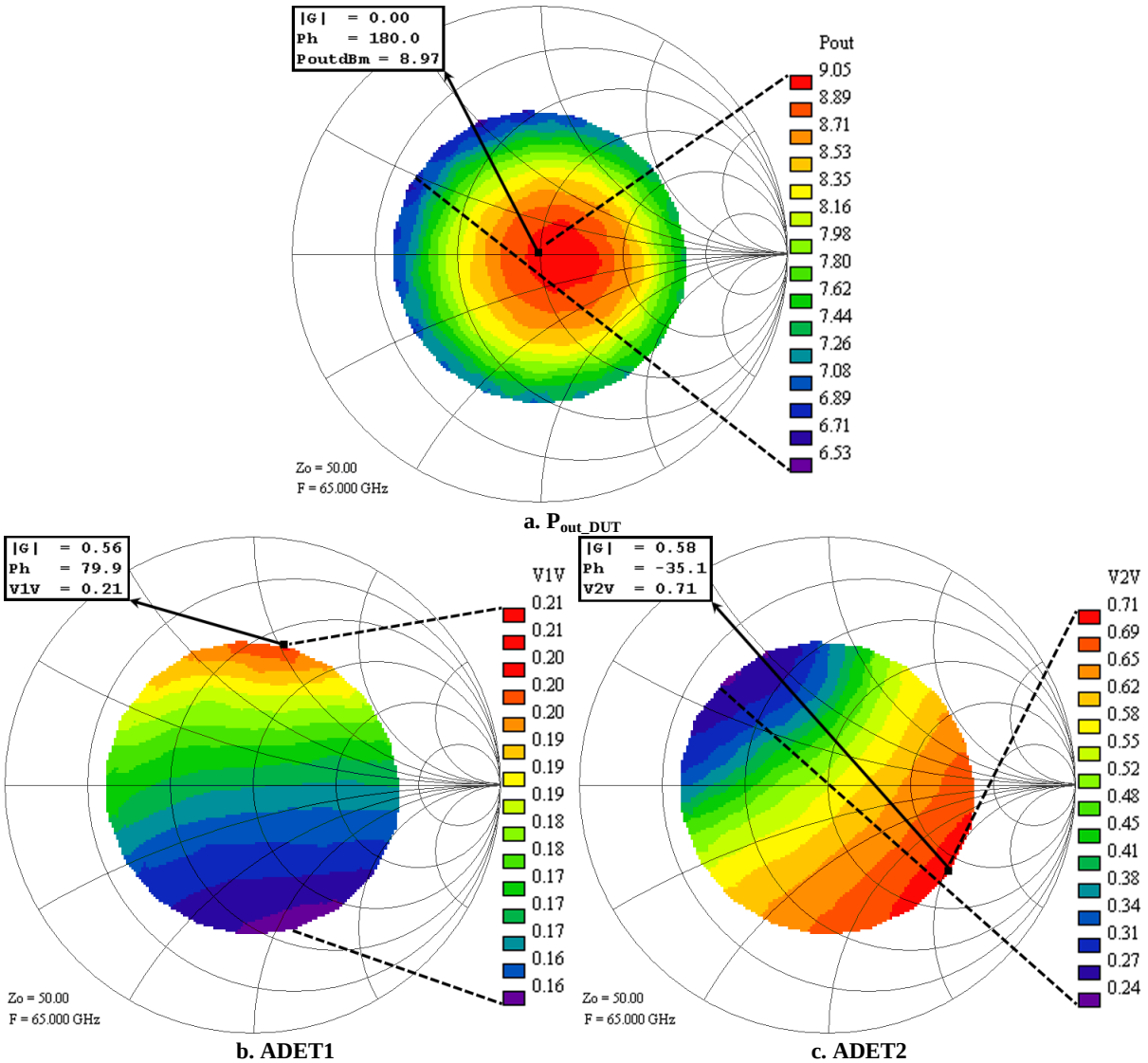
corresponds to a fully capacitive load impedance (arg(Γ)=-90°) and the maximum to a fully inductive impedance (arg(Γ)=90°). On the other hand, ADET2 actually varies from 0.27V up to 0.63V. Its minimum corresponds to a low resistive impedance (arg(Γ)=180°) and the maximum to a high resistive and a little capacitive impedance (arg(Γ)=-20°). Those distributions are fully compliant with the load-pull simulations (see Figure IV-21 in section IV.3.3). Moreover, the values obtained for ADET1 and ADET2 are well in accordance with the characteristics measured in the previous section.

ii. 2nd chip at 65GHz

The same measurements are performed with a 65GHz sinewave input signal. The input power is fixed to 7.3dBm, which gives 9.05dBm P_{out_DUT} and 1.72dB gain. The PPA actually is in deep saturation. The different measurement results are shown in Figure IV-38. ADET1 and ADET2 still have no difficulty to detect the load impedance mismatch.

However the two distributions on the Smith chart have suffered from a small rotation with respect to the 60GHz distributions. ADET1 has turned counterclockwise whereas ADET2 has turned clockwise. This actually results from the constant distance between the 2 detectors, which corresponds to a higher proportion of the wavelength at 65GHz than at 60GHz.

Note finally that ADET2 exhibits larger dynamic range than at 60GHz. But ADET2 starting to saturate, the distribution is less linear at 65GHz than at 60GHz (larger steps at high levels of ADET2).



a. P_{out_DUT}

b. ADET1 **c. ADET2**

Figure IV-38 Load-pull measurements on the 2nd chip with 670mV Bias_log and with 65GHz sinewave excitation

IV.5. VSWR-regulation concept

IV.5.1. Concept overview

The open-loop simulations, in section IV.3, have predicted that the 2 power detectors should be sensitive to the load impedance mismatch and furthermore should give complementary information on this load impedance mismatch. Those predictions are validated by the measurements of the circuit PADet60G detailed in the previous section. However the information given by our 2 power detectors has to be computed in the digital decision block (see Figure IV-8) to close the regulation loop and, so, built a VSWR-regulated PPA.

In this circuit demonstrator, the information that we want to regulate is the PPA output power. The concept here is hence to keep a constant PPA output power whatever the load impedance mismatch is.

Figure IV-39 shows the complexity to establishing a link between the available information, which is given by the 2 power detectors, and the PPA output power, which is what is going to be regulated (Smith charts obtained by simulation).

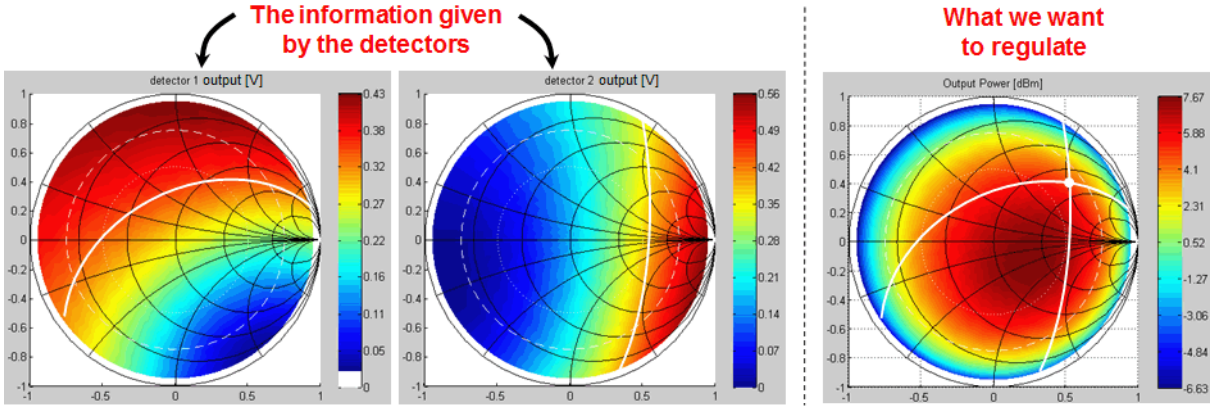


Figure IV-39 Complexity to link the available information with the PPA output power to be regulated

The idea is actually to use the information given by each power detector to reduce the research area of the load impedance from the full Smith chart to only a line, as can be seen on the two first diagrams of Figure IV-39. By correlating those two lines, one can then determine exactly the current impedance presented by the antenna, as can be seen on the last diagram of Figure IV-39. Ideally, if the LADCs at the output of the two power detectors provide sufficient resolution, the 2 lines are very thin and the detected load impedance is reduced to a point on the Smith chart.

Knowing now the current impedance applied on the PPA output, one can determine the DAC code, which means the PPA gain, to apply in order to compensate the output power loss induced by the impedance mismatch. The power loss can be determined either by a theoretical approach (knowing both the PPA output impedance and the antenna input impedance), or by simulation results, or, best of all, by measurement results.

However, for the three possible cases, one should know the desired power level on the PPA output and considering 50Ω antenna impedance. The power loss is actually a function of the 50Ω power level. This information requires the integration of a third power detector, with a phase of the Smith chart distribution different from the 2 detectors already integrated, to be automatically obtained. This 3rd power detector being not integrated in the demonstrator circuit PADet60G, the desired power level on 50Ω antenna impedance should be externally given to the regulation algorithm.

IV.5.2. Algorithm to be implemented in the digital decision block

Figure IV-40 shows a general synoptic of the regulation algorithm to be implemented in the digital decision block. First of all, the decision block has to obtain the current value of the two power detectors and to take into account that the circuit PADet60G generates raw codes which are not

calibrated. The 8 bits with 7.5 significant bits coming from the LADC, here referred as Det<7:0>, have to be interpreted to form a monotonous and linear code on 7bits, referred as Det_c<6:0>, following the LADC calibration procedure explained in section III.2.4.v. This operation has to be performed for the two detectors to compensate the digital multiplexer integrated in PADet60G (see Figure IV-11.c) and obtain the current value of the two power detectors, Det1<6:0> and Det2<6:0>.

Those two values are used to address a table, which gives the DAC code, DAC<4:0>, to be applied to the circuit PADet60G to compensate the impedance mismatch. As previously explained, the two detectors actually give complementary information and the current load impedance is given by correlating those two data. This is directly what is implemented here. The code generated by the 1st detector is used to address the table vertically, whereas the code generated by the 2nd detector is used to address the table horizontally.

As previously mentioned, the power loss, which means the requested PPA gain, is a function of the 50Ω power level at the PPA output. This is schematically represented in Figure IV-40 as a file selection, each file containing the table associated to the current power level. The true difficulty is to establish the table DAC<4:0> = *f(*Det1<6:0>*;* Det2<6:0>*)* for each value of the power level.

A simple calculus tell us each table request 10ko of memory as it contains one 5bits data for each intersection of the 2^7 lines addressed by Det1 and of the 2^7 columns addressed by Det2.

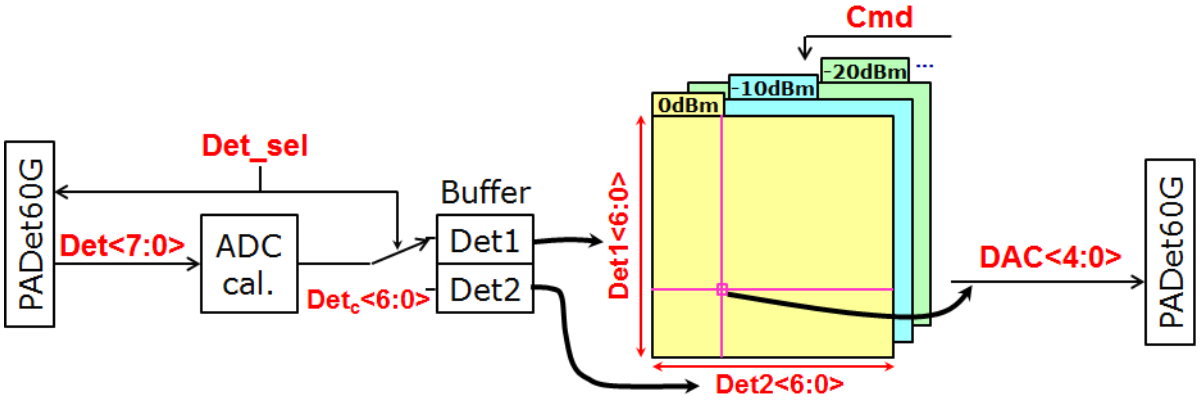


Figure IV-40 Regulation algorithm to be implemented in the FPGA

IV.5.3. Table establishment in a simple practical case

Table IV-5 presents the table to be integrated in the algorithm for a very simple example case where the digital codes coming from the two detectors are reduced to 13 or 14 values. This actually corresponds to the measurements of the 2nd chip of the circuit PADet60G with 670mV *Bias_log* and 15 as DAC code (intermediate value of the PPA gain) for a constant 2.72dBm PPA input power. The method to obtain this table is discussed hereafter.

			ADET2													
	Code			1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Code	Volt.	0.26	0.28	0.3	0.33	0.35	0.37	0.39	0.42	0.44	0.46	0.48	0.5	0.53	0.55	0.57
			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADET1	13	0.21	0	0	0	0	0	0	7	7	8	8	8	0	0	0	0
	12	0.2077	0	0	0	0	5	7	8	9	9	9	8	8	8	0	0
	11	0.2054	0	0	0	7	7	10	10	11	11	10	10	9	9	0	0
	10	0.2031	0	0	5	7	11	12	12	12	12	12	11	11	10	10	0
	9	0.2008	0	5	7	11	13	13	13	13	13	13	13	12	11	10	0
	8	0.1985	0	6	11	12	13	14	14	14	14	14	14	13	12	9	0
	7	0.1962	0	5	11	13	14	14	14	15	15	14	14	13	12	9	9
	6	0.1938	0	4	10	13	14	14	14	15	15	14	14	13	12	10	9
	5	0.1915	0	4	8	11	13	14	14	14	14	14	14	13	12	10	9
	4	0.1892	0	3	4	7	9	11	12	13	13	13	13	12	11	10	9
	3	0.1869	0	2	3	5	6	7	9	10	11	11	11	11	10	9	9
	2	0.1846	0	0	3	3	4	4	5	7	7	8	9	9	9	9	8
	1	0.1823	0	0	0	0	0	3	4	5	5	6	7	7	7	8	8
		0.18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table IV-5 Example of regulation table

In practice, the 2 LADCs integrated in the circuit PADet60G do not exhibit the expected results and no valid code is observed on the digital output DET. This mainly results from the difficulty to obtain valid analog signals from the PCLA integrated in the LADC as explained in section IV.4.4.iii.

One has hence to use the available information coming from the circuit PADet60G to establish the regulation table. The signals ADET1 and ADET2 are so being used, but they are analog signal and digital codes are required to address the table. The idea is then to use external linear ADCs on the signals ADET1 and ADET2 in replacement of the problematic LADCs integrated in the circuit.

In this table establishment explanation, the color codes obtained on the Smith charts a. and b. of Figure IV-41 can be seen as a digital view of the signals ADET1 and ADET2 (the multimeters work as external ADCs). One can then associate codes to analog voltages as it is shown in the first lines and in the first columns of Table IV-5.

Those codes are then used to divide the Smith chart distribution of the PPA output power (Figure IV-41.c) into sections that can be addressed by the color codes of ADET1 (Figure IV-41.a) and ADET2 (Figure IV-41.b). A DAC code being attributed to each section, it results in the Smith chart of Figure IV-41.d. Table IV-5 corresponds to a table view of the diagram of Figure IV-41.d.Obviously, this division is rough here and should be refined to be more realistic.

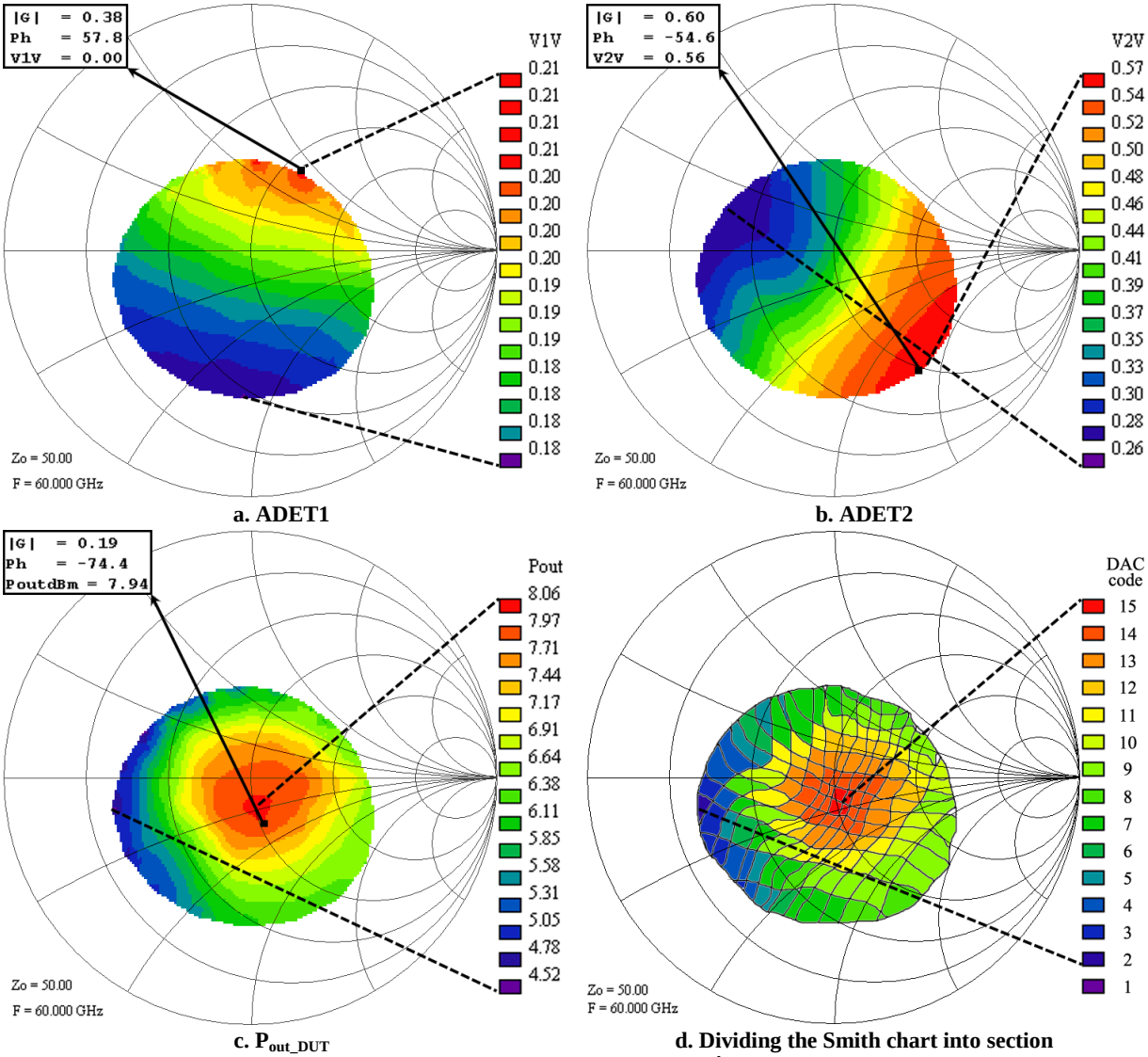


Figure IV-41 Table establishment from load-pull measurements (2nd chip, 650mV Bias_log, 15 DAC code)

Unfortunately, this solution has not been tested yet as it is not possible to send the color code information back to the digital decision block (FPGA).

Chapter conclusion

This chapter has first presented the different solutions to regulate a power amplifier against antenna impedance mismatches. Although a direct regulation on the matching network would be the best solution, this solution is currently not available with the current technology capabilities. Regulations on the driver amplifier or on the power amplifier itself are hence the only available solutions.

This last solution has been chosen to be implemented in the novel architecture which is proposed here. Two feedback loops are integrated to a PA: a fast analog protection loop and a more complex digital regulation loop.

This architecture has been implemented in 65nm CMOS process from STMicroelectronics in a circuit called PADet60G. This circuit notably integrates a PPA, two power detector circuits, two LADCs, one DAC and the protection loop circuitry. The digital decision block is kept external. PADet60G occupies 640x2300µm², but with an active area reduced to 640x400µm².

Some simulations on the analog part of the circuit PADet60G have shown that the two power detectors should be able to sense the variation of the PPA output power on more than 35dB dynamic range. The two power detector should also be able to sense the load impedance mismatch and generate complementary information, which can then be used in a regulation loop.

Three test boards are used to measure this circuit: the Chip Board on which is wirebonded the circuit PADet60G; the Interface Board which generates the different supply and references voltages; and the FPGA DE2 Board from Altera which is used to implement the digital decision block.

Measurement results show that the 5bits DAC is fully functional. The LADC seems to be present a logarithmic characteristic, but noise limitation drastically reduces the dynamic range that can be observed in measurements. The functioning of the LADC can hence not be fully validated.

Measurement results then show that the PPA exhibits 10.44dBm P_{sat}, 5.6dBm *OCP1* and 9.6dB power gain under 1.4V supply. Those results are lower than expected in simulation, but are fully compliant with previous measurement results performed by the designer of the PPA. It is also validated that the DAC effectively controls the gain of the PPA.

Difficulties then occur with the measurement results of the analog signal coming from the two power detectors through the PCLAs. One signal ADET1 or ADET2 actually presents unexpected characteristics on the two chips that have been tested. The associated digital code generated by the LADC does not provide better results (few valid codes), what has brought us to renounce to close the regulation loop the way it was planned.

However, interesting results have been obtained after a careful tuning of the signal *Bias_log*. It has actually be observed, thanks to load-pull measurements, that the two detectors well sense the load impedance mismatch and give complementary results just as it was predicted by the simulations. Similar results have also been obtained at 65Gz.

This chapter concludes by a presentation of the VSWR-regulation concept and by a presentation of the algorithm which should be integrated in the digital decision block. The establishment of a regulation table is also described in a simple but practical case.

A possible way to test this regulation algorithm and close the regulation loop would consist in the use of external ADCs connected on the signals ADET1 and ADET2; the digital code being sent to the FPGA which realizes the regulation algorithm. A module such as the NI USB-6008 from National Instrument, controlled with LabVIEW, could work as the external ADCs. But this solution has not been tested yet.

Chapter references

[1] A. van Bezooijen, R. Mahmoudi, and A. H. M. van Roermund, "Adaptive Methods to Preserve Power Amplifier Linearity Under Antenna Mismatch Conditions," *IEEE Transactions on Circuits and Systems I (TCAS I), Regular Papers*, vol. 52, no. 10, pp. 2101-2108, Oct. 2005.

[2] A. Scuderi, L. La Paglia, F. Carrara, and G. Palmisano, "A High Performance RF Power Amplifier with Protection against Load Mismatches," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, vol. 2, Philadelphia, PA, USA, Jun. 2003, pp. 699-702.

[3] A. Scuderi, L. La Paglia, F. Carrara, and G. Palmisano, "A VSWR-Protected Silicon Bipolar RF Power Amplifier With Soft-Slope Power Control," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 611-621, Mar. 2005.

[4] F. Carrara, C. D. Presti, A. Scuderi, C. Santagati, and G. Palmisano, "A 3W 55% PAE CMOS PA with Closed-Loop 20:1 VSWR Protection," in *IEEE International Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*, vol. 4.2, San Francisco, CA, USA, Feb. 2007, pp. 80-82.

[5] A. van Bezooijen, C. Chanlo, and A. H. M. van Roermund, "Adaptively preserving power amplifier linearity under antenna mismatch," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, vol. 3, Fort Worth, TX, USA, Jun. 2004, pp. 1515-1518.

[6] K. Yamamoto, et al., "A 3.2 V Operation Single-Chip Dual-Band AlGaAs/GaAs HBT MMIC Power Amplifier with Active Feedback Circuit Technique," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1109-1120, Aug. 2000.

[7] J. R. King, "High VSWR mismatch output stage," U.S. Patent 6,137,366, Oct. 24th, 2000.

[8] N. Zimmermann, R. Wunderlich, and S. Heinen, "An over-voltage protection circuit for CMOS power amplifiers," in *IEEE 15th International Conference on Electronics, Circuits and Systems (ICECS)*, St. Julian's, Malta, Sep. 2008, pp. 161-164.

[9] W. Karoui, P. Riondet, T. Parra, and G. Montoriol, "An Adaptative Protection Circuit for Power Amplifer Ruggedness Improvement," in *IEEE Radio Frequency Integrated Circuits (RFIC 2005) Symposium*, Long Beach, CA, USA, Jun. 2005, pp. 433-436.

[10] E. L. Firrao, A. J. Annema, and B. Nauta, "An Automatic Antenna Tuning System Using Only RF Signal Amplitudes," *IEEE Transactions on Circuits and Systems II (TCAS II), Express Briefs*, vol. 55, no. 9, pp. 833-837, Sep. 2008.

[11] Ansoft. (2010, Aug.) HFSS 3D Full-wave Electromagnetic Field Simulation. [Online]. http://www.ansoft.com/products/hf/hfss/

[12] Agilent Technologies. (2010, Aug.) Momentum 3D Planar EM Simulator. [Online]. http://www.agilent.com/find/eesof-momentum

[13] Agilent Technologies. (2010, Aug.) RF Design Environment (RFDE). [Online]. http://www.agilent.com/find/eesof-rfde

[14] M. de Matos, E. Kerhervé, H. Lapuyade, J. B. Bégueret, and Y. Deval. (2009) Centre National pour la Formation en Microélectronique. [Online]. http://www.cnfm.fr/VersionFrancaise/animations/JP/Matos.pdf

Chapter V. System Simulations

Chapter introduction

This last chapter focuses on some research works on the co-simulation of a complete RF/mmW and mixed-signal system. This work has been carried on in close collaboration with the Agilent Technologies on-site support provided to STMicroelectronics. Some advanced research teams from Agilent Technologies have also been working with us in order to solve some issues and to understand some simulator limitations. This project is one of the first application in a realistic industrial environment of the co-simulation of an RF/mmW and mixed-signal system that integrates a regulation loop.

This research co-simulation project has been performed separately from the design flow of the VSWR-regulated PA circuit presented in the previous chapter as it was not already available. This project is hence presented in this separate chapter.

This chapter is divided into two sections. The first one presents the system co-simulation strictly speaking and first introduces the system to be simulated and the co-simulation capabilities using Agilent's software. The implementation of the co-simulation is then detailed, notably the repartition between the three simulator engines: Ptolemy, the envelope simulator and the transient convolution simulator. Some issues that occur during this implementation are then discussed with the solution we have found with Agilent's teams. This system co-simulation section is concluded with some simulation results.

The second section of this chapter focuses on the speed-up of transient simulations. Using multithreading and multiprocessing computing transient simulations, which are traditionally very long with respect to other simulation kinds (DC analysis, envelope, harmonic balance…), can actually be accelerated with up to 5.2 speed-up ratio. Moreover, some typically parallel operations can be evaluated on a GPU which also accelerates the transient simulation with up to 4.3 speed-up ratio. Those too acceleration techniques can be implemented simultaneously. The transient simulation has been accelerated by up to 6.5 speed-up ratio.

Chapter outline

V.1. System co-simulation

V.1.1. Introduction

i. System to be simulated

This work has been initiated in order to check the stability of the regulation loop integrated in the VSWR regulated power amplifier (PA) presented in Chapter IV. The final target is hence to simulate the reaction of the regulated PA to an antenna impedance variation. The system to be simulated, illustrated in Figure V-1, is hence composed as follows.

First of all, the RF direct path is simply composed of a power amplifier connected to an antenna. This RF front-end has been designed to respect the 60GHz W-HDMI specifications.

Then, a regulation loop is integrated into the RF chain in order to regulate the gain of the power amplifier in function of the power level measured between the PA and the antenna. A power coupler and an RMS power detector, both introduced in Chapter II, realize the measure of the power level between the PA and the antenna.

The information given by this detector is converted in the digital domain through a logarithmic ADC, introduced in Chapter III, to be processed in a digital decision block before acting on the PA gain through a DAC. This digital regulation loop works at about 1MHz.

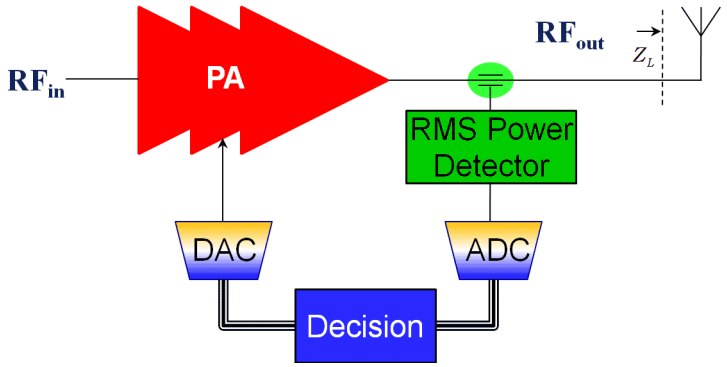


Figure V-1 Block diagram of the system to be simulated

This regulated system has been integrated on a single chip except the antenna and the digital decision block and has been implemented in 65nm bulk CMOS process from STMicroelectronics. The different modules are hence defined at the transistor level.

The major difficulty when trying to simulate such complete systems lies in the high difference between the low frequency phenomenon induced by the digital regulation loop – 1MHz here – and the high frequencies used in the RF chain – 60GHz here. Moreover, the converters between the analog and the digital domain need clock commutations to work correctly which means the DAC and ADC can only be simulated using the transient simulator. But simulating the RF chain (which works at 60GHz) in the time domain on several micro-seconds (in order to obtain sufficient clock cycles to stabilize the regulation loop) is totally impossible and we prefer to simulate such RF chain with envelope simulator.

The solution is hence to simulate simultaneously each block with the most appropriated simulator, what is called a co-simulation. However, performing a co-simulation which integrates a regulation loop is not an easy thing and very few simulation software integrates this capability

ii. ADS co-simulation capabilities

Advanced Design System (ADS) from Agilent Technologies is one major platform that provides an integrated design environment to designers of RF electronic products [**1**]. ADS supports every step of the design process ranging from the schematic capture to the layout and from electromagnetic simulations to complex frequency or time domain circuit simulations. ADS is also progressively

integrating system simulation capabilities in order to answer the needs of RF designers that have to simulate and optimize their complete system integrating simultaneously the RF chain and the baseband DSP.

The last versions of ADS, from ADS 2009 update 1, hence target to enable comprehensive RF mixed-signal system design and optimization with both the behavioral and the transistor-level blocks [**2**]. One example provided by Agilent Technologies (internal documentation) concerns the co-simulation of a complete RF receiver which block diagram is represented in Figure V-2. This RF receiver integrates all the RF chain from the first antenna filter to the down-converter mixers which can be simulated with the circuit envelop simulator. Then the analog-to-digital and the digital-to-analog blocks can be simulated with the transient convolution simulator. And finally, the baseband DSP receiver is described at a behavioral-level and can be simulated using Ptolemy.

The full system can hence be simulated with an ADS co-simulation that uses successively the circuit envelop simulator, the transient convolution simulator and Ptolemy. The major difference between this example and our system lies in the fact that we integrate a regulation loop. In this example, the baseband DSP receiver controls the gain of an amplifier in the RF chain but this control is not dependent of the output of the ADC resulting in an open-loop which is much easier to simulate.

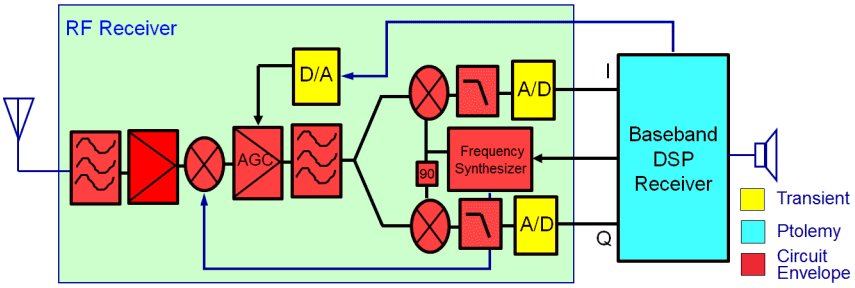


Figure V-2 Example of co-simulation of an RF receiver using ADS

V.1.2. Co-simulation implementation

i. Overview

Figure V-3 shows the detailed block diagram of the circuit to be simulated and the repartition of the different blocks in three modules which are going to be simulated with different tools. This block diagram is similar to the one of the implemented circuit presented in Chapter IV (see Figure IV-8). The only difference lies in the fact that the protection loop is not integrated here. The following simulation hence only focuses on the regulation loop that uses a complex digital decision block.

All the blocks are described at the transistor-level – still except the decision block described at a behavioral-level. Moreover, the pads, which are represented by the small squares in Figure V-3, have also been integrated in this co-simulation, resulting in a problematic extension of the simulation time as it will be discussed in section V.1.3.i.

As for the generic case introduced in the previous section (V.1.1.ii), the system is decomposed in three different blocks which are going to be co-simulated with different simulation engines. The RF path, including the PA, the power couplers, the power detectors and the RF pads, is going to be treated by the envelope simulator. This “envelope block” generates low-frequency signals at the power detector outputs and uses a low-frequency signal as the PA gain control. Those signals hence come from a low-frequency module which is going to be simulated using the transient convolution simulator. This “transient module” integrates the two logarithmic Analog-to-Digital Converters (ADC), the following multiplexer, the Digital-to-Analog Converter (DAC) and all the low-frequency pads. Finally, the digital decisions block which is described at a behavioral-level is simulated using Ptolemy.

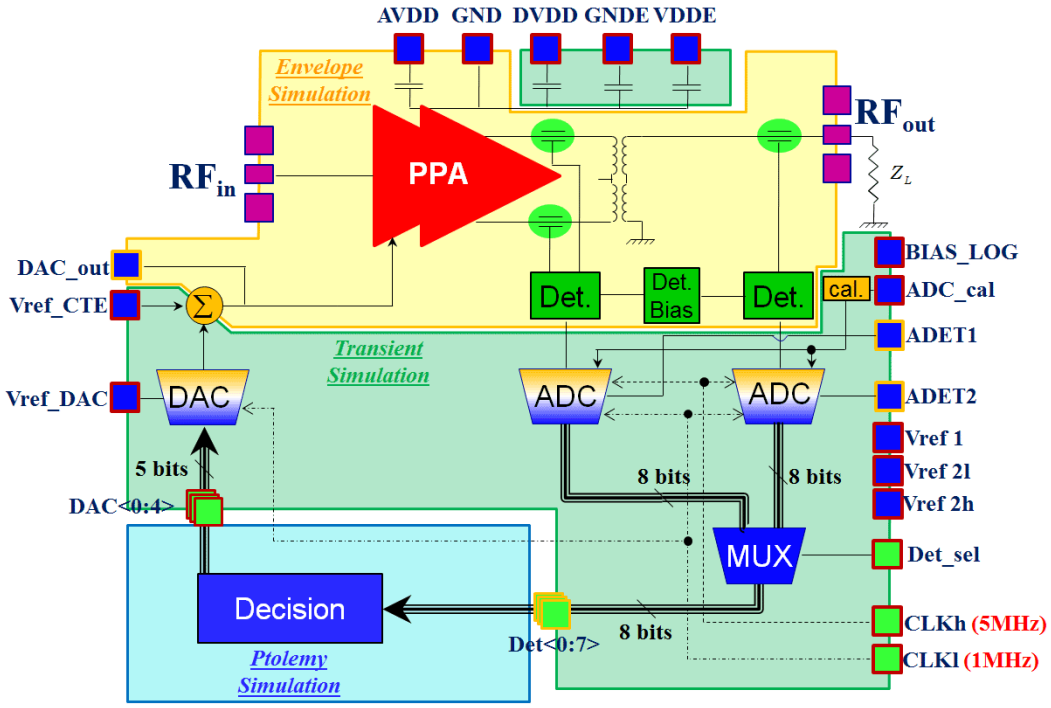


Figure V-3 Block diagram of the implemented co-simulation

ii. Top level schematic under Ptolemy

Figure V-4 is the transcription in ADS of the block diagram presented at Figure V-3. The top-level schematic actually integrates three different modules. At the top lies the power amplifier and RF components which are going to be simulated using the envelope simulator. In the middle of the schematic lies the ADC and DAC module which is going to be simulated using the transient convolution simulator. Finally, the digital decision loop, which is going to be simulated using Ptolemy, lies on the bottom of the schematic. Those three different blocks are detailed here after.

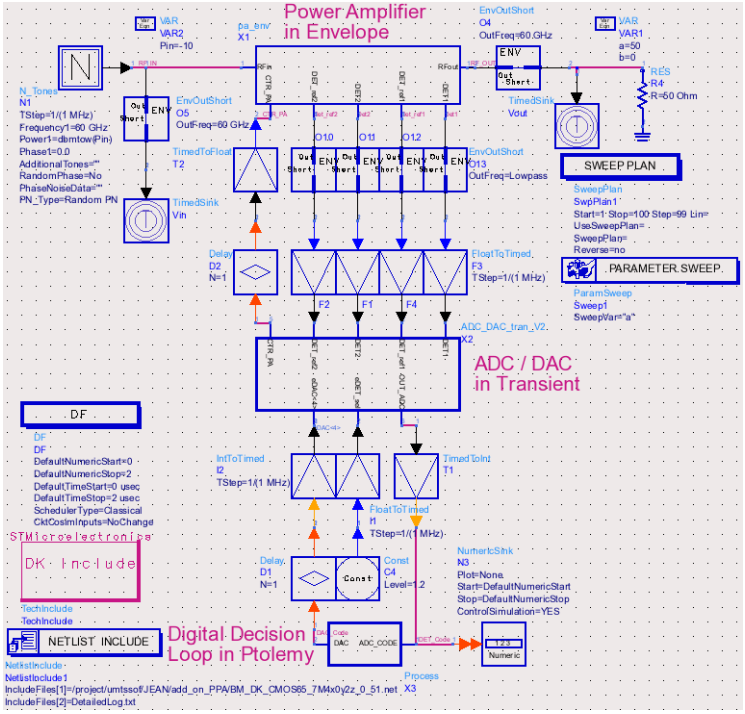


Figure V-4 ADS schematic of the full circuit (top level)

Some additional converters have to be integrated between those modules to realize the data conversion between the different simulation domains. The data coming from the envelope module – which correspond the power detector outputs – are first converted into Ptolemy data thanks to EnvOutShort blocks before being converted thanks to FloadToTimed converters in order to be understood by the transient convolution simulator. At the output of the transient module, the data is directly converted into Ptolemy data (into an integer number) thanks to a TimedToInt converter. The reverse path from the decision block to the envelope module integrates similar data converters. Some delays are integrated in this feedback loop in order to let the time for the regulation loop to initialize itself.

The co-simulation is controlled by Ptolemy which runs successively the envelope simulator and the transient convolution simulator. This is the reason why the data coming from the envelope and the transient modules are first converted into Ptolemy data. Another consequence is that Ptolemy is directly called and parameterized in the top-level schematic of Figure V-4 (the block DF). The digital decision module hence does not call any additional simulator contrarily to the two other modules.

The envelop and transient modules are both defined at a transistor-level which means they both require the Design-Kit (DK) to be defined and parameterized. Defining it inside the two different modules would results in some conflicts as each element of the DK would be defined twice for the simulator. The DK include block is hence integrated at the top-level schematic as can be seen in Figure V-4. Some additional netlist calls are also made at this top-level.

Finally, the PA's load, corresponding to the antenna and represented by a simple impedance, can be easily tuned as it is defined under Ptolemy. A parameter sweep simulation can hence act as a load-pull simulation and can be used to check the reaction of the regulation loop to an antenna impedance variation.

iii. Envelope module

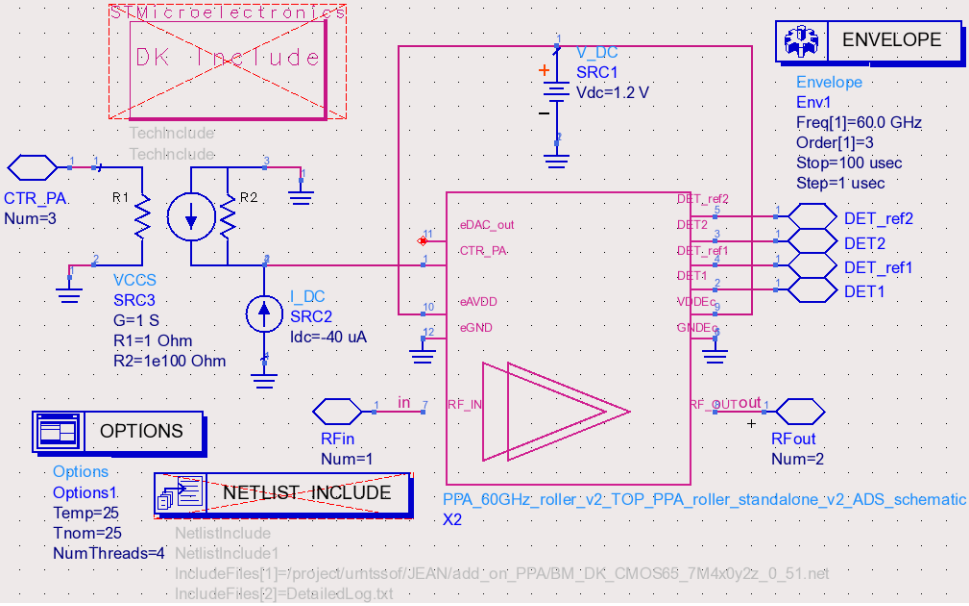


Figure V-5 ADS schematic of the envelope module

Figure V-5 shows the ADS schematic of the envelope module. The DK include and netlist include are both defined in the top-level schematic and are hence not activated here. The envelope simulator, nevertheless, is called and parameterized in this schematic with some options which allows accelerating the simulation thanks to multi-threading computing (see section V.2 for more details).

The signal controlling the gain of the PA comes from the transient module. As it is first converted into Ptolemy data, the signal is considered as voltage information. This voltage information is hence converted in terms of current thanks to a unity gain "Voltage Controlling a Current Source"

(VCCS) component in ADS. The other signals coming to and from this envelope module are directly voltage information which do not need such conversion.

The main component that integrates the PA, the power couplers and the power detectors (PPA_60GHz_roller_v2_TOP_PPA_roller_standalone_v2_ADS_schematic in Figure V-5) is defined at the transistor-level in Cadence environment thanks to the ADS DynamicLink tool from Agilent Technologies [**3**]. When in ADS using the tool "push into the hierarchy" on this block, the Cadense schematic is open. In the same way, a modification on the schematic in Cadence environment is directly taken into account in this ADS envelope simulation. This DynamicLink is very useful to perform powerful ADS simulation with a schematic captured with classical Cadence tools.

This main component, defined in Cadence, integrates some active devices (see Figure I-11 and Figure II-19), but also some passive devices (see Figure IV-12) defined in terms of S-parameters. Those S-parameters have been obtained by performing electromagnetic simulations using Momentum from Agilent Technologies.

iv. Transient module

Figure V-6 shows the ADS schematic of the transient module. Similarly to the previous envelope module, the DK include and the netlist include are not activated here as they are both already defined in the top-level schematic. The transient convolution simulator, nevertheless, is called and parameterized here with some multi-threading options (see section V.2 for more details).

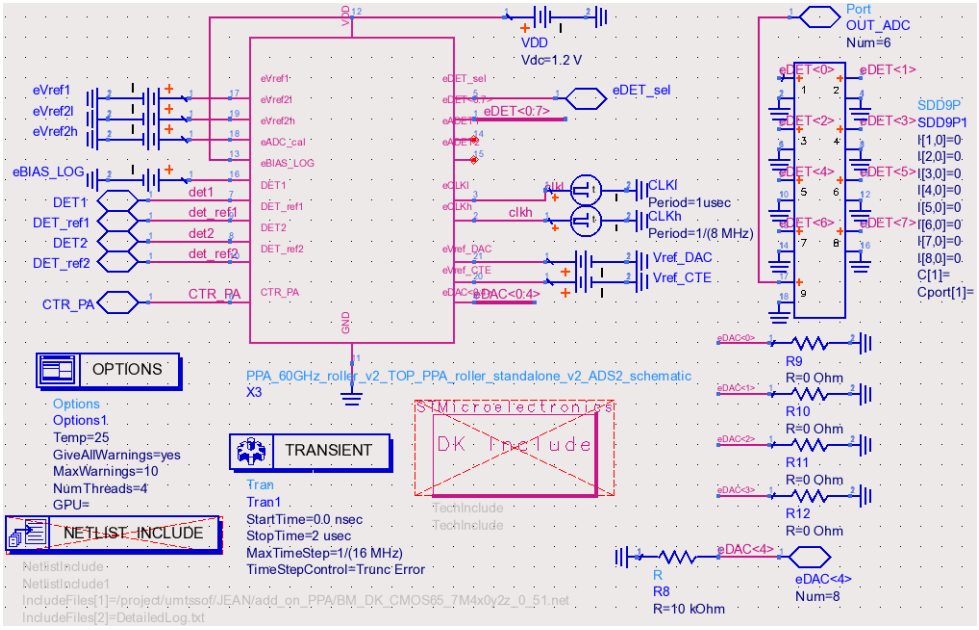


Figure V-6 ADS schematic of the transient module

As for the PA, the couplers and the detectors, the main component of the ADS schematic, which includes the two LADCs and the DAC, is defined at the transistor-level and connected to the Cadence schematic thanks to DynamicLink [**3**]. This component integrates about 10300 transistors defined with the BSIM4 model which makes this transient module the slowest of this co-simulation to simulate.

This schematic also includes some voltage sources and basic components required by the DAC and the ADCs. A 9-ports "Symbolically Defined Device" (SDD9P) is used to convert the 8-bit signal at the output of the ADC multiplexer into a single code that can be directly used in Ptolemy by the decision module.

v. Digital decision module

Figure V-7 shows the ADS schematic of the digital decision module. As introduced in section V.1.2.ii, the simulator is already defined at the top-level schematic. This module has been hierarchized only for readability simplification and is hence directly simulated by Ptolemy simultaneously with the top-level schematic.

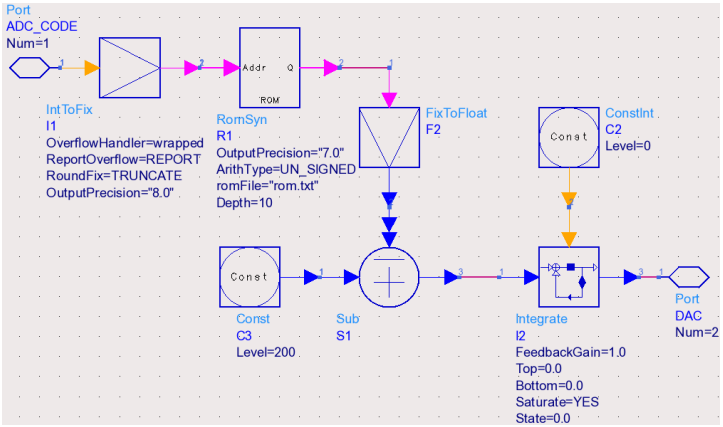


Figure V-7 ADS schematic of the digital decision module

The schematic presented in Figure V-7 is an initial test case which does not correspond to any peculiar regulation scheme. It has been designed to establish a co-simulation architecture that could respond to our system simulation. However this test case integrates several behavioral components such as a Read-Only Memory (ROM) table, which could correspond to the de-embedding of the LADC data (see section III.2.4.v), and an integrator that could works as a very simple regulation loop.

In a second time the simple schematic of Figure V-7 could be replaced directly by the digital regulation loop integrated in the FPGA to perform the digital decision in the practical measurement conditions (see section IV.4). Quartus II from Altera, which is used to program the decision loop in the FPGA, can actually generate a VHDL code of the full FPGA program [**4**]. Ptolemy could then lunch a co-simulation with NCSim from Cadence Design Systems [**5**] or ModelSim from Mentor Graphics [**6**] that directly integrates the VHDL code extracted from Quartus. This could be a good way to push the simulation of the regulated PA as close as possible to the reality. However this has not been tested for time reasons.

V.1.3. Difficulties and solutions

During this study, we have encountered some difficulties to establish a functional simulation and to optimize the different parameters. Some of those difficulties are presented here after with the associated solutions we have developed. The first one is generated by the pad access resistance. The second one concerns the impedance link between the envelope and the transient modules.

i. Pad access resistance

As presented in section V.1.2.i and illustrated in Figure V-3, the RF and DC pads are taken into account in the ADS co-simulation. However we have observed very long simulation times (several tens of hours). Moreover, when using multi-threading computing, the simulation time stay very long and the acceleration was much lower than the theoretical acceleration that should be observed (see section V.2.1). This problem has been reported to Agilent on-site support who has transferred it to Agilent research division in the United-States.

When observing in details the computed matrix of this simulation, the research division has noted a very few occurrence of the ground and supply voltage nodes which means the different elements of the circuit were not directly connected between the supply voltage and the ground. This problem could hence only result from the integration of the pads in the co-simulation. The observation of the electrical model of the different pads puts into evidence this problem.

The pads integrate one resistance to model the resistive metal access between the alucap layer, where the pad is connected to the external of the chip, and the copper layers, where the pad is connected to the internal circuitry. The two supply voltage pads (GND and VDD) hence integrate a very low value (several 10mΩ) access resistance in their model as can be seen in Figure V-8.

The consequence of this resistance would be negligible if no current is consumed on the supplies. When considering the 30mA average current which is consumed by the PA on the analog supply voltage AVDD, the access resistances induce a small voltage drop and rise on respectively AVDD and GND. But this voltage drop and rise fluctuate with the current consumption which means both have to be calculated at each simulation point.

This drastically complicates the simulation matrix as each branch of the circuit is no more calculated with respect to constant voltages generated by ideal sources, but has to be calculated with respect to varying supply voltages which need themselves to be computed with respect to the current consumption of the different branches.

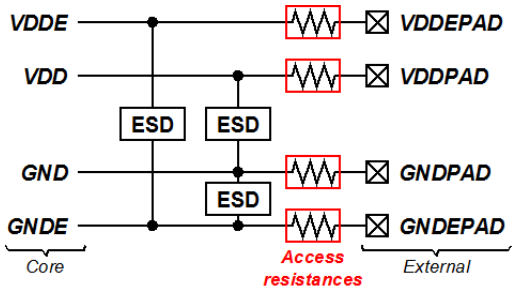


Figure V-8 Schematic model of the supply voltage pads

The only way to overcome this problem is to remove the supply pads. Having no supply pad, no access resistance has to be considered. This means the internal circuitry is directly connected to the external supply sources. This corrects the computed matrix and hence accelerates considerably the simulation.

On the other hand, this simplification introduces a larger gap between the simulation and the reality of the circuit implementation. However, the impact of those resistive accesses on the circuit running has been estimated negligible. Moreover, the quality of the voltage source which is almost never simulated should have more impacts on the circuit operation that the resistive accesses of the pads.

ii. Impedance correspondence between the envelope and the transient modules

Another problem which has been partially solved lies in the fact that the envelope and the transient modules are connected together under a Ptolemy simulation (see Figure V-3). The data coming from and to the envelope module to and from the transient module are hence interpreted as Ptolemy data which means they are not considered as electrical quantity but as dataflow [**7**]. The LADCs in the transient module connected to the output of the power detectors in the envelope module does not load the detectors as no impedance information is given to the envelope module.

This would not pose any problem if the different modules were fully independent. But in our application, the LADCs integrated in the transient module and the detectors integrated in the envelope module are highly interconnected being both integrated in the same chip (see Figure V-3).

The proposed solution, illustrated in Figure V-9, is to transfer the current information from the transient module to the envelope module; the voltage information being already transferred from the envelope module to the transient module. In this way, a regulation loop can be created working on the voltage level and depending on the current consumption. The output voltage of the first module being dependent on the current consumed by the second module, this regulation loop is equivalent to a classical electrical connection working with impedances.

To transfer the current information between the two modules, the current has to be converted into a voltage through a unity gain Current-Controled Voltage Source (CCVS) in the first module and re-converted into a current trhough a unity gain Voltage-Controled Current Source (VCCS) in the second module. With this technique, the data-flow threated by Ptolemy, which realizes the interface between the two modules, is composed only of voltage information.

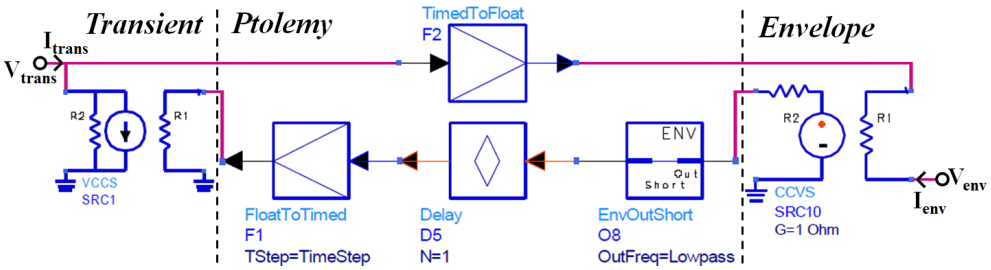


Figure V-9 Proposed solution for impedance correspondence between the envelope and the transient modules

The difficulty to implement this solution lies in the management of the different time streps between the different elements of the co-simulation. Moreover, having integrated a regulation loop between three different simulators engines in the same co-simulation, the loop has to be stabilized thanks to the addition of some delays as have been explained in section V.1.2.

This solution has not been implemented in the full co-simulation yet.

V.1.4. Simulation results

Figure V-10 shows the first results obtained with this co-simulation. The mmW PA input and output voltages are plotted on the first diagram (top left). The PA does not amplifies the signal as the ADC digital input code is null as can be seen on the 3rd diagram (bottom left). The 2nd diagram (top right) shows both the detector and reference detector output voltages and the voltage difference. This difference being almost null, the LADC also outputs a null digital code. The digital decision module which input and outputs are plotted on the 4th diagram (bottom right) has hence an abnormal comportment as its input information is meaningless. Moreover, the regulation algorithm is only for test purpose as evocated in section V.1.2.v.

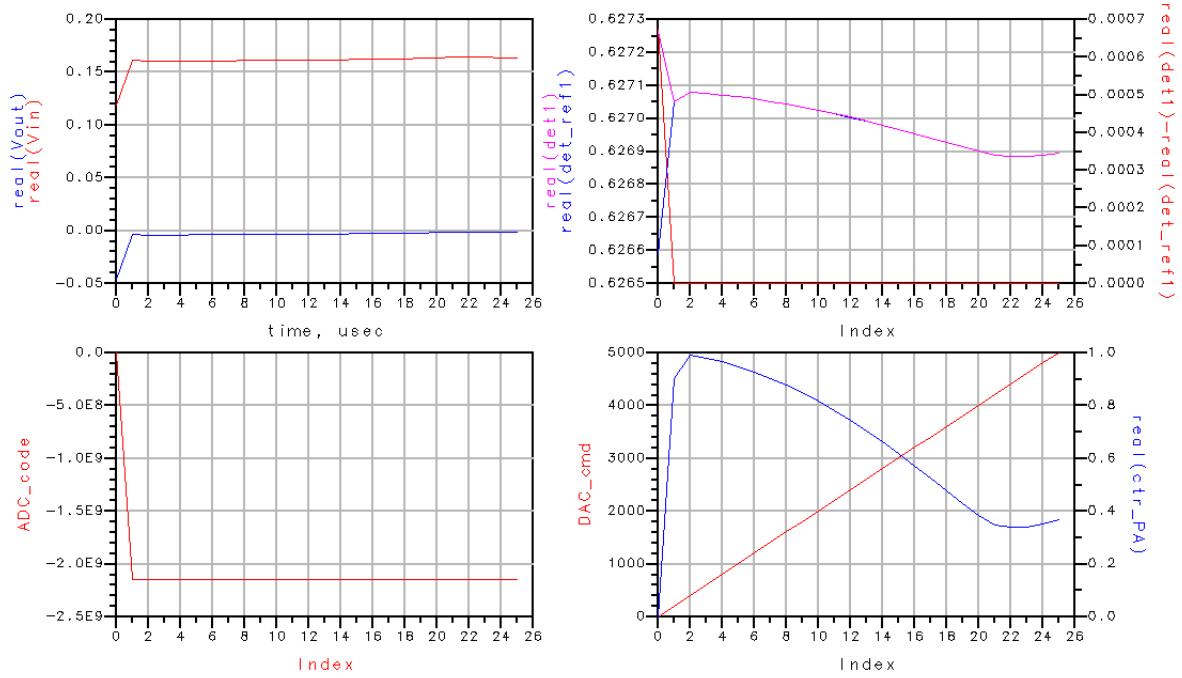


Figure V-10 ADS co-simulation results

Those simulation results cannot actually be used to verify the good working of the regulation loop. However, those results highlight the working of the co-simulation.

It took almost 4 hours of computing to perform this co-simulation on only 25 time steps (1µs per time step). This is too long to plan to perform a simulation with a variation of the PA load impedance in order to verify the reaction of the regulation loop to an antenna impedance variation. Some solutions have hence been investigated to speed-up this co-simulation.

V.2. Transient simulation speedup

In the co-simulation presented above, the major part of the simulation runtime is spent on the evaluation of the transient module. Transient simulations generally require more computing capabilities than the other kinds of simulation as those simulations are performed on relatively long periods with respect to the time-step, which has to be small enough to integrate RF effects at several GHz. And this huge need of computing capabilities is accentuated with large circuits. This is hence totally normal that our transient module, which integrates more than 10200 BSIM4 transistors, needs much longer time to be simulated than the envelope module.

However the simulation runtime of the complete co-simulation is too long (several tens of hours for only 4 or 5 time steps) and does not enable parametric simulations such as antenna impedance variation. We have hence to accelerate the computing time required by the co-simulation which means to accelerate the transient simulation as it consumes the major part of the computing time.

Two techniques of parallelization can be used to accelerate transient simulations: using multithreading and using Graphics Processing Units (GPU). They are both going to be presented and evaluated in this section.

V.2.1. Theoretical speedup

i. Using multiprocessing and multithreading

For decades, it has been considered that the only ways to increase computing capabilities of a computer was either to accelerate the speed of the processor, or to increase the number of bits treated at each operation (the width of the processor bus). Increasing the width of the processor bus is very complicated as the complete architecture and instruction set has to be totally modified. Moreover, most of the processors are already built on 64bits registers while very few software are currently designed to take advantage of those 64bits. On the other hand, accelerating the speed of the processor is also becoming very difficult as the shape of digital signals is no more square when reaching frequencies of several GHz (a square wave involves more than 20 harmonics to have almost vertical edges). Conventional solutions can hence no more be implemented.

The solution that has been found in the early 2000's is to parallelize the computing operations into several cores. The so-called multi-core CPU can hence treat several operations simultaneously and significantly increase its capabilities. However, as several cores are used, they cannot be used at their maximum individual performance. One of the reasons for this lack of scalability is memory bandwidth limitation – the computer's main memory cannot deliver data to the processor cores fast enough to be fully utilized [**8**]. We might cote also Amdahl's law [**9**]: there are parts of the simulator that cannot be written to operate in parallel. If only 90% of the program can be parallelized, then with 8 cores the speedup would only be *100 / (90/8 + 10)* which is 4.7x. With an infinite number of cores the speedup would be a factor of 10x [**8**].

In addition to the parallelization of the cores, the different tasks to be executed can also be parallelized. Multithreading has actually been developed to optimize the use of all the CPU capabilities. By time-division multiplexing, the processor switches between different threads thus being continuously supplied by new computing operations to be performed coming from one or another threads. This globally increases the processor capabilities as the processor has still some calculus to perform even during the different memory accesses – which are relatively slow operations.

ii. Using GPU

The increasing of computing capabilities of the Graphics Processing Units – mainly developed for the video and gaming industries – has progressively interested some software companies from other business. The GPU is then not used for its original graphical applications but simply as an additional computing unit for general purpose applications. This is called General-Purpose computing on Graphics Processing Units (GPGPU) [**10**]. GPGPU has greatly increased since 2006 and the development by Nvidia of the Compute Unified Device Architecture (CUDA). With the addition of

programmable stages, software developers can hence much easily use stream processing on non-graphics data [**10**].

Agilent Technologies has developed GPGPU on transient simulations in ADS by moving the BSIM4 transistor evaluation to the graphics card and take advantage of the one teraflop of performance on a single plug-in card for less than $300 [**8**].

More precisely [**8**], the instance and model parameters for all transistors are copied from the CPU to the GPU once at the beginning of the simulation, as they do not change during the simulation. Then, at the start of every iteration, all the input voltages for the transistors are transferred from the CPU to the GPU. The BSIM4 instances are evaluated on the GPU by computing the currents ***I***, the charges ***Q***, the admittances ***G*** and the capacitances ***C*** from the voltages ***V*** for each transistor. The results Right Hand Side ***RHS*** and Jacobian matrix ***J*** are then transferred back from the GPU to the CPU.

The remainder of the transient simulation is still done with the CPU, notably the evaluation of the devices other than the BSIM4s. This means that currently only BSIM4 transistors are accelerated by activating the GPU. The simulation of a circuit with a very low number of BSIM4 transistors would not be accelerated significantly. Moreover, some technologies are not modeled using BSIM4, but with some other transistor models. Those technologies would not be accelerated using a GPU card.

Figure V-11 shows the speedup of the GPU-based transient simulation over the CPU-based transient simulations [**8**]. The simulations were run on a Dell T7400 workstation with two four-core Intel Xeon X5460 CPUs (multithreading deactivated) running at 3.16GHz, and 16GB of RAM. The GPU was an Nvidia GTX280 with 240 processors running at 1.296GHz and having 1GB of memory. 56 circuits have been simulated both with and without activating the GPU in addition to the CPU (multithreading deactivated). Those 56 circuits can be divided into 2 categories: inverter trees and standard circuits which integrate not only BSIM4 components.

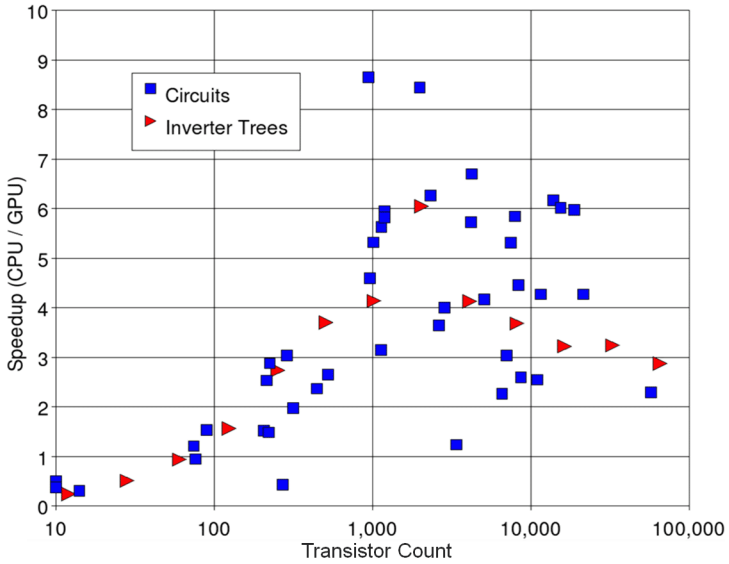


Figure V-11 GPU speed-up with respect to the transistor count for 56 circuits [8]

For small circuits, less than 60 BSIM4 instances, the GPU simulation is slower than the CPU simulation as not all the 240 cores of the GPU are used. Then for circuits including between 60 and 720 BSIM4 instances, the speedup progressively rises from 1 up to 3 (3.8 for the inverter trees) as all the 240 cores of the GPU are used but there are not enough threads running on each GPU – ideal would be between 2 and 4 threads per processor – to take advantage of the maximum capacity of the GPU.

Above 900 transistors, the average speedup is 4.7x with a standard deviation of 1.6, for a one-sigma speedup range of 3.1-6.3x. The deviation is mainly linked to the number of additional components which are still computed on the CPU. The two circuits showing a speedup greater than 8x actually contain very few components other than BSIM4 transistors.

V.2.2. Practical speedup

Some practical experiments have been performed on the transient module detailed in section V.1.2.iv in order to verify the theoretical speedup presented above. The transient simulation has been performed on 25µs with a 62.5ns maximum time step. Considering the theoretical curve of Figure V-11 applied on our 10274 BSIM4 transistors, the GPU advantage for one thread should be between 4x and 6x.

Both the multithreading and the GPU techniques of computing parallelization have been tested simultaneously. Those results are reported in speedup tables (from Table V-1 to Table V-3) by comparing the actual simulation time with respect to the simulation time obtained when computing on only one thread without the use of the GPU. The GPU advantage is then calculated by comparing the speedup obtained with the GPU with respect to the speedup obtained without the GPU both for the same number of threads.

Those experiments were also a way for Agilent to check the proper functioning of the GPU acceleration with a real circuit in the environment of one of their costumer. For this reason, the set of simulations has been repeated identically in both Agilent Technologies and STMicroelectronics environments.

The Agilent Technologies environment is the same of the one presented in [**8**] and detailed above. A Dell T7400 workstation integrates two four-core Intel Xeon X5460 CPUs running at 3.16GHz and 16GB of RAM. The GPU is an Nvidia GTX280 with 240 processors running at 1.296GHz and having 1GB of memory.

On the other hand, the STMicroelectronics environment is composed of a SUN workstation with one eight-core Intel Xeon X5550 CPU running at 2.67GHz and 12GB of RAM. The GPU is an Nvidia Tesla C1060 with 240 processors running at 1.3GHz and having 4GB of DDR3 memory.

Table V-1 presents the speedup results obtain by Rick Poore in the Agilent Technologies environment. The GPU advantage with one activated thread equal to 4.3x is well in the expected range of Figure V-11. With 4 activated threads the GPU advantage decreases to 2x as the CPU alone rises up to 3.1x. Taking advantage of both CPU and GPU the total speedup can reach 6.1x which means a transient which takes 3 hours on a single thread CPU can be performed in about 30 minutes when activating 4 threads and the GPU.

Threads →	1	2	4
CPU	**1.00**	**1.90**	**3.10**
CPU+GPU	**4.30**	**5.30**	**6.10**
GPU Advantage	**4.30**	**2.79**	**1.97**

Table V-1 Transient simulation speedup observed by Agilent Technologies

Table V-2 and Table V-3 present the speedup results obtained by ourselves in the STMicroelectronics environment. The simulation times have also been reported in those two tables for the reader to have an idea of the ranges involves. Table V-2 has been obtained with the Trunc-Error algorithm while Table V-3 has been obtained with the Iteration Count algorithm which has also been used to obtain Table V-1.

Threads →	1	2	3	4	5	6	7	8
CPU	3h01m	1h36m	1h09m	54m	46m	41m	37m	34m
	1.00	**1.87**	**2.60**	**3.32**	**3.90**	**4.41**	**4.87**	**5.19**
CPU+GPU	1h13m	43m	39m	36m	35m	34m	35m	35m
	2.47	**4.16**	**4.61**	**4.97**	**5.04**	**5.26**	**5.17**	**5.07**
GPU Advantage	**2.47**	**2.22**	**1.77**	**1.50**	**1.29**	**1.19**	**1.06**	**0.98**

Table V-2 Transient simulation speedup observed by ourselves using the Trunc-Error Algorithm

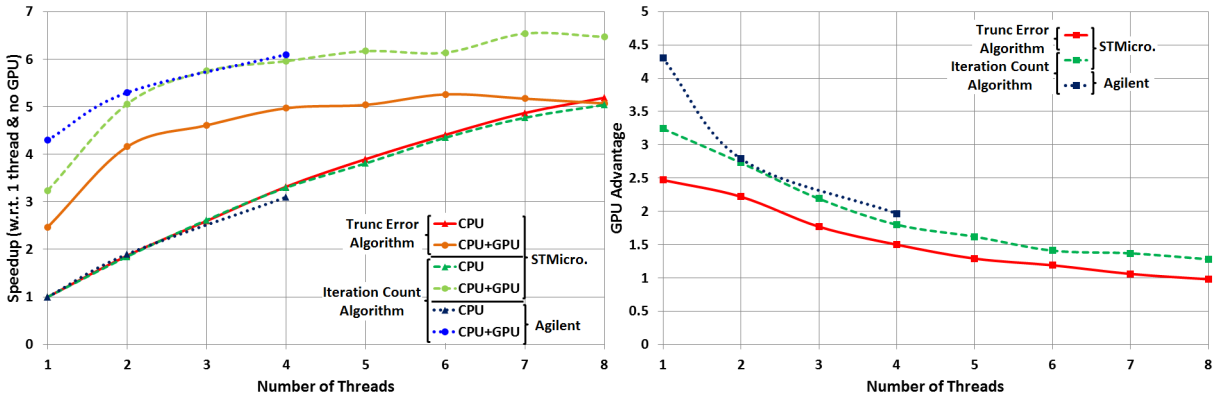
Threads →	1	2	3	4	5	6	7	8
CPU	2h41m	1h27m	1h01m	48m	42m	37m	33m	32m
	1.00	**1.85**	**2.62**	**3.30**	**3.81**	**4.35**	**4.77**	**5.04**
CPU+GPU	49m	31m	28m	27m	26m	26m	24m	24m
	3.24	**5.06**	**5.75**	**5.96**	**6.17**	**6.14**	**6.54**	**6.47**
GPU Advantage	**3.24**	**2.73**	**2.19**	**1.80**	**1.62**	**1.41**	**1.37**	**1.28**

Table V-3 Transient simulation speedup observed by ourselves using the Iteration Count Algorithm

The speedup, obtained for the different simulation conditions, is plotted in Figure V-12.a and the GPU advantage is plotted in Figure V-12.b. It can first be noticed that, for the CPU alone, the speedup is not directly proportional to the number of activated threads. This is the application of Amdahl's law [**9**]. The part of the program which cannot be computed in parallel is responsible of the saturation of the CPU capabilities. We can also calculate this part being about 92.3% in our case.

This effect is more significant when activating the GPU, but the explanation is quite different. The GPU actually computes all the BSIM4 equations which means the CPU is only used to compute the other components equations and to manage the progress of the overall simulation. When increasing the number of active threads the operations which are computed by the CPU are effectively accelerated but not are the operations computed by the GPU. As a conclusion, the activation of several threads hence accelerates the overall simulation but in a much lower range than when the GPU is off. As a result the GPU advantage is progressively reduced with the number of active threads.

Moreover, if the operations computed by the CPU correspond to the part of the program which cannot be parallelized, the saturation of the CPU capabilities is reach for a much lower number of active threads. This is probably also the explanation of the speedup difference between the two truncation algorithms. The iteration count algorithm is much faster than the trunc-error one and the speedup is also larger on the first one than on the second one. However, in this case, the simulation results are not significantly different. We will hence prefer the iteration count algorithm.



a. Speedup **b. GPU advantage**

Figure V-12 Simulated speedup and GPU advantage with respect to the number of threads

To conclude, we can remark the good correlation between the speedup curves obtained for the iteration count algorithm in Agilent environment and in STMicroelectronics environment. It should be noticed that the involved hardware are not totally identical in the two environments, notably the frequency of the processors. Taking advantage of both the eight-core processor and the GPU in STMicroelectronics environment, the transient simulation can be accelerated up to 6.47x from 2h41min down to about 24min.

However those very good results cannot yet be fully exploited in the Ptolemy co-simulation. The multithreading cannot actually be activated in the transient module of the co-simulation as Agilent Technologies is still working both on the co-simulation aspects and on the GPU/multithreading speedup aspects, those developments being made by two different teams. Agilent Technologies should hence implement the compatibility between those two functionalities in the near future.

Chapter conclusion

This chapter has presented both a co-simulation project of an RF/mmW and mixed-signal system, and different techniques to accelerate transient simulations.

The co-simulation project was built on the architecture and on the design of the VSWR-regulated PA presented in Chapter IV. This system has been divided into three different modules which have been simulated using different simulator engines integrated in Advanced Design System from Agilent Technologies. The first module which integrates all the RF/mmW blocks (the PA, the power couplers, and the power detectors) has been simulated with the envelope simulator. The second module which integrates all the data converters (LADC and DAC) has been simulated with the transient convolution simulator. And finally, the rest of the circuit, mostly corresponding to the digital regulation algorithm, has been simulated at a behavioral level with Ptolemy.

Unfortunately the co-simulation project has to be stopped before having obtained interesting results that could be advantageously used in the design flow of the VSWR-regulated PA circuit presented in Chapter IV. The results we have obtained do not actually correspond to the desired function we were trying to simulate. Some discrepancies in the co-simulation schematic are still to be solved, such as the initial condition of the regulation loop. However, having obtained some simulation results already means the co-simulation architecture is functional. This is one major step toward a co-simulation that could be used as part of the design flow. This is also one remarkable step as it is one of the first co-simulation of a regulated system integrating simultaneously mmW transmitter and data converters, both defined at a transistor level, with a behavioral digital regulation loop.

During this study we have tried to accelerate the transient simulation of the system co-simulation – the longest one of the three simulations composing this co-simulation – by reducing the number of transistor defined with complex analog model (BSIM4). All the purely digital logic gates can actually be easily replaced by their behavioral description. However, the simulation results of the "behavioral transient module" were very different from the results obtained with the original block. This probably results from the complexity of the integrated Logarithmic-ADC (see Chapter III) where the analog part cannot be separated from the digital part. We have hence not pursued in this way and have preferred to use multithreading and GPU techniques to accelerate this simulation.

In a second time, this chapter has hence presented two other techniques to accelerate transient simulations. Both techniques are based on the parallelization of the computing operations. The first one dispatches the operations on the different processors, on the different cores or on the different threads which are integrated in the workstation. The second technique uses the very high level of computing capabilities provided by a GPU to lighten the use of the CPU for the computation of BSIM4 models. The use of additional GPU is hence limited to circuits that include a large number of BSIM4 transistors while multithreading can be used regardless of the circuit.

Some speed-up results have been obtained by the simulation in different conditions of the transient module that includes 10274 BSIM4 transistors. We have observed up to 3.3x acceleration using 4-threads and up to 5.2x acceleration using 8-threads when activating the multithreading option. On the other side, we have observed up to 3.2x and up to 4.3x accelerations respectively with ST's and with Agilent's configurations when activating the GPU. Those two techniques can be activated simultaneously which results in up to 6.5 speed-up ratio.

Chapter references

[1] Agilent Technologies. (2010, Jul.) Agilent | Overview: Advanced Design System (ADS). [Online]. http://www.agilent.com/find/eesof-ads

[2] Agilent Technologies. (2010, Jul.) Cosimulation with Analog RF Systems. [Online]. http://edocs.soco.agilent.com/display/ads2009/Cosimulationn+with+Analog-RF+Systems

[3] Agilent Technologies. (2010, Jul.) ADS 2009 - About RFIC Dynamic Link. [Online]. http://edocs.soco.agilent.com/display/ads2009/About+RFIC+Dynamic+Link

[4] "Chapter 1: simulation designs with EDA tools," Altera Quartus II Handbook Version 10.0, Volume 3: Verification, Jul. 2010. [Online]. http://www.altera.com/literature/hb/qts/qts_qii53025.pdf

[5] Cadence. (2010, Aug.) Functional verification. [Online]. http://www.cadence.com/products/fv/Pages/default.aspx

[6] Mentor Graphics. (2010, Aug.) ModelSim: ASIC and FPGA design. [Online]. http://www.mentor.com/products/fv/modelsim/

[7] Agilent Technologies. (2010, Jul.) Theory of operation for ADS Ptolemy simulation. [Online]. http://edocs.soso.agilent.com/display/ads2009/Theory+of+Operation+for+ADS+Ptolemy+Simulation

[8] R. E. Poore, "GPU-accelerated time-domain circuit simulation," in *IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, USA, Sep. 2009, pp. 629-632.

[9] G. M. Amdahl, "Validity of the single processor approach to achieving large scale computing capabilities," in *American Federation of Information Processing Societies - Spring Joint Computer Conference (AFIPS-SJCC)*, vol. 30, Atlantic City, NJ, USA, Apr. 1967, pp. 483-485.

[10] Wikipedia. (2010, Jul.) General-Purpose computing on Graphics Processing Units. [Online]. http://en.wikipedia.org/wiki/GPGPU

General conclusion

This thesis has investigated one major reliability issue on mmW CMOS power amplifiers: the impedance mismatch between the power amplifier and the antenna, which can result from wave propagation obstacles in the close vicinity of the antenna. The phenomenon has first been studied through a theoretical approach. A measurement campaign on antenna VSWR in obstructed vicinity has then been conducted for the first time at the millimeter-wave frequencies, for Wireless-HD applications. The unpublished measurement results are presented in this thesis. Those studies come to the conclusion that a reliable PA working in the 60GHz band should be protected against this phenomenon up to 7:1 VSWR. Moreover, regulation circuitry could also be implemented to automatically compensate the impedance mismatch up to 3:1 VSWR.

This thesis then presents a power detection circuit which aims to detect the antenna impedance mismatch. Based on the square law characteristic of CMOS transistors in saturation, the power detector, which is implemented in 65nm CMOS process from STMicroelectronics, exhibits more than 25dB dynamic range at 60GHz. Using capacitive couplers to interface with the transmitter chain, the implemented power detection circuit presents negligible impact on the 60GHz signal flowing from the PA to the antenna. Load-pull measurement results show that the power detection circuit is able to sense up to 3:1 VSWR, limited by the measurement equipment capability. The design methodology of the capacitive coupler, from the electro-magnetic simulation to the modeling, is notably detailed in this thesis.

This thesis has then introduced a novel architecture of Logarithmic Analog-to-Digital Converter (LADC), which has been patented. Classical linear ADC structures are actually closely connected to the intermediate signals generated by a Progressive Compression Logarithmic Amplifier (PCLA). It results in a very flexible and compact architecture, which is fully compatible with known techniques of ADC linearization. This novel architecture of LADC has been integrated in 65nm CMOS process from STMicroelectronics together with the fully VSWR-regulated PA. The concept of this architecture has been validated in measurements. Nevertheless more experimental investigations should be performed. The digital codes generated by the LADC actually correspond to a logarithmic progression of the input signal.

A novel architecture of VSWR-regulated PA has finally been proposed in this thesis. The system architecture integrates two feedback loops. The first one is analog and aims to protect the PA against overvoltage effects of high values of impedance mismatch. The second one is semi-digital and aims to optimize the PA output power to compensate the losses induced by a variation of the load impedance.

A circuit implementation of the proposed architecture has been realized in 65nm CMOS process from STMicroelectronics. This circuit integrates, amongst other things, a Wireless-HD pre-power amplifier (PPA), a DAC, two power detection circuits, each being connected to a LADC.

Measurement results have shown that the 5bits DAC is fully functional and is efficient to control the gain of the integrated PPA. However, difficulties have been encountered in the measurement of the analog signals ADET1 and ADET2 coming from the two power detectors through the PCLAs. A so far unexplained behavior has actually been observed on one of those two signals for the two chips that have been tested. Consequently, the regulation loop implemented on chip cannot be closed as initially planned.

Nevertheless, open-loop measurement results have shown that the two power detectors sense the load impedance mismatch and give complementary results just as it was predicted by the simulations. This thesis has hence proved that it is probably possible to establish a regulation loop which acts on the gain of a PA, by using only two simple power detectors for the antenna impedance mismatch sensor.

Finally, this thesis has explored the co-simulation aspects of a complex regulated system which integrates RF/mmW elements with mixed-signal data converters and behavioral blocks. This work, carried in close collaboration with Agilent Technologies R&D, has proved that it currently becomes possible to perform a co-simulation of a complex regulated system with elements defined at the transistor level.

Simultaneously to this project, this thesis has evaluated the gain in terms of simulation time which could be expected by implementing parallel computing for transient simulations using Advanced Design System from Agilent Technologies. Speed-ups up to 5.2x and 3.2x have actually been observed when using respectively an 8-threads CPU and a GPU, with respect to a single thread CPU alone. Those two techniques being activated simultaneously, it results in up to 6.5 speed-up ratio.

→ *Future directions*

The scientific progresses presented in this thesis can be continued and developed into several future directions.

As a short term perspective, the regulation loop can be closed by using another external method. The analog signals ADET1 and ADET2 actually give sufficient information for this. The only additional need is to digitize those two signals thanks to external linear ADCs. Many commercial ADC components could fulfill this objective, but the simplest solution is to use a ready-made module such as the NI USB-6008 from National Instrument. This module integrates at least 2 ADCs with sufficient resolution (5V scale digitize on 11bits, which gives 2mV steps, just the required resolution on ADET1). This module can also control 12 digital outputs to send the digital information to the FPGA which integrates the regulation algorithm.

As a mid-term future, the LADC should be implemented in a standalone configuration to provide a direct access to the analog inputs. This implementation may be performed simply by adding pads to the already designed LADC. It could notably validate the novel LADC architecture which has been presented in this thesis.

Finally, as a long term perspective, the proposed architecture for power amplifier protection and regulation against antenna impedance mismatch (see Figure IV-8, page 140) can be generalized to a multipath PA with the architecture presented in Figure X-1 (simplified detection and regulation circuits).

As introduced in section C.3 of Annex C, mmW PAs often overcome the output power limitation (technology limitation) by parallelizing an elementary PA. A power combiner is then requested to sum the contributions of the different elementary PAs before transferring the power to the antenna.

Integrating protection and regulation loops in such complex architecture could result in a much optimized solution with a more advanced regulation strategy. By collecting the information coming from each elementary PA and bringing it to a global decision unit, the power gain could be dispatched on the different paths.

It could hence be decided to supply only one or two signal paths to reduce the global consumption of the multipath PA. Or the decision unit could also dispatch the missing power gain on the other signal paths in case of a breakdown of a dysfunction on one or two elementary PA, hence increasing the lifetime of the multipath PA.

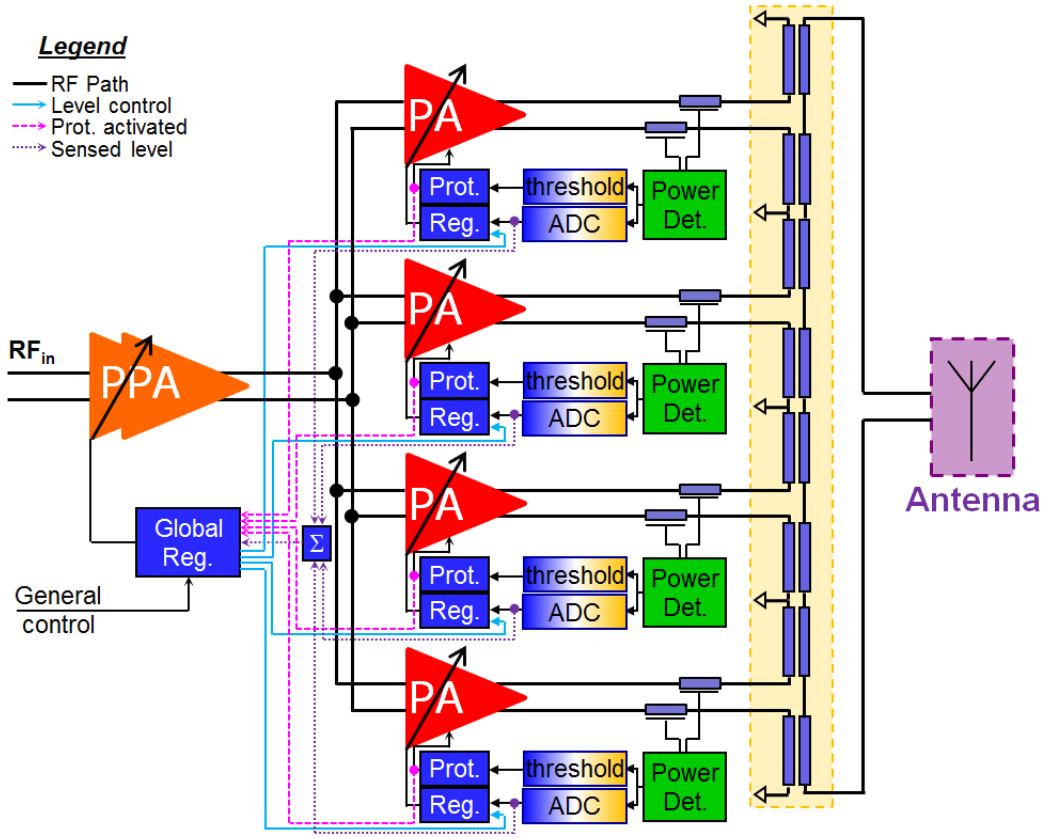


Figure X-1 Proposed VSWR-regulation architecture for a multipath PA

Author's publications

Relative to this thesis :

[1] A. Cathelin, B. Martineau, N. Seller, S. Douyere, **J. Gorisse**, S. Pruvost, C. Raynaud, F. Gianesello, S. Montusclat, S.P. Voinigescu, A.M. Niknejad, D. Belot, and J.P. Schoellkopf, "Design for millimeter-wave applications in silicon technologies", *Proceedings of the 33rd IEEE European Solid State Circuits Conference (ESSCIRC 2007)*, pp 464-471, Munich, Germany, September 2007.

[2] **J. Gorisse.**, A. Cathelin, A. Kaiser, and E. Kerherve, "Détecteur de puissance RMS à 60GHz en CMOS pour la détection de désadaptation d'impédance d'antenne", *Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM 2008)*, Bordeaux, France, May 2008.

[3] **J. Gorisse**, A. Cathelin, A. Kaiser, and E. Kerherve, "A 60GHz CMOS RMS power detector for antenna impedance mismatch detection", *Proceedings of the Joint 6th International IEEE Northeast Workshop on Circuits and Systems (NEWCAS 2008) and TAISA Conference*, pp 93-96, Montréal Canada, June 2008.

[4] **J. Gorisse**, A. Cathelin, A. Kaiser, and E. Kerherve, "A 60GHz 65nm RMS power detector for antenna impedance mismatch detection", *Proceedings of the 35th IEEE European Solid State Circuits Conference (ESSCIRC 2009)*, pp 172-175, Athens, Greece, September 2009.

[5] **J. Gorisse**, A. Cathelin, A. Kaiser, and E. Kerherve, "Progressive Compression Logarithmic Analog-to-Digital Converter", French Patent INPI patent filing, February 2010.

Previous works:

[6] C.N. Nzeza, **J. Gorisse**, A. Frappé, A. Flament, A. Kaiser, and A. Cathelin, "Reconfigurable digital Delta-Sigma Modulator Synthesis for digital wireless transmitters", *Proceedings of the 18th IEEE European Conference on Circuit Theory and Design (ECCTD 2007)*, pp 480-483, Sevilla, Spain, August 2007.

[7] C. Nsiala Nzéza, A. Frappé, **J. Gorisse**, A. Flament, B. Stefanelli, and A. Kaiser, "Reconfigurable RF signal generation for software radio transmitters", *Actes du 8ème colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications (TAISA 2007)*, pp 89-92, Lyon, France, Octobre 2007.

[8] C. Nsiala Nzéza, A. Frappé, **J. Gorisse**, A. Flament, B. Stefanelli, A. Cathelin, and A. Kaiser, "Direct digital RF signal generation for Software-Defined Radio transmitters using reconfigurable Delta-Sigma modulators", *Proceedings of the 11th International Symposium on Microwave and Optical Technology (ISMOT 2007)*, Monte Porzio Catone, Italy, December 2007.

Annex A. Transferring data, audio and video in 2010

Overview

At the time a new high data rate short range wireless specification is being created by different consortiums or IEEE workgroups; it is often useful to investigate the advantages and drawbacks of the different existing solutions. Some wireless or even some wired standards can currently provide similar performance to the emerging Wireless-HD specification. Knowing the data rates and the distance range of the rival specifications gives a good idea of the real capabilities of the new standard.

After having briefly presented the different existing standards to transfer data, audio and video, this annex discusses their main characteristics.

Outline

A.1. Wired connections

A.1.1. Data transfer

In the field of computing equipment there are many standards of wired connections. Some of them are internal to the equipment as the Serial Advanced Technology Attachment (SATA) created in 2003, which enables connecting mass storage devices (hard disc, optical disc…) to the mother board with a data rate of 1.5Gb/s in its first version and 3Gb/s in its second version [**1**]. A third version (3.0) at 6Gb/s has been standardized in May 2009. But wired connections which are internal to the user equipment should not be replaced in the near future by a complex wireless system which will provide lower data rates without any further advantage for the user. So, internal wired connections will not be more detailed herein. In contrary, the external version of this standard the External SATA (eSATA) created in 2004 could be challenged by a Multi Gigabit Wireless System (MGWS) as it offers a 3Gb/s data rate only, what could be the technical limitation of a MGWS. And there are many external wired standards that provide lower data rates that could be replaced by a MGWS.

Universal Serial Bus (USB) enables a 12Mb/s data rate in its version 1.1 of 1998 and 480Mb/s in its version 2.0 of 2000. A "super speed" version 3.0 has just been created to reach a 4800Mb/s data rate using only two additional cables. Products using this specification are expected to arrive in 2010.

The North American equivalent of the European USB, IEEE 1394 standard or FireWire was created in 1995 to replace the parallel Small Computer System Interface (SCSI) standard by a serial interface that furthermore enables the linking with audio and video equipment. The first version of 1995, updated in 2000 (IEEE 1394a) allowed data rates of 100, 200 or 400Mb/s in half-duplex. A 800Mb/s data rate in full-duplex (IEEE 1394b) was added by the second version in 2002 by growing up from 6 to 9 connectors, as well as two higher data rates of 1600Mb/s and 3200Mb/s that are used since 2008.

Ethernet network standard, based on the IEEE 802.3 specification, has been implemented in many versions since its creation in 1983 to evolve with supports technology (coaxial cable, twisted pair, optic fiber…). Considering only twisted pair versions (RJ45 connector), most-used in consumer equipment, the version "e" or 1BASE5 appeared in 1987, with a 1Mb/s data rate. The version "i" or 10BASE-T was released in 1990 which enables a 10Mb/s data rate. In 1995, it is the version "u" also called Fast Ethernet working at 100Mb/s (100BASE-T). In 1998, the data rate reaches 1000Mb/s and this version "z" is called Gigabit Ethernet (1000BASE-T). In 2006, the version "an" or 10GBASE-T adds the 10Gb/s data rate. Other versions are still planned for next years as the "ba" to reach data rates of 40 or 100Gb/s.

A.1.2. Audio and video data transfer

Video Graphic Array (VGA) standard created in 1987 by IBM can manage video transfer with a maximal size of 640x480 pixels and a refreshment frequency up to 70Hz. The color of each pixel is defined thanks to the 3 fundamentals colors, Red, Green and Blue (RGB) and transferred in an analog way. In analog video standards the appearance of each pixel may be affected by its adjacent pixels and by many analog signal distortions. For this reason, analog standards are often replaced by digital ones that don't have those drawbacks.

The Digital Visual Interface (DVI) was created in 1999 as the video interface standard that transfers uncompressed digital video data to a display. The largest resolution possible with a single DVI link is 2.75megapixels at 60Hz that allows screen resolutions of 1915x1436 (ratio 4:3), 1854x1483 (ratio 5:4) and 2098x1311 (ratio 8:5). Each pixel is defined by its RGB components on 24bits (3x8). Thereby the total data rate of a single DVI link is 3.96Gb/s. A dual DVI link exists too that doubles the data rate so 7.92Gb/s providing the resolution of 4megapixels (screen resolution WQXGA of 2560x1600) at 60Hz (the resolution is inversely proportional to the frequency as the data rate is constant) or doubling the number of bits per pixel.

High Definition Multimedia Interface (HDMI) was created at the end of 2002 to transfer uncompressed digital video data to a display, as the DVI, but also to transfer digital audio data. The maximum screen resolution allowed is WQXGA 2560x1600 (either called 1600p) at 75Hz and 24bits

per pixel or WUXGA 1920x1200 at 60Hz and 48bits per pixel, what makes a video data rate of 8.62Gb/s when using the Coordinated Video Timings - Reduced Blanking (CVT-RB) for display synchronization. HDMI supports 8 audio channels at sample sizes up to 24bits with sample rates up to 192kHz what makes an audio data rate of 36.86Mb/s. Using the Transition Minimized Differential Signaling (TMDS) coding technology for minimizing the electromagnetic interferences due to high-speed serial data transmission, the final data rate for version 1.3 of HDMI (audio and video) is 10.2Gb/s. Previous versions 1.0 to 1.2a had a lower data rate of 4.95Gb/s.

As for wired data transfer standards, audio and video existing standards could be replaced by a wireless link. However the 10.2Gb/s data rate provided by the version 1.3 of HDMI seems to be very difficult to reach by a wireless link considering the additional constraints of power consumption and chip integration induced by mobile applications.

A MGWS which would provide a useful Video link should be able to transfer HDTV that means 1920x1080i at 60Hz. That makes 2,073,600 pixels 60 times per second; that is 124,416,000 pixels per second. Each pixel is coded on 24 bits. The resulting video data rate is 2.78 Gb/s. Hence, the Wireless-HDMI standard logically targets a 3Gb/s data rate link for HDTV applications [**2**].

Some Wireless Personal Area Network (WPAN) and Wireless Local Area Network (WLAN) standards could be upgraded to a MGWS too.

A.2. Wireless connections

A.2.1. Wireless Personal Area Network

WPAN is used to interconnect devices that are within a personal workspace – typically less than 10m – without any wire. Infra-red Data Association (IrDA) is one of the oldest PAN standard that could provide data rates from 2.4kb/s to 16Mb/s in a distance range less than 1m by an optical link. For radio frequencies standardization of WPAN, the IEEE Standards Association has established the working group IEEE 802.15, which is specialized in WPAN standards. It includes six task groups.

Task Group 1 (TG1) wrote the IEEE 802.15.1-2002 standard in 2002, which is based on the Bluetooth V1.1 specifications, a corrected version of the first V1.0 created in 1999 by the Bluetooth Special Interest Group (Bluetooth SIG). This standard provides a 721kb/s data rate. An updated version was published as IEEE 802.15.1-2005 based upon the additions incorporated into Bluetooth V1.2. The IEEE TG1 has then decided to suspend their relationship with the Bluetooth SIG. Furthermore, the version 2.0 of Bluetooth specifications with Enhanced Data Rate (EDR) was written in November 2004 increasing the data rate up to 3Mb/s.

Task Group 2 (TG2) works on the coexistence of WPAN with other wireless devices operating in unlicensed frequency bands such as WLAN.

Task Group 3 (TG3) is specialized in High Data Rate WPAN. It wrote the standard IEEE 802.15.3-2003 that provides data rates from 11 to 54Mb/s working in the 2.4 to 2.4835GHz band. This TG was divided in 3 different sub-groups (a, b and c). The first one, called TG3a, was to provide an alternative higher speed Ultra Wide-Band (UWB) Physical Layer (PHY) working in the 3.1 to 10.6GHz band. 23 PHY specifications were merged into two proposals based on very different modulation schemes: one on the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) UWB could provide data rates up to 480Mb/s and was supported by the WiMedia Alliance; and the other on Direct Sequence – UWB (DS-UWB) could provide data rates up to 1320Mb/s and was supported by the UWB Forum. In 2006, as no compromise was conceivable between those two proposals, this IEEE work group was abandoned concluding that it was probably too early to write a UWB standard. However each alliance continues to support its specification out of the IEEE Standards Association.

The second sub-group of TG3, called TG3b, is working on an amendment to IEEE 802.15.3 on the MAC specifications.

The third sub-group, called TG3c, was formed in March 2005 to supply a millimeter-wave alternative PHY, which should provide data rates up to 3Gb/s and more using the 7GHz unlicensed wide band ranging from 57 to 64GHz. This task group is of special interest for us as it is the one which has to write a complete 60GHz WPAN specification.

Task Group 4 (TG4) is specialized in Low Rate WPAN (LR-WPAN). In October 2003, IEEE 802.15.4-2003 was written. It specifies the MAC and PHY layers. This standard is a Low-Rate WPAN (LR-PAN) for which objectives are: ease of installation (self-organizing mesh network), reliable data transfer, short-range operation, extremely low cost, and a reasonable battery life-time. 2 PHY layers are defined in the first version: one working in the 868/915MHz bands providing data rates of 20 and 40kb/s; and the other in the 2450MHz band providing 250kb/s of data rate. The second version of 2006 adds 2 PHY layers: one increasing the data rates in the 868/925MHz bands to 100 and 250kb/s; the other changing the modulation scheme in the 868/925MHs bands. In August 2007 was adopted IEEE 802.15.4-2006 (from the Task Group 4a) that adds 2 PHY layers: one using Ultra-WideBand (UWB) Pulse Radio in three frequency bands (below 1GHz, between 3 and 5GHz, and between 6 and 10GHz); the other changing the modulation scheme in the 2,450MHz ISM band. Another modification provided by this update is the addition of high precision ranging and location capability (1m accuracy and better). Based on this IEEE standard was created ZigBee in December 2004, which targets applications such as industrial control, embedded sensing, medical and security data collection and building and home automation.

Finally, Task Group 5 (TG5) and Task Group 6 (TG6) are focusing on mesh networking and on Body Area Network (BAN) respectively.

A.2.2. Wireless Local Area Network

WLAN is used to interconnect devices that are in a limited area – typically from 10 to 100m – without using wires. The IEEE Standards Association has decided to allocate a work group IEEE 802.11 to deal with WLAN standards [**1**]. In 1997, after 7 years of discussion, the first WLAN standard was created and called IEEE 802.11-1997 (legacy mode) or more commonly WiFi as it resulted from the collaboration with the WiFi Alliance. This first standard provides two data rates of 1 and 2Mb/s and uses the ISM frequency band at 2.4GHz. Many versions have been written since to improve the data rate, or the range, or to change the frequency band. The following detailed standards contain the most important evolutions.

IEEE 802.11a-1999 (WiFi-a) uses the ISM frequency band at 5GHz and provides a maximum net data rate of 54Mb/s. Using a higher frequency band, WiFi-a avoids the use of the crowded 2.4GHz ISM frequency band (microwave ovens, Bluetooth devices, baby monitors, cordless phones…). But this reduces the distance range as signals are absorbed more readily by walls and other obstacles in their path.

IEEE 802.11b-1999 (WiFi-b) is the first really popular WLAN standard. This is in fact an upgrade of the IEEE 802.11-1997 as the frequency band is the same and the MAC layer is the same too. The modulation technique is only an extension of the one defined in the original standard, which allows a maximum data rate of 11Mb/s.

IEEE 802.11g-2003 uses the frequency band of IEEE 802.11b-1999 with the OFDM based transmission technique of IEEE 802.11a-1999. The resulting maximum data rate is 54Mb/s. Officially ratified in June 2003, most of the consumer equipment produced since summer 2003 were dual-band (ISM 2.4 and 5GHz) and tri-mode, supporting a, b and g specifications.

In 2007, the task group "am" merged 8 amendments (IEEE 802.11a, b, d, e, g, h, i, j) and the base standard into a single document IEEE 802.11-2007, which contains cumulative changes from other previously ratified IEEE 802.11 standards.

IEEE 802.11n is an amendment which adds Multiple-Input Multiple-Output (MIMO) technique thanks to the use of several antennas for both emission and reception. The resulting data rate is considerably increased in comparison with single antenna links, stretch to 540Mb/s. The distance range is enhanced too, up to 250m in free space (outdoor). This amendment has been ratified in

October 2009 although since 2008 many "Draft N" products have been created, which provides data rates up to 300Mb/s.

IEEE 802.11y is another amendment (not yet approved), which increased considerably the transmitted power (up to 20W EIRP) and used the 3,650 to 3,700MHz band in the United-States. Such High-Power WiFi should be able to operate at a distance of 5km or more with data rates up to 54Mb/s. Targeted applications are for backhaul, fixed point to point or point to mobile links, Last-Mile Wireless Broadband Access…

A.2.3. Other wireless communication systems

The IEEE 802-2001 standard defines the Metropolitan Area Network as "optimized for a larger geographical area than a LAN, ranging from several blocks of buildings to entire cities". In practice, Wireless Metropolitan Area Networks (WMAN) are built to be a tradeoff between the long range provided by mobile phones and the data rate provided by LAN such as WiFi.

The Task Group IEEE 802.16 has been allocated to create a WMAN standard and has been dubbed "WiMAX" (for Worldwide Interoperability for Microwave Access) by the industry group WiMAX Forum. In 2001 was written the IEEE 802.16-2001 standard that specified a point to multipoint Broadband Wireless transmission in the 10-66GHz band. IEEE 802.16a-2003, adopted in 2003, delivered a point to multipoint capability in the 2-11GHz band and refined the modulation to work even in Non-Line-Of-Sight (NLOS) situations to provide "last mile" fixed broadband access. In 2004, the IEEE 802.16d-2004 superseded the earlier 802.16 documents and aligned with the HIPERMAN standard (High Performance Radio MAN) provided by the ETSI. Mobility aspects were considered in the IEEE 802.16e-2005 document including also better support for Quality of Service (QoS). WiMAX can provide a data rate of 10Mb/s at 10km in Light-of-Sight (LoS) mobile applications. It can reach higher data rates up to 70Mb/s at lower range and operate at a higher range up to 50km with lower data rates. An amendment is currently at pre-draft stage, IEEE 802.16m and should be approved in March 2010. In this amendment, data rates are planned to reach 100Mb/s for mobile applications and 1Gb/s for fixed applications.

With a similar goal than IEEE 802.16e, the Task Group IEEE 802.20 works on a Mobile Broadband Wireless Access (MBWA), nicknamed as Mobile-Fi. This standard is at draft stage as a first draft was approved in early 2006. It specifies the use of frequency bands below 3.5GHz and the peak data rate of 1Mb/s.

In 2004, IEEE 802 also allocated a Task Group 802.22 to work on a Wireless Regional Area Network (WRAM). Using unused channels of the allocated TV frequency spectrum in an opportunistic way (cognitive radio), it should provide a maximum data rate of 19Mb/s at a 30km distance or higher.

A.2.4. Mobile phones

Finally, although Mobile phones are not fundamentally designed for data transfer, recent standards have added this useful function to the regular sound transfer. So it seems interesting to have a look on digital cellular phone standards.

In 1992 the European Telecommunication Standard Institute (ETSI) created the Global System for Mobile communications (GSM) standard which is the 2nd generation of Mobile phone standard (1st one was not a mass market). The GSM provides a data rate of 9.6kb/s that does not allow data transfer or internet connection. To increase the data rate, the General Packet Radio Service (GPRS) was created in 2001. By using several time slots per user – in previous GSM standard, each user uses only one of the eight slot of time – GPRS provides data rates up to 170kb/s. Thus enabling wireless multimedia IP-based data services and applications. In 2002, by using a different modulation and new channel coding schemes, Enhanced Data rates for GSM Evolution (EDGE) increased again the data rate to reach 384kb/s.

Those standards use several frequency bands:

- GSM450: 450.4-457.6MHz (UL), 460.4-467.6MHz (DL);
- GSM 480: 478.8-486MHz (UL), 488.8-496MHz (DL);
- GSM 850: 824-849MHz (UL), 869-894MHz (DL);
- Extended-GSM 900: 880- 915MHz (UL), 925- 960MHz (DL);
- DCS 1800: 1710-1785MHz (UL), 1805-1880MHz (DL);
- PCS 1900: 1850-1910MHz (UL), 1930-1990MHz (DL).

UL stands for Up-Link, when the User Equipment (UE) is emitting to the Base Station (BS) that is receiving. DL stands for Down-Link, when the UE is receiving what has been emitted by the BS.

The GSM standard is mainly a European one and some other countries of the world have developed their own standards too. That is the case of North America who adopted the mobile phone standard Integrated Dispatch Enhanced Network (iDEN) in 1994, followed by Korea, China and South America. It uses the 800MHz, the 900MHz and the 1.5GHz frequency bands and provides 64kb/s.

For the next generation of mobile phone standards (3rd one in Europe), quite every country of the world have changed the modulation, henceforth using the Code Division Multiple Access (CDMA) rather than previous Time Division Multiple Access (TDMA). First of all, in 1995, the CDMA-One (or TIA/EIA) appeared in North America and Korea that could provide up to 115kb/s. The CDMA-2000 increased the data rate of CDMA-One to 307.2kb/s and was adopted in 2001 by Japan also. The same countries adopted the 1xEV-DO and 1xEV-DV (except Japan) in 2002 and 2003 that provide data rates up to 2.5Mb/s and up to 3.1Mb/s respectively. Several frequency bands are used by those standards.

In 1999, Korea, Japan and USA joined Europe and some other Asian countries to adopt the Wideband-CDMA (W-CDMA) often called Universal Mobile Telecommunication System (UMTS), but commercial products became available only in 2004 in France when the licenses were attributed to operators. This standard operates in the frequency bands DCS 1800, PCS 1900 and IMT-2000 (1920-1980MHz (UL) and 2110-2170MHz (DL)) and can provide data rates up to 2Mb/s.

For downloading data, mobile phone standards were completed in 2004 by the High Speed Downlink Packet Access (HSDPA) standard which works in DL bands of mobile phone standards. Adopted in Japan, Europe, United States and Korea, this data link can provide data rates up to 10.8Mb/s.

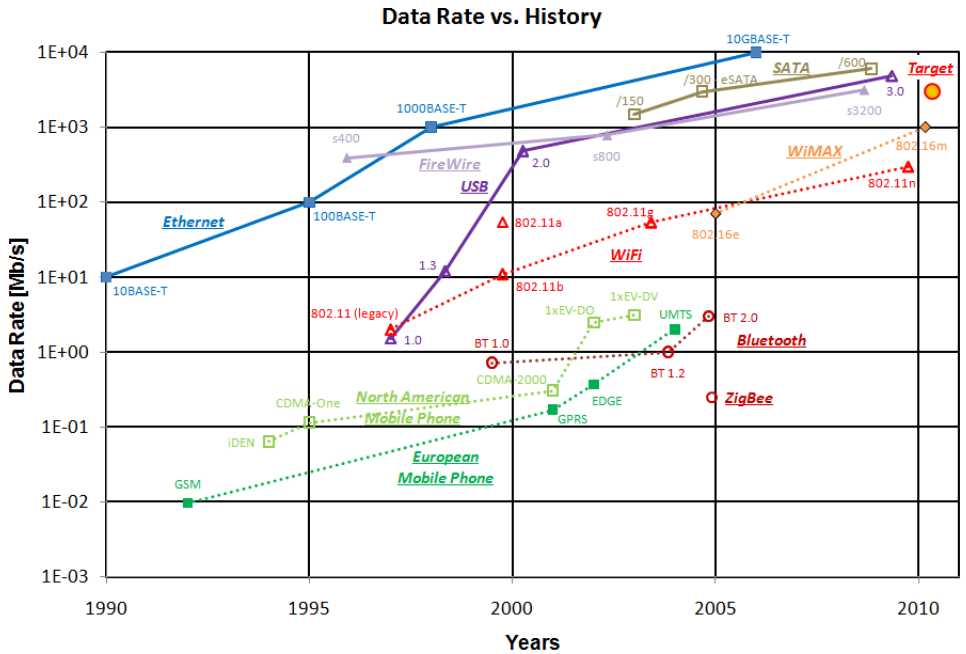
A.3. Discussion

Several standards exist for transferring data – audio and video transfer standards are quite different especially in the way of calculating the data rates. Table A-1 summaries the main wired, WPAN, WLAN, WMAN and mobile phone standards that were previously detailed. This table matches standard names to their corresponding IEEE task group, the publication year and the maximum provided data rate.

	IEEE Task Group	Name	Year	Speed [Mb/s]
Wired	802.3e	Ethernet 1BASE-T	1987	1
	802.3i	Ethernet 10BASE-T	1990	10
	802.3u	Ethernet 100BASE-T	1995	100
	802.3ab	Ethernet 1000BASE-T	1998	1,000
	802.3an	Ethernet 10GBASE-T	2006	10,000
	-	USB 1.0	1997	2
	-	USB 1.3	1998	12
	-	USB 2.0	2000	480
	-	USB 3.0	2009	4,800
	1394a	FireWire s400	1995	393
	1394b	FireWire s800	2002	786
	1394b	FireWire s3200	2008	3,144
	-	SATA/150	2003	1,500
	-	SATA/300 - eSATA	2004	3,000
	-	SATA/600	2008	6,000
Mobile Phone	Europe			
	-	GSM	1992	0.0096
	-	GPRS	2001	0.17
	-	EDGE	2002	0.37
	-	UMTS	2004	2

	IEEE Task Group	Name	Year	Speed [Mb/s]
WLAN	802.11a	WiFi-a	1999	54
	802.11b	WiFi-b	1999	11
	802.11g	WiFi-g	2003	54
	802.11n	WiFi-n	2009	300
WPAN	802.15.1	Bluetooth 1.0	1999	0.72
	802.15.1	Bluetooth 1.2	2003	1
	-	Bluetooth 2.0	2004	3
	802.15.3		2003	54
	802.15.3a	UWB	####	1,320
	802.15.3c	mm-W	2010	3,000
	802.15.4	ZigBee	2004	0.25
WMAN	802.16e	WiMAX-e	2005	70
	802.16m	WiMAX-m	2010	1,000
	802.20	Mobile-Fi	2008	1
Mobile Phone	North America / Korea / Japan			
	-	iDEN	1994	0.064
	-	CDMA-One	1995	0.115
	-	CDMA-2000	2001	0.307
	-	1xEV-DO	2002	2.5
	-	1xEV-DV	2003	3.1

Table A-1 Main data transfer standards



Wired connection standards: continuous line; WPAN: dotted line, circles, WLAN: dotted line, triangles; WMAN: dotted line, lozenges; Mobile phone: dotted line, squares

Figure A-1 Data rate versus history for main wired and wireless standards used for data transfer

Figure A-1 shows a graphical overview of Table A-1 data focusing on the data rates versus history. Wired standards are plotted with continuous lines whereas wireless ones are plotted with

dotted lines. Wireless standard types are differenced with the markers shape: circles are for WPAN, triangles for WLAN, lozenges for WMAN and squares for mobile phone.

First of all, this figure highlights the perpetual increase of data rates for each standard, wired or not. This evolution is linear as the data rate is given by the commercial / consumer need. We could hence predict the data rate of future standards versions. Moreover, lines formed by the different versions of each standard tend to become parallel and seem to be limited by the technology of the physical links and devices.

Second point that seems obvious in Figure A-1 is that wireless standards provide lower data rates than wired standards. Everybody can understand that it is much easier to build an efficient link using a wire than using two transponders to transform electrical signals into electromagnetic waves. However this is the key aspect that could make a Multi Gigabit Wireless System (MGWS) become a mass market product. By challenging classical wired connections with an equivalent wireless link that is easier to set up for the users and that can provide quite the same data rate and the mobility given by the absence of wire, the success of a MGWS should be guaranteed.

Considering now wireless standards only, we can notice that the provided data rate varies of several decades between the different standards. At the same date in 2005, ZigBee currently allows one decade lower data rate than Bluetooth (V2.0) and mobile phone (UMTS – 1xEV-DV) which provide themselves more than one decade lower data rate than WiFi (802.11g) of WiMAX (802.16e). Those differences mainly depend on the modulation, but also on some other parameters, like the emitted power, the technology, and the complexity of the devices… Some telecommunication standards are designed to be used in mobiles terminals like smart-phones where the battery lifetime is critical. So, the emitted power is reduced, that results in a low range or a low data rate. The cost of devices is often critical for products that use Bluetooth or ZigBee. Low prices reduce drastically the complexity of the systems, resulting in lower data rates too. Some products simply do not need a high data rate. That is the reason why so many wireless communication standards currently co-exist: the needs are not identical for all applications. If some applications need high data rates, others would need low power consumption, low complexity or low cost. And one or another standard will be used to match the requirements of the application. However, there is currently no very high data rate wireless standard that could compete with wired links. That is why a MGWS is planned.

Finally, for a constant baseband modulation, the data rate is proportional to the bandwidth. Mobile phone standards well illustrate this principle. GSM channels are concentrated on a 200kHz bandwidth and the resulting data rate is 10kb/s; whereas UMTS channels stretch over 5MHz and the resulting data rate is 2Mb/s. And all presented wireless standards work in the frequency bands below 6GHz; therefore, they provide quite low data rates, bellow 300Mb/s (for WiFi-n). Building a high data rate system of several Gb/s requires the use of a large frequency bandwidth of several GHz that is not available in those low frequency bands. That was the starting idea of the task group 3a for building a PHY alternative of IEEE 802.15.3-2003 by using Ultra-Wide-Band between 3.1 and 10.6GHz. Thus it should provide a data rate of 1.32Gb/s what is 4 times higher than other existing wireless standards. But unfortunately it has not been completed. Anyway, the targeted frequency band (from 3.1 to 10.6GHz) was not totally free which would have resulted in many interferences with other wireless systems if no detection and avoidance mechanism were integrated.

For those reasons, it has been decided to get interest in the millimeter-Wave (mmW) frequencies between 57 and 64GHz to design a new MGWS.

References

[1] Wikipedia, The free encyclopedia. [Online]. http://en.wikipedia.org

[2] A. Sadri, "802.15.3c Usage model document (UMD), Draft," Project IEEE P802.15 15-06-0055-15-003c, Jan. 2007. [Online]. http://www.ieee802.org/15/pub

Annex B. mmW transmitters

Overview

An RF transmitter is a complex circuit, which integrates at least a baseband signal generator, a power amplifier and an antenna, following the scheme of Figure B-1. A mixer, a VCO and several filters can also be added to this simple architecture. It results that building a transmitter at higher frequencies drastically increases the complexity in terms of design as all the blocks have to provide good performances at the targeted frequency.

Building a transmitter working at mmW frequencies is hence a challenge for the different research teams all over the world. Some institutions or companies have currently reached this objective and have published their work. This annex aims to be a state-of-the-art of transmitters working in the mmW frequency band.

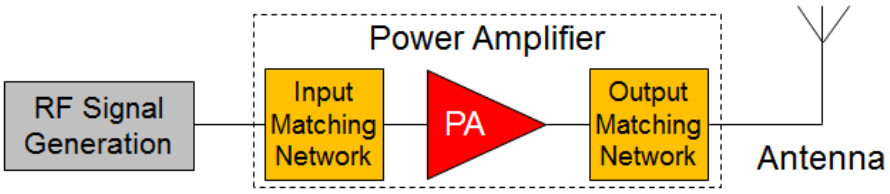


Figure B-1 General synoptic of an RF transmitter

Outline

B.1. From III-V technologies…

mmW frequencies have long time been reserved to aerospace and military applications such as satellite communications or radar applications. Those frequencies are actually difficult to generate and to test. Military and spatial organizations were the only one that could afford the high research & development and financial costs. Military and spatial industries have radically opposite needs in comparison to mass market: the production is really limited (rarely more than some tens or thousands of pieces) and the cost of the final product is not necessarily prohibitive. So III-V technologies are well suited as they provide high performance with a relatively low cost for limited editions. Thus III-V technologies were used in the past 30 years for mmW applications. In addition, transmitters were mostly implemented through a discrete vision with separate components in III-V technologies such as GaAs, waveguides elements and horn antennas. Figure B-2 shows one of them [**1**].

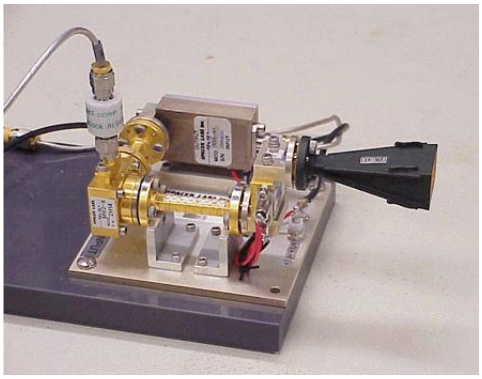
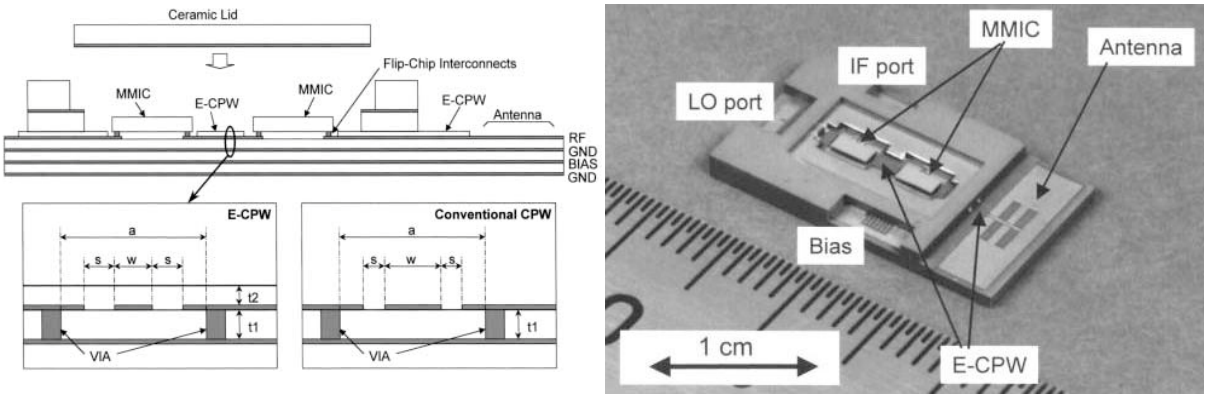


Figure B-2 A GaAs mmW transmitter: integration limitation

But commercial applications such as automotive radars or WLAN-WPAN communication systems are now targeted to work at millimeter-Wave frequencies. Such mass-market products need to be fully integrated – including the antenna – to reduce the cost and the size to be easily implemented in mobile devices. So, the way of building a transmitter has to be changed. Several solutions can be considered to solve this problem: Chip-on-Board (CoB), System-in-Package (SiP), or System-on-Chip (SoC).

Since mass-market applications are in discussion at millimeter-waves (in the 2000's), compact solutions were considered even by III-V manufacturers. It's the case in particular of NEC which designed an InGaAs/AlGaAs MMIC transmitter with double slot antenna integrated on 5-layers LTCC using cavity and cover [**2**]. Interconnections between chips are realized by Embedded Coplanar Waveguide (E-CPW) and flip-chip techniques as illustrated in Figure B-3.a. The fully integrated transmitter shown in Figure B-3.b is 18x8.6x1.28mm^3 large. The output power at 1dB compression point reaches 10dBm and the antenna provides an additional 4.1dBi gain. NEC has also realized a receiver with similar process and physical characteristics.



a. **b.**

Figure B-3 InGaAs/AlGaAs MMIC TX/RX with double slot antenna on 5-layers LTCC

Some other similar 60GHz integrated transmitters were realized in III-V technologies during the past 10 years. However mass-market products are not economically imaginable in III-V technology. The cost of III-V technology is actually directly proportional to the number of produced pieces whereas in silicon technologies, there is a high cost for pre-production steps (mask generation) and the cost of each chip is then very low. So, mass-market products (more than 100 000 units) are generally made in silicon.

B.2. … to SiGe technologies…

Since its formulation in 1965, Moore's law [**3**] has always been respected. So much that it has become a target for engineers and researchers working on silicon integrated circuits to respect Moore's predictions: the number of transistors used in processors is doubled every 24 months. To reach this objective, the International Technology Roadmap for Semiconductors (ITRS) [**4**] recommends three dimensions (3D) scaling for active components like transistors, and for interconnections too. However silicon technology nodes are commonly referred by their minimum transistor gate length. As an example, at the end of 2009, the node 65nm is quite an old CMOS process as the node 45nm is replacing it in production. And semiconductor manufacturers are currently adapting experimental process of nodes 32nm and 22nm to large scale production.

This recurrent scaling results in an increase of digital circuit performances. But this is not true for analog and RF components. As f_t and f_{max} technology parameters increases, the speed increases too, enabling the use of the elementary active component at higher frequencies. But the maximum generated power is lowered as transistors are smaller. The 3D scaling of interconnections generates more losses in passive devices too.

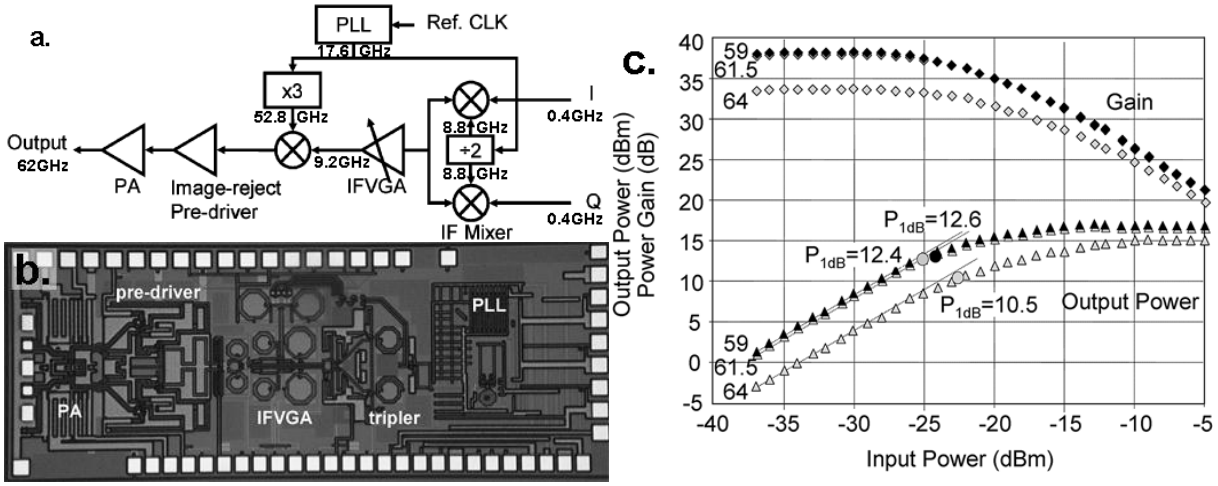
However, although those extreme technologies are not the most suitable for analog operations, they provide several considerable advantages. First of all, the cost of silicon devices is quite low which is crucial for mass market commercial applications. This has already been discussed previously in the comparison with III-V technologies.

Another advantage of silicon technologies is the co-integration of digital blocks with analog and RF ones. The resulting chip is smaller. This also minimizes the loss due to the blocks interconnections. Ideally, we should be able to integrate a full transceiver with the digital signal processor, the analog/RF frontend (up-converter, amplifier and filter) and the antenna into a single chip.

Two silicon technologies are widely used in production: the well-known CMOS and the Silicon-Germanium BiCMOS (SiGe). Considering the same technology node, SiGe provides better performances than CMOS technology with notably higher output power and better performances in terms of cutoff and maximum frequencies. However the technology nodes are not developed simultaneously in SiGe and in CMOS and when the ultimate SiGe technology is 0.12µm, CMOS technologies are produced in 65nm. Thus considering this technology node difference, SiGe and CMOS technologies will advantage the RF or the digital components respectively. Choosing between SiGe or CMOS technologies for a fully integrated transmitter that comprises both the RF chain and the baseband digital signal processor will hence be a trade-off between the cost of the global chip and the performances of both digital and RF parts of the chip. However, considering only the RF performances, SiGe technologies are often investigated before CMOS ones as it has occurred for 60GHz applications.

In August 2005, IBM published a first transmitter integrated on 0.13µm SiGe BiCMOS technology [**5**]. This transmitter chip is based on super-heterodyne architecture as illustrated in Figure B-4.a. PLL, frequency multiplier and divider, IF mixer, IFVGA and RF mixer are parts of the RF signal generator depicted on section I.2.1.i. A pre-driver is then used to increase the power level at the input of the PA. The die – shown in Figure B-4.b – is 4x1.3 mm² large.

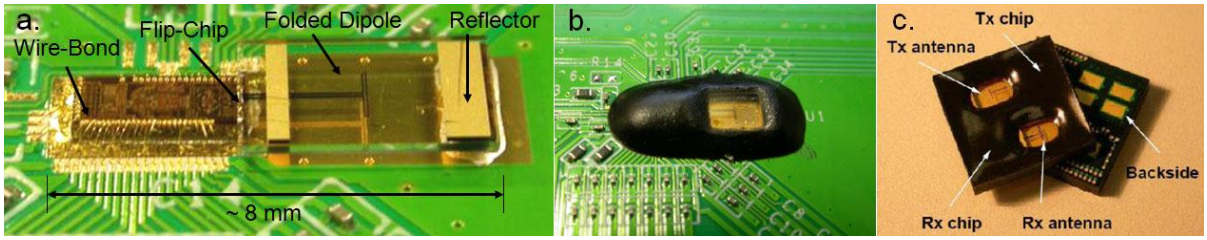
Figure B-4.c shows the measurements results of this transmitter. The output power reaches 10-12dBm at the 1-dB compression point and 15-17dBm at the PA saturation. The conversion gain of the RF chain is higher than 34dB on the entire 59-64GHz frequency band. The spurious responses are also quite good with, at the 1-dB compression point, an image rejection between 20 and 30dB, a carrier suppression between 21 and 25dB and 20 to 25dB of sideband suppression. The chip dissipates 800mW power.



a. Architecture | b. Die photograph **c. Measurements results**

Figure B-4 SiGe integrated transmitter designed by IBM

This chip is coupled with an antenna to form the 1st silicon fully integrated transmitter chipset working at 60GHz. The TX chip is wire-bonded on an FR-4 circuit board. The antenna is a folded dipole on silica with back cavity, metallic frame and reflectors. Antenna gain is approximately 7 dBi with a beam-width of 30°, a 20GHz bandwidth (at -10dB of S_{11}), and a 90% efficiency. The interconnection with the transmitter SiGe chip uses flip-chip techniques [**1**]. Finally, the chip-on-board packaging is realized by plastic molding Direct Chip Attach (DCA) with a window to keep good antenna efficiency as shown in Figure B-5 a. and b.. The resulting chipset size is 11x7mm². Figure B-5.c shows another packaging approach: Plastic molded Land Grid Array (LDA). The transmitter and the receiver are integrated into a single package to build a full transceiver [**6**]. IBM has also studied some other packaging techniques for such mmW modules [**7**].



a. & b. Chip-on-board / Plastic molded Direct Chip Attach (DCA) **c. Land Grid Array (LDA)**

Figure B-5 Packaging aspects of 1st IBM 60GHz transmitter chipset

A second generation of this transmitter has been realized by IBM in 2007 [**8**]. It integrates some additional modules as an RMS detector and a base-band modulator which are highlight in gray in Figure B-6. The measurement results are very similar to those of the 1st chipset except that a complete TX-RX demonstrator has been realized and has established a 2Gb/s link without any Analog-to-Digital conversion. The 1st demonstrator established only a 640Mb/s link with ADC. The frequency band has also been enhanced to 57-64GHz.

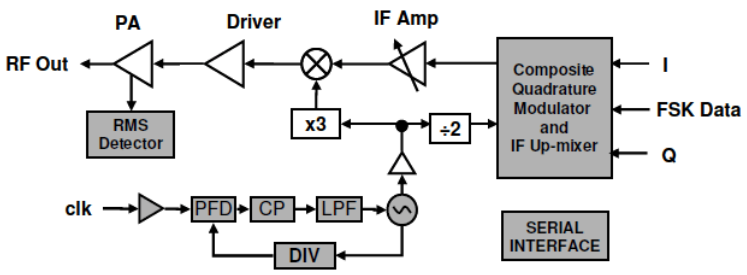
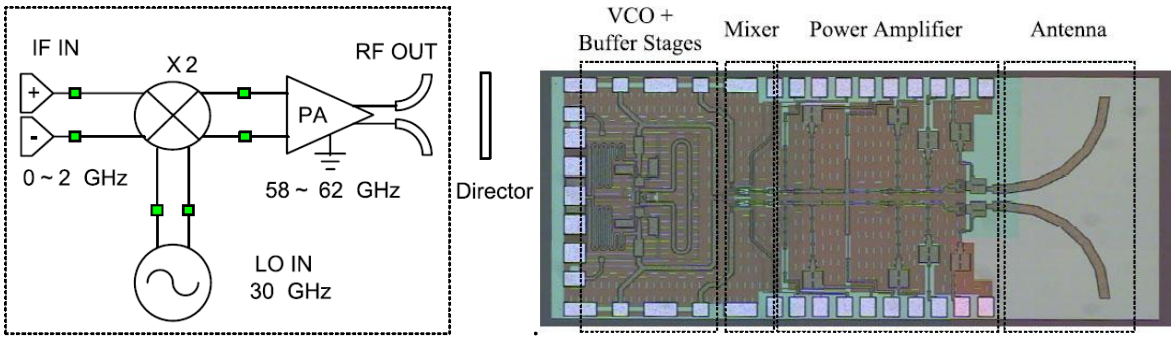


Figure B-6 Block diagram of IBM Gen-2 transmitter

In February 2006, the National Taiwan University, the Chung-Shan Institute of Science and Technology and TSMC published in [**9**] their works on a 60GHz transmitter IC with integrated antenna in a standard-bulk 0.18µm SiGe BiCMOS technology. The circuit integrates a balanced mixer with built-in cross-coupled VCO and two buffer stages, 2 single-ended three-stage class-A amplifiers working in balanced mode, and a differential tapered slot antenna following the architecture of Figure B-7.a. The chip – shown in Figure B-7.b – has a 1.3x0.8mm² die size.

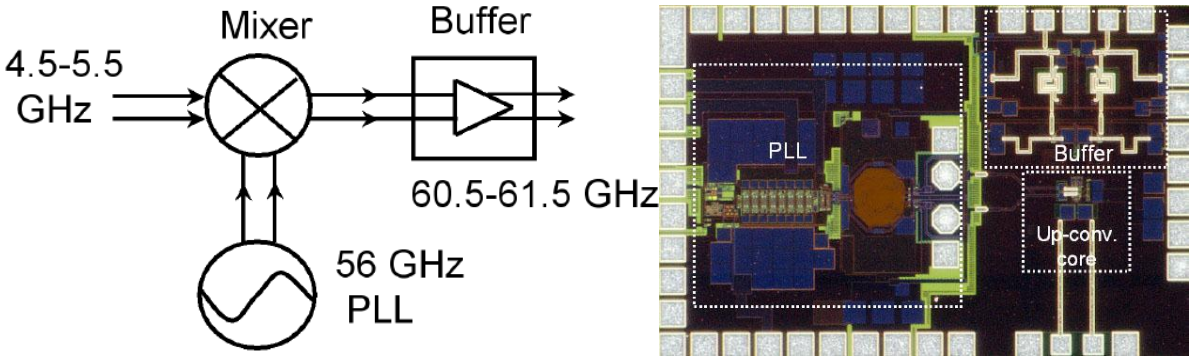


a. Block diagram **b. Die photograph**

Figure B-7 NTU and TSMC SiGe transmitter

For integration matter, the antenna is very small – the strip length is designed for slightly longer than λ/4 at 60GHz – resulting in degradation of gain and directivity (-15dBi). However, the antenna gain can be increased to -2dBi by placing an off-chip director at λ/2 away from the end of the antenna. The conversion gain of the antenna is estimated to be 20.2dB. The balanced PA has a 15.8dBm saturated output power, an 11.5dB small signal gain while consuming only 281mW from power supply.

The Wireless World Research forum has also proposed a 60GHz transmitter and receiver in April 2006 [**10**]. The transmitter chip includes a Gilbert cell up-converter, a two-stage buffer and a 56GHz PLL following the architecture of Figure B-8.a. This chip is designed in 0.25µm SiGe BiCMOS technology. The die – shown in Figure B-8.b – is mounted onto a Printed Circuit Board (PCB) and wire bonded. An external GaAs PA is added to provide sufficient power as the designed chip shows a 5dBm output 1dB compression point (see section I.2.2.i for more details on this PA). An 8dBi gain Vivaldi antenna is integrated onto the board. The input signal is fixed at a 5GHz intermediate frequency (IF) in order to use an 802.11a circuit as a baseband signal generator. A very clear constellation has been measured using a 250Mb/s QPSK input signal transmitted through this 60GHz link with a 1m distance between the transmitter and the receiver.



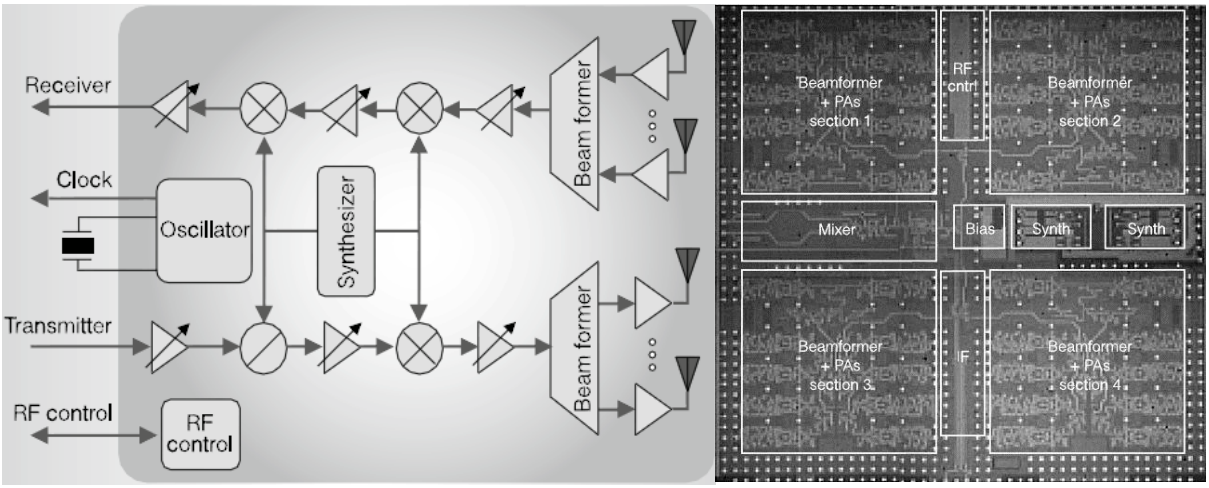
a. Block diagram **b. Die photograph**

Figure B-8 Wireless World Research forum SiGe transmitter

B.3. … and CMOS technology

The SiGe BiCMOS technology highly reduces the cost of mmW transmitters with respect to III-V technologies. However SiGe is only an intermediate research step in order to reach very low cost products in CMOS technologies.

SiBEAM was the first company to resolve the many challenges of producing an all-CMOS fully integrated 60GHz chipset for WirelessHD system in January 2008 [**11**] [**12**]. This complete chipset includes 2 components: a Digital Base-Band (BB) MAC chip which contains Analog-to-Digital (AD) and Digital-to-Analog (DA) converters, digital PHY and MAC, audio and video interface unit and embedding CPU; and an RF chip which is particularly interesting. The architecture of this RF chip, shown in Figure B-9.a, includes the 60GHz low-noise amplifiers (LNAs), 60GHz power amplifiers (PAs), mixers, and intermediate-frequency (IF) and baseband amplifiers, thus resulting in a complete 60GHz transmitter and receiver.



a. Block diagram **b. Die photograph**

Figure B-9 SiBEAM CMOS RF chip for WirelessHD

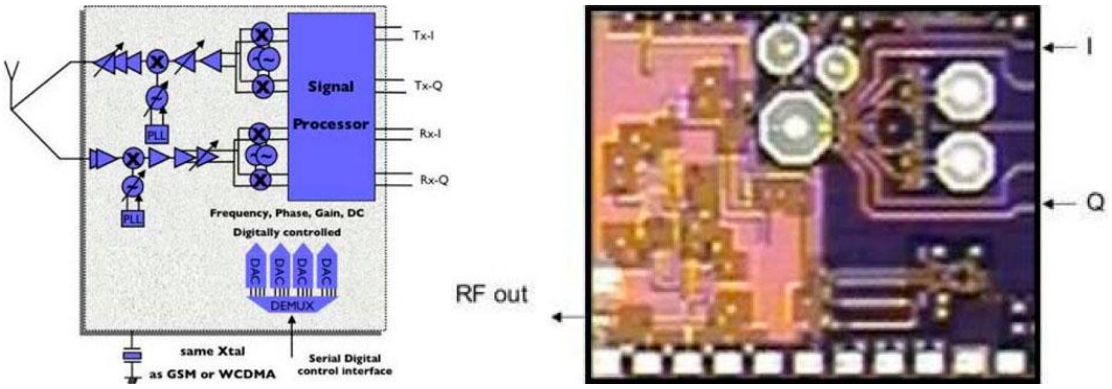
Several independent antennas and RF chains – more than 10 – are used to form an agile focused beam. Omni-directional mode allows broadcast operation for device discovery and coordination. Then the beam can be electronically focused on the desired direction to establish a high data rate link by LOS or NLOS path. Environment can be searched and optimal beam found in millisecond time scales thus providing a high Quality-of-Service (QoS). This RF transceiver circuit is integrated in a ceramic package measuring about 20mm². Figure B-9.b shows a die photograph of the chip, which is fabricated in a standard 90nm digital CMOS process.

The chipset designed by SiBEAM achieves full 10m NLOS coverage at a 4Gb/s data rate. The resulting WirelessHD link – including 2 chipsets, one per equipment – should cost between 80$ and 100$, which was similar to an HDMI wired connection in year 2008. This solution is very promising for WirelessHD to be implemented soon in mass-market equipment.

The Georgia Institute of Technology has also presented a CMOS 60GHz radio solution in 2008 [**13**]. Both transmitter and receiver front ends have been designed in a 90nm CMOS process and have been implemented in a single chip solution with the addition of a high-speed digital signal processor for analog-to-digital conversion and high speed PHY signal processing to support both advanced OFDM and single carrier modulation scheme as shown in Figure B-10.a.

The single-chip solution enables data throughputs exceeding 7Gbps with a QPSK OFDM modulated digital signal while consuming less than 200mW supply power. However the condition of operation to obtain this result – in terms of distance between the emitter and the receiver notably – is not detailed in the publication. Well-informed readers would so keep a critical eye on this 7Gbps 60GHz link.

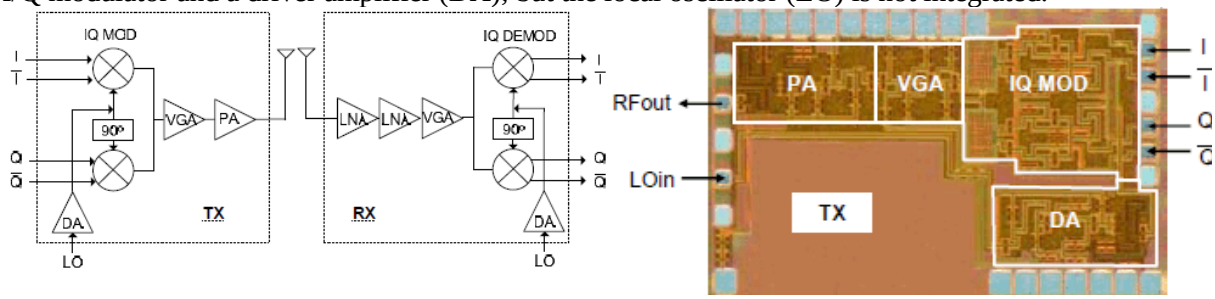
Figure B-10.b shows the die photograph – 1.75x1.5mm² – of the single-chip transmitter including a double-balanced quadrature Gilbert-cell mixer, a quadrature VCO, a common-source digitally controlled VGA, a mmW resistive up-conversion mixer.



a. Transceiver block diagram **b. Transmitter chip die photograh**

Figure B-10 Georgia Institute of Technology CMOS 60GHz solution

NEC has presented another CMOS implementation for 60GHz band also in 2008 [**14**]. Both TX and RX front-ends have been designed in a 90nm standard bulk CMOS process. Figure B-11.a shows the block diagram of the TX and the RX modules. The direct-conversion configuration is adopted for chip miniaturization and wider bandwidth operation. The transmitter is composed of a PA; a VGA, an I/Q modulator and a driver amplifier (DA); but the local oscillator (LO) is not integrated.



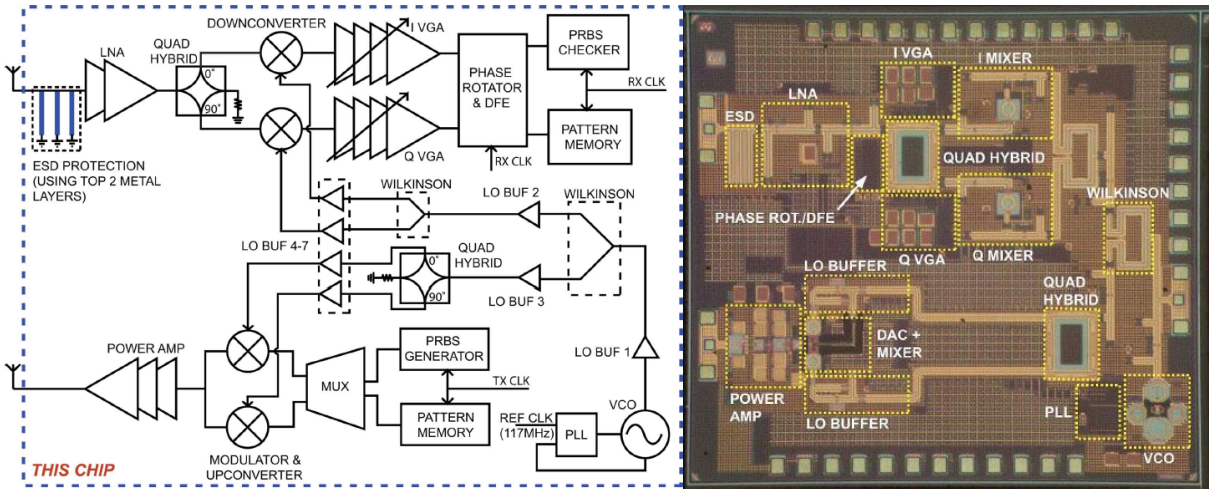
a. Transceiver block diagram **b. Transmitter chip die photograph**

Figure B-11 NEC CMOS 60GHz solution

Figure B-11.b shows the die photograph of the transmitter module which occupies 1.5mm² including the pads. Working under 0.7V supply voltage, the transmitter provides low power consumption (133mW) which results from the simplicity of the direct conversion technique used here and the non-integration of any signal carrier or clock generation. Furthermore, the output RF power is limited to 6dBm which is very far from the Wireless-HDMI specification (see section I.1.3). However during the measurements performed with a waveguide connection between the transmitter and the receiver a high 2.6Gbps data rate link has been established using QPSK modulation.

The University of California at Berkeley has also presented a 90nm CMOS transceiver [**15**] that uses the entire 60GHz band as a single channel (not based on a particular standard). The transmitter design includes a digital baseband pattern generator, an integrated digital-to-analog (DAC) / mixer structure, a power amplifier, and an on-chip voltage-controlled oscillator (VCO) and PLL, as can be seen in Figure B-12.a. Due to some measurement constraints, the I and Q channels could not be measured simultaneously. However, the transmitter achieves 5Gb/s data rate on the I-channel. Thus, with the same data rate being transmitted on the Q-channel, this would be equivalent to 10Gb/s QPSK transmission. The receiver design consists of an ESD protected two-stage cascode LNA, quadrature hybrid I/Q downconversion mixers, and a four-stage variable-gain amplifier (VGA). The receiver shares the VCO and PLL with the transmitter, as can be seen in Figure B-12.a.

Figure B-12.b shows the die photograph of the full transceiver that occupies 2.5x2.75mm². The transceiver consumes 170mW while transmitting 10dBm and 138mW while receiving, both being measured under a 1.2V supply voltage. The highest data rates achieved in measurements are 7Gb/s in loop-back mode (the PA output being directly connected to the LAN input of the same transceiver chip), 6Gb/s over a wired channel (a 3m 1.85mm coaxial cable was connected between the PA of one transceiver used as transmitter and the LNA of another transceiver used as receiver), and 4Gb/s over a wireless channel (the coaxial cable was replaced by a 1m wireless link between two 25dBi horn antennas).



a. Block diagram **b. Die photograph**

Figure B-12 CMOS 60GHz transceiver designed by the University of California at Berkeley

References

[1] B. Gaucher, "Completely integrated 60 ghz ism band chip set and test results," Project IEEE P802.15 15-06-0003-00-003c, Jan. 2006. [Online]. http://www.ieee802.org/15/pub/

[2] K. Maruhashi, et al., "Low-Cost 60GHz-Band Antenna-Integrated Transmitter_Receiver Modules Utilizing Multi-Layer Low-Temperature Co-Fired Caramic Technology," in *IEEE International Solid-State Circuits Conference (ISSCC 2000), Digest of Technical Papers*, vol. 19.4, San Francisco, CA, USA, 2000.

[3] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114-117, Apr. 1965.

[4] (2010, Feb.) Iternational Technology Roadmap for Semiconductors (ITRS). [Online]. http://www.itrs.net

[5] S. K. Reynolds, et al., "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2820-2831, Dec. 2006.

[6] B. A. Floyd, et al., "Silicon Millimeter-Wave Radio Circuits at 60-100 GHz," in *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Long Beach, CA, USA, 2007, pp. 213-218.

[7] S. K. Reynolds, et al., "Progress Toward a Low-Cost Millimeter-Wave Silicon Radio," in *IEEE Proceedings of the Custom Integrated Circuits Conference (CICC)*, San Jose, CA, USA, 2005, pp. 563-570.

[8] S. Reynolds, et al., "Second Generation 60-GHz Transceiver Chipset Supporting Multiple Modulations at Gb/s data rates (Invited)," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM 2007)*, Boston, MA, USA, 2007, pp. 192-197.

[9] C. Wang, et al., "A 60 GHz Transmitter with Integrated Antenna in 0.18 um SiGe BiCMOS Technology," in *IEEE International Solid-State Circuits Conference (ISSCC 2006), Digest of Technical Papers*, vol. 10.4, San Francisco, CA, USA, 2006.

[10] Y. Sun, et al., "An integrated 60 GHz transceiver front-end for OFDM in SiGe: BiCMOS," in *16th meeting of the Wireless World Research Forum*, Shanghai, China, Apr. 2006. [Online]. http://www.ihp-microelectronics.com/173.0.html

[11] J. M. Gilbert, C. H. Doan, S. Emami, and C. B. Shung, "A 4-Gbps wireless uncompressed HD AV transceiver chipset," *IEEE Micro*, vol. 28, no. 2, pp. 56-64, Jan. 2008.

[12] J. M. Gilbert, D. H. Doan, S. Emami, and S. B. Shung, "A 4 Gbps wireless true uncompressed 1080p-capable HD AV transceiver using 60 GHz," SiBEAM White paper, 2007. [Online]. http://www.sibeam.com

[13] S. Pinel, et al., "A 90nm CMOS 60GHz Radio," in *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, vol. 6.8, San Francisco, CA, USA, 2008.

[14] M. Tanomura, et al., "TX and RX Front-Ends for 60GHz Band in 90nm Standard Bulk CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, vol. 31.1, San Francisco, CA, USA, Feb. 2008.

[15] C. Marcu, et al., "A 90nm CMOS Low-Power 60GHz Transceiver with Integrated Baseband Circuitry," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3434-3447, Dec. 2009.

Annex C. Overview on power amplifier

Overview

The Power Amplifier, or PA, is a critical block in a transmitter chain as it is often the last one before the antenna. As a consequence it has to deal with the highest power level while being as linear as possible not to disturb the signal waveform induced by the modulation scheme.

This annex aims to give some general information on this peculiar RF block. The different key parameters to characterize a power amplifier are hence defined here.

This annex also investigates the different PA topologies and the power combining techniques, which are widely used at mmW frequencies to increase the level of output power and overcome the technology limitations.

A state-of-the-art of mmW PA can be found in section I.2.2.i, which can be more easily understood after having read this annex.

Outline

C.1. Overview on PA characteristics

Being an RF block, a power amplifier can be seen as a black box that transforms an RF input signal into an RF output signal using a DC supply, as schematized in Figure C-1. The relation between the input and the output signals is characterized considering first the small signal condition and then considering the large signal condition.

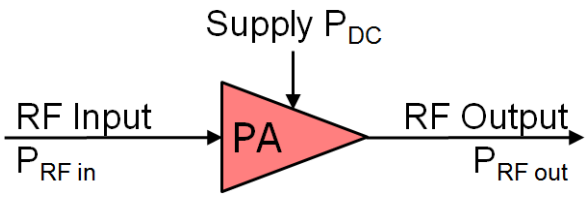


Figure C-1 Power definitions of Power Amplifier

In small signal condition, the behavior of nonlinear devices can be approximated with linear equation. This linearization is accurate only for small excursions about the DC bias point of the device. Considering small signal condition, PAs are characterized as any other RF block by the scattering parameters (S-parameters). With one input and one output, PAs are two-port networks. The S_{11} and S_{22} parameters hence define respectively the input and output reflection coefficients – also called matching parameters – while the S_{12} and S_{21} parameters correspond respectively to the wave propagation from the output to the input and from the input to the output – also called isolation and transmission parameters.

The S-parameters are defined in the frequency domain and for small signal, and hence characterize the capability of the network to reflect or transmit a signal at a given frequency. The bandwidth is defined for small signal S-parameters as the frequency band in which the PA can provide a gain at least -3dB to its maximum gain which is obtained at the frequency called center frequency.

The S-parameters can be converted into Z-parameters (see Annex D for details) and expressed in terms of input and output impedance Z_{in} and Z_{out}. Hence the PA can be decomposed in three different blocks as shown in Figure I-9 (in section I.2.1), the active part and a matching network at both input and output that tune the input and output impedances to the desired value in order to maximize the power transfer with the other blocks of the RF chain.

However, the S-parameters are not sufficient to characterize a PA and the nonlinear effects have to be taken into consideration too. A PA is actually characterized by the large signal gain which is defined as the ratio between the output power and the input power as written in the relation (C.1).

$$Gain = \frac{P_{RFout}}{P_{RFin}} \tag{C.1}$$

The large signal gain is generally given at the center frequency of the PA where the small signal gain is maximal – i.e. where the S_{21} parameter is the highest. The gain is calculated with respect to the input power and progressively decreases when the input power increases as the PA becomes nonlinear. The maximum gain is hence obtained at low input power which corresponds to the small signal condition. As a consequence, the maximum gain should be equal to the S_{21} parameter at the center frequency of the PA.

PAs are not fully linear blocks and, in practice, the RF output power P_{RFout} cannot go beyond a certain level called saturated output power and noted P_{sat}, even if the RF input power P_{RFin} is increased. However at the saturated output power, the PA is highly non-linear and using a PA in its saturation region would generate many unwanted harmonics resulting in a huge useless power consumption that means a very low efficiency.

Considering only a single carrier signal will hence generate components at integer multiples – 2, 3, 4 … times – of the input signal frequency that can be easily filtered. But considering now a modulated signal, the harmonics interfere and generate some frequency components very closed or in

the wanted frequency band and cannot hence be filtered. In order to characterize those effects a two tones signal is applied at the PA input and the power of the 3rd order harmonics is measured with respect to the wanted power (1st order or linear components) to determine the 3rd order Intercept Point noted *IP3* [**1**]. This point can be defined at the input of the PA *IIP3* or at the output *OIP3*, both *IIP3* and *OIP3* being separated simply by the PA gain at the given power level.

In order to characterize the output power of the PA when still working in its linear region, the 1dB compression output power, noted P_{-1dB} or OCP1, has been defined as the output power when the gain of the PA is just 1dB below its maximum. This 1dB compression output power is a very good parameter to characterize a PA when working with modulated signals such as OFDM while the saturated power is more significant when working with single carrier signals.

PAs often consume a huge DC power P_{DC} with respect to the other blocks of an RF transmitter chain and their efficiency is hence a critical characteristic. However the notion of PA efficiency can be expressed in several ways. First, the total efficiency is defined as the ratio between the RF output P_{RFout} power and the total input power that means the RF input power P_{RFin} and the supply power P_{DC} as defined in the relation (C.2).

$$Total\ Efficiency = \frac{P_{RFout}}{P_{DC} + P_{RFin}} \tag{C.2}$$

The Power Added Efficiency *PAE* is defined as the ratio of the power added by the PA on the RF path that means the RF output power P_{RFout} minus the RF input power P_{RFin}, with respect to the supply power P_{DC} following the equation (C.3).

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \tag{C.3}$$

A third method to characterize the efficiency of a PA consists of focusing on the efficiency of the last power transistor. The drain efficiency is hence often used by designers and is defined as the ratio between the RF output power P_{RFout} and the supply power P_{DC} following the relation (C.4).

$$Drain\ Efficiency = \frac{P_{RFout}}{P_{DC}} \tag{C.4}$$

The easiest way to characterize the efficiency of a PA at the system level is to consider the power added efficiency *PAE* rather than the total efficiency or the drain efficiency, as it gives an idea of the power that is added to the RF signal by the PA while also considering the supply power which is consumed. The PAE can be calculated at each input power level resulting in a complete curve. This PAE curve always starts at zero when no signal is applied at the PA input no RF power is added by the PA while it is still consuming some DC supply power. This curve also presents a maximum which is often used as a comparison parameter. However this maximum does not necessarily correspond to the input power that generates the maximum output power the PA being in saturation – at P_{sat} – or the PA being still quite linear – P_{-1dB}.

PAs are generally characterized also by their working class [**1**]. Classes A, B, AB and C are linear working classes. D, E and F are switching classes. In fact, the non-linearity level increases with respect to the class letter. A class A amplifier should generate a quasi-pure sinusoidal signal, the harmonic level then increases progressively when considering class B and class C amplifiers. Class D, E and F amplifiers generate so many harmonics that the output signal becomes square which means digital. Those "digital" classes cannot be used for 60GHz applications as the OFDM modulation requires a highly linear power amplifier.

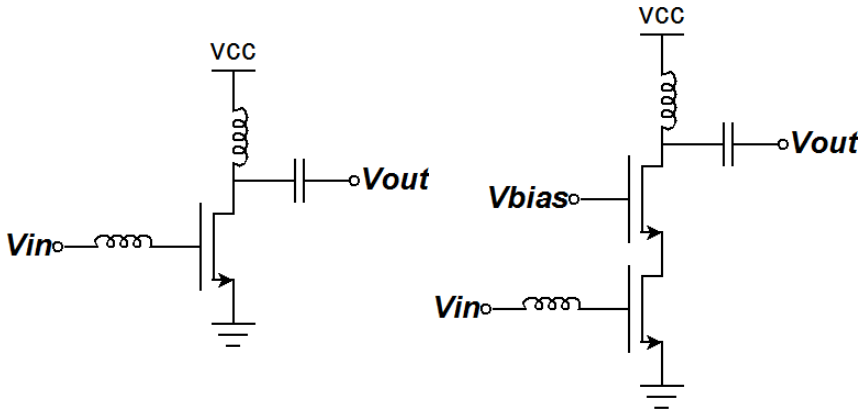
Analog classes are defined as a function of the conduction angle of the PA, which corresponds to the portion of the input signal cycle during which the amplifying device conducts (expressed as an angle in degrees or radians). For Class A amplifiers, the conduction angle is equal to 360° and 100% of the input signal is directly amplified. This is the most linear amplifier class. However this is also the

less efficient class as the power transistor is always biased with a constant current even if no RF signal is applied at the PA input. In order to increase the efficiency of a PA, the biasing current can be lowered. This results in a lower conduction angle, between 360° and 180°, which means that for a full scale input signal, a portion of the sinusoid will not be amplified by the PA. This corresponds to the Class AB. When the conduction angle reaches 180°, 50% of the sinusoid input signal only is amplified and the PA is in Class B. Class C stands for PAs which conduction angle is lower than 180°. Class C PAs present a good efficiency but present also a reduced linearity.

As introduced in section I.1.3.ii, the OFDM modulation induces a high Peak-to-Average Power Ratio (PAPR). This implies a high linearity constraint on the RF system. Hence the PA should be as linear as possible and millimeter-waves PAs should be in classes A or AB.

C.2. Overview on PA topologies

Considering CMOS PA cores, only two topologies are actually used and those two are the only ones which can provide enough linearity and output power at mmW frequencies: the common source, and the cascode. The general implementation of the two configurations are shown in Figure C-2 a and b with lumped components.



a. Common source **b. Cascode**

Figure C-2 General implementation of a common source (a.) and a cascode (b.) configuration

The cascode topology can handle higher supply voltage and hence a higher output voltage swing can be obtained which means higher power level. The cascode topology also presents higher gain, higher bandwidth and higher stability than common source topology but with lower power added efficiency and lower linearity.

Those two topologies are sometimes used in the same design. The cascode can be used for the driver stage when the power stage uses the common source topology [**2**]. The opposite configuration has also been implemented in [**3**] but in this case the amplifier was also distributed along a transmission line which is a specific method to increase the bandwidth.

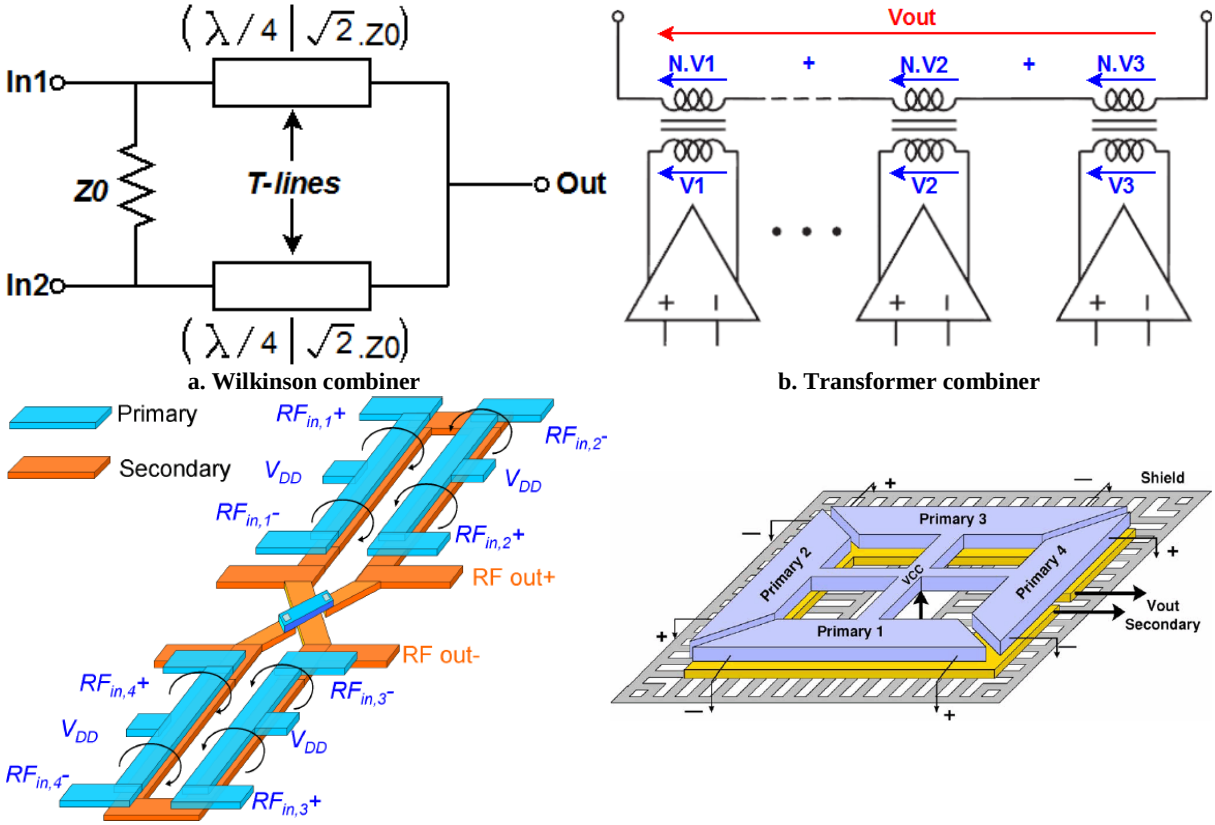
At millimeter Waves, the lumped components shown in Figure C-2 a and b can be replaced by transmission lines as the wavelength reaches the range of the circuit size. This represents quite a new approach for designers coming from lower frequencies from 900MHz to 5GHz (mobile phone, WiFi … applications). However this technique is often used in ultra-high frequencies by designers in III-V technologies since several tens of years [**4**]. A combination of both lumped components and transmission lines can be used simultaneously as in [**5**].

Moreover at mmW frequencies, every small metal access has a non-negligible effect on the global circuit as the size of those accesses becomes non negligible with respect to the wavelength. Those accesses working as transmission lines have to be taken into consideration by performing electromagnetic simulations [**6**]. On the other hand, the metal accesses to the active devices can be advantageously used to perform the required impedance matching function, thus reducing considerably the needs of additional transmission lines.

C.3. Power combining techniques

Increasing the output voltage or current are the two ways to raise the maximum output power of a PA. However, the voltage can only be increased in given limits, otherwise it would result in a degradation of the PA lifetime (see section I.3.3.iii) or even its destruction. On the other hand, the only solution to increase the current flowing through power transistors is to increase the width of those transistors. And the PA's maximum available gain decreases at 60GHz when the transistor width exceeds one or two hundred microns [**6**]. So the current can also only be increased in given limits.

Neither the current nor the voltage can actually be increased on the power stage. Power-combining techniques can overcome such limitations by increasing the voltage or the current in passive components which are less limited than MOS transistors. The PA hence becomes a combination of several PA units connected together by a power splitter (or divider) at the input and by a power combiner at the output. Working on passive components, a power combiner can also be used as a power divider. The power can be increased by combining the currents as in the Wilkinson combiner or by combining the voltages as in the transformers combiner.



a. Wilkinson combiner

b. Transformer combiner

c. Improved transformer combiner [7]

d. Distributed-Active-Transformer [8]

Figure C-3 Power combining techniques

The principle of a Wilkinson combiner is to combine in phase the currents from several power transistors while the current generated by one power transistor cannot perturb another power transistor (opposite phase). The schematic of a Wilkinson combiner is shown in Figure C-3.a. This technique has been used in [**9**]. Some other current combiner have been implemented in [**10**] and [**11**] as an open-short stub matching network at the PA output.

On the other hand, the voltages can also be combined in phase in order to obtain a higher voltage swing at the global PA output. Transformers are good candidates to combine RF voltage swings on the secondary winding while the primary windings connected to the power transistor drain is isolated from the DC voltage on the secondary winding. The principle of voltage summation using transformers is shown in Figure C-3.b.

The topology can be optimized to integrate several primary windings on a unique secondary winding [**7**] as shown in Figure C-3.c. One of the best solutions in terms of optimization is the distributed active transformer (DAT) introduced at lower frequencies by Aoki in [**12**] and applied at 60GHz in SiGe technologies in [**8**] and in CMOS technologies in [**13**]. The principle of DAT power combiner is shown in Figure C-3.d.

References

[1] Wikipedia, The free encyclopedia. [Online]. http://en.wikipedia.org

[2] S. Pinel, et al., "A 90nm CMOS 60GHz Radio," in *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, vol. 6.8, San Francisco, CA, USA, 2008.

[3] M. D. Tsai, H. Wang, and J. F. Kuan, "A 70GHz Cascaded Multi-Stage Distributed Amplifier in 90nm CMOS Technology," in *IEEE International Solid-State Circuits Conference (ISSCC 2005), Digest of Technical Papers*, vol. 21.7, San Francisco, CA, USA, Feb. 2005.

[4] O. S. A. Tang, et al., "A 560 mW, 21% Power-Added Efficiency V-band MMIC Power Amplifier," in *IEEE 18th Annual Gallium Arsenide Integrated Circuit (GaAs IC 1996) Symposium, Technical Digest*, Orlando, FL, USA, Nov. 1996, pp. 115-118.

[5] S. Aloui, E. Kerhervé, D. Belot, and R. Plana, "A 60GHz, 13dBm Fully Integrated 65nm RF-CMOS Power Amplifier," in *Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference (NEWCAS-TAISA 2008)*, Montréal, Canada, Jun. 2008, pp. 93-96.

[6] B. Martineau, V. Knopik, A. Siligaris, F. Gianasello, and D. Belot, "A 53-to-68GHz 18dBm power amplifier with an 8-way combiner in standard 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2010), Digest of Technical Papers*, vol. 23.8, San Francisco, CA, USA, Feb. 2010, pp. 428-429.

[7] J. W. Lai and A. Valdes-Garcia, "A 1V 17.9dBm 60GHz power amplifier in standard 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2010), Digest of Technical Papers*, vol. 23.6, San Francisco, CA, USA, Feb. 2010, pp. 424-425.

[8] U. R. Pfeiffer and D. Goren, "A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 857-865, May 2007.

[9] C. Y. Law and A. V. Pham, "A high-gain 60GHz power amplifier with 20dBm output power in 90nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC 2010), Digest of Technical Papers*, vol. 23.7, San Francisco, CA, USA, Feb. 2010, pp. 426-427.

[10] M. Bohsali and A. M. Niknejad, "Current combining 60GHz CMOS power amplifiers," in *IEEE Radio Frequency Integrated Circuits (RFIC 2009) Symposium*, Boston, MA, USA, Jun. 2009, pp. 31-34.

[11] D. Dawn, et al., "60GHz CMOS power amplifier with 20-dB-gain and 12dBm Psat," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, Boston, MA, USA, Jun. 2009, pp. 537-540.

[12] I. Aoki, S. D. Kee, D. Rutledge, and A. Hajimiri, "A 2.4 GHz, 2.2 W, 2 V Fully-Integrated CMOS Circular-Geometry Active-Transformer Power Amplifier," in *IEEE Proceedings of the Custom Integrated Circuits Conference (CICC)*, San Diego, CA, USA, May 2001, pp. 57-60.

[13] Y. N. Jen, J. H. Tsai, T. W. Huang, and H. Wang, "Design and analysis of a 55-71-GHz compact and broadband distributed active transformer power amplifier in 90-nm CMOS Process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 7, pp. 1637-1646, Jul. 2009.

Annex D. N-port networks

Overview

Designers often consider circuits as an assembling of active and passive devices. However, system designers consider circuits with a black-box vision. Each circuit is seen as an N-port network with input and output ports. The way the network links the outputs to the inputs is characterized using Z, Y, h, ABCD, T or S-parameters. RF transmitter or receiver chains are hence a cascade of N-port networks and basic matrix operations are used to find the whole system performance.

This annex focuses on the most usual case of a two-port network. Some generalizations on N-port networks are also presented as the capacitive coupler presented in this thesis is a three-port network.

This annex first defines each parameter by its relation between the ports. In a second section are detailed the conversion operations between the parameters types. Those conversions are then generalized to N-port networks. The reduction of the port number is then studied which corresponds to a load impedance connected to one of the N-port network. Finally some N-port networks cascading operations are presented.

Outline

D.1. Definition of Z, Y, h, ABCD, S & T-parameters

Considering a generic two-port network with currents and voltages defined as in Figure D-1. This network can be modeled into a matrix by several ways.

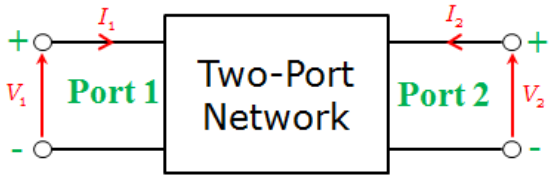


Figure D-1 A general two port network with voltages and currents defined

For more simplicity, we consider here the most common case where the 2 ports of the network are normalized on the same purely real impedance Z_0 (typically 50Ω). Otherwise, the definitions and conversion relations can be found in [**1**]. Generalization for more than two-port networks can be found in [**2**].

D.1.1. Definitions

First, we can consider the impedance Z-parameters, defined by the equation (D.1).

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{D.1}$$

But we can also consider the inverse relation (D.2) and define the admittance Y-parameters.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{D.2}$$

We can then define hybrid h-parameters by the relation (D.3).

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \tag{D.3}$$

Or chain ABCD-parameters by the equation (D.4).

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{D.4}$$

As they link the current and voltage of the two ports, these equations are usually used for electronic applications. In the microwave domain, it is often more useful to know the power of the incident and reflected waves as defined by the system (D.5) and illustrated by Figure D-2 [**3**].

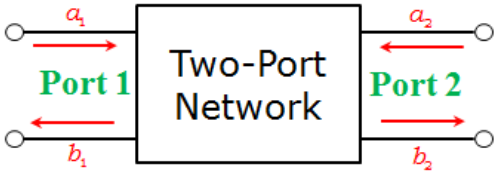


Figure D-2 A general two-port network with a's and b's waves defined

$$\begin{cases} a_1 = \dfrac{V_1 + I_1.Z_0}{2.\sqrt{Z_0}} = \dfrac{voltage\ wave\ incident\ on\ port\ 1}{\sqrt{Z_0}} = \dfrac{V_{i1}}{\sqrt{Z_0}} \\ a_2 = \dfrac{V_2 + I_2.Z_0}{2.\sqrt{Z_0}} = \dfrac{voltage\ wave\ incident\ on\ port\ 2}{\sqrt{Z_0}} = \dfrac{V_{i2}}{\sqrt{Z_0}} \\ b_1 = \dfrac{V_1 - I_1.Z_0}{2.\sqrt{Z_0}} = \dfrac{voltage\ wave\ reflected\ on\ port\ 1}{\sqrt{Z_0}} = \dfrac{V_{r1}}{\sqrt{Z_0}} \\ b_2 = \dfrac{V_2 - I_2.Z_0}{2.\sqrt{Z_0}} = \dfrac{voltage\ wave\ reflected\ on\ port\ 2}{\sqrt{Z_0}} = \dfrac{V_{r2}}{\sqrt{Z_0}} \end{cases} \quad (D.5)$$

The two-port network can now be defined by the scattering S-parameters as in the equation (D.6). This is the most used characterization technique in the Radio-Frequency community.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} . \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (D.6)$$

Also based on wave's propagation, we can finally define the chain transfer T-parameters by the relation (D.7). This last definition can differ in the literature with an inversion on both port of waves *a* and *b*.

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} . \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \quad (D.7)$$

D.1.2. Normalized parameters

All those parameters are sometimes normalized in order to simplify the equations. The normalized [*z*] matrix is actually derived from the [*Z*] matrix by the relation (D.8).

$$[z] = \frac{1}{Z_0} . [Z] \quad (D.8)$$

By the same way, the normalized [*y*] matrix is derived from the [*Y*] matrix by the relation (D.9).

$$[y] = Z_0 . [Y] \quad (D.9)$$

The normalized matrix of the h-parameters will be noted [h_n] and is defined in (D.10).

$$[h_n] = \begin{bmatrix} h_{11n} & h_{12n} \\ h_{21n} & h_{22n} \end{bmatrix} = \begin{bmatrix} h_{11}/Z_0 & h_{12} \\ h_{21} & Z_0.h_{22} \end{bmatrix} \quad (D.10)$$

The normalized matrix of the ABCD-parameters will be noted [$ABCD_n$] and is defined in (D.11).

$$[ABCD_n] = \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} = \begin{bmatrix} A & B/Z_0 \\ Z_0.C & D \end{bmatrix} \quad (D.11)$$

All those definition being made, we can now establish the relationships between Z, Y, h, ABCD, S and T-parameters. In the next section we will use appropriately natural or normalized parameters in order to simplify as most as possible the equations.

D.2. Conversion between parameters

D.2.1. Conversion into Z-parameters

i. From Y-parameters

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{Y_{22}}{Y_{11}.Y_{22} - Y_{12}.Y_{21}} & \dfrac{-Y_{12}}{Y_{11}.Y_{22} - Y_{12}.Y_{21}} \\ \dfrac{-Y_{21}}{Y_{11}.Y_{22} - Y_{12}.Y_{21}} & \dfrac{Y_{11}}{Y_{11}.Y_{22} - Y_{12}.Y_{21}} \end{bmatrix} \quad \text{(D.12)}$$

ii. From h-parameters

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{h_{11}.h_{22} - h_{12}.h_{21}}{h_{22}} & \dfrac{h_{12}}{h_{22}} \\ \dfrac{-h_{21}}{h_{22}} & \dfrac{1}{h_{22}} \end{bmatrix} \quad \text{(D.13)}$$

iii. From ABCD-parameters

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{A}{C} & \dfrac{A.D - B.C}{C} \\ \dfrac{1}{C} & \dfrac{D}{C} \end{bmatrix} \quad \text{(D.14)}$$

iv. From S-parameters

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{(1+S_{11})(1-S_{22}) + S_{12}.S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}.S_{21}} & \dfrac{2.S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}.S_{21}} \\ \dfrac{2.S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}.S_{21}} & \dfrac{(1-S_{11})(1+S_{22}) + S_{12}.S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}.S_{21}} \end{bmatrix} \quad \text{(D.15)}$$

v. From T-parameters

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{T_{11} + T_{12} + T_{21} + T_{22}}{T_{11} + T_{12} - T_{21} - T_{22}} & \dfrac{2.(T_{11}.T_{22} - T_{12}.T_{21})}{T_{11} + T_{12} - T_{21} - T_{22}} \\ \dfrac{2}{T_{11} + T_{12} - T_{21} - T_{22}} & \dfrac{T_{11} - T_{12} - T_{21} + T_{22}}{T_{11} + T_{12} - T_{21} - T_{22}} \end{bmatrix} \quad \text{(D.16)}$$

D.2.2. Conversion into Y-parameters

i. From Z-parameters

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_{22}}{Z_{11}.Z_{22} - Z_{12}.Z_{21}} & \dfrac{-Z_{12}}{Z_{11}.Z_{22} - Z_{12}.Z_{21}} \\ \dfrac{-Z_{21}}{Z_{11}.Z_{22} - Z_{12}.Z_{21}} & \dfrac{Z_{11}}{Z_{11}.Z_{22} - Z_{12}.Z_{21}} \end{bmatrix} \quad \text{(D.17)}$$

ii. From h-parameters

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{h_{11}} & \dfrac{-h_{12}}{h_{11}} \\ \dfrac{h_{21}}{h_{11}} & \dfrac{h_{11}.h_{22} - h_{12}.h_{21}}{h_{11}} \end{bmatrix} \quad \text{(D.18)}$$

iii. From ABCD-parameters

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{D}{B} & \dfrac{B.C - A.D}{B} \\ \dfrac{-1}{B} & \dfrac{A}{B} \end{bmatrix} \quad \text{(D.19)}$$

iv. From S-parameters

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{(1-S_{11})(1+S_{22}) + S_{12}.S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}.S_{21}} & \dfrac{-2.S_{12}}{(1+S_{11})(1+S_{22}) - S_{12}.S_{21}} \\ \dfrac{-2.S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}.S_{21}} & \dfrac{(1+S_{11})(1-S_{22}) + S_{12}.S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}.S_{21}} \end{bmatrix} \quad \text{(D.20)}$$

v. From T-parameters

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{T_{11} - T_{12} - T_{21} + T_{22}}{T_{11} - T_{12} + T_{21} - T_{22}} & \dfrac{-2.(T_{11}.T_{22} - T_{12}.T_{21})}{T_{11} - T_{12} + T_{21} - T_{22}} \\ \dfrac{-2}{T_{11} - T_{12} + T_{21} - T_{22}} & \dfrac{T_{11} + T_{12} + T_{21} + T_{22}}{T_{11} - T_{12} + T_{21} - T_{22}} \end{bmatrix} \quad \text{(D.21)}$$

D.2.3. Conversion into h-parameters

i. From Z-parameters

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_{11}.Z_{22} - Z_{12}.Z_{21}}{Z_{22}} & \dfrac{Z_{12}}{Z_{22}} \\ \dfrac{-Z_{21}}{Z_{22}} & \dfrac{1}{Z_{22}} \end{bmatrix} \tag{D.22}$$

ii. From Y-parameters

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{Y_{11}} & \dfrac{-Y_{12}}{Y_{11}} \\ \dfrac{Y_{21}}{Y_{11}} & \dfrac{Y_{11}.Y_{22} - Y_{12}.Y_{21}}{Y_{11}} \end{bmatrix} \tag{D.23}$$

iii. From ABCD-parameters

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{B}{D} & \dfrac{A.D - B.C}{D} \\ \dfrac{-1}{D} & \dfrac{C}{D} \end{bmatrix} \tag{D.24}$$

iv. From S-parameters

$$\begin{bmatrix} h_{11n} & h_{12n} \\ h_{21n} & h_{22n} \end{bmatrix} = \begin{bmatrix} \dfrac{(1+S_{11})(1+S_{22}) - S_{12}.S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}.S_{21}} & \dfrac{2.S_{12}}{(1-S_{11})(1+S_{22}) + S_{12}.S_{21}} \\ \dfrac{-2.S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}.S_{21}} & \dfrac{(1-S_{11})(1-S_{22}) - S_{12}.S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}.S_{21}} \end{bmatrix} \tag{D.25}$$

v. From T-parameters

$$\begin{bmatrix} h_{11n} & h_{12n} \\ h_{21n} & h_{22n} \end{bmatrix} = \begin{bmatrix} \dfrac{T_{11} - T_{12} + T_{21} - T_{22}}{T_{11} - T_{12} - T_{21} - T_{22}} & \dfrac{2.(T_{11}.T_{22} - T_{12}.T_{21})}{T_{11} - T_{12} - T_{21} - T_{22}} \\ \dfrac{-2}{T_{11} - T_{12} - T_{21} - T_{22}} & \dfrac{T_{11} + T_{12} - T_{21} - T_{22}}{T_{11} - T_{12} - T_{21} - T_{22}} \end{bmatrix} \tag{D.26}$$

D.2.4. Conversions into ABCD-parameters

i. From Z-parameters

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{Z_{11}}{Z_{21}} & \frac{Z_{11}.Z_{22} - Z_{12}.Z_{21}}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{bmatrix} \tag{D.27}$$

ii. From Y-parameters

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{-Y_{22}}{Y_{21}} & \frac{-1}{Y_{21}} \\ \frac{Y_{12}.Y_{21} - Y_{11}.Y_{22}}{Y_{21}} & \frac{-Y_{11}}{Y_{21}} \end{bmatrix} \tag{D.28}$$

iii. From h-parameters

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{h_{12}.h_{21} - h_{11}.h_{22}}{h_{21}} & \frac{-h_{11}}{h_{21}} \\ \frac{-h_{22}}{h_{21}} & \frac{-1}{h_{21}} \end{bmatrix} \tag{D.29}$$

iv. From S-parameters

$$\begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} = \begin{bmatrix} \frac{(1+S_{11})(1-S_{22}) + S_{12}.S_{21}}{2.S_{21}} & \frac{(1+S_{11})(1+S_{22}) - S_{12}.S_{21}}{2.S_{21}} \\ \frac{(1-S_{11})(1-S_{22}) - S_{12}.S_{21}}{2.S_{21}} & \frac{(1-S_{11})(1+S_{22}) + S_{12}.S_{21}}{2.S_{21}} \end{bmatrix} \tag{D.30}$$

v. From T-parameters

$$\begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} = \begin{bmatrix} \frac{T_{11} + T_{12} + T_{21} + T_{22}}{2} & \frac{T_{11} - T_{12} + T_{21} - T_{22}}{2} \\ \frac{T_{11} + T_{12} - T_{21} - T_{22}}{2} & \frac{T_{11} - T_{12} - T_{21} + T_{22}}{2} \end{bmatrix} \tag{D.31}$$

D.2.5. Conversion into S-parameters

i. From Z-parameters

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{(z_{11}-1)(z_{22}+1)-z_{12}.z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}.z_{21}} & \frac{2.z_{12}}{(z_{11}+1)(z_{22}+1)-z_{12}.z_{21}} \\ \frac{2.z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}.z_{21}} & \frac{(z_{11}+1)(z_{22}-1)-z_{12}.z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}.z_{21}} \end{bmatrix} \quad \text{(D.32)}$$

ii. From Y-parameters

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{(1-y_{11})(1+y_{22})+y_{12}.y_{21}}{(1+y_{11})(1+y_{22})-y_{12}.y_{21}} & \frac{-2.y_{12}}{(1+y_{11})(1+y_{22})-y_{12}.y_{21}} \\ \frac{-2.y_{21}}{(1+y_{11})(1+y_{22})-y_{12}.y_{21}} & \frac{(1+y_{11})(1-y_{22})+y_{12}.y_{21}}{(1+y_{11})(1+y_{22})-y_{12}.y_{21}} \end{bmatrix} \quad \text{(D.33)}$$

iii. From h-parameters

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} -\frac{(1-h_{11n})(1+h_{22n})+h_{12n}.h_{21n}}{(1+h_{11n})(1+h_{22n})-h_{12n}.h_{21n}} & \frac{2.h_{12n}}{(1+h_{11n})(1+h_{22n})-h_{12n}.h_{21n}} \\ \frac{-2.h_{21n}}{(1+h_{11n})(1+h_{22n})-h_{12n}.h_{21n}} & \frac{(1+h_{11n})(1-h_{22n})+h_{12n}.h_{21n}}{(1+h_{11n})(1+h_{22n})-h_{12n}.h_{21n}} \end{bmatrix} \quad \text{(D.34)}$$

iv. From ABCD-parameters

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{A_n+B_n-C_n-D_n}{A_n+B_n+C_n+D_n} & \frac{2.(A_n.D_n-B_n.C_n)}{A_n+B_n+C_n+D_n} \\ \frac{2}{A_n+B_n+C_n+D_n} & \frac{-A_n+B_n-C_n+D_n}{A_n+B_n+C_n+D_n} \end{bmatrix} \quad \text{(D.35)}$$

v. From T-parameters

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{T_{21}}{T_{11}} & \frac{T_{11}.T_{22}-T_{12}.T_{21}}{T_{11}} \\ \frac{1}{T_{11}} & \frac{-T_{12}}{T_{11}} \end{bmatrix} \quad \text{(D.36)}$$

D.2.6. Conversion into T-parameters

i. From Z-parameters

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{(z_{11}+1)(z_{22}+1)-z_{12}.z_{21}}{2.z_{21}} & \frac{(z_{11}+1)(z_{22}-1)+z_{12}.z_{21}}{2.z_{21}} \\ \frac{(z_{11}-1)(z_{22}+1)-z_{12}.z_{21}}{2.z_{21}} & \frac{(z_{11}-1)(z_{22}-1)+z_{12}.z_{21}}{2.z_{21}} \end{bmatrix} \quad \text{(D.37)}$$

ii. From Y-parameters

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{(-1-y_{11})(1+y_{22})+y_{12}.y_{21}}{2.y_{21}} & \frac{(1+y_{11})(1-y_{22})+y_{12}.y_{21}}{2.y_{21}} \\ \frac{(-1+y_{11})(1+y_{22})-y_{12}.y_{21}}{2.y_{21}} & \frac{(1-y_{11})(1-y_{22})-y_{12}.y_{21}}{2.y_{21}} \end{bmatrix} \quad \text{(D.38)}$$

iii. From h-parameters

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{(-1-h_{11n})(1+h_{22n})+h_{12n}.h_{21n}}{2.h_{21n}} & \frac{(1+h_{11n})(1-h_{22n})+h_{12n}.h_{21n}}{2.h_{21n}} \\ \frac{(1-h_{11n})(1+h_{22n})+h_{12n}.h_{21n}}{2.h_{21n}} & \frac{(-1+h_{11n})(1-h_{22n})+h_{12n}.h_{21n}}{2.h_{21n}} \end{bmatrix} \quad \text{(D.39)}$$

iv. From ABCD-parameters

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{A_n+B_n+C_n+D_n}{2} & \frac{A_n-B_n+C_n-D_n}{2.} \\ \frac{A_n+B_n-C_n-D_n}{2} & \frac{A_n-B_n-C_n+D_n}{2} \end{bmatrix} \quad \text{(D.40)}$$

v. From S-parameters

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{S_{21}} & \frac{-S_{22}}{S_{21}} \\ \frac{S_{11}}{S_{21}} & \frac{S_{12}.S_{21}-S_{11}.S_{22}}{S_{21}} \end{bmatrix} \quad \text{(D.41)}$$

D.3. Conversion between parameters, generalization for N-port networks

When generalizing to an N-port network, only Y, Z and S-parameters have a similar definition that for a 2-port network without any ambiguity. Moreover, the conversion between those three parameters can be generalized easily using matrix operation. In the following equations, [*I*] stands for the unity matrix.

D.3.1. Conversion into Z-parameters

i. From Y-parameters

$$[Z] = [Y]^{-1} \tag{D.42}$$

ii. From S-parameters

$$[Z] = Z_0.([I]+[S]).([I]-[S])^{-1} \tag{D.43}$$

D.3.2. Conversion into Y-parameters

i. From Z-parameters

$$[Y] = [Z]^{-1} \tag{D.44}$$

ii. From S-parameters

$$[Y] = Z_0^{-1}.([I]-[S]).([I]+[S])^{-1} \tag{D.45}$$

D.3.3. Conversion into S-parameters

i. From Z-parameters

$$[S] = ([Z]+Z_0.[I])^{-1}.([Z]-Z_0.[I]) \tag{D.46}$$

ii. From Y-parameters

$$[S] = ([I]+Z_0.[Y])^{-1}.([I]-Z_0.[Y]) \tag{D.47}$$

D.4. N-port into M-port networks conversion

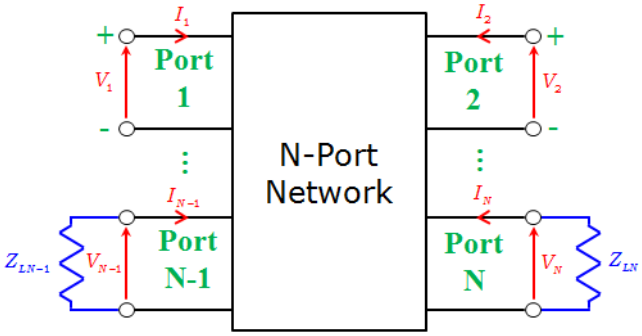


Figure D-3 N-port into M-port networks conversion

D.4.1. 3-port into 2-port conversion

Considering a 3-port network defined by its Z-parameters as written by the equation (D.48), the Z-parameters matrix has been decomposed in 4 sub-matrixes A, B, C and D.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \left[\begin{array}{cc|c} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ \hline Z_{31} & Z_{32} & Z_{33} \end{array}\right] . \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} . \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \quad \text{(D.48)}$$

The load condition on the 3rd port is known, which gives the well-known Ohm's relation of the equation (D.49) between the voltage and the current of this port.

$$V_3 = Z_L . I_3 \quad \text{(D.49)}$$

The 3-port network being charged by a fixed load impedance on its 3rd port as illustrated in Figure D-3, it can be simplified into a 2-port network defined by a new Z-parameter matrix in equation (D.50).

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11}' & Z_{12}' \\ Z_{21}' & Z_{22}' \end{bmatrix} . \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = Z' . \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad \text{(D.50)}$$

The Z-parameters matrix of the new 2-port network can be calculated as a function of the Z-parameters matrix of the old 3-port network using the equation (D.51).

$$\begin{bmatrix} Z_{11}' & Z_{12}' \\ Z_{21}' & Z_{22}' \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} + \begin{bmatrix} Z_{13} \\ Z_{23} \end{bmatrix} . \left(Z_L - Z_{33}\right)^{-1} . \begin{bmatrix} Z_{31} & Z_{32} \end{bmatrix} \quad \text{(D.51)}$$

This relation can be written in a more simple way by the equation (D.52) where the 2-port Z-parameters matrix Z' in defined as a simple operation on the A, B, C, D and Z_L matrix previously defined.

$$Z' = A + B . \left(Z_L - D\right)^{-1} . C \quad \text{(D.52)}$$

D.4.2. 4-port into 2-port conversion

Considering now a 4-port network defined by its Z-parameters as written by the equation (D.53). As previously explained, the Z-parameters matrix has been decomposed in 4 sub-matrixes A, B, C and D.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \left[\begin{array}{cc|cc} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ \hline Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{array}\right] \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \quad \text{(D.53)}$$

The load condition on the 3rd and the 4th port are known which gives the well-known Ohm's relation of the equation (D.54) between the voltages and the currents of those ports.

$$\begin{bmatrix} V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{L3} & 0 \\ 0 & Z_{L4} \end{bmatrix} \cdot \begin{bmatrix} I_3 \\ I_4 \end{bmatrix} = Z_L \cdot \begin{bmatrix} I_3 \\ I_4 \end{bmatrix} \quad \text{(D.54)}$$

The 4-port network being charged by fixed load impedances on its 3rd and 4th port, it can be simplified into a 2-port network defined by a new Z-parameter matrix defined by the equation (D.55).

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11}' & Z_{12}' \\ Z_{21}' & Z_{22}' \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = Z' \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad \text{(D.55)}$$

The Z-parameters matrix of the 2-port network can be calculated in terms of the Z-parameters matrix of the 4-port network using the equation (D.56).

$$\begin{bmatrix} Z_{11}' & Z_{12}' \\ Z_{21}' & Z_{22}' \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} + \begin{bmatrix} Z_{13} & Z_{14} \\ Z_{23} & Z_{24} \end{bmatrix} \cdot \left(\begin{bmatrix} Z_{L3} & 0 \\ 0 & Z_{L4} \end{bmatrix} - \begin{bmatrix} Z_{33} & Z_{34} \\ Z_{43} & Z_{44} \end{bmatrix} \right)^{-1} \cdot \begin{bmatrix} Z_{31} & Z_{32} \\ Z_{41} & Z_{42} \end{bmatrix} \quad \text{(D.56)}$$

This relation can be written in a more simple way by the equation (D.57) where the 2-port Z-parameters matrix *Z'* in defined as a simple operation on the *A*, *B*, *C*, *D* and Z_L matrix previously defined.

$$Z' = A + B.\left(Z_L - D\right)^{-1}.C \quad \text{(D.57)}$$

Note that equations (D.57) and (D.52) are identical meaning that this relation could probably be generalized to a N-port to M-port conversion.

D.5. Cascading 2 two-port networks

The interest in working with matrix becomes obvious when trying to cascade several RF blocks. Cascading 2 two-port networks can be seen by simulators as a simple operation on matrixes rather than a complex assembling of active and passive devices. We present here the easiest way to compute the cascading of 2 two-port networks, which is to use T-parameters.

We consider the cascade of 2 two-port networks defined by their T-matrix [*T*] and [*T'*] as illustrated in Figure D-4.

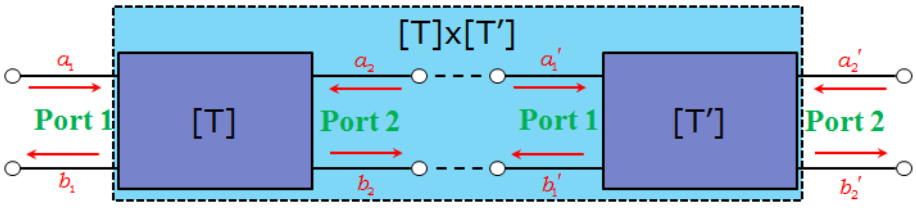


Figure D-4 Cascading 2 two-port networks

Both networks can so be defined by the T-parameters relation (D.58) between incidents *a*'s and reflected *b*'s waves.

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = [T] \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \quad \& \quad \begin{bmatrix} a_1' \\ b_1' \end{bmatrix} = [T'] \begin{bmatrix} b_2' \\ a_2' \end{bmatrix} \tag{D.58}$$

Following the definitions of incident and reflected waves (see section D.1.1), we can match the port 2 of the 2nd network with the port 1 of the 1st network by the relation (D.59).

$$\begin{bmatrix} b_2 \\ a_2 \end{bmatrix} = \begin{bmatrix} a_1' \\ b_1' \end{bmatrix} \tag{D.59}$$

We can then simplify the 2 relations of equation (D.58) into the simple equation (D.60).

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = [T] . [T'] \begin{bmatrix} b_2' \\ a_2' \end{bmatrix} \tag{D.60}$$

To conclude, the T-matrix of the cascade of 2 two-port networks is simply the product of the T-matrix of each individual two-port network. Furthermore, the Z, Y, h, ABCD or S-matrix of the cascade of 2 two-port networks can be calculated as the conversion – using equations (D.12) to (D.41) – from the product of the T-matrix of each two-port network that can also be converted using equations (D.12) to (D.41) from Z, Y, h, ABCD or Z-parameters.

D.6. Cascading 2 three-port networks

In the previous section, 2 two-port networks have been cascaded. The same cascade operation will be presented in this section but now considering 2 three-port networks coupled together between the port 2 of the first network and the port 1 of the second network, as shown in Figure D-5.

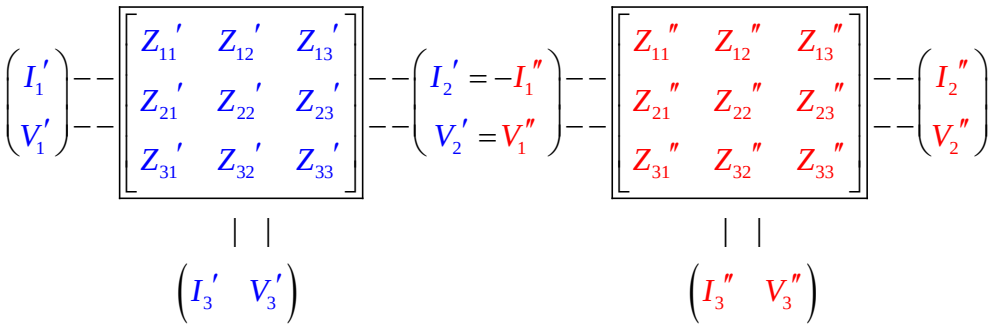


Figure D-5 Cascading 2 three-port networks

The cascading of 2 three-port networks with only one port in common between the two networks generates a single four-port network. The resulting Z-parameters can be presented in several ways, depending of the arrangement of the four ports. For reading simplicity, the Z-parameters of the four-port network links the resulting voltages V_1' and V_3' of the first three-port network and the resulting voltages V_2'' and V_3'' of the second three-port network to their respecting currents I_1', I_3', I_2'', and I_3''.

The equation (D.61) presents the resulting Z-parameters of the four-port network as a simple matrix operation between the parameters of the two three-port networks.

$$\begin{bmatrix} V_1' \\ V_3' \\ V_2'' \\ V_3'' \end{bmatrix} = \left(\begin{bmatrix} Z_{11}' & Z_{13}' & 0 & 0 \\ Z_{31}' & Z_{33}' & 0 & 0 \\ 0 & 0 & Z_{22}'' & Z_{23}'' \\ 0 & 0 & Z_{32}'' & Z_{33}'' \end{bmatrix} - \frac{1}{Z_{22}' + Z_{11}''} \cdot \begin{bmatrix} Z_{12}' \\ Z_{32}' \\ -Z_{21}'' \\ -Z_{31}'' \end{bmatrix} \cdot \begin{bmatrix} Z_{21}' & Z_{23}' & -Z_{12}'' & -Z_{13}'' \end{bmatrix} \right) \cdot \begin{bmatrix} I_1' \\ I_3' \\ I_2'' \\ I_3'' \end{bmatrix} \quad \text{(D.61)}$$

D.7. Cascading one three-port network and one two-port network

After having cascaded 2 two-port networks and 2 three-port networks, this section investigates the cascade of one three-port network with one two-port network. This cascading operation is illustrated in Figure D-6.

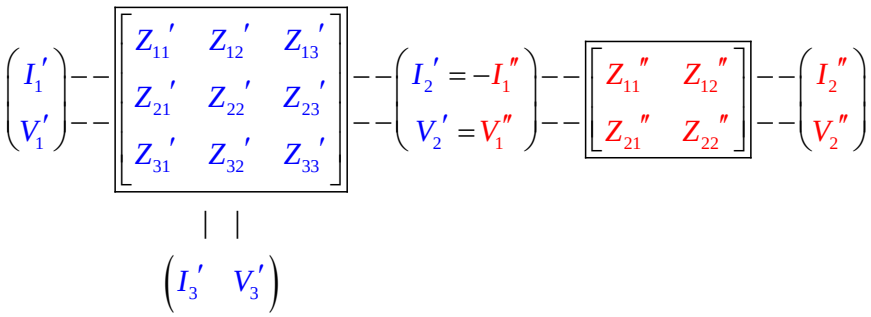


Figure D-6 Cascading one three-port network and one two-port network

The cascading of the two networks generates a single three-port network as the two-port network is only a prolongation of one of the three port of the other network. Here again, the resulting Z-parameters can be presented in several ways, depending of the arrangement of the three ports. For reading simplicity, the Z-parameters of the final three-port network links the resulting voltages V_1' and V_3' of the first three-port network and the resulting voltage V_2'' of the second three-port network to their respecting currents I_1', I_3', and I_2''. The equation (D.62) presents the resulting Z-parameters of the three-port network as a simple matrix operation between the parameters of the two initial networks.

$$\begin{bmatrix} V_1' \\ V_3' \\ V_2'' \end{bmatrix} = \left(\begin{bmatrix} Z_{11}' & Z_{13}' & 0 \\ Z_{31}' & Z_{33}' & 0 \\ 0 & 0 & Z_{22}'' \end{bmatrix} - \frac{1}{Z_{22}' + Z_{11}''} \cdot \begin{bmatrix} Z_{12}' \\ Z_{32}' \\ -Z_{21}'' \end{bmatrix} \cdot \begin{bmatrix} Z_{21}' & Z_{23}' & -Z_{12}'' \end{bmatrix} \right) \cdot \begin{bmatrix} I_1' \\ I_3' \\ I_2'' \end{bmatrix} \quad \text{(D.62)}$$

References

[1] D. A. Frickey, "Conversions Between S, Z, Y, h, ABCD, and T Parameters which are Valid for Complex Source anc Load Impedances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 205-211, 1994.

[2] R. A. Soares, "GaAs MESFET Circuit Design," Artech House Publishers ISBN 0890062676, 1998.

[3] D. Anderson, L. Smith, and J. Gruszinsky, "S-Parameter Techniques," Hewlett Packard Application Note AN 95-1, 1997. [Online]. http://www.hpmemory.org

Annex E. T-lines: theory and modeling

Overview

Transmission lines are widely used at millimeter-wave frequencies. The wavelength actually becomes small enough to facilitate the integration of such propagation components. This annex is dedicated to the T-lines that have been used in this Ph.D. work.

The theory of such propagation elements is first presented through the definition of characteristic parameters. A transmission line is composed of two connectors; the first one is used to propagate the signal while the second one works as a ground reference. Several structures can actually be imagined to work as a transmission line. Three of them are often used in circuit design: microstrip, coplanar and grounded-coplanar. Those three structures are detailed in this annex with a discussion of their performance.

It is often necessary to model transmission lines with an equivalent circuit composed of usual lumped components. Electro-magnetic simulations have actually to be performed to obtain the electrical characteristics of a transmission line. Building an equivalent circuit from the EM simulation results highly simplifies the circuit simulations. Moreover, T-lines are, most of the time, characterized in terms of S-parameters which are defined in the frequency domain, while transient simulation requires components defined in the time domain. The modeling is hence presented in this annex through a brief description of the interest of building a model, and a presentation of two well-known models: the RLCG and the symmetrical RLCG.

Outline

E.1. Theory on transmission lines

E.1.1. T-line parameters

Transmission lines are characterized by specific parameters [**1**] which will be presented hereafter. First we have to consider that the structures use only Transverse Electro-Magnetic (TEM) or quasi-TEM propagation modes, which mean that both the electric and the magnetic fields are perpendicular to the propagation direction. This assumption being made, we can define the characteristic impedance Z_c as the impedance presented to the connected components at both ends of the T-line.

Another specific parameter is the propagation constant γ which characterizes the propagation of the electro-magnetic waves along the T-line and in its vicinity. As an example, a unidirectional propagation wave along the x-axis is composed of an incident wave and a reflected wave depending of the propagation constant γ as shown in the equation (E.1).

$$E(x) = E^{+}.e^{-\gamma.x} + E^{-}.e^{+\gamma.x} \tag{E.1}$$

A transmission line with Z_c characteristic impedance, γ propagation constant and L length can be considered as a quadripole with the chain matrix *ABCD* defined by the equation (E.2).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma.L) & Z_c.\sinh(\gamma.L) \\ \sinh(\gamma.L)/Z_c & \cosh(\gamma.L) \end{bmatrix} \tag{E.2}$$

The chain matrix *ABCD* being linked to the *S* matrix (see Annex D for more details on chain matrix), the characteristic impedance Z_c can be expressed in terms of S-parameters by the equation (E.3) where Z_0 stands for the reference impedance for the S-parameters (most of time 50Ω).

$$Z_c = Z_0.\sqrt{\frac{(1+S_{11})(1+S_{22})-S_{21}.S_{12}}{(1-S_{11})(1-S_{22})-S_{21}.S_{12}}} \tag{E.3}$$

In the same way, the propagation constant γ can be expressed in terms of S-parameters of the T-line by the equation (E.4).

$$\gamma = \frac{1}{L}.\cosh^{-1}\left(\frac{(1+S_{11})(1-S_{22})+S_{21}.S_{12}}{2.S_{21}}\right) \tag{E.4}$$

This propagation constant γ can be decomposed in 2 components, the real part α called attenuation constant, and the imaginary part β called phase constant (equation (E.5)).

$$\gamma = \alpha + i.\beta \tag{E.5}$$

The natural units of the attenuation constant α are Nepers per meter [Np/m] which can be converted into [dB/m] using the relation (E.6).

$$\alpha_{[dB/m]} = 20.\log_{10}(e).\alpha_{[Np/m]} \approx 8.686.\alpha_{[Np/m]} \tag{E.6}$$

The phase constant β links the velocity v_φ of the wave phase that propagates in the T-line to the exciting signal frequency *f*. So the phase constant β is proportional to the opposite of the guided wave length λ_g as written in the equation (E.7).

$$\beta = \frac{2\pi.f}{v_\varphi} = \frac{2\pi}{\lambda_g} \tag{E.7}$$

The guided wavelength λ_g can be expressed in terms of wave celerity in free space c, wave frequency f and dielectric permittivity ε_r of the oxide that encloses the T-line. λ_g can so be linked to the free space wave length λ_0 and the dielectric permittivity ε_r as highlights the equation (E.8).

$$\lambda_g = \frac{c}{f \cdot \sqrt{\varepsilon_r}} = \frac{\lambda_0}{\sqrt{\varepsilon_r}} \tag{E.8}$$

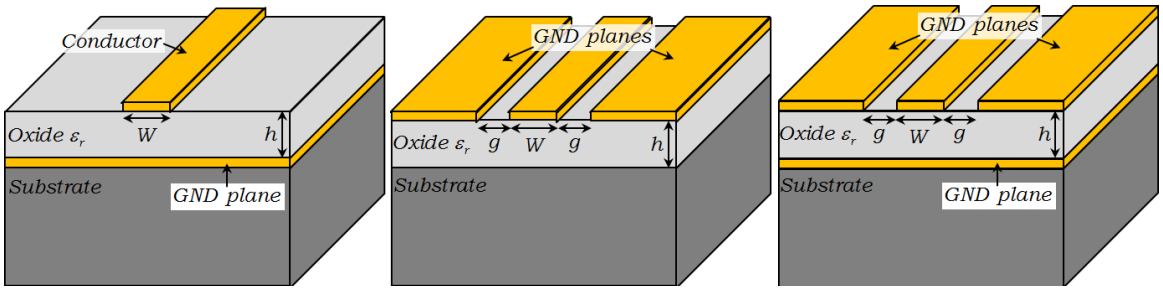
T-lines are often designed to reach a 50Ω characteristic impedance (measurement equipment often presents 50Ω input impedance). The attenuation constant is always minimized as much as possible.

E.1.2. T-line structure

Several structures, detailed in [**1**], can be considered as transmission lines. First, microstrip lines (sometimes written µstrip), invented in 1952 by Grieg and Engelman [**2**], are composed of a conductor line in which will propagate the wave and a ground plane working as a reference for the current loop. A dielectric separates these two elements as shown in Figure E-1.a.

The second structure, called coplanar waveguide (often referred as CPW), was invented in 1969 by Wen [**3**]. CPW are composed of a conductor line in which the wave propagates and a ground plane on each side of this conductor in the same plane. Those two ground planes are used as a reference for the current loop. Those three elements (the conductor line and the two ground planes) lies on a dielectric as can be seen in Figure E-1.b.

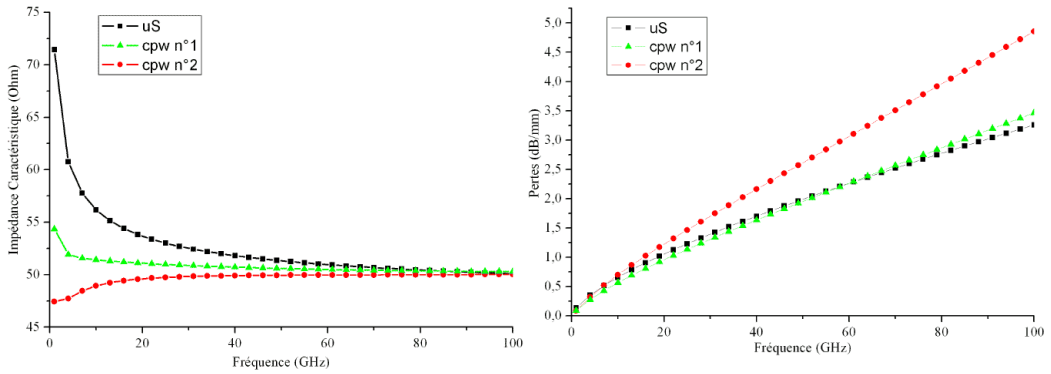
Finally combinations of both microstrip and coplanar structures can be imagined resulting in several structures as the grounded coplanar waveguide (G-CPW) represented in Figure E-1.c which is more similar to classical non-integrated waveguides as the conductor line has three blinded sides.



a. Microstrip (µstrip) **b. Coplanar (CPW)** **c. Grounded coplanar (G-CPW)**

Figure E-1 Three different T-line structures

A brief comparison between µstrip and CPW lines can be found in [**1**] for the CMOS 65nm process with a 6 metal layers Back-End-Of-Light (BEOL) from STMicroelectronics. The characteristic impedance and the attenuation coefficient of two CPW and one µstrip is shown in Figure E-2 respectively a and b.



a. Characteristic impedance **b. Attenuation constant**

µS: Microstrip ; CPW: Coplanar

Figure E-2 Comparison of 3 T-lines designed in CMOS 65nm 6metal layers BEOL from STMicroelectronics [1]

The three T-lines manage to provide around 50Ω characteristic impedance (within 5% errors) for frequencies higher than 50GHz. However it is more complicated to conclude on the attenuation coefficient. One of the CPW has a high 3dB/mm attenuation constant at 60GHz while with another configuration of CPW – different conductor width and gap between the conductor and the coplanar ground planes – 1dB/mm attenuation constant is saved and this CPW has similar performances than the µstrip. Those contrasted results prove that it is more the configuration than the structure of the T-line that impacts the performances of the T-line.

The attenuation constant highly depends on the degrees of freedom of the chosen structure. The first one which is common to every integrated T-line structure is the distance between the mmW conductor and the substrate (or the ground plane in microstrip configuration) which is fixed by the choice of the metal layer in a given process.

Figure E-3 extracted from [**4**] presents the performances that could be expected for different line types (MS stands for microstrip, CPW for coplanar waveguide) and different technologies. Note that the CMOS 65nm process is clearly not the best one in comparison with mmW-dedicated BEOL. This is due to the fact that decreasing the active devices lengths, the same scaling factor occurs on the BEOL. Especially, the distance between the upper metal and the substrate decreases dramatically, thus increasing the attenuation constant of propagation elements. However, using a 7 metal layers rather than a 6 metal layers BEOL of the same CMOS 65nm technology has significant positive impact on a T-line performance.

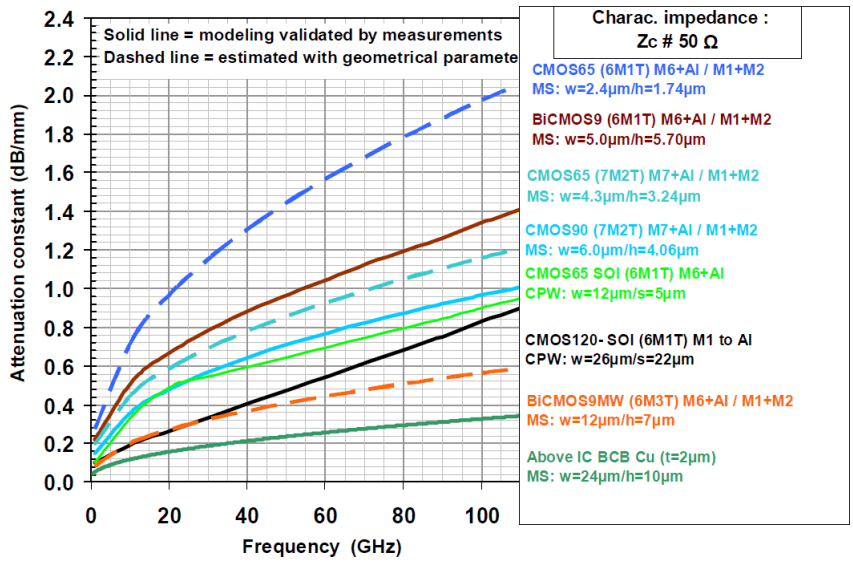


Figure E-3 Measured attenuation constants for 50Ω transmission lines in different technologies (pure digital and mmW-dedicated BEOL) [4]

Thus, in the different circuit implementation presented in this PhD thesis, we have used the upper metal layer, M7 in our targeted 65nm CMOS 7 metal layers BEOL, for the signal conductor and the M1 and M2 layers for the ground plane – M1 is a thin metal that is not well suited for ground planes. This way, we maximize the distance between the conductor and the ground plane for the microstrip propagation mode.

E.2. Modeling a T-line

E.2.1. Interest of the modeling

The S-parameters – obtained by electro-magnetic simulations performed either using Momentum from Agilent or HFSS from Ansoft – can be imported in Cadence environment to perform the circuit simulations including the propagation elements such as transmission lines. This is very powerful for frequency domain simulations. However this will cause a problem for time domain

simulations like transient analysis. The S-parameters, which are defined in the frequency domain, need to be converted in the time domain using the inverse fast Fourier transfer algorithm (i-FFT). This conversion introduces some imprecision and also processing time.

This imprecision is considered to be negligible if the i-FFT can dispose of enough frequency samples. It is usually admitted that a factor 5 should be guaranteed between the highest operation frequency and the Shannon sampling frequency to have an accurate enough i-FFT conversion. Reminding that the Shannon sampling frequency is twice the higher frequency that could be simulated – and Shannon frequency is a minimum value… This means that the S-parameters should be defined up to 10 times the higher time simulated frequency. To be able to simulate a 60GHz sinewave (an OFDM modulated signal will induce higher simulation frequencies…), the S-parameters should be defined up to 600GHz to be used directly in a time domain simulator.

This requirement will induce a high cost in terms of time duration of the electro-magnetic simulations. Assuming the mesh size of the EM simulator depends on the maximum frequency, the simulator has to deal with too many meshes, thus drastically increasing the simulation time. Another solution to overcome this issue is to build an electrical analytical model of the propagation element. This model will be directly simulated in the time domain without any use of i-FFT algorithm.

E.2.2. RLCG model

The transmission line equivalent circuit decomposed the T-line in *N* sections of elementary lumped components [**5**]. Ideally, *N* is infinite and each section represents an infinitesimally short segment of the T-line. Each segment is a two-port network including a series resistance *r* which represents the distributed resistance of the conductor, a series inductance *l* which represents the distributed inductance of the conductor, a shunt capacitor *c* which corresponds to the capacitance between the two conductors, and a shunt conductance *g* which corresponds to the conductance of the dielectric material separating the two conductors. This elementary line section is represented in Figure E-4.

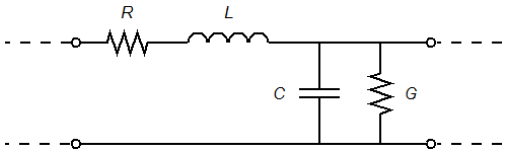


Figure E-4 Equivalent RLCG circuit of one section of a T-line

The characteristic impedance Z_c and the propagation constant γ of the T-line – presented earlier in this section – can now be written as a function of the lumped elements *r*, *l*, *c* and *g* of the T-line distributed model following the equations (E.9) and (E.10).

$$Z_c = \sqrt{\frac{r + j.l.\omega}{g + j.c.\omega}} \tag{E.9}$$

$$\gamma = \sqrt{(r + j.l.\omega)(g + j.c.\omega)} \tag{E.10}$$

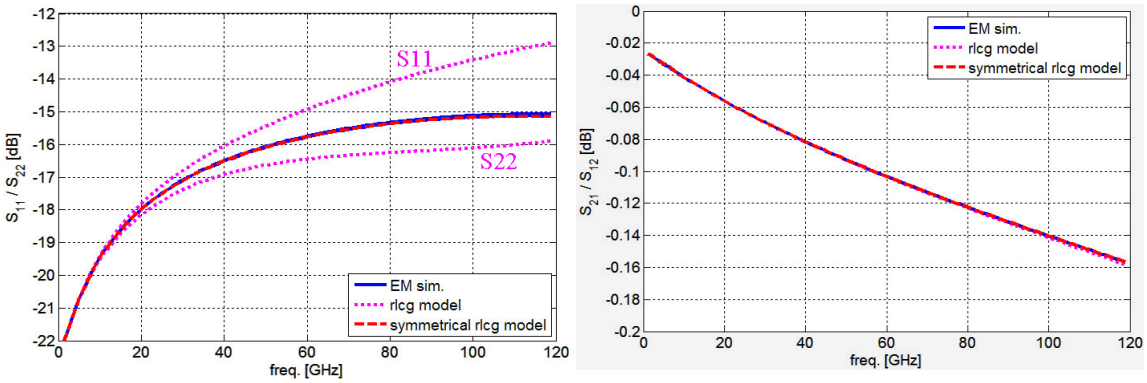
The four lumped elements *r*, *l*, *c* and *g* can so be calculated from the T-line characteristic impedance Z_c and propagation constant γ using the relation (E.11).

$$\begin{cases} r_{[\Omega/m]} = \mathrm{Re}(Z_c.\gamma) & l_{[H/m]} = \mathrm{Im}(Z_c.\gamma)/\omega \\ c_{[F/m]} = \mathrm{Im}(\gamma/Z_c)/\omega & g_{[S/m]} = \mathrm{Re}(\gamma/Z_c) \end{cases} \tag{E.11}$$

Considering in practice a finite number N of sections for the T-line model, the length of each section is $L_N = L/N$. The distributed lumped elements *r* (in [*Ω/m*]), *l* (in [*H/m*]), *c* (in [*F/m*]) and *g* (in [*S/m*]) can be multiplied by the length L_N of each section to constitute real resistance (in [*Ω*]), inductance (in [*H*]), capacitance (in [*F*]) and admittance (in [S]).

E.2.3. Symmetrical RLCG model

Figure E-5 establishes a comparison between the EM simulation results (using HFSS software) and the RLCG model presented above. This comparison has been built considering the G-CPW transmission line designed for the first circuit implementation and presented in section II.2.2.ii. The RLCG model corresponds to a decomposition of the 190µm long T-line into 19 segments of 10µm long as explained in section II.2.2.ii. The reflection parameters S_{11} and S_{22} are plotted in Figure E-5.a and the transmission parameters S_{12} and S_{21} are plotted in Figure E-5.b.



a. Reflection S_{11} and S_{22} parameters **b. Transmission S_{21} and S_{12} parameters**

Figure E-5 Comparison between the electro-magnetic simulation (HFSS) and the RLCG models

This very simple electrical model achieves very good results in comparison to the EM simulation. The only difference concerns the reflection parameters: as a line segment is inherently symmetrical, S_{11} and S_{22} should be equal. Therefore a minor modification is made on the RLCG model to have a "symmetrical RLCG model" as shown in Figure E-6. In regards to its performance (see Figure E-5), this model has been used in simulations instead of the EM simulation. Note that an EM simulation is still required to determine the 4 parameters of the electrical model.

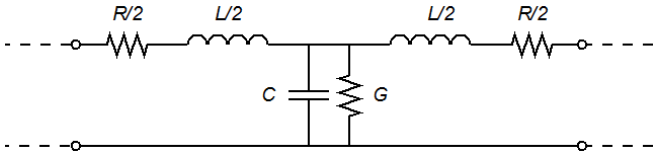


Figure E-6 Symmetrical equivalent RLCG circuit of one T-line section

References

[1] N. Seller, "Contribution à l'Étude, au Développement et à la Réalisation d'Oscillateurs à Commandes Numériques en Technologie Silicium CMOS Avancée," Ph.D. Thesis, Université Bordeaux 1, Bordeaux, France.

[2] D. D. Grieg and H. F. Engelmann, "Microstrip - A new transmission technique for the kilomegacycle range," in *IEEE Proceedings of the Institute of Radio Engineers (IRE)*, New-York, NY, USA, Dec. 1952, pp. 1644-1650.

[3] C. P. Wen, "Coplanar waveguide: A surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-17, no. 12, pp. 1087-1090, Dec. 1969.

[4] A. Cathelin, et al., "Design for Millimeter-wave Applications in Silicon Technologies," in *IEEE Proceedings of the 33rd European Solid-State Circuits Conference (ESSCIRC 2007)*, Munich, Germany, 2007, pp. 464-471.

[5] B. Martineau, "Potentialités de la technologie CMOS 65nm SOI pour des applications sans fils en bande millimétrique," Ph.D. Thesis, Université des Sciences et Techniques de Lille, Lille, France, May 2008.

Annex F. PowDet60G: physical circuit implementation for testability

Overview

The power detector and power coupler presented in section II.2 have been implemented on a test chip called PowDet60G in order to verify the functionality of the power detector before using it in a regulation loop (see Chapter IV). The circuit realization should hence validate the electromagnetic simulations of the capacitive coupler (section II.2.2) and prove that the power detector circuit effectively works at 60GHz as seen in the simulations of section II.2.1.

However some precautions have to be taken in order to be able to test the circuit and some adjacent components have to be implemented together with the power detector and the power coupler which are the "useful" part of the final circuit (see section II.3.2.i). Some de-embedding structures have also to be implemented in addition to the final circuit to be able to deduce the desired characteristics on the useful part of the circuit from the full circuit measurements. This annex presents all those elements.

Outline

F.1. Designed circuit for testability

F.1.1. Circuit synoptic

Figure F-1 shows the synoptic of the PowDet60G circuit implementation (also presented in section II.3.1). The differential detector is integrated between the two couplers. Each coupler is integrated inside a coplanar wave-guide (CPW) transmission line (T-line). A buffer is necessary to amplify and convert the detector output current into a voltage that can be sensed by measurement equipment with 50Ω input impedance.

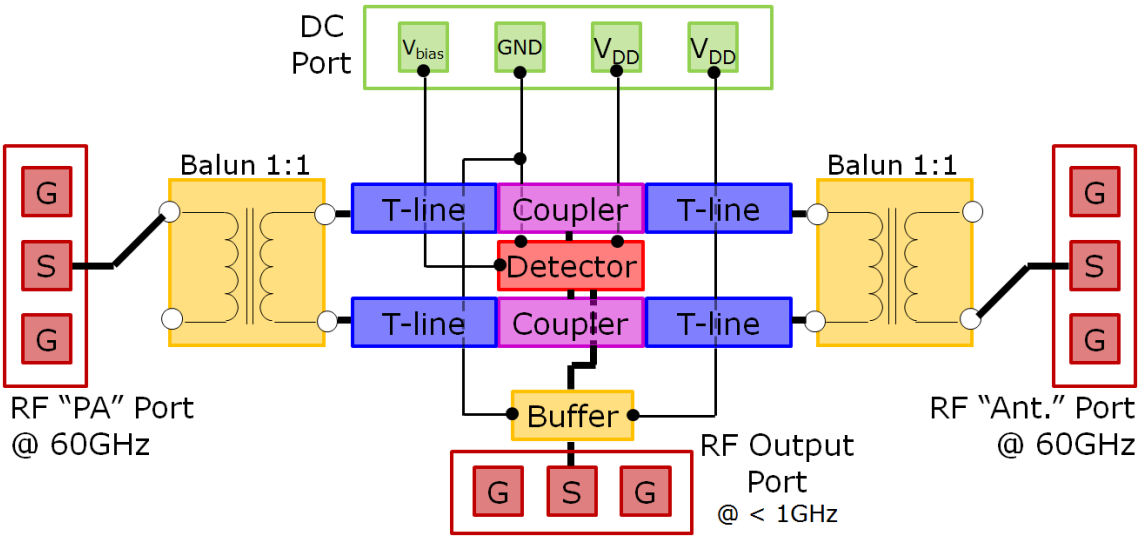


Figure F-1 PowDet60G circuit synoptic

When this circuit was designed, none of our laboratories had 60GHz differential probes. Therefore baluns were integrated at both sides of the transmission line to be compatible with the available equipment.

The next sections detail separately the implementation of each block which are parts of the circuit synoptic of Figure F-1. However the useful part (the power couplers and the power detector) of the circuit has already been presented in section II.3.2.i and is not described in this annex. Some explanations on the DC signal connections integrated inside the ground beams of the G-CPW can also be found in section II.3.2.ii.

F.1.2. Buffer

The buffer was introduced in section II.2.1.iii as a current-to-voltage converter. This converter was designed to drive a 50Ω load. But this functionality is not necessary to the power detection operation. Hence the buffer has not been integrated just close to the power detector inside the ground wall between the two T-lines and power couplers.

Figure F-2 shows the layout of the buffer which has been implemented with a proper power supply to be able to separate the power consumption of this block and the one of the power detector. The only layout constraint is set on the input where the parasitic capacitors should be minimized to let this block work at up to 100MHz. But this is a much lower constraint than for the power detector layout where the signals reach 60GHz. The size of this block is 48 x 36µm².

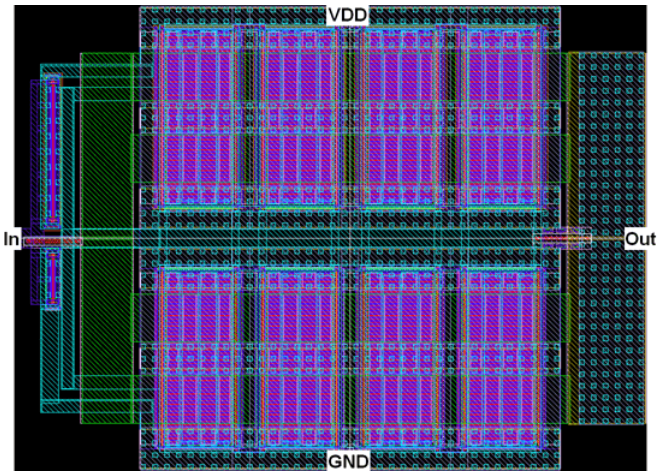


Figure F-2 Buffer layout

F.1.3. Baluns

Baluns are integrated at both ends of the transmission line to interface this differential T-line with the single-ended pads. A balun is composed of 2 coupled inductances, one called primary, the other called secondary. The wave that flows in the primary winding induces a similar wave in the secondary winding by electromagnetic coupling effects. A balun is hence able to transfer RF signals with no DC connection between its input (primary) and output (secondary). This corresponds to our application where the DC ground is set to one end of the primary inductor and to the middle of the secondary loop resulting in a single-ended to differential conversion.

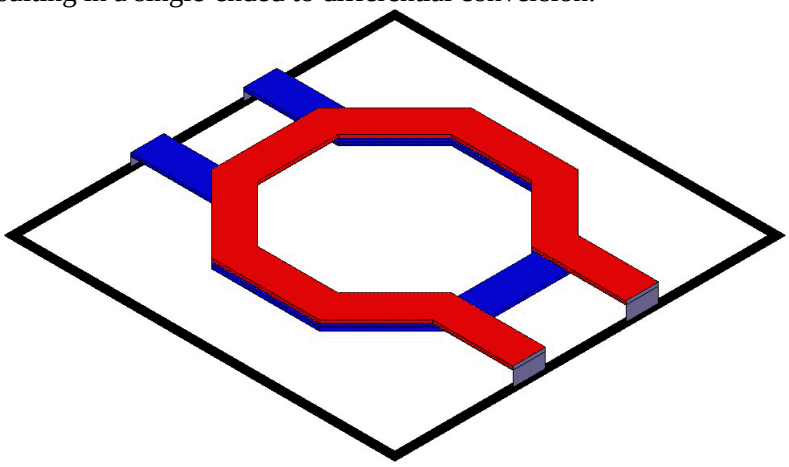


Figure F-3 Designed balun (3D view from Ansoft HFSS)

Figure F-3 shows a 3D view of the designed balun. The primary (in blue) and the secondary (in red) are stacked in the two thick upper metal layers, the 6^{th} and the 7^{th} ones. The shape of the two inductors is 60µm diameter octagons (the diameter is defined at the center of the signal path) and an 8µm width signal path. The two windings are flipped in order to connect this balun in a series manner. The design and optimization of such mmW transformers is part of another PhD work currently on-going at IMS laboratories by Bernardo Leite [**1**].

The empty black square and the gray rectangles in Figure F-3 correspond respectively to the ground reference and to the ports which have to be defined for the EM simulation using Ansoft HFSS. The EM simulations have been performed considering 4 excitation ports which are the two connections of each of the two inductors. However those 4 ports are reduced to 2 ports here – equivalent to a fully single-ended configuration – to simplify the understanding. This simplification is made by selecting one port on each winding and grounding the other one. The two remaining ports

should ensure a common direction of the currents flowing into the two windings. The computation of the 4-port network into a 2-port network is detailed in Annex D.

Figure F-4 shows the simulation results in terms of S-parameters. The isolation S_{12} parameter is equal to the transmission S_{21} parameter considering a passive network and is hence not represented in Figure F-4. The matching S_{11} and S_{22} parameters are not exactly the same as the primary winding is nearer to the substrate than the secondary one. This results in a -2dB attenuation coefficient at 60GHz while the input and output matching are around -5.5dB.

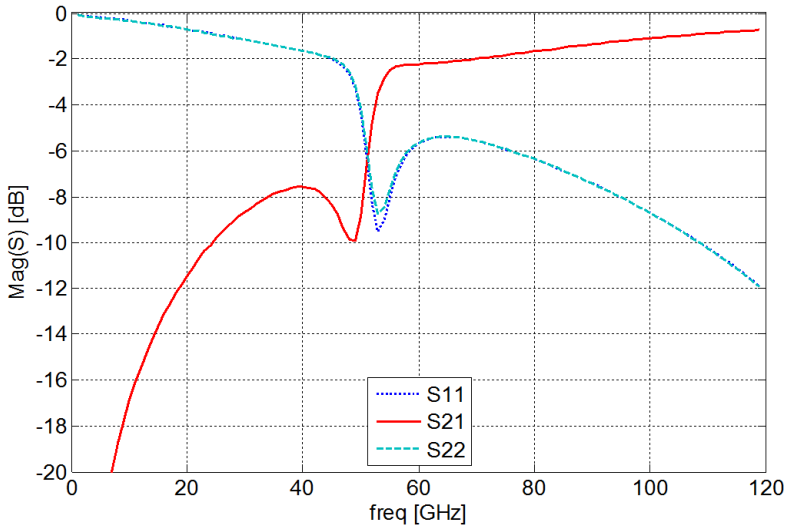


Figure F-4 S-parameters simulation results of the Balun (obtained with Ansoft HFSS)

Those S-parameters can be traduced in more expressive parameters as explained in [**1**]. The primary L_p and secondary L_s effective inductances can actually be calculated from the Z-parameters (see Annex D for S to Z parameters conversion) using the relation (F.1).

$$L_p = \mathrm{Im}(Z_{11})/\omega \;;\; L_s = \mathrm{Im}(Z_{22})/\omega \tag{F.1}$$

The quality factor of each winding Q_p and Q_s are given by the relation (F.2). It corresponds to the ratio between the net magnetic energy stored in the device and its associated loss.

$$Q_p = \mathrm{Im}(Z_{11})/\mathrm{Re}(Z_{11}) \;;\; Q_s = \mathrm{Im}(Z_{22})/\mathrm{Re}(Z_{22}) \tag{F.2}$$

The k_{im} and k_{re} parameters given by the relation (F.3) correspond to the imaginary and real terms of the mutual coupling factor [**2**].

$$k_{im} = \sqrt{\frac{\mathrm{Im}(Z_{12}).\mathrm{Im}(Z_{21})}{\mathrm{Im}(Z_{11}).\mathrm{Im}(Z_{22})}} \;;\; k_{re} = \sqrt{\frac{\mathrm{Re}(Z_{12}).\mathrm{Re}(Z_{21})}{\mathrm{Re}(Z_{11}).\mathrm{Re}(Z_{22})}} \tag{F.3}$$

Finally the minimum insertion loss IL_m is calculated following the relation (F.4). It corresponds to a kind of figure of merit for the transformers [**1**].

$$IL_m = -10.\log\left(1+2.\left(x-\sqrt{x^2+x}\right)\right) \;;\; \text{where: } x = \frac{1-k_{re}{}^2}{k_{im}{}^2.Q_p.Q_s + K_{re}{}^2} \tag{F.4}$$

Figure F-5 shows the primary and secondary inductances (L_p and L_s; on the top left graph) and quality factors (Q_p and Q_s; on the top right graph), the imaginary and real terms of the mutual coupling factor (k_{im} and k_{re}; on the bottom left graph) and the minimum insertion loss (IL_m; on the bottom right graph) that have been extracted from the simulated S-parameters.

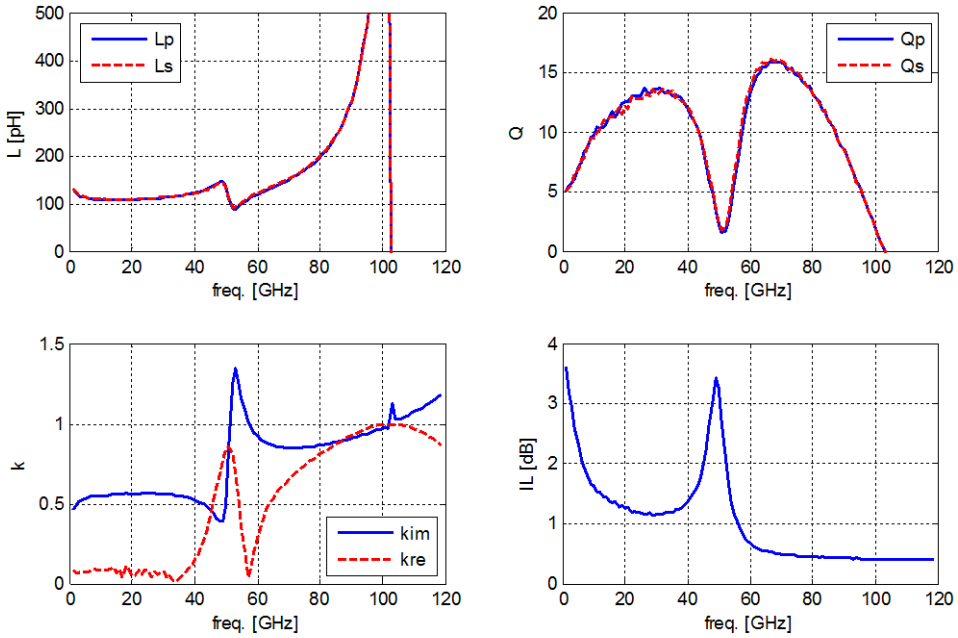


Figure F-5 Extracted inductances, quality factors, coupling factors and insersion loss of the balun

Although the primary and the secondary windings are not built in the same metal layer, their effective inductances are similar. So are their quality factors. There is a kind of "anti-resonance" around 50GHz as the quality factors decrease drastically and the insertion loss increase up to 3.5dB. This "anti-resonance" is characteristic of the flipped configuration of the transformer [**1**]. This transformer presents at 60GHz a 0.6dB minimum insertion loss.

F.1.4. Pads

The chip has two mmW ports on the east and west sides (for 60GHz signals), one RF port on the south side (for the buffer output), and a DC port on the north side. This ports distribution, illustrated in Figure F-1, is set to be compliant with measurement benches.

The mmW and RF ports are designed for ground-signal-ground probes (GSG) with a 100µm pitch. The DC port is composed of 4 pads designed for a DC probing rake with a 100µm out pitch. The DC pads are attributed, from the left to the right, to the detector biasing voltage, the ground, the detector supply voltage and the buffer supply voltage. The two supply voltages have been separated to be able to sense the power consumption separately on the power detector and on the buffer.

The chip is pad-limited as its size is determined by the integration of the 13 pads (3 GSG and 4 DC). The length of the transmission line integrated between the two baluns is directly a function of the circuit size.

Electrostatic discharge (ESD) protections have been integrated to the pads that could be sensible to those destructive effects. The RF port, which is connected to the buffer output, is directly connected to the drain of MOS transistors and has hence been protected by two diodes (0.5 x 15µm² MOS transistors connected in diodes), one with respect to the circuit ground, the second to the buffer supply voltage. The 3 DC voltages have also been protected against ESD by a single diode (0.5 x 15µm² MOS transistor connected in diode) with respect to the circuit ground. The mmW ports do not require any ESD protection as they are connected to active components through baluns and capacitive couplers that isolate the DC voltages.

F.2. Test structures

Figure F-6 shows the layout of the full chip called PowDet60G including the power detector circuit presented before (circuit a. on the top left corner) and some test structures. The test structures are needed to separately characterize the passive components and hence to calculate the measurement performances of the power couplers and detector independently of the measurement artifacts (see Annex G for details on de-embedding techniques). Some backup solutions have also been integrated in case of a dysfunction or a design error on the main chip.

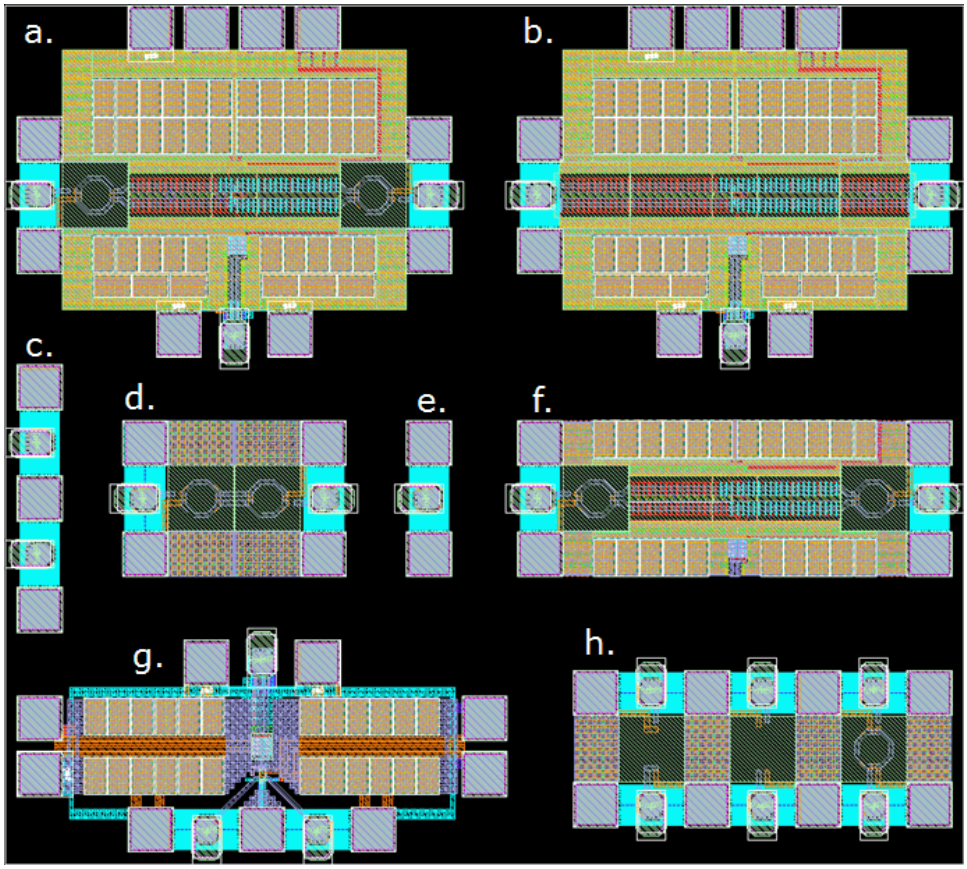


Figure F-6 Layout of the full circuit PowDet60G

F.2.1. Pads

The first structure needed for de-embedding is the interface between the circuit and the output world: the pads. Circuits e. and c. in Figure F-6 are respectively single-ended and differential millimeter-wave pads. The GSG and GSGSG (ground-signal-ground-signal-ground for differential probe) – see section F.1.4 for more details – are simply inserted without any additional connection resulting in open circuits.

The capacitive effect of the pads is deduced from the reflective S_{11} parameter measurements. This capacitive pad contribution being known, it can be subtracted from the other measurements to characterize the desired circuit without taking into account the unwanted effect of the pads (Annex G).

F.2.2. Single-ended balun

The second element which presents an unwanted effect on the RF path is the balun which is used for single-ended to differential conversion as explained in section F.1.3. However the characterization of such block requires a calibration procedure during which the accesses to the device under test (DUT) are subtracted. To properly remove the accesses effects, a short and an open

structures have been integrated in addition to the desired balun DUT (see Annex G for details on de-embedding techniques). Figure F-7 shows the layout implementation of those three structures. Note that the ground pads and connections are reused from one structure to the following one. This solution permits to characterize each structure using GSG probes while optimizing the total surface used for the balun characterization.

Figure F-7 is an enlargement of Figure F-6.h and shows the balun characterization circuit.

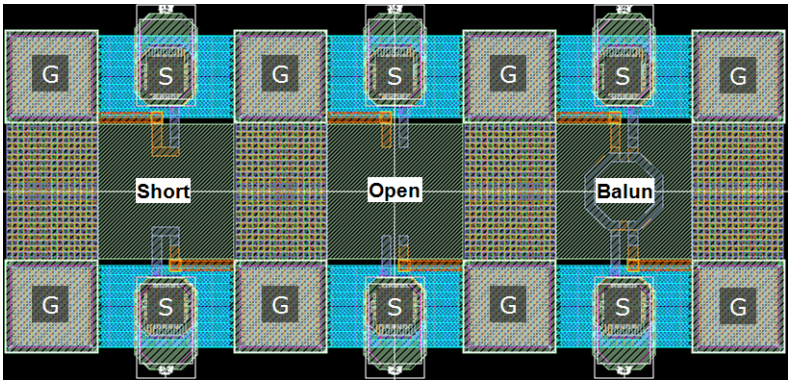


Figure F-7 Single-ended balun and de-embedding structures

F.2.3. Differential balun

The structure presented in the previous section permits to characterize the balun in a 2-port configuration which corresponds to a single-ended to single-ended use of the transformer. However the structure used in the power detector circuit includes two baluns with a differential current circulation in the internal loop. Figure F-8 shows the synoptic of a differential structure including two baluns as in the power detector circuit. The two baluns have to be connected in a way to ensure a good current circulation in the internal loop. This structure is integrated to the PowDet60G chip and its layout corresponds to the circuit d. of Figure F-6.

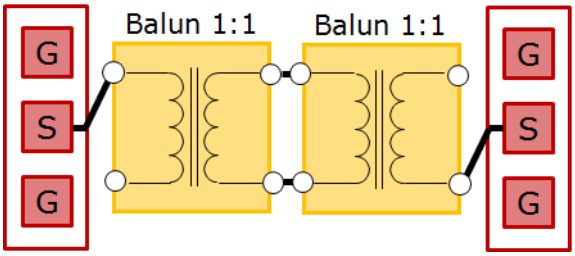


Figure F-8 Synoptic of the differential baluns

F.2.4. T-line and single-ended version of the power detector

The power detector circuit then integrates a differential transmission line on the RF path. This transmission line can be characterized in two different configurations. First using the structure f. of Figure F-6 which presents a similar RF path to the one of the power detector circuit except the capacitive couplers which have both been removed. The influence of the capacitive couplers on the RF-path can hence be measured.

The second way to characterize the T-line consists in considering a negligible effect of the capacitive coupler and to use the structure b. of Figure F-6. This structure is a single-ended version of the power detector. As a result there is only one capacitive coupler which is integrated and the T-line is hence single-ended (one of the two T-lines that composed the differential T-line is connected to the ground at both ends). Furthermore, no balun is necessary and none has been implemented; the structure is hence balun-free, which is a backup solution in case of an issue with the baluns.

F.2.5. Power detector in stand-alone

Finally, another backup solution has been integrated in the PowDet60G chip and is shown in Figure F-6.g. To overcome any simulation issue with the passive components, the baluns, the transmission line and the capacitive coupler have purely been removed. Only the detector is present in this circuit.

However this backup solution has huge limitations. Although the impedance matching is key for a good characterization of a power detector, it is not achievable in this implementation. This circuit also requires a differential probe that is rather unusual at millimeter-wave frequencies.

So even if the detector only should give very interesting information, the measurement process is very complex and might not give the expected results. This solution will be used only in the unlikely event of a major issue with the passive components.

F.3. Die photograph

Figure F-9 shows the die photograph of the full circuit including the different structures presented in the previous section following the disposition presented in Figure F-6. This circuit called PowDet60G occupies 1720µm per 1540µm.

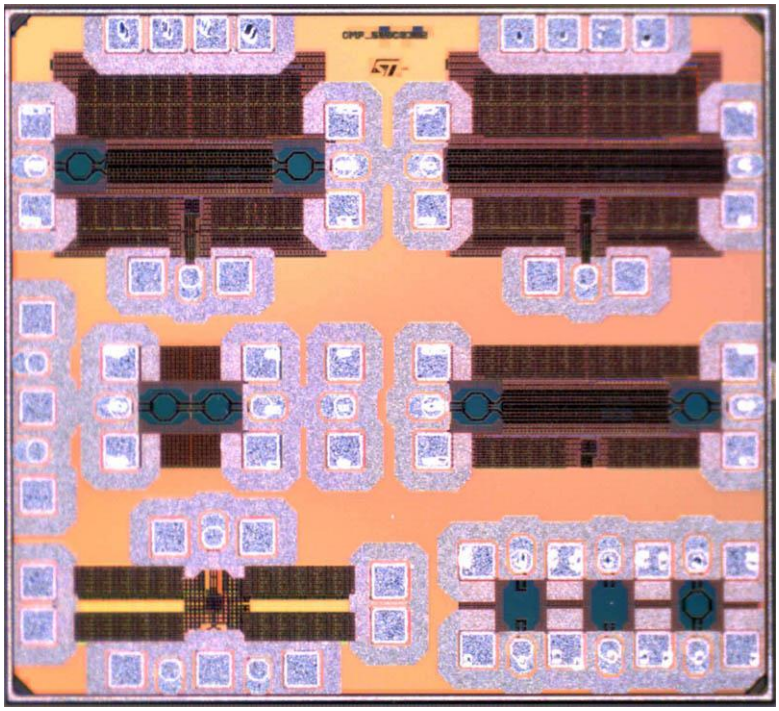


Figure F-9 Die photograph of the full circuit PowDet60G

References

[1] B. Leite, E. Kerhervé, J.-B. Bégueret, and D. Belot, "Transformer topologies for mmW integrated circuits," in *IEEE Proceedings of the 39th European Microwave Conference (EuMC)*, Rome, Italy, Sep. 2009, pp. 181-184.

[2] O. El-Gharniti, E. Kerhervé, and J.-B. Bégueret, "Characterization of Si-based monolithic transformers with patterned ground shield," in *IEEE Radio Frequency Integrated Circuits (RFIC 2006) Symposium*, San Francisco, CA, USA, Jun. 2006, pp. 261-264.

Annex G. De-embedding techniques

Overview

Circuits which are not targeted to be used in standalone mode often need to be characterized with some additional components requested by measurement considerations. This is notably the case of our 1st circuit implementation, PowDet60G, which targets to characterize power couplers and power detectors (see section II.3). Some components such as the pads, the balun and the buffer, have actually been added to facilitate the measurements (see Annex F).

However, all those additional components are not part of the circuit to be characterized. Some de-embedding techniques have hence to be used in order to extract the desired characteristics of the Device-Under-Test (DUT) from the raw measurements. This annex aims to presents some of those de-embedding techniques.

The theory on de-embedding techniques is first presented. Then, the Open-Short and Short-Open techniques are applied to the balun of the circuit PowDet60G. The final section of this annex presents a specific test configuration where some particular de-embedding techniques have to be implemented.

Outline

G.1. De-embedding theory

G.1.1. Overview

The small signal characteristics of passive devices are obtained by performing S-parameters measurements using a network analyzer. The network analyzer has been beforehand calibrated. This calibration is performed on a reference substrate with low resistive gold contacts which are taken into consideration during the calibration phase to be not erroneously considered during the measurement phase. The Programmable Network Analyzer (PNA) gives hence S-parameters de-embedded in the plane of the probes which means that every parasitic effect of the measurement equipment including the cables, the probes, and the VNA itself are taken into account.

However, some components such as the pads, the baluns and the transmission lines have been added in order to be able to perform the measurements of the power detection circuit (see Annex F for details on the components which have been added for the testability of PowDet60G). And the parasitic effects of those components are not automatically subtracted by the PNA. This is not a problem when considering a complete circuit that will always be used including the pads, but those effects are not considered as part of the final circuit here and should hence be removed by some calculation to obtain the S-parameters of the useful part of the circuit, thus placing the reference plane directly at the input and output of the DUT, as illustrated in Figure G-1.

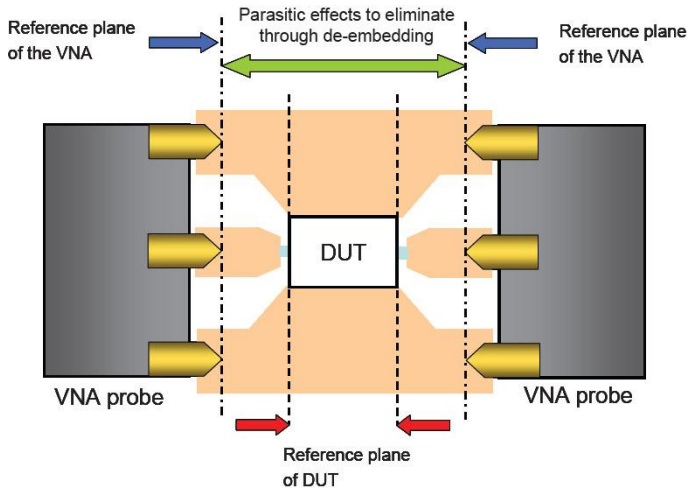


Figure G-1 Measurement configuration and de-embedding consideration [1]

G.1.2. Open pad

As an example, we have measured the reflection coefficient on a single-ended pad that should ideally be a perfect open circuit. The measured reflection coefficient S_{11} is plotted on the Smith chart at Figure G-2 (left).

The pad effectively presents an ideal open circuit for DC signals, but the infinite impedance presented for a DC signal progressively decreases when the frequency of the signal increases, thus reaching the value *3.7 -29.7xj* for a 67GHz signal which is far from the ideal infinite impedance. The pad can actually be modeled by a capacity in parallel with a resistance, which globally corresponds to the physical phenomenon where the metal plane formed by the RF contact creates a capacity with respect to the grounded substrate (the oxide between the two capacitance terminals always presents a certain resistivity).

Figure G-2 (right) shows the capacitance value that is extracted by the single-ended pad measurements. The measurements have been performed for 3 different chips with similar results around 80fF from DC up to 67GHz.

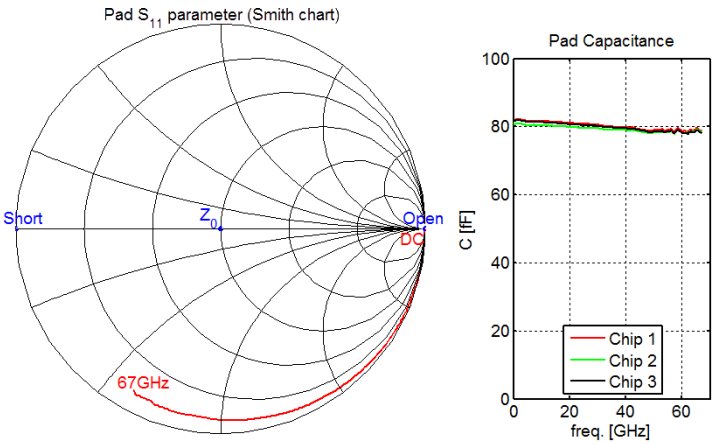


Figure G-2 Pad measurements: S_{11} parameter on Smith chart (left) and extracted pad capacitance (right)

The effects of the pads can hence be de-embedded quite easily, simply by considering they work as additional parallel impedances at the inputs of the circuit with no serial component. The S-parameters of the useful circuit, called Device Under Test (DUT) in the following equations, can be deduced from the T-parameters (following the rules detailed in Annex D) calculated from the measured T-parameters T_{MEAS} following the equation (G.1), where T_P stands for the T-parameters of the pad.

$$T_{DUT} = T_P^{-1}.T_{MEAS}.T_P^{-1} \tag{G.1}$$

The T-parameters of the pad are deduced from the 2-port network S-parameters of the pad S_{pad_2port} which are calculated from S_{pad}, the 1-port network S-parameter measurements of the pad (see above), following the equation (G.2).

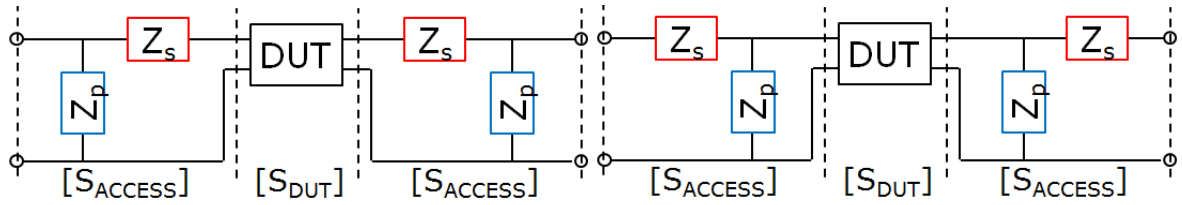
$$S_{pad\_2port} = \begin{bmatrix} \frac{-(1-S_{pad})}{(3+S_{pad})} & \frac{2(1+S_{pad})}{(3+S_{pad})} \\ \frac{2(1+S_{pad})}{(3+S_{pad})} & \frac{-(1-S_{pad})}{(3+S_{pad})} \end{bmatrix} \tag{G.2}$$

However, this de-embedding technique only subtracts the effect of the pad, seen as a parallel impedance on both sides of the DUT. The serial access from the pad to the DUT is not taken into consideration. This technique is hence rarely used at millimeter-wave frequencies as the size of the pad itself is non-negligible in comparison to the signal wave-length, thus resulting in a serial component that has to be taken into consideration in addition to the parallel impedance previously introduced.

G.1.3. Open-Short & Short-Open

Some other techniques have been developed that consider a combination of serial and parallel elements on both sides of the DUT [**1**]. Some additional structures are required to use those de-embedding techniques. First, the structure called “open” includes the pads and the access to the DUT in exactly the same configuration that the circuit to be measured, but here, the DUT itself is removed resulting in an open circuit. The second structure, called “short” is similar to the previous open structure at the difference that the DUT is replaced this time by a short circuit between the two ports and also with respect to the ground reference. Some additional structure such as the “thru” (the DUT is replaced by a reference impedance transmission line) can also be implemented resulting in more precise de-embedded results. However, only the open and short structures have been implemented. This should provide sufficient precision for this work and the integration of additional structures result in extra cost of silicon. Those de-embedding structures are illustrated in Figure F-7.

The short and open structures have been measured that generate two S-parameters data files S_{SHORT} and S_{OPEN} (respectively) which can be easily converted into Y or Z-parameters (see Annex D). However several de-embedding techniques are based on those two structures that generate different results. Once can actually easily understand that by subtracting the effects of the short and the open one before the other, the calculated result will be different. In fact, the de-embedding technique is linked to the modeling consideration that is made to progressively remove the serial and parallel effects of the pads and the access to the DUT.



a. Open-Short **b. Short-Open**

Figure G-3 Open-Short and Short-Open de-embedding model configurations

The first technique, known as "open-short", is based on the model for the parasitic access devices that is illustrated in Figure G-3.a. The accesses to the DUT is hence considered as first a parallel component that can correspond to a pad as an example, and then serial component that can correspond to the metal connection between the pad and the DUT. Mathematically, equation (G.3) describes this de-embedding technique. Y_{DUT} and Y_{MEAS} respectively stand for the DUT Y-parameters (wanted results) and the measured Y-parameters. By this technique, the effect of the open is subtracted before the effect of the short.

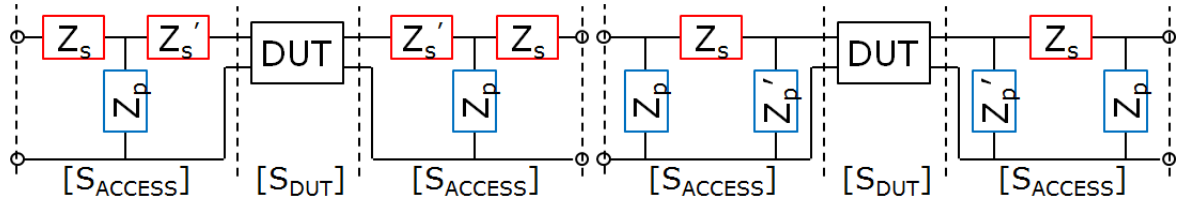
$$Y_{DUT} = \left(\left(Y_{MEAS} - Y_{OPEN} \right)^{-1} - \left(Y_{SHORT} - Y_{OPEN} \right)^{-1} \right)^{-1} \quad \text{(G.3)}$$

The opposite operation can also be made, thus subtracting the effect of the short before the effect of the open. This technique is hence logically called "short-open". This time, the serial component is considered to be before the parallel component, thus following the model of Figure G-3.b. Mathematically, the Y-parameters of the DUT Y_{DUT} is given by the equation (G.4) that computes the measured, the short and the open Z-parameters, respectively Z_{MEAS}, Z_{SHORT} and Z_{OPEN}.

$$Y_{DUT} = \left(Z_{MEAS} - Z_{SHORT} \right)^{-1} - \left(Z_{OPEN} - Z_{SHORT} \right)^{-1} \quad \text{(G.4)}$$

G.1.4. Corrected Open-Short & corrected Short-Open

A better solution consists in using the two sets of measurements to assess the parameters of a T or Π network [**1**] [**2**]. These two models are called respectively "Corrected Short-Open" (or Short-Open-Short) and "Corrected Open-Short" and are illustrated in Figure G-4.



a. Corrected Short-Open **b. Corrected Open-Short**

Figure G-4 Corrected de-embedding model configurations

Mathematically, the Y-parameters of the DUT Y_{DUT} is a combination between the $Y_{DUT\_OPEN-SHORT}$ and $Y_{DUT\_SHORT-OPEN}$ obtained respectively by applying the equations (G.3) and (G.4), and is given by the equation (G.5) when considering the Corrected Short-Open technique.

$$Y_{DUT} = \left[(1 - Cs).Y_{DUT\_OPEN-SHORT} + Cs.Y_{DUT\_SHORT-OPEN} \right] \quad \text{(G.5)}$$

The Corrected Open-Short technique directly uses the measurement, the open and the short Y-parameters as can be seen in the equation (G.6).

$$Y_{DUT} = \left(\left(Y_{MEAS} - Cp.Y_{OPEN} \right)^{-1} - \left(Y_{SHORT} - Cp.Y_{OPEN} \right)^{-1} \right)^{-1} - (1 - Cp).Y_{OPEN} \quad \text{(G.6)}$$

The correction factors *Cs* and *Cp* can be evaluated manually as they correspond to the repartition between the two serial or the two parallel components. But both can also be calculated following the equation (G.7). However those calculus need two additional de-embedding structures as the short or the open is applied directly on the pad or after the access (just replacing the DUT). Those structures have not been implemented here for chip size considerations.

$$Cs = \left(\frac{\mathrm{Im}\left(Z_{11}^{\ access-short} \right)}{\mathrm{Im}\left(Z_{11}^{\ pad-short} \right)} + 1 \right)^{-1} \quad Cp = \left(\frac{\mathrm{Im}\left(Y_{11}^{\ access-open} \right)}{\mathrm{Im}\left(Y_{11}^{\ pad-open} \right)} \right)^{-1} \quad \text{(G.7)}$$

G.2. Application to the balun circuits in PowDet60G

G.2.1. Single-ended balun circuit

Having now the methodology to de-embed the measurement results, we can characterize the single-ended balun structure integrated in PowDet60G (see Figure F-7). This balun uses similar access – one RF pad and a small serial metal access – that the open and short structures. The open-short and short-open de-embedding techniques can hence be applied directly.

Figure G-5 shows the S_{11} and S_{21} parameters that are directly extracted from the measurements (plain line) and that are de-embedded using the open-short (dashed line) and short-open (dotted line) techniques. The first observation that can be made is the high difference level between the original measurement results and the two de-embedded results, especially considering the S_{11} parameter. This indicates that the pads and the serial access have a huge impact on the global circuit characteristics.

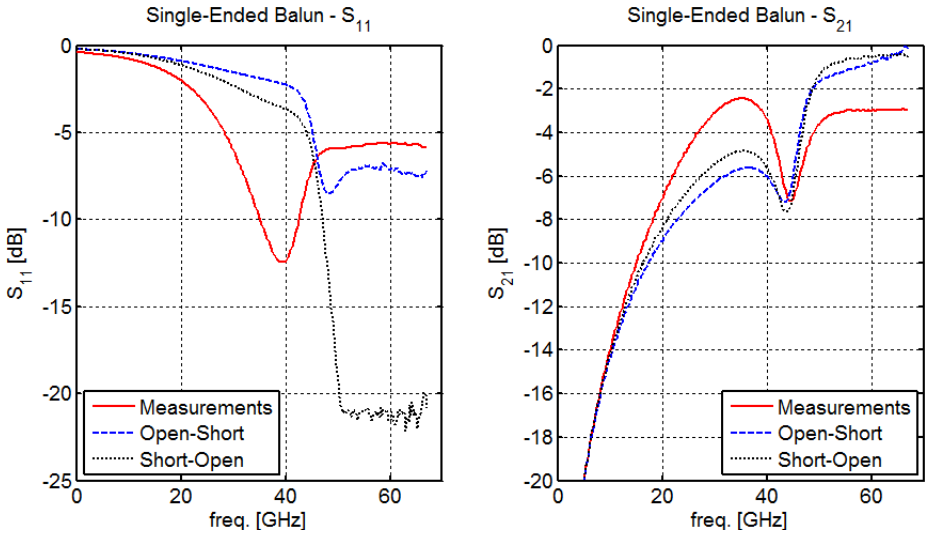


Figure G-5 Single-Ended balun S_{11} and S_{21} parameters; measurements and de-embedded results

Although the two de-embedding techniques generate same range results below 45GHz, the difference becomes very high above 45GHz, the S_{11} parameter reaching -7dB at 60GHz considering the open-short technique, and -22dB considering the short-open technique. In fact, the measured structure resonates at around 40GHz as the S_{11} parameter is below -10dB meaning the structure is quite matched to 50Ω. Above this resonance frequency no de-embedding technique can be applied correctly and the results of both open-short and short-open de-embedding are no more valuable above 40GHz. This explained the high difference level between the two de-embedding techniques.

Considering now the structure of the access to the balun, the probe is applied on the pad that acts as a parallel component (mainly a capacitor as explained above), a metal rectangle then connects the pad to the DUT – the balun here – that works as a serial component (resistance & inductance). The model that best fit this configuration is hence the Open-Short of Figure G-3.a. The Open-Short de-embedding technique will hence be preferred in this situation.

G.2.2. Differential balun circuit

The Open-Short technique is also the best de-embedding one when considering the differential balun circuit presented in Figure F-8. Figure G-6 shows the measured and de-embedded (Open-Short) results of this differential balun structure.

After being de-embedded, the differential balun structure resonates at 45GHz and presents a 4GHz bandwidth on which the input is well matched to 50Ω (S_{11} below -10dB). At the resonance frequency, the structure presents a -2.8dB attenuation coefficient between the input and the output (S_{21}). Hence, a circulation loop between the two baluns has effectively been created that is totally isolated with respect to the input and the output of the circuit, as explained in Figure F-8. The structure can hence convert a single-ended signal into a differential one before converted it back in single-ended mode. This test confirms the functionality of the complete structure including the power couplers integrated inside a differential transmission line between the two baluns.

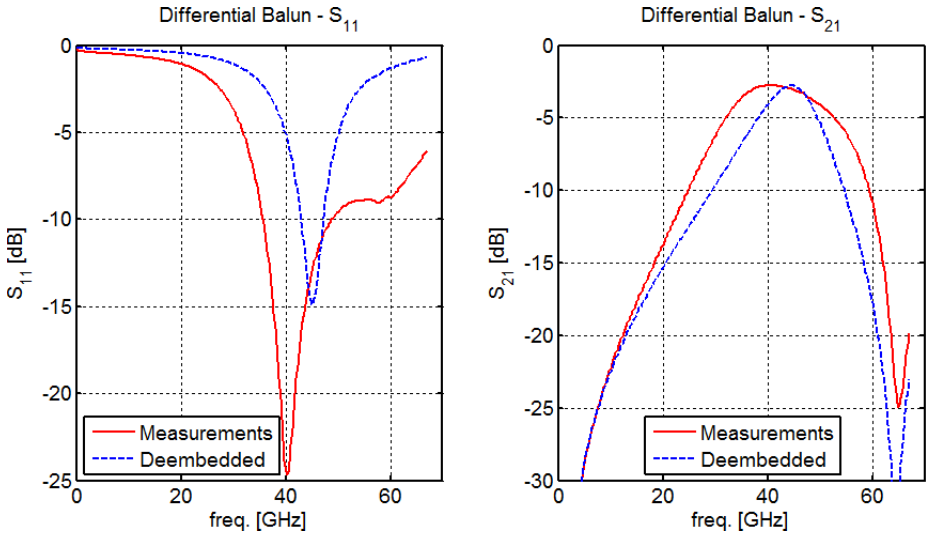


Figure G-6 Differential balun S_{11} and S_{21} parameters; measurements and Open-Short de-embedded results

G.3. Power-sweep configuration de-embedding

In order to characterize the power detector behavior of the circuit PowDet60G (see Figure II-41), power sweeps are applied on the transmission line input. A careful de-embedding procedure is required on the raw measurement data in order to obtain the measured detector output voltage with respect to the actual power in a vertical plane on the top of the coupler metal square.

G.3.1. Experimental configuration

A 60GHz programmable signal generator (PSG) is connected to the mmW input of the circuit while the mmW output is loaded by a 50Ω impedance. The DC power is provided by a voltage generator and sent to the DUT via an adequate 4-pins probe. Finally, the detector output voltage is probed on the 4th circuit port and displayed on an oscilloscope. This measurement configuration is illustrated in Figure G-7.

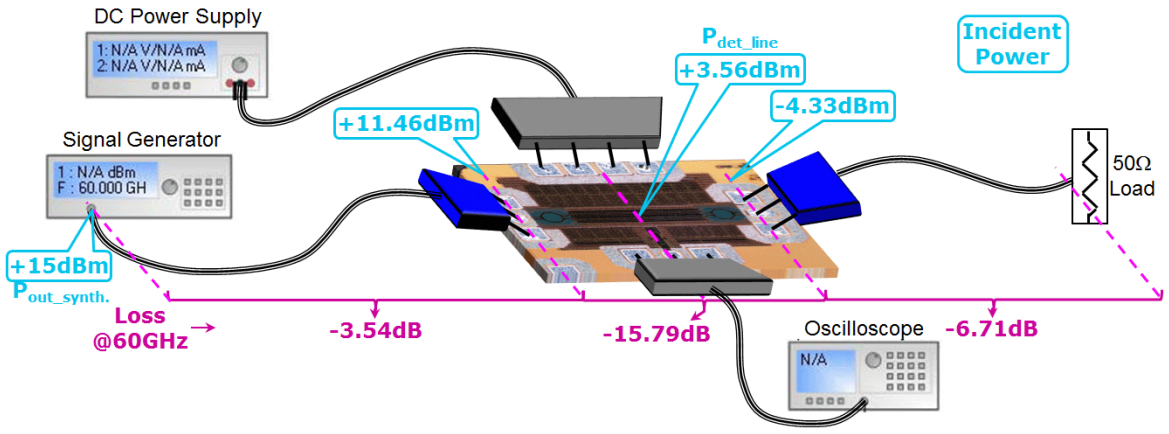


Figure G-7 Differential detector: power measurement test bench

However all those equipment and cables are not ideal and present some attenuation at mmW frequencies which are not automatically de-embedded. All those losses have to be considered and de-embedded in order to obtain the correct power characteristics of the circuit.

G.3.2. Cables & probes

Two RF cables have been used during those measurements: a short one that connects the signal generator to the circuit; and a long one that connects the circuit to the 50Ω load impedance. Those two cables have been measured with the probes in terms of small-signal S-parameters. The measured attenuation coefficients (S_{21} parameter) are shown in Figure G-8. The short and long cables associated to their probes present respectively -3.54dB and -6.71dB insertion loss at 60GHz. The short cable – only one was available in the laboratory – has hence been placed at the input of the circuit to maximize the power sent to the DUT.

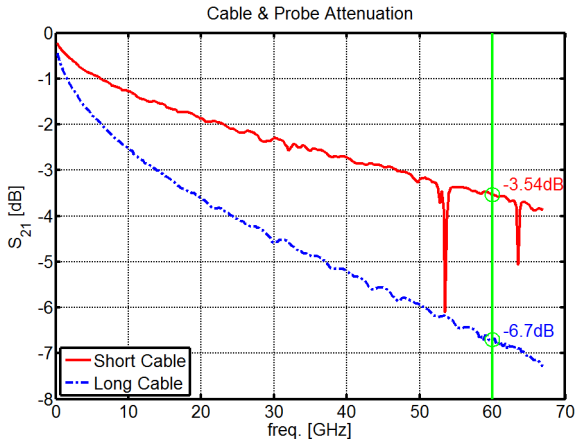


Figure G-8 Short and long cables attenuation

G.3.3. De-embedding calculation

In addition to those equipment attenuations, the small-signal attenuation coefficient of the circuit itself has to be considered. As already discussed, the pads, the baluns and even the transmission line are actually not part of the circuit that we want to characterize here and their contribution has to be removed. The mmW signal path between the input and the output of the circuit including only passive devices, the small-signal S_{21} parameter can directly be used as large-signal insertion loss which is at 60GHz -15.79dB for the differential circuit and -6.67dB for the single-ended one.

To calculate the power level in a vertical plane on the top of the coupler metal square, we consider that the insertion losses are equally dispatched on the two halves of the circuit as the structure is fully symmetrical, the coupler being precisely placed at the center of the mmW part of the circuit.

This assumption is not totally true when considering the possibility that some reflection waves could appear due to the impedance mismatch between the transmission-line and the baluns, thus resulting in a detected power that corresponds not exclusively to the incident wave. However this is the best approximation that we can make as we cannot measure this impedance mismatch inside the chip.

As a conclusion, the power delivered in the T-line in a vertical plane on the top of the coupler metal square, noted P_{det_line}, can be evaluated from the synthesizer output power P_{out_synth} following the equation (G.8) for the differential power detector circuit.

$$P_{\det\_line} = P_{out\_synth} - 11.43dB \quad \text{(G.8)}$$

The different insertion loss contributions have been reported on the bottom of Figure G-7 while an example of power level at different locations of the measurement configuration have been reported on the top of the same figure (the circled values). Considering a +15dBm generated signal at 60GHz, the power coupler receives only +3.56dBm.

The same de-embedding operation is performed on the single-ended power detector circuit. However the small-signal S_{21} parameter value being quite lower than previously, the resulting power level seen by the power coupler is much higher. Still considering a +15dBm generated signal at 60GHz, the power coupler receives +8.125dBm this time. The equation (G.8) hence becomes the equation (G.9).

$$P_{\det\_line} = P_{out\_synth} - 6.87dB \quad \text{(G.9)}$$

G.3.4. Signal Generator

Moreover, the generated power that is indicated on the signal generator is not regulated in real-time inside the equipment and the true generated power that is effectively sent to the circuit is quite different to the power level that is displayed on the generator. A correspondence table between those two power levels has hence to be built to be able to calculate the effected power that is detected by the power detector circuit. Figure G-9 illustrates the insertion loss between the displayed power level and the effective power generated by the PSG. Those insertion losses are negligible for low power levels but reach -0.84dB for the maximal displayed PSG output power of +15dBm.

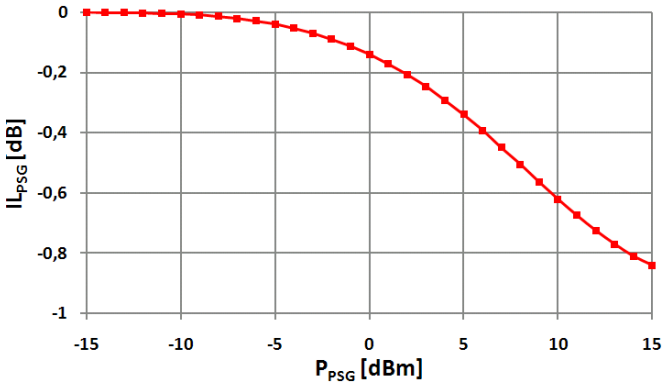


Figure G-9 Insertion loss versus displayed output power characteristic of the signal generator (PSG) at 60GHz

References

[1] B. Martineau, "Potentialités de la technologie CMOS 65nm SOI pour des applications sans fils en bande millimétrique," Ph.D. Thesis, Université des Sciences et Techniques de Lille, Lille, France, May 2008.

[2] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *IEEE Proceeding of the Bipolar Circuits and Technology Meeting (BCTM)*, Sep. 1991, pp. 188-191.

Abstract

With the emergence of mass-market applications, such as Wireless-HD, low-cost CMOS technologies are requested to democratize the use of mmW frequencies. However, before being commercialized, mmW transmitters have to ensure sufficient reliability. One major reliability issue lies in the impedance mismatch between the power amplifier (PA) and the antenna, which can result from wave propagation obstacles in the close vicinity of the antenna. Such impedance mismatch generates standing waves, which can cause irreversible damage on the power amplifier.

This thesis aims to propose an innovating regulation architecture that could protect the power amplifier from such deterioration and optimize its performance. By integrating several power detectors between the PA and the antenna, the impedance mismatch can be evaluated. Using this information, a digital regulation loop could then elaborate a complete strategy in order to optimize the PA performance. This thesis notably investigates the power detection circuits, which should sense the antenna impedance mismatch. A circuit realization in 65nm CMOS process from STMicroelectronics shows that the power detector provides 25dB dynamic range at 60GHz and is able to detect up to 3:1 VSWR. A second circuit realization integrates a power amplifier, the power detection circuits and data converters (ADC & DAC). The regulation loop acts on the power amplifier gain to keep a constant PA output power whatever the antenna impedance is. A second loop is also integrated, which protects the PA from destruction.

This thesis also covers two alternative projects developed simultaneously to the VSWR-regulated PA architecture. First, a novel architecture of Logarithmic-Analog-to-Digital-Converter is proposed, which is based on the progressive compression architecture of logarithmic amplifier. Then the simulation aspect of the VSWR-regulated PA is investigated through an ADS co-simulation of an RF/mmW PA with its mixed-signal regulation loop.

Key words: power amplifier, antenna mismatch, WiHD, 65nm CMOS, power detector, mixed signal regulation loop, logarithmic ADC, ADS co-simulation

Résumé

Avec l'apparition d'applications grand-public, comme le Wireless-HD, les fréquences millimétriques nécessitent l'utilisation de technologies CMOS faible coût. Cependant, avant d'être commercialisés, les transmetteurs mmW doivent être suffisamment résistants notamment à la désadaptation d'impédance entre l'amplificateur de puissance (AP) et l'antenne qui peut résulter d'un obstacle dans le champ proche de l'antenne. Une telle désadaptation d'impédance se traduit par l'apparition d'ondes stationnaires qui peuvent engendrer des dommages irrémédiables sur l'AP.

Cette thèse propose une architecture innovante de régulation qui vise à protéger l'AP de telles dégradations tout en optimisant ses performances. La désadaptation d'impédance peut être évaluée en intégrant plusieurs détecteurs de puissance entre l'AP et l'antenne. Une boucle de régulation numérique peut ensuite établir une stratégie d'optimisation des performances de l'AP. Cette thèse s'intéresse particulièrement aux circuits de détection de puissance qui captent la désadaptation d'impédance de l'antenne. Réalisé en technologie CMOS 65nm de STMicroelectronics, le détecteur de puissance présente 25dB de dynamique à 60GHz et est capable de détecter jusqu'à 3 :1 de TOS. Ces détecteurs de puissance ont ensuite été intégrés dans un second circuit avec un AP et des convertisseurs (CAN & CNA). Une boucle de régulation agissant sur le gain de l'AP permet ainsi de garder une puissance de sortie constante quelle que soit l'impédance d'antenne tandis qu'une seconde boucle protège l'AP de la destruction.

Cette thèse couvre également deux projets développés en parallèle de l'architecture de régulation de TOS. D'abord est proposée une nouvelle architecture de convertisseur analogique numérique logarithmique, basée sur l'architecture d'amplificateur logarithmique à compression progressive. Ensuite, une co-simulation sous ADS d'un AP RF/mmW avec sa boucle de régulation numérique permet de simuler l'AP à TOS régulé.