Study of Active Filters Topologies for Telecommunications Applications

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To the memory of my father

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You see, wire telegraphy is a kind of very, very long cat. You pull his tail in New York and his head is meowing in Los Angeles. Do you understand this? And radio operates exactly the same way: you send signals here; they receive them there. The only difference is that there is no cat.

Albert Einstein, 1879–1955

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By

Cristian ANDRIESEI

ABSTRACT

The scope of this thesis is to propose solutions to improve the performances of the CMOS transistor only simulated inductors (TOSI) aiming RF filtering applications. We are interested in TOSI architectures because they prove better performances than the classical g_m–C filters, being superior with respect to the number of transistors, power consumption, frequency capability and chip area. Furthermore, TOSI architectures have many potential applications in RF design.

In the general context of the multi–standard trend followed by wireless transceivers, TOSI based RF filters may offer the possibility of implementing reconfigurable devices. However, satisfying the telecommunications requirements is not an easy task therefore high order TOSI based filters should be implemented. Consequently, using good second order TOSI cells is a matter of the utmost importance and we propose a novel quality factor tuning principle which offers an almost independent tuning of self resonant frequency and quality factor for simulated inductors. An improved TOSI architecture with increased frequency capability is also reported.

Thesis Supervisors: Liviu Goraş, Farid Temcamani and Bruno Delacressonnière

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This thesis may have been written well enough, had sufficient number of relevant references, transmit interesting ideas and valuable information or maybe not but what this thesis has to prove is the intellectual maturity and design experience I have attained during this doctoral program and mandatory for any research based post doctoral activity (educational research or in industry). Consequently, I express first my acknowledgements to my Romanian adviser, Prof. Liviu Goraş, for his guidance, patience, effort, enthusiasm and support of any kind to create a perfect research climate while conducting the research activity. The same appreciation goes to the French advisers, Mr. Farid Temcamani and Bruno Delacressonnière for their guidance, valuable advices and effort in having this thesis finished.

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Abbreviations and Symbols

1G	First Generation Wireless Technology
3G	Third Generation Wireless Technology
3GPP	3rd Generation Partnership Project
4G	Fourth Generation Wireless Technology
AC	Alternating current
ADC	Analog–to–Digital Converter
AES	Advanced Encryption Standard
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone System
ASIC	Application–Specific Integrated Circuit
BAW	Bulk Acoustic Wave
BB	Baseband
BiCMOS	Bipolar CMOS
BOK	Bi–Orthogonal Keying
BPF	Bandpass Filter
BPSK	Bipolar PSK
CCK	Complementary code keying
CCO	Current controlled oscillator
CD	Common Drain
CDMA	Code division multiple access
CG	Common Gate
CMOS	Complementary metal–oxide semiconductor
CS	Common Source
DAC	Digital–to–Analog Converter
DCR	Direct Conversion Receiver
DC	Direct current
DCS	Digital Cellular Service
DECT	Digital Enhanced Cordless Telecommunications
DL	Downlink
DoD	Department of Defense
DPSK	Differential PSK
DQPSK	Differential QPSK
DSP	Digital Signal Processor
DSSS	Direct–sequence spread spectrum
EDGE	Enhanced Data rates for GSM Evolution
EGSM	Extended GSM
ESA	European Space Agency
ETACS	Extended Total Access Communication System
FCC	Federal Communications Commission
FDD	Frequency–division duplexing
FDMA	Frequency division multiple access
FDNR	Frequency Dependent Negative Resistance

FET	Field–effect transistor
FHSS	Frequency–Hopping Spread Spectrum
FM	Frequency Modulation
FPGA	Field–Programmable Gate Array
FSK	Frequency–Shift Keying
GaAs	Gallium arsenide
GFSK	Gaussian Frequency–Shift Keying
GIC	General Impedance Converter
GLONASS	Global Navigation Satellite System
GMSK	Gaussian MSK
GNSS	Global Navigation Satellite Systems
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global Systems for Mobile Communications
HPSK	Hybrid PSK
HSDPA	High–Speed Downlink Packet Access (3.5G)
IEEE	Institute of Electrical and Electronics Engineers
IM3	Third–Order Inter–Modulation
IMEC	Interuniversity Microelectronics Centre
IIP2	Second–order Intermodulation Intercept Point
IIP3	Third–order Input Intercept Point Third–order Intermodulation Intercept Point
IP3	Third–order Intercept Point
IF	Intermediate Frequency
IMT2000	International Mobile Telecommunications–2000
IS–95	Interim Standard 95 (cdmaOne)
ISM	Industrial, Scientific, and Medical
LAN	Local area network
LNA	Low noise amplifier
LO	Local Oscillator
M–BOK	M-ary BOK
MEMS	Micro–Electro–Mechanical Systems
MESFET	Metal Semiconductor FET
MIMO	Multiple-Input, Multiple-Output
MMIC	Monolithic Microwave Integrated Circuits
NF	Noise Figure
NIC	Negative Impedance Converter
NMOS	n-channel MOSFET
NMT	Nordic Mobile Telephony
NRZ	Non–return–to–zero
OFDM	Orthogonal frequency–division multiplexing
OFDMA	Orthogonal Frequency–Division Multiple Access
OQPSK	Offset QPSK
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PCS	Personal Communications System
PDC	Personal Digital Cellular
PMOS	p-channel MOSFET
PSK	Phase Shift Keying

QAM	Quadrature amplitude modulation
QPSK	Quadrature Phase Shift Keying
Rx	Receiver
SAW	Surface Acoustic Wave
SDD-AI	SourceDegenerated Differential Active Inductor
SDR	Software defined radio
SiGe	Silicon–germanium
SMR	Specialized mobile radio
SNR	Signal–to–noise ratio
TACS	Total Access Communication System
TAI	Tunable Active Inductor
TDD	Time Division Duplexing
TDM	Time Division Multiplexing
TDMA	Time Division Multiple Access
THD	Total Harmonic Distorsion
TOI	Third–order Intercept Point
TOSI	Transistor only simulated inductor
UL	Uplink
UMTS	Universal Mobile Telecommunications System
UWB	Ultra Wide Band
VCO	Voltage–controlled oscillator
VHF	Very High Frequency (30 MHz–300 MHz)
WCDMA	Wideband CDMA
WiMAX	Worldwide Interoperatibility for Microwave Access
WLAN	Wireless Local Area Network
WPAN	Wireless personal area network
WWiSE	World Wide Spectrum Efficiency

1. INTRODUCTION

1.1 Motivation

The telecommunications market requirements and continuous technology development impose a continuous research for both baseband and RF transceiver sides. During the last three decades, telecommunications transceivers evolved from entirely analog 1G terminals (AM and FM transmitters) to multistandard wireless devices with mixed digital baseband – analog front–end parts, the fourth generation (4G) being expected. On the transceiver side, the filtering part (active and passive) had an important contribution to the transceiver reconfigurability and smaller size. However, if the analog baseband filtering does not impose problems in implementing reconfigurable terminals, the RF passive filtering still represents a challenge. Thus, the surface acoustic wave (SAW) RF filters used in any wireless transceiver are external, bulky and offer no frequency tuning opportunity therefore, decreasing the customer satisfaction degree against size and device portability. Although SAW filters are cheap, the final cost for a multi–standard terminal is greatly increased since at least 8 such filters are used for different filtering operations. Many passive (MEMS), pseudo–passive (Q–enhanced LC) and active (g_m–C) solutions have been proposed until now in literature but no one can beat the excellent frequency performances offered by the SAW filters. A promising small size, low power entirely active implementation makes use of transistor only simulated inductors (TOSI) which have the main benefit of being reconfigurable devices. These architectures are addressed in this research.

1.2 Thesis Outline

The content of this thesis, presented in a very concise form, covers three different topics as follows.

Since filtering in telecommunications is envisaged, Chapter 2 is entirely dedicated to the telecommunications field. The first section is a brief description at basic level (due to size constraints) of telecommunications standards, covering frequencies up to 5 GHz. The interest in this regard are the frequency allocation and attenuation requirements for particular applications since these represent key aspects for the RF filtering design. Other

standard specifications regard different transceiver blocks, like the modulation scheme which becomes important for the power amplifier design but also the low noise amplifier. An overview of the wireless transceiver architectures is presented in the second section. Since hundreds of papers and tens of books have been reported in literature covering the transceiver architectures and design, an overview of RF transceivers is beyond the scope of this thesis. Only a concise, clear and up to date review of RF transceivers in a form that synthesizes the relevant information from a great number of sources but also describe the current multi–standard trend is given.

Chapter 3 covers the gyrator concept and is intended to be a 'state of the art' regarding the concept of 'transistor only simulated inductor'. All TOSI architectures reported in literature and mentioned in this thesis envisage applications in the GHz range thanks to their frequency capability. These capacitorless simulated inductors represent promising architectures for RF filtering applications and not only, since their successful use in implementing CCOs, LNAs and bandpass amplifiers has been reported in literature.

A more detailed insight into CMOS simulated inductors is provided in Chapter 4 where the TOSI frequency behavior is addressed. The main contributions for this research are presented in this final chapter.

A final conclusion is drawn at the end of this thesis in Chapter 5.

2. WIRELESS TELECOMMUNICATIONS STANDARDS AND RF TRANSCEIVERS

2.1 Introduction

In this introductory chapter, the most common wireless telecommunications standards in the frequency band up to 5 GHz are presented. Since a detailed presentation of each standard is beyond the scope of this thesis, more details can be found in the references. The reason of introducing this review chapter is that any engineering problem on RF transceivers design requires a corresponding insight on the telecommunications standard at least at basic level.

Two reasons imposed taking into consideration the frequency of 5 GHz as the maximum frequency:

1) The widest spread wireless implemented standards aiming civilian applications which represent also the most important part of the telecommunications market are represented by GSM/3G, WiMAX, WLAN and GPS applications, all operating in the lower microwave spectrum. The first UWB frequency band belongs to this spectrum too.

2) Much research has been devoted for developing different RF Front–ends, aiming the low frequency microwave applications. Thus, at least 350 papers submitted to different journals and conferences, dedicated to different wireless transceiver architectures, may be counted from 1990 to 2010.

The continuous expanding of the CMOS technology compared to other technologies (GaAs, SiGe) [2.1]…[2.5] due to its low cost, small size but also the increasing cut–off frequency, facilitated the implementation of high speed digital circuits and competitive RF CMOS circuits. However, this is not the case for higher frequencies, aiming radar applications (22–29 / 76.5 / 77–81 GHz), where RF CMOS technology is inferior to SiGe BiCMOS in terms of cut–off frequency and sensitivity to parasitics and layout configurations [2.6]. In any case, the continuous technology scaling will help CMOS technology to surpass these issues when it reaches the quantum limit, expected to be 2036 [2.7]. It is difficult to say how the RF circuits will be designed in twenty six years but if the software defined radio (SDR) becomes reality then a mixing between SDR and perhaps quantum computing may constitute an exciting transceiver.

Most papers proposed until now in the literature and dedicated to CMOS RF applications envisage frequencies up to 5 GHz (0.35 μm, 0.18 μm) but there are RF circuits implemented in smaller CMOS processes (130 nm, 95 nm, 65 nm) working at higher frequencies [2.8]…[2.13], as well. Through a careful design of the baseband part by implementing efficient algorithms (coding and modulation) to fulfill the system level design requirements in terms of SNR, fading and interference minimization, the RF analog part is also minimized [2.14]. An important contribution to the transceiver design is added by an efficient antennas system design that can simplify the overall circuit design (at circuit level) while improving the coverage and network capacity [2.15]…[2.18] (at system level). In other words, through a conjugate effort of telecommunications engineers and RF/analog designers, the transceivers performances are significantly improved and the path of truly inexpensive global multistandard terminals is opened.

Regarding the spectrum allocation, there are many differences between the frequencies bands allocated to the same standard over the world thus raising many problems when designing worldwide reconfigurable devices. The spectrum allocation in Europe for telecommunications applications is given in [2.19] being very difficult to be reproduced here due to its irregular allocation.

A very short review of wireless standards in the 5 GHz band is presented in the following sections together with a detailed overview of different transceiver architectures.

2.2 Telecommunications Standards and Frequency Allocation

2.2.1 2G/3G/4G Mobile Systems

The mobile telecommunications represent an important part of the telecommunications market with billions of users over the world (3 billions in 2008 and 4 billions in 2009) and even increasing benefits. They knew a continuous expanding history, beginning with the first generation analog system 1G, continuing with digital generation (2G) and achieving 3G nowadays thus opening the path for the future 4G networks. A brief review [2.20]…[2.22] of the spectrum allocation and parameters for 1G and 2G mobile implementations is presented in the following tables (Table 1 and 2).

While 2G systems were focused on voice data transmission only, the third generation 3G systems give the opportunity of simultaneous transfer of both voice (telephone call) and non–voice data while by offering low cost and high–speed Internet

services (WLAN) through mobile connectivity (downloading information, e–mail, instant messaging).

Parameter	C 450	NMT 450	NMT 900	TACS	ETACS	AMPS
Original country	Germany	Scandinavia	Scandinavia	GB	GB	USA
Standardized by	DBP Telecom			CRAG	CRAG	FCC
Introduced in	1985	1981	1986	1984		1983
Uplink [MHz]	450.3–454.74	453–457.5	890–915	890–915	872–905	824–849
Downlink [MHz]	461.3–465.74	463–467.5	935–960	935–960	917–950	869–894
Channel spacing [KHz]	20	25 (20)	25 (12.5)	25	25	30
Access method	FDMA	FDMA	FDMA	FDMA	FDMA	FDMA
Modulation	FM	FM	FM	FM	FM	FM
Cell diameter		15–40 km	2–20 km			

Table 1 Overview of analog cellular mobile radio (1G)

Standard	Digital cellular telephony (voice/data)	
	GSM	cdmaOne
Frequency Range (MHz)	GSM850 DL(869-894)-UL(824-849) GSM900 DL(935-960)-UL(890-915) GSM1800 (DCS) DL(1805-1880)-UL(1710-1785) GSM1900 (PCS) DL(1930-1990)-UL(1850-1910) PDC 800 DL(810-888)-UL(893-958) PDC1500 DL(1477-1501)-UL(1429-1453)	DL(869-894)-UL(824-849) DL(1930-1990)-UL(1850-1910)
Modulation	GMSK DQPSK (PDC) 8-PSK (EDGE only)	QPSK/OQPSK
Multiple access	TDMA/FDMA	CDMA/FDMA
Duplex (UL/DL)	FDD	FDD
Channel bandwidth	200 KHz / 25 KHz (PDC)	1.25 MHz
Peak data rate	14.4 kbit/s 53.6–114 kbit/s (GPRS) 384 kbit/s (EDGE)	14.4 kbit/s (IS-95-A) 115.2 kbit/s (IS-95-B)

Table 2 Overview of digital cellular mobile radio (2G)

The main supplementary services specific to 3G networks are: Mobile TV, Video Conferencing, Tele–medicine, Location Based Services and Video on Demand. The evolution of mobile technology from the second phase to the third one (with specifications regulated by IMT–2000), is represented by the chart given in Fig. 2.1 while the allocated spectrum is given in Table 3.

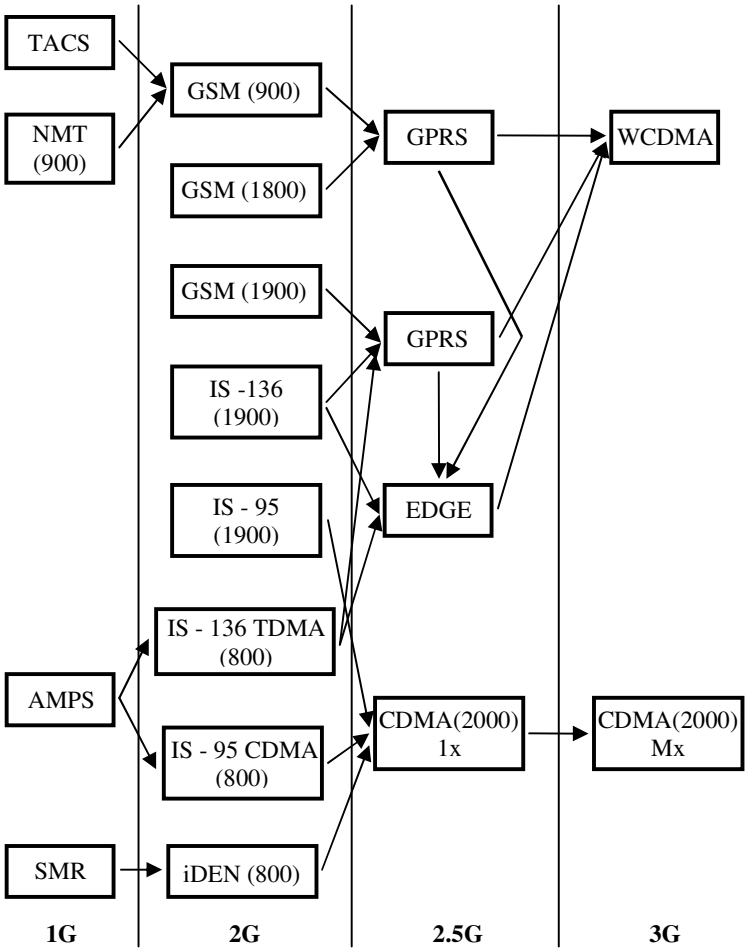


Fig. 2.1 IMT–2000 Specs

Standard	**Digital cellular telephony (voice/data)**		
	cdma2000	**WCDMA 3GPP/FDD**	**WCDMA 3GPP/TDD**
Frequency range (MHz)	450; 700 800; 900 1700; 1800 1900; 2100	DL(2110-2170);UL(1920-1990) DL(1930-1990);UL(1850-1910) DL(1805-1880);UL(1710-1785)	2010-2025 1900-1920 1930-1990 1850-1910 1910-1930
Modulation	QPSK, OQPSK HPSK	UL: Dual BPSK DL: QPSK, 16QAM	UL+DL: QPSK DL: 8PSK
Multiple access	CDMA	CDMA/FDMA	TDD
Duplex	FDD	FDD	FDD
Channel bandwidth	1.25 MHz	5 MHz	5 MHz
Peak data rate	307.7 kbit/s (CDMA2000 1x) 2.4 Mbit/s	2 Mbit/s 10 Mbit/s (HSDPA)	2 Mbit/s 10 Mbit/s (HSDPA)

Table 3 Overview of the most important 3G wireless standards

Different 3G bands (8 frequency bands) are regulated over the world a thing that makes the design of multistandard mobile terminals much more difficult. In Europe, the 2100 MHz (W–CDMA) frequency band is established as UMTS band, with 1920–1980 MHz for uplink and 2110–2170 MHz for downlink. The knowledge of these frequencies is of utmost importance when designing RF transceivers aiming 2G, 2.5G and 3G multistandard mobile terminals. It is obvious that regarding the RF filtering part for these mobile transceivers a large number of SAW RF preselective filters are used, with negative effects on the final product cost. Moreover, the out-of-band attenuation requirements in the case of mobile transceivers are more stringent than for other wireless standards. Beside the filtering issue, supplementary problems are rising on the transceiver part since different modulation schemes and power requirements are particular to each telecommunications standard with negative effects on the transmitter linearity, mainly in the case of the power amplifier. From this point of view, the practical design of a multistandard transceiver is by far not an easy task.

The frequency response of a SAW filter [2.23] satisfying the EGSM spectrum requirements for the frequency band 925–960 MHz (f_0=942.5 MHz) is shown in Fig. 2.2, not easy to obtain. Such frequency characteristic, not easy to obtain, should be envisaged if an active implementation is researched. The filter is 50Ω input and output matched. Other filtering solutions are presented in [2.24].

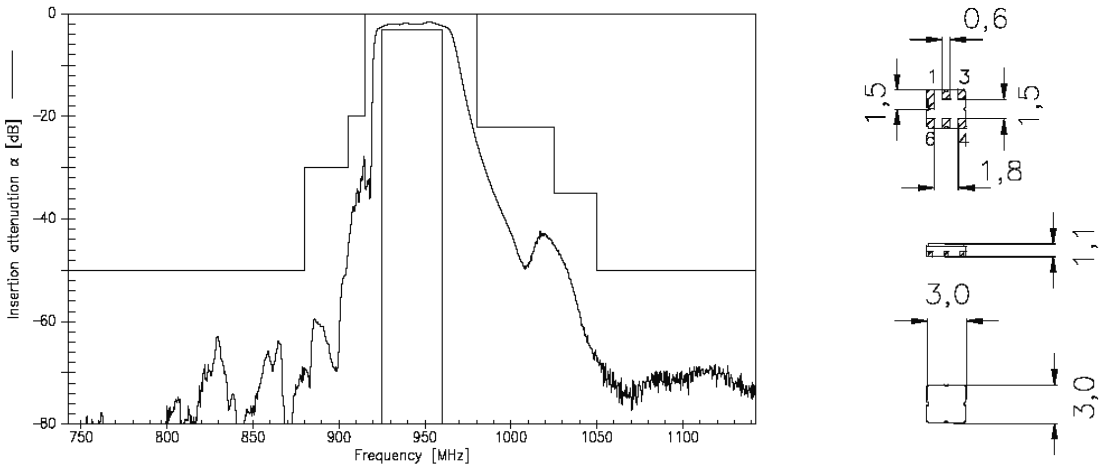


Fig. 2.2 B4141 SAW EGSM filter frequency response and chip size (mm) [2.23]

The frequency response of a SAW filter [2.24] satisfying the WCDMA spectrum requirements for the frequency band 2110–2170 MHz (f_0=2140 MHz) is shown in Fig. 2.3. The filter is single–ended 50Ω input matched and has balanced output (100 Ω).

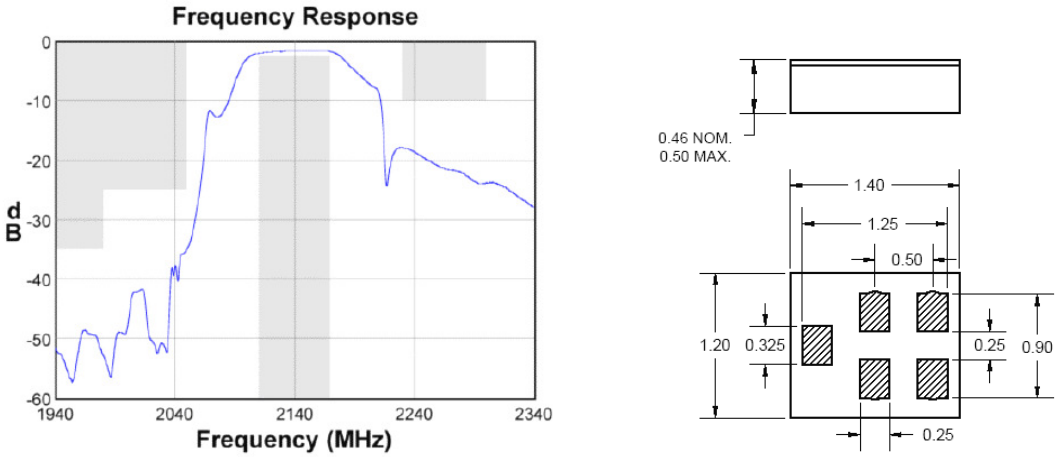


Fig. 2.3 856562 SAW WCDMA frequency response and chip size (mm) [2.24]

Design guidelines for SAW and BAW filters are given in [2.25] and [2.26] respectively.

2.2.2 Wireless LAN Standards (IEEE 802.11)

A **wireless LAN (WLAN)** is a telecommunications system that offers network service access to portable wireless devices using radio waves [2.27]…[2.32]. It consists of a network hardware backbone, along with a series of detached components, like computer desktops, computer laptops, personal digital assistants (PDAs), cell phones, security cameras, printers. This network can be deployed as a stand-alone network or together with a wired network. As any other wireless standard, being wired offers opportunities but has also drawbacks when talking about interference.

The WLAN technology is regulated by the IEEE 802.11 family of specifications established by the WLAN Group [2.27]. There are four implementations of the IEEE 802.11 wireless LAN Standard, each one evolving from the basic IEEE 802.11 specifications and being defined by its frequency band and modulation scheme. A short review of these modulations is presented in Table 4:

WLAN Standard	Year of Introduction	Frequency Band	Modulation Scheme	Maximum Data Rate
IEEE 802.11	1999	2.4 GHz	OFDM	1 – 2 Mb/s
IEEE 802.11a (USA) IEEE 802.11h (EU) IEEE 802.11j (JAP)	1999 2003 2004	5 GHz	OFDM	54 Mb/s
IEEE 802.11b	1999	2.4 GHz	DSSS/CCK	11 Mb/s
IEEE 802.11g	2003	2.4 GHz	DSSS/OFDM/CCK	54 Mb/s
IEEE 802.11n	Not ratified	2.4 / 5 GHz	MIMO - OFDM	540 Mb/s

Table 4 WLAN standard and its implemented amendments

When designing RF WLAN transceivers, the followings aspects must be taken into consideration:

a) the increasing demand for portable multistandard devices existent on the market;
b) a superior amendment (IEEE 802.11n) must support the inferior amendments;
c) the use of previous modulation scheme makes the practical design much easier;
d) multiple antennas (as in the case of IEEE 802.11n) strongly ameliorates the data rate (a supplementary antenna simply doubles the data rate);
e) OFDM modulation scheme makes difficult the transceiver design.

A throughout study of a WLAN multistandard transceiver designed to support IEEE 802.11a/b/g/n standards is presented in [2.31].

Finally, it is interesting to note that choosing a suitable topology for a wireless transceiver is not an easy task. Thus, regarding the last amendment (IEEE 802.11n), about 61 proposals have been submitted to IEEE but only two have been selected (from WWiSE and TGn Sync) [2.33]. The first scheme was able to transmit data at rates of 135 Mb/s while the second up to 315 Mb/s. No one has gained the majority voting support so that a mixing between all these proposed schemes was chosen for implementation. Devices supporting the IEEE 802.11n wireless network already appeared on the market.

The frequency response of a SAW filter satisfying the WLAN (IEEE 802.11 b/g) spectrum mask requirements for the frequency band 2400–2483.5 MHz (f_0=2441.75 MHz) is showed in Fig. 2.4. Much more relaxed attenuation requirements are required for WLAN applications than for mobile ones. This standard should be complied with when designing RF active filters.

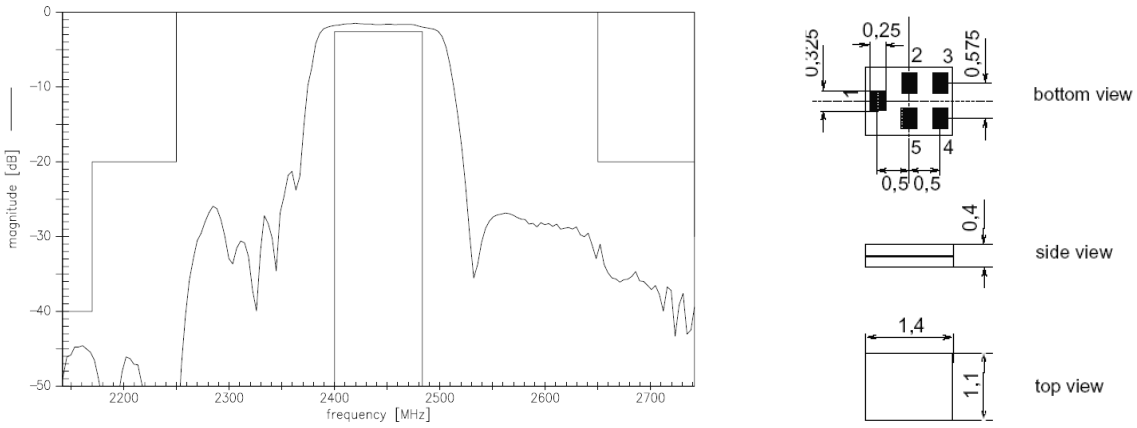


Fig. 2.4 B9410 SAW WLAN filter frequency response and chip size (mm) [2.23]

BAW RF filters are used for higher frequencies instead of SAW ones. The frequency response of a BAW filter satisfying the WLAN (IEEE 802.11a) spectrum mask

requirements for a centre frequency of 5775 MHz is shown in Fig. 2.5. The filter is 50Ω input and output matched. The filter occupies a significant chip area.

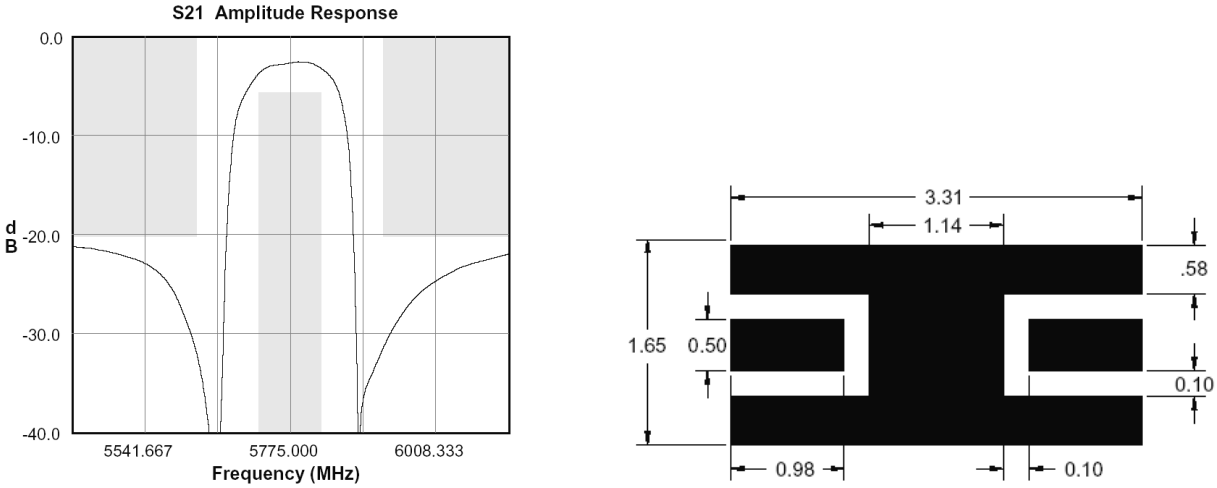


Fig. 2.5 880369 BAW WLAN filter transfer function and chip size (mm) [2.24]

2.2.3 Bluetooth Standard (IEEE 802.15.1)

Bluetooth is the name given to a telecommunication system that facilitates wireless communications between portable and/or fixed electronic devices [2.34]…[2.38]. From the very beginning the idea behind Bluetooth was to avoid cables for short range communications (less than 10 m). Working in the 2.4 GHz ISM band (2.4–2.4835 GHz), like WLAN devices (IEEE 802.11b/g), Bluetooth transceivers are designed to work in noisy environments due to the free interference FHSS frequency hoping scheme with low power and cost requirements. It is obvious that working in the ISM band, the main source of interference for Bluetooth systems is represented by the WLAN b/g transceivers. As in the case of the previously mentioned WLAN standard, Bluetooth knew a continuous development, as shown in Table 5:

Bluetooth Version	Year of Regulation	Frequency Band (GHz)	Modulation Scheme	Data Rate (Mb/s)
Core v1.0 [2.34]	Dec. 1999	2.4 – 2.4835 (EU*), USA) 2.471 – 2.497 (JAP) *) 2.445 – 2.475 (ESP) *) 2.446 – 2.4835 (FR)	GFSK	1 Ms/s[1)]
Core v2.0 +EDR [2.35]	Nov. 2004	2.4 GHz Band	GFSK[2)] π/4–DQPSK[3)] 8DPSK[3)]	1 2 3[4)]
Core v3.0	Apr. 2009	2.4 GHz Band	BR/EDR	1–3[5)]
Core v4.0	Dec. 2009	2.4 GHz Band	BR/EDR	1–3[6)]

Table 5 Bluetooth Standard Specifications

[1)] Practically max. 721 kb/s (v1.2)
[2)] Basic Rate (BR)
[3)] Enhanced Data Rate (EDR)
[4)] Practically max. 2.1 Mb/s
[5)] 24 Mb/s theoretical data rate by using WiFi – 802.11 resources [2.37]
[6)] 24 Mb/s theoretical data rate, low power devices (one year battery life) [2.38]

2.2.4 Zigbee Standard (IEEE 802.15.4)

Zigbee is a specification for high level short–range radio frequency communication protocols using small, simple, less expensive low power and data rate digital radios based on the IEEE 802.15.4 standard for WPAN. This standard aims to fit the market that is not filled by other wireless technologies. The standard specifications [2.39] have been regulated by ZigBee Alliance [2.40]. Instead of working in a single band as Bluetooth does, its spectrum is spread over three different frequencies, depending on local spectrum regulations: 2450 MHz band (16 channels – worldwide), 915 MHz band (10 channels – USA/Australia) and 869 MHz band (1 channel – EU). Until now only the highest regulated frequency was used but the standard is continuously expanding over the world. The spreading scheme is DSSS, BPSK is used for lower bands and OQPSK for 2.4 GHz band.

ZigBee products are used currently in different applications like:

- wireless control (home automation): audio/video), smart lighting;
- monitoring applications: security systems, water/fire/smoke detectors;
- telecommunications applications: secured networks;
- personal/hospital care;
- toys.

Through its very low power requirements (up to 5 years battery life), network capabilities (self-organizing and self-healing dynamic mesh network) and size (thousands of devices per network) but also its secure communications (by using 8–bit microcontroller implantable AES–128 encryption algorithm), ZigBee proves to be a reliable wireless technology [2.41]. Through its excellent performances in low signal–to–noise ratio environments it proves greater performances than any other wireless technology (GSM/3G, Bluetooth/WiFi).

2.2.5 GPS Applications

The second technological major achievement in the human history after the practical implementation of telecommunications systems may be considered the Global Navigation Satellite Systems (GNSS) that enable any user to know his position on Earth thanks to satellite systems. The first fully operational localization system is the American Global Positioning System (GPS), developed by the Department of Defense (DoD). The second one, partially available due to financial constraints is GLONASS, developed by the former Soviet Union now used rather as a back–up system to American GPS than a fully functional one. Both systems were developed as military applications and although they are currently accessible to civilians, they remain under army control (national defense departments) which also supports their costs. EU and ESA agreed in 2002 to implement an entirely European localization system, named Galileo, thought as complementary to the American GPS systems and expected to be operative in 2012. The first GALILEO satellite (Giove-A) was put into orbit in 2005 (Kazakhstan). The cost required for the second generation (the addition of four satellites and the development of the Galielo ground network) reached €950 million while the third phase (putting the rest of Galilleo satellites on the orbit) is expected to cost €3.6 billion. The high interest of different private companies in supporting the implementation of any GNSS systems is not surprising since the market of satellite navigation products and services knew an average annual increase of 25% even during crisis times. Although road applications represent an important GNSS market, many different areas makes use of this system. Thus, the main emerging GNSS applications are: Location Based Services, Road applications, Aviation, Maritime, Rail, Oil and Gas, Precision Agriculture, Fisheries, Survey and maritime engineering, Science, Electricity Networks, Social, Customs and Justice Affairs.

The satellite frequencies were chosen as a compromise between the required satellite transmission power and ionospheric errors, the errors significantly decreasing for frequencies higher than 1 GHz. This is also the reason why all GNSS bands are established between 1 and 2 GHz. The most important frequency bands are L1 and L2 while the modulation is BPSK. For the sake of generality, the GPS systems are working in the frequencies bands L2 (1215–1240 MHz) and L1 (1559–1610 MHz) and in future the band E5A (1164–1188 MHz) is to be reserved. L1 is expected to be used by Galileo together with E5A–B bands (1164–1215 MHz).

An overview (including design issues) of the GPS/Galielo RF Frontends proposed in literature until now is made in [2.42] while a good review of satellite systems is presented in [2.43].

2.2.6 WiMAX Applications

If two thirds of the entire world's population uses portable terminals to communicate instantly, the Internet users do not surpass 20% of the world's population although more of the productivity gains in today's economies are due to the Internet and ecommerce. The emerging countries are the most affected from this point of view due to economic problems, lack of infrastructure, affordability of personal computers and so on. The next step after designing 3G mobile and WLAN networks is the practical implementation of **mobile Internet** considered a revolutionary step. The purpose of WiMAX [2.44]…[2.46], based on IEEE.802.16 standards specifications, is to enable mobile Internet from the physical layer to the network layer. This novel technology makes use of OFDMA as multiple access method and MIMO, both to optimize coverage and spectral efficiency. A comparison between this novel technology and the previous broadband solutions already implemented over the world is presented in Table 6.

Parameter	Fixed WiMAX	Mobile WiMAX	HSPA	Wi-Fi
Standards	IEEE 802.16-2004	IEEE 802.16e-2005	3GPP release 6	IEEE 802.11 a/g/n
Frequency	3.5 GHz and 5.8 GHz initially	2.3 GHz, 2.5 GHz, 3.5 GHz initially	800/900/1800/ 1900/2100 MHz	2.4 GHz, 5 GHz
Multiplexing	TDM	TDM/OFDMA	TDM/CDMA	CSMA
Modulation	QPSK, 16 QAM, 64 QAM	QPSK, 16 QAM, 64 QAM	QPSK, 16 QAM	BPSK, QPSK, 16 QAM, 64 QAM
Bandwidth	3.5/7MHz - 3.5GHz 10MHz – 5GHz	3.5, 7, 5, 10 and 8.75 MHz	5 MHz	10MHz for a/g 20/40MHz for /n
Coverage	3-5 miles	< 2 miles	1 – 3 miles	< 100 ft indoors; <1000 ft outdoors

Table 6 Comparison of WiMAX and other broadband technologies [2.44]

2.2.7 Wireless USB Applications

Wireless USB applications are in fact practical implementations of the UWB standard (IEEE 802.15.3a) [2.47]…[2.49]. UWB refers to any radio or wireless device

where the occupied bandwidth is greater than 25% of the center frequency or greater than 1.5 GHz. This facilitates that a great number of users communicate using UWB technology. An ultra wideband communication consists of transmitting very short pulses with low energy where, the impulse radio UWB is a carrier–less radio technology (no mixer needed), therefore the practical implementation being quite simple. However, since UWB systems operate in a very large bandwidth shared with other telecommunications standards, interferences always exists mainly for frequencies lower than 5 GHz (WiMAX, WLAN) and must be minimized. The radiation mask regulated by FCC imposes a maximum radiation level of –41.3 dBm/MHz in the frequency range 3.1–10.6 GHz. According to this, there are three architectures that fulfill the power requirements, as presented in Table 7 [2.49].

Standard	OFDM	DS-UWB	TD/FDMA pulses
Bands	3–13	2	3–13
Bandwidths	3x528 – 13x528 MHz	1.5 GHz 3.6 GHz	3x550 – 13x550 MHz
Frequency ranges [GHz]	3.1–4.8 4.8–10.6	3.1–5.15 5.825–10.6	3.1–5 4.9–10.6
Modulation	OFDM–QPSK	M–BOK, QPSK	M–BOK, QPSK
Modulation Efficiency (10^{-3} BER)	6.8 dB	4.1–6.8 dB	6.1–6.8 dB
Error correction	Convolutional	Convolutional and Reed–Solomon codes	Convolutional and Reed–Solomon codes

Table 7 Three ways of implementing UWB systems

2.3 RF Front-ends Receivers and Multistandard Trend

The RF front-end is part of the overall radio receiver–transmitter or transceiver system and is represented by all blocks between the antenna and the digital baseband part. The front-end receiver task is to extract the original information from the transmitted radio waves while at the transmitter part to convert the baseband signal into an appropriate form supported by the telecommunications channel and also recognized by the receiver.

Any published microwave book includes one or more chapters dedicated to wireless transceivers meaning that a basic knowledge on RF part is compulsory when dealing with radio signals. This justifies a further review of wireless transceivers architectures generally used in telecommunications systems while the filtering part is emphasized. Several RF resources have been used for this section [2.50]…[2.62]. Moreover, hundreds

of articles envisaging different implementations of RF transceivers for one or more wireless standards (wideband or reconfigurable architectures) have been published in the literature until now. It is obvious that choosing one transceiver architecture may enhance the device performances therefore making the design of a particular RF block much easier or even may offer the opportunity to avoid certain blocks if the overall performances are not negatively influenced. The RF designers but also the companies behind them will do all the best to simplify the RF circuit and implement different methods in baseband to avoid some bulky or expensive RF blocks, thus decreasing the overall product cost and making the circuit design easier. An example in this case is the choosing of a particular modulation scheme. As presented in Table 8, the modulation scheme is very important for the power amplifier (PA) linearity [2.63].

Modulation scheme	Parameter	Crest factor (dB)
Wideband CDMA	16 occupied channels	10.5
	32 occupied channels	11.1
	64 occupied channels	12.2
	128 occupied channels	13.6
π/4-DQPSK	α=0.20	4.86
	α=0.25	4.55
	α=0.30	4.23
	α=0.35	3.87
	α=0.40	3.38
	α=0.50	3.21
16-QAM	α=0.20	6.03
	α=0.25	5.92
	α=0.30	5.66
	α=0.35	5.40
	α=0.40	5.18
	α=0.50	4.94
GSM EDGE (8-PSK)		3.21

Table 8 Three ways of implementing UWB systems

In the table above, “crest factor”, “peak ratio”, “peak to average ratio” and “peak to mean ratio” are *methods of defining the statistics of a modulated signal in a manner which an amplifier designer can understand and interpret* [2.63]. The “crest factor” (CF) is defined as the ratio of the peak to r.m.s. amplitude of a signal while “peak-to-mean ratio” ($PMR=CF^2$) is the ratio of the peak power to r.m.s. power of a signal. Therefore, the minimization of a multicarrier signal crest factor is envisaged when choosing a modulation scheme with a significant impact upon the power rating of the PA and its linearity. Baseband coding by implementing different codes like *Shapiro–Rudin sequences*,

maximal–length sequences, *Barker codes*, *Newman or Schoeder phases*, *block coding*, *selected mapping* and *partial transmit sequences*, the RF efficiency is greatly improved.

In the following, a brief review of the RF wireless transceiver architectures is presented, identifying, among others, the filtering issue. Since there are many references on this topic, a minimum condensed bibliography has been reported. Only CMOS circuits have been envisaged since this is the main technology used for RF circuits design aiming the lower microwave spectrum.

It is worth noting that instead of using voltages and currents, as they are employed for baseband circuits (analog/digital) design, power concepts are used in RF. Since the transceiver operates with low power input signals, this is usually expressed in dBm where the reference load resistance is considered 50 Ω if not otherwise stated.

The development of different transceivers schemes has an intrinsic reason: the technological impossibility of filtering a particular channel of hundred KHz or MHz directly in the RF domain in the GHz domain. Otherwise, RF preselective filters with very large quality factors are needed. In other words, the decision of choosing a particular architecture is determined in fact by the filtering possibilities. In the following sections a review of all RF transceiver types is presented.

2.3.1 Super–heterodyne Transceiver

The super–heterodyne receiver has the following block diagram (Fig. 2.6).

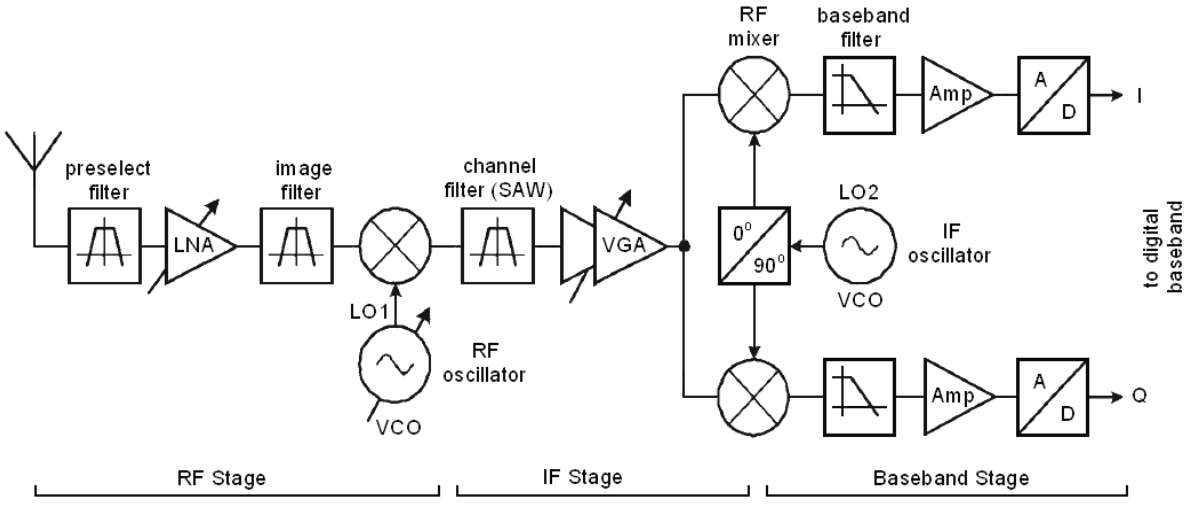


Fig. 2.6 Block diagram of the super-heterodyne receiver architecture

This architecture translates the desired signal band from higher frequencies (GHz domain) at a much smaller frequency (called intermediate frequency – IF), much lower

than the channel carrier frequency. The translation is carried out by a mixer, usually seen as an analog multiplier but passive mixers may be used as well. Channel select filtering is usually performed at the IF where relaxed requirements are imposed to SAW filters with respect to relative bandwidth. Several factors are taken into consideration when choosing the IF: (1) system requirements, (2) the radio frequency band (RF), (3) the usage of neighboring frequency bands, (4) possible interferer signals, (5) possible mixing products and (6) the availability of IF SAW filters.

This is a well–known architecture for its best overall system performance, still regarded the most reliable RF architecture for single band transceivers. However, it becomes useless for multi–band (reconfigurable) terminals due to the fixed IF section. Furthermore, consecutive amplification and filtering yield very high sensitivity and selectivity in the RF, IF and baseband part. This results in good image and interferer rejection, high channel selection and lower power consumption since the linearity constraints are more relaxed. These make it suitable for UMTS where the spectrum is more optimized compared to GSM cellular systems.

The main drawback is represented mainly by the increased number of blocks. It is obvious that the overall cost of such architecture using a large number of components is noticeable increased. Making use of two local oscillators (LO) and synthesizers together with three SAW filters is an important aspect. In addition, the LO and IF filter have different specifications, particular to world regions where the standard is regulated. Consequently, the design becomes more difficult and much effort is required for IF frequency planning to avoid spurious signals.

Different versions of heterodyne receivers have been developed: dual–IF receiver, image–reject receiver, wideband–IF receiver and digital–IF receiver. The dual–IF receiver makes use of two or more intermediate frequencies to optimize the trade–off between image–rejection and channel selection. In the case of image–reject receiver, the signal and its image are processed differently in order to achieve cancellation of the image. The wideband–IF receiver with double conversion suits best high level integration requirements. However, the large number of components (mainly of mixers) increases the power consumption making it a difficult choice. In digital–IF receivers the IF stage is digitized using high frequency ADCs. Digital IF signal processing avoids all problems encountered by the analog IF like I/Q amplitude and phase mismatch yielding to excellent image rejection. However, high performance ADCs results in high power consumption.

The super–heterodyne transmitter is shown in Fig. 2.7.

In a heterodyne transmitter, the baseband is converted to RF signal in two steps. By using variable power amplifiers in the RF part, the overall power consumption can be reduced, depending on the particular standard requirements. The intermediate filter (IF SAW) reduces the noise and spurs in adjacent channels.

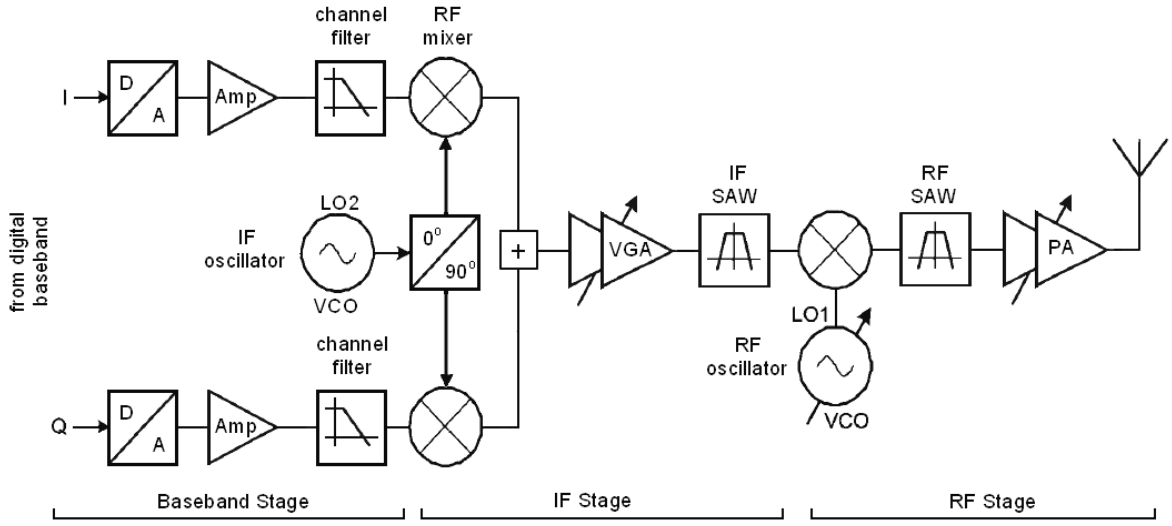


Fig. 2.7 Super-heterodyne transmitter architecture

The super–heterodyne transceiver is not suitable for multi–standard application due to its large number of building blocks and consequently the final cost but also its difficult IF frequency planning. The filtering part cannot be neglected since it consists of five SAW filters (3 for the receiver and 2 for the transmitter). The practical implementation of such circuit in practical multi–standards wireless devices is not possible until all filtering blocks are actively implemented.

A main drawback of heterodyne receivers is represented by the image frequency interference which is related to the mixing process. Considering that the frequency obtained at the mixer output port is equal to $f_{IF}=f_{LO}\pm f_{RF}$, the desired intermediate frequency signal ($f_{IF}=f_{RF}-f_{LO}$) is the difference one while the image frequency is the sum ($f_{LO}+f_{RF}$) and must be removed (Fig. 2.8).

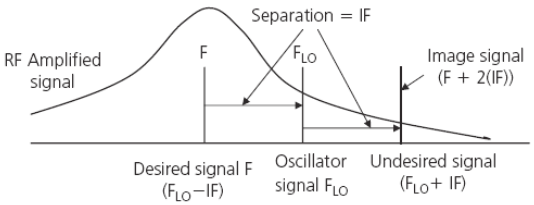


Fig. 2.8 Mixing process [2.61]

However, if a signal with the frequency $f_{RF}–2f_{IF}$ is applied to the input, the mixer generates the same image frequency (denoted as $f_{IF}^{*}=F+2(IF)$) therefore corrupting the desired intermediate frequency signal. This is the reason why a supplementary image–reject filter is used before the mixer which represents also the main drawback of this architecture.

To avoid the image problem, two image–reject receivers have been proposed as alternatives for heterodyne systems. One of them is the Hartley architecture (Fig. 2.9). The simplest phase shifter is implemented as RC–CR bridges (Fig. 2.10). This receiver topology is sensitive to amplitude balance and phase quadrature between two paths, the last being dependent on the parasitics and passive component matching.

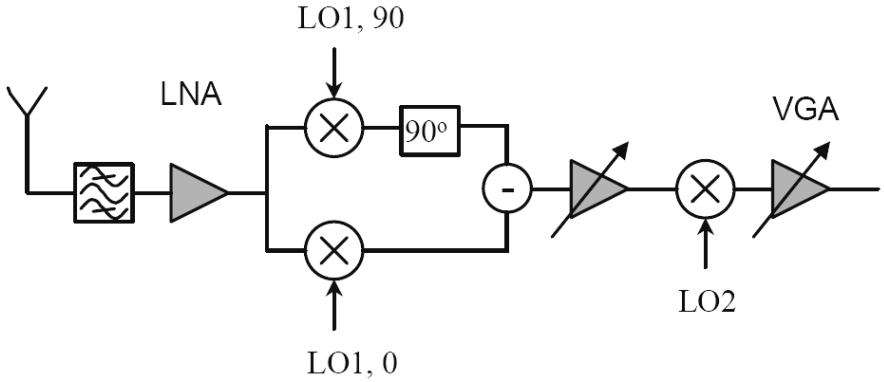


Fig. 2.9 Hartley receiver

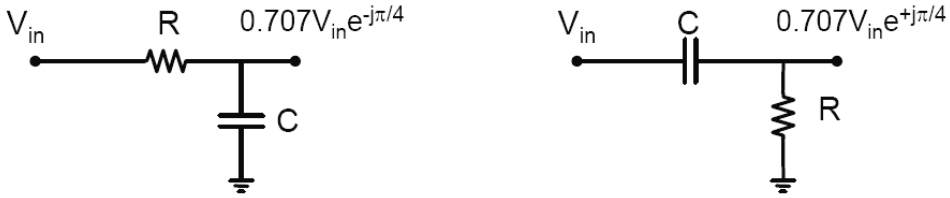


Fig. 2.10 Phase shifter used in Hartley receiver

The Weaver architecture is the second alternative to heterodyne receivers (Fig. 2.11). This architecture utilizes an additional pair of mixers to perform the phase shifting prior to IF combination therefore achieving greater image rejection despite temperature and process variations. These constitute the main advantage over Hartley topology although the gain and phase mismatches between the signal paths still represent a critical problem. However, the use of the second set of mixers brings new concern for a second image which must be addressed using proper frequency planning and filtering. If the signal is converted directly to BB by the second mixer than this image problem is avoided.

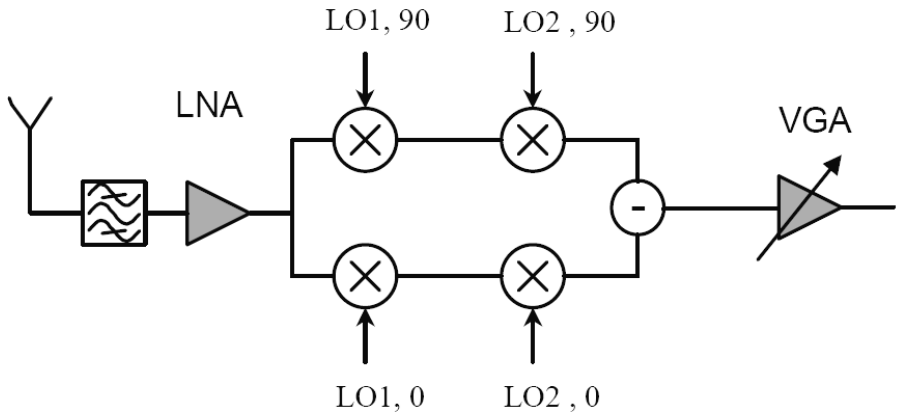


Fig. 2.11 Weaver receiver architecture

For the both configurations, low–pass filters are used after the mixing process. A self–calibrating Weaver architecture has been proposed by Razavi [2.64] – Fig. 2.12.

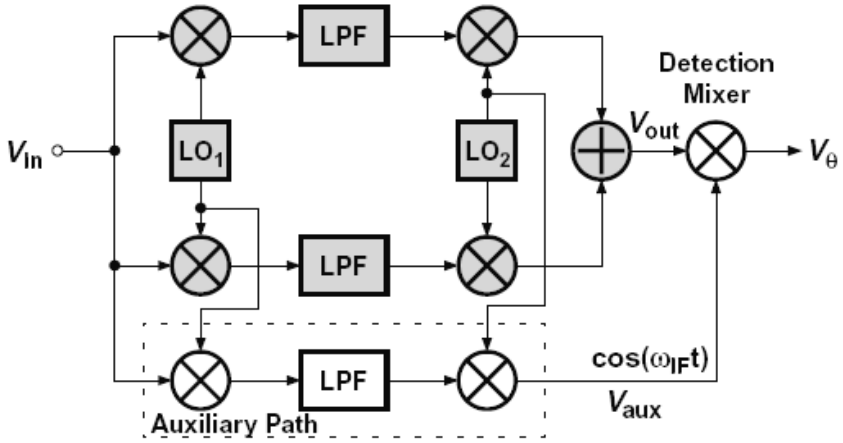


Fig. 2.12 Self-calibrating Weaver architecture [2.64]

2.3.2 Direct Conversion Architecture

The block diagram of the homodyne receiver, known also as direct conversion receiver or simply DCR, is presented in Fig. 2.13. The idea behind this configuration is to translate the desired signal band from higher frequencies (RF input signal) directly into the baseband where it is easier recovered. The channel filtering is implemented in this case by a low–pass filter which, being active, allows bandwidth tuning and thus the receiver can be configured as multi–standard architecture. Due to its simplicity, the need for frequency planning (time consuming and hard to validate) is avoided. Although direct conversion transceivers have worse performances compared to super–heterodyne transceivers (used in military applications), they are preferred for civilian applications since they are cheaper.

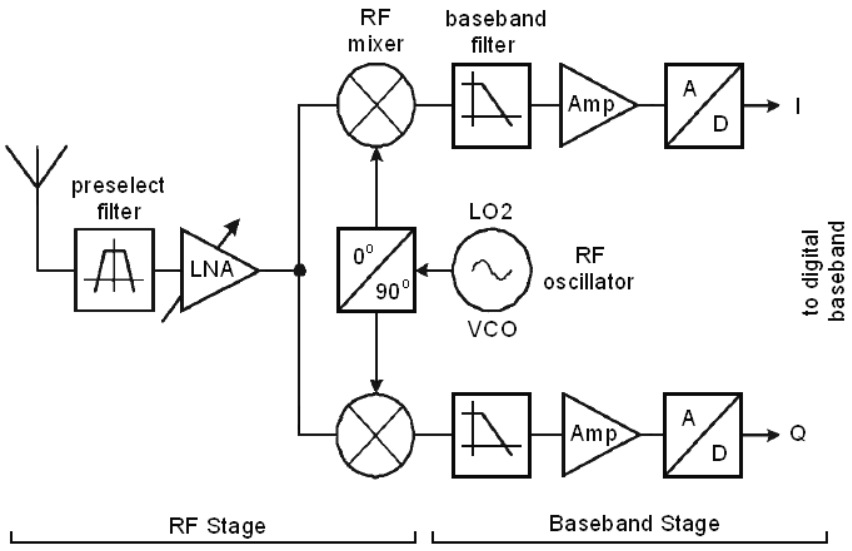


Fig. 2.13 Direct conversion receiver architecture

The circuit shown in Fig. 2.13 works as follows. The RF input signal is received by the antenna (modern wireless transceivers have multiple antennas) and the resulted signal is applied to a high quality factor passive external filter (usually SAW filter). This pre–select filter rejects the out–of–band interferences and image frequencies. Since only one filter is needed for this architecture, it must have a high quality factor. A common method of implementing wireless transceivers is to use duplexers instead of filters which separate the transmission and receiver paths which reject also the transmission leakage power. The signal is further amplified by a low noise amplifier (LNA), ideally designed with a high gain since it is the first RF front-end component. Currently, several successive identical LNAs are used in modern receivers in order to achieve higher gains (~ 60–80 dB) and thus maximizing the SNR ratio. By filtering and amplifying the input signal, the noise (not only the thermal one) that sets the transceiver sensitivity but also by other out of band RF signals (sources of interference), is lowered sufficiently compared to the signal level.

After maximizing the SNR level with LNA stage(s), the input RF signal is mixed (on a diode or FET mixer) with a reference signal generated by a local oscillator (LO) whose frequency, f_{LO}, is equal to that of the carrier f_{RF}. After the mixer, two signals are obtained: one with the frequency $f_{RF}' = 2f_{RF}$ and a second one in the baseband. In other words, the image frequency, a potential problem in super–heterodyne topology, coincides with the desired signal (IF = 0). The original signal is simply recovered through a corresponding low frequency filtering in KHz (switched capacitor filters) or MHz domain (g_m–C filters),

according to the standard specifications. After low–pass filtering, the signal is amplified and applied to an analog to digital converter (ADC), the signal being further digitally processed. As in the previous scheme, two orthogonal signals are received therefore the transmission efficiency being increased.

The main advantage of this architecture is that any supplementary local oscillator or mixer, required by heterodyne receiver to translate the information from IF to baseband, is not needed. Therefore, the design becomes simpler and smaller cost is achieved. Furthermore, the front–end is less affected by the individual nonlinearity and noise which, together with the possibility of channel bandwidth tuning, make this architecture well suited for multi–band and multi–mode application.

However, there are several drawbacks for this architecture as mentioned in the following.

1. The local oscillator must generate a signal synchronized to the exact carrier frequency, a requirement that makes the design more difficult. If they do not have identical frequencies, the signal cannot be recovered in BB.

2. DCR receivers are very sensitive to spurious LO leakage that can generate large DC offsets (self interference). A large DC offset compromise the amplification of the next low–pass filter amplifier that becomes saturated. The leakage problem is caused by the inherent LO leakage existing due to the weak isolation between LO port and LNA input. This problem characterizes any super–heterodyne receiver but due to its principle, the direct conversion architecture is much more affected by this problem.

The first type of leakage manifests when a fraction of reference signal (generated by LO), arrives to LNA input through capacitive and substrate coupling and mixes with the original LO generating a supplementary DC offset (self mixing) as shown in Fig. 2.14. The second type is encountered when a small part of the received input RF signal applied to LNA or mixer leaks to the LO port and mixes with the input signal at the mixer stage. This type of leakage is described in Fig. 2.15.

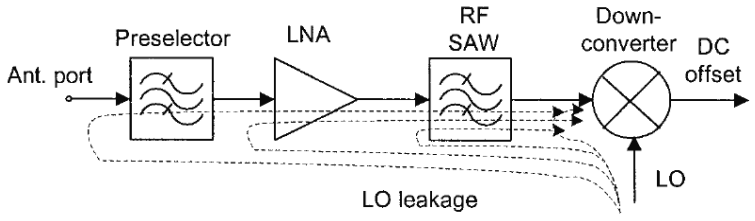


Fig. 2.14 DC offset caused by LO mixing [2.53]

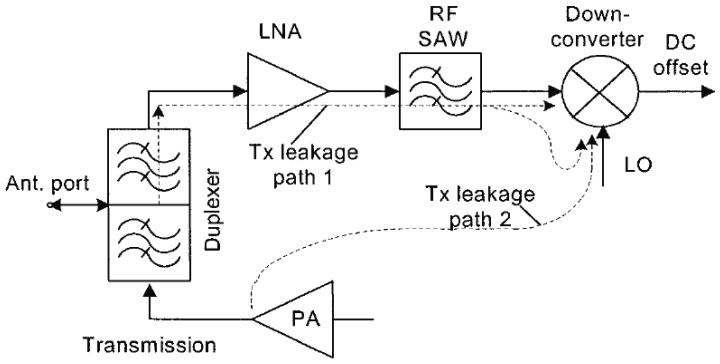


Fig.2.15 DC offset caused by the transmission leakage self–mixing [2.53]

The third one refers to the time variant self–mixing. In the case of moving objects (car, train), the reference signal generated by the local oscillator may leak to the antenna and be radiated in space. Being reflected back to the receiver, it mixes with LO and generates a time variable offset, thus making difficult the correct recovering in BB. Moreover, through this type of leakage, this transceiver acts as a source of interference for other transceivers working in the same frequency range since the "noise" signal generated by this LO–antenna leakage becomes baseband signal or DC offset for others. The pre–select filter selects the entire bandwidth allocated to a particular standard and thus any receiver, working at a particular time on a specific channel, receives also other in–band signals (emitted be other transmitters) which are in fact interferences.

However, this leakage problem can be minimized by applying the following methods:

a) Careful transceiver design (RF design level), including the possibility of implementing near zero DCR where the signal is recovered at very low frequencies but not 0, thus exploiting that mixers have not the same carrier frequency but with the requirement of using higher frequency ADCs. However, the use of high frequencies ADC does not represent a problem since even GHz bandwidth ADCs are currently on the market.

b) Maintaining good isolation between the LO and the RF part at a layout level, also including the possibility of using a high reverse isolation LNA. A LNA gain of 20 dB is high enough to increase the LNA isolation. The insertion loss of RF bandpass filter (and of preselector) further enhances the isolation. However, the implementation of differential LNAs or circuit independent single ended LNAs strongly ameliorates the LNA isolation and decreases the leakage.

c) Efficient bit representation (using NRZ or bipolar encoding) of the BB signal before being modulated so that, after demodulation, little energy is near DC.

d) AC coupling in baseband simply avoids this problem but adds new drawbacks since this coupling decreases the signal energy around DC and introduces group delay distortion near the DC further reducing the SNR and affecting receiver sensitivity. An alternative is to filter out the DC component (high–pass filtering) if the baseband spectrum is predominantly away from DC as in the case of WLAN a/g spectrum but not applicable otherwise (Blutetooth case where the spectrum is concentrated at very low frequencies).

3. As the down-converted RF signal is usually of low amplitude and low frequency (near 0 Hz), flicker noise (1/f) from the mixer output decreases the SNR. This depends on what telecommunications standard is implemented, the GSM one being more sensitive to this noise due to its small bandwidth.

4. Second order intermodulation distortion becomes significant for this architecture, two mechanisms being responsible: RF self–mixing and device nonlinearity and mismatches. When designing a high performance direct conversion transceiver, higher IIP2 compression points must be envisaged. For example, in the case of UMTS – frequency division duplexing system a minimum IIP2 value of 48 dBm is required. The use of high quality factor RF bandpass filters relaxes the IIP2 receiver requirements.

The concept of direct conversion transceiver was introduced in 1924 and adopted for the first time in 1932, as a replacement for heterodyne transceivers. However, they have seen limited use in the past, for over half a century, due to implementation complexities when building it with discrete components. A well known example of direct conversion receiver built with discrete components is the amplitude demodulator. Owing to the technological advancements during the last decades, this architecture has been widely adopted (first time for GSM standard in 90's) and now it represents an attractive solution for reconfigurable multistandard 3G/4G transceivers due to its simplicity, low cost, small size and low power consumption. In other words, the technological trend of using direct conversion transceivers in RF wireless terminal is a positive one, proving to be different of what Razavi expected in 1998 [2.50]. Moreover, the DCR architecture is more suitable for multistandard applications employing wide channel bandwidth since this mitigates the classical DCR problems like flicker noise and DC offset. The first analog systems used a bandwidth of 25 KHz, GSM uses 200 KHz while currently WCDMA systems make use of 5 MHz bandwidth. It is obvious that multimedia services require large bandwidths a fact that makes direct conversion architectures an attractive choice for the coming generations of cellular receivers. From this point of view, the main advantage of DCR structure over

super–heterodyne architecture is that the latter becomes quite complex for multi–standard applications due to the great required number of mixers, local oscillators and filters negatively affecting the overall cost. However, an important drawback for these transceivers that still remains is the use of RF filters (before LNA) which are external, bulky and, though cheap, the final cost for using between 8 and 12 RF filters or even more when implementing a multi–standard device is greatly increased, taking into consideration the billions of mobile devices sold over the world. A considerable effort may be put in future for designing SAW–less homodyne transceivers or integrating RF filters in an active reconfigurable topology.

The architecture of direct conversion transmitter is shown in Fig. 2.16.

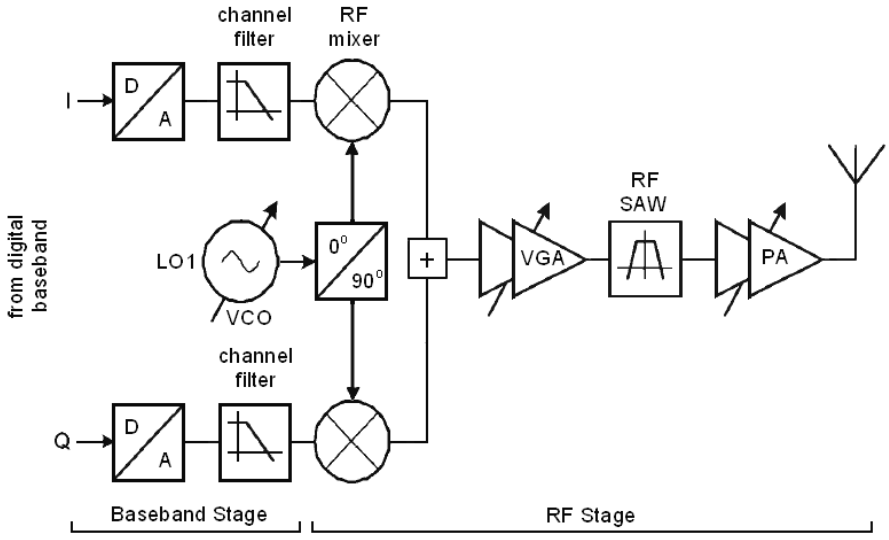


Fig. 2.16 Direct conversion transmitter

The advantage of the direct conversion transmitter consists in the rejection of the IF path with its SAW filter leading to high integration level and lower cost. Using a single mixer and VCO, fewer mixing products and lower level spurious signals are generated in the output spectrum. All these make this architecture suited for multi–band multi–mode operation. However, it seems that the power consumption is comparable to a heterodyne receiver, despite its high integration level.

It is worth mentioning that for the receiver part, the baseband analog circuits establish the overall receiver gain (approximately 75%) in opposite to the transmitter part where more than 90% of its gain is in the RF part from I/Q modulator to the power amplifier (PA). Furthermore, the direct conversion transmitter has fewer drawbacks than the receiver counterpart, therefore being easier to be implemented. However, direct

conversion transmitter architectures make use of the same SAW filter introduced in between power amplifier and driver amplifier, in order to minimize the out–of–band and spurious emissions for the receiver part. From this point of view, the single gain of a direct conversion transmitter over the super–heterodyne transmitter consists in it's LO. This is the reason why much profit is obtained rather with the receiver part than the transmitter one for a direct conversion scheme.

A clear drawback of this architecture is the mechanism of *injection locking/pulling*. It refers to the fact that the LO is disturbed by the up–converter or power amplifier and consequently causes spurious signals and noise in the transmit spectrum. If the PA is turned on and off periodically as in the case of 3G systems (3GPP–TDD), the problem worsens. Other challenges consist in high I/Q phase accuracy, high linearity and noise performance for the RF blocks, higher LO–RF isolation, low noise floor requirements as well as output spectrum purity.

2.3.3 Low–IF Receiver

The architecture of a Low–IF receiver is shown in Fig. 2.17.

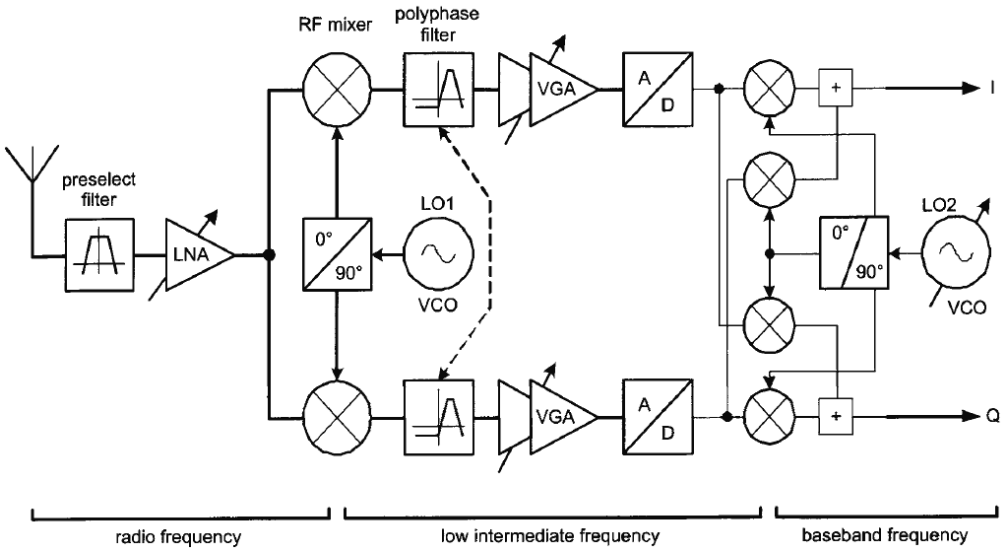


Fig. 2.17 Low–IF receiver architecture

It represents in fact a compromise between the heterodyne and the homodyne architectures. In this case, the signal is quadrature down–converted to a very low IF (for example hundreds of kHz i.e. the order of one channel spacing) by exploiting the mixing properties of a complex mixer (used to multiply two complex signals). Such mixer only

mixes the positive RF frequencies with a negative LO frequency thus achieving an active image rejection.

The low–IF allows the use of low–Q channel select filter while avoiding the dc–offset problems encountered in zero–IF. The complex signal applied to the mixer input is generated in a complex form by the polyphase filters which act as an allpass filter for positive frequencies and band–stop one for negative frequencies. This is superior to zero–IF architectures since is not sensitive to dc–offset, LO leakage and intermodulation product of third order (IM3). However, due to the limited matching between I and Q generators, limited image rejection is achieved while asymmetric poly–phase filters used to enhance the image rejection introduce insertion loss and cause noise degradation. This architecture is more suitable for telecommunications applications with low adjacent channel power or with exceptions for image frequencies like GSM, Bluetooth or DECT. It envisages rather the receiver side than the transmitter one and thus a mixing between heterodyne transmitter and low–IF receiver may be used as well.

2.3.4 Software Defined Radio (SDR) Architectures

SDR represents an ideal revolutionary concept regarding the RF design. In a SDR transceiver the signal is entirely processed by means of software control. They are known also as *digital transceivers*. The basic idea is to place the ADC/DAC pair in the RF front–end near the antenna as possible which means more digital/software processing instead of analog RF processing. Often thought in terms of baseband DSPs, hence the term *software radio*, by making use of FPGAs, ASICs, parallel processor arrays and other techniques, the SDR transceiver is a flexible software based radio architecture, increasingly adopted and researched. It may be obvious that an important application of these SDR architectures would be represented by military communications where the opportunity of changing not only the scrambling or encryption codes (avoiding the communications interception) but also the modulation format, channel bandwidth, data rate and voice codec type is of high interest.

The ideal SDR architecture is shown in Fig. 2.18. As it can be noticed, by extensively minimizing the analog RF part, all stringent requirements are imposed to ADCs and DACs which must have wide dynamic range and high sampling rates (of many GHz) with a negative impact on the power consumption. In this case, the converter must

work at an RF sampling frequency higher than twice the greatest carrier of the frequency of interest while the samples are processed by a programmable signal processor.

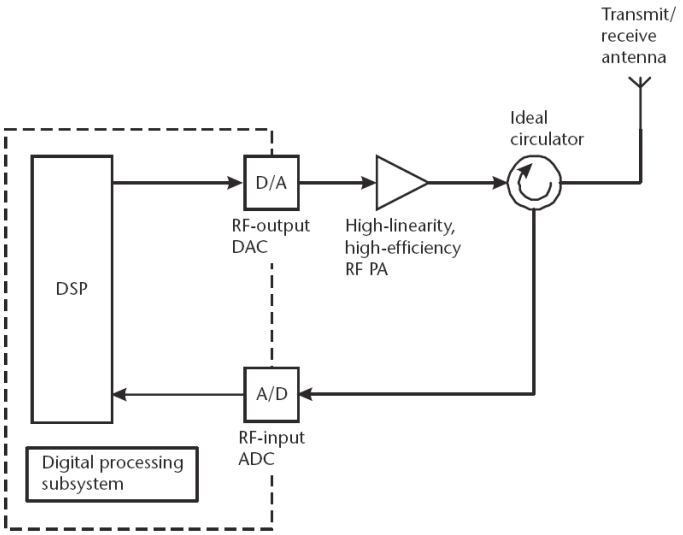


Fig. 2.18 Ideal SDR architecture

The technology achieved during the last three years the required maturity level to provide devices with such sampling rate. An example is the 12–bits MAX 5881 converter with a sampling rate of 4.3Gsps [2.65] optimized for direct RF synthesis of multichannel downstream QAM signals. Therefore, the path for the ideal SDR concept mentioned previously is already opened.

So far, several steps to a fully SDR implementation have been made and consequently are mentioned in the following. One of them, already implemented in mobile terminals, is the so called *digital direct conversion* architecture or *digital transceiver* (Fig. 2.19), mentioned previously.

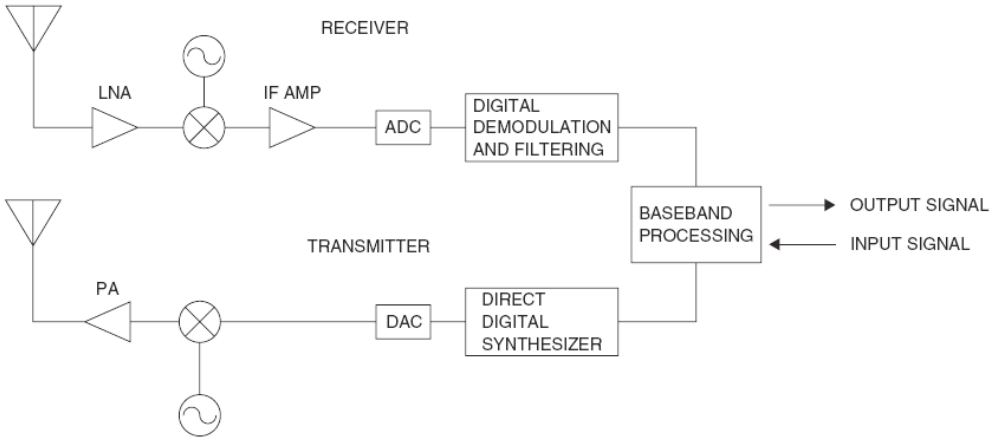


Fig. 2.19 Digital transceiver arhictecture [2.66]

This structure is based on the superheterodyne architecture but the mixing and IF filtering is done by analog–to–digital converters and digital filters. In other words, the IF filtering and demodulations are made by means of digital signal processing software. The transmitter uses a direct digital synthesizer (DDS) to generate the modulated transmitter frequency. For this architecture, phase, frequency and amplitude variations of the carriers as functions of the baseband data are implemented by the software with no change in hardware. As noticed in the figure above, the filtering part is implemented also by means of software therefore greatly improving the size, flexibility and performances while decreasing the cost. Such architecture is currently used in CDMA communications [2.56] known also as *bandpass sampling radio* transceiver (Fig. 2.20) and as can be noticed this topology posses some features of the ideal software radio.

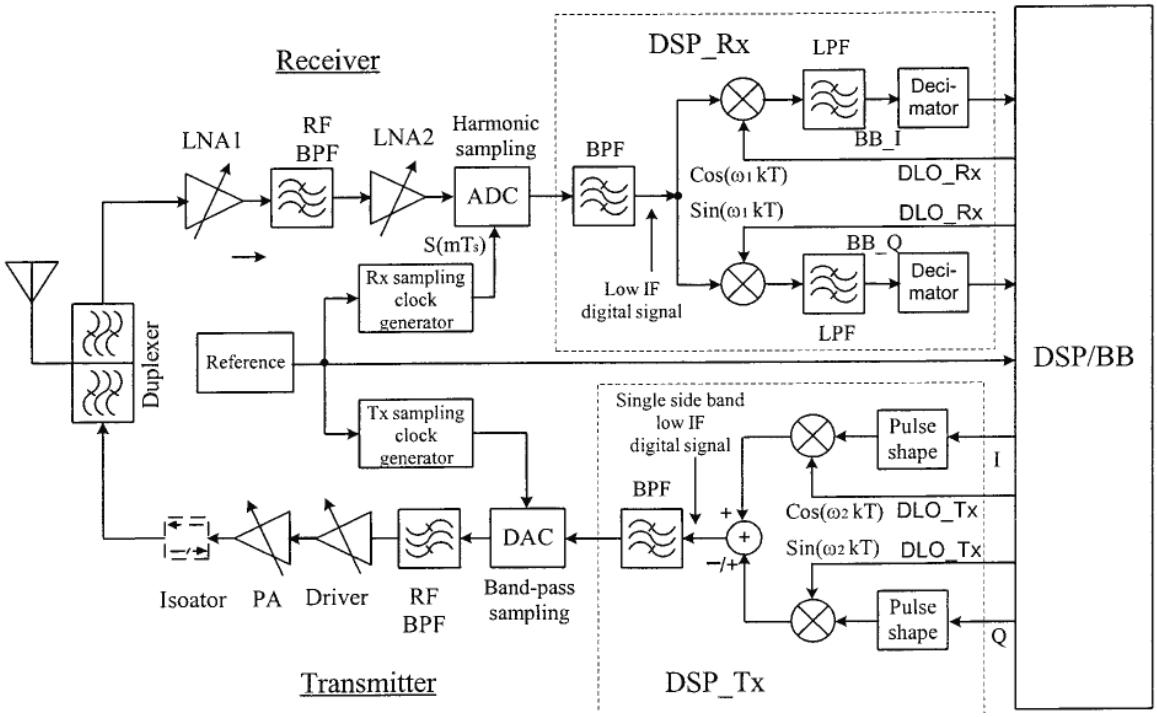


Fig. 2.20 Bandpass Sampling Radio transceiver [2.56]

The implementation of this architecture wouldn't be possible without a corresponding development of ADC and DAC. This represents another example about the positive effects obtained in the RF part when applying strong principles / innovative ideas in baseband. It is obvious that the architecture in Fig. 2.20 is much simpler than the previous topologies since the low frequency processing (analog filters, VGA) is not required anymore. However, good ADC supporting higher data rates with large dynamic range are required, thing possible now. The "innovative idea" in this case is the use of

undersampling / *harmonic / IF sampling* or *direct IF-to-digital conversion* [2.67], illustrated in Fig. 2.21. Simply stated, the idea is to sample the IF signals directly at higher frequencies without any demodulation process. The Nyquist theorem states that *a signal must be sampled at a rate equal to or greater than twice its* ***bandwidth*** *in order to preserve all the signal information*. Bandwidth may signify the maximum frequency of a baseband signal ([0, f_a]) or the bandwidth of a high frequency signal ([f_a, f_b]). The sampling frequency must be at least twice the bandwidth which signifies $f_s>2f_a$ and also $f_s>2(f_a–f_b)$ for the latter. The second case is known also as *bandpass sampling* and is a very useful technique since it replaces the analog demodulation.

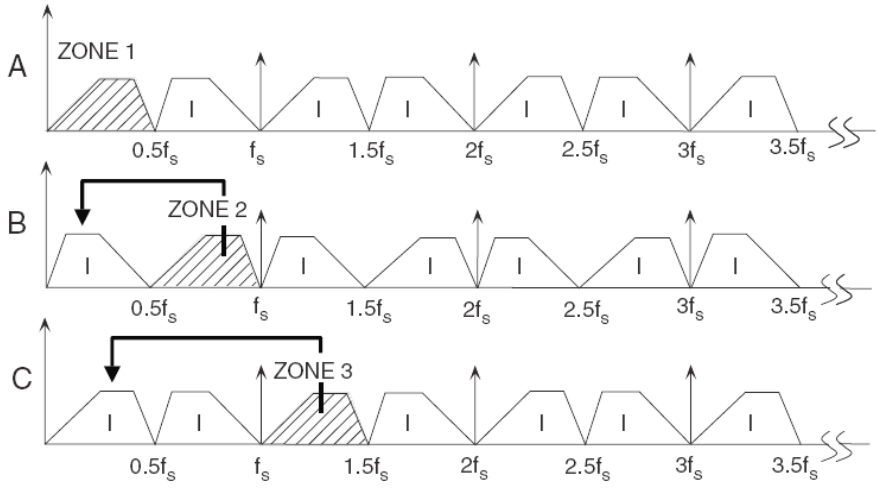


Fig. 2.22 Undersampling and Frequency Translation between Nyquist Zones [2.67]

Three steps must be followed in order to find the sampling frequency which facilitates the correct signal recovering, where NZ is the number of Nyquist band (zone):

$$\begin{cases} 1. \quad f_{s,\min} = 2(f_b - f_a) \\ 2. \quad f_s = \dfrac{4f_c}{2NZ-1} (\geq f_{s,\min}) \Rightarrow NZ = \dfrac{4f_c + f_s}{2f_s} \\ 3. \quad f_s = \dfrac{4f_c}{2[NZ]-1} \end{cases} \tag{2.1}$$

Another approach, much closer to the SDR concept, was proposed in [2.68]. The circuit (Fig. 2.23) represents a multiband RF–sampling receiver designed for the both WLAN bands (2.4 GHz and 5–6 GHz) in 0.13 μm CMOS process. The circuit uses a wideband low noise amplifier and a sampler together with a discrete–time switched–capacitor (SC) filter to achieve zero–IF down–conversion. Prior to A/D converter the

sampled signal is decimated and bandlimited. The filter removes the image bands. The circuit has the sufficient degree of generality for being applied to UMTS, WCDMA and Bluetooth standards.

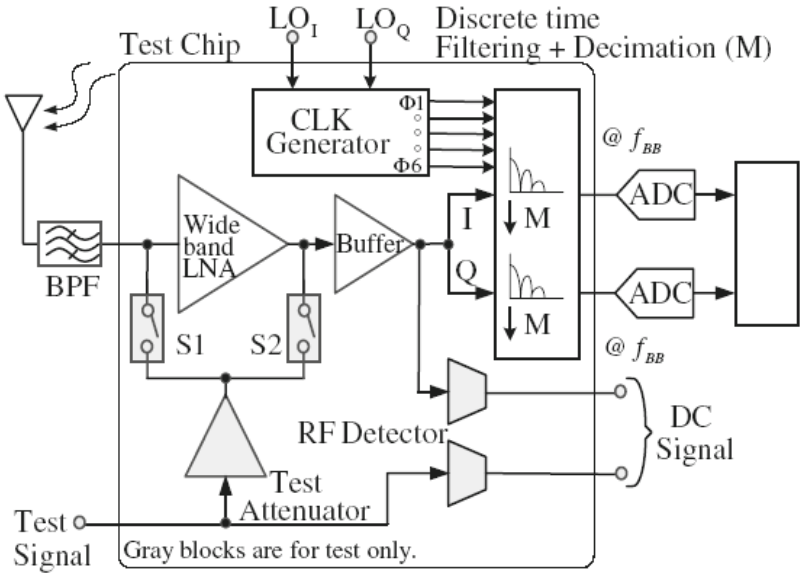


Fig. 2.23 Multiband RF sampling receiver [2.68]

A third SDR architecture was proposed in [2.69] and shown in Fig. 2.24.

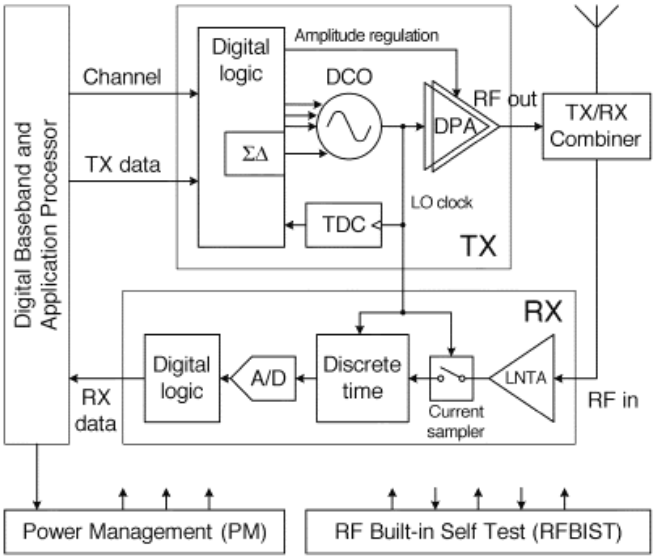


Fig. 2.24 Single-chip Bluetooth radio with an all-digital transmitter and a discrete-time receiver [2.69]

A fourth architecture (Fig. 2.25) is a full SDR transceiver designed in IMEC [2.70], considered the largest independent research center in nanoelectronics and nano–technology in Europe.

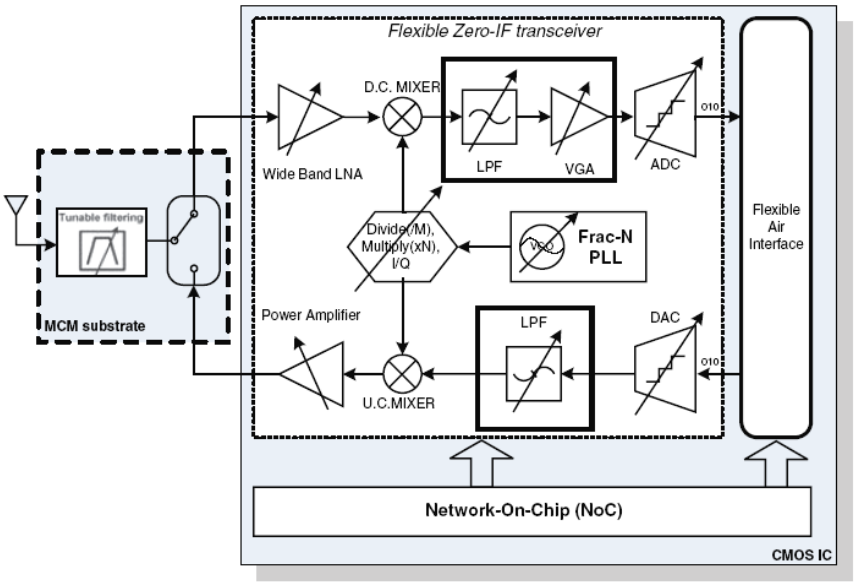


Fig. 2.25 Zero–IF transceiver implemented by IMEC [2.70]

2.3.5 SAW–less Wireless Transceivers

As noticed before, the SAW filters existent on the market are bulky and offers no possibility of tuning although they are widely used in telecommunications transceivers since are currently the best solution. Although these filters are cheap, a great number of filters used in a reconfigurable transceiver, as showed in Fig. 2.26, increase the chip area and cost.

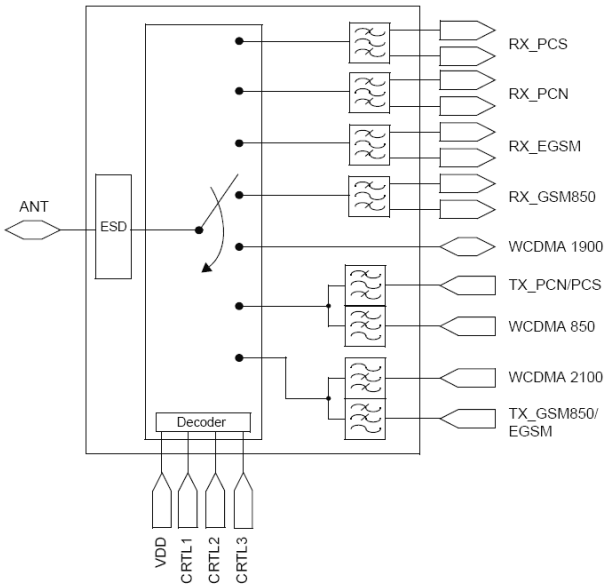


Fig. 2.26 D2024 EPCOS SAW Front–end module [2.23]

Alternative solutions have been searched in order to avoid these passive filters by means of supplementary RF or BB processing. The first notable one (Fig. 2.27) is the transceiver proposed by Kaben Wireless Silicon [2.71].

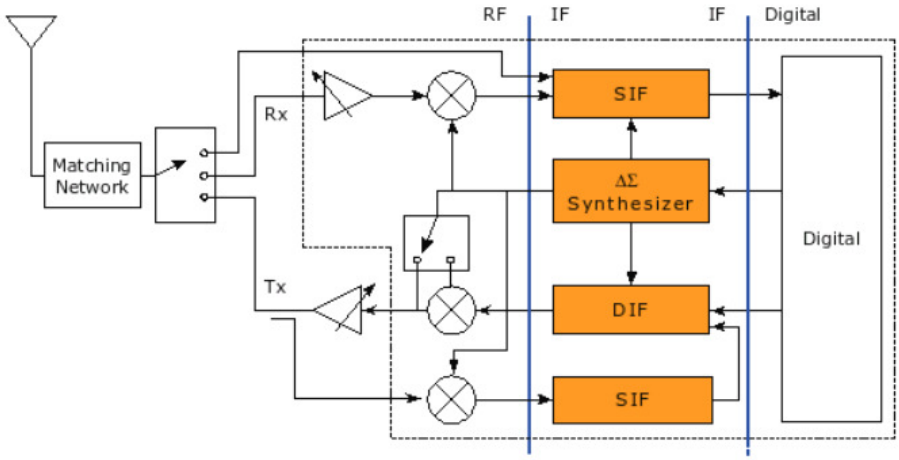


Fig. 2.27 SAW–less reconfigurable transceiver architecture [2.71]

From the solutions proposed in the literature, one makes use of supplementary processing on the LNA stage in order to reject the out–of–band interference signals (Fig. 2.28) [2.72].

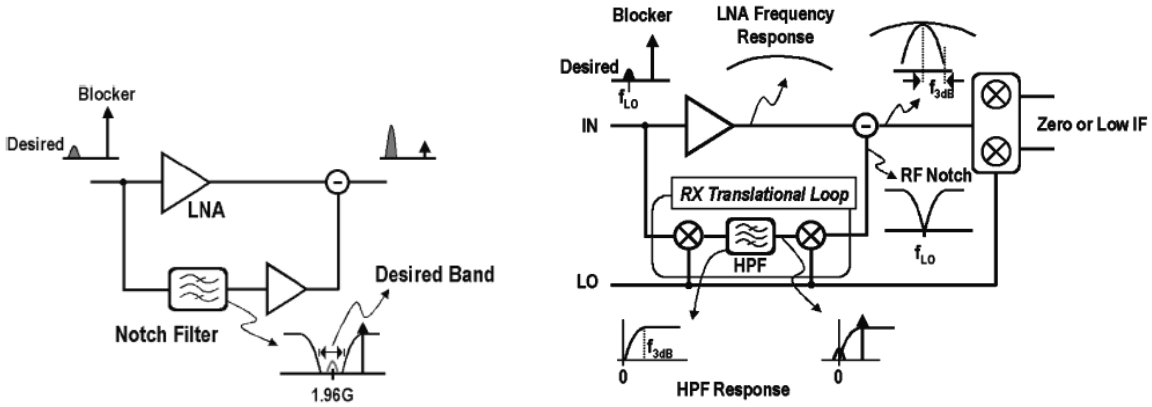


Fig. 2.28 Feed–forward blocker cancellation in the LNA [2.72]

The idea is to subtract a replica of the input signal which does not contain the desired signal from the input signal. Therefore, in the ideal case, the LNA output signal represents only the desired signal. As proved in this paper, the same out–of–band rejection ratio is obtained for this RF front–end as in the original case when SAW filters are used. Such blocker filtering LNA was proposed in [2.73] and showed in Fig. 2.29. As used in most implementations, a passive notch filter is used although it may be implemented in active form too.

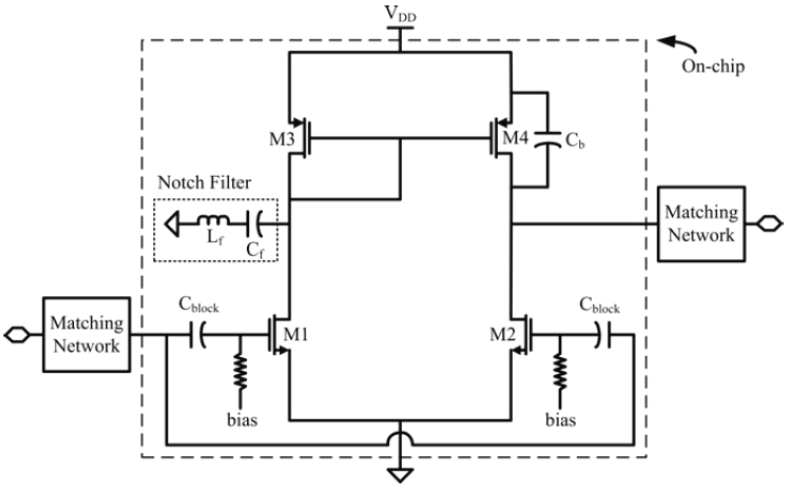


Fig. 2.29 Blocker filtering LNA [2.73]

Another solution envisages the rejection of the second SAW filter (Fig. 2.30) used after the LNA [2.74] and makes use of passive mixers which ensure supplementary rejection of 15 dB.

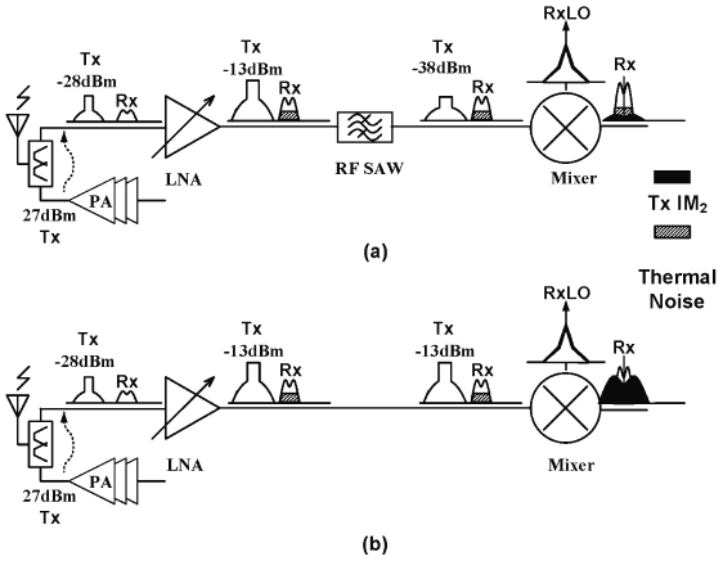


Fig. 2.29 Conventional receiver (a) and SAW – less architecture (b) [2.74]

The avoidance of SAW filters, currently used in WCDMA transmitters (Fig. 2.30) to reject the interference on the receiver part, is proposed in [2.75]. The transmitter uses direct quadrature voltage modulation via a passive voltage mixer driven by 25%-duty-cycle LO. It proves very good noise performances which makes the SAW passive filter useless.

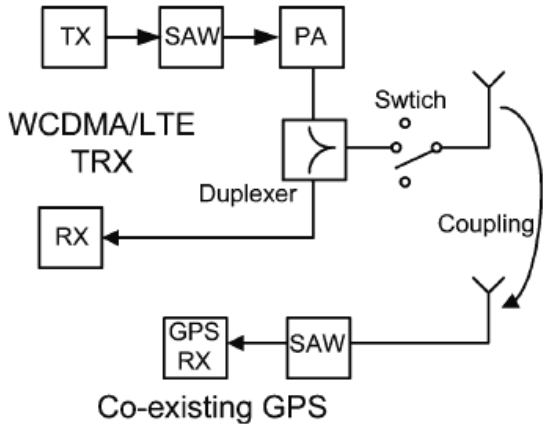


Fig. 2.30 WCDMA TRX and the co–existing GPS receiver [2.75]

An improvement of this method was reported in [2.76] where the external LNA and inter–stage SAW filter are avoided, resulting in a low size, noise and power consumption 3G multi–standard terminal (Fig. 2.31).

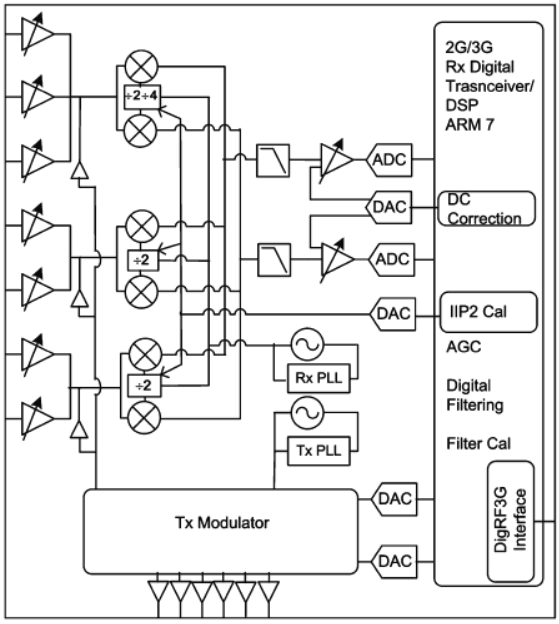


Fig. 2.31 SAW–less 3G transceiver [2.76]

2.4 CONCLUSION

The continuous development of wireless standards imposes new constraints not only on the spectrum and power efficiency but also on the chip area and circuit reconfigurability. In addition to these, as emphasized in this introductory chapter, the practical implementation of a full on–chip multi–standard device is still a challenge mainly due to the RF filtering part and new filtering solutions must be investigated in this regard.

2.5 REFERENCES

[2.1] Radio Frequency Integrated Circuit Technology for Low-Power Wireless Communications, L. E. Larson, IEEE Personal Communications, Vol. 5, No. 3, pp. 11–19, 1998

[2.2] CMOS: A Paradigm for Low Power Wireless?, M. Steyaert and P. Vancorenland, Proc. of the 39th Annual Design Automation Conference, DAC, 2002, New Orleans, Louisiana (USA)

[2.3] Digital RF Processing: Toward Low-Cost Reconfigurable Radios, K. Muhammed, R. B. Staszewski and D. Leipold, IEEE Communications Magazine, Vol. 43, No. 8, pp. 105–113, 2005

[2.4] Choosing RF CMOS or SiGe BiCMOS in mixed-signal design, A. H. Pawlikiewicz and D. Hess, RF Design, pp. 36–44, 2006

[2.5] Evolutional Trend of Mixed Analog and Digital RF Circuits, S. Tanaka, IEICE Trans. Electron., Vol. E92–C, No. 6, 2009

[2.6] A Comparison of Si CMOS and SiGe BiCMOS Technologies for Automotive Radars, A. Margomenos, IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, SiRF, pp. 1–4, 2009

[2.7] The Quantum Limit to Moore's Law, J. R. Powell, Proceedings of the IEEE, Vol. 96, No. 8, pp. 1247 – 1248, 2008

[2.8] 10-GHz-Band VCO With Low Phase-Noise Using 0.18µm CMOS Process, W. –N. Chen, K. –H. Cheng, J. –Y. Deng and W. C. –Chung, 8th IEEE International Conference on Solid-State and Integrated Circuit Technology, ICSICT, pp. 1583-1585, 2006

[2.9] A Low Phase Noise 10 GHz VCO in 0.18µm CMOS Process, T. –y. Choi, H. Lee, L. P. B. Katehi and S. Mohammadi, European Microwave Conference, Vol. 3, 2005

[2.10] Fully-Integrated 10 GHz CMOS VCO for multi-band WLAN applications, L. Perraud, J. –L. Bonnot, N. Sornin and C. Pintael, 29th European Conference on Solid-State Circuits Conference, pp. 353-356, 2003

[2.11] A 16-GHz 0.18-µm CMOS Differential Colpitts VCO with a Moderate Output Power for DS-UWB and 60-GHz Applications, C. –C. Lee, C. –L Lu and H. –R. Chuang, Proceedings of the Asia-Pacific Microwave Conference, 2006

[2.12] Microwave Active Inductors, D. Zito, A. Fonte and D. Pepe, IEEE Microwave and

Wireless Components Letters, Vol. 19, No. 7, 2009
[2.13] 40-Gb/s Amplifier and ESD Protection Circuit in 0.18-μm CMOS Technology, S. Galal and B. Razavi, IEEE Journal of Solid-State Circuits, Vol. 39, No. 12, 2004
[2.14] Techniques Simplify Wireless Transmission, C. Wise, Wireless System Design, pp. 38-40, Jan. 2003
[2.15] Smart Antenna Systems and Wireless LANs, G. T. Okamoto, Kluwer Academic Publishers, 2002
[2.16] Smart Antenna Technologies for Future Wireless Systems: Trends and Challenges, A. Alexiou and M. Haardt, IEEE Communications Magazine, Vol. 40, No. 9, pp. 90-97, 2004
[2.17] Smart Antennas, L. C. Godara, CRC Press, 2004
[2.18] Handbook on Advancements in Smart Antenna Technologies for Wireless Networks, C. Sun, J. Cheng and T. Ohira, Information Science Reference, 2009
[2.19] www.efis.dk
[2.20] Mobile Radio Networks. Networking and Protocols, B. H. Walke, John Wiley & Sons, 1999
[2.21] 3G Wireless Networks, C. Smith and D. Collins, McGraw-Hill, 2002
[2.22] 3G Evolution: HSPA and LTE for Mobile Broadband, E. Dahlman, S. Parkvall, J. Sköld and P. Beming, Elsevier, 2007
[2.23] www.epcos.com
[2.24] www.triquint.com
[2.25] Surface Acoustic Wave Filters, D. Morgan and E. G. S. Paige, Elsevier Ltd.,2007
[2.26] RF Bulk Acoustic Wave Filters for Communications, Ken-ya Hashimoto, Artech House, 2009
[2.27] Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, IEEE Std 802.11 – 2007
[2.28] Introduction to 802.11 Wireless LAN (WLAN): Technology, Market, Operation, Profiles, & Services, L. Harte, e-book, 2004
[2.29] Emerging Wireless LANs, Wireless PANs, and Wireless MANs, Y. Xiao and Y. Pan, John WIey & Sons, New Jersey, USA, 2009
[2.30] Wireless Networking, A. Kumar, D. Manjunath and J. Kuri, Elsevier, 2008
[2.31] Wireless LAN Radios. System Definition to Transistor Design, A. Behzad, Wiley – Interscience, 2008

[2.32] Next Generation Wireless LANs, E. Perahia and R. Stacey, Cambridge University Press, 2008
[2.33] Wireless LAN Comes of Age: Understanding the IEEE 802.11n Amendment, T. Paul and T. Ogunfunmi, IEEE Circuits and Systems Magazine, Vol. 8, No. 1, pp. 28-54, 2008
[2.34] Specification of the Bluetooth System, v1.0 B, Dec. 1999
[2.35] Specification of the Bluetooth System, v2.0 + EDR, Nov. 2004
[2.36] Introduction to Bluetooth: Technology, Market, Operation, Profiles, & Services, L. Harte, e-book, 2004
[2.37] Bluetooth Specification Version 3.0 + HS, Apr. 2009
[2.38] Bluetooth Specification Version 4.0, Dec. 2009
[2.39] IEEE Std 802.15.4 – 2003, Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)
[2.40] http://www.zigbee.org/
[2.41] Zigbee Wireless Networking, D. Gislason, Elsevier Inc., 2008
[2.42] GPS & Galileo: Dual RF Front-end Receiver and Design, Fabrication, and Test, J. M. Samper, R. B. Pérez and J. M. Lagunilla, McGraw-Hill Companies, 2009
[2.43] Global Positioning. Technologies and Performance, N. Samama, Wiley-Interscience, 2008
[2.44] Fundamentals of WiMAX. Understanding Broadband Wireless Networking, J. G. Andrews, A. Ghosh, R. Muhamed, Prentice Hall, 2007
[2.45] Mobile WiMAX, K. –C. Chen and J. R. B. de Marca, John Wiley & Sons, Ltd., 2008
[2.46] WiMAX Evolution, M. D. Katz and F. H. P. Fitzek, John Wiley & Sons, Ltd., 2009
[2.47] Ultra-Wideband Radio Technology, K. Siwiak and D. McKeown, John Wiley & Sons, Ltd, 2004
[2.48] Ultra Wideband. Circuits, Transceivers and Systems, R. Gharpurey and P. Kinget, Springer Science, 2008
[2.49] Introduction to Ultra Wideband for Wireless Communications, H. Nikookar and R. Prasad, Springer Science, 2009
[2.50] RF Microelectronics, B. Razavi, Prentice Hall, 1998
[2.51] RF and Microwave Wireless Systems, K. Chang, John Wiley & Sons, Inc., 2000
[2.52] The Design of CMOS Radio-Frequency Integrated Circuits, T. Lee, Cambridge

University Press, 1998

[2.53] Transceiver architectures for W-CDMA mobile terminal applications, W. Thomann, J. Fenk, R. Hagelauer and R. Weigel, e & i Elektrotechnik und Informationstechnik, Vol. 120, No. 3, 2003, Springer Wien

[2.54] Modern Receiver Front-Ends, J. Laskar, B. Matinpour and S. Chakraborty, Wiley-Interscience, 2004

[2.55] RF and Baseband Techniques for Software Defined Radio, P. B. Kenington, Artech House, 2005

[2.56] RF Engineering for Wireless Networks, D. M. Dobkin, Elsevier, 2005

[2.57] RF System Design of Transceivers for Wireless Communications, Q. Gu, Springer Science, 2005

[2.58] Analog-Baseband Architectures and Circuits for Multistandard and Low Voltage Wireless Transceivers, P. –I. Mak, S. –P. U, R. P. Martins, Springer Science, 2007

[2.59] Wireless Transceiver Design, A. Luzzatto and G. Shirazi, John Wiley & Sons, Ltd., 2007

[2.60] Baseband Analog Circuits for Software Defined Radio, V. Giannini, J. Craninckx and A. Baschirotto, Springer Science, 2008

[2.61] RF & Wireless Technologies, B. Fette, R. Aiello, P. Chandra, D. M. Dobkin, A. Bensky, D. Miron, D. A. Lide, F. Dowla and R. Olexa, Elsevier, 2008

[2.62] RF Front-End. World Class Designs, J. S. Love, Elsevier, 2009

[2.63] High-Linearity RF Amplifier Design, P. B. Kenington, Artech House, 2000

[2.64] A Self-Calibrating 900-MHz CMOS Image-Reject Receiver, R. Montemayor and B. Razavi, Proc. of ESSCIRC, pp. 292-295, 2000

[2.65] www.maxim-ic.com

[2.66] RF & Wireless Technologies, B. Fette et all, Elsevier, 2008

[2.67] Data Conversion Handbook, W. Kester, Elsevier, 2005

[2.68] Multiband RF – sampling receiver front–end with on–chip testability in 0.13 μm CMOS, R. Ramzan, S. Andersson, J. Dabrowski and C. Svensson, Analog Integrated Circuits and Signal Processing, Vol. 61, No. 2, 2009

[2.69] All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS, R. B. Staszewski et all., IEEE Journal of Solid-State Circuits, Vol. 39, No. 12, 2004

[2.70] www2.**imec**.be

[2.71] http://kabenwireless.com

[2.72] A Blocker Filtering Technique for SAW-Less Wireless Receivers, H. Darabi, IEEE Journal of Solid-State Circuits, Vol. 42, No. 12, pp. 2766-2733, 2007

[2.73] Blocker filtering low-noise amplifier for SAW-less Bluetooth receiver system, H. Seo, H. Song, C. Park, J. Yoon, I. Choi and B. Kim, International Journal of Microwave and Wireless Technologies, Cambridge University Press and the European Microwave Association, Vol. 1, No. 5, pp. 447 – 452, 2009

[2.74] A Highly Linear SAW-Less CMOS Receiver Using a Mixer With Embedded Tx Filtering for CDMA, N. Kim, L. E. Larson and V. Aparin, IEEE Journal of Solid-State Circuits, Vol. 44, No. 8, pp. 2126-2137, 2009

[2.75] A Low-Power, Low-EVM, SAW-Less WCDMA Transmitter Using Direct Quadrature Voltage Modulation, X. He and J. v. Sinderen, IEEE Journal of Solid-State Circuits, Vol. 44, No. 12, pp. 3448-3458, 2009

[2.76] A Single–Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and +90 IIP2, D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han and A. Raghavan, IEEE Journal of Solid-State Circuits, vol. 44, No. 3, pp. 718-739, 2009

3. GYRATOR BASED TRANSISTOR ONLY SIMULATED INDUCTORS FOR RF DESIGN

3.1 Introduction

Although scaling in CMOS technology offered only benefits for RF transceivers in terms of speed, operating frequency (f_T^{90nm}=100 GHz, f_T^{45nm}=280 GHz and expected f_T>400GHz for L<32 nm [3.1]), chip area and power consumption, the silicon on–chip passive inductances do not benefit from technology scaling [3.2]. This justifies the development of active implementations to replace passive inductors mainly in RF design where they cannot be avoided. Since most active inductors are implemented with gyrators, a detailed review of the gyrator theory is presented in the following.

The gyrator invention in 1948 by Bernard D. H. Tellegen (1900–1990) facilitated the development of integrated active filters. The concept has been widely deployed in low frequency design where operational transconductance amplifiers (OTAs) were used to simulate grounded or floating inductors making use of external on–chip capacitors. Since these OTA based simulated inductors are not suitable for higher frequencies, other architectures with improved frequency capability were proposed.

During the last decades, many gyrator based simulated inductors, implemented with several transistors and internal/external capacitors, have been reported. **T**ransistor **o**nly **s**imulated **i**nductors (TOSI), implemented with internal parasitic capacitors, constitute a promising solution for RF design when implementing RF preselective filters (to replace external SAW filters), low noise amplifiers, current controlled oscillators and RF bandpass amplifiers. All these implementations exploit either the inductive behavior or the frequency selectivity around the self resonance frequency. In the following, a first section is entirely dedicated to the gyrator concept.

The state of the art in transistor only simulated inductors (TOSI) is presented in the second section where many architectures proposed in literature during the last decades are described. Calculations are left for the next chapter since the way gyrators are implemented with transistors is of high interest.

A last section is dedicated to higher order TOSI architectures designed for filtering applications.

3.2 Gyrator model

3.2.1 Ideal Gyrator and its Applications in Circuit Design

In linear network theory, impedance inverters and converters are important building blocks in many circuit design applications two of them being the 'gyrator' and 'negative impedance converter'.

It is well known that a linear n–port is said to be a reciprocal network if the port voltages and currents satisfy Eq. (3.1):

$$\sum_{k=1}^{n}[v_k^{(1)}i_k^{(2)} - v_k^{(2)}i_k^{(1)}] = 0\,, \tag{3.1}$$

where $v_k^{(1)}, i_k^{(1)}$ and $v_k^{(2)}$, $i_k^{(2)}$ are two distinct sets of port voltages and currents that fulfill Kirchhoff's laws for linear n–port [3.3]. If (3.1) is not satisfied, this n–port is said to be nonreciprocal. Tellegen had the idea of isolating the nonreciprocity of a linear passive n–port in a single network building block and thus the concept of gyrator was obtained (Fig. 3.1) [3.4]. This 2–port is necessary and sufficient to implement this idea.

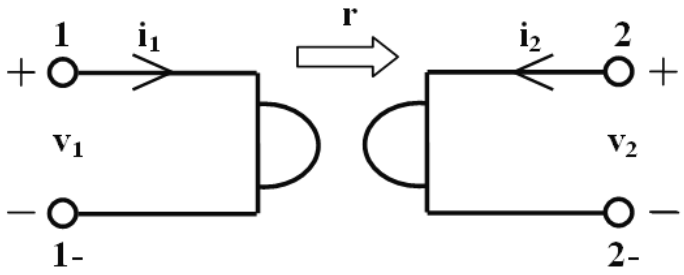


Fig. 3.1 The ideal 2–port gyrator

As a 2–port network, the gyrator is described by the open–circuit impedance matrix [Z]:

$$\begin{cases} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = [Z]\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \\ [Z] = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} 0 & -r \\ r & 0 \end{bmatrix} \end{cases} \tag{3.2}$$

where *r* is the gyration resistance.

As it can be seen from (3.2), any gyrator is fully described by its gyration resistance r and orientation. Rewriting (3.2), Eq. (3.3) is obtained:

$$\begin{cases} v_1 = -r\, i_2 \\ v_2 = r\, i_1 \end{cases} \Leftrightarrow \begin{cases} i_1 = \dfrac{v_2}{r} \\ i_2 = -\dfrac{v_1}{r} \end{cases} \Leftrightarrow v_1 i_1 + v_2 i_2 = 0 \tag{3.3}$$

Eq. (3.3) states that no energy is generated, dissipated or stored since the input power is equal to the output one. Taking into account the reciprocity condition which requires det Z=1, the ideal gyrator is a nonenergic nonreciprocal 2–port since $z_{11}z_{22} - z_{12}z_{21} \neq 1$.

When the gyrator is loaded by an impedance Z_L (therefore 1–port) in practical implementations (Fig. 3.2) then its input impedance is expressed by Eq. (3.4).

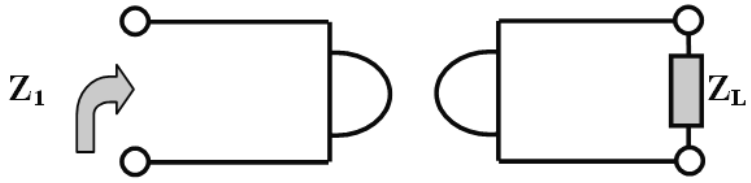


Fig. 3.2 Gyrator terminated in an impedance Z_L

$$[Z] = \begin{bmatrix} Z_{11} & z_{12} \\ z_{21} & Z_L \end{bmatrix} \Rightarrow Z_{11} = -\frac{z_{12}z_{21}}{Z_L} = \frac{r^2}{Z_L} \tag{3.4}$$

The last relation shows that when impedance terminated, the ideal 2–port gyrator represents an ideal positive impedance inverter and from this point of view it represents a two–port circuit whose input impedance is inversely proportional to the load impedance. Consequently, when terminated on an ideal capacitor C the gyrator input impedance is an ideal inductor (3.5):

$$Z_{11} = \frac{r^2}{Z_L} = r^2 sC = sL_{11} \tag{3.5}$$

Relation (3.5) is very important since it proves the possibility of using ideal gyrators and capacitors to implement simulated inductors, circuit design method exploited for over 60 years mainly in low frequency filter design. The simulation of grounded and floating inductors with gyrators is illustrated in Fig. 3.3.

From 1948, many papers have been proposed on the use of gyrator model in circuit synthesis, beside the inductor simulation. One of them refers to the possibility of implementing coupled coil inductors. Thus, the gyrator theory may be used to simulate

not only floating/grounded inductors but also coupled inductors, as reported in [3.5]. The modified gyrator is showed in Fig. 3.4, the inductance values being described by Eq. (3.6).

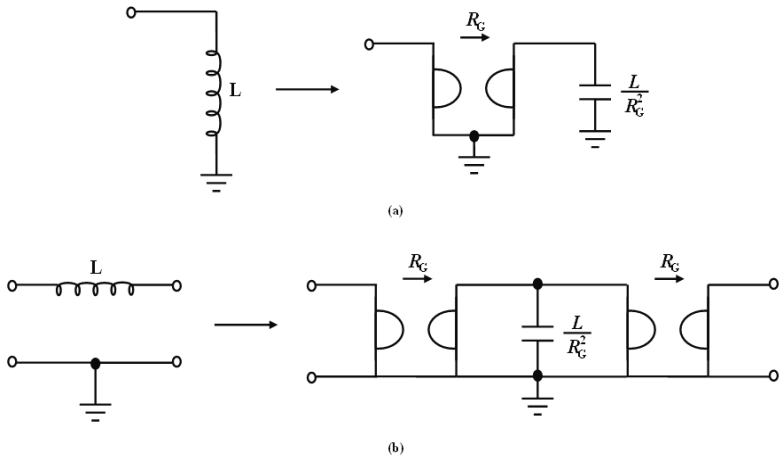


Fig. 3.3 (a) Grounded and (b) floating inductor implemented with gyrators

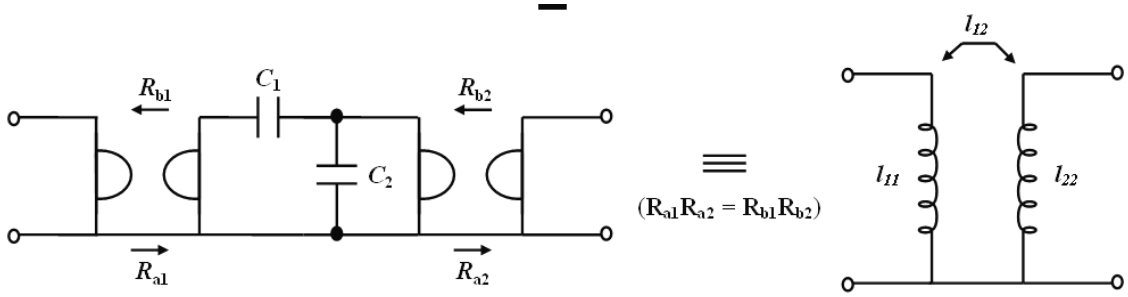


Fig. 3.4 Coupled coil simulation

$$\begin{cases} L = \begin{bmatrix} R_{a_1} R_{b_1} C_1 & R_{a_1} R_{a_2} C_1 \\ R_{a_1} R_{a_2} C_1 & \dfrac{R_{a_1}}{R_{b_1}} R_{a_2}^2 (C_1 + C_2) \end{bmatrix} \\ R_{a_1} R_{a_2} = R_{b_1} R_{b_2} \end{cases} \tag{3.6}$$

A generalized method is proposed for synthesizing any positive real driving–point impedance with cascaded capacitor–gyrator sections terminated in a single resistance [3.6]. According to this method, a particular transfer function as expressed by (3.7) may be synthesized as shown in Fig. 3.5. The method is fully presented in the mentioned paper.

$$Z = \frac{s^3 + \frac{14}{3} s^2 + 2s + 4}{s^3 + 4s^2 + \frac{44}{3} s + 2} \tag{3.7}$$

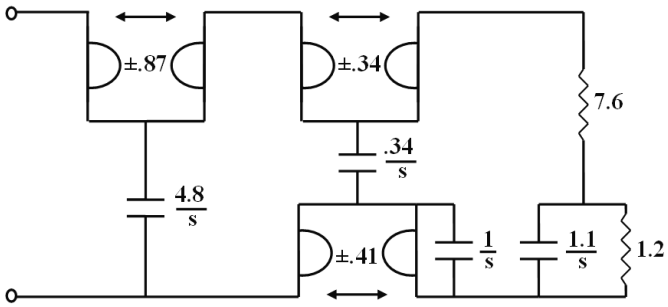


Fig. 3.5 Synthesis of the Z impedance given by (3.7)

A gyrator circuit containing only three (bipolar) transistors and behaving like a two–way feedback system with transfer immitance parameters equal in magnitude and opposite in phase has been proposed in [3.7]. No negative resistance was required to compensate the residual input and output impedances and furthermore this architecture may be cascaded in between two RC two–port networks to realize complex conjugate poles with reduced pole sensitivity to gyration resistance changes.

A review of the gyrator application to filter design is presented in [3.8] where the bidirectional facility offered by capacitor loaded gyrators is emphasized.

3.2.2 Gyrator Practical Implementations

Since gyrators can not be directly implemented, the gyration function must be emulated with appropriate blocks. In practice, active implementations are preferred for gyrator implementation, the synthesized impedance suffering from different limitations. Obviously, designing good gyrators strongly depends on the technology development. Historically speaking, the gyrator concept was tested at low frequencies, the first gyrator being actively implemented with operational amplifiers. The Antoniu's GIC architecture [3.9], presented in Fig. 3.6, is a well known architecture with respect to low frequency implementations.

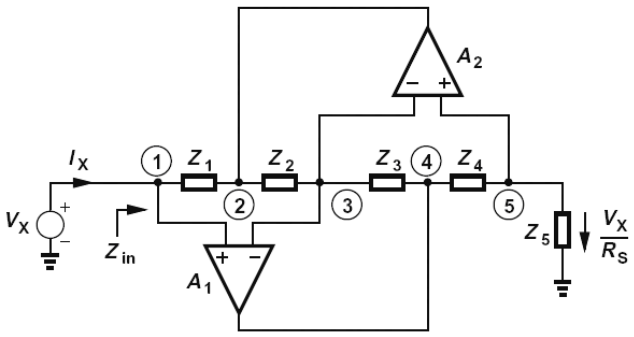


Fig. 3.6 Antoniu's architecture [3.9]

For this implementation, the ideal op amps A_1 and A_4 are used in feedback loop forcing the voltages V_1, V_3 and V_5 be equal. By calculating the currents through $Z_1 – Z_5$, the Antoniu's structure input impedance is obtained as:

$$Z_{11} = \frac{V_1}{I_1} = (\frac{Z_1 Z_3}{Z_2 Z_{Z4}}) Z_5 \tag{3.8}$$

In order that Z_{11} be a simulated pseudo passive inductor, it is necessary that $Z_{1,3,5}$ be resistances ($R_{1,3,5}$) and Z_2 (type–A) or Z_4 (type–B) be capacitor (and correspondingly Z_4 or Z_2 be resistors). By a corresponding change of the gyrator architecture, it becomes an impedance convertor and can be used for implementing FDNRs. More details may be found in [3.10].

Since the operational amplifiers are useful only for low frequencies (KHz range, maximum tens of MHz), OTAs are used for higher frequencies (tens–hundred MHz). The idea of using OTAs resides in the fact that from rel. (3.3) the gyrator may be interpreted as a connection between an inverting transconductor and a non–inverting one, in which case $r^2=1/gm_1gm_2$. If identical transconductors are used, their common value is $g_m=1/r$. Thus, the grounded gyrator will consist of two transconductors in negative feedback: one with an inverting and the other one with a non–inverting input (Fig. 3.7), the gyrator being described in this case by (3.9).

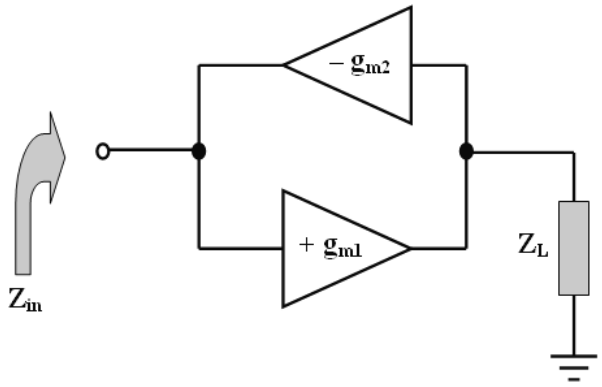


Fig. 3.7 Realization of grounded gyrator

$$[Z] = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{g_{m1}} \\ \frac{1}{g_{m2}} & 0 \end{bmatrix} \tag{3.9}$$

Operational transconductance amplifiers make filter design much easier since they have better frequency performances than operational amplifier and therefore gyrators with enhanced frequency response may be implemented. An example of active inductor

simulated with OTA is presented in Fig. 3.8, for grounded inductor and floating one respectively.

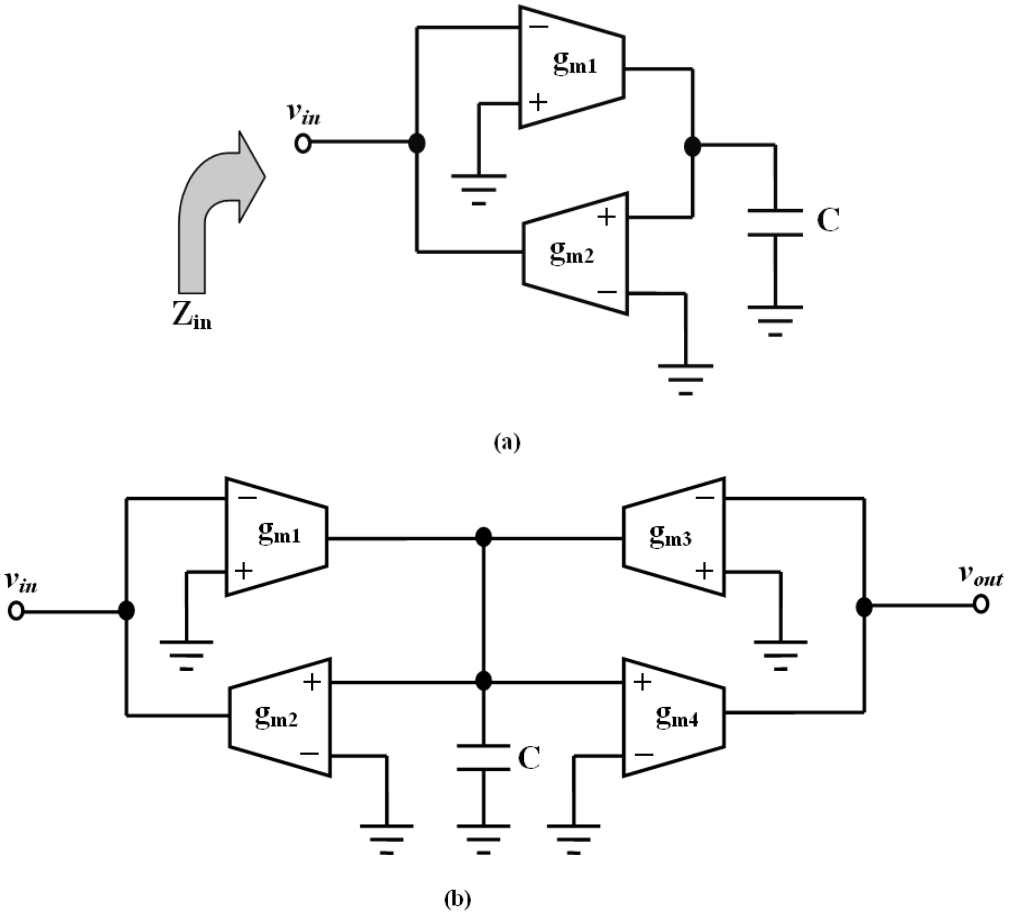


Fig. 3.8 Grounded (a) and floating (b) simulated inductor

Another particular scheme [3.11] directly implements the gyration function since in order to realize an ideal gyrator, the small–signal input current (denoted as i_{in}) must be proportional to the product between the port voltage v_{in} and the terminating load impedance 1/(jωC). Thus, if we denote the input gyrator node as X and the voltage and current associated with this node with V_X and I_X respectively, we have:

$$-I_X = -g_{m2}(g_{m1}V_X \times \frac{1}{sC}) \Rightarrow \frac{V_X}{I_X} = \frac{sC}{g_{m1}g_{m2}} = sL \tag{3.10}$$

In this case, neither OTAs nor single transistors are used to implement the gyration function but two independent stages (Fig. 3.9 – left).

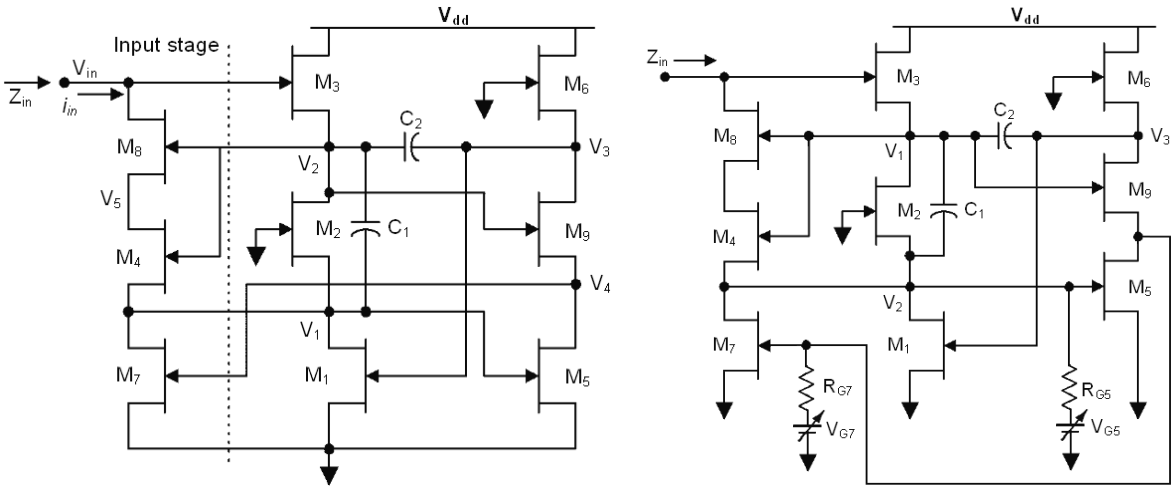


Fig. 3.9 MESFET simulated inductor [3.11] – left and improved one [3.12] - right

The first input stage is a voltage–to–current converter. The second one is a six–MESFET frequency–dependent voltage generator. The circuit behaves as a gyrator with tunable series loss resistance where C_1 is the gyrator load. To implement an ideal gyrator, it is necessary that i_{in} be proportional to the product between the port voltage v_{in} and the terminating load impedance $1/(j\omega C_1)$. This condition can be fulfilled if a small–signal voltage, proportional to the load impedance and linear function of v_{in}, can be generated. For the same circuit, the required frequency–dependent voltages are given by V_1 and V_2 and their difference $V_2–V_1$ is converted to a proportional current by the input stage thus setting i_{in} as required. M_1, M_2 and M_3, used in a common–source cascade topology, generate V_1 and V_2 in such way that if the current i_{in} is proportional to V_1 or V_2, both (simulated) L_{eq} and R_{loss} will depend on C_1 and C_2. The inductance independence from R_{loss} is obtained if it does not depend on both C_1 and C_2 fact that is accomplished with a second cascade arrangement (M_5, M_6 and M_9) which forms a feedback loop.

The input stage (M_7, M_4 and M_8) represents a voltage–to–current conversion that sets the input impedance Z_{in} inversely proportional to $V_2–V_1$ (voltages generated by the second 6 transistors block). M_4 sets the small–signal input current equal to $g_{m4}(V_2–V_1)$ resulting in an input impedance with resistive and inductive terms only and with the required independent tunable inductance and series resistance. If M_7 and M_4 are matched then M_9 sets the drain current of M_7 to $g_{m4}(V_2–V_1)$ and has no effect upon the feedback voltage V_3. The input stage has no effect on node voltages V_1 and V_2 since M_4 injects a current into node V_1 equal to that pulled from the node by M_7. This architecture was patented in 2001.

An improved version of this simulated inductor which facilitates the tuning of both inductance and series resistance with external dc voltages was proposed in [3.12] and presented in the same Fig. 3.9 – right. Both circuits are intended to be used in the frequency range (0.1–1) GHz.

Another gyrator implementation called 'Meunier gyrator' was proposed in [3.13] which is a compensated gyrator. This method was used to design a 5-nH MMIC inductance for the frequency range 1.5–2.5 GHz by terminating a nonideal transistor gyrator in a special compensating RLC port. This gyrator implementation is based on the Meunier negative resistance circuit (Fig. 3.10 left) whose input impedance is given by Eq. (3.11).

$$Z_{in} = -\frac{1}{g_{m1}g_{m2}R} \tag{3.11}$$

The idea is that by connecting a third transistor stage the same way the previously mentioned negative resistance is created, the Meunier gyrator circuit is also obtained (Fig. 3.10 right).

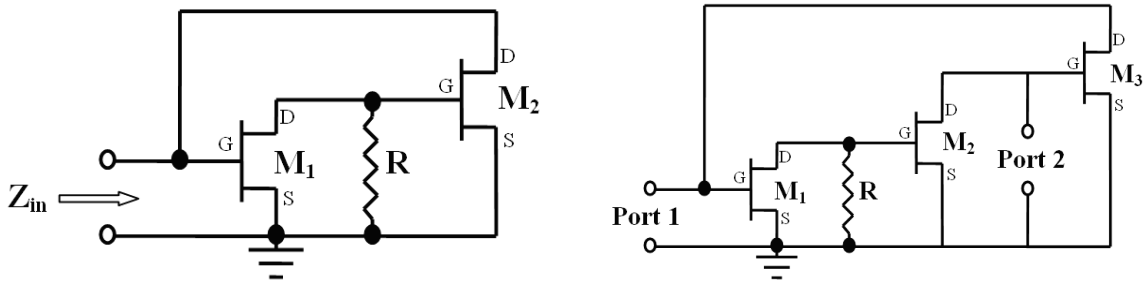


Fig. 3.10 Meunier negative resistance and gyrator circuit [3.13]

It can be proved that in this case, the input impedance is given by (3.12) if a load capacitor C_L is used:

$$Z_{in} = s\frac{C_L}{g_{m1}g_{m2}g_{m3}R} \tag{3.12}$$

As it can be seen, the passivity of the gyrator is not necessary. However, the circuit has parasitics which affect the gyrator function and consequently, by connecting a corresponding passive network to the Port 2, used as a compensating network, an ideal inductor is seen at the input Port 1. The final gyrator circuit used to simulate an ideal inductance is given in Fig. 3.11 together with the simulation results.

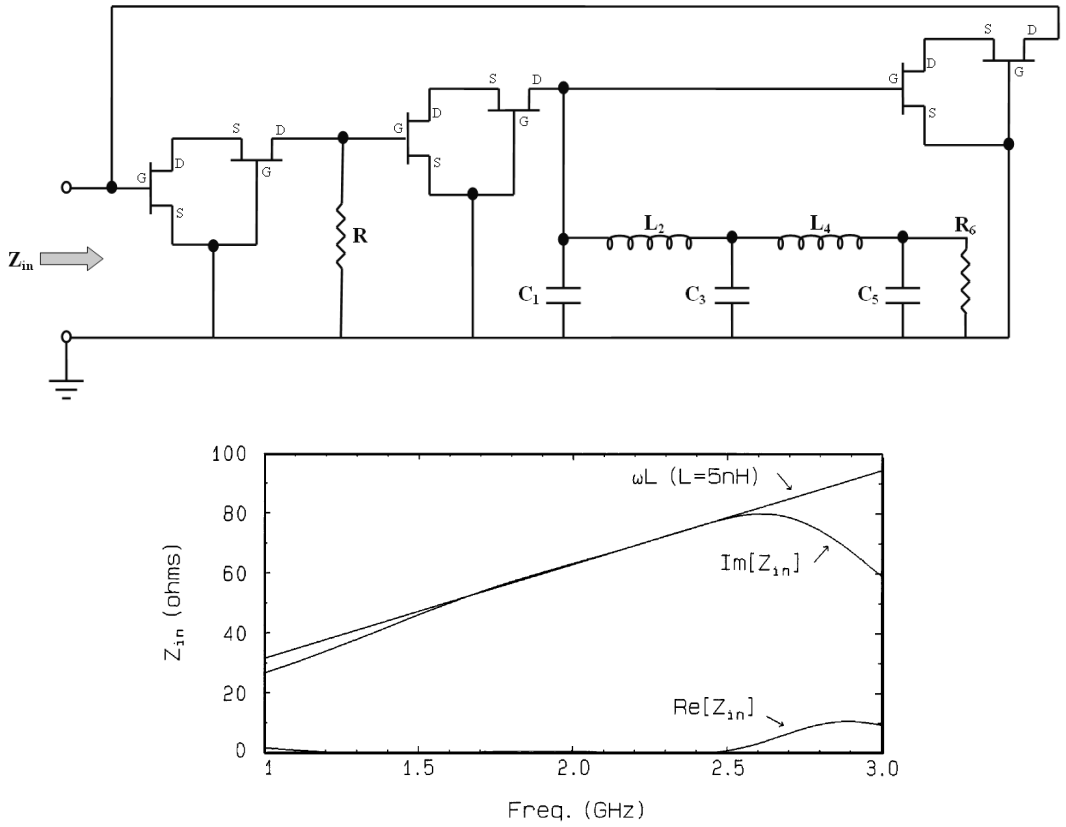


Fig. 3.11 MMIC Inductance simulated with the Meunier gyrator [3.13]

Although the final circuit does not implement a gyrator, a similar idea of obtaining an active inductor at the input of a 3–port simply by connecting a passive inductor to another input was proposed in [3.14]. Active inductor with very good quality factor values can be obtained, being suitable for millimeter wave applications (the frequency range 15–30 GHz). The 3–port is represented in fact by a single common gate transistor with proper biasing (not shown) as presented in Fig. 3.12. The total current consumption is 1.2 mA for a supply voltage of 1.5V.

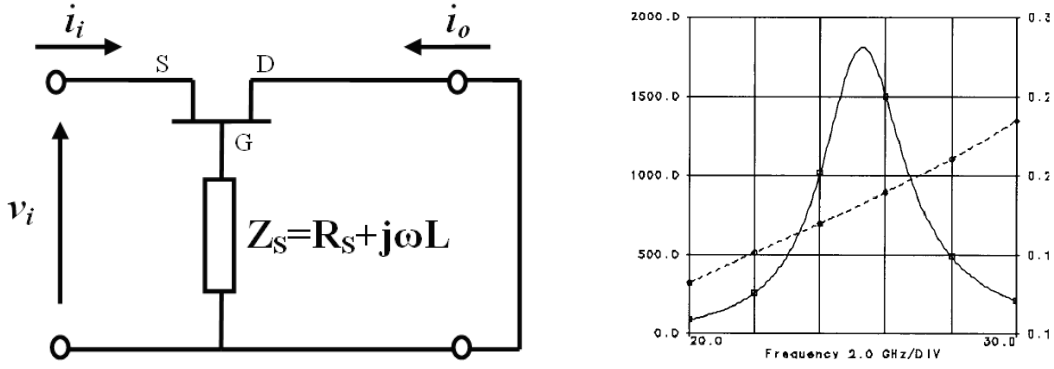


Fig. 3.12 Common gate network active inductor and its quality factor [3.14]

Although not based on the gyrator theory, another interesting active inductor implementation [3.15] based on a cross–coupled configuration and proposed for VCO applications is shown in Fig. 3.13. The active inductor is simulated by transistors $M_{1\text{-}6}$ and the phase noise achieved for this configuration is from –101 to –118 dBc/Hz at a 1–MHz offset within the entire frequency range (0.5 – 3 GHz).

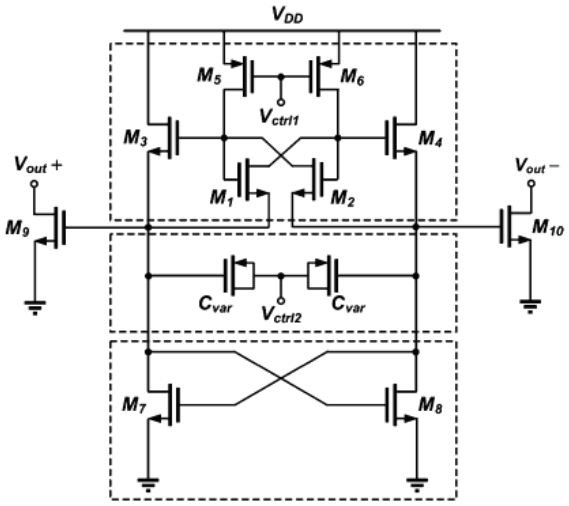


Fig. 3.13 Wide–tuning range VCO with simulated inductor [3.15]

3.2.3 The Gyrator Power Transfer

The first issue when implementing gyrators with either operational amplifiers or transconductors is to design them in such way that $z_{12}=z_{21}=r$ or equivalently $g_{m1}=g_{m2}$. If this relation is fulfilled then an ideal passive gyrator is obtained, the relation (3.3) being accomplished. Since operational amplifiers used in practice are not ideal and it is very difficult to achieve equal transconductances (due to mismatch or design specs), the passivity of the gyrator is no longer maintained and parasitic inductances are obtained to the ground. In other words, the Eq. (3.3) is no longer fulfilled. In general, the gyrator is active if $z_{12}\neq z_{21}$ and in this case the gyrator amplifies the signal in one direction and acts as an attenuator in the opposite direction. Thus, this (in)equality has an intrinsic important implication on the gyrator power transfer since if $g_{m1}\neq g_{m2}$ different powers are obtained to the output port as described in Fig. 3.14 and as stated also in [3.16].

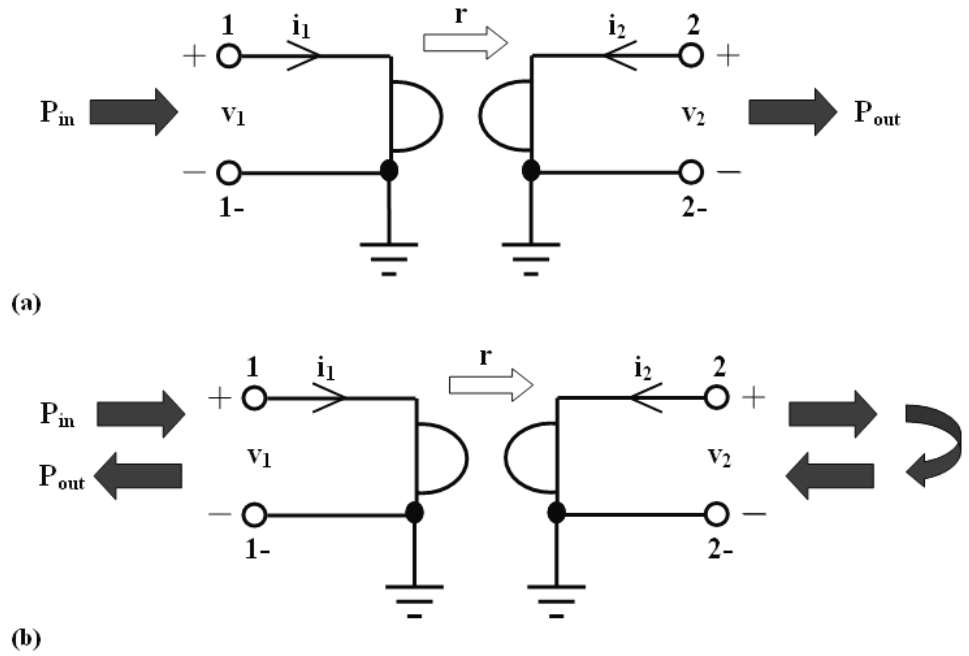


Fig. 3.14 Grounded gyrator with signal power flowing from terminal 1 to terminal 2 (a) and back (b) [3.16]

In general, if the power is taken from the second gyrator port (Fig. 3.14a), since $P_{out}=(g_{m1}/g_{m2})P_{in}$ and the gyrator is passive, the output power is equal to the input one. An increased output power is obtained if $g_{m1}>g_{m2}$. In the second case, e.g. the power is taken from the same port (Fig. 3.14b), the transconductances mismatch has no effect on the output power since $P_{out}=(g_{m1}/g_{m2})(g_{m2}/g_{m1})Pin=P_{in}$.

However, as demonstrated in [3.17], the power transmission for OTA based grounded inductor (Fig. 3.8a) is unity, similar to real passive inductors, being independent on the relation between the transconductances (g_1, g_2) while in the case of floating inductors is unity when $g_1g_3=g_2g_4$. Therefore, the design of active inductors is much more relaxed when talking about power efficiency and therefore the equality of the transconductances is not critical.

However, a drawback for the active gyrator implementation still remains since its parameters z_{12} and z_{21} are in practical applications frequency dependent and constant as in passive case only in a small bandwidth.

3.2.4 Gyrator and the Series/Parallel Simulated Inductor Equivalent Model

The main issue in transconductor design is its finite input and output resistances [3.18] as shown in Fig. 3.15 (in this case considered identical). Thus, the OTA introduces

a supplementary output conductance to the circuit which appears across the input and load gyrator terminals. Moreover, the second design issue regards the other two gyrator parameters z_{11} and z_{22} which become nonzero for practical implementations, i.e. $z_{11}\neq 0$, $z_{22}\neq 0$. In other words, their finite value will contribute to the value of the simulated impedance, making the design a little more difficult.

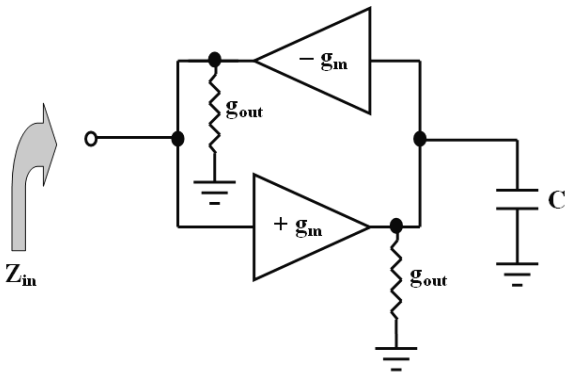


Fig. 3.15 Capacitively loaded gyrator with nonzero OTA output conductances

In order to establish the equivalent model of the inductor simulated with non–ideal transconductances (as presented in Fig. 3.15), the gyrator impedance conversion rule described in Fig. 3.16 must be reconsidered. Thus, an important aspect regarding the gyrator theory refers to the interdependence between the equivalent series/parallel inductor model and the loading gyrator impedance. This conversion rule is very useful for a good understanding of TOSI structures studied in the following sections. The idea is that a series circuit is converted by the gyrator into a parallel one and vice–versa.

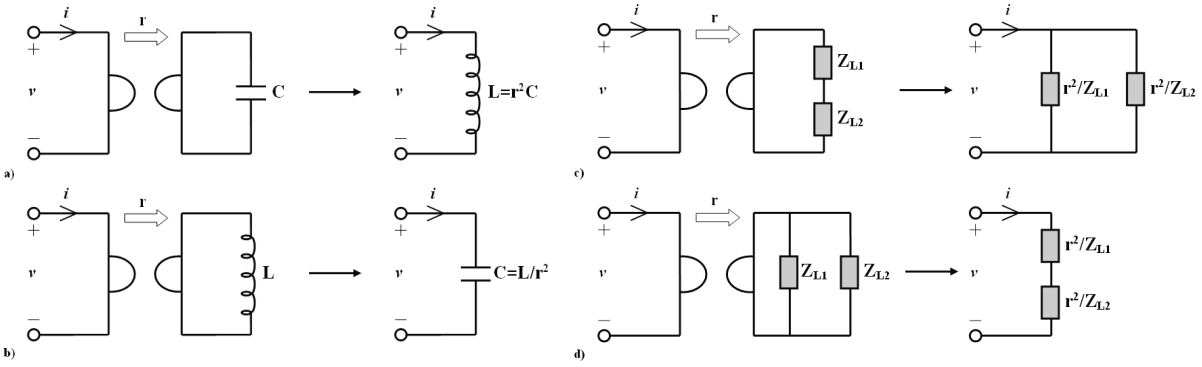


Fig. 3.16 Loading an ideal gyrator [3.16]

This conversion rule is used to obtain the equivalent model for grounded (Fig. 3.17) and floating (Fig. 3.18) inductors simulated with a real RC circuit.

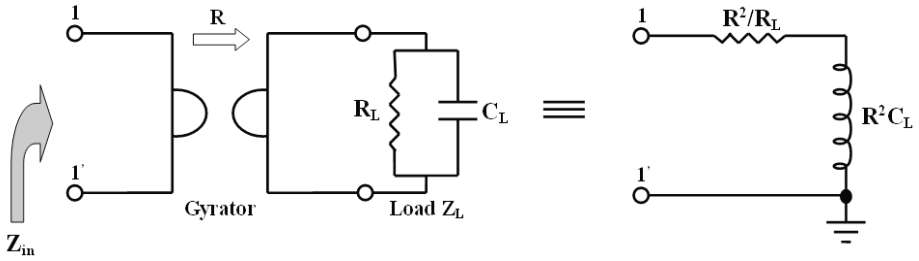


Fig. 3.17 Simulation of a real grounded inductor

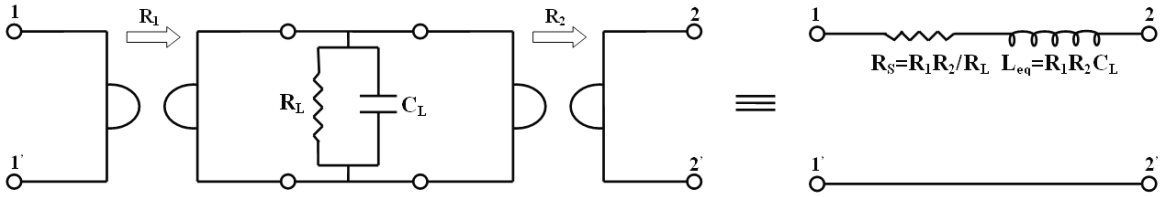


Fig. 3.18 Simulation of a real floating inductor

With these configurations, the parallel RC circuit in Fig. 3.15 has the equivalent model for its simulated grounded inductor shown in Fig. 3.19 and emphasized in [3.17] too.

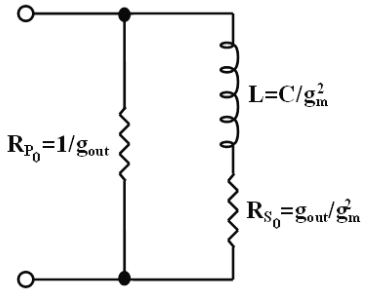


Fig. 3.19 The equivalent circuit of the simulated lossy inductor

It is obvious that the output conductance of the non–inverting transconductor stage sets the inductor series resistance while the conductance of the inverting transconductor stage sets the parallel inductor loss resistance. As stated in [3.18], the output conductance sets the maximum transconductor gain at dc, since $A_{dc} = g_m/g_{out}$ while the simulated inductor quality factor is one half the transconductor dc gain ($Q = g_m/2g_{out}$). The use of cascode transistors may represent a solution to minimize the output conductance and thus obtaining low loss simulated inductors.

It becomes clearer now that using good transconductors is compulsory when designing simulated inductors. However, practically it is impossible to design transconductors with very high output resistances and in most cases a negative resistance is used to compensate the inductor losses.

Finally, for any loaded capacitor non–ideal gyrator the followings are valid:

- the equivalent model is a series circuit consisting of the simulated inductor (L_S) and its parasitic resistance (r_S);

- both series elements are frequency dependent;

- having a parasitic resistance, the inductor has a finite Q whose maximum value is independent of frequency;

- the maximum quality factor value is dependent on the gyrator parasitic conductances and this is the reason why they should be minimized as possible, as stated also in [3.19].

3.2.5 The Effect of the Parasitic Capacitors on the Simulated Inductor

This problem has two aspects:

1. The first one is related to the internal transconductor poles. Thus, any transconductance implemented with compound transistors stages exhibits supplementary poles due to the internal parasitic capacitors which produce a phase shift at high frequencies. The main effect on the simulated inductors implemented with OTAs is the introduction of a negative resistance in parallel to the simulated inductor, as shown in Fig. 3.20:

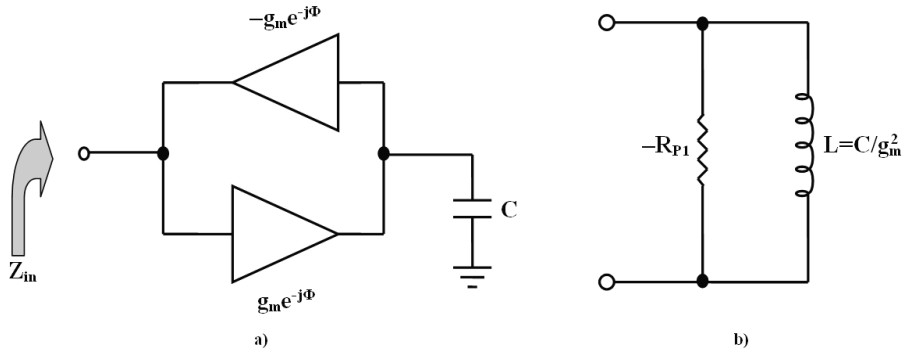


Fig. 3.20 (a) Phase lag and (b) negative loss in the simulated inductor [3.18]

The effect of this negative resistance is a parasitic increase in filter gain beyond the design specifications at resonance when the inductor is used in a bandpass filter. To avoid this effect, the gyrator poles should lie beyond 4Q times the resonant frequency which means using fast analog circuits.

2. The second aspect refers to the input and output transconductance parasitic capacitors which strongly affect the overall gyration function. A more complete high frequency transconductor model is showed in Fig. 3.21 [3.20].

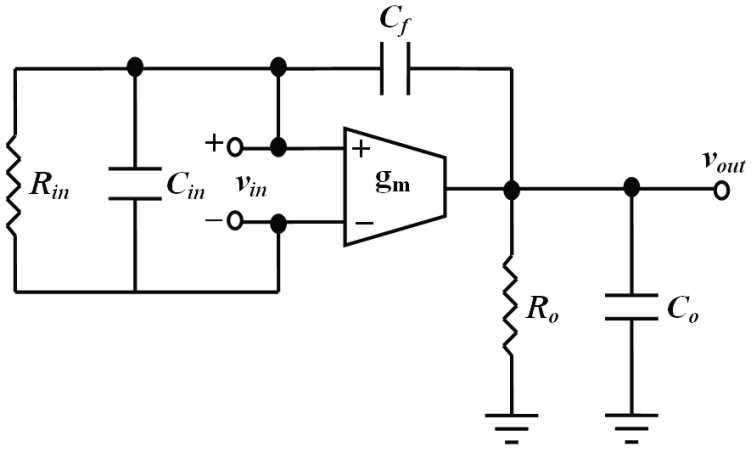


Fig. 3.21 High frequency OTA macromodel

In this case, the complete equivalent model of the lossy simulated inductor in Fig. 3.15 is shown in Fig. 3.22 where C is the load capacitor, $C_{i,o}$ is the parasitic capacitor of the input/output terminals, C_s is the bottom–plate–to–substrate parasitic capacitor as stated by (3.13).

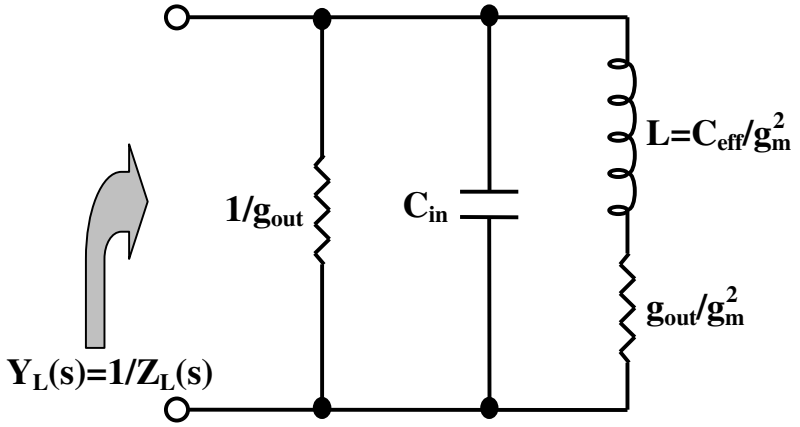


Fig. 3.22 Passive equivalent circuit for OTA–C simulated grounded inductor

$$\begin{cases} C_{in} = C_i + C_o \\ C_{eff} = C + \frac{1}{2}\left(\frac{C_s}{2} + C_{in}\right) \end{cases} \tag{3.13}$$

In other words, the simulated inductor has a RLC resonator equivalent scheme with a self resonant frequency expressed by (3.14):

$$\begin{cases} \omega_0 = \dfrac{1}{\sqrt{L_{eff}\, C_{in}}} \\ L_{eff} = \dfrac{C_{eff}}{g_m^2} \\ Q_L = \dfrac{\omega L_{eff}}{g_o} \end{cases} \tag{3.14}$$

Relations (3.14) are important when designing OTA–C based simulated inductors and an interesting point is that these structures have similar RLC equivalent passive model as the TOSI architectures.

Regarding its sensitivity to parasitic capacitors, the gyrator is sensitive to transconductance parasitic capacitors which influence the frequency behavior. For example, the inductance value of the inductor simulated in [3.20] was degraded at 1.42 GHz with about 80% from its original low frequency inductance value measured at 171 MHz.

However, OTA based simulated inductors are not used in implementations where cascaded g_m–C cells are preferred (as interconnected integrators). In any case, OTA based simulated inductor architectures cannot be used in the GHz range and therefore other gyrator based architectures must be developed as presented in the following section.

3.3 Proposed TOSI Architectures for RF Design

3.3.1 TOSI Concept

From the theory of analog circuit design [3.21] it is well known that the number of poles of a transfer function is dependent on the number of circuit nodes (containing grounded capacitors) and thus, using a large number of transistor stages will degrade the frequency capability. This is the reason why transconductances (OTAs) cannot work at higher frequencies due to their increased number of parasitic capacitors and thus gyrator implementations for GHz domain with OTAs is practically impossible. The single solution while still using the gyrator principle is to reduce the transistors number, fact that signifies actually a consequently replace of transconductors with simpler stages with similar function. Since transistors are in fact transconductors, the idea was to replace the entire OTA with single transistor stages properly biased. The gyrator will consist in this case of an inverter and a non–inverter transistor stage in negative feedback. Since these transistors have intrinsic parasitic capacitors, the simulation of inductors is based on the idea of using these transistor parasitics. Thus, no need for external capacitors is required, representing an important technique for chip area minimization. Since the parasitic capacitors have values of tens – maximum hundred fF, the self resonant frequency is in GHz domain, these inductors being limited in the GHz domain only by the technological

limitations, since mathematically speaking they can achieve frequencies higher than 10 GHz.

During the last decades, many TOSI architectures have been proposed in literature, several of them making use of varactors or even external capacitor in order to increase the parasitic capacitor if necessary. Several have been implemented, positively tested and some patented too. In other words, there is no 'mystification' on the TOSI concept and furthermore this is not only a theoretical concept, the principle of simulating gyrator with parasitic capacitors proving to be valid. However, the frequency response must be traded off against power consumption, linearity, noise and chip area.

In the following sections, several TOSI architectures proposed until now in literature are presented and their use in different RF applications (current/voltage controlled oscillators, low noise amplifiers, bandpass amplifiers, etc) is exemplified. In other words, only the applications exploiting the inductive behavior are envisaged. Consequently, the simulated inductors are compared in terms of power consumption, chip size and self resonance frequency value.

3.3.2 TOSI Architectures using MESFET Transistors

A well known MESFET based simulated inductor architecture was proposed by Hara in [3.22], presented in Fig. 3.23 together with its equivalent model. A comparison between active and passive implementations in terms of chip area is also presented in Fig. 3.23, proving that the former is superior.

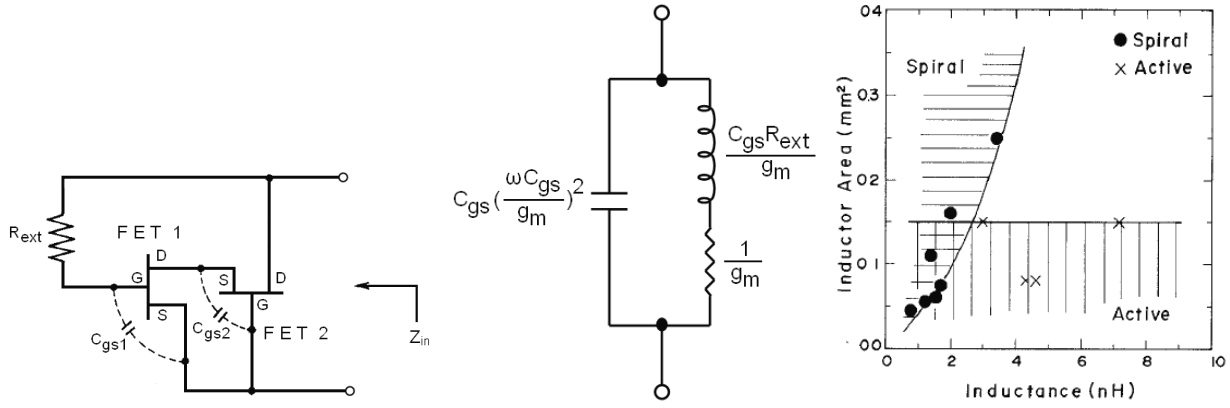


Fig. 3.23 FET TOSI architecture, its equivalent model and chip area comparison

The active inductor consists of two FET transistors and an external feedback resistance used to change the inductance value which becomes independent of the chip area. It is obvious that the transistor FET_2 is the non–inverting transconductor while FET_1

is the inverting one since the input signal is applied to the gate of FET_1. The gate voltage of transistor FET_2 is used also to change the inductance value. Since parasitic capacitors are used to emulate the inductive behavior, the resulting device is much smaller than in the case of passive inductors and works in GHz domain as well. Due to its particular structure, if both transistors are identical, the parasitic capacitors cancel each other therefore yielding to wide frequency range operation since each transistor has large cut off frequency.

The same simulated inductor was used for implementing a broadband microwave amplifier operating in the frequency range 0.1–10 GHz (Fig. 3.24), its performances being reviewed in the same reference.

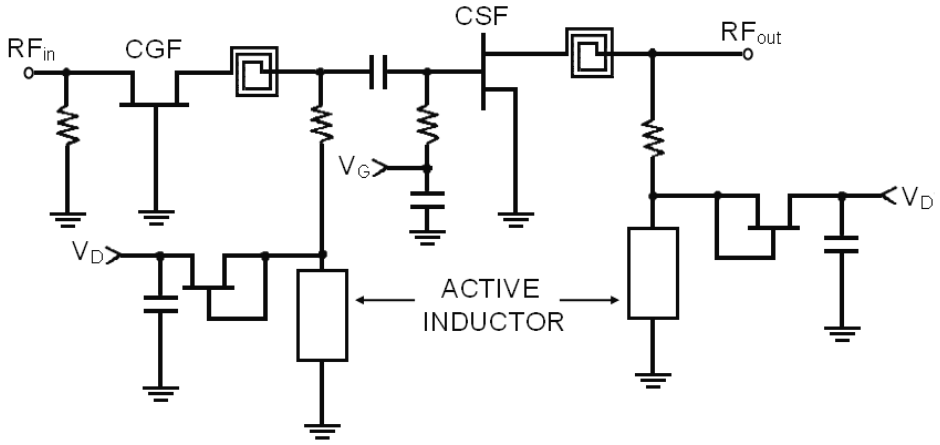


Fig. 3.24 Active matching amplifier with simulated inductor [3.22]

A power divider (Fig. 3.25) using the same inductor was also reported [3.23].

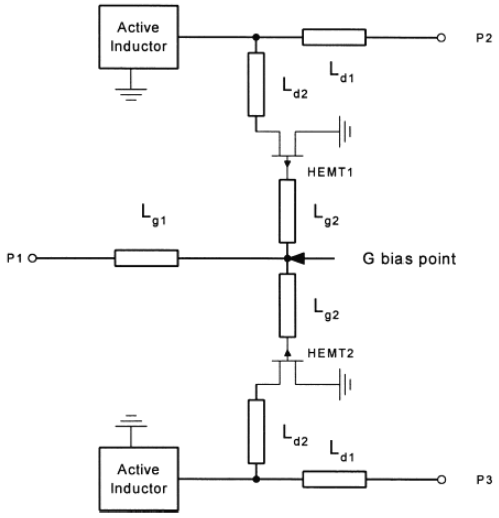


Fig. 3.25 Active power divider with active inductor

Based on this simulated inductor, two other improved architectures were proposed in [3.24] and shown in Fig. 3.26. The first one (Type (a)) implements the external feedback resistance with a FET transistor. In this case, supposing identical gyration transistors, a lossless active inductor is obtained, the configuration being superior to the previous one. Furthermore, by replacing the common gate FET with a cascode configuration, the second configuration (Type (b)) is obtained. Taking into account identical transistors for the cascode and feedback stages, the equivalent circuit consists of a simulated inductor and shunt negative resistance. With this configuration, a lossless active inductor may be obtained by connecting a shunt positive resistance to the input node. A maximum quality factor of 65 was demonstrated at 8 GHz and an infinite one can be obtained with the penalty of potential instability.

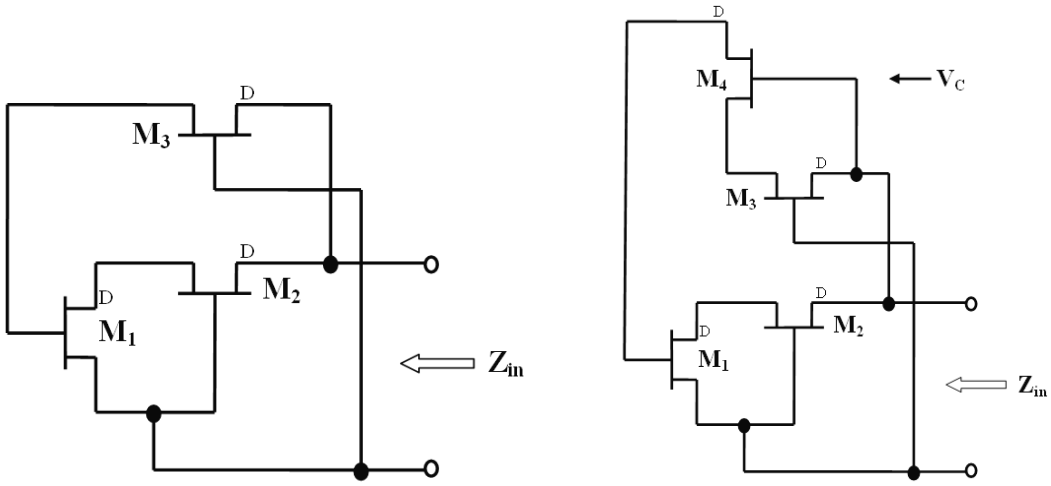


Fig. 3.26 Improved simulated inductors with 3 (left) and 4 (right) FETs [3.24]

As could be noticed, the inductor scheme presented in Fig. 3.26 (b) makes use of a frequency dependent compensation scheme. An improved topology for this architecture (Fig. 3.27) was proposed in [3.25].

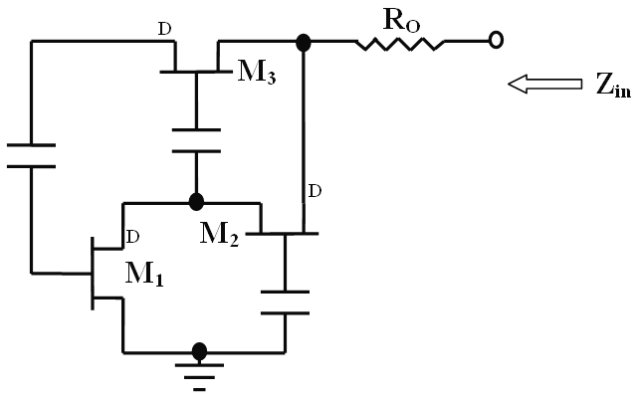


Fig. 3.27 Active Inductor and its equivalent circuit [3.25]

This architecture has better performances (Fig. 3.28) than the previous one since by a suitable change of R_o and g_{m2}, a lossless inductor may be implemented at any frequency. A phase shifter (Fig. 3.29) for GHz domain was designed using this improved architecture [3.26].

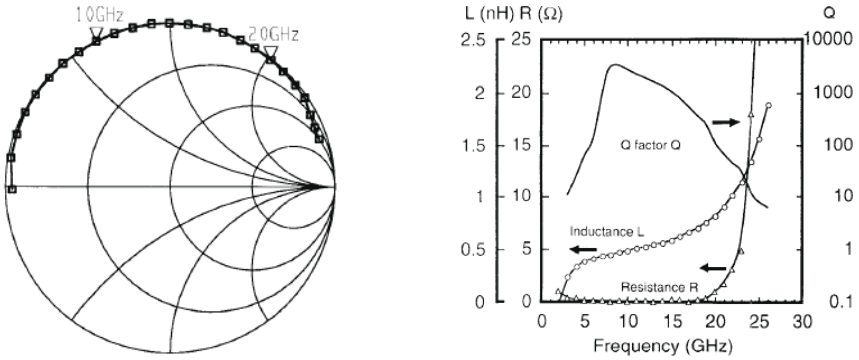


Fig. 3.28 Measured S parameters and impedance characteristics for TOSI [3.25]

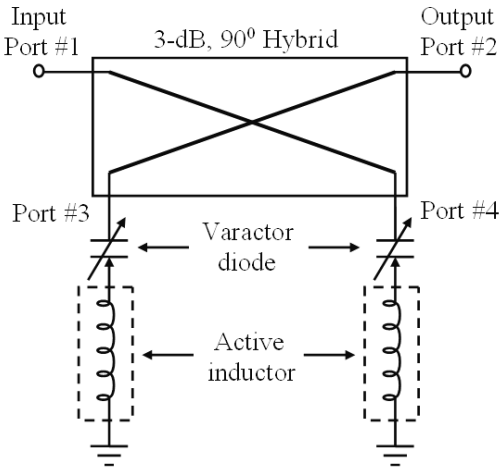


Fig. 3.29 C Band analog phase shifter with FET simulated inductors [3.26]

Another MESFET **t**unable **a**ctive **i**nductor (**TAI**) has been reported in [3.27] and shown in Fig. 3.30 together with the scheme of a VCO implemented with this inductor.

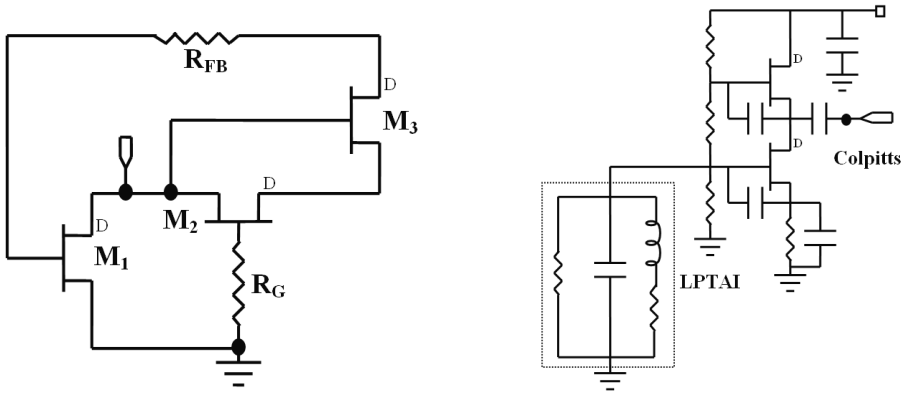


Fig. 3.30 Low power TAI and its application to a VCO implementation [3.27]

As depicted also in Fig. 3.30, the gyrator is simulated with a common source (CS) (inverting stage) and common gate (CG) cascade stage. CG is a used in all active gyrators to implement the inverting transconductor. R_{FB} and R_g are used to control the inductance value and its series loss. Implemented in 0.5 μm MESFET technology, the simulated inductance has several nH and was used to implement a VCO with 35% tuning ratio in the frequency range 2.1 GHz to 3 GHz. The phase noise appears approximately –85 dBc/Hz at 1 MHz offset.

Another MESFET TOSI used also in a VCO implementation, shown in Fig. 3.31 together with its equivalent circuit, has been proposed in [3.28]. The active inductor is simulated by the transistor stages FET_1 – FET_2 – (FET_3 – FET_4) and the transfer function is given by the Eq. (3.15).

It is obvious that the tuning of the transconductance g_{m2} determines an independent tuning of the negative resistance. Consequently, a lossless simulated inductor is obtained. The VCO has 50% tuning range, from 1.56 to 2.85 GHz and a power consumption of 80 mW for an output power of 4.4 dBm. The phase noise at 1–MHz offset was less than –110 dBc/Hz.

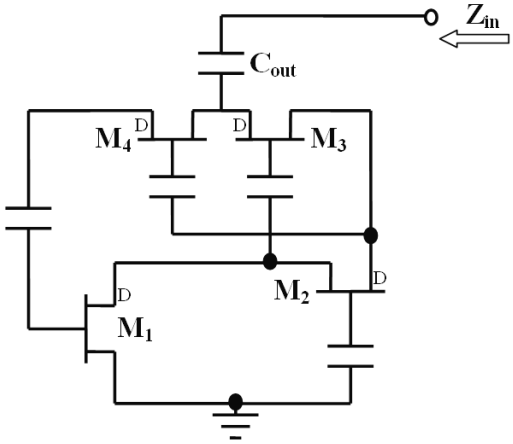


Fig. 3.31 MESFET VCO with simulated inductor [3.28]

$$Z_{out} = j\omega \frac{C_{gs1}}{g_{m1}} \left(\frac{1}{g_{m3}} + \frac{1}{g_{m4}}\right) - \left(\frac{1}{g_{m2}} + \frac{1}{g_{m3}}\right) + \frac{1}{j\omega C_{out}} \tag{3.15}$$

A cascode common source stage together with a non–inverting common gate transistor (Fig. 3.32) is also used to implement an active inductor [3.29]. The tunable active inductor is simulated by T_1 and T_2 used in a cascode configuration and T_3 as a CG stage. The biasing voltage V_{g3} effectively controls the inductor series resistance, V_{g4} controls the inductance value since the transistor T_4 is used as a variable resistor. With

this simulated inductor a wide range of inductance values can be synthesized for a wide range of positive and negative series resistance values (T_3 generates a negative resistance if resistance R_2 is used). The inductor is designed at a frequency of 2 GHz and was used for a practical implementation of a 3–resonator active filter.

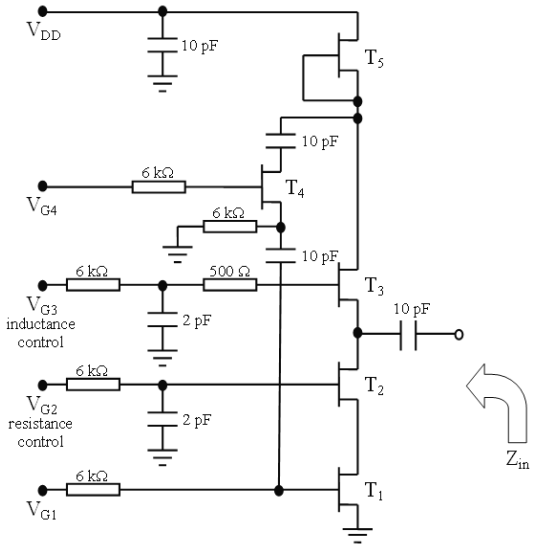


Fig. 3.32 Tunable active inductor [3.29]

A good review but also an original method for the determination of all possible simulated inductors architectures as a function of the number of FET transistors is presented in [3.30]. The space limits and the fact that a throughout study of MESFET simulated inductors is beyond the scope of this thesis, no further details are presented regarding this reference. To conclude this section, MESFET TOSI implementations prove to be more reliable than the inductors implemented in other technologies (CMOS, bipolar) since no negative resistance as a distinct block is required and very good quality factor simulated inductor may be obtained with relatively low power and small chip area. Moreover, the MESFET TOSIs are quite simple and easier to design, being suitable for millimeter wave applications.

3.3.3 CMOS TOSI Architectures

By far the widest used technology in implementing TOSI architectures is the CMOS one. A possible reason may be, as mentioned in Chapter 2, the fact that the most stringent telecommunications standards are in the lower GHz spectrum, up to 5 GHz, exactly the bandwidth served by the CMOS technology. The race for low power, small size, portable and multi–standard terminals has a strong impact on the passive circuits

design, the current trend consisting in a consequent minimization of passive circuits with respect to size and number. This is not a simple task and furthermore is a critical problem since although the CMOS technology evolved to 45 nm, meaning that the chip size reduced with more than 30% during the last years, the number of passive devices used in a mobile terminal is quite large if not almost the same. Since the inductors are required in any application and especially in RF design, an adequate research must be devoted to simulated inductors which can facilitate the implementation of a CMOS RF preselective filter.

This section represents, as the previous one, only a brief review of active inductor topologies implemented in CMOS process aiming any RF application except the filtering one which is presented separately. It is obvious that the continuous technology development determined the researchers to find equivalent CMOS architectures for MMIC and bipolar TOSI implementations which, due to the intrinsic technology properties, facilitates the implementation of low power–cost–chip area circuits. This is the reason why most papers dedicated to simulated inductors, published during the last two decades envisage the CMOS technology.

To our knowledge, the first CMOS TOSI architecture reported in literature is that showed in Fig. 3.33 and proposed in [3.31]. Its small signal equivalent passive model is the same RLC model presented in Fig. 3.20, also available for MESFET inductors (Fig. 3.30).

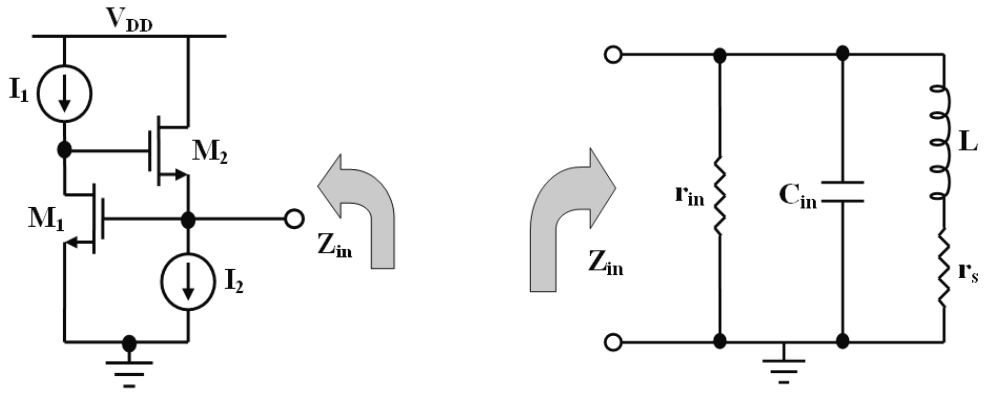


Fig. 3.33 NMOS TOSI and approximate RLC equivalent model [3.31]

The inductive behavior is emulated by an inverting CS stage (M_1) and a non–inverting CD stage (M_2) used in a back–to–back connection. The gyrator loading capacitor is represented by the parasitic capacitor C_{gs}, either of the transistors M_1 or M_2 since identical transistors were supposed to be used in this paper. This represents also

the main particularity of this structure since the gyrator capacitor is connected between the two ports of the gyrator rather than being grounded.

Doing some calculations, a second order transfer function is obtained to characterize the frequency behavior of the inductor in Fig. 3.33, the circuit having a low frequency integration zero, set by the output conductance g_{ds1} ($\omega_z=g_{ds1}/(C_{gs2}+C_{gd1}+C_{gd2})$, and two poles which represent the cut off frequency of each transistor ($\omega_{T1}=g_{m1}/C_{gs1}$, $\omega_{T1}=g_{m2}/C_{gs2}$). Therefore, the circuit proves an inductive behavior from the integration zero up to the ω_{T2} which is the dominant pole. No compensation scheme was proposed for this TOSI.

An interesting approach [3.32] for this architecture consists in the implementation of a high–Q pseudo–passive inductor by combining the TOSI architecture presented above in Fig. 3.33 with a passive on–chip inductor, a novel pseudo–passive inductor being obtained (Fig. 3.34). The idea is to decrease the negative effect of C_{gs2} upon the TOSI quality factor by connecting in the input node a supplementary inductor. Although the original active inductor has very small quality factors (up to 10) due to the lack of a compensation scheme, good quality factors are obtained for the final inductor. However, since large size is expected for inductance values larger than 2.3 nH, a supplementary capacitor C is used in parallel to it.

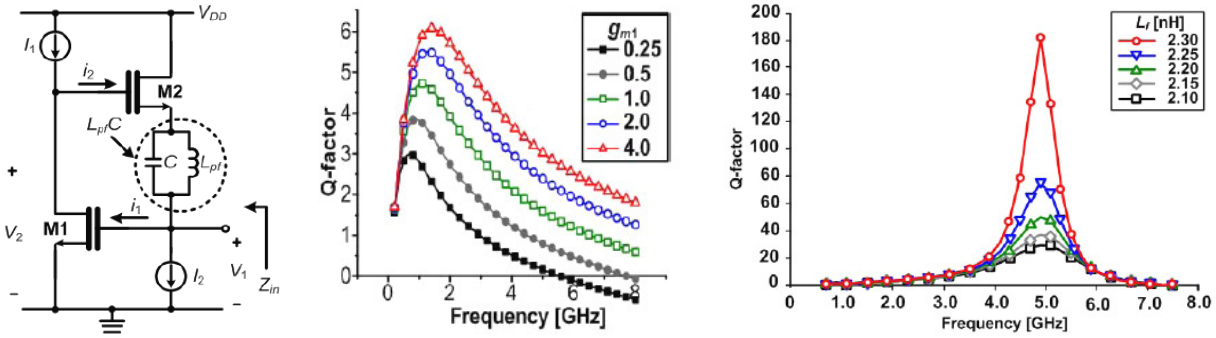


Fig. 3.34 Feedback spiral inductor and its final Q value [3.32]

Regarding the same TOSI discussed above, in order that this transistor based gyrator implementation behave as an ideal gyrator, its zero must cancel one pole (an impossible solution for this topology) or its zero must be zeroed ($g_{ds1}=0$). Since in practical implementations zero output conductances are not possible, the output conductance g_{ds1} may be decreased by implementing a cascode stage in the gyrator structure, the final structure [3.33] being presented in Fig. 3.35.

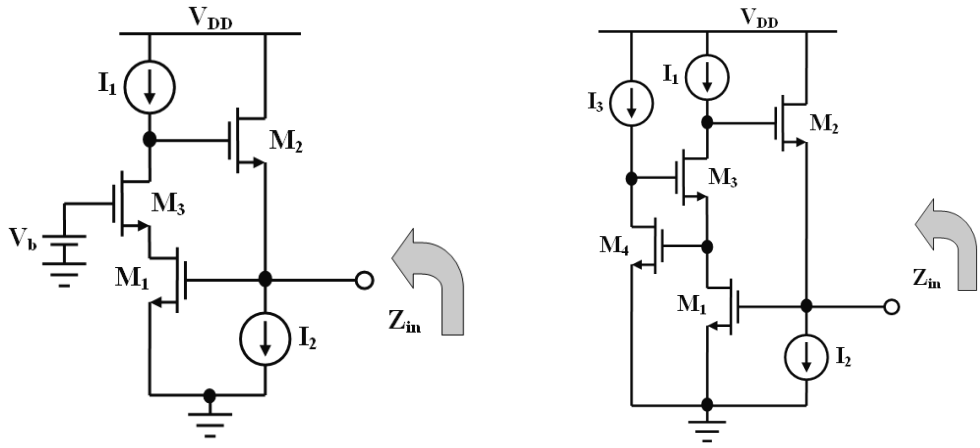


Fig. 3.35 Simple cascode (left) and regulated cascode TOSI (right) [3.33]

The inductor with simple cascode (Fig. 3.35) may be used to implement a bandpass amplifier [3.34] as shown in Fig. 3.36 together with its frequency performances. For this amplifier, the transistors M_1–M_3 together with $I_{1,2}$ are used to implement the active inductor. Since the circuit is designed at a single frequency, it is passively matched at the input while at the output a common drain is used to exploit its good linearity. The circuit is designed for a center frequency of 1 GHz but its frequency can be tuned down (900 MHz) with a power consumption of 50–57 mW when the circuit is biased from a 3V supply voltage. The quality factor can be tuned between 20 and 56. The power gain is 23 dB while the noise figure is 4.3 dB.

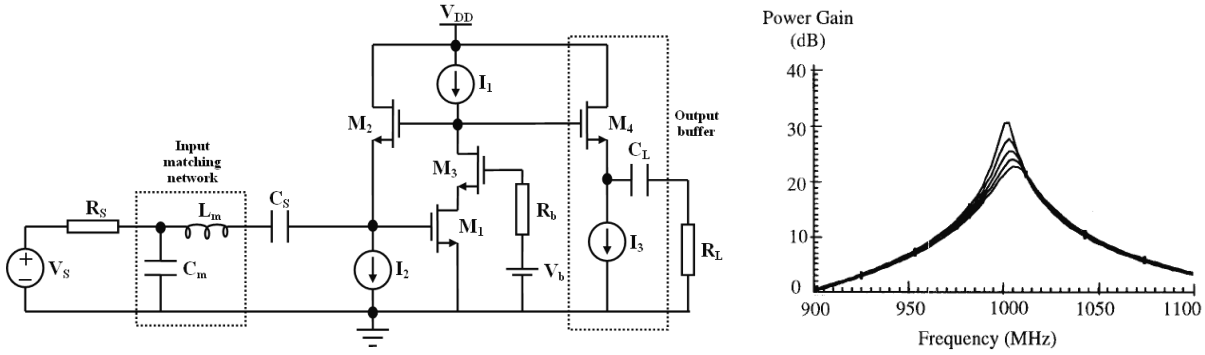


Fig. 3.36 Bandpass amplifier with TOSI [3.34]

The simple cascode TOSI was used to design a 'quadrature hibrid' (Fig. 3.37) that represents a four–port network which behaves as a directional coupler [4.36]. The coupler is designed at a centre frequency of 4.2 GHz, has a bandwidth of 9.5% (from its centre frequency) and a chip area of 0.72x0.64 mm^2 (active area = 0.4x0.2 mm^2) while the power consumption ranges between 17.5mW (3.6 GHz) and 24.6mW (4.7 GHz).

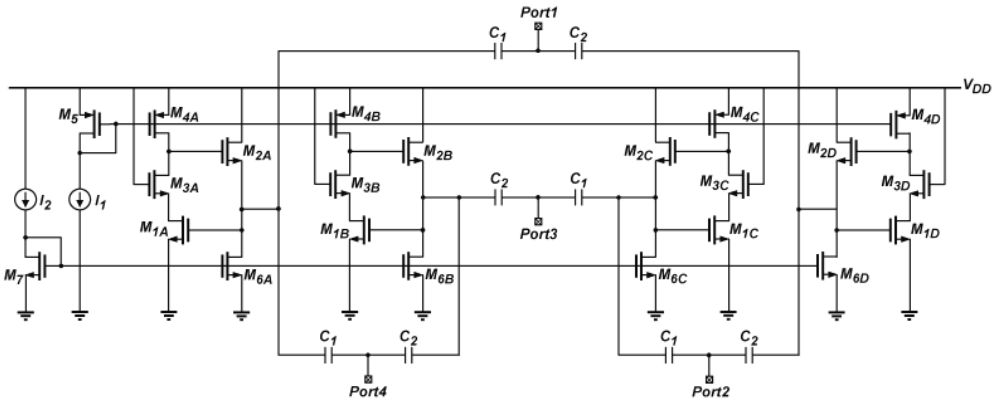


Fig. 3.37 Quadrature hybrid with CMOS TOSI [3.36]

The regulate cascode TOSI (from Fig. 3.35) was used for a LNA design [3.35] as presented in Fig. 3.38. The circuit is designed for a center frequency of 1 GHz, has a maximum power consumption of 3.3 mW and a noise factor of 3.65 dB although the circuit is designed as single–ended. The use of TOSI instead of passive inductors is advisable when large on–chip inductances are required.

A 5.7 GHz LNA architecture using the same regulate cascode TOSI has been proposed in [3.37] and presented in Fig. 3.39. The gain and noise figure are 17 dB and 3.4 dB while the power consumption is 19 mW.

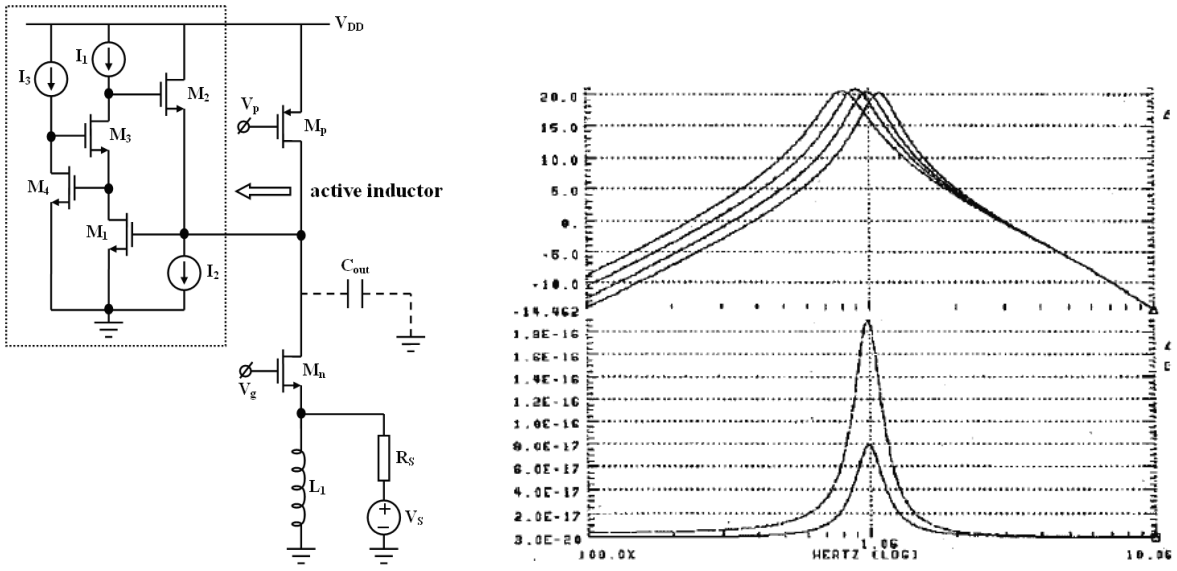


Fig. 3.38 TOSI based LNA and frequency performances [3.35]

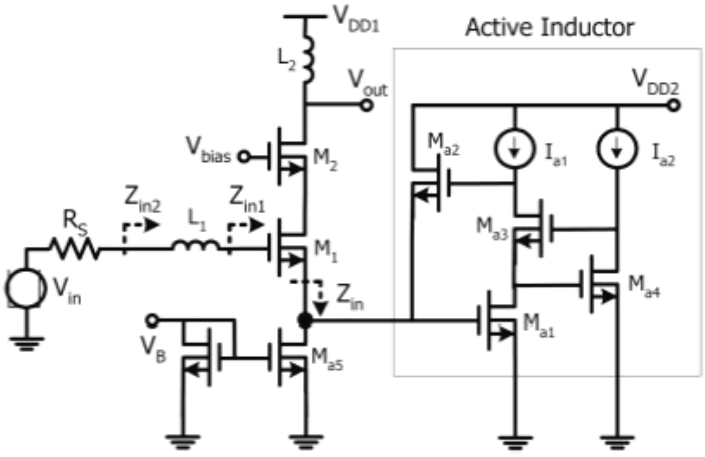


Fig. 3.39 A 5.7 GHz TOSI based LNA [3.37]

A modified topology (Fig. 3.40) for the simple cascode TOSI given in Fig. 3.35 has been proposed in [3.38]. By using the supplementary current I_3, an independent tuning of the frequency and quality factor becomes possible together with an increase of the inductance value. This topology is suitable for filtering applications.

A modified structure for the regulated cascode TOSI given in Fig. 3.35 has been proposed in [3.39] and is presented in Fig. 3.41. This idea is to alleviate the problems associated to near-threshold bias point for the input node by simply adding a diode–connected transistor (M_5) below M_1. The novel TOSI has been used in designing a 250 MHz Wilkinson 3 dB power divider making use of a 9 pF series capacitors and TOSI grounded inductors (~ 45 nH), with the general architecture presented in Fig. 3.41.

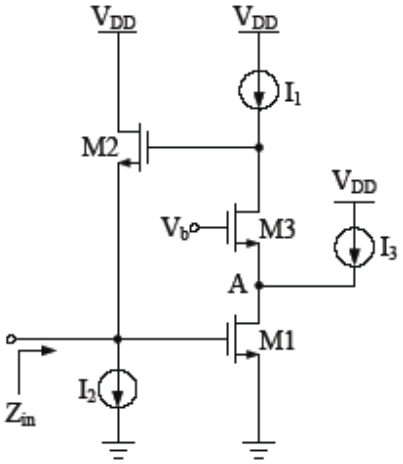


Fig. 3.40 CMOS TOSI with independent tuning [3.38]

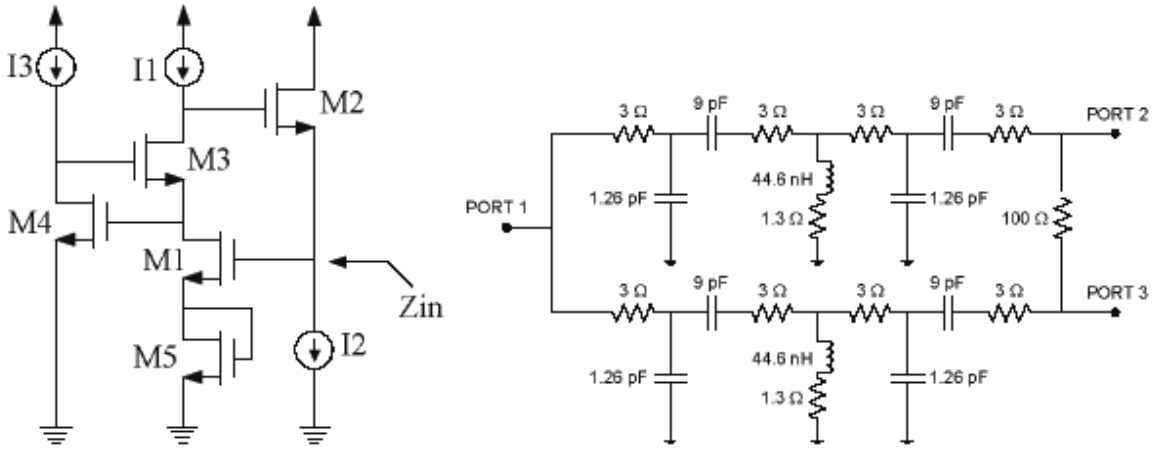


Fig. 3.41 Modified regulated cascode TOSI and its use in a Wilkinson divider [3.39]

A modified topology (Fig. 3.42) for the basic active inductor presented in Fig. 3.33 has been proposed in [3.40]. In this case, the transistors M_{n1} and M_{p2} implement the gyrator transconductances g_{m1} and $-g_{m2}$. The gyrator loading capacitor is C_{gs2} while C_{gs1} is the inductor parasitic capacitor. The minimum headroom voltage of $v_{gs}+2v_{ds,sat}$ make it suitable for low power supply applications. As mentioned above, cascode configurations are used to decrease the inductance loss resistance as also negative resistances do. In this case, to compensate the inductor losses at the frequency of interest, the cross–coupled transistors M_{p4a} and M_{p4b} are used as negative resistance. The main drawback consists in the strong frequency deviation created while changing the negative resistance value since it is dc coupled and thus the TOSI biasing is much influenced.

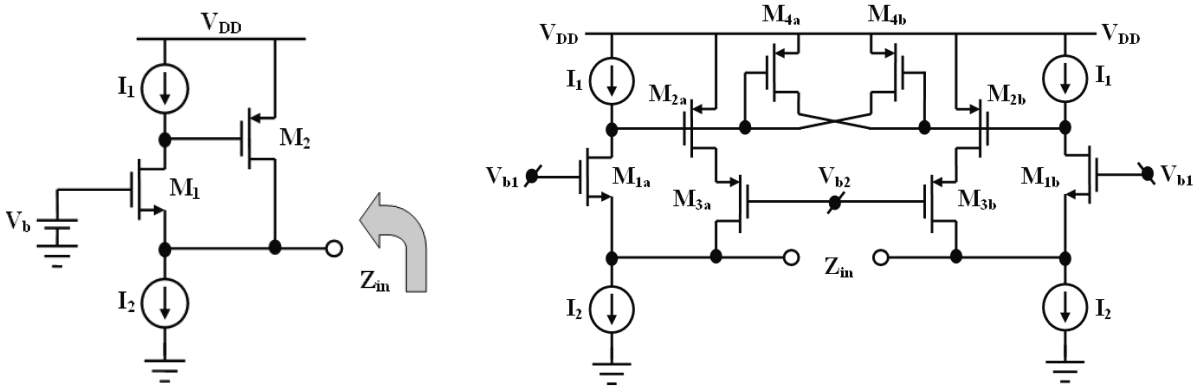


Fig. 3.42 CMOS grounded and floating TOSI [3.40]

The same floating TOSI structure has been used for an RF bandpass amplifier design [3.41] which is illustrated in Fig. 3.43.

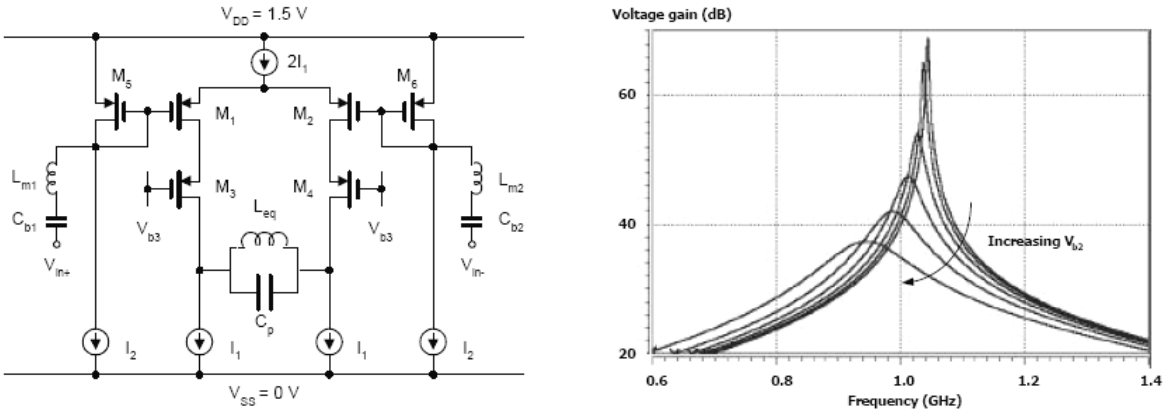


Fig. 3.43 TOSI based 1 GHz bandpass amplifier and reported results [3.41]

The bandpass amplifier consists of a matching stage (25 Ω) implemented with $M_{5,6}$, a cascode stage which implements a transconductor necessary for a voltage to current signal conversion and a LC load built with the shunt capacitor C_p and the simulated inductor (in Fig. 3.42). No negative resistance is used so that the centre frequency of the amplifier is the TOSI self resonant frequency. The circuit is designed at 1 GHz, consumes 30 mA from a 1.5 V voltage source, with THD < 1% (for a maximum voltage swing of 30 $mV_{p\text{-}p}$), about 4.2 dB noise figure and good input matching (S_{11}< - 40 dB). Output matching has not been considered since the amplifier output is connected to an integrated mixer.

A 3–transistor CMOS TOSI was proposed in [3.42] and presented in Fig. 3.44.

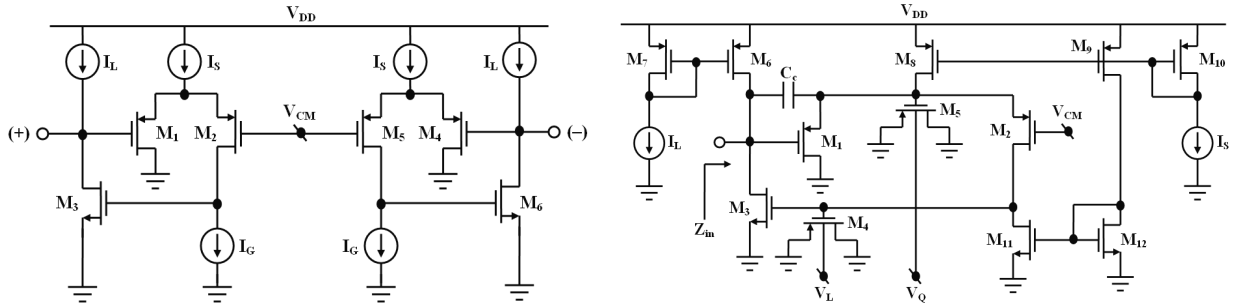


Fig. 3.44 3-transistor differential and single ended CMOS TOSI [3.42]

The gyrator is implemented (for the single version topology) by transistor M_3 ($-g_{m3}$) and the pair formed by M_1 and M_2 which implement the non–inverting transconductor g_m). Two current sources are required to implement the gyration function and consequently three voltage sources are necessary. As it can be noticed, no negative resistance is required since the inductor self resonant frequency and quality factor can be tuned independently by tuning the parasitic capacitor C_{gs2}, for example by using a parallel coupled MOS varactor which is controlled externally (M_5 in the complete scheme). Beside

a suitable change of biasing currents, the inductance value also can be changed by using a second MOS varactor connected in parallel with M_3 (M_4 in the complete scheme). This TOSI architecture has been designed for a frequency range 0.8–1.1 GHz, large inductance values being obtained from 300 to 630 nH with theoretical infinite quality factors. The circuit consumes only 4.16 mW from a 3-V power supply. The authors suggested its use in current controlled oscillators (CCO) configurations and proposed such a circuit in [3.43] for a differential topology (Fig. 3.45).

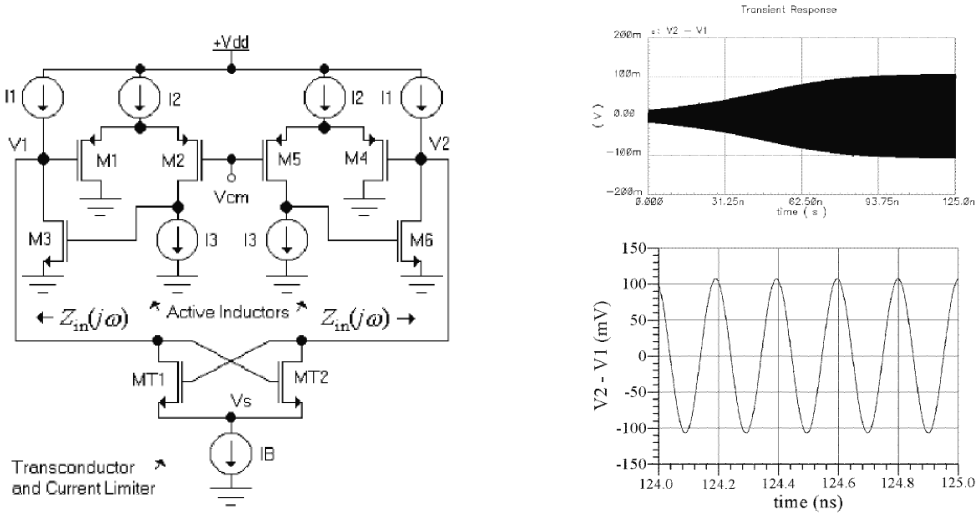


Fig. 3.45 Active inductor oscillator circuit and transient response [3.43]

The CCO contains the active inductor and a current limiter (MT_1, MT_2 and IB) known also as a negative resistor. As noticed from the transient response, the output reaches its steady state after 125 ns (for the complete circuit, not showed here) and the oscillation frequency is 4.93 GHz.

A new structure (Fig. 4.46) obtained by simply connecting a CS CMOS transistor ($-g_m$) with a CG one ($+g_m$) in a feedback configuration was proposed by Ismail in [3.44]. Two NMOS and PMOS topologies may be developed and since the use of a cascode stage is difficult for this architecture, only a negative resistance is used to compensate the inductor losses. For the single ended case, a modified dc coupled negative resistance has been proposed, the main drawback consisting in the use of decoupling capacitors, C_{b1} and C_{b2}. However, comparing with other proposed CMOS architectures, this TOSI is simple and has a minimum number of transistors (only two) and current sources (one). Although the biasing for this TOSI architecture is a little bit difficult, this architecture was chosen also for the research in this thesis.

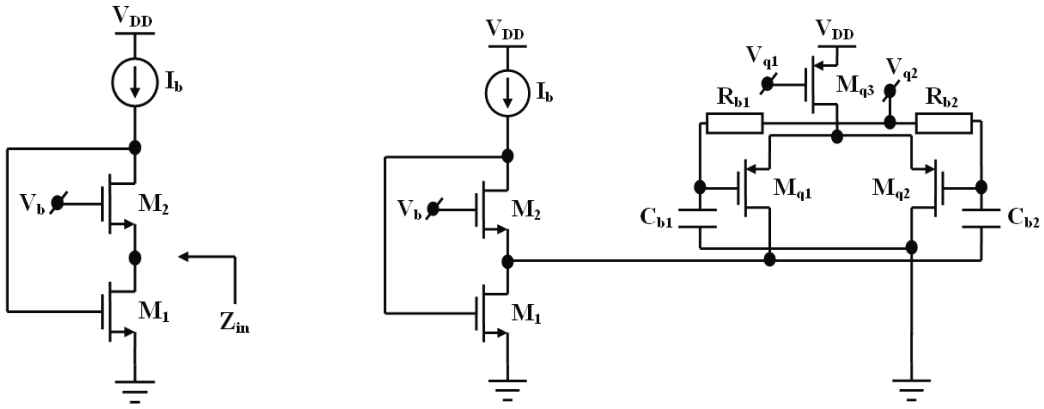


Fig. 3.46 Simulated inductor with negative resistance compensation [3.44]

The above architecture can be used in filtering applications (discussed later) but also in RF oscillators, the same author proposing a current controlled oscillator (CCO) in [3.45], built with this simulated inductor and is presented in Fig. 4.47. As can be noticed, the architecture of the CCO consists of the simulated inductor (previously presented but in a PMOS configuration) and the cross coupled negative resistance (Mn1 and Mn2). The start–up condition of the oscillator is satisfied by the negative resistance which must overcome the damping resistance of the active inductor and generates positive poles in s-plane. With the increase of the oscillation amplitude, the large–signal response of the negative resistance will bring the poles to the imaginary axis. A constant amplitude oscillation is built only when the negative resistance (NIC) cancels the damping resistance. No varactor is required since the oscillation frequency is set by a corresponding change of the current I_C. This is an example of application in which the TOSI self resonant frequency is exploited rather than its inductive behavior.

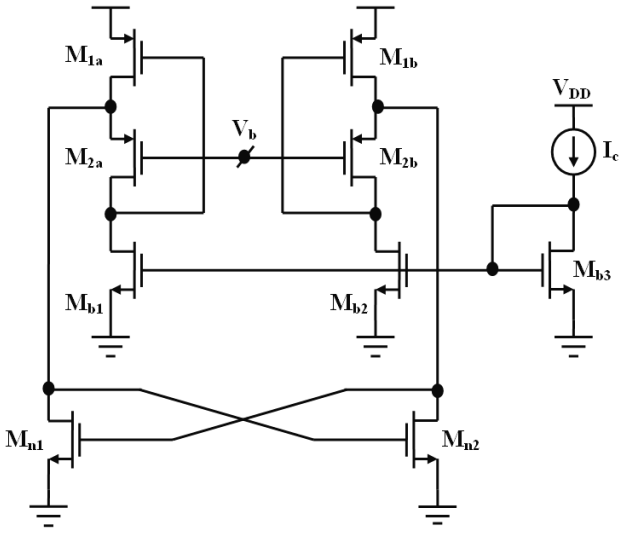


Fig. 3.47 Current controlled oscillator with CMOS TOSI [3.45]

An improved architecture of this CMOS TOSI architecture was proposed in [3.46] where a review of 2–transistor CMOS TOSI architectures reported in the literature until 2002 is presented too. However, it regards the PMOS implementations (Fig. 3.48).

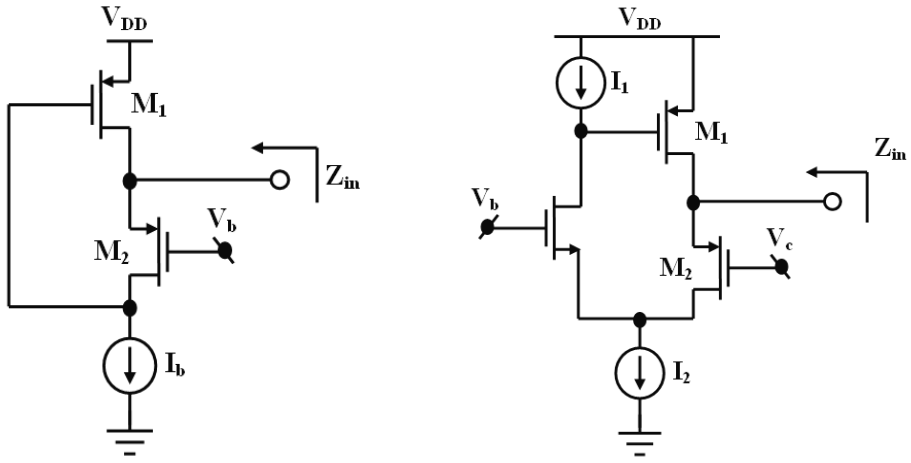


Fig. 3.48 High-Q compact CMOS TOSI (basic and improved structures) [3.46]

The enhancement consists in the use of a supplementary transistor M_3 to increase the loop gain within the shunt–shunt negative feedback of the circuit, thereby reducing the series resistance of the inductor. This inductor aims the filtering applications, its performances being studied at frequencies around 1 GHz. The same inductor has been reported also in [3.47].

Based on the simple cascode TOSI architecture presented in Fig. 3.36, an improved TOSI (Fig. 3.49) has been used for a LNA design [3.48].

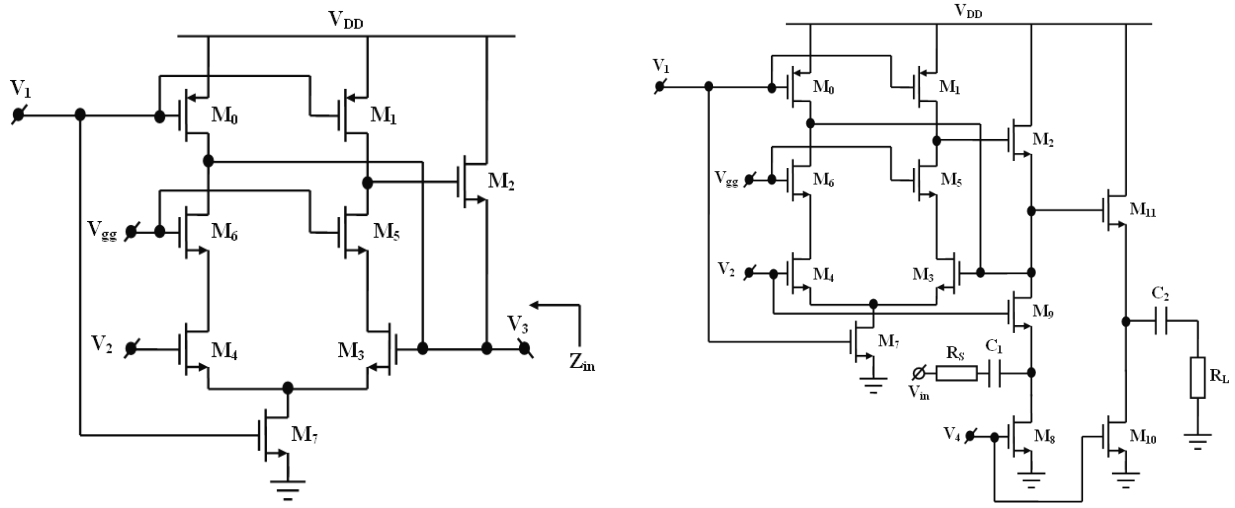


Fig. 3.49 High-Q TOSI and its LNA implementation [3.48]

This enhanced TOSI structure was obtained by simply replacing the cascode common source amplifier with a cascode pair transconductor as presented in Fig. 3.49

(left). In this circuit, $M_{0,1,7}$ represent current sources, $M_{2,3,5}$ implement the active inductor while $M_{4,6}$, in a positive feedback, are used to compensate the series loss. For the previous structure, there is an ac path to the ground formed by the parasitic capacitors of M_1 and M_2. By introducing this positive feedback, the currents circulating through these parasitic capacitors are summed in the drain node of M_7 which is a virtual ground and thus, the total current will flow out the drain of M_6 which is added to the input node. Thus, the undesirable coupling paths are compensated. A CG stage ($M_{8,9}$) is chosen as the input stage offering good matching and linearity performances while the amplifier load is the TOSI mentioned above, implemented by $M_{2\text{-}6}$. The CD stage ($M_{10,11}$) represents the output buffer used mainly for matching. Designed at a frequency of 1.75 GHz, this LNA has a gain of 24 dB for a power of 9.3 mW and a chip area of only 0.03 mm^2.

Another improvement of the cascode TOSI proposed in [3.33] was reported in [3.49] and is shown in Fig. 3.50. The main enhancement of the previous inductor consists in a supplementary passive resistor added to the feedback path. The feedback resistance R_f forms an additional inductive reactance of the impedance looking into the source of M_1 which significantly increases the inductance of cascode–grounded active inductor, therefore improving the quality factor.

The same architecture has been proposed in [3.50] with the main differences that I_1 is implemented by a PMOS transistor, I_2 by a NMOS one and R_f is tunable (Fig. 3.51). This TOSI architecture was used to implement a Colpitts VCO (Fig. 3.51).

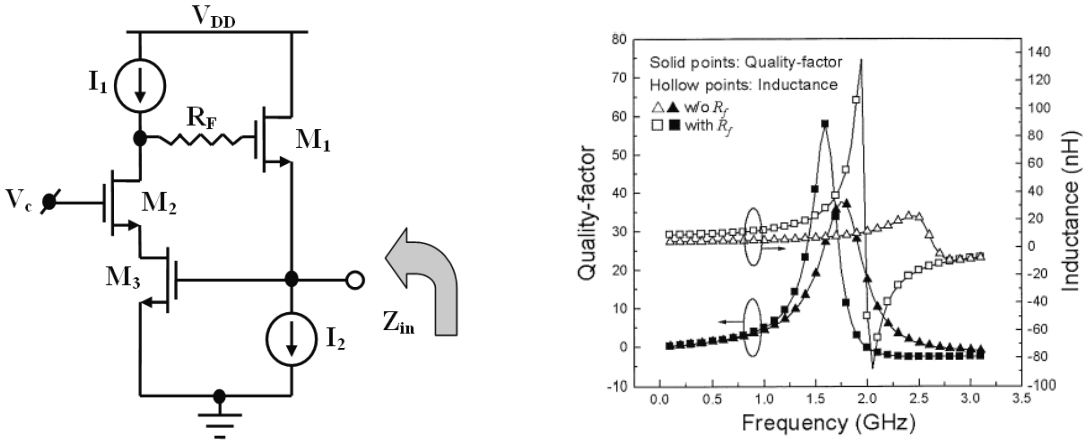


Fig. 3.50 Improved CMOS TOSI and its reported performances [3.49]

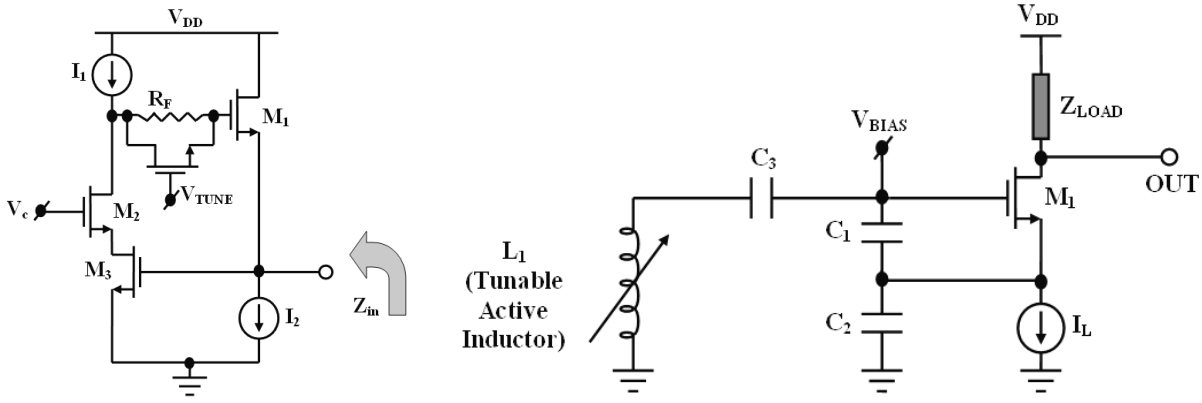


Fig. 3.51 Tunable CMOS TOSI and its application in VCO applications [3.50]

A wide frequency range (0.5–2 GHz) is covered by this VCO in CMOS technology while consuming only 13.8 mW from a 1.8V power supply and occupying an area of 300x300μm^2. The phase noise varies from –78 to –90 dBc/Hz at 1 MHz offset from the carrier throughout the tuning range.

A throughout study of the application of the same TOSI architecture to RF reconfigurable front–ends is presented in [3.51] and [3.52]. The inductor proposed in [3.50] was used to design a multi–band LNA [3.53] thanks to a frequency selector that, depending on what frequency is desired, selects a corresponding feedback resistance from a resistor network. By using common gate (CG) and common drain (CD) as input/output stages, a differential LNA was designed, showing the multi–band capability as shown in Fig. 3.52.

A wideband bandpass amplifier implemented with the same high–Q simulated inductor has been implemented in [3.54] and presented in Fig. 3.53.

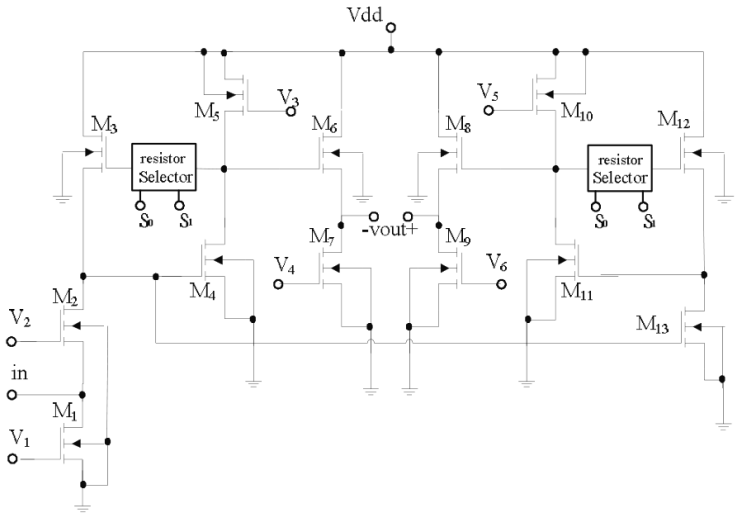


Fig. 3.52 High–Q TOSI with band selector and LNA implementation [3.53]

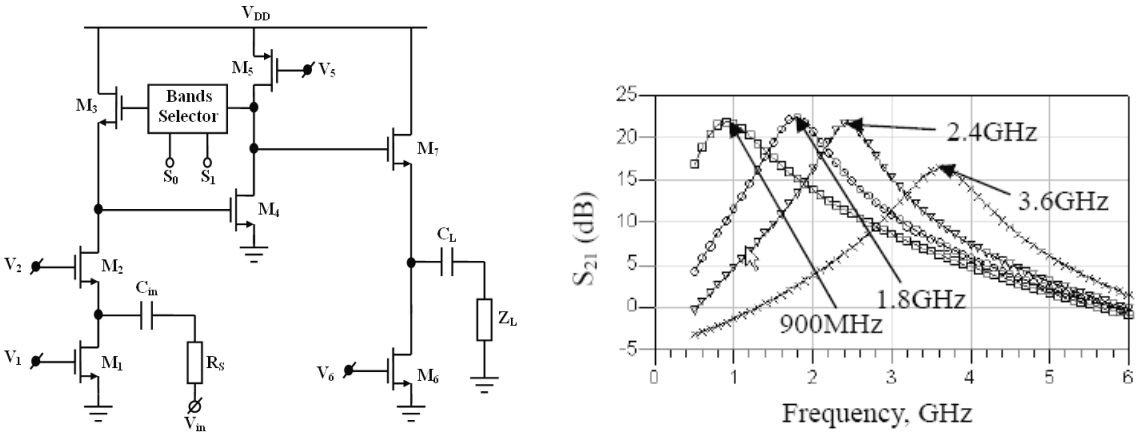
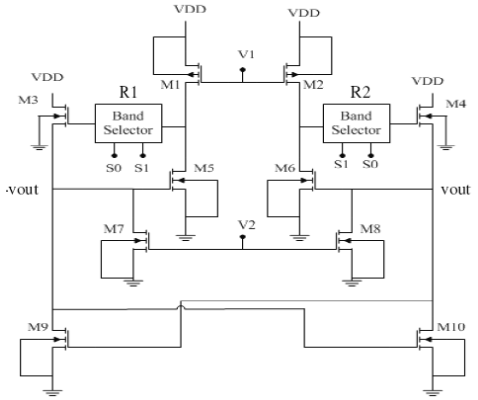


Fig. 3.53 High–Q TOSI based bandpass amplifier and its frequency behavior [3.54]

A multi–band VCO [3.55] was implemented with the previous reported high–Q active inductor, thanks to the resistor network, as shown in Fig. 3.54 together with its frequency response. Particular to this configuration is the presence of two cross–coupled transistors ($M_{9\text{-}10}$) which simulate the negative impedance converter necessary to bring and keep the oscillator in steady state.



Technology	0.18µm CMOS			
VCO_bias	Analog 1.8V			
Frequency	900MHz	1.8GHz	1.9GHz	2.4GHz
Tuning Frequency	0.3~2.9 GHz	1.0~3.5 GHz	1.1~3.6 GHz	1.6~3.9 GHz
Tuning range	181.3%	111.1%	106.4%	83.6%
Phase Noise @1MHz	-86.916 dbC/Hz	-84.486 dbC/Hz	-83.774 dbC/Hz	-81.168 dbC/Hz
Power	9.43 mW			
Chip area	0.3 x 0.3 mm^2			
Core area	0.1 x 0.3 mm^2			

Fig. 3.54 Multi–band VCO and reported performances [3.55]

Another VCO architecture implemented with the simulated inductor shown in Fig. 3.34 but using a feedback resistor instead of a resistor network has been proposed in [3.56] and is shown in Fig. 3.55. The frequency range covered by this VCO is 1.3 to 4 GHz with an average in–band phase noise of –86 dBc/Hz.

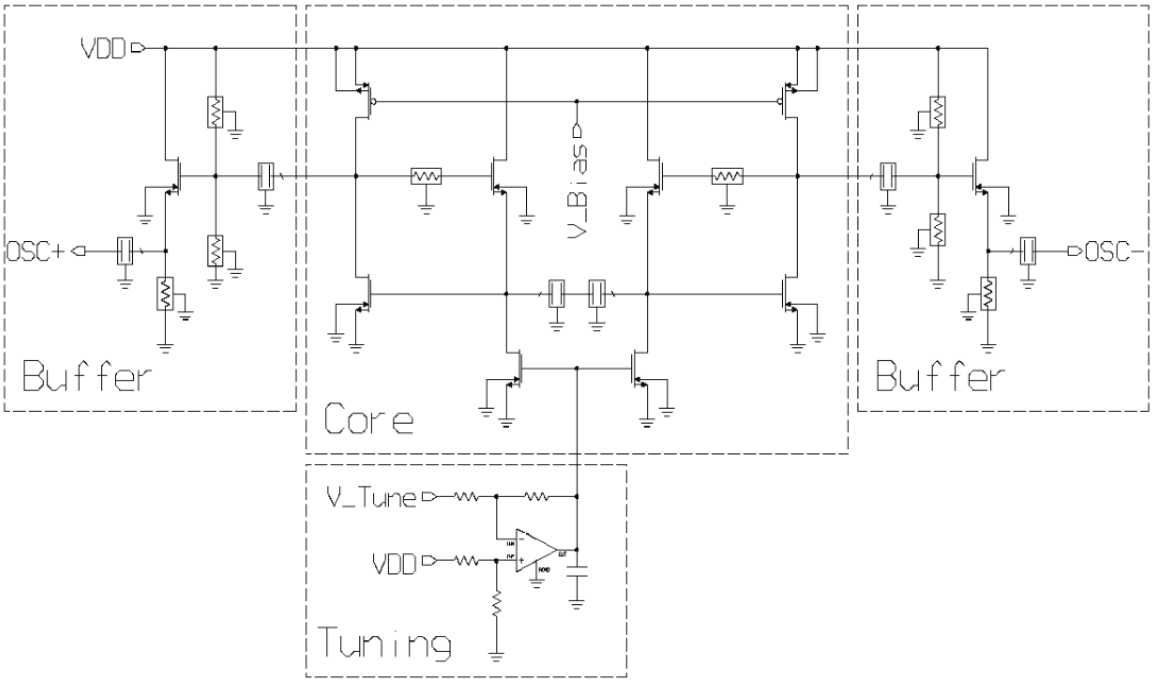


Fig. 3.55 VCO implementation with resistive feedback based TOSI [3.56]

An improved version of the architecture presented in Fig. 3.34 has been reported in [3.57] and presented in Fig. 3.56 together with its frequency performances.

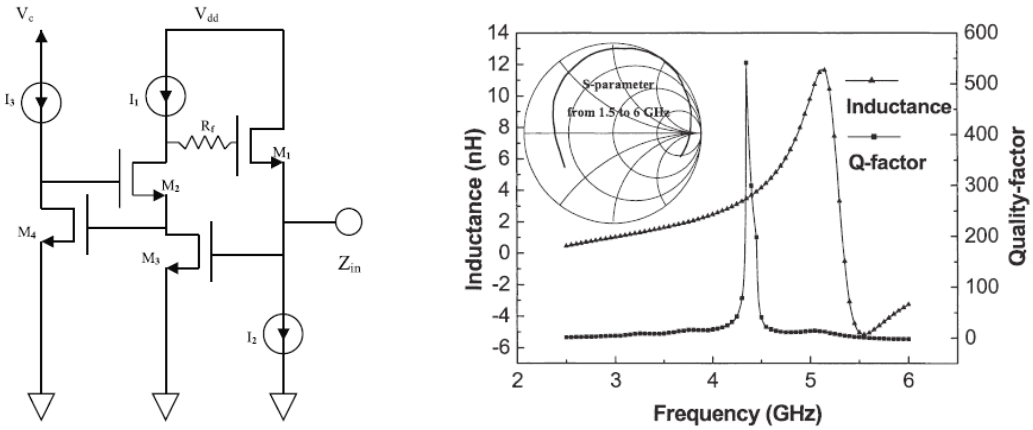


Fig. 3.56 Improved TOSI and its frequency performances [3.57]

As it can be noticed, the proposed topology is a combination of the original regulated cascode TOSI (Fig. 3.35) with the topology in Fig. 3.50 that makes use of feedback resistor. This TOSI configuration has the followings advantages:

- low current consumption due to the presence of the additional stage M_4 with no negative effect on the circuit linearity since M_4 is not on the signal path ;
- I_2 has a high output resistance since it is implemented as a double–cascode current mirror;

- the inductor quality factor is changed independently of the center frequency due to the presence of M_4 that is biased separately.

Another improvement that can be applied to the TOSI architecture reported above [3.33] consists in replacing the simple cascode stage with an RC feedback cascode network [3.58] in order to compensate the internal inductance loss (Fig. 3.57).

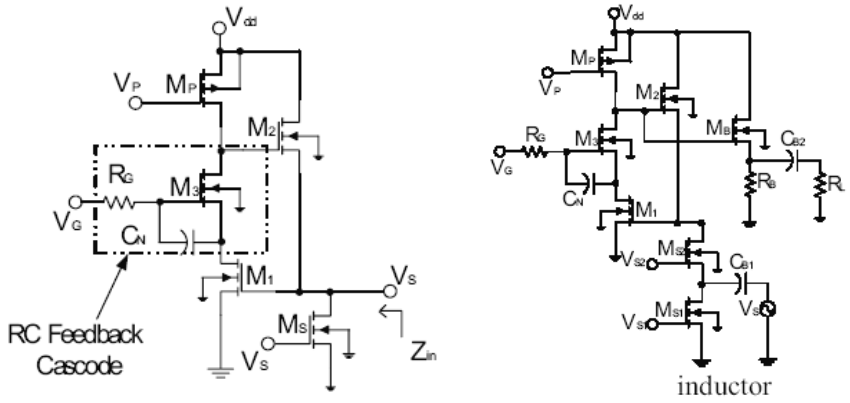


Fig. 3.57 Improved CMOS TOSI architecture and its use in a bandpass amplifier [3.58]

The idea is that by adding R_G and C_N, a negative impedance is created that compensates the output conductances of transistors M_P and M_S. Since M_3 is used to decrease the output conductance of M_1, a TOSI architecture with improved quality factor is obtained. A bandpass amplifier, biased from a 2.5 V power supply, built with this simulated inductor was presented in Fig. 3.57 (right). The CG input stage provides a simple 50Ω input matching with higher linearity without any source inductor. The amplifier has a constant gain of 20 dB up to 1 GHz while the noise figure is about 8 dB.

Another improved architecture of the circuit presented in Fig. 3.30 and proposed in [3.59] makes use of a resistive bias (Fig. 3.58) which, although requires higher silicon area and less controlability, is more stable and less sensitive to fabrication errors.

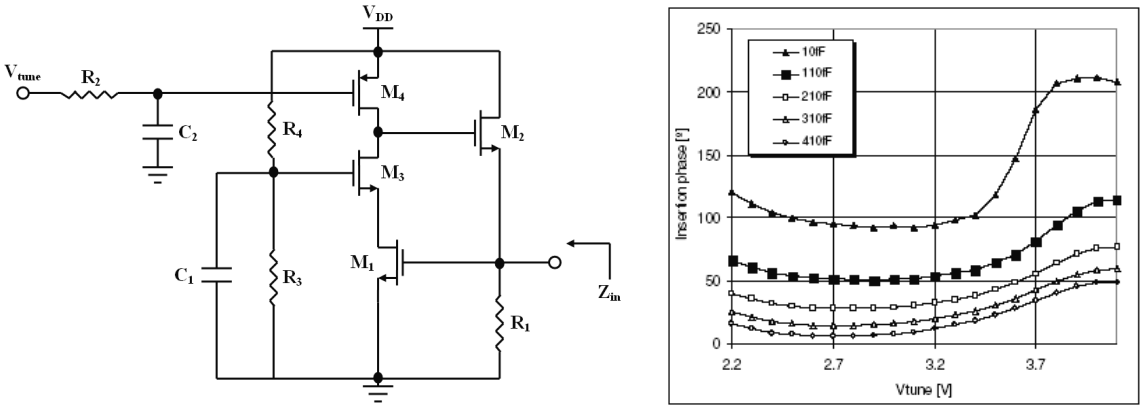


Fig. 3.58 CMOS active inductor with resistive bias and its use at a T-LC phase shifter

This active inductor is designed at the frequency of 2 GHz where higher inductance values then 20nH and higher quality factor values. This aims the practical implementations of phase shifters (T-LC shifter).

An interesting application for simulated inductors is proposed in [3.60] where RF buffers are envisaged. The use of buffers at the VCO output is mandatory in order to avoid the loading effect in which case the loading capacitor (seen at the input of the following block) decreases the VCO resonant frequency. Moreover, there is the leakage problem too. These problems impose the use of RF buffers and a possible configuration making use of TOSI architectures was proposed in the above paper and presented in Fig. 3.59.

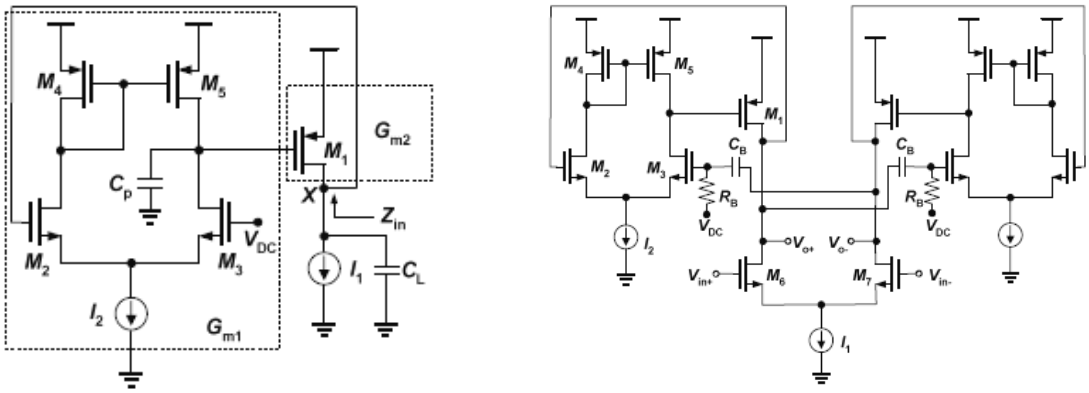


Fig. 3.59 CMOS TOSI and its use for RF buffers [3.60]

For this structure, the inductive behavior is emulated by a gyrator consisting of the CS transconductor (M_1 – inverting stage) and the differential-to-single-ended transconductor ($M_{2\text{-}5}$ – non–inverting stage) and the parasitic capacitor denoted as C_p. This parasitic capacitor is the sum of all parasitic capacitors seen in the drain of M_5. Both transconductances have large output impedances, the differential stage being superior to the simple CG stage. An important aspect is that very high–Q active inductors are not required since the buffer operates in large signals and this may be a cause of instability. Thus, compensation schemes are not required. The RF buffer built with this active inductor is shown in Fig. 3.59 (right).

Another topology (similar to the previous one) with single and differential transconductors interconnected together was proposed in [3.61] and shown in Fig. 3.60. Proposed for low frequency operation (~140 MHz), the active inductor is simulated by the single CS stage implemented by M_2 (inverting transconductance) and the differential–to–single–ended stage (non–inverting transconductance), implemented by M_{1A} and M_{1B}.

Small power consumption is required to implement this active inductor (544 μW, V_{DC}=2.5V) but the power will be largely increased if the circuit intends higher frequencies design, with matching stages and good linearity requirements. This TOSI architecture can be used in filtering applications.

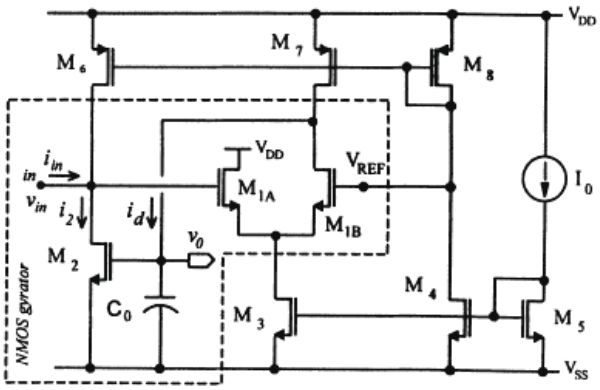


Fig. 3.60 NMOS TOSI [3.61]

A VCO architecture designed with the same TOSI configuration has been proposed in [3.62] and is presented in Fig. 3.61. The gyrator capacitor is the total gate capacitance of M_{n3} while the inductor parasitic capacitor is the total gate capacitor of M_{n2}, or equivalently, seen at the input node. A negative resistance is used to compensate the active inductor (L_{act}) losses where the transistor M_{p1} replaces M_{pb3} for the left half circuit. By tuning the control voltage V_{ctrl} between 0.7 and 1.6V, the oscillation frequency is tuned from 0.4 to 1.45 GHz. In other words, this VCO has a centre frequency of 915 MHz and exhibits a tuning range of 84% for a power consumption of less than 10.5mW under 3.3V supply voltage. Its phase noise is around – 90 dBc/Hz at 0.5 MHz offset from the carrier.

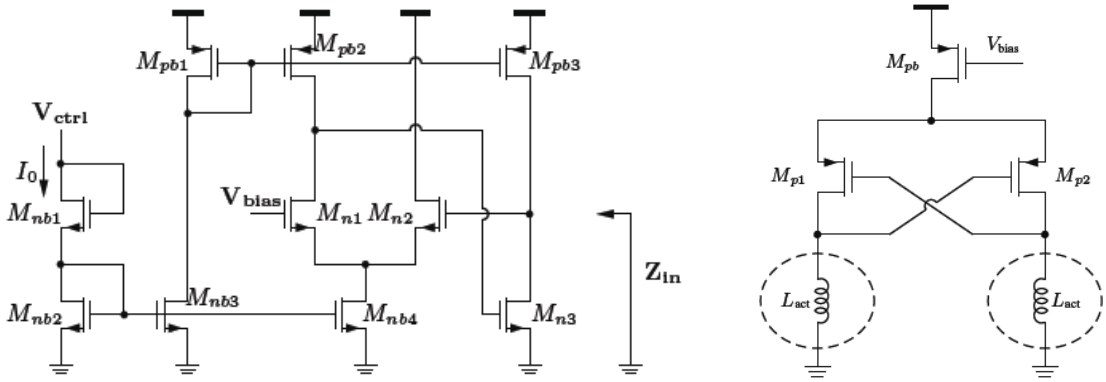


Fig. 3.61 TOSI based VCO architecture [3.62]

Another gyrator based simulated inductor has been studied in [3.63]. This architecture makes use of two transistors only to implement the gyration function and two current sources (Fig. 3.62).

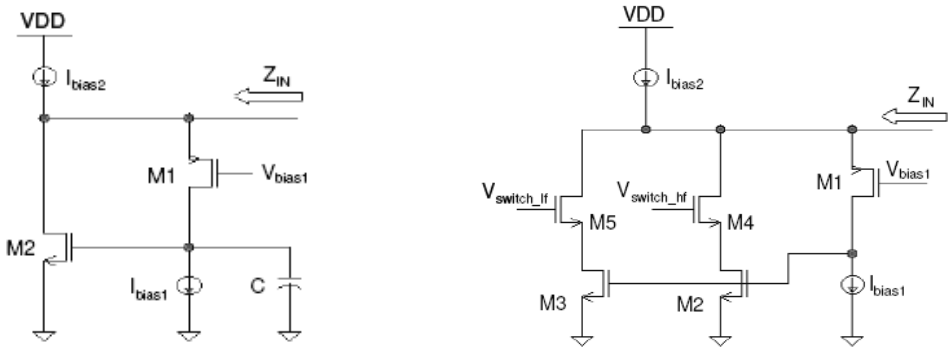


Fig. 3.62 CMOS single and switched TOSIs [3.63]

C_{gs2} is the gyrator loading capacitor, an optional external capacitor C being connected to the loading capacitor node that can be used for the inductance value tuning. This architecture, intended for filter design, facilitates the use of switching transistors that furthermore improves the inductor frequency capability. As it can be noticed, instead of using transistor M_2, two switched transistors are used (M_2, M_3). By properly sizing these transistors, three regions of operation can be established: a low–frequency one in which a single small transistor is enabled, a mid–frequency where the second one is enabled and high–frequency operation when both transistors are enabled. Although a larger capacitance is obtained when the both transistors are enabled, a larger equivalent transconductance is obtained and therefore a much higher frequency is obtained.

An original implementation of the gyrator principle with a transistor only was proposed in [3.64] [3.65]. According to this method, one transistor is sufficient to simulate the gyrator function (Fig. 3.63).

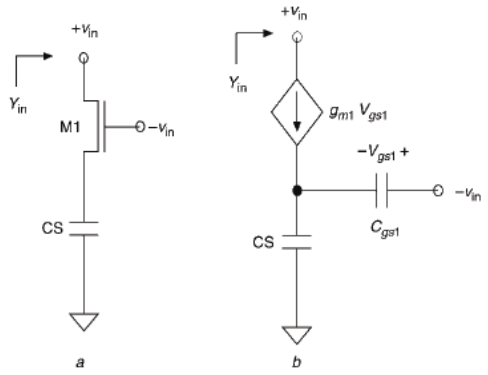


Fig. 3.63 Capacitive source degenerated transistor and equivalent model [3.64]

According to the equivalent small signal model, this novel gyrator is described by the following relations where the approximation $g_m >> \omega C_{gs}$ was considered:

$$\begin{cases} v_{(1)} = v_{in} \\ s(C_S + C_{gs})v_{(2)} - sC_{gs}v_{(3)} = g_m(v_{(3)} - v_{(2)}) \\ v_{(3)} = -v_{in} \end{cases} \tag{3.16}$$

$$v_{(2)} = -v_{in}\frac{g_m + sC_{gs}}{sC_S + sC_{gs} + g_m} \tag{3.17}$$

$$Z_{in} = \frac{v_{(1)}}{g_m(v_{(3)} - v_{(2)})} = \frac{v_{in}}{g_m(-v_{in} + v_{in}\dfrac{g_m + sC_{gs}}{g_m + sC_{gs} + sC_S})} \approx \frac{1}{-g_m + \dfrac{g_m^2}{g_m + s(C_S + C_{gs})}} \tag{3.18}$$

The last relation may be rearranged so that (3.19) is obtained:

$$Z_{in} = \frac{1}{-g_m + \dfrac{g_m^2}{g_m + s(C_S + C_{gs})}} = \frac{1}{-g_m + \dfrac{1}{\dfrac{1}{g_m} + s\dfrac{C_S + C_{gs}}{g_m^2}}} \tag{3.19}$$

The equivalent circuit of this 1–transistor gyrator is a real inductor (L_S in series with its parasitic resistantce r_S) in parallel to a negative resistance. This negative resistance is a source of potential instability for the single ended configuration and furthermore supplementary transistors should be added, a symmetrical (differential) CMOS SDD-AI being obtained (Fig. 3.64).

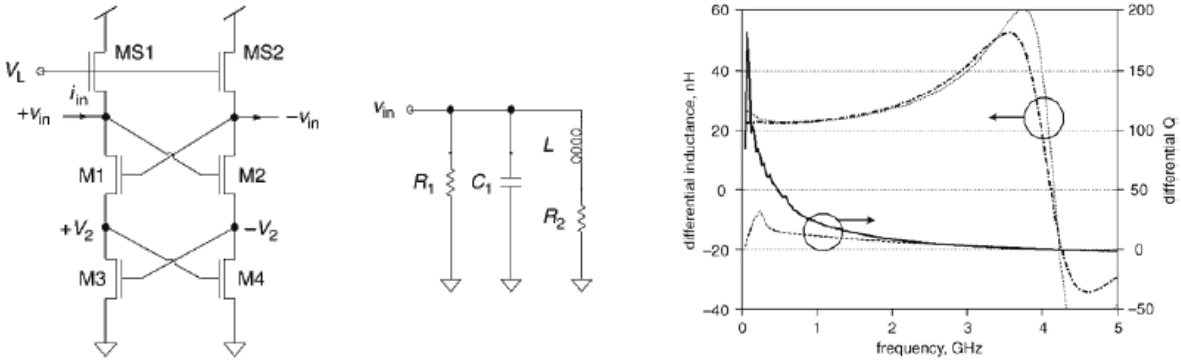


Fig. 3.64 CMOS SDD-AI and its measured parameters [3.64][3.65]

3.4 TOSI Based Preselective Filter Solutions

From the previous sections it became clear that any TOSI architecture has an inductive behavior up to its self resonance frequency and a capacitive one for higher frequencies. At the self resonant frequency the equivalent impedance is determined entirely by its resistive losses. If the inductive behavior is envisaged for a certain bandwidth then the inductor must be designed with a self resonance frequency much larger than the operation frequency. However, also the self resonance frequency may be envisaged in particular applications, as RF filtering, since good selectivity may be achieved at this frequency. The implementations which envisage the RF filtering function, by exploiting the self resonance frequency, are presented in this section.

The use of simulated inductors around the cut off transistors frequency may be unusual when designing analog circuits. However, since no gain is required for the simulated inductor, as required for amplifiers, one transistor from the gyrator structure may be used very well at frequencies higher than its cut off frequency.

3.4.1 2nd Order TOSI Based Filters

Most TOSI structures proposed in the literature are used in filtering operations. Due to their good selectivity at the resonant frequency, mainly when using compensation schemes (negative resistances), these architectures suits best the RF filtering design. All structures reviewed in the previous section as bandpass amplifiers can be used very well as RF filters since they have the intrinsic filtering property. However, only the TOSI structures implemented as independent filters are reviewed in this section.

The first CMOS TOSI architecture proposed for filtering applications is the basic architecture reported in [3.31] used to implement a VHF bandpass filter (Fig. 3.65). Although the cell didn't use any compensation scheme, this TOSI section (Fig. 3.33) can be used in filtering applications thanks to its intrinsic RLC equivalent model. The filter has been designed for the frequency band 400–500 MHz and exhibited very small current consumption.

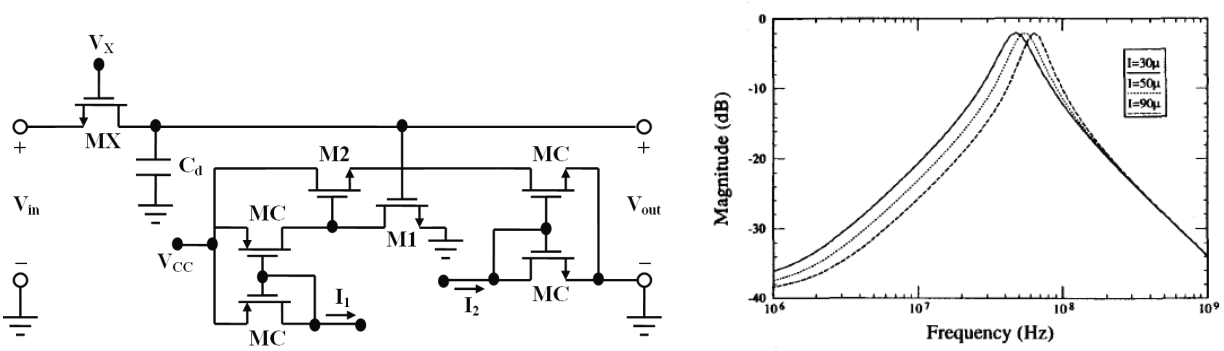


Fig. 3.65 TOSI based VHF bandpass filter [3.31]

For the inductor presented in Fig. 3.40, an RF bandpass filter (Fig. 3.66) was reported in the same reference [3.38]. So far it is obvious that having a particular structure of transistor only simulated inductor (TOSI) and adding two buffers, one at the input and the second to the output port are sufficient to obtain an RF bandpass filter. Buffers are needed in order that the synthesized filter works with voltages at the input and currents at the inductor level and for filter matching (50Ω at input/output).

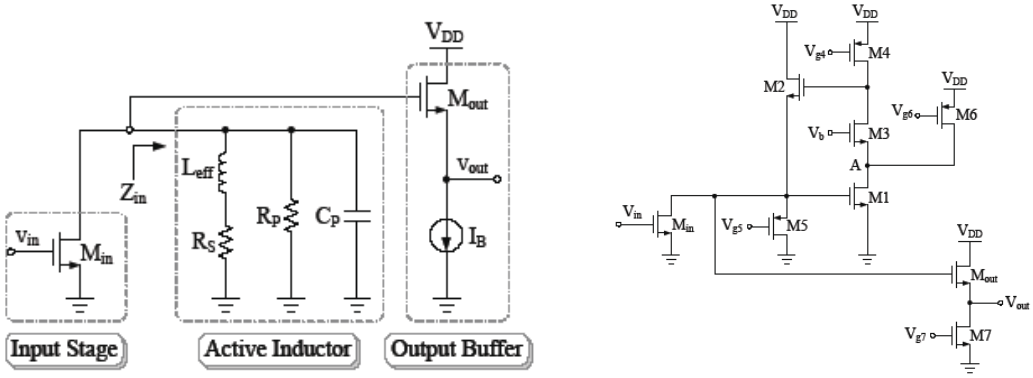


Fig. 3.66 2.4 GHz TOSI based bandpass filter [3.38]

The frequency filter performances are illustrated in Fig. 3.67, with maximum power consumption of 4mW, minimum Q of 109 and works in a frequency range of 2–2.9 GHz:

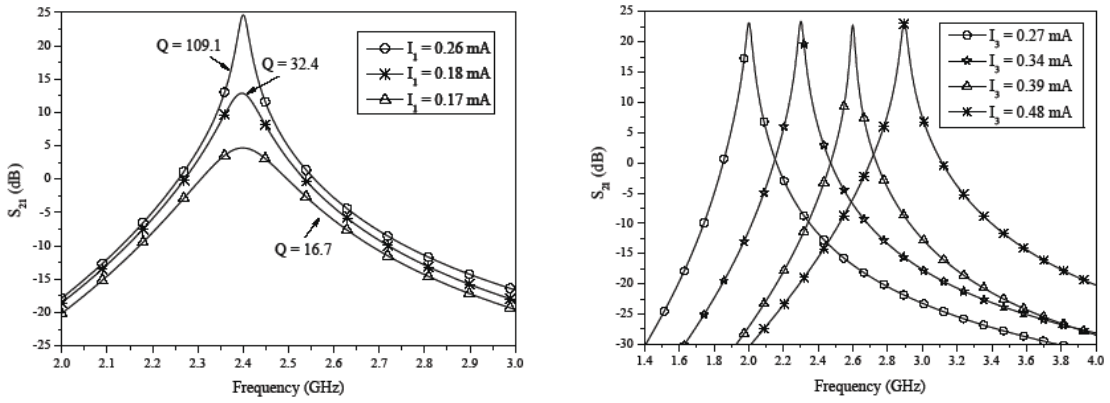


Fig. 3.67 TOSI BPF quality factor and frequency tuning performances [3.38]

The second TOSI architecture proposed by Ismail in [3.44] was used also to implement a BPF (Fig. 3.68). Proposed in a differential architecture, this filter is designed at a centre frequency of 918 MHz with Q=75 where the current consumption is approximately 400µA (Fig. 3.69). Obviously, the current consumption increases with the operating frequency. A cascode stage is used as the input buffer in order to minimize its parasitic effect on the simulated inductor behavior. Common drain stages are used in general as output buffers and particularly for this BPF structure.

A differential BPF using the TOSI configuration proposed in [3.63] was designed in a 0.18µm CMOS process. It makes use of switches in order to facilitate a 3–band operation.

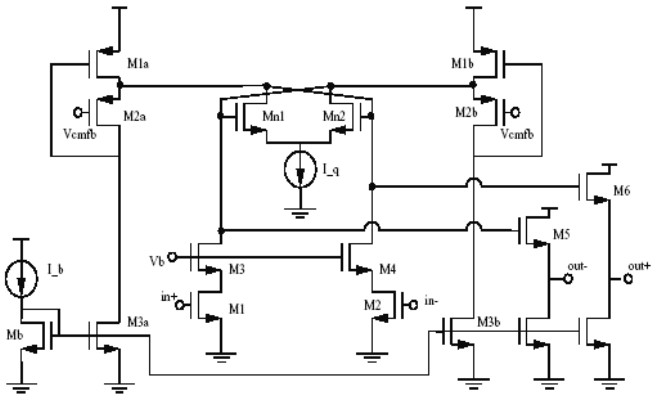


Fig. 3.68 Fully differential BPF with TOSI [3.44]

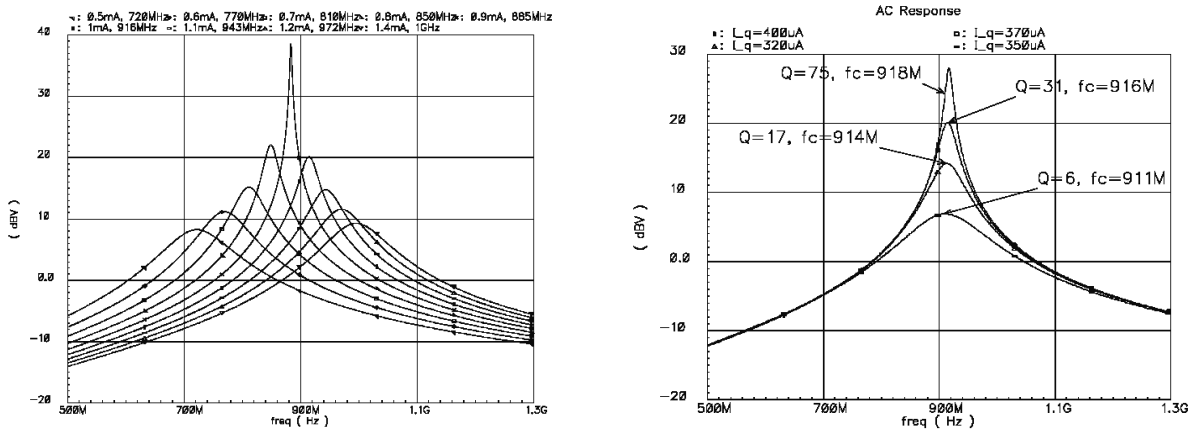


Fig. 3.69 Frequency and quality factor tuning performances for TOSI based BPF [3.44]

Being differential (Fig. 3.70), it rejects the common–mode noise and has a large dynamic range for the input signals but with the cost of doubled power consumption. A fully differential source degenerated stage is used as the input buffer ($M_{6a,b}$ and M_{11}), the

current being reused by the simulated inductor. A common drain stage is used as the output buffer, this transistor biasing having better linearity than other configurations. Cross–coupled transistors ($M_{7a,b}$ and M_{12}) are used to implement the negative impedance converter, required to compensate the inductor losses. Depending on the selected centre frequency, the power consumption is between 12mW and 26mW where an important power ratio is due to the matching buffers. If this filter is directly integrated into a receiver, the matching buffers are not needed. The filter quality factor is about 40 but it can be tuned from 2 to 300 as well. IIP3 has values between -12.4dBm and -21dBm, depending on the operation frequency.

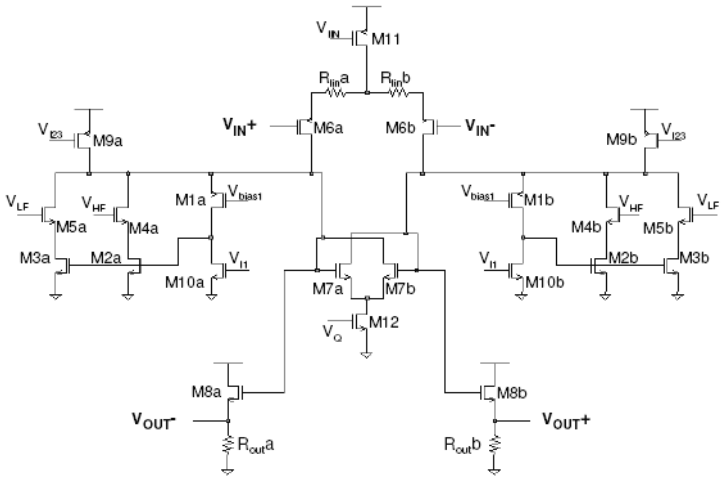


Fig. 3.70 Fully differential TOSI based BPF [3.63]

A modified topology for the architecture reported in [3.31] and similar to that reported in [3.42] but designed with NMOS transistors was reported in [3.66] and presented in Fig. 3.71 together with its frequency behavior.

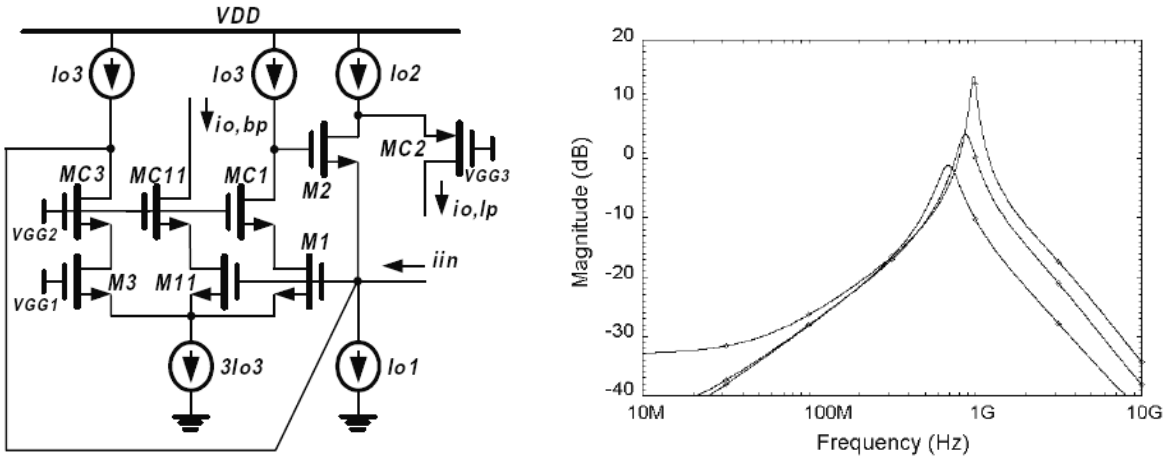


Fig. 3.71 TOSI based VHF current mode filter and frequency response [3.66]

The particularity of this structure is that it can be used as a bandpass (M_{C11} output) or a lowpass (M_{C2} output) filter as well. The basic structure consists of the transistors M_1–M_3, the others being added to implement cascode stages, Q tuning or the supplementary lowpass filtering operation. Designed in a 0.35μm CMOS process, the circuit operates in the band 685–973 MHz with low current consumption.

A differential RF bandpass filter designed with 3–transistor NMOS TOSI, similar to the previously reported one in [3.31], at a frequency of 5.42 GHz was reported in [3.67].

The basic TOSI structure is presented in Fig. 3.72 where supplementary CS and CD buffers were used at input and output ports. This filter is able to cover a wide frequency range with a corresponding current consumption.

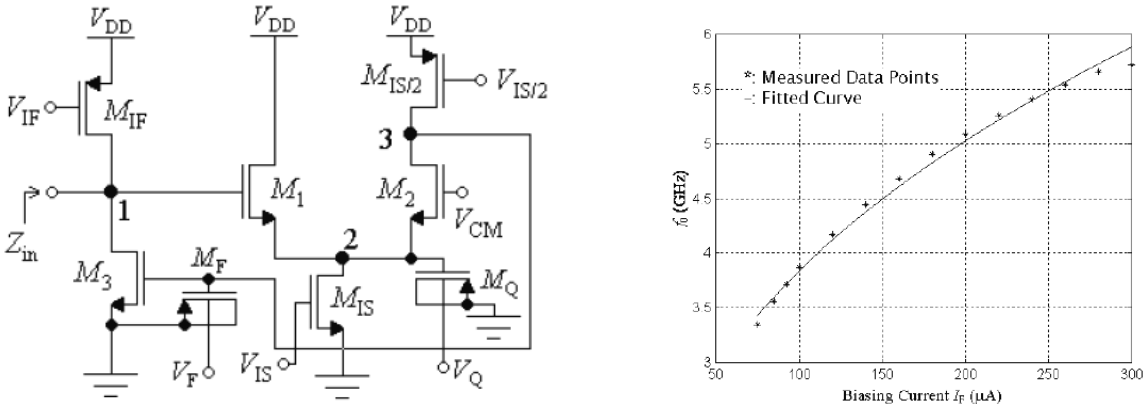


Fig. 3.72 Active inductor and its frequency capability [3.67]

An improved version of this topology has been reported in [3.68]. The same filter was designed also in AMS 0.35μm CMOS process with a centre frequency of 2.32 GHz as reported in [3.69] which consumes 5.1mW from a 2.4V supply voltage.

The simulated inductor proposed in [3.40] has been used for the implementation of an RF bandpass filter [3.70] with wide frequency tuning range (Fig. 3.73). Designed in TSMC 0.25μm CMOS process, the filter centre frequency can be tuned from 1.6 GHz to 2.45 GHz with an average power consumption of 8.6mW when biased from a 1.8V supply voltage.

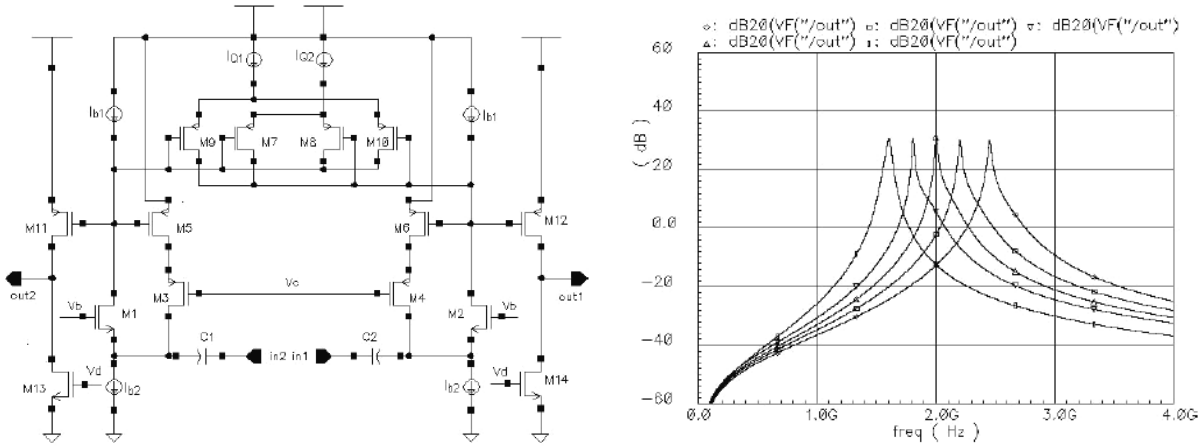


Fig. 3.73 Wide frequency tuning range TOSI based RF bandpass filter [3.70]

A single–ended RF bandpass filter based on the active inductor proposed by Ismail [3.44] was designed in AMS 0.35µm CMOS technology (Fig. 3.74) [3.71]. The filter covers the frequencies from 0.5 GHz to 1.3 GHz proving a total current consumption of 54mA when the circuit is biased by a 3.5V supply voltage and has a noise factor of 8.5 dB.

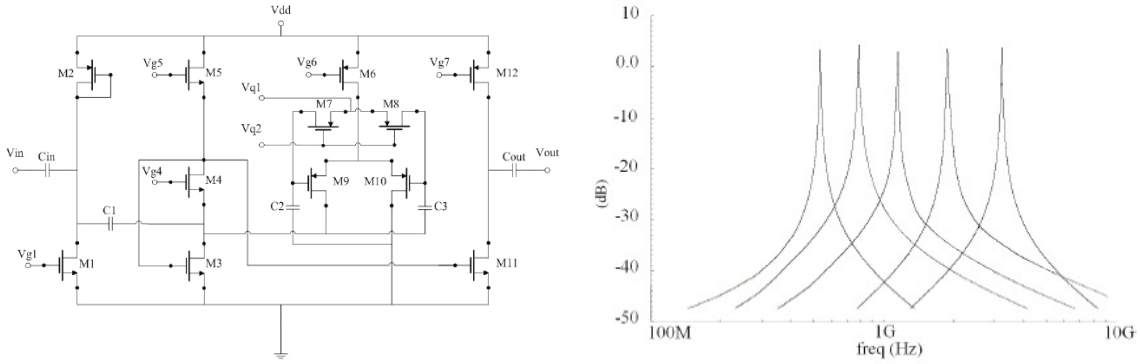


Fig. 3.74 2nd order TOSI based RF bandpass filter and frequency response [3.71]

Until now, transistor based input buffers were used to convert the input voltage signal to a current one, required for the proper inductor functioning. However, another interesting possibility was reported in [3.72] where very small on-chip capacitors can be used as well to implement this conversion. The authors proposed a modified version of the TOSI reported in [3.40] making use of input capacitors as shown in Fig. 3.75. A differential bandpass filter – similar to the previous one reported in Fig. 3.42 excepting the input capacitor – was designed in 0.35µm CMOS process, having a resonant frequency of 2.5 GHz. The filter consumes only 1.68mA when biased from a 2V supply voltage. The centre frequency can be tuned between 2.4 GHz and 2.6 GHz.

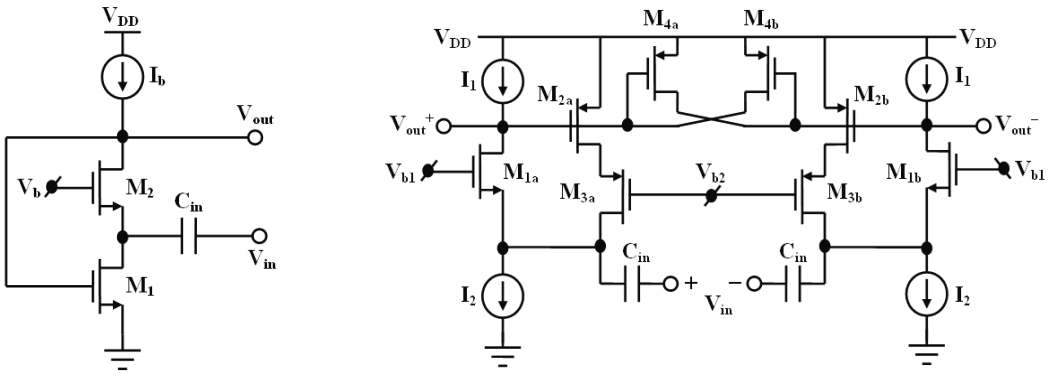


Fig. 3.75 Single–ended and tunable differential RF bandpass filter [3.72]

3.4.2 RF Filters with Multiple TOSI Cells

In this section several high order RF filters based on the TOSI concept are reviewed. As will be further noticed, the most reliable method to implement high order filters is to couple more (almost) identical 2nd order TOSI cells through coupling capacitors with appropriate values.

A lowpass filter based on the 3–transistor CMOS TOSI previously reported in [3.42] aiming RF filtering was designed at the frequency of 4.57 GHz [3.73]. The complete circuit configuration is presented in Fig. 3.76 together with its frequency response.

The filter consists of two ideally identical second-order sections (the TOSI structure) and one source-follower output buffer which act as a first-order lowpass filter. PMOS buffers are used to work at low V_{CM}. The on-chip capacitor C_C and C_N are used for additional control of the filter performance. As it can be noticed, varactors are used for separate frequency and quality factor tuning. Designed in TSMC 0.18μm technology, the circuit has a total power consumption of only 1.6mW from a 1.8V supply voltage.

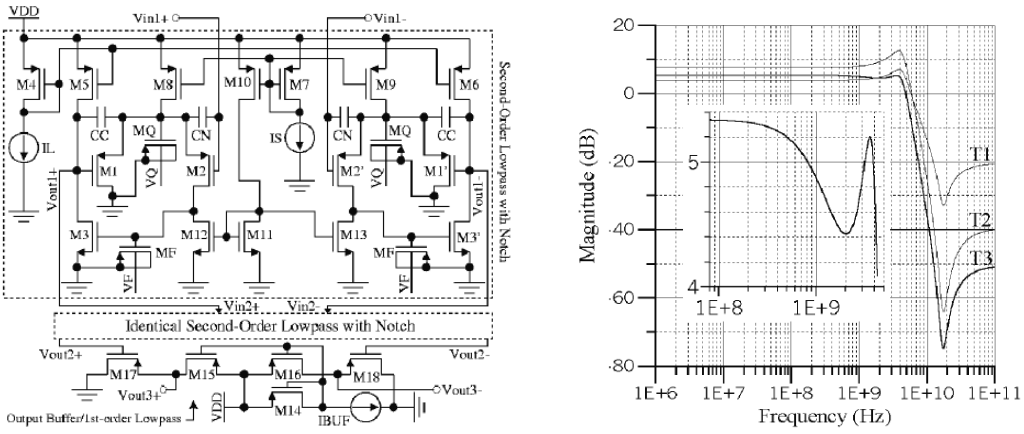


Fig. 3.76 4.57 GHz TOSI based fifth-order lowpass filter [3.73]

A 4th order RF bandpass filter obtained by cascading two 2nd order cells identical to that proposed in [3.72] and working at 2.51 GHz with 70 MHz bandwidth, has been reported in the same paper (Fig. 4.77). The filter frequency characteristics are shown in Fig. 3.78.

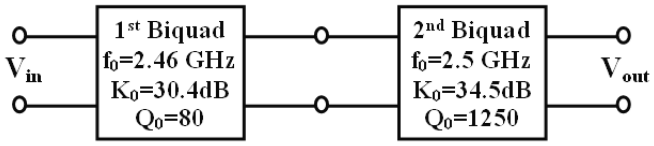


Fig. 3.77 4th order bandpass filter obtained by cascading 2nd order cells [3.72]

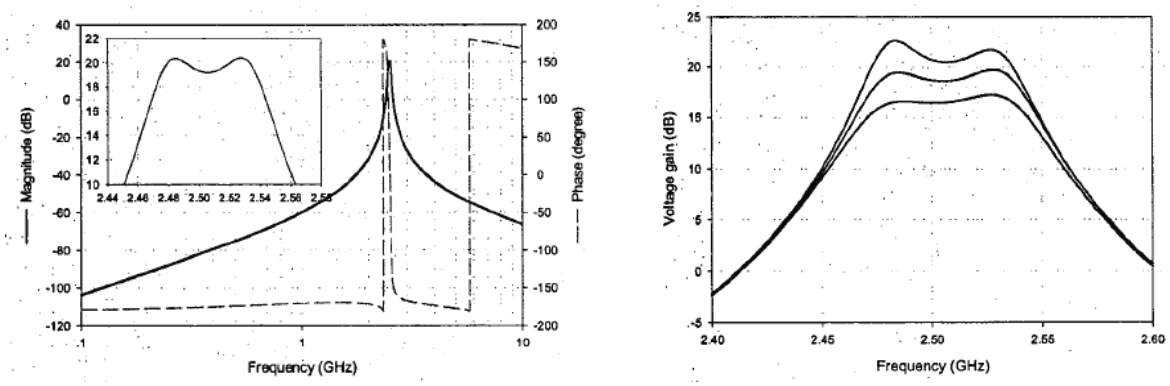
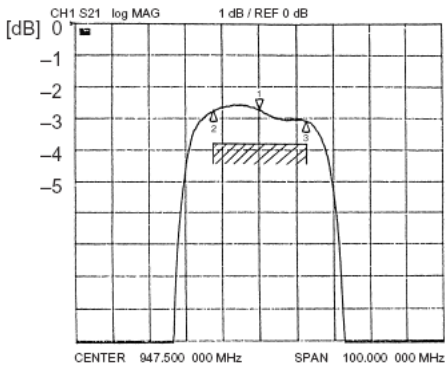


Fig. 3.78 Magnitude (phase) response and Q-tuning possibility [3.72]

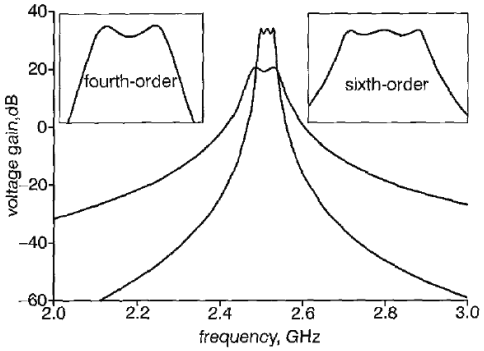
These reported results are very important for further design on this research topic since the implementation of an RF bandpass filter with very high Q aiming wireless standards is still a challenge. As it can be noticed from Fig. 3.78, this 4th order filter offers only 13 dB attenuation in a band of 30 MHz which is not suitable for wireless applications constraints compared to the SAW GSM Rx RF filter MF1043S-1. The latter, designed for the frequency band 935–960 MHz, offers in a stopband bandwidth of 20 MHz a minimum attenuation of 20 dB (typically 37 dB) as shown in Fig. 3.79.



Parameter	MF1043S-1 Min	Typ	Max	Units
PASSBAND FREQUENCY	935 – 960			MHz
PASSBAND CHARACTERISTICS				
Insertion Loss		3.1	3.8	dB
Ripple		0.8	1.5	dBp-p
VSWR		2.0	3.0	
STOPBAND ATTENUATION				
0 – 860 MHz	40	50		dB
860 – 905 MHz	25	42		dB
905 – 915 MHz	20	37		dB
990 – 1040 MHz	20	27		dB
1040 – 1200 MHz	40	50		dB

Fig. 3.79 Frequency specifications for MF1043S-1 Rx GSM filter

The active filter remains attractive by its power consumption (only 3.36mW from 2V supply voltage) and may be suitable for WLAN, Bluetooth or UWB applications where the out-of-band requirements are more relaxed than for the GSM case. In any case, the coupling of a third supplementary 2nd order cell can be an advantage. The version of a 6th order RF bandpass filter consisting of three 2nd order coupled cells was also reported by the same author in [3.74]. The frequency characteristics are shown in Fig. 3.80 together with a comparative study between 4th and 6th order filters performances.



Parameters	Fourth-order		Sixth-order	
Technology	0.35 µm CMOS		0.35 µm CMOS	
Power supply voltage	2 V		2 V	
Total supply current	2.2 mA		3.17 mA	
Centre frequency	2.4-2.6 GHz		2.4-2.6 GHz	
-3 dB bandwidth	20-200 MHz		20-200 MHz	
Maximum passband gain	0-40 dB		0-40 dB	
Input referred noise	395 μV_{rms}	f_0=2.5 GHz	405 μV_{rms}	f_0=2.51 GHz
IIP3	-10 dBV	Q_0=36	-20 dBV	Q_0=70
SFDR	24 dB	K_0=20 dB	20 dB	K_0=34 dB

Fig. 3.80 6th order TOSI based RF bandpass filter [3.74]

A 4th order RF bandpass filter has been reported also by Ismail in 2004 [3.75][3.76]. The filter was obtained by coupling two identical 2nd order cells (Fig. 3.81) and has the frequency response illustrated in the same figure. This proposed version has the advantage of using matched bandpass cells but external LNAs must used to compensate the signal loss created by the input/output buffers. A drawback is the low centre frequency achieved through this method.

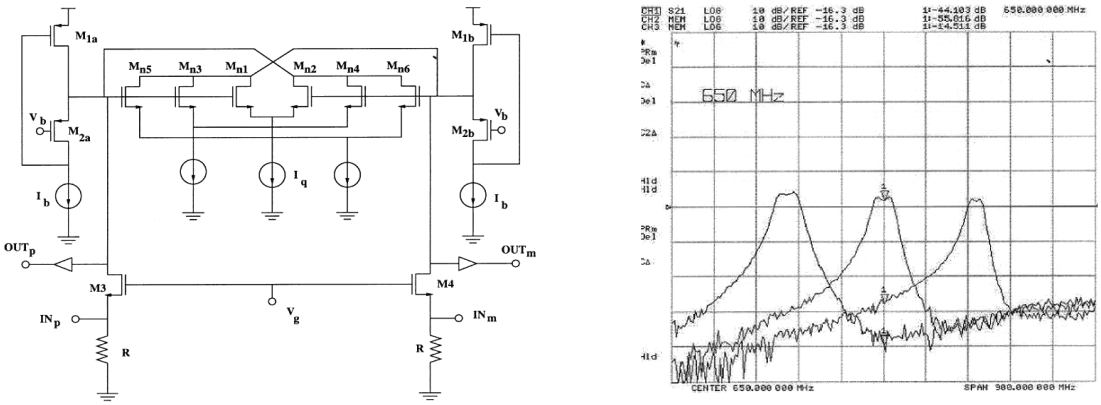


Fig. 3.81 4th order TOSI based bandpass filter [3.75]

The inductor proposed in [3.57] has been used for the implementation of a 5th order RF CMOS bandpass filter in 0.18µm CMOS technology. The architecture is presented in Fig. 3.82 together with its frequency response. This topology proves frequency tuning capability (3.45–3.6 GHz) with the cost of high power consumption (28 mW from 1.9V) and NF (13–18 dB).

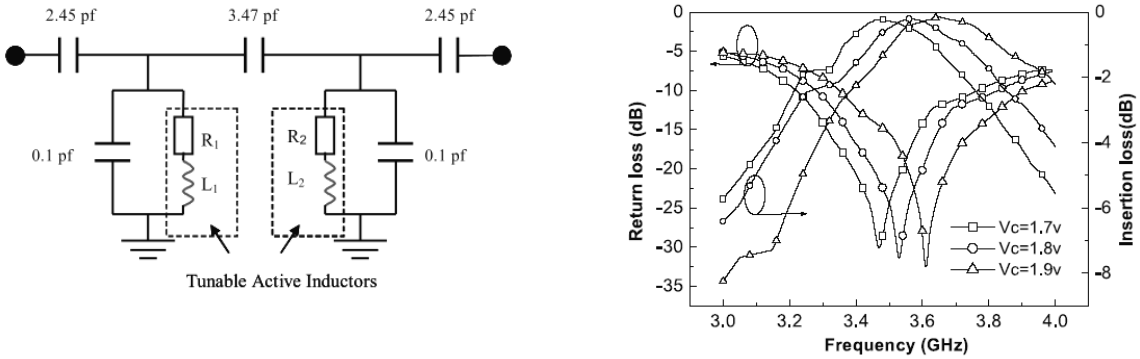


Fig. 3.82 5th order RF bandpass filter and frequency response [3.57]

3.5 CONCLUSION

Active inductors, based on the gyrator theory, have a long history and demonstrate good performances for RF applications, significant enough in order to be considered as a possibility of implementing reconfigurable RF devices and even RF filters. This chapter reviewed the most active inductor topologies proposed until now in literature, being written as a state of the art in this field and emphasizing the promising results achieved in the both MESFET and CMOS technologies.

3.6 REFERENCES

[3.1] International Technology Roadmap for Semiconductors, 2007 (www.itrs.net)

[3.2] Scaling LC Oscillators in Nanometer CMOS Technologies to a Smaller Area but With Constant Performance, S. –A. Yu and P. R. Kinget, IEEE Transactions on Circuits and Systems – II: Express Briefs, Vol. 56, No. 5, pp. 354 – 358, May 2009

[3.3] Fundamentals of Circuits and Filters, W. –K. Chen, CRC Press, 2009

[3.4] The gyrator, a new electric network element, B. D. H. Tellegen, Phillips Res. Rep., 3, 81–101, 1948

[3.5] Proposed Adjustable Tuned Circuits for Microelectronics Structures, B. D. Anderson, W. New and R. Newcomb, Proceedings of the IEEE, Vol. 54, No. 3, pp. 411–411, March 1966

[3.6] RC-Gyrator Cascade Synthesis, J. B. Murdoch, IEEE Transactions on Circuit Theory, Vol. 11, No. 2, pp. 268 – 271, June 1964

[3.7] Practical Realization of a Gyrator Circuit and RC-Gyrator Filters, B. A. Shenoi, IEEE Transactions on Circuit Theory, Vol. CT.-12, No. 3, pp. 374–380, Sept. 1965

[3.8] Inductorless filters: a survey, G. S. Moschytz, IEEE Spectrum, pp. 63–75, Sept. 1970

[3.9] Realization of gyrators using operational amplifiers and their use in RC-active network synthesis, A. Antoniou, IEE Proc., Vol. 116, No. 11, pp. 1838–1850, Nov. 1969

[3.10] Filter Theory and Design: Active and Passive, A. S. Sedra and P. O. Brackett, Pitman Publishing Limited, 1978

[3.11] Monolithic Tunable Active Inductor with Independent Q Control, C. Leifso, J. W. Haslett and J. G. McRoy, IEEE Transactions on Microwave Theory and Techniques, Vol. 48, No. 6, June 2000

[3.12] A Fully Integrated Active Inductor with Independent Voltage Tunable Inductance and Series-Loss Resistance, C. Leifso and J. W. Haslett, IEEE Transactions on Microwave Theory and Techniques, Vol. 49, No. 4, April 2001

[3.13] MMIC-Simulated Inductors Using Compensated Gyrators, S. E. S. – Fort and L. Billonnet, John Wiley & Sons, Inc., pp. 241–249, 1997

[3.14] A novel high Q active inductor for millimeter wave applications, G. Avitable, B. Chellini, F. Giannini and E. Limiti, Proceedings of the 30th European Microwave

Conference, vol. 1, pp. 198–201, Oct. 2000

[3.15] A Wide Tuning-Range CMOS VCO With a Differential Tunable Active Inductor, IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 9, 2006

[3.16] Analog CMOS Filters for Very High Frequencies, B. Nauta, Kluwer Academic Publishers, 1993

[3.17] On Power Transmission of LC Ladder Filters Using Active Inductor Realizations, M. M. Green, IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 43, No. 6, June 1996

[3.18] CMOS Active Filter Design at Very High Frequencies, Y. –Ti Wang and A. A. Abidi, IEEE Journal of Solid–State, Vol. 25, No. 6, Dec. 1990

[3.19] Equivalent Inductance and Q of a Capacitor-Loaded Gyrator, T. N. Rao, P. Gray and R. W. Newcomb, IEEE Journal of Solid–State Circuits, Vol. 2, No. 1, March 1967

[3.20] Gyrator-Based Synthesis of Active On-Chip Inductances, T. Bakken and J. Choma, Analog Integrated Circuits and Signal Processing, Vol. 34, pp. 171–181, 2003

[3.21] Design of Analog CMOS Integrated Circuits, B. Razavi, McGraw Hill International Edition, 2001

[3.22] Broadband Monolithic Microwave Active Inductor and Its Application to Miniaturized Wide-Band Amplifiers, S. Hara, T. Tokumitsu, T. Tanaka and M. Aikawa, IEEE Transactions on Microwave Theory and Techniques, Vol. 36, No. 12, Dec. 1988

[3.23] An Active MMIC Power Divider with Active Inductor Termination, Y. Wang, B. L. Ool and M. S. Leong, Microwave and Optical Technology Letters, Vol. 28, No. 3, Feb. 2001

[3.24] Lossless Broad-Band Monolithic Microwave Active Inductors, S. Hara, T. Tokumitsu and M. Aikawa, IEEE Transactions on Microwave Theory and Techniques, Vol. 37, No. 12, Dec. 1989

[3.25] A novel loss compensation technique for high-Q broad-band active inductors, H. Hayashi, M. Muraguchi, Y. Umeda and T. Enoki, IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 103 – 106, June 1996

[3.26] A High-Q Broad-Band Active Inductor and Its Application to a Low-Loss Analog Phase Shifter, H. Hayashi, M. Muraguchi, Y. Umeda and T. Enoki, IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 12, Dec. 1996

[3.27] Low power, tunable active inductor and its applications to monolithic VCO and

BPF, J. –Su Ko and K. Lee, IEEE MTT-S Digest, pp. 929 – 932, 1997

[3.28] A Novel Broad-Band MMIC VCO Using an Active Inductor, H. Hayashi and M. Muraguchi, Analog Integrated Circuits and Signal Processing, Vol. 20, pp. 103 – 109, 1999

[3.29] Monolithic Narrow-Band Filter Using Ultrahigh-Q Tunable Active Inductors, S. Lucyszyn and I. D. Robertson, IEEE Transactions on Microwave Theory and Techniques, Vol. 42, No. 12, Dec 1994

[3.30] New Approach to the Design of Active Floating Inductors in MMIC Technology, S. G. El Khoury, IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 4, April 1996

[3.31] A High-Speed Continuous-Time Bandpass VHF Filter in MOS Technology, M. Ismail, R. Wassenaar and W. Morrison, pp. 1761–1764, 1991

[3.32] VHF CMOS integrated active inductor, A. Thanachayanont and A. Payne, Electronics Letters, Vol. 32, No. 11, pp. 999–1000, 1996

[3.33] Novel High-Q Inductor using Active Inductor Structure and Feedback Parallel Resonance Circuit, S. Seo, N. Ryu, H. Choi and Y. Jeong, IEEE Frequency Integrated Circuits Symposium, 2007, pp. 467-470

[3.34] A 3-V RF CMOS Bandpass Amplifier Using an Active Inductor, A. Thanachayanont and A. Payne, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, ISCAS '98, Vol. 1, pp. 440-443, Monterey, CA, June 1998

[3.35] Programmable Low Noise Amplifier with Active-Inductor Load, W. Zhuo, J. P. de Gyvez and E. S. –Sincencio, IEEE International Symposium on Circuits and Systems, Vol. 4, pp. 365-368, 1998

[3.36] A Compact Quadrature Hybrid MMIC Using CMOS Active Inductors, H. –H. Hsieh, Y. –T. Liao and L. –H. Lu, IEEE Transactions on Microwave Theory and Techniques, Vol. 55, No. 6, pp. 1098-1104, 2007

[3.37] A 5.7-GHz Low-Noise Amplifier with Source-Degenerated Active Inductor, C. –H. Chu, I. –L. Huang, Y. –H. Lin and J. Gong, Microwave and Optical Technology Letters, Vol. 51, No. 8, pp. 1955-1958, 2009

[3.38] An ω_0-Q Tunable CMOS Active Inductor for RF Bandpass Filters, R. M. Weng and R. C. Kuo, 2007

[3.39] Practical Considerations in the Use of CMOS Active Inductors, W. Bucossi and J. P. Becker, IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF

Systems, SiRF 2008, pp. 90-93, Orlando, FL, Jan. 2008

[3.40] A 1.5-V High-Q CMOS Active Inductor for IF/RF Wireless Applications, A. Thanachayanont, IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS), 2000, pp. 654-657

[3.41] A 1.5-V CMOS Fully Differential Inductorless RF Bandpass Amplifier, A. Thanachayanont, Proc. IEEE ISCAS 2001, Vol. 1, pp. 49-52, 2001

[3.42] A High-Frequency High-Q CMOS Active Inductor with DC Bias Control, A. I. Karşilayan and R. Schaumann, IEEE Midwest Symposium on Circuits and Systems, Vol. 1, pp. 486-489, Aug. 2000

[3.43] A Low-Voltage Low-Power CMOS 5-GHz Oscillator Based on Active Inductors, H. Xiao and R. Schaumann, 9th IEEE International Conference on Electronics, Circuits and Systems (ICECS2002), Vol. 1, pp. 231-234, 2002, Croatia

[3.44] A Novel CMOS Fully Differential Inductorless RF Bandpass Filter, Y. Wu, M. Ismail and H. Olsson, IEEE International Symposium on Circuits and Systems (ISCAS), pp. 149-152, Vol. 4, 2000

[3.45] CMOS VHF/RF CCO based on active inductors, Y. Wu, M. Ismail and H. Olsson, Electronics Letters, Vol. 37, No. 8, pp. 472–473, 2001

[3.46] Low voltage high Q VHF CMOS transistor-only active inductor, A. Thanachayanont and S. S. Ngow, The 45th Midwesr Symposium on Circuits and Systems, MWSCAS 2002, Vol. 3, pp. III-552 – III.555, Aug. 2002

[3.47] CMOS Transistor-Only Active Inductor for IF/RF Applications, A. Thanachayanont, IEEE International Conference on Industrial Technology, ICIT 2002, Vol. 2, pp. 1209–1212, 2002

[3.48] A 1.75GHz Inductor-less CMOS Low Noise Amplifier With High-Q Active Inductor Load, J. –N. Yang, Y. –C. Cheng, T. –Yin Hsu, T. –R. Hsu and C. –Yi Lee, Proc. of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems, MWSCAS 2001, Vol. 2, pp. 816-819, 2001

[3.49] Improved Quality-Factor of 0.18-um CMOS Active Inductor by a Feedback Resistance Design, C. –C. Hsiao, C. –W. Kuo, C. –C. Ho and Y. –J. Chan, IEEE Microwave and Wireless Components Letters, Vol. 12, No. 12, Dec. 2002

[3.50] Reconfigurable RFICs for Frequency-Agile VCOs in Si-Based Technology for Multi-Standard Applications, R. Mukhopadhyay, Y. Park, P. Sen, N. Srirattana, J. S. Lee, S. Nuttinck, A. J. Joseph, J. D. Cressler and J. Laskar, IEEE MTT-S International

Microwave Symposium Digest, Vol. 3, pp. 1489-1492, 2004

[3.51] Reconfigurable RFICs in Si-Based Technologies for a Compact Intelligent RF Front-End, R. Mukhopadhyay, Y. Park, P. Sen, N. Srirattana, J. S. Lee, C. –H. Lee, S. Nuttinck, A. J. Joseph, J. D. Cressler and J. Laskar, IEEE Transactions on Microwave Theory and Techniques, Vol. 53, No. 1, 2005

[3.52] Investigation of Inductors for Digital Si-CMOS Technologies, R. Mukhopadhyay, S. W. Yoon, Y. Park, C. –H. Lee, S. Nuttinck and J. Laskar, IEEE International Symposium on Circuits and Systems, ISCAS, pp. 3750-3753, 2006

[3.53] A CMOS Multi-band Low Noise Amplifier Using High-Q Active Inductors, M. –J. Wu, Y. –H. Lee, Y. –Y. Huang, Y. –M. Mu and J. –T. Yang, International Journal of Circuits, Systems and Signal Processing, Issue 2, Vol. 1, pp. 199–202, 2007

[3.54] A Radio Frequency CMOS Band Pass Amplifier Using High-Q Active Inductor Loads with Binary Code for Multi-Band Selecting, M. –J. Wu, P. –J. Yen, C. –C. Chou, J. –T. Yang, Proceedings of the 6th WSEAS International Conference on Instrumentation, Measurement, Circuits & Systems, pp. 138-143, 2007

[3.55] Designs of CMOS Multi-band Voltage Controlled Oscillator Using Active Inductors, M. –J. Wu, Y. –Y. Huang, Y. –H. Lee, Y. –M. Mu and J. –T. Yang, International Journal of Circuits, Systems and Signal Processing, Issue 2, Vol. 1, pp. 207-210, 2007

[3.56] Wideband 0.18μm CMOS VCO Using Active Inductor with Negative Resistance, G. Szczepkowsji, G. Baldwin and R. Farrell, 18th European Conference on Circuit Theory and Design, ECCTD 2007, pp. 990-993, Seville, 2007

[3.57] CMOS RF Band-Pass Filter Design Using the High Quality Active Inductor, K. –H. Liang, C. –C. Ho, C. –W. Kuo and Y. –J. Chan, IEICE Trans. Electron., Vol. E88-C, No. 12, 2005

[3.58] A Design of CMOS Broadband Amplifier with High-Q Active Inductor, J. –N. Yang, Y. –C. Cheng and C. –Yi Lee, The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications, pp. 86-89, July 2003

[3.59] Voltage Controlled Phase Shifters on CMOS Technology, G. Mascarenhas, J. C. Vaz and J. C. Freire, Proceedings of Asia-Pacific Microwave Conference, 2006

[3.60] An Optimization Technique for RF Buffers with Active Inductors, T. –C. Lee and Y. –C. Huang, IEEE International Symposium on Circuits and Systems, Vol. 4,

pp. 3692-3695, 2005

[3.61] NMOS transistors based Karsilayan & Schaumann gyrator: 'lowpass and bandpass filter applications', H. Barthélemy and W. Rahajandraibe, IEEE International Symposium on Micro-NanoMechatronics and Human Science, Vol. 1, pp. 97-100, 2003

[3.62] Design of a wide tuning range VCO using an active inductor, M. Fillaud and H. Barthélemy, Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference, NEWCAS-TAISA 2008, pp. 13-16, Montreal, June 2008

[3.63] A Widely Tunable Active RF Filter Topology, K. Allidina and S. Mirabbasi, IEEE International Symposium on Circuits and Systems, ISCAS 2006, pp. 879-882, 2006

[3.64] CMOS source degenerated differential active inductor, C. L. Ler, A. K. B. A'ain and A. V. Kordesh, Electronics Letters, Vol. 44, No. 3, pp. 2008

[3.65] Compact, High-Q, and Low-Current Dissipation CMOS Differential Active Inductor, C. –L. Ler, A. K. B. A'ain and A. V. Kordesh, IEEE Microwave and Wireless Components Letters, Vol. 18, No. 10, pp. 683-685, 2008

[3.66] VHF Current – Mode Filter Based on Intrinsic Biquad of the Regulated Cascode Topology, U. Yodprasit and K. Sirivathanant, IEEE International Symposium on Circuits and Systems, ISCAS, Vol. 1, pp. 172 – 175, 2001

[3.67] A Radio-Frequency CMOS Active Inductor and Its Application in Designing High-Q Filters, H. Xiao, R. Shcaumann, W. R. Daasch, P. K. Wong and B. Pejcinovic, IEEE International Symposium on Circuits and Systems, ISCAS, Vol. 4, pp. IV- 197-200, 2004

[3.68] A 5.4-GHz high-Q tunable active-inductor bandpass filter in standard digital CMOS technology, H. Xiao and R. Schaumann, Analog Integrated Circuits and Signal Processing, Vol. 51, No. 1, pp. 1-9, 2007

[3.69] A 2.3-GHz CMOS High-Q Bandpass Filter Design using an Active Inductor, D. Córdova, J. De la Cruz and C. Silva, XV Workshop Iberchip, pp. 496–500, Buenos Aires, Argentina, 2009

[3.70] A CMOS Bandpass Filter with Wide-Tuning Range for Wireless Applications, Z. Gao, M. Yu, Y. Ye and J. Ma, IEEE International Symposium on Circuits and Systems, ISCAS, 2006

[3.71] A Tunable 0.5-1.3 GHz CMOS 2nd order Bandpass Filter with 50Ω Input-Output

Impedance Matching, V. Stornelli, G. Ferri, G. Leuzzi and A. De Marcelis, IEEE International Symposium on Circuits and Systems, ISCAS, 2006

[3.72] 2-V 3.36-mW 2.5-GHz Fourth-Order Inductorless CMOS RF Bandpass Filter, A. Thanachayanont, Asia-Pacific Conference on Circuits and Systems, APCCAS, Vol. 1, pp. 127-130, 2002

[3.73] Very-High-Frequency Lowpass Filter Based on a CMOS Active Inductor, H. Xiao and R. Schaumann, IEEE International Symposium on Circuits and Systems, ISCAS, Vol. 2, pp. II-1 – II. 4, 2002

[3.74] Low-voltage low-power high-Q CMOS RF Bandpass filter, A. Thanachayanont, Electronics Letters, Vol. 38, No. 13, 2002

[3.75] RF Bandpass Filter Design Based on CMOS Active Inductors, Y. Wu, X. Ding, M. Ismail and H. Olsson, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 50, No. 12, pp. 942-949, 2003

[3.76] CMOS Active Inductor and Its Application in RF Bandpass Filter, Y. Wu, X. Ding, M. Ismail and H. Olsson, IEEE Radio Frequency Integrated Circuits Symposium, pp. 655-658, 2004

4. FREQUENCY RESPONSE IMPROVEMENT OF CMOS TOSIs

4.1 Introduction

As noticed in Chapter 2, the filtering part represents a critical issue when implementing RF transceivers. Although SAW passive filters solved the stringent telecommunications requirements, the RF filtering part still remains a challenge. These are bulky, expensive (at least 8 SAW filters are used in reconfigurable wireless devices) and offer no tuning possibility. In other words, once a problem solved a new one arises.

A possible solution is to fully implement the reconfigurability option into the baseband part. So far this represents an only ideal transceiver although some successful preliminary steps were achieved (SDR). Moreover, as noticed in the second chapter, the SAW preselective filter is still in use in SDR configurations. A second possibility is to replace the SAW passive filters with LC (pseudo) passive ones. Although some attempts were reported in literature, these are not suitable for current multi–standard transceivers owing to their large chip area. The third one is to use RF MEMS filters but no successful solution has been reported in the literature.

The fourth possibility is to develop SAW–less architectures and some attempts succeeded in this regard. This represents an original and efficient solution but alternative RF architectures for replacing the classical ones must be explored and developed in such way that the RF filter is useless.

Finally, the fifth possibility consists in using entirely active RF filters based on TOSI architectures.

As stated previously, TOSI based active filters may be used for RF filtering mainly due to their simplicity and small chip area. However, until now, no architecture has been proposed to fulfill the stringent out–of–band telecommunications filtering requirements. Since several 2^{nd} order TOSI cells must be connected in order to satisfy the attenuation requirements, it is obvious that working with good 2^{nd} order TOSI cells is a must when talking about, frequency and quality factor tuning. This is the reason why, the research focused on finding solutions to ameliorate the frequency response of simulated inductors

and not on designing TOSI based bandpass filters dedicated to a particular telecommunications application. Other problems, typical for active filters, like dynamic range, linearity, noise and stability depend on the particular design and consequently are not addressed.

4.2 Simulated Inductor Equivalent Passive Model

From the very beginning, the idea behind the simulated inductors (TOSI) was the desire to obtain an ideal inductor. In other words, only the inductance value was of interest. However, since the inductor is actively implemented with transistors and parasitics are inherent to all transistors, either CMOS/MESFET or bipolar, the gyrator is not ideal. Moreover, from the TOSI architectures previously presented, it seems much easier to build almost ideal MESFET based TOSI architectures than MOSFET ones. The bipolar TOSI structures are even more difficult since the base resistance together with C_{π} introduces a new pole and a negative resistance is added in parallel to the simulated inductance which is not the case of MOSFET implementations. Thus, the parasitics have a stronger negative effect in the bipolar case rather than in the CMOS one.

In this section, a more accurate RLC model is proposed for TOSI inductors. Although for lower frequencies both RLC models are similar regarding the frequency behavior, our proposed model gives better results for higher frequencies in GHz domain.

4.2.1 CMOS Transistor Small–Signal Models

The first step in finding TOSI equivalent model is to determine the input impedance Z_{in} since any TOSI architecture is in fact 1–port network. This point of view is true mainly when the inductive behavior is envisaged in practical applications where the simulated inductor is directly connected to the circuit (LNAs, phase shifters). For other applications like VCOs, CCOs, bandpass amplifiers / filters, an output buffer is usually used after the TOSI structure in order to reject the loading effect and for matching issue. Another input buffer is necessary to convert the voltage input signal into current signal since all RF circuits work with voltages only. However, the frequency behavior of the final structure is entirely established by the TOSI no matter if a buffer is used or not.

The second step after deciding to compute the input impedance is to establish which small signal model for MOSFET transistors has to be used. As it is well known, time–varying voltages are applied to the transistor terminal in real circuit operation and

depending on the magnitude of these signals, the device operates either with large signals (large signal operation) or small signals (small signal operation). Both regimes are influenced by the capacitive effects of the device. Regarding the MOSFET small signal model, two different models were developed during the time and the most important thing is that erroneous results may be obtained by mixing these two models. Basically, they are the same *hibryd–π* small signal model but the difference between them refers to the transistor capacitor network model used to characterize the transistor behavior.

The first small signal model developed for MOSFET transistors [4.1][4.2] which considers reciprocal capacitors network (Fig. 4.1 – left) is shown in Fig. 4.1 – right. Built for saturated transistors, it is sufficient to describe the transistor behavior in mixed design, intending low frequency applications [4.3]. This transistor model based on the reciprocal capacitor network model is called *capacitance model*.

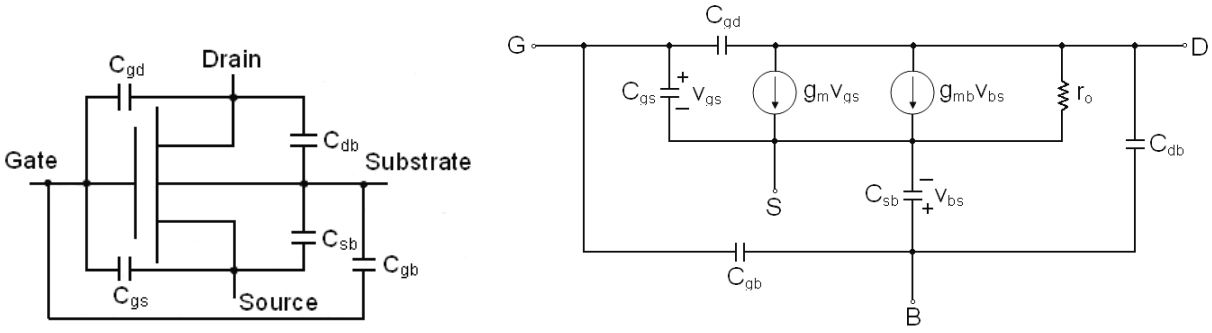


Fig. 4.1 MOSFET capacitances and small–signal model

According to this model, any MOSFET transistor may be used as a transconductor since its small–signal output current (i_d) depends linearly on the small–signal input voltage (v_{gs}) (4.1) and therefore is fully characterized by its transconductance g_m (4.2). Taking into account that the transistor is saturated and thus Eq. (4.3) is true, the final value for g_m is expressed by (4.4) while g_{ds} is given by (4.5). An NMOS transistor was considered and so V_{thn} and μ_n are used.

$$i_d = g_m v_{gs} \tag{4.1}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{4.2}$$

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{thn})^2 \tag{4.3}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{thn}) = \mu_n C_{ox}\frac{W}{L}V_{eff} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{eff}} \tag{4.4}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \lambda \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{thn})^2 = \lambda I_{D-sat} \cong \lambda I_D \quad \Leftrightarrow \quad r_{ds} \cong \frac{1}{\lambda I_D} \tag{4.5}$$

These aspects justify the use of MOS transistors in implementing the simulated inductors (TOSI) and their input buffer. In order not to significantly decrease the input signal power, the input buffer must be designed with very large size for a plus of signal power, linearity and little noise. In all RF circuits which use transistor buffers for matching, the main power consumption is at the input/output buffers. This represents an important difference between digital and RF design since the latter deals with large signal powers compared to the former.

When the source and bulk transistor terminals have different potential, the body–source voltage determines a corresponding change of the transistor threshold voltage (*body effect*). In this case, the drain current depends also on the body–source voltage, being a function of both the gate–source and body–source voltages while the substrate acts as a second gate. In the small–signal transistor model this phenomenon is modeled by a supplementary controlled current source with the conversion ratio g_{mb}. Usually, the transconductance from the main gate (g_m) is typically 3 to 10 times larger than the transconductance from the body (second gate). The expression for V_{th} is given in (4.6) while g_{mb} is expressed in (4.7).

$$V_{th} = V_{th0} + \gamma [\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}] \tag{4.6}$$

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} g_m = \chi g_m \tag{4.7}$$

From (4.6) it is apparent that by connecting the source and bulk together, the body–effect is simply rejected in which case $V_{th}=V_{th0}$. Although preferred from a theoretical point of view, this is not possible in practical implementations where four or even five transistors are stacked. Consequently, the threshold voltage offset problem is avoided only for transistors connected to the ground (NMOS transistors) or supply voltage (PMOS transistors) and not for the mid transistors.

Regarding the parasitic capacitors, four capacitors are sufficient to describe the transistor frequency behavior (C_{gs}, C_{ds}, C_{gd}, C_{bg}), the corresponding network being a reciprocal one. Earlier transistor model did address only the reciprocal behavior for transistor parasitics. From all these, the most important one is the gate to source capacitor C_{gs} which sets the cut–off/transition frequency of the MOS transistor, as expressed by (4.8). This frequency is defined as the frequency where the current–gain is

unity or equivalently 0 dB, meaning that the transistor stops functioning as an amplifier and turns attenuative.

$$f_T = \frac{1}{2\pi}\omega_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gb}+C_{gd}} \tag{4.8}$$

In the saturation region, the parasitic capacitor C_{gd} approaches to zero because the channel pinches off before reaching the drain and thus the drain voltage exerts little influence on either the channel or the gate charge. The parasitic C_{gb} is smaller than C_{gd} and thus both capacitors may be neglected in (4.8). Taking into account that C_{gs} is given by (4.9), where C_{ox} is stated by (4.10) the equivalent relation for f_T is equivalently written in (4.11), where Q_T is the total charge stored in the channel.

$$C_{gs} = \frac{\partial Q_T}{\partial V_{gs}} = \frac{2}{3}WLC_{ox} \tag{4.9}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \tag{4.10}$$

$$f_T = 1.5\frac{\mu_n}{2\pi L^2}V_{eff} \tag{4.11}$$

The last formula simply states that the frequency capability is extended for short channel devices with the price of higher second order effects. In the both RF and digital, a minimum transistor length is used therefore the parasitic capacitors being decreased while g_m and f_T are increased.

So far, it is obvious that this transistor *capacitance model* consists of a reciprocal capacitive network since a simple capacitor is sufficient to be considered between any two transistor terminals in order to model the high frequency transistor behavior. However, although widely used and accurate enough for many applications, this small signal model is not suitable for higher GHz frequencies where another improved model was developed [4.4]. This different model belongs to a second class of transistor models called *charge based capacitance models* and is presented in Fig. 4.2.

This model refers to the non–reciprocal character of the MOS capacitive network and ensures the transistor charge conservation by using the so–called *trans–capacitances*. In this case, the 4–terminal MOSFET device has a small–signal model with 16 transcapacitances as described by (4.12) and (4.13). The trans–capacitance seen from the node *i* to node *j* represents a measure of how the total charge in the node *i* is changed when the voltage of the node j is varied. The time constant τ contains the trans–

capacitance effect while for RF design it takes into account also the parasitic resistances and inductances [2.62]. The relations (4.1)–(4.7) are valid for this second model too.

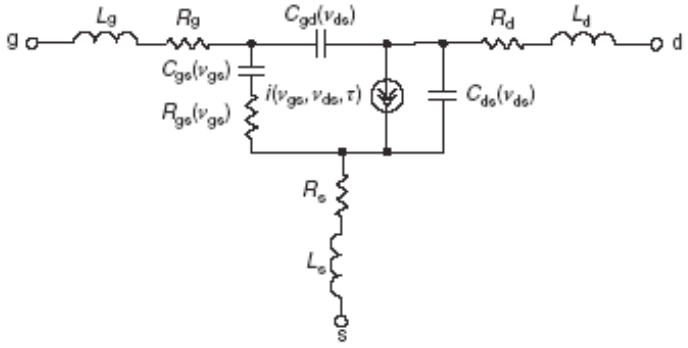


Fig. 4.2 Improved MOSFET small–signal model taking into account trans–capacitances

$$C_{ij} = -\frac{\partial Q_i}{\partial V_{ij}}, \quad i \neq j,\ i, j = G, D, S, B \tag{4.12}$$

$$C_{ij} = \frac{\partial Q_i}{\partial V_{ij}}, \quad i = j \tag{4.13}$$

These relations signify that instead of using C_{gs} given by (4.9) and which characterizes a reciprocal port, three capacitors must be used:

- C_{gs} trans–capacitance used to calculate the total gate capacitance (C_{gg});
- C_{sg} trans–capacitance used to compute the total source capacitance (C_{ss});
- C_{gg} capacitance which represents the total parasitic capacitance seen in the gate of MOS transistor.

The total gate capacitance C_{gg} is positive as C_{dd} or C_{ss} and given by Eg. (4.14) where all trans–capacitances are negative as expressed in (4.12).

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} \tag{4.14}$$

The same discussion is valid for the other trans–capacitances describing the other terminal. An important remark is that two trans–capacitances describing the parasitics of two nodes are different (e.g. $C_{gs} \neq C_{sg}$) and this concentrates the non–reciprocal character of the transistor capacitors network. Moreover, since C_{gs} (denoted here as C_{gs}^{r}) concentrates the reciprocal character of the transistor capacitors model (4.9) and the trans–capacitance C_{gs} the non–reciprocal behavior, $C_{gs}^{r} \neq C_{gs} + C_{sg}$. This is the reason why several RF books emphasized the importance of deciding from the very beginning

what transistor model is to be used since erroneous results may be obtained by mixing these two models.

4.2.2 RLC TOSI Passive Equivalent Model

The active inductor (TOSI) architecture proposed by Ismail in [3.44] (Fig. 4.3) and mentioned previously was used also in this research. An active inductor configuration is optimum for RF design if it has the smallest number of transistors and a minimum number of current mirrors and biasing voltages. These represent intrinsic conditions before going further to practical implementation. During the design process, optimization methods which depend on the particular circuit configuration must be developed in order to minimize the number of current and voltage references. From this point of view, the active inductor proposed by Ismail was chosen as a reference for this research since it has minimum number of transistors (two), current sources (one) and voltage references (one). If the current source is implemented as a simple PMOS transistor than two voltage references must be used.

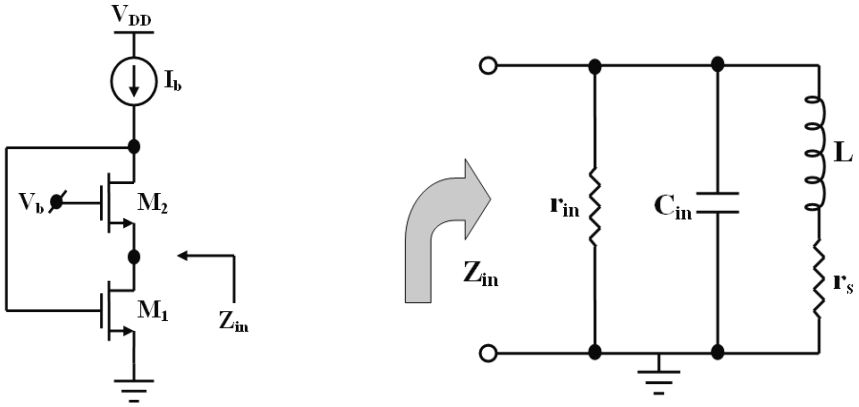


Fig. 4.3 CMOS TOSI and its attributed equivalent RLC model

Taking into account the previous review of MOS transistor models, the input TOSI impedance may be computed not before mentioning that all papers proposing CMOS TOSI architectures, except that proposed by Schaumann, used the classical transistor model (Fig. 4.1). This reciprocal model was used even in the case of inductor simulated at several GHz, fact that has a negative impact on the inductor equivalent passive model and its element values. Consequently, the equivalent TOSI equivalent passive model will be derived in the following basically using the MOS transistor small–signal model presented in Fig. 4.1 where only C_{gs} parasitic capacitance is taken into account since it is

the most significant. The bulk effect is neglected too. Considering again the TOSI structure presented in Fig. 4.3, the following equations describe with good approximation its frequency behavior:

$$\begin{cases}(g_{o1}+g_{o2}+sC_{gs2})v_{(1)}-g_{o2}v_{(2)}=J_{in}-g_{m1}v_{(2)}-g_{m2}v_{(1)}\\ -g_{o2}v_{(1)}+(g_{o2}+sC_{gs1})v_{(2)}=g_{m2}v_{(1)}\end{cases} \tag{4.15}$$

By solving this system, the input impedance $Z_{in}=\frac{v_{(1)}}{J_{in}}$ is obtained as (4.16):

$$Z_{in}=\frac{g_{o2}+sC_{gs1}}{s^2C_{gs1}C_{gs2}+s(g_{o1}C_{gs1}+g_{o2}C_{gs2}+g_{m2}C_{gs1}+g_{o2}C_{gs1})+g_{m1}g_{m2}+g_{m1}g_{o2}+g_{o1}g_{o2}} \tag{4.16}$$

As it can be noticed, the input impedance is a second order transfer function which proves that its equivalent circuit is an RLC resonator that can be used very well in filtering applications and oscillators.

In order to synthesize this transfer function to obtain the equivalent TOSI passive model, some simple synthesis operations are done as follows:

$$Y_{in}=\frac{s^2C_{gs1}C_{gs2}+s(g_{o1}C_{gs1}+g_{o2}C_{gs2}+g_{m2}C_{gs1}+g_{o2}C_{gs1})+g_{m1}g_{m2}+g_{m1}g_{o2}+g_{o1}g_{o2}}{g_{o2}+sC_{gs1}} \tag{4.17}$$

$$Y_{in}=sC_{gs2}+\frac{s(g_{o1}C_{gs1}+g_{m2}C_{gs1}+g_{o2}C_{gs1})+g_{m1}g_{m2}+g_{m1}g_{o2}+g_{o1}g_{o2}}{g_{o2}+sC_{gs1}} \tag{4.18}$$

$$Y_{in}=sC_{gs2}+g_{o1}+\frac{s(g_{m2}C_{gs1}+g_{o2}C_{gs1})+g_{m1}g_{m2}+g_{m1}g_{o2}}{g_{o2}+sC_{gs1}} \tag{4.19}$$

$$Y_{in}=sC_{gs2}+g_{o1}+\frac{g_{m2}(g_{m1}+sC_{gs1})+g_{o2}(sC_{gs1}+g_{m1})}{g_{o2}+sC_{gs1}} \tag{4.20}$$

$$Y_{in}=sC_{gs2}+g_{o1}+\frac{(g_{m2}+g_{o2})(g_{m1}+sC_{gs1})}{g_{o2}+sC_{gs1}} \tag{4.21}$$

$$Y_{in}=sC_{gs2}+g_{o1}+Y' \tag{4.22}$$

$$Y'=\frac{(g_{m2}+g_{o2})(g_{m1}+sC_{gs1})}{g_{o2}+sC_{gs1}}=\frac{sC_{gs1}(g_{m2}+g_{o2})+g_{m1}(g_{m2}+g_{o2})}{sC_{gs1}+g_{o2}} \tag{4.23}$$

If some approximations (4.24) are made in (4.23) for Y' around the frequency of interest, considered in the GHz domain, the synthesized transfer function has the equivalent form in (4.25):

$$g_{m2}>>g_{o2},\quad \omega C_{gs1}>>g_{o2},\quad g_{m2}>>g_{o1} \tag{4.24}$$

$$Y_{in} = sC_{gs2} + g_{m2} + \frac{1}{s\frac{C_{gs1}}{g_{m1}g_{m2}} + \frac{g_{o2}}{g_{m1}g_{m2}}} \tag{4.25}$$

Eq. (4.25), which is another form for (4.16), demonstrates that the equivalent TOSI model is a parallel RLC tank consisting of an inductor ($L_S=C_{gs1}/g_{m1}g_{m2}$ and $r_S=g_{o2}/g_{m1}g_{m2}$), a parasitic resistance ($1/g_{m2}$) and a parasitic capacitor (C_{gs2}). It is clear that the parasitic capacitor C_{gs2} is the only one capacitor seen at the input node. However, these are approximate values since the approximations (4.24) have been considered.

In the ideal case, the resonant frequency of the LC parallel tank, taking into account the approximate inductance value $L_{eq}=C_{gs1}/g_{m1}g_{m2}$ and its parasitic capacitor value $C_{eq}=C_{gs2}$, is given by (4.26):

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C_{eq}}} = \frac{1}{\sqrt{\frac{C_{gs1}}{g_{m1}g_{m2}}C_{gs2}}} = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} = \sqrt{\omega_{t1}\omega_{t2}} \tag{4.26}$$

The last relation (4.26) shows that the self resonant frequency of the CMOS TOSI is in fact the geometric mean of the cut–off transistor frequencies. This relation shows also that when the operational frequency is right the resonant frequency where the active inductor may be used in filtering applications thanks to its good quality factor, one transistor works beyond its cut–off frequency. However, this in not a problem since the amplification is not required for TOSI and on the other hand large gain is expected at the resonant frequency. The self resonant frequency for the real case is obtained from (5.16) too:

$$\omega_o^2 = \frac{g_{m1}g_{m2} + g_{m1}g_{o2} + g_{o1}g_{o2}}{C_{gs1}C_{gs2}} \cong \frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}} \tag{4.27}$$

As it can be noticed, the self resonant depends also on the parasitic series and parallel resistances due to their finite values. If this configuration envisages filtering application then ω_0 is increased when small output resistances are expected for gyrator transistors with negative effect on the inductor quality factor.

For this simulated inductor, the quality factor is given by (4.28), approximate values being used:

$$Q = \frac{\omega L_S}{r_S} = \frac{\omega\frac{C_{gs1}}{g_{m1}g_{m2}}}{\frac{g_{o2}}{g_{m1}g_{m2}}} = \omega\frac{C_{gs1}}{g_{o2}} \tag{4.28}$$

As expected, the output resistance of M_2 sets the inductor quality factor, the higher resistance the higher the quality factor. An increase of r_{ds1} determines an increase of the inductor quality factor and a corresponding decrease of the self resonant frequency. A similar behavior regards the parasitic capacitance C_{gs1}. Due to the circuit simplicity, it is practically impossible to tune the quality factor and self resonant frequency independently.

4.2.3 Improved RLC TOSI Equivalent Passive Model

For the same TOSI architecture presented in Fig. 4.3, a more accurate equivalent model may be obtained if a non–canonical circuit synthesis method is used. This is obtained by processing the expression for $Y^{'}$, being thus an alternative to various approximations made during the synthesis by different authors. The most important approximation considered above was based on the assumption that $\omega C_{gs1} >> g_{o2}$ at the operation frequency which is not always true. If we do not neglect g_{o2}, a single first order transfer function is to be synthesized which is a little difficult because of its intrinsic zero (4.23). In this case, the idea is to continuously expand this fraction so that the following relations are obtained:

$$Y^{'} = \frac{sC_{gs1}(g_{m2}+g_{o2})+g_{m1}(g_{m2}+g_{o2})}{sC_{gs1}+g_{o2}} = \frac{sC_{gs1}(g_{m2}+g_{o2})}{sC_{gs1}+g_{o2}} + \frac{g_{m1}(g_{m2}+g_{o2})}{sC_{gs1}+g_{o2}} \tag{4.29}$$

$$Y^{'} = \frac{1}{\frac{sC_{gs1}+g_{o2}}{sC_{gs1}(g_{m2}+g_{o2})}} + \frac{1}{\frac{sC_{gs1}+g_{o2}}{g_{m1}(g_{m2}+g_{o2})}} \tag{4.30}$$

$$Y^{'} = \frac{1}{\frac{1}{g_{m2}+g_{o2}} + \frac{g_{o2}}{sC_{gs1}(g_{m2}+g_{o2})}} + \frac{1}{s\frac{C_{gs1}}{g_{m1}(g_{m2}+g_{o2})} + \frac{g_{o2}}{g_{m1}(g_{m2}+g_{o2})}} \tag{4.31}$$

$$Y^{'} = \frac{1}{\frac{1}{g_{m2}+g_{o2}} + \frac{1}{sC_{gs1}\frac{g_{m2}+g_{o2}}{g_{o2}}}} + \frac{1}{s\frac{C_{gs1}}{g_{m1}(g_{m2}+g_{o2})} + \frac{g_{o2}}{g_{m1}(g_{m2}+g_{o2})}} \tag{4.32}$$

$$Y^{'} = \frac{1}{\frac{1}{g_{m2}+g_{o2}} + \frac{1}{sC_{gs1}\frac{g_{m2}+g_{o2}}{g_{o2}}}} + \frac{1}{s\frac{C_{gs1}}{g_{m1}(g_{m2}+g_{o2})} + \frac{g_{o2}}{g_{m1}(g_{m2}+g_{o2})}} \tag{4.33}$$

It is obvious that Eq. (4.33) describes an input admittance with two branches: one containing a series RC group and another one containing the LC series group. In other words, the supplementary branch contains a resistance of value $1/(g_{m2}+g_{o2})$ which is

"stronger" or "weaker" coupled to the circuit by the capacitor $C_{gs1}(g_{m2}+g_{o2})/g_{o2}$. This coupling capacitor is practically much larger than transistor parasitic capacitors being in practical implementations hundreds of fF. Although the inductance value is not influenced by this synthesis, the overall self resonant frequency is affected significantly. In other words, this synthesis is important mainly for filtering applications.

The novel model [4.5] is presented in Fig. 4.4 together with the classical one, where the value of G_{eq} is expressed by (4.34). The second improvement consisted in taking into consideration the bulk effect while using the charge based small–signal transistor model (with transcapacitances).

$$G_{eq} = g_{m2} + g_{mb2} + g_{ds2} \tag{4.34}$$

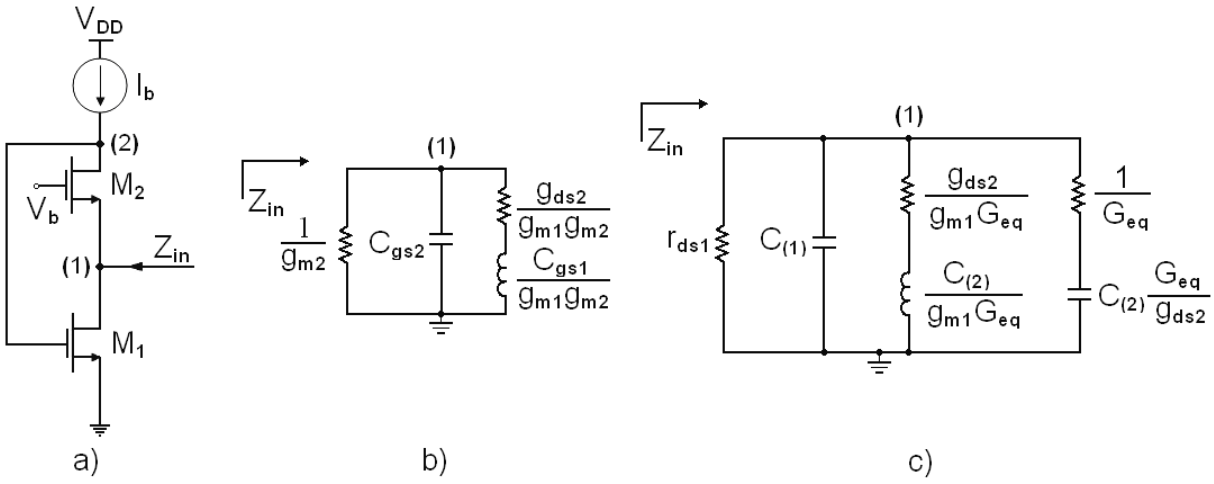


Fig. 4.4 TOSI Architecture (a) with Classical RLC Model (b) and its more Accurate Model (c)

According to the small–signal transistor model, $C_{(i)}$ is the total node capacitance determined by trans–capacitances. By using this RF transistor model, the value of the simulated inductance is changed too; therefore, a second enhancement is obtained for the TOSI equivalent model through such detailed synthesis.

The simulation results are shown in Fig. 4.5 proving the validity and accuracy of the improved model. Even for lower frequencies the classical RLC model gives frequency errors regarding the resonant frequency, the error increasing with frequency from 90 MHz at 860 MHz to 822 MHz at 3.84 GHz. The error given by this improved RLC model is less than 23 MHz in all frequency range.

It is of utmost importance to mention that during the simulations, errors of 30–50% in approximating the inductance value have been obtained with the RLC classical model

compared to the proposed one. The novel simulated inductor parameters are as follows (Eq. 4.35):

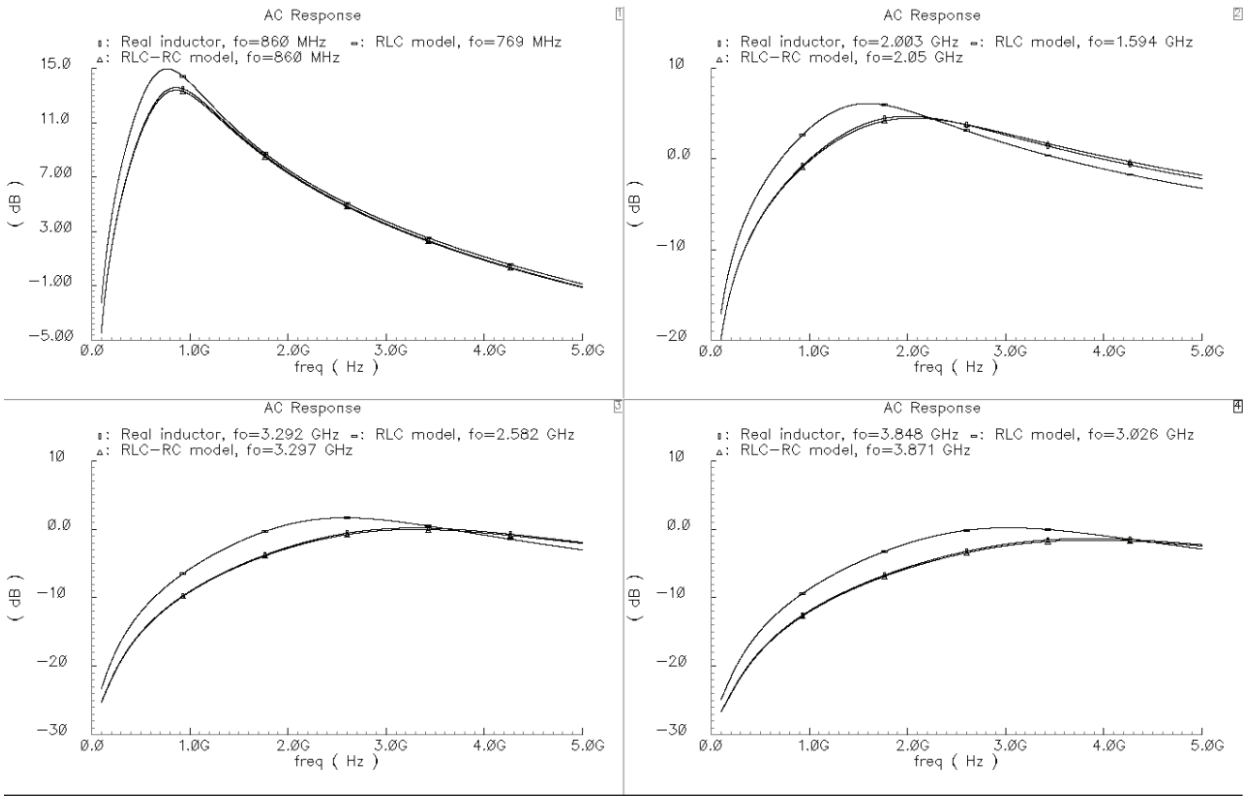


Fig. 4.5 Improved RLC Model vs. Classical RLC Model and Real TOSI

$$\begin{cases} L_S = \dfrac{C_{(2)}}{g_{m1}(g_{m2} + g_{ds2} + g_{mb2})} \\ C_P = C_{(1)} \\ r_S = \dfrac{g_{ds2}}{g_{m1}(g_{m2} + g_{ds2} + g_{mb2})} \end{cases} \tag{4.35}$$

In order to prove the generality of this model and its validity to any particular TOSI architecture, several TOSI architectures proposed in literature and previously presented in Chapter 3 are taken into considerations and studied. If the input impedance for these simulated inductors is identical to that expressed by (4.16) then the equivalent passive model for these structures is the same to the model presented in Fig. 4.4 c). Consequently, the input admittance has been computed for the inductors shown in Fig. 4.6, previously reported in Chapter 3.

Taking into account the transistor symbols in Fig. 4.6 and that the input node is always node (1), the following relations describe the frequency behavior of these simulated inductors (left – 4.36, middle – 4.37 and right – 4.38):

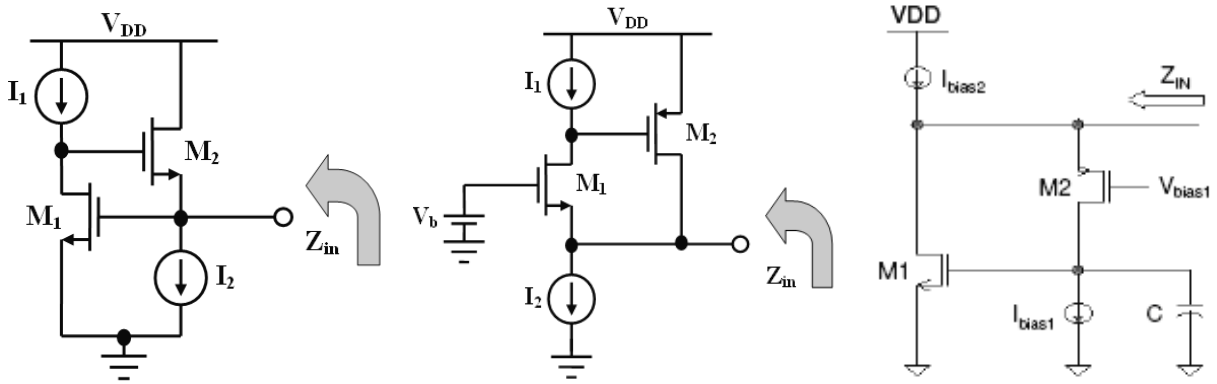


Fig. 4.6 TOSI Architectures with the Same Input Impedance ([3.31], [3.40] and [3.63])

$$\begin{cases}(g_{o1}+s(C_{gs1}+C_{gs2})v_{(1)}-sC_{gs1}v_{(2)}=J_{in}+g_{m1}(v_{(2)}-v_{(1)})\\-sC_{gs1}v_{(1)}+(g_{o2}+sC_{gs1})v_{(2)}=-g_{m2}v_{(1)}\end{cases} \tag{4.36}$$

$$\begin{cases}(g_{o1}+g_{o2}+sC_{gs2})v_{(1)}-g_{o2}v_{(2)}=J_{in}-g_{m1}v_{(2)}-g_{m2}v_{(1)}\\-g_{o2}v_{(1)}+(g_{o2}+sC_{gs1})v_{(2)}=g_{m2}v_{(1)}\end{cases} \tag{4.37}$$

$$\begin{cases}(g_{o1}+g_{o2}+sC_{gs2})v_{(1)}-g_{o2}v_{(2)}=J_{in}-g_{m1}v_{(2)}-g_{m2}v_{(1)}\\-g_{o2}v_{(1)}+(g_{o2}+sC_{gs1})v_{(2)}=g_{m2}v_{(1)}\end{cases} \tag{4.38}$$

Solving these systems, the same input impedance as that expressed by (4.16) is obtained for all three architectures. This signifies that any 2–transistor TOSI architecture has the input impedance given by (4.16) and furthermore the proposed model is sufficiently general to be applied to any TOSI structure.

4.3 Frequency Enhancement Solutions

4.3.1 Negative Resistance and TOSI Loss Compensation

A concept introduced for the first time in 1911 and used first in telecommunications systems, the negative resistance became widespread in the oscillator design (VCOs and CCOs). Basically speaking, the simplest way to compensate an undesired parasitic resistance (denoted as R_P) is to introduce a negative resistance (denoted as R_N) with the same value in series so that R_P is fully compensated. The advantage of this method consists in its frequency independence. Since this technique is impossible in most cases,

the idea of using negative resistance with equal value remains true also when connecting them in parallel, as proved by the following simple calculus:

$$R_{eq} = R_P \parallel (-R_N) = \frac{-R_P R_N}{R_P - R_N} = \frac{R_P R_N}{R_N - R_P} \Rightarrow R_{eq}\Big|_{R_N = R_P} \to \infty \tag{4.39}$$

For any parallel RLC tank, the filter quality factor increases when the parallel resistance increases too, an ideal LC resonator being obtained when this resistance is sufficiently high, theoretically infinite. In practical applications, parallel resistances with values of hundred kΩ are sufficient although values of MΩ are desirable. From the previous chapter it is clear that any active inductor has an equivalent RLC scheme (R_P, C_P, real inductor with L_S and r_S). According to the proposed model, the parallel resistance is in fact the transistor r_{ds} output resistance which in practical implementations has very small values in the range 5 … 10 kΩ or lower, continuously decreasing with frequency due to the higher currents required for operation. This is the reason why small quality factors are obtained at the resonant frequency and consequently, by connecting an external negative resistance in parallel, the effect of this 'parasitic' resistance can be minimized according to (4.39). However, the simulated inductor is not ideal and has a loss series resistance (r_S). By connecting the parallel negative resistance R_N to this series inductance equivalent circuit, the inductor losses may be compensated as well. The equivalent impedance is found as in (4.40).

$$Z_{eq} = (r_S + j\omega L_S) \parallel -R_N = \frac{-(r_S + j\omega L_S)R_N}{(r_S - R_N) + j\omega L_S} = \frac{-R_N (r_S + j\omega L_S)[(r_S - R_N) - j\omega L_S]}{(r_S - R_N)^2 + (\omega L_S)^2}$$

$$Z_{eq} = \frac{-R_N [r_S (r_S - R_N) + (\omega L_S)^2 - j\omega L_S R_N]}{(r_S - R_N)^2 + (\omega L_S)^2} = \frac{-R_N r_S (r_S - R_N) - R_N (\omega L_S)^2}{(r_S - R_N)^2 + (\omega L_S)^2} + \frac{j\omega L_S R_N^2}{(r_S - R_N)^2 + (\omega L_S)^2}$$

$$Z_{eq}\Big|_{\substack{\omega L << r_S \\ r_S < R_N}} \cong r_S - \frac{(\omega L_S)^2}{R_N} + j\omega L_S \tag{4.40}$$

It is obvious that in order to compensate the inductor losses, the real term in (4.40) must be zero which means that relation (4.41) must be fulfilled.

$$r_S - \frac{(\omega L_S)^2}{R_N} = 0 \Rightarrow R_N = \frac{(\omega L_S)^2}{r_S} = \omega L_S Q \tag{4.41}$$

By converting the series inductor model to a parallel one, the equivalent parallel inductor loss resistance (r_P) will give together with R_P an equivalent parallel resistance that will be compensated by the negative resistance. However, since r_P is frequency

dependent, this parallel compensation scheme has the main drawback of being frequency dependent.

If an ideal negative resistance is connected to the TOSI structure in Fig. 4.3, the circuit behavior is described by the system (4.42), where the negative resistance influences the circuit through its conductance $-G_{neg}$. Regarding the equivalent passive model, it is obvious that this negative resistance appear in parallel to the RLC tank.

$$\begin{cases} Z_{in} = \dfrac{b_1 s + b_o}{s^2 + 2\alpha s + \omega_o^2} \\ b_1 = 1/C_{gs2}; \quad b_0 = g_{o2}/C_{gs1}C_{gs2} \\ 2\alpha = \dfrac{C_{gs1}(g_{o1} + g_{m2} + g_{o2} - G_{neg}) + g_{o2}C_{gs2}}{C_{gs1}C_{gs2}} \\ \omega_o^2 = \dfrac{g_{m1}(g_{m2} + g_{o2}) + g_{o2}(g_{o1} - G_{neg})}{C_{gs1}C_{gs2}} \end{cases} \tag{4.42}$$

As expected, the negative resistance influences both the quality factor and resonant frequency. Since $Q=\omega_0/2\alpha$, a good filter quality factor is obtained only by decreasing the term 2α which is the s coefficient which signifies an increase of the negative conductance. This in turn decreases also the self resonant frequency. A general manner to describe the circuit behavior is the following (4.43):

$$\begin{cases} \omega_0 = f_1(g_{m1}, g_{m2}, G_{neg}) \\ Q = f_2(g_{m1}, g_{m2}, G_{neg}) \end{cases} \tag{4.43}$$

4.3.2 Proposed Method for ω_0–Q Independent tuning

In the previous section only an ideal negative resistance was considered in order to offer an intuitive explanation of the compensation technique. In real cases, a cross coupled CMOS pair negative resistance, useful for differential TOSIs or even single–ended is used, as reported by Ismail (Fig. 4.7).

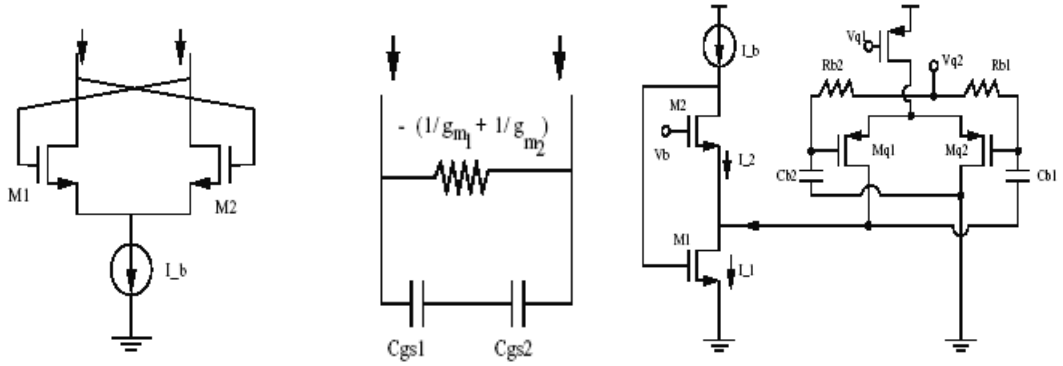


Fig. 4.7 Differential/Single–Ended Cross Coupled Negative Resistance [3.44]

As it can be noticed from the previous chapter, some TOSI architectures make use of negative resistances to compensate the inductor losses, while others use cascode stages to increase the output resistance.

Considering that a current testing source (i_X) is connected between the drains of the cross–coupled transistors ($M_{1,2}$), the equivalent input impedance is obtained as follows:

$$\begin{cases}(g_{o1}+sC_2)v_X = g_{m1}v_X + i_X \\ -(g_{o2}+sC_1)v_X = -g_{m2}v_X - i_X\end{cases} \Leftrightarrow Z_{in} = \frac{v_X}{i_X} = \frac{2}{-(g_{m1}+g_{m2})+g_{o1}+g_{o2}+s(C_{gs1}+C_{gs2})} \tag{4.44}$$

Rewriting (4.44), the negative inverting behavior is obtained as follows:

$$Z_{in} = -\frac{2}{(g_{m1}+g_{m2})-[g_{o1}+g_{o2}+s(C_{gs1}+C_{gs2})]} \tag{4.45}$$

Taking into account that $g_{m1,2}>>g_{o1,2}$ and $g_{m1,2}>>\omega C_{gs1,2}$, this cross–coupled circuit has the following approximate input impedance:

$$Z_{in} = -\left.\frac{2}{g_{m1}+g_{m2}}\right|_{g_{m1}=g_{m1}=g_m} = -\frac{2}{g_m} \tag{4.46}$$

The negative resistance value set by transconductances values is affected by the finite values of r_{ds}. Regarding its frequency behavior, the negative resistance introduces a parasitic capacitance with a negative influence on the resonant frequency since it increases the parasitic capacitor of the simulated inductor.

The single ended version, presented in Fig. 4.7 – right contains supplementary AC short circuit capacitors $C_{b1,2}$ used to implement the negative resistance only in AC with the main drawback of an increased number of voltage sources. Since this negative resistance is directly connected to the TOSI structure, the self resonant frequency is very sensitive to any current change through the negative resistance. Therefore, the quality factor must be tuned carefully due to the higher risk of instability. In other words, beside to the intrinsic frequency deviation created during the negative resistance tuning, a supplementary frequency deviation, much stronger than the first, is caused by the current sharing. This phenomenon is described by (4.47):

$$\begin{cases}\omega_0 = f_1(g_{m1}, g_{m2}, G_{neg}) \\ Q = f_2(g_{m1}, g_{m2}, G_{neg}) \\ g_{m1,2} = f_3(G_{neg})\end{cases} \tag{4.47}$$

A solution has been proposed to reduce this frequency deviation. The proposed principle [4.6] consists of two improvement steps:

1. DC decoupled negative resistances are used therefore the negative resistance influence on the active inductor being minimized.

Simulations carried out for this architecture (with decoupled negative resistances) in both 0.18µm UMC process and 0.35µm AMS technology, showed frequency deviations of tens MHz, dependent on the centre frequency value chosen in GHz range. The problem of frequency deviation is illustrated in the following figures for the ideal case. In the first case (Fig. 4.8), a self resonant frequency of 2.545 GHz is obtained with a very high quality factor and small TOSI current consumption (only 10 µA). While tuning the quality factor, through a suitable change of the negative resistance (from –3.559 kΩ to –3 kΩ), the self resonant frequency decreases to 2.515 GHz (Q=4.7). In other words, a frequency deviation of 30 MHz is obtained which is almost half of the Bluetooth bandwidth.

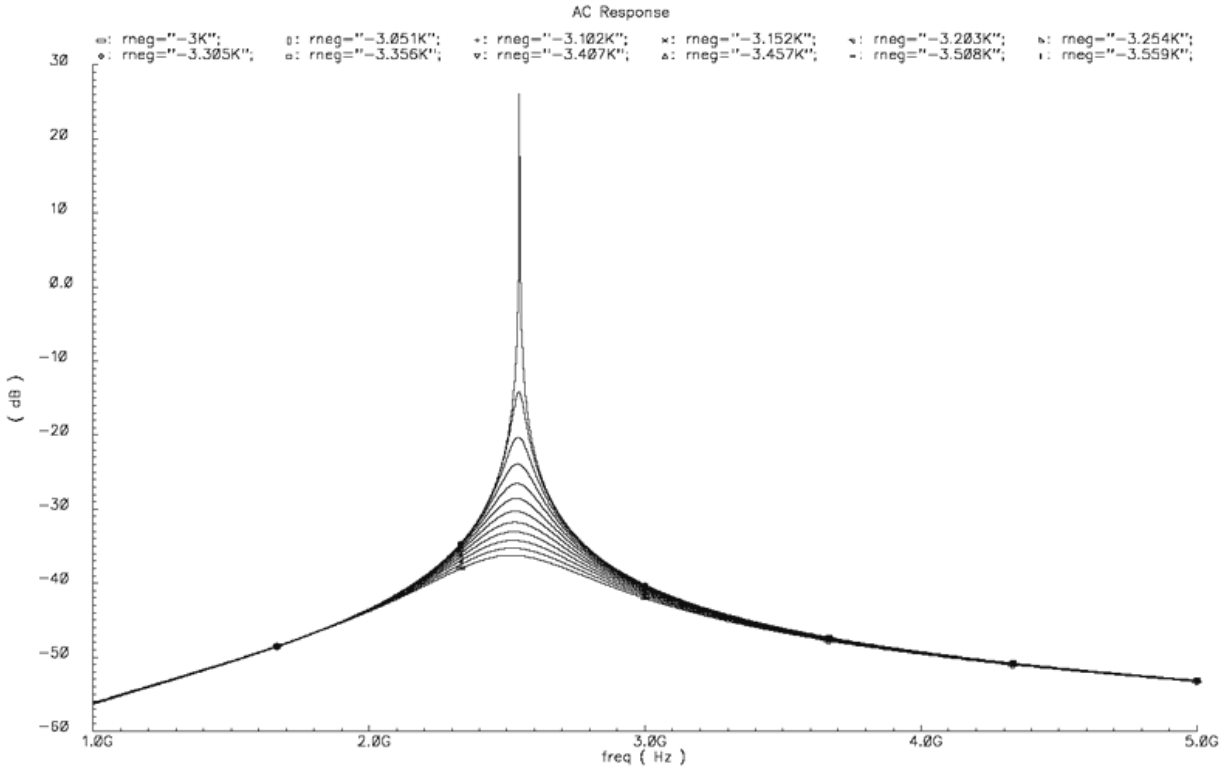


Fig. 4.8 Q–tuning using decoupled negative resistance (Δf=30 MHz)

In the second case (Fig. 4.9), a centre frequency of 5.476 GHz is obtained with a very high quality factor and small TOSI current consumption (only 30 µA). While tuning the quality factor, through a suitable change of the negative resistance (from –1.477 kΩ to –1.245 kΩ), the self resonant frequency decreases to 5.403 GHz while keeping the same quality factor. In other words, a frequency deviation of 73 MHz is obtained which is more

than 2/3 of the WLAN (IEEE 802.11a) bandwidth. The transistor sizing is 6u/0.18u for M_1 and 5u/0.18u for M_2 for both situations, V_b being 0.8V and 0.9V respectively.

It is important to note that as the simulated inductor is designed for higher frequencies, a much smaller negative resistance is required to compensate the intrinsic inductor losses. This constitutes also the main drawback of the TOSI architectures since low negative resistance signifies in fact large transconductances and therefore large current consumption. In other words, the very small current consumption required by the active inductor is compensated by a corresponding higher current consumption at the negative resistance level.

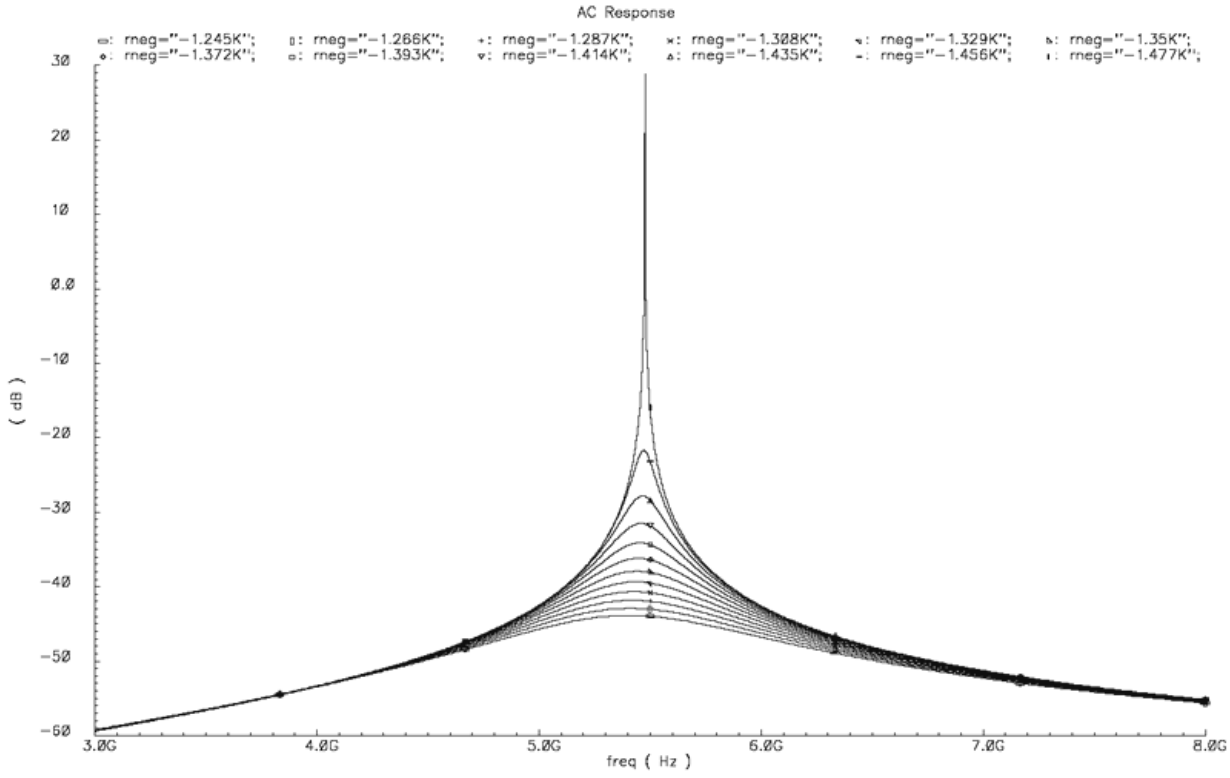


Fig. 4.9 Q–tuning using decoupled negative resistance (Δf=73 MHz)

If such active inductor is used in a multistandard transceiver and has frequency deviations of tens MHz from the centre frequency, with more significant errors when several cells are connected in series, the circuit (filter) becomes useless. This fact imposes further improvements of the tuning principle. The importance of designing filters with independent tuning facility is based on the assumption that a reconfigurable multi–standard transceiver switches the center frequency with an imposed quality factor to other centre frequencies characterized by particular quality factors (as regulated by different telecommunications standards). An independent frequency and quality factor tuning

makes the automatic control loop useless otherwise iterative steps must be followed in order to bias the TOSI in such manner that a particular Q is achieved at one frequency.

By decoupling the negative resistance, the design constraints are much relaxed since no limitations are imposed to transistor size or biasing currents/voltages. The decoupled negative resistance proposed for single–ended implementations is shown in Fig. 4.10a). This negative resistance is simulated by the ac cross–coupled transistors M_1 and M_2, two off transistors $M_{3,4}$ used for a fine quality factor tuning (as proposed in [3.44]) and a supplementary transistor M_5 used to close the DC path to the ground. It is apparent that the negative resistance is seen into the drain of M_5.

2. The principle makes use of a supplementary DC decoupled negative resistance connected to the second node. The proposed TOSI architecture which allows independent frequency and quality factor tuning is shown in Fig. 4.10b).

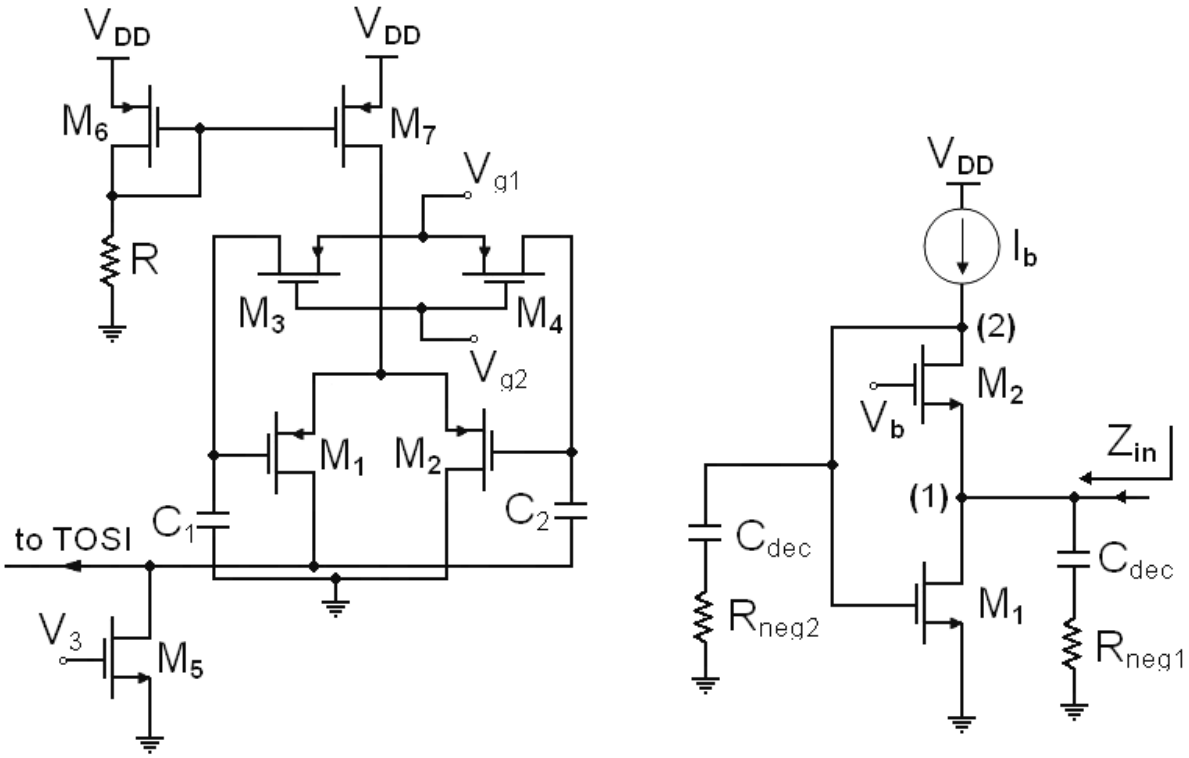


Fig. 4.10 a) DC decoupled negative resistance for b) single–ended TOSI with independent f and Q control [4.6]

From the very beginning it is necessary to specify that this principle of frequency and quality factor independent tuning is intended to make easier the TOSI design (f_0 and Q imposed by specs) and the tuning process while switching to another telecommunications standard. Consequently, it is not proposed for implementing automatic control loops used

in master–slave structures to avoid the frequency or quality factor sensitivity to the supply voltage, biasing currents or temperature.

Considering the circuit proposed in Fig. 4.10b), the frequency behavior is described by the following system:

$$\begin{cases}(g_{o1}+g_{o2}-G_1+sC_{gs2})v_{(1)}-g_{o2}v_{(2)}=J_{in}-g_{m1}v_{(2)}-g_{m2}v_{(1)}\\ -g_{o2}v_{(1)}+(g_{o2}-G_2+sC_{gs1})v_{(2)}=g_{m2}v_{(1)}\end{cases} \tag{5.48}$$

The input impedance is given by:

$$\begin{cases}Z_{in}=\dfrac{b_1 s+b_o}{s^2+2\alpha s+\omega_o^2}\\ b_1=\dfrac{1}{C_{gs2}};\quad b_0=\dfrac{g_{o2}-G_2}{C_{gs1}C_{gs2}}\\ 2\alpha=\dfrac{C_{gs1}g_{o1}+C_{gs1}g_{o2}+C_{gs1}g_{m2}+g_{o2}C_{gs2}-C_{gs1}G_1-C_{gs2}G_2}{C_{gs1}C_{gs2}}\\ \omega_o^2=\dfrac{g_{m1}g_{m2}+g_{m1}g_{o2}+g_{o1}g_{o2}-G_1g_{o2}-G_2(g_{m2}+g_{o1}+g_{o2})+G_1G_2}{C_{gs1}C_{gs2}}\end{cases} \tag{4.49}$$

The idea behind this novel tuning principle was to avoid the influence of the negative resistance on both frequency and filter selectivity, thing that may be possible only when introducing a second identical supplementary negative resistance.

To explain the method, relations (4.49) are taken into consideration. First, it is obvious that both negative resistances influence the centre frequency and selectivity ($-G_1$ and $-G_2$). Now it is clear that no independent tuning may be achieved. However, establishing suitable values for one negative resistance, an independent frequency and quality factor tuning may be obtained while tuning the second negative resistance. This becomes clearer if the terms containing G_1 and G_2 from the frequency expression are chosen for being studied separately (4.50), a factor K being associated to them:

$$K=G_1G_2-G_1g_{o2}-G_2(g_{m2}+g_{o1}+g_{o2}) \tag{4.50}$$

From (4.50) it is apparent that two methods are possible, depending on which negative resistance has a fixed value.

a) If the negative resistance R_{neg1} is chosen to be fixed (4.51), the method is denoted as ‘left’ tuning:

$$\begin{cases} G_1 = g_{m2} + g_{o1} + g_{o2} \\ K = -g_{o2}(g_{m2} + g_{o1} + g_{o2}) \\ \omega_o^2 = f(G_1) = \dfrac{g_{m1}g_{m2} + g_{m1}g_{o2} - g_{m2}g_{o2} - g_{o2}^2}{C_{gs1}C_{gs2}}, \quad G_1 = ct. \\ 2\alpha = \dfrac{C_{gs2}(g_{o2} - G_2)}{C_{gs1}C_{gs2}} = \dfrac{g_{o2} - G_2}{C_{gs1}} \quad \Rightarrow \quad Q = f(G_2), \quad G_2 = \forall \end{cases} \tag{4.51}$$

In this case, ω_0 is a function of G_1 only and is kept constant. The quality factor Q is tuned with a suitable change of G_2. The frequency results obtained for this principle [4.6] are presented in Fig. 4.11.

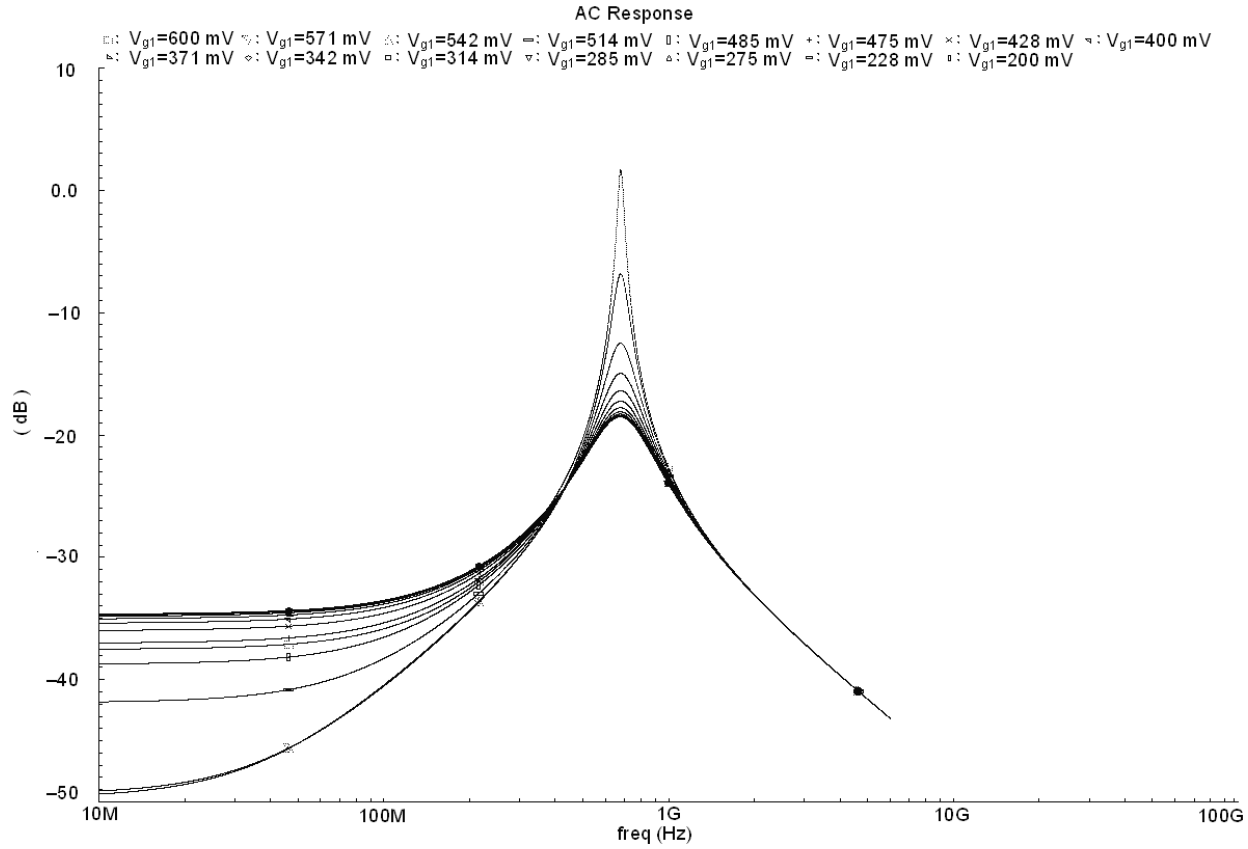


Fig. 4.11 Independent tuning principle with 'left' tuning (f_0=682 MHz) [4.6]

b) If the negative resistance R_{neg2} is chosen to be fixed (4.52), the method is denoted as 'right' tuning:

$$\begin{cases} G_2 = g_{o2} \\ K = -g_{o2}(g_{m2} + g_{o1} + g_{o2}) = ct. \\ \omega_o^2 = f(G_2) = \dfrac{g_{m1}g_{m2} + g_{m1}g_{o2} - g_{m2}g_{o2} - g_{o2}^2}{C_{gs1}C_{gs2}}, \quad G_2 = ct. \\ 2\alpha = \dfrac{g_{m2} + g_{o1} + g_{o2} - G_1}{C_{gs2}} \quad \Rightarrow \quad Q = f(G_1), \quad G_1 = \forall \end{cases} \tag{4.52}$$

In this case, ω_0 is a function of G_2 only and is kept constant. The quality factor Q is tuned with a suitable change of G_1. The frequency results obtained for this case are presented in Fig. 4.12, where the voltage control V_{g1} of the negative resistance was tuned between 0.1V and 0.3V.

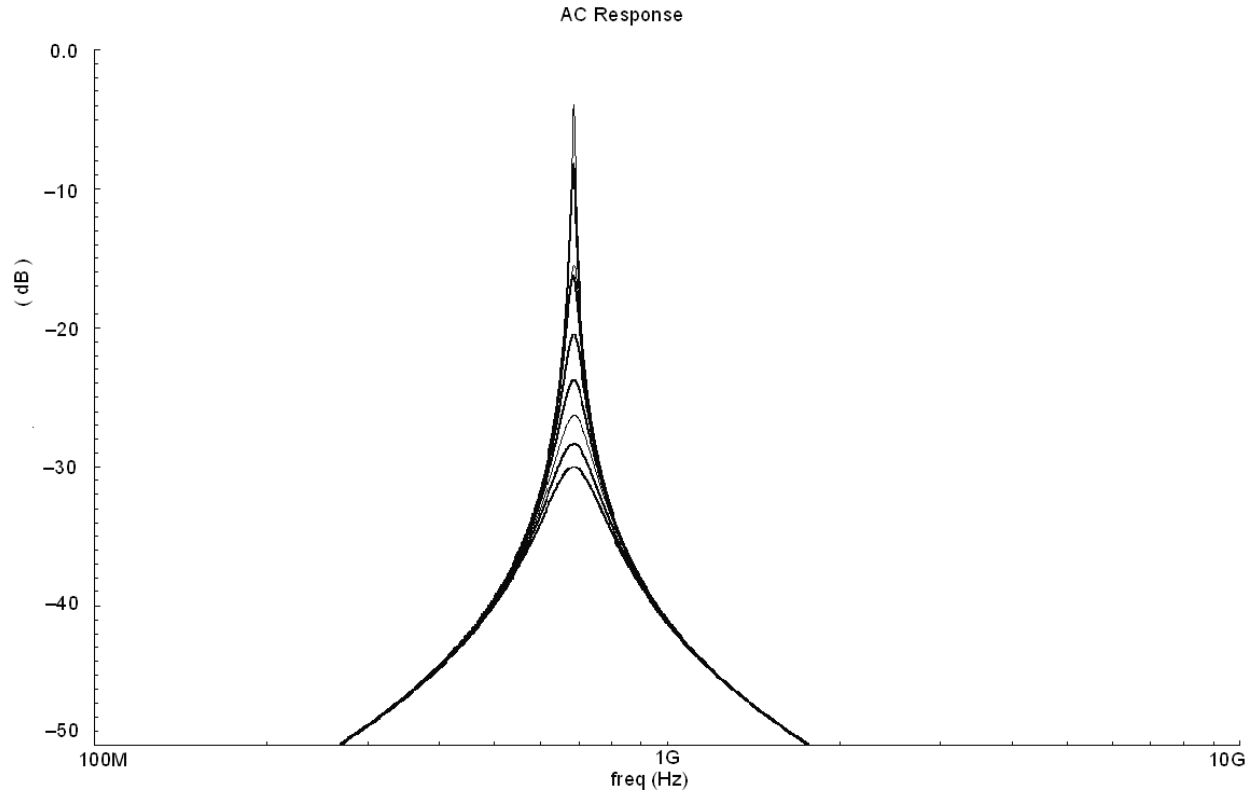


Fig. 4.12 Independent tuning principle with 'right' tuning (f_0=691 MHz) [4.6]

Two interesting things are noticed regarding this principle of independent tuning:

1) No matter which negative resistance is kept constant, the centre frequency has the same value. This means that the frequency is not sensitive to the tuning method constituting an advantage of this principle.

2) The symmetry of this approach can be noticed. Indeed, the value set for a negative resistance in order to keep the frequency constant when using one tuning scheme is the value required for the same resistance to increase the quality factor when using the second tuning scheme.

The effect of the transistor parasitics in the case of the negative resistances was studied in [4.7] where the principle was studied at a higher frequency (f_0=1.54 GHz). This method, applied to a single–ended topology, was reported also in [4.8] and [4.9] respectively.

Nowadays, most RF blocks (LNA, mixer, VCO, PA) used in “zero” IF transceivers are implemented in differential configurations. Used mainly for common mode rejection, differential architectures require more components than single ended topologies while the layout area is theoretically doubled. Other drawbacks are higher power consumption and increased noise [4.10]. A supplementary balun is required for differential circuits in order to convert the signals from single ended to differential thus increasing the chip area. However, differential circuits have better performances regarding the nonlinearity since the even order harmonics are cancelled together with the DC offset. This is also the main reason of using differential RF blocks and consequently, all research focused on TOSI envisaged differential circuits even if ideal differential circuits do not exist in practical implementations and therefore DC offset and second order distortions still exist.

Before presenting further results obtained during the research, several considerations on the decoupling capacitors are presented. Thus, as emphasized in [4.10], ‘zero’ and DC blocking capacitors can be used to decouple a particular circuit and do not attenuate the signal. The “zero” capacitors connect a circuit terminal to the ground in AC therefore leaving unchanged the applied DC voltage. Their value must be chosen in such manner that the impedance approaches infinity at the frequency of interest. The DC blocking capacitors are connected in series with an input/output terminal in order to block the DC voltages while bypassing the AC signal. The impedance of blocking capacitor approaches zero (usually <2 Ω) at the frequency of interest (in AC) – like a short, therefore having very large capacitance values (even tens to hundred pF).

Considering that the simulated inductor has the loading resistance R_L and the blocking/decoupling capacitor C, to reject the DC offset it is necessary that $T>>R_LC$, where T is the period of the input signal. This corresponds to the case when the capacitor charges and discharges faster than the signal period, thus being able to follow the variation of the input (source) signal. A good approximation is $T=10R_LC_{max}$. As it can be noticed in Table 9, even tens of fF are required when load resistances of kΩ values are used in GHz domain.

Although these results are valid for any RF circuit, this is not the case for TOSI implementations which make use of negative resistances. In this case, the circuit becomes easily unstable if the decoupling capacitor is not properly chosen. Thus, figures 4.13 and 4.14 showed that minimum decoupling capacitors of 1 pF correspond to the

usual values of the negative resistance. Identical results were obtained with the both real and ideal negative resistances.

Table 9 Maximum values of the DC blocking capacitors (pF)

f [MHz]	$\mathbf{R_L}$ =0.7 kΩ	$\mathbf{R_L}$ =1 kΩ	$\mathbf{R_L}$ =1.5 kΩ	$\mathbf{R_L}$ =2 kΩ	$\mathbf{R_L}$ =2.5 kΩ	$\mathbf{R_L}$ =3 kΩ
700	0.207	0.142	0.095	0.071	0.057	0.047
900	0.158	0.111	0.074	0.055	0.044	0.037
1300	0.109	0.077	0.051	0.038	0.030	0.025
1600	0.089	0.062	0.041	0.031	0.025	0.017
1800	0.079	0.055	0.037	0.027	0.022	0.016
2100	0.068	0.047	0.031	0.023	0.019	0.013
2400	0.059	0.041	0.027	0.021	0.166	0.011
3500	0.040	0.028	0.019	0.014	0.011	0.008
5000	0.028	0.02	0.013	0.010	0.008	0.006

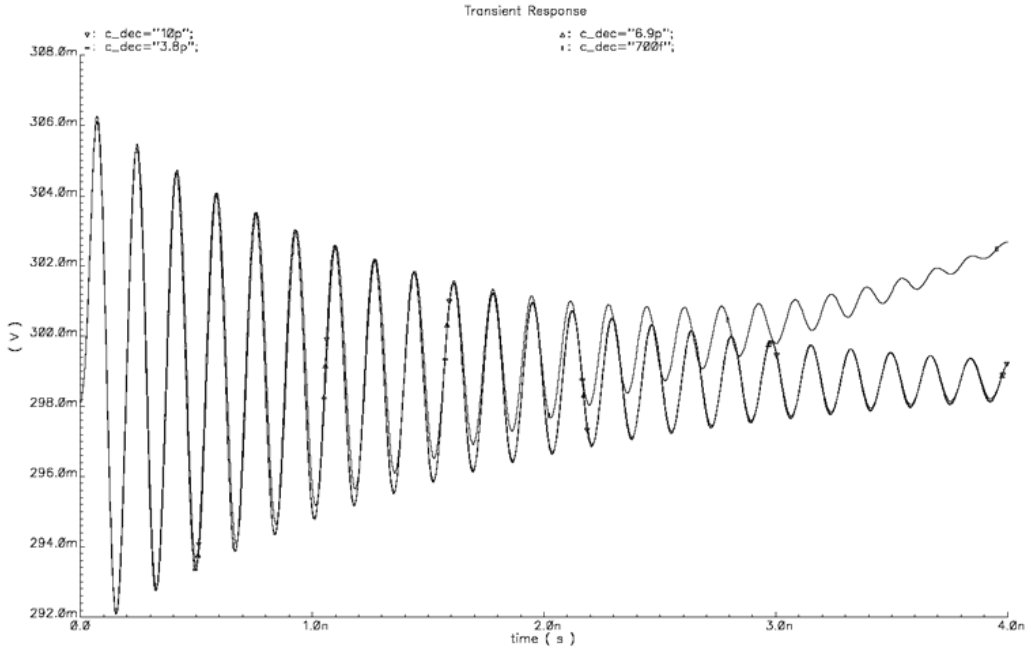


Fig. 4.13 TOSI output transient response before the decoupling capacitor

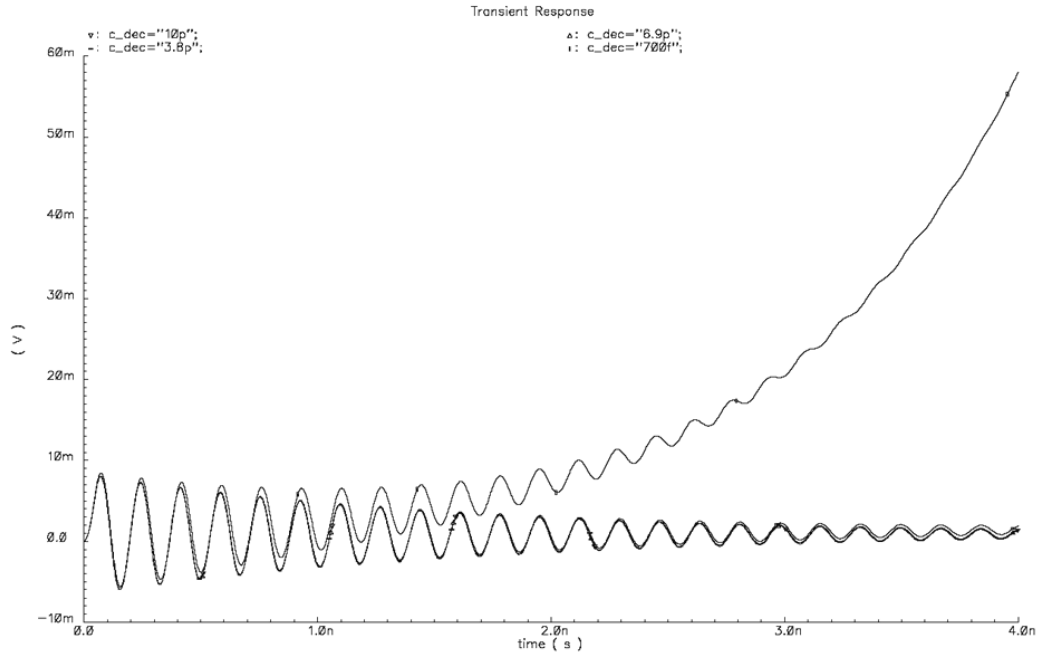


Fig. 4.14 TOSI output transient response on the negative resistance

However, the research focused mainly on differential configurations, a first one being presented in Fig. 4.15 [4.11]. The negative resistance is shown in Fig. 4.16a) together with the gate resistance R_{gate} (Fig. 4.16b).

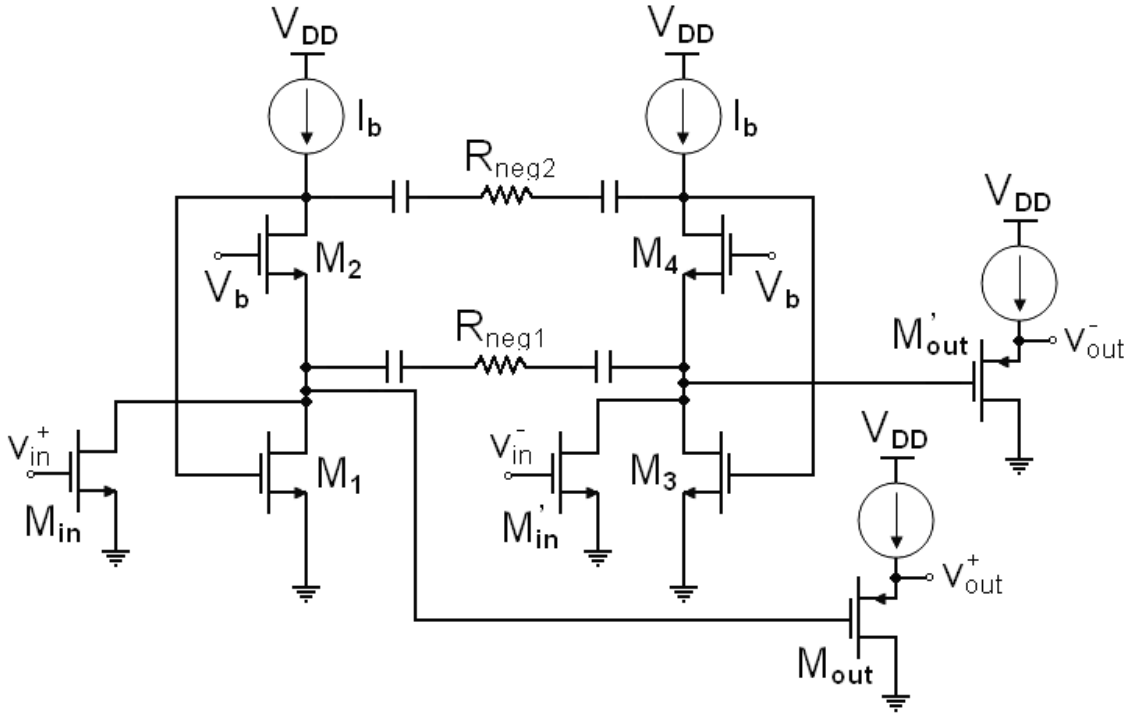


Fig. 4.15 Differential TOSI with independent tuning possibility [4.10]

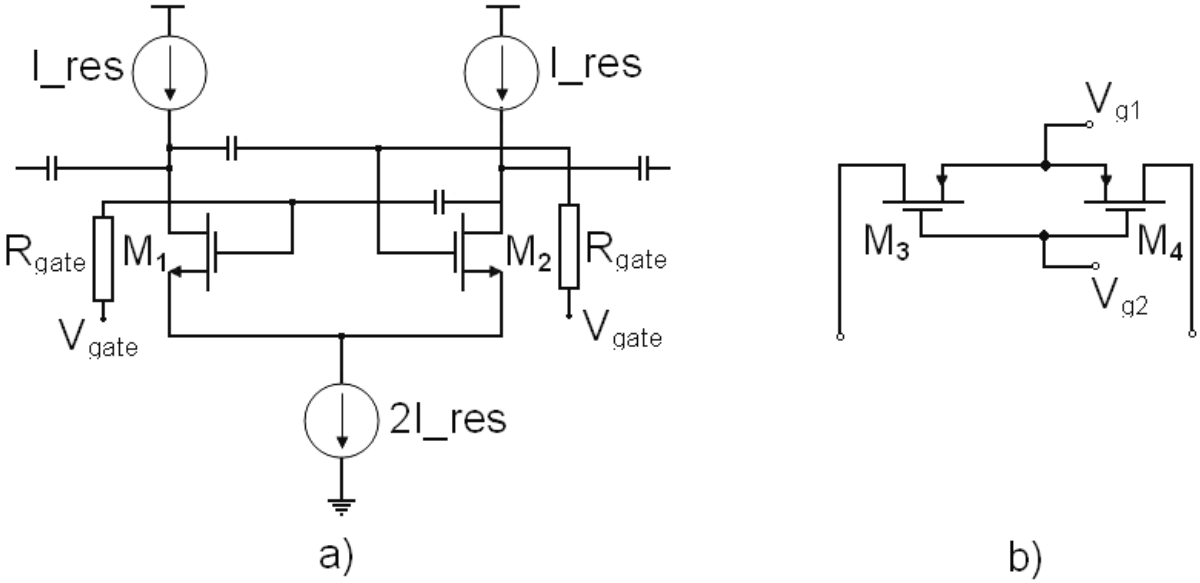


Fig. 4.16 Proposed DC decoupled differential negative resistance [4.10]

For this topology, the filter makes use of two buffers (M_{in}, M_{in}') in common source configuration (CS) to convert the input voltage signal to current signal. Their transconductance value must be as large as possible to avoid any loss of the input signal power but also for a plus of linearity and smaller noise factor. Other two p–MOS common drain (CD) transistors are used as output buffers since this configuration offers better linearity and noise performances compared to other biasing schemes. As in the case of input buffers, their transconductances must be as large as possible.

In practical applications, the entire circuit must be matched on 50Ω or 25Ω at both inputs and outputs, for single ended or differential configurations. The use of CS buffers makes more difficult this matching. Thus, two possible matching solutions may be implemented for CS buffers:

1. Passive matching networks may be used, as in the LNAa case, with the main drawback that these networks, being based on the resonant method, are matched at a single frequency. Therefore, switched matching networks must be used increasing in this way the chip area.

2. A simpler way to match the filter is to connect a shunt resistance (R_g) to the gate of the input buffers, with the required values (25/50 Ω). Therefore, the input impedance has the value:

$$Z_{in} = \frac{1}{\frac{1}{R_g} + j\omega C_{gs}} \tag{4.53}$$

It is obvious that the input buffer may affect the matching only in the cases when the input transistor has large sizes. Two examples are further presented, 20 fF and 200 fF being chosen as possible values for C_{gs}:

$$Z_{in} = \frac{1}{\frac{1}{50} + j \cdot 6.28 \cdot 10^{9} \cdot 20 \cdot 10^{-15}} \Omega = \frac{1}{2 \cdot 10^{-2} + j \cdot 125 \cdot 10^{-6}} \Omega$$

$$Z_{in} = \frac{1}{\frac{1}{50} + j \cdot 6.28 \cdot 10^{9} \cdot 200 \cdot 10^{-15}} \Omega = \frac{1}{2 \cdot 10^{-2} + j \cdot 125 \cdot 10^{-5}} \Omega$$

As it can be noticed even an input parasitic capacitance of 200 fF is not enough to "distort" the input impedance, the buffer being matched. However, supplementary noise is added due to the presence of this input resistance. If the filter is interconnected between two LNAs and the noise of the other stages is minimized, this matching method may be used as well. This is the reason why, the design of a TOSI based filter for GHz domain is not a simple task. Supplementary knowledge in the LNA design represents an advantage when dealing with simulated inductors.

The matching for the output buffer is not a problem since CD stages offer small impedance values in their source. If the transistor is careful designed for minimum noise and good linearity while satisfying the relation $Z_{out}=1/g_m=50\ \Omega$, the filter is output matched as well.

The negative resistance seen between the transistor drains is:

$$R_{in} = -\frac{1}{g_m - \frac{1}{R_{gate}}} \tag{4.54}$$

By tuning the gate voltage V_{gate}, a very fine quality factor tuning may be implemented. However, greater sensitivity to the temperature is expected for this circuit due to the presence of these off transistors, used to implement the negative resistance. The main drawback when using decoupled negative resistances is an increased chip area due to the use of decoupling capacitors.

Two advantages are possessed by differential configurations over the single ended ones. The first refers to the chip area occupied by the negative resistance which is efficiently used in differential case. For single ended configuration, one transistor used to implement the cross–coupled configuration and consequently the negative resistance is grounded. Therefore, the inverting effect is not exploited on this side for single–ended while for differential case the inverting effect is used for both transistors. The second plus

refers to the negative resistance value required for compensation which is twice the value used for single ended topologies. This improves the current consumption (halved) but also the chip area. Practically speaking, the negative resistance must be as high as possible so that the chip area and power consumption are minimized.

The independent tuning principle has been tested at two frequencies: 1.67 GHz (Fig. 4.17) and 2.42 GHz (Fig. 4.18). The transient response of this circuit at 2.4 GHz is shown in Fig. 4.19, being obvious that the circuit is stable.

The current consumption is about 0.5 mA at 2.4 GHz from a 1.8V supply voltage from which only 0.1 mA represents the current consumed by the TOSI structure. This is not surprising since small negative resistances must be implemented (several kΩ), the same small values being required for DC coupled topologies, as previously reported in literature. The design of low negative resistances in CMOS technology still represents a challenge from this point of view. As in the previous cases, the simulations have been carried out in a 0.18μm CMOS process.

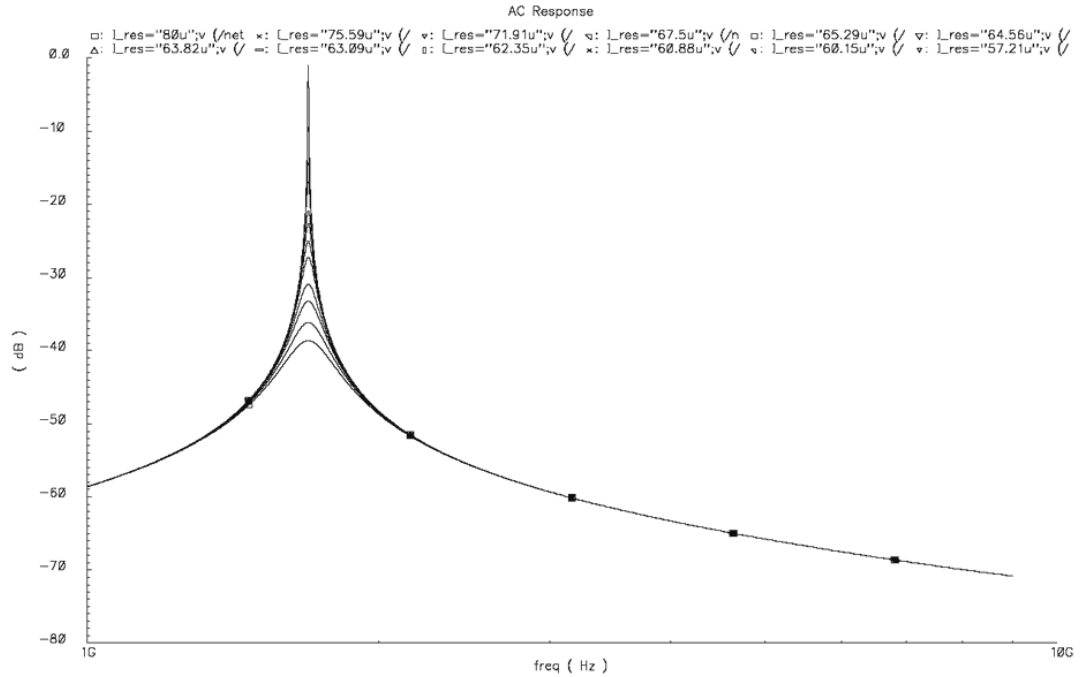


Fig. 4.17 Independent tuning principle implemented at f_0 = 1.67 GHz [4.11]

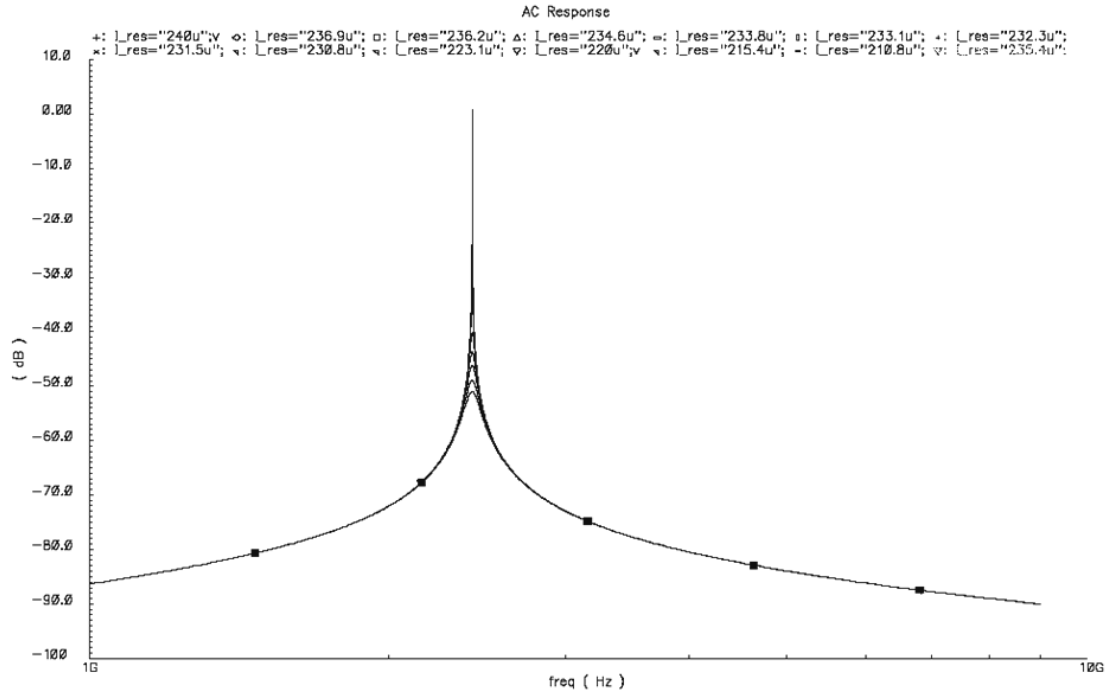


Fig. 4.18 Independent tuning principle implemented at f_0 = 2.42 GHz [4.11]

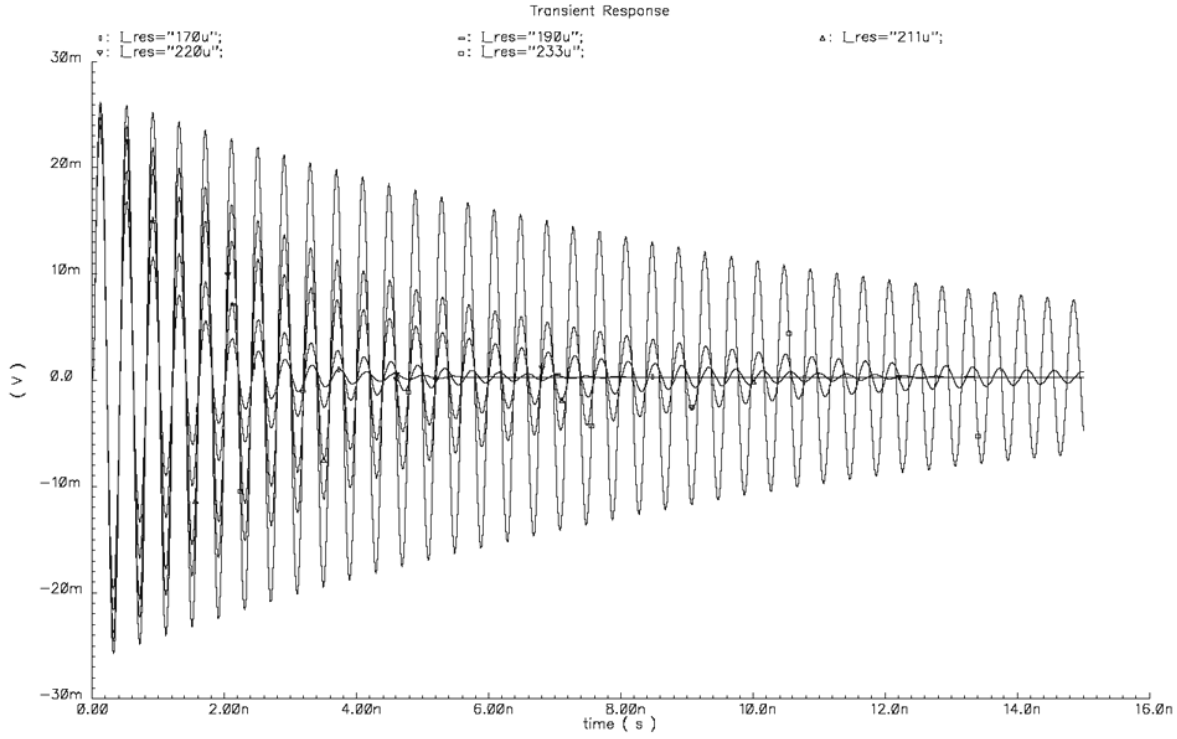


Fig. 4.19 Transient response when tuning the quality factor (f_0=2.42 GHz) [4.11]

The same circuit was designed at other two different RF frequencies (1.6 GHz and 2.6 GHz), the tuning scheme giving positive results, as stated in [4.12].

Regarding the performances of this principle, a deeper insight on the limitations of this principle may be obtained if the TOSI behavior in the ideal case is reviewed i.e.

$$\begin{cases} Q = \sqrt{\dfrac{g_{m2}C_{gs1}}{g_{m1}C_{gs2}}} \\ \omega_o^2 = \dfrac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}} \end{cases} \tag{4.55}$$

By studying these formulas, the frequency behavior of TOSI structure can be accurately described as it follows, where ↑ means 'increases' and → 'leads to':

$g_{m1}\uparrow \rightarrow$ *high* f_0*, low Q, low* r_S*, low* L_S

$g_{m2}\uparrow \rightarrow$ *high* f_0*, high Q, low* r_S*, low* L_S

$C_{gs1}\uparrow \rightarrow$ *low* f_0*. high Q*

$C_{gs2}\uparrow \rightarrow$ *low* f_0*. low Q*

From these relations it is apparent that high values are required for both g_{m1} and g_{m2} in order to obtain high self resonant frequency but to obtain a simultaneous high quality factor g_{m2} must be larger than g_{m1}. The second aspect refers to the capacitor values. Thus, the both capacitor values decrease the self resonant frequency but a higher Q value may be obtained only when C_{gs1} is much larger than C_{gs2}. When using the principle of independent tuning, these comments are still valid when studying the relations:

$$\begin{cases} 2\alpha = \dfrac{g_{o2} - G_2}{C_{gs1}}, & \textit{left tuning} \\ 2\alpha = \dfrac{g_{m2} + g_{o1} + g_{o2} - G_1}{C_{gs2}}, & \textit{right tuning} \end{cases} \tag{4.56}$$

As expressed by (4.56), the principle of independent tuning is superior to the simple compensation scheme since a more relaxed designed is facilitated. Since the parasitic capacitors have a certain influence on the TOSI compensation, it remains to establish what tuning scheme may be implemented to obtain high quality factor values. To establish this, an accurate formula for quality factors is considered in the followings for both tuning schemes (4.57).

$$\begin{cases} Q_1 = \sqrt{\dfrac{C_{gs1}(g_{m1}g_{m2} + g_{m1}g_{o2} - g_{o1}g_{o2} - g_{o2}^2)}{C_{gs2}(g_{o2} - G_1)^2}} \\ Q_2 = \sqrt{\dfrac{C_{gs2}(g_{m1}g_{m2} + g_{m1}g_{o2} - g_{o1}g_{o2} - g_{o2}^2)}{C_{gs1}(g_{m2} + g_{o1} + g_{o2} - G_2)^2}} \end{cases} \tag{4.57}$$

Therefore, three cases of compensation exist, as presented in [4.13]:

a) $C_{gs1}=C_{gs2}$, in this case the tuning performances are identical for both 'right' and 'left' schemes;

b) $C_{gs1}>C_{gs2}$, in this case the 'right' tuning scheme offers best tuning performances, the circuit being stable while obtaining good quality factors; using the 'left' tuning in this case, the circuit passes into the instability region and low quality factor values are obtained;

c) $C_{gs2}>C_{gs1}$, in this case the 'left' tuning scheme offers best tuning performances, the highest quality factor is achieved and the circuit still remains stable while the 'left' scheme is useless.

A supplementary freedom degree may be obtained if the parasitic capacitors are tuned with varactors [4.14] as illustrated in Fig. 4.20. The filter has the same scheme with DC decoupled negative resistances as the previous one (Fig. 4.15) with the main improvement of using CMOS varactors. By introducing CMOS varactors in parallel to the transistor of interest, the quality factor may be changed with no penalty regarding the centre frequency since the principle of independent tuning is implemented. The same negative resistance architecture presented in Fig. 4.16 is used in this circuit. No supplementary problems are associated to CMOS varactors since this circuit does not work with time variant large voltages as VCOs do.

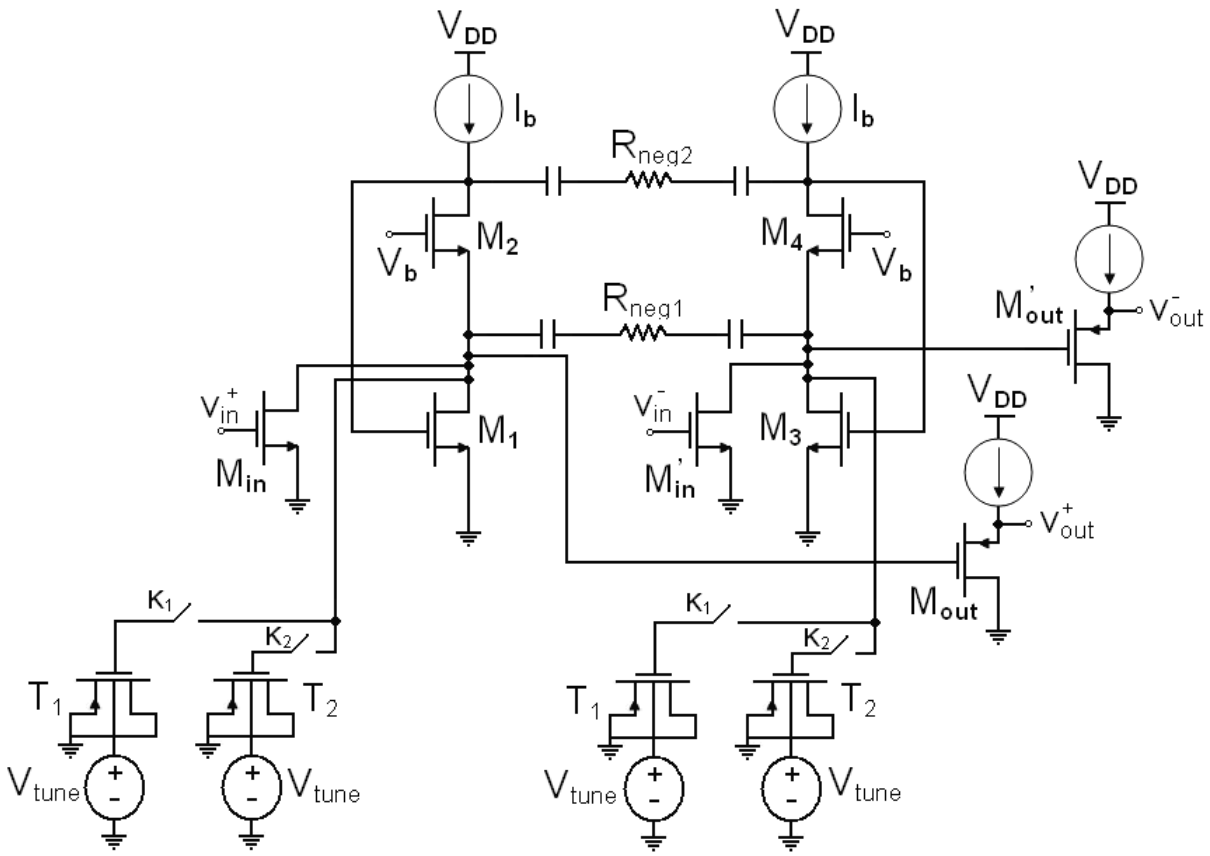


Fig. 4.20 Wide frequency tunable RF filter [4.14]

The circuit, designed in the same 0.18µm CMOS process as the previous circuits, was basically designed to have a centre frequency of 2.4 GHz where a total power consumption of 1 mW was obtained with 1.8 V supply voltage. At this frequency, the independent tuning principle was implemented, as proved by the simulation results in Fig. 4.21. Wide range quality factor values (6 to 2000) have been obtained with this architecture with no stability problem as shown in Figure 4.22. However, by continuously tuning the negative resistance the circuit can oscillate, in which case an oscillator is obtained.

By introducing the first varactors T_1 (3.5/1), a tuning of the centre frequency in the frequency range 1.77–1.99 GHz becomes possible (Fig. 4.23). As can be noticed in Fig. 4.24, the filter remains stable in the entire band.

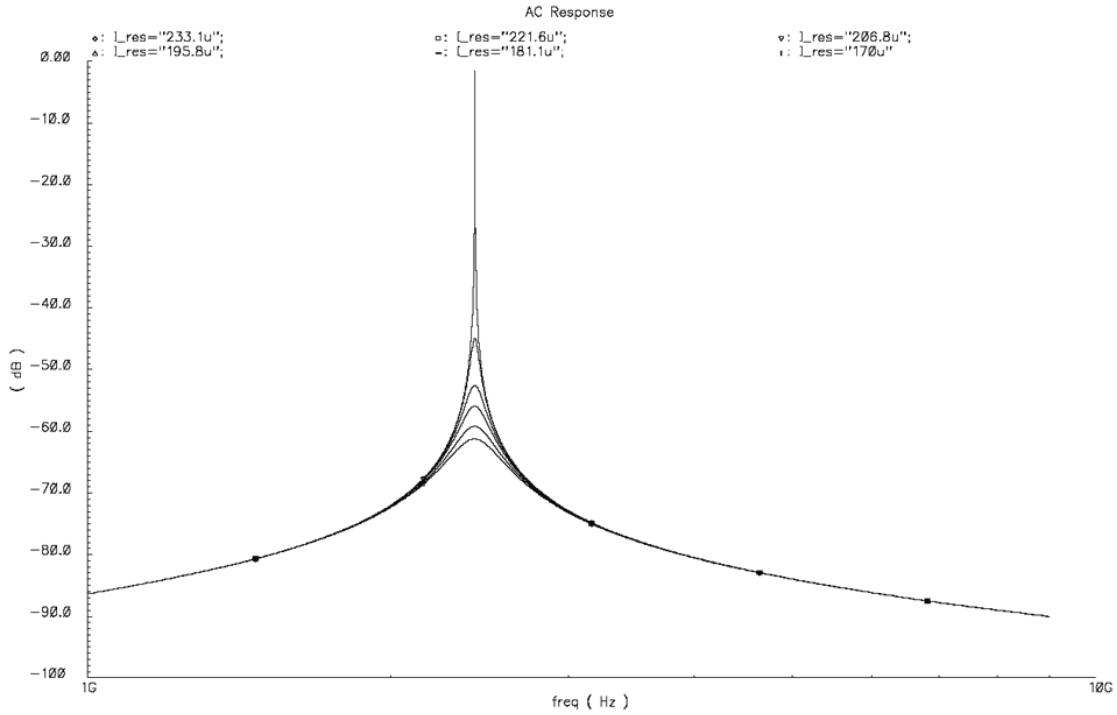


Fig. 4.21 Independent f_0 and Q tuning (f_0 = 2.42 GHz) without varactors [4.14]

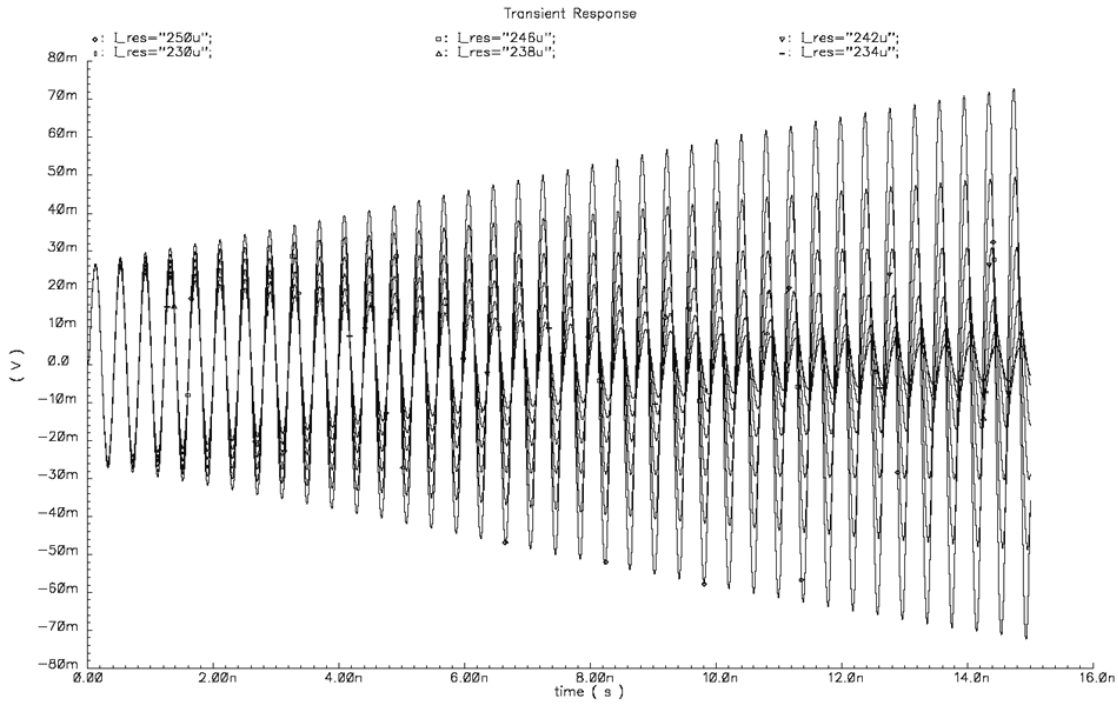


Fig. 4.22 Quality factor tuning and potential instability [4.14]

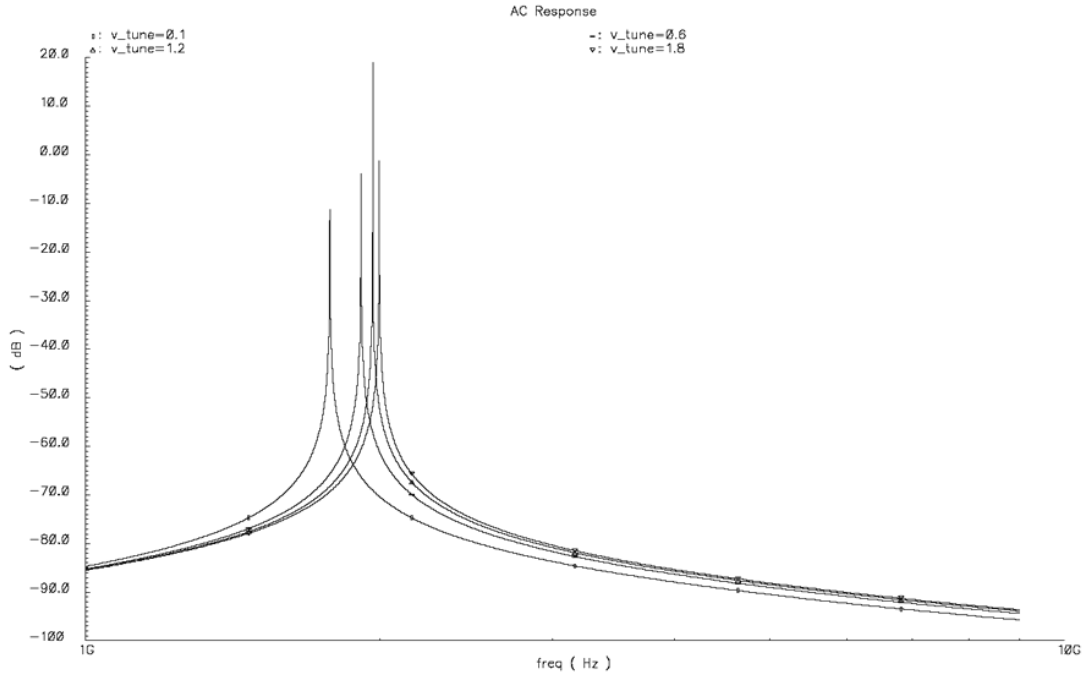


Fig. 4.23 Frequency tuning in the range 1.77–1.99 GHz [4.14]

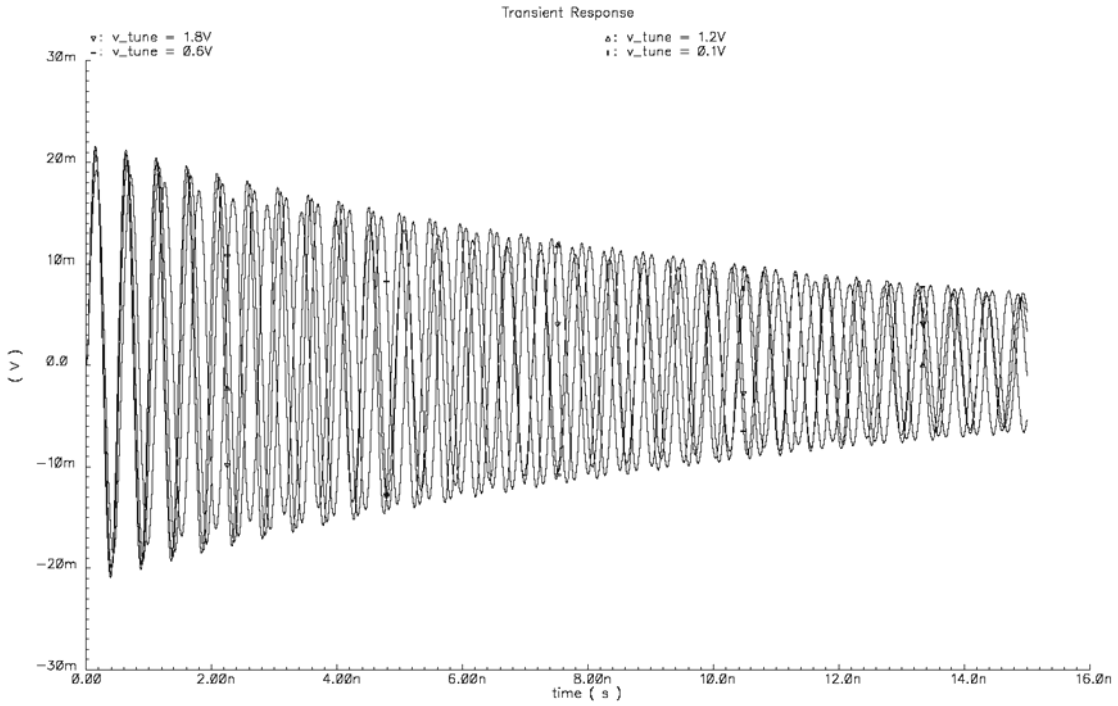


Fig. 4.24 Transient response proving stable operation (1.77–1.99 GHz) [4.14]

By introducing a second pair of varactors T_2 (6.5/6), the centre frequency is tuned in the frequency band 600–990 MHz (Fig. 4.25).

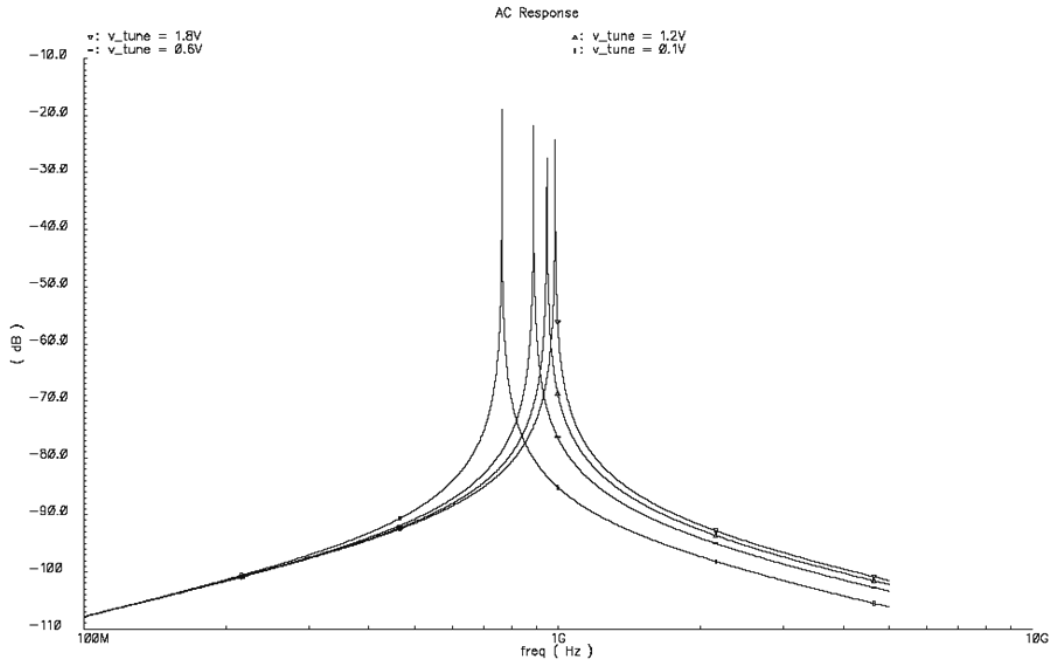


Fig. 4.25 Tuning possibility in the frequency band 600–990 MHz [4.14]

The varactors characteristics as functions of bulk–gate voltages are represented in Figure 4.26 and 4.27 where *vgate* represents the dc voltage of the input node.

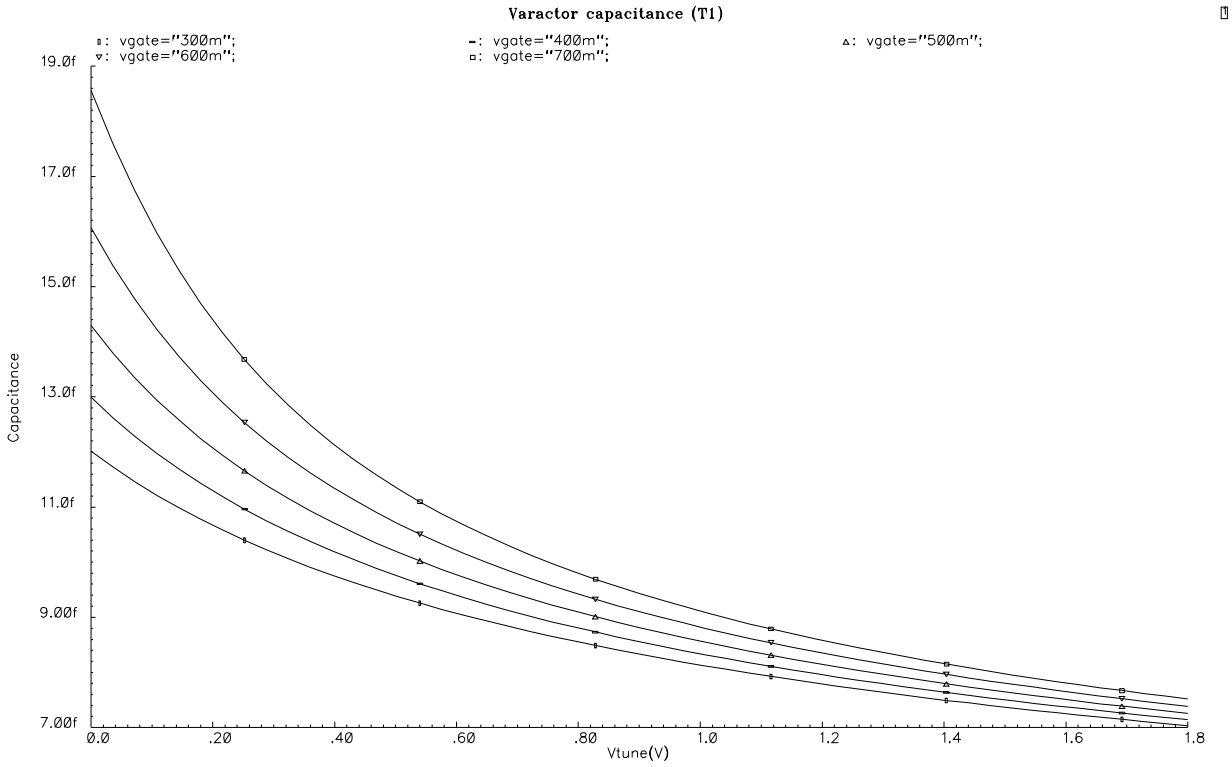


Fig. 4.26 T1 varactor characteristics

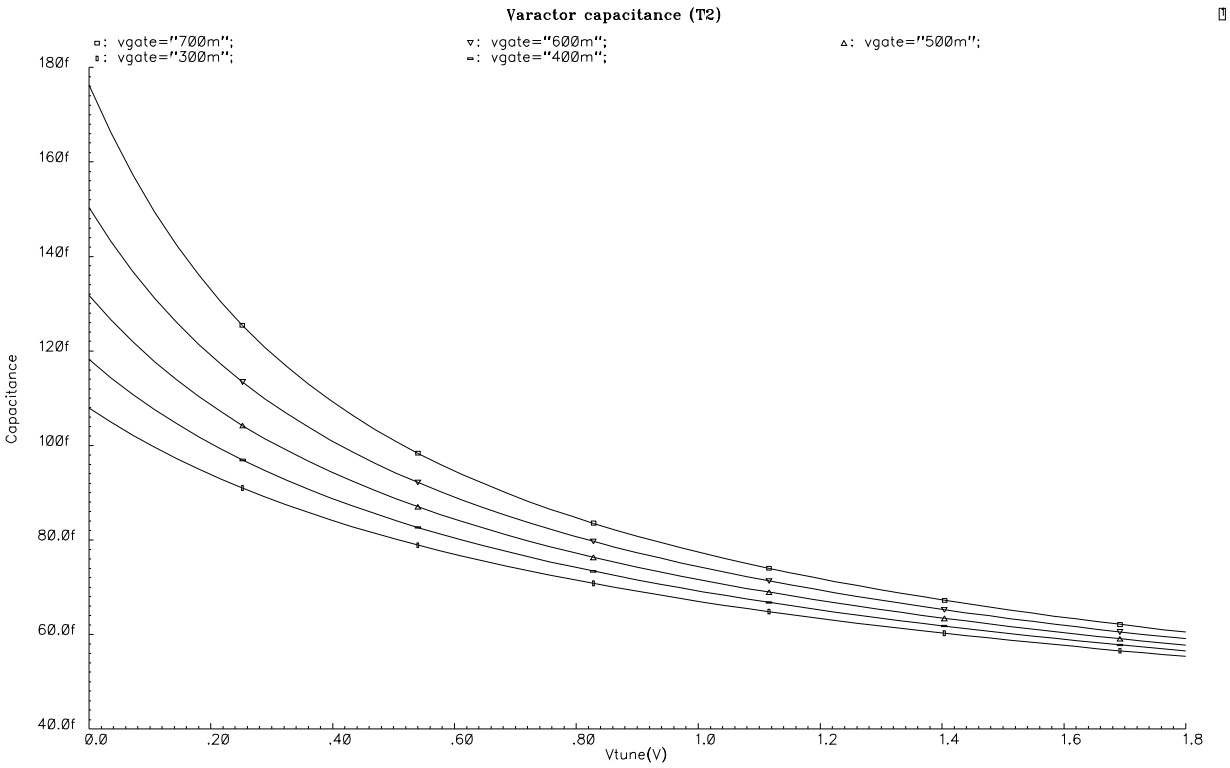


Fig. 4.27 T2 varactor characteristics

The independent tuning principle was proved for all these frequency bands. The advantage of using varactor is the low power consumption since no dc current is required for varactors. Regarding the negative resistances, always the same power consumption will be noticed when using this principle. The circuit has been reported also in [4.15] and a detailed analysis of the circuit was presented in [4.16].

Finally, it must be mentioned that this principle has an intrinsic limitation caused by the second order character of the transfer function. This can be easily understood from the poles expression for Z_{in}:

$$\begin{cases} Z_{in} = \dfrac{b_1 s + b_o}{s^2 + 2\alpha s + \omega_o^2} = \dfrac{b_1 s + b_o}{s^2 + \dfrac{\omega_0}{Q} s + \omega_o^2} \\ p_{1,2} = -\dfrac{\omega_0}{2Q} \pm \dfrac{1}{2}\sqrt{(\dfrac{\omega_0}{Q})^2 - 4\omega_o^2} \end{cases} \tag{4.58}$$

It is obvious that both the quality factor and the self resonant frequency establish the poles values. This signifies that anytime when Q or ω_0 is changed, the poles are changed consequently and inherently the second one is changed too. When high quality factors

are obtained, the real part approaches to zero and in this case very small frequency deviations are obtained or in some cases the change is not noticeable. This is the reason why the frequency deviation is measured for two frequencies, corresponding to a very low quality factor and high value respectively. Simulations done in 0.35µm AMS CMOS process showed deviations of maximum 4 MHz in the GHz domain with the principle of independent tuning. In other words, this proposed principle cannot eliminate the intrinsic dependence between those two parameters but offers good frequency performances when compared to other previously reported methods.

4.4 Simulated Inductor with Improved Frequency Response

In this section, two improved TOSI structures, based on the same architecture proposed by Ismail and discussed in the previous section, are proposed.

4.4.1 Active Inductor with Supplementary Gate Resistance

Until now only the TOSI frequency behavior enhancement from the quality factor perspective has been discussed. Since the architectures proposed in the previous sections solved the problem of the frequency deviation when changing the filter selectivity (or the inductor quality factor), the scope of other research direction was to find an improved TOSI structures which have better frequency behavior. One improved topology was proposed in [4.17] and is presented in Fig. 4.28.

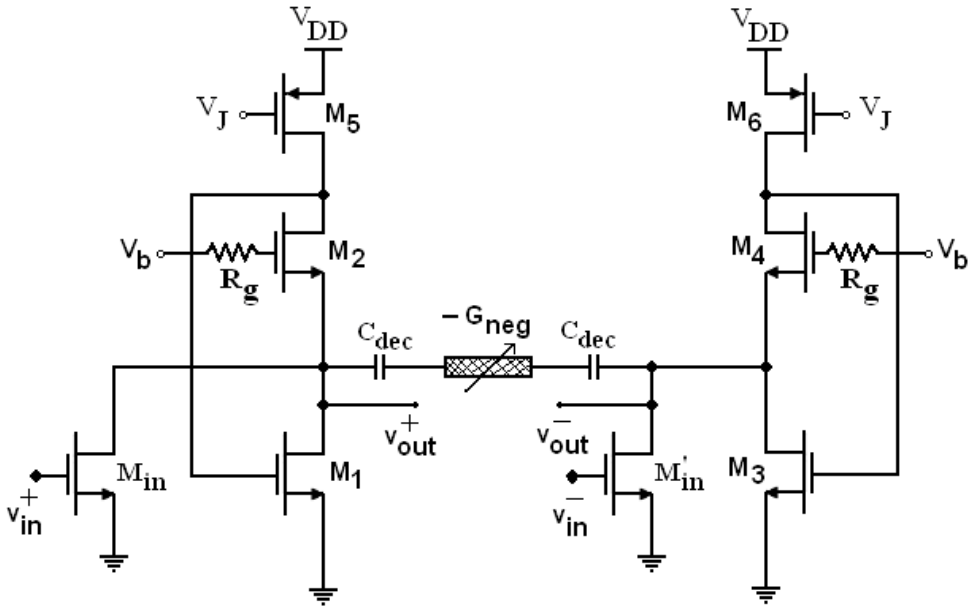


Fig. 4.28 Differential RF bandpass filter with frequency tuning enhancement [4.17]

The circuit, as the previous reported configurations, contains input buffers, output buffers (not shown in figure), improved TOSI and one decoupled negative resistance, identical to that presented above. The simulated inductor, implemented with transistors M_1–M_4, uses supplementary gate resistances R_g. This improved structure offers simultaneous good frequency response and quality factor.

The improved active inductor with supplementary gate resistance has a frequency response fully described by the following system (4.59), where node (3) is assigned to the gate of M_2 and (1) to the input one:

$$\begin{cases} (g_{o1}+g_{o2}+sC_{gs2})v_{(1)} - g_{o2}v_{(2)} - sC_{gs2}v_{(3)} = J_{in} + g_{m2}(v_{(3)}-v_{(1)}) - g_{m1}v_{(2)} \\ -g_{o2}v_{(1)} + (g_{o2}+sC_{gs1})v_{(2)} = -g_{m2}(v_{(3)}-v_{(1)}) \\ -sC_{gs2}v_{(1)} + (G_g+sC_{gs2})v_{(3)} = 0 \end{cases} \tag{4.59}$$

The input impedance has a more complicated expression as expressed by (4.60):

$$\begin{cases} Z_{in} = \dfrac{b_2 s^2 + b_1 s + b_o}{s^2 + 2\alpha s + \omega_o^2} \\ b_2 = \dfrac{1}{K_d}; \quad b_1 = \dfrac{C_{gs2}g_{o2} + C_{gs1}G_g}{K_d C_{gs1}C_{gs2}}; \quad b_0 = \dfrac{g_{o2}G_g}{K_d C_{gs1}C_{gs2}} \\ 2\alpha = \dfrac{K_1 C_{gs2} + K_2 G_g}{K_d C_{gs1}C_{gs2}} \\ \omega_o^2 = G_g \dfrac{g_{m1}g_{m2} + g_{m1}g_{o2} + g_{o1}g_{o2}}{K_d C_{gs1}C_{gs2}} \\ K_d = g_{o1} + g_{o2} + G_g; \quad K_1 = g_{o2}(g_{m1} + g_{o1}) \\ K_2 = C_{gs1}(g_{m2} + g_{o1} + g_{o2}) + C_{gs2}g_{o2} \end{cases} \tag{4.60}$$

As Eq. (4.60) show, the novel self resonant frequency decreased since $G_g/K_d<1$. In other words, no frequency enhancement may be obtained by using only this supplementary gate resistance. However, when a DC decoupled negative resistance is added to the TOSI structure, the novel relations are expressed by (4.61).

As can be seen noticed, a positive gate resistance and a negative one (represented by $-G_{neg}$) may have a positive effect on the frequency behavior in terms of self resonant frequency value. Thus, by introducing a negative resistance to the circuit, it changes also the term K_d which is reduced now, becoming K_d'. If the negative resistance has a value much larger than $(g_{o1}+g_{o2}+G_g)$ then $G_g/K_d'>1$ and the self resonant frequency is increased. This method has the advantage of low power consumption since for implementing a tuned gate resistance, a transistor is connected in parallel to R_g, its resistance value being simply controlled by the gate voltage. Therefore, only a

supplementary supply voltage is required. The simulation results are summarized in Table 10 while the waveforms are shown in Fig. 4.29–4.31 for ideal case and Fig. 4.32–4.33 for real case.

$$\begin{cases} Z_{in} = \dfrac{b_2 s^2 + b_1 s + b_o}{s^2 + 2\alpha s + \omega_o^2} \\ b_2 = \dfrac{1}{K_d^{'}}; \quad b_1 = \dfrac{C_{gs2} g_{o2} + C_{gs1} G_g}{K_d^{'} C_{gs1} C_{gs2}}; \quad b_0 = \dfrac{g_{o2} G_g}{K_d^{'} C_{gs1} C_{gs2}} \\ 2\alpha = \dfrac{K_1 C_{gs2} + K_2 G_g}{K_d^{'} C_{gs1} C_{gs2}} \\ \omega_o^2 = G_g \dfrac{g_{m1} g_{m2} + g_{m1} g_{o2} + g_{o1} g_{o2} - G_{neg} g_{o2}}{K_d^{'} C_{gs1} C_{gs2}} \\ K_d^{'} = g_{o1} + g_{o2} + G_g - G_{neg}; \quad K_1 = g_{o2}(g_{m1} + g_{o1} - G_{neg}) \\ K_2 = C_{gs1}(g_{m2} + g_{o1} + g_{o2} - G_{neg}) + C_{gs2} g_{o2} \end{cases} \tag{4.61}$$

Centre Frequency	Centre Frequency Increase	Gate Resistance Value
1.5 GHz	16.6 %	6.8 kΩ (ideal)
3.08 GHz	14.2 %	4.1 kΩ (ideal)
4.92 GHz	16.6 %	3.1 kΩ (ideal)
2.75 GHz	8 %	1.9 kΩ (real)
3.57 GHz	5.3%	1.7 kΩ (real)

Table 10 TOSI Frequency enhancement with gate resistance

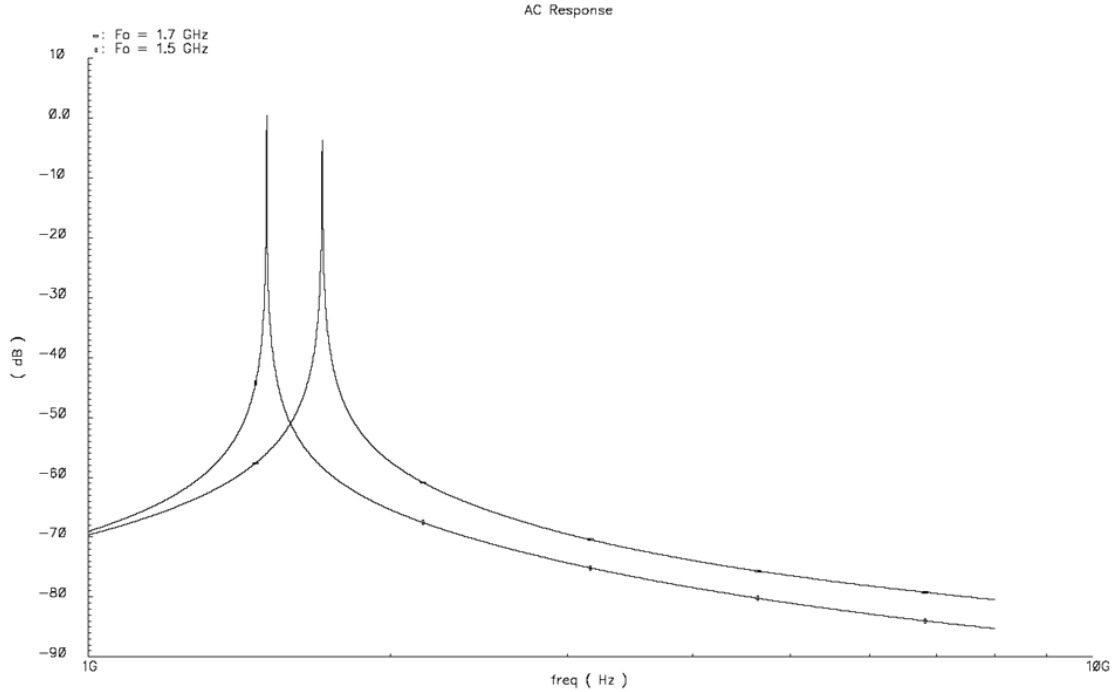


Fig. 4.29 Bandwidth increase with 200 MHz at 1.5 GHz (ideal case)

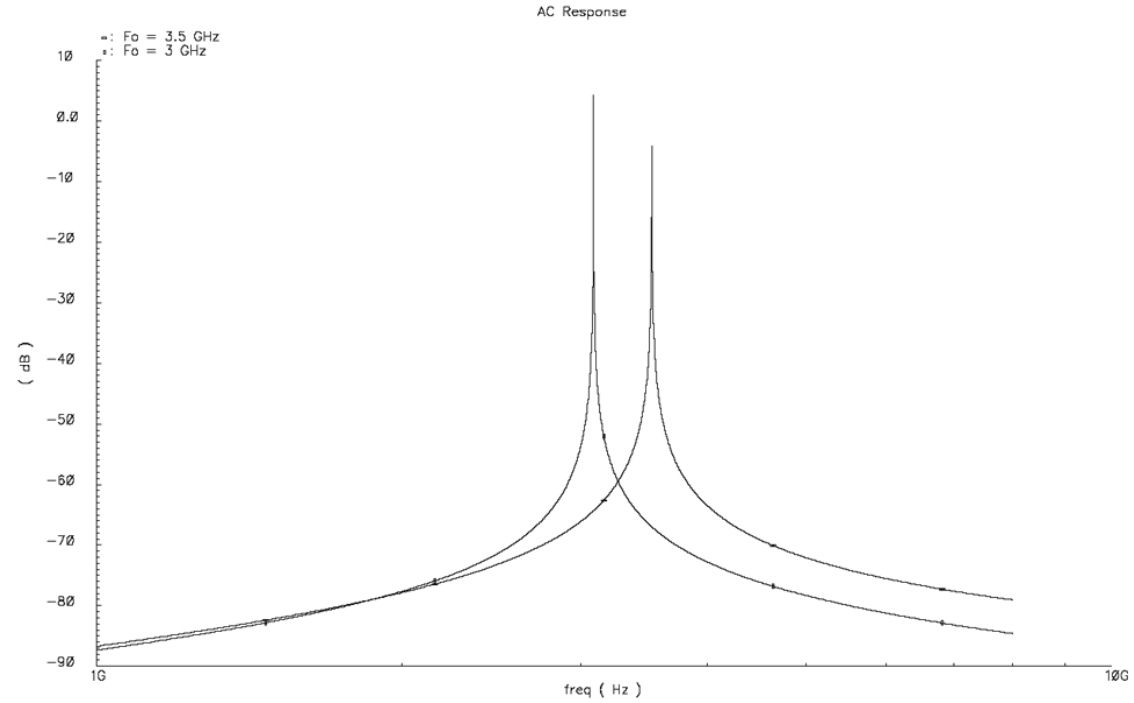


Fig. 4.30 Bandwidth increase with 500 MHz at 3 GHz (ideal case)

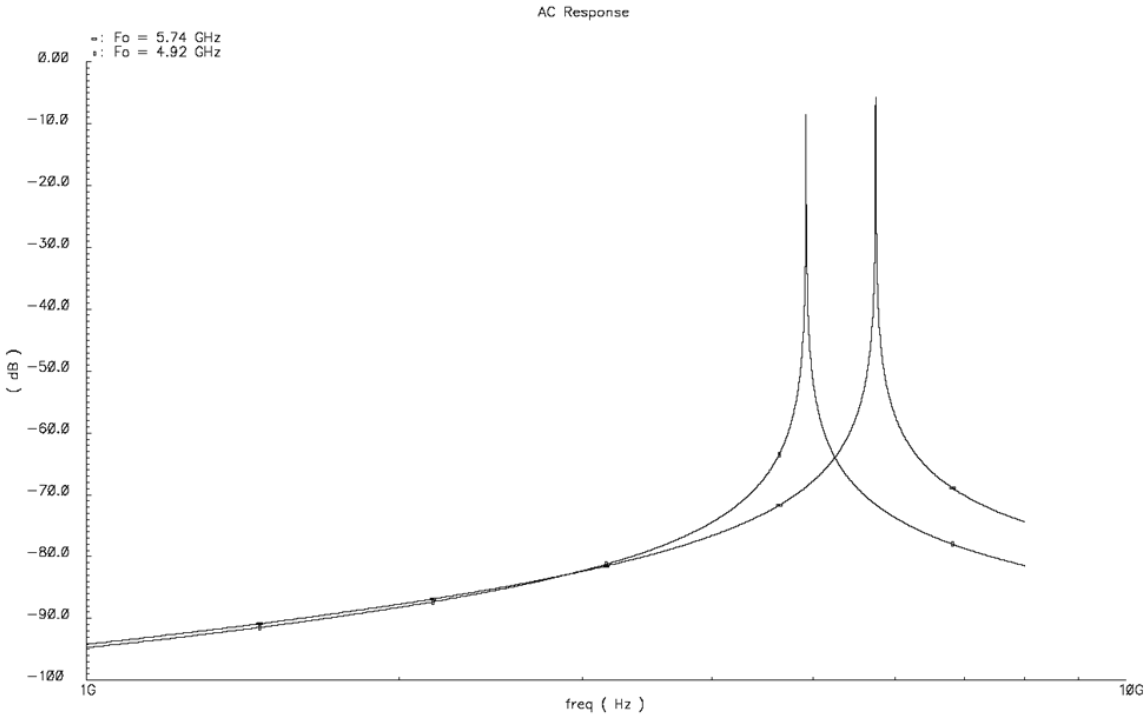


Fig. 4.31 Bandwidth increase with 820 MHz at 4.92 GHz (ideal case)

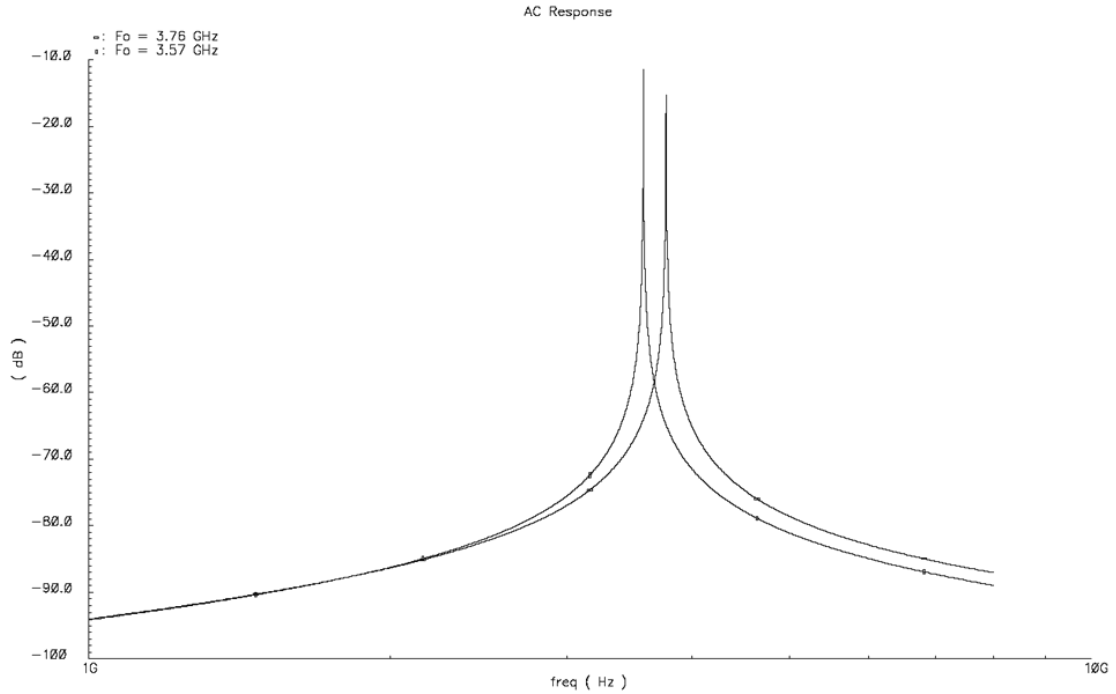


Fig. 4.32 Bandwidth increase with 190 MHz at 3.57 GHz (real case)

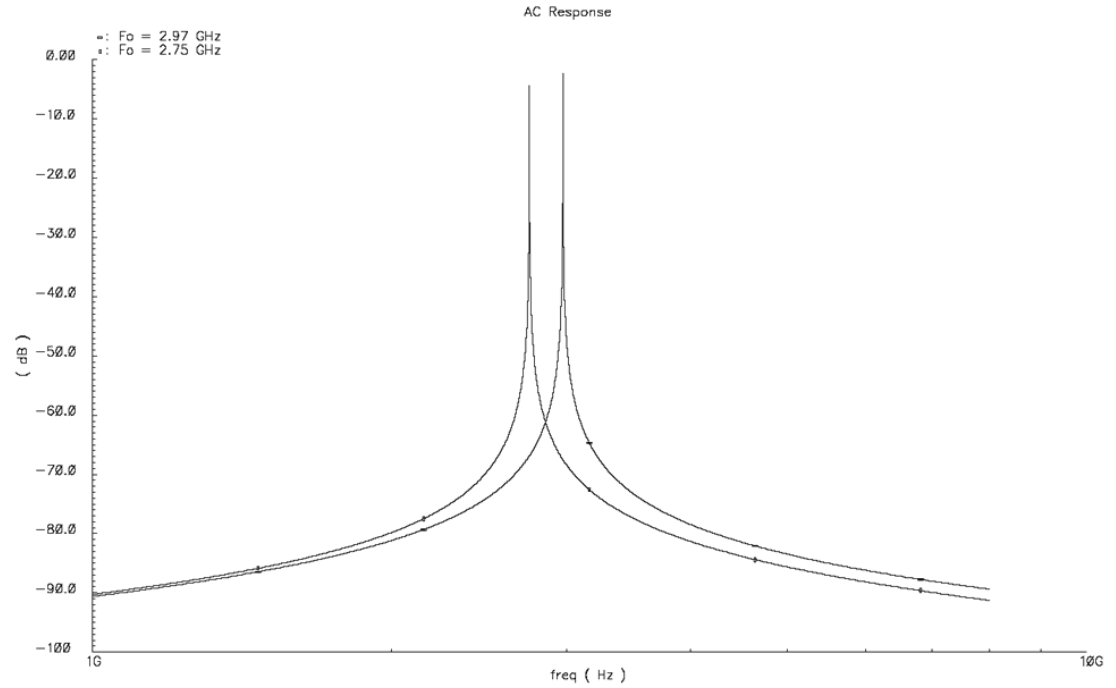


Fig. 4.33 Bandwidth increase with 220 MHz at 2.75 GHz (real case)

Even if lower frequency improvement is obtained for this enhancement method with real circuit (due to the negative resistance parasitics), a certain frequency enhancement is obtained when using negative resistance compared to the original inductor where the frequency decreases as the quality factor is improved.

The steps to implement this method are the followings:

1. The active inductor, without any resistance, is designed at a particular frequency.

2. The negative resistance is used in order to obtain the highest quality factor value. A decreased value for ω_0 is obtained.

3. The supplementary gate resistance is tuned up until the self resonant increases to the highest achievable frequency when the positive resistance keeps its novel value. The quality factor will decrease correspondingly.

4. The negative resistance is tuned to improve the quality factor and all steps are repeated until no frequency enhancement is obtained.

4.4.2 Active Inductor with Improved Biasing Scheme

Rewriting the equations which describe the inductor behavior as given by (4.62) an interesting aspect can be noticed regarding the quality factor tuning.

$$\begin{cases} 2\alpha = \dfrac{C_{gs1}(g_{o1} + g_{m2} + g_{o2} - G_{neg}) + g_{o2}C_{gs2}}{C_{gs1}C_{gs2}} \\ \omega_o^2 = \dfrac{g_{m1}(g_{m2} + g_{o2}) + g_{o1}g_{o2} - g_{o2}G_{neg}}{C_{gs1}C_{gs2}} \end{cases} \tag{4.62}$$

As can be noticed from (4.62), the influence of the negative resistance on the self resonant frequency is 'mediated' by a single factor term – g_{o2}. In other words, if the output resistance is infinite, the frequency is not influenced by the quality factor tuning. Therefore, the second method to implement an approximate independent frequency and quality factor tuning is to increase the output resistance for transistor M_2. Two possibilities exist:

- to use a cascode configuration, impossible to design for this configuration since no voltage can be left for a fourth V_{ds};

- to increase the output resistance of transistor M_2 by increasing V_{ds2}, in other words letting much voltage on this transistor.

The second possibility was implemented in this research and the single way to implement the second possibility seems to be the use of a floating voltage source. The improved active inductor was proposed in [4.18] and illustrated in Fig. 4.34.

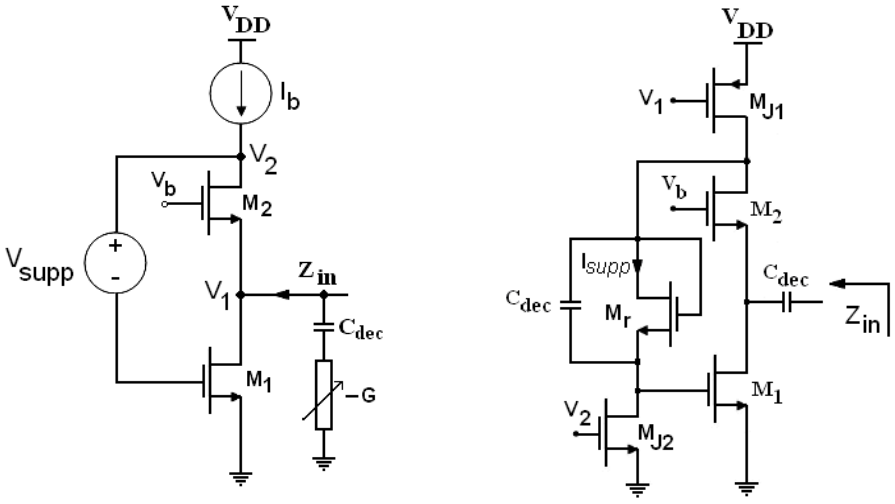


Fig. 4.34 Proposed active inductor, ideal case (left) and real implementation (right)

The simplest way to implement this floating voltage is to connect the gate of transistor M_2 to the node (2) through a parallel RC tank and introducing a supplementary NMOS transistor to draw the resistor current to the ground. Only a floating voltage is seen on the dc path while in ac it is a short circuit. However, this is not a simple task since connecting a passive resistor on the signal path adds much noise and deteriorates the overall noise factor. A possibility is to use small resistors but the current consumption is increased. To minimize the noise, the resistor may be implemented with diode connected transistors, solution proposed in [4.18] and presented in Fig. 4.34 too. In turn, a high resistance is implemented with small size transistors and furthermore facilitating small currents to implement the voltage source. In the proposed circuit, the resistor is implemented by M_r while the current source is M_{J2}.

Reconsidering the original active inductor, V_{gs1} and $V_2=V_{ds1}+V_{ds2}$ are identical fact that represents the most important drawback when designing this circuit. This constraint envisages particularly the output transistor voltages V_{ds} since by coupling the above mentioned transistors in such configuration it is difficult to design high drain to source voltages. In turn, by introducing the supplementary voltage V_{supp}, as showed in Fig. 4.34, the biasing of M_1 and M_2 become independent. However, this method is not perfect since the supplementary voltage added to M_1 and M_2 is taken from the output V_{ds} of the current source (I_b) fact that imposes careful design. This voltage may be distributed to M_2 only, if V_g is kept constant, or be shared by both transistors when V_g is changed correspondingly. To conclude, the method of using floating voltages has only benefits for the transistors biasing and frequency behavior.

Simulations carried out in a 0.18μm CMOS technology have proved that if higher values are set for the floating voltage, the effect of the negative resistance on the frequency value is strongly decreased, as presented in Table 11.

V_{supp} [V]	f_0 [GHz]	g_{ds1} [μS]	g_{ds1} [μS]	-R [kΩ]	f_0' [GHz]	Δf [MHz]
0	3.690	8.63	8.22	3.364	3.565	125
0.1	3.738	8.59	7.24	3.339	3.623	115
0.2	3.776	8.55	6.44	3.321	3.671	105
0.3	3.810	8.52	5.79	3.305	3.712	98
0.4	3.839	8.49	5.24	3.292	3.748	91
0.5	3.867	8.47	4.78	3.280	3.780	87
0.6	3.889	8.45	4.39	3.269	3.809	80
0.7	3.913	8.43	4.05	3.259	3.836	77

Table 11 The influence of the floating voltages on the frequency–Q interdependence

Rewriting the equations which describe the inductor behavior and taking into account the finite output resistance of the current source M_{j1}, the novel relations for ω_0 and Q are the following (4.63):

$$\begin{cases} 2\alpha = \dfrac{C_{gs1}(g_{o1}+g_{m2}+g_{o2}-G_{neg})+(g_{o2}+g_{oJ})C_{gs2}}{C_{gs1}C_{gs2}} \\ \omega_o^2 = \dfrac{g_{m1}(g_{m2}+g_{o2})+g_{o1}g_{o2}-G_{neg}(g_{o2}+g_{oJ})+g_{oJ}(g_{o1}+g_{o2}+g_{m2})}{C_{gs1}C_{gs2}} \end{cases} \quad (4.63)$$

As seen from the above equation, the use of real current sources deteriorates the overall frequency behavior since a supplementary term (g_{oJ}) increases the inter–dependence of the inductor parameters (f_0, Q). As the simulations show, a compromise between the value of the supplementary voltage and the quality of tuning should be addressed.

Finally, since no high precision is required and the current consumption is small, this method is attractive when implementing TOSI based reconfigurable RF filters.

4.5 CONCLUSION

The most important contributions added to the simulated inductors field were presented in this chapter. Original and promising results obtained for one particular inductor architecture and covering the active inductor passive model, the independent frequency and quality factor tuning but also some frequency behavior improvement methods (active inductor with supplementary gate resistance and floating voltage source) were presented and described in detail. If the research continues on this direction, a

reconfigurable TOSI based high order active bandpass filter will be designed in CMOS process.

4.6 REFERENCES

[4.1] Analog Integrated Circuit Design, Ken Martin, 1997

[4.2] Analysis and Design of Analog Integrated Circuits, 4th Edition, P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, John Wiley & Sons Ltd, 2001

[4.3] CMOS Circuit Design, Layout and Simulation, Baker, 1997

[4.4] CMOS RF Modeling, Characterization and Applications, J. Deen and T. A. Fjeldly, Selected Topics in Electronics and Systems – Vol. 24, World Scientific Publishing, 2002

[4.5] Improved RF CMOS Active Inductor with High Self Resonant Frequency, C. Andriesei, L. Goraş, F. Temcamani and B. Delacressonnière, ICECS, December 12–15, 2010, Greece

[4.6] On the Tuning Possibilities of an RF Bandpass Filter with Simulated Inductor, C. Andriesei and L. Goraş, Proc. of the 30th International Semiconductor Conference (CAS), vol. 2, pp. 489–492, October 2007, Sinaia, Romania

[4.7] On Frequency and Quality Factor Independent Tuning Possibilites for RF Band–pass Filters with Simulated Inductors, C. Andriesei and L. Goraş, Romanian Journal of Information Science and Technology, Vol. 11, No. 4, pp. 367-382, 2008

[4.8] On High Frequency Active Inductor Based Active Filters, C. Andriesei and L. Goraş, Workshop on Signal Processing Systems for Wireless Communications, Cluj–Napoca, July, 3 – 4th, 2008, Romania

[4.9] Accordabilite des Filtres RF Passe-Bande Integres Utilisant Une Inductance Active, C. Andriesei, L. Goraş, B. Delacressonnière and F. Temcamani, Congres Mediterraneen des Telecommunications et Exposition, 14–16 March 2008, Tanger, Maroc

[4.10] RF Circuit Design, R. C. –H. Li, John Wiley & Sons, 2009

[4.11] Negative Resistance Based Tuning of an RF Bandpass Filter, C. Andriesei, L. Goraş and F. Temcamani, Proc. of the 4th European Conference on Circuits and Systems for Communications, ECCSC, pp. 1–4, July 10–11, Bucharest, Romania, 2008

[4.12] On an RF Bandpass Filter Tuning Method, C. Andriesei, L. Goraş and F. Temcamani, Revue Roumaine des Sciences Techniques, Serie Électrotechnique et Énergétique, in print (2010)

[4.13] On the Tuning Performance of an Active RF Bandpass Filter, C. Andriesei and

L. Goraş, ACTA TECHNICA NAPOCENSIS, Electronics and Telecommunications Vol. 49, No. 3, pp. 29–34, 2008

[4.14] Active RF Bandpass Filter with Wide Frequency Tuning Range, C. Andriesei, L. Goraş and B. Delacressonnière, Proc. of the 31st International Semiconductor Conference (CAS), Vol. 2, pp. 397–400, October 2008, Romania

[4.15] Filtre différentiel basé sur une inductance active avec commande indépendante de la bande passante et de la fréquence, C. Andriesei, L. Goraş, F. Temcamani and B. Delacressonnière, 16èmes Journées Nationale Microondes, Mai 2009, Grenoble, France

[4.16] Wide Tuning Range Active RF Bandpass Filter with MOS Varactors, C. Andriesei, L. Goraş, F. Temcamani and B. Delacressonnière, Romanian Journal of Information Science and Technology, Vol. 12, No. 4, pp. 485–495, 2009

[4.17] Frequency Enhancement Method Applied to a CMOS RF Simulated Inductor BP Filter, C. Andriesei, L. Goraş, F. Temcamani and B. Delacressonnière, Proc. of the 9th International Symposium on Signals, Circuits and Systems (ISSCS), Vol. 2, pp. 357–360, July 2009, Iaşi, Romania

[4.18] CMOS RF Active Inductor with Improved Tuning Capability, C. Andriesei, L. Goraş, F. Temcamani and B. Delacressonnière, Proc. of the 32nd International Semiconductor Conference (CAS), Vol. 2, pp. 397–400, October 2009, Sinaia, Romania

5. Conclusion and Future Work

In the following several conclusions regarding this thesis and personal contributions of the author are presented with respect to the articles published so far.

The thesis envisages the study and development of transistor only simulated inductor based filters suitable for RF applications in GHz domain.

After an introductory chapter presenting the filtering problem existent in the telecommunications applications, an entire chapter (Chapter 2) is dedicated to wireless standards and transceiver architectures. Spectrum allocation, out–of–band attenuation requirements for RF filters and the trend of multi–standard transceivers are all reviewed. Chapter 3 is thought as a 'state of the art' regarding the transistor only simulated inductor architectures. The gyrator concept is also reviewed here. Chapter 4 contains all the original contributions added with respect to the TOSI concept. The main contributions are further presented.

1. A method of independent frequency and quality factor tuning has been proposed for a single ended configuration of CMOS TOSI for lower frequencies (690 MHz).

2. The same method has been validated for a differential architecture for higher frequencies (1–3 GHz).

3. A study on the effect of the parasitic capacitors value on this independent tuning and the limitations of this method are reported.

4. The use of varactors in implementing wide frequency TOSI based active filters with independent tuning is investigated.

5. The frequency enhancement of a particular TOSI architecture by means of supplementary gate resistance is investigated.

6. A biasing improvement for the same simulated inductor with great benefits in frequency domain with positive effect on the independent tuning principle is proposed.

7. Finally, a state of the art is presented, including the most significant achievements in TOSI design.

Some of our research results have been published in journals indexed and abstracted to Thomson Reuters products while others were presented to international conferences.

If the research continues on this direction, the implementation of multi–standard 6^{th} order TOSI based active filter will be investigated aiming practical on–chip implementation. However, other RF applications making use of simulated inductors may be addressed as well.