

# Contribution à la Conception et Assistance au Prototypage de Systèmes Intégrés sur Silicium (CAPsis).

## Application à l'interrupteur automatique VD-MOSFET

Loïc Vincent

le 17 Novembre 2010

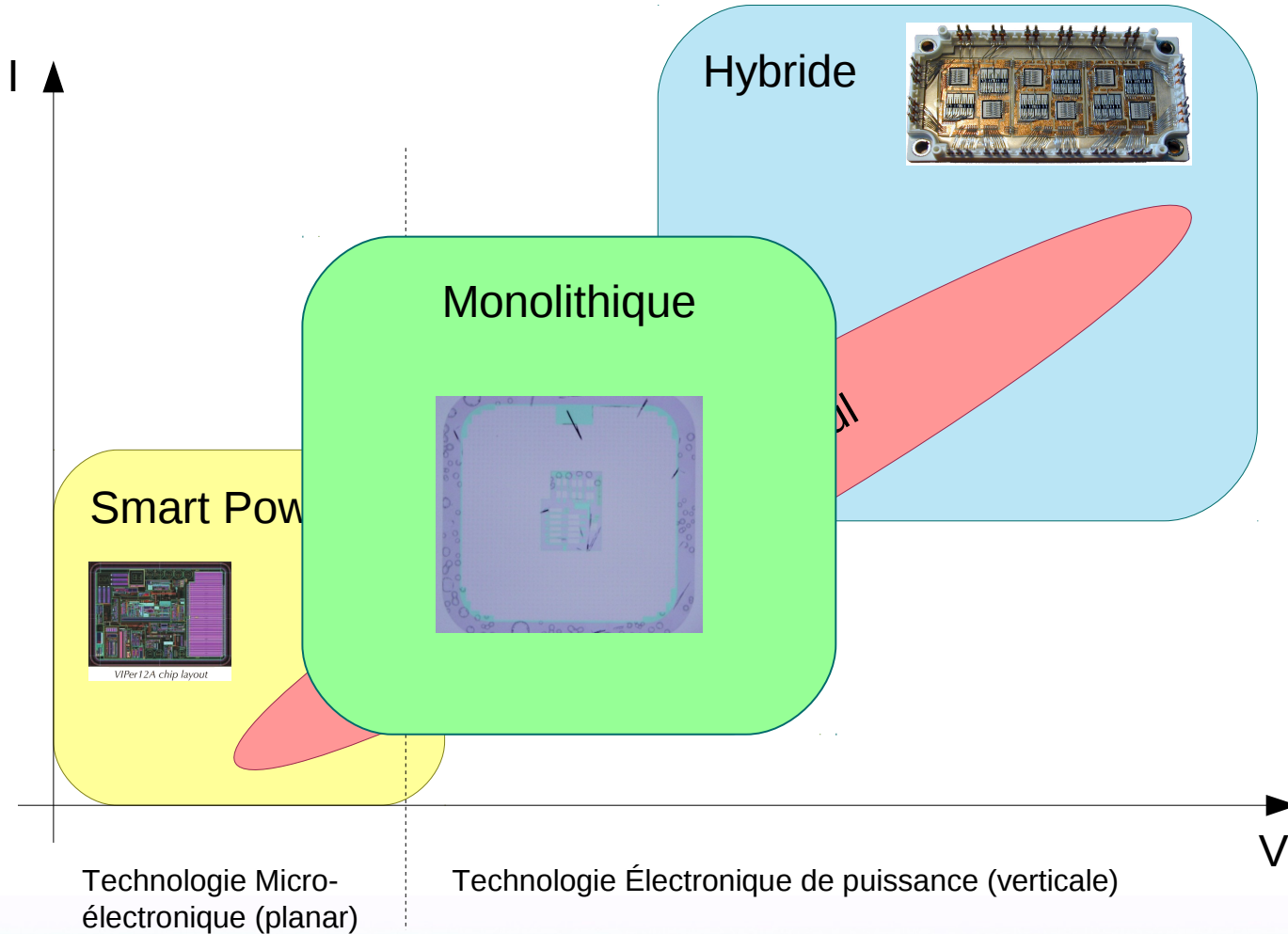
### Encadrement :

M. Christian Schaeffer,	Directeur de thèse
M. Jean-Christophe Crébier,	Co-encadrant
M. Laurent Gerbaud,	Co-encadrant

### Membres du jury :

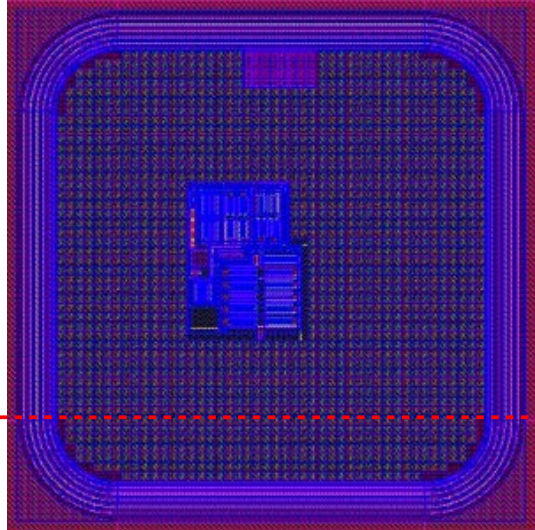
M. Bruno Allard,	Rapporteur
M. Frédéric Richardeau,	Rapporteur
M. Abdelhakim Bourennane,	Examineur

# Intégration en électronique de puissance

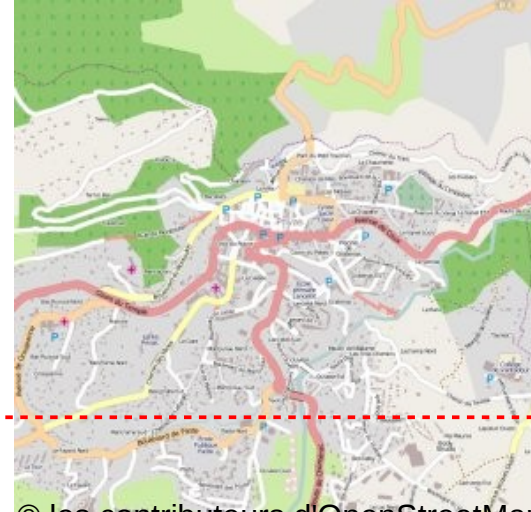


Composant pour application réseau en moyenne puissance

Jeu de masques VD-MOSFET fonctionnel

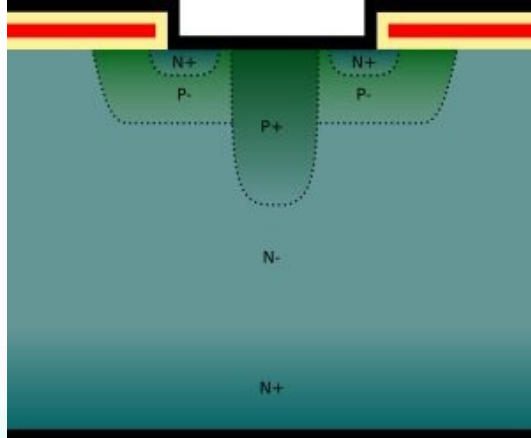


Carte géographique

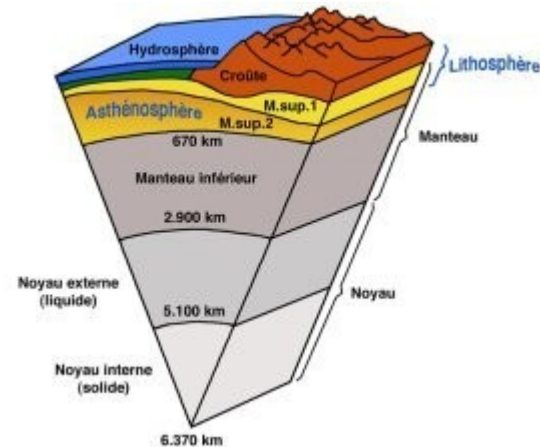


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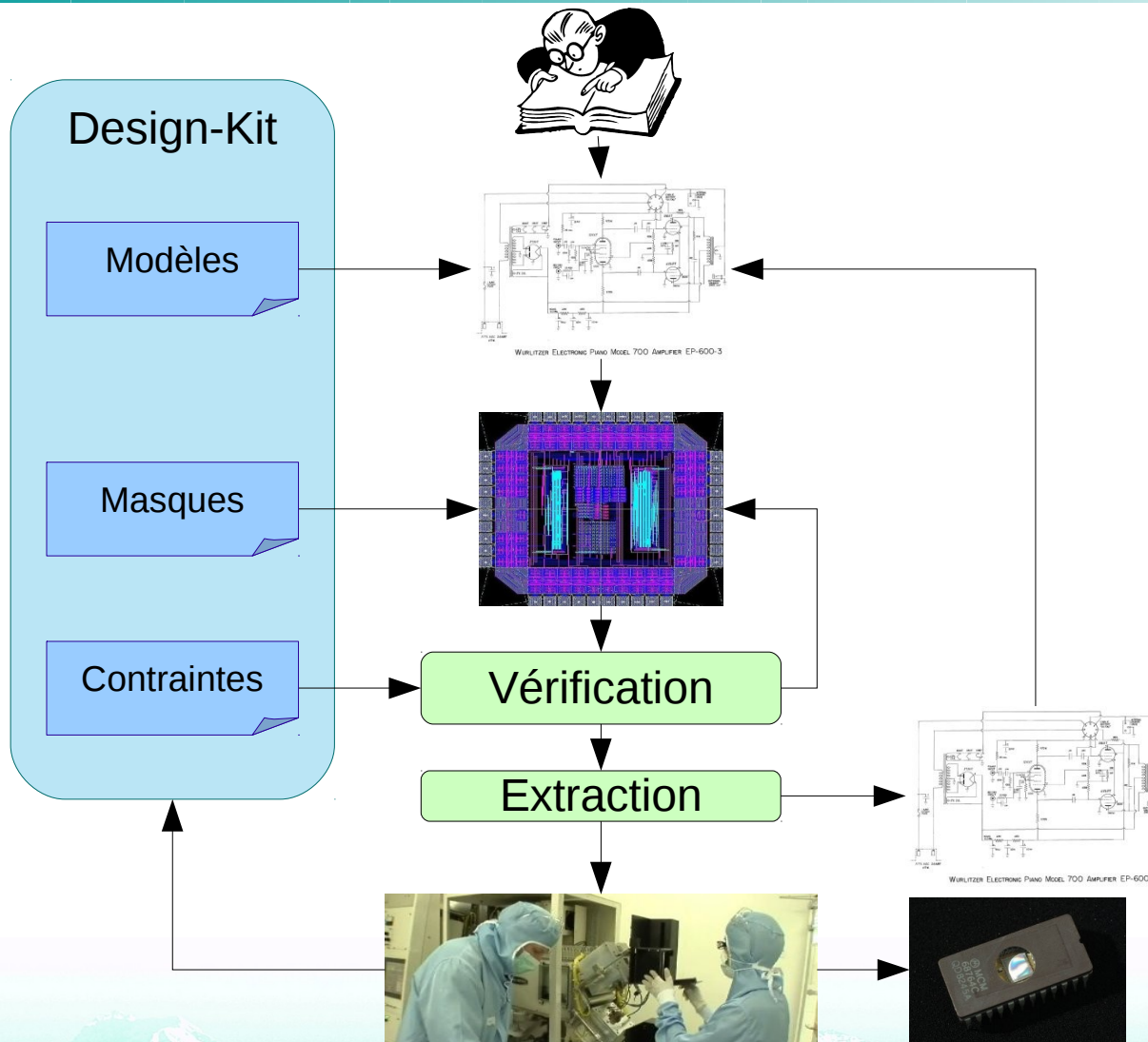
Coupe d'une cellule de VD-MOSFET



Géologie du sol

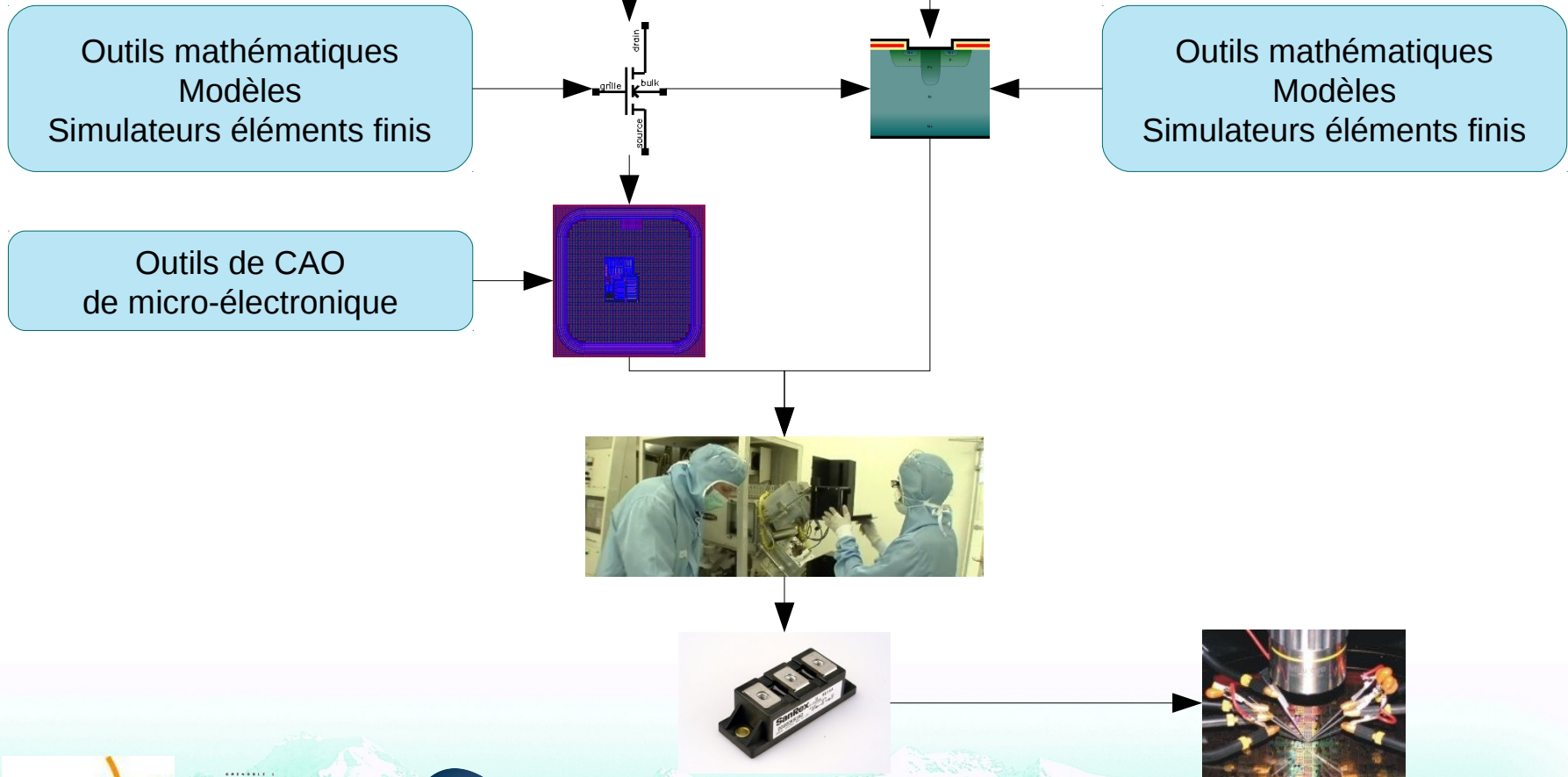


# Conception micro-électronique













# Conception académique actuelle en EP

Grenoble Génie Electrique  
Grenoble Electrical Engineering



# Micro-électronique vs électronique de puissance

	Micro-électronique	Électronique de puissance
Simulation		
Création de masques		
Vérification des masques		
Rebouclage		
Gestion des technologies		

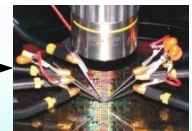
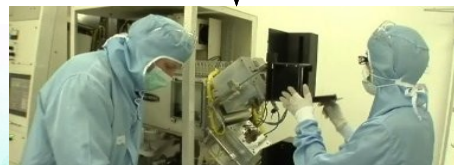
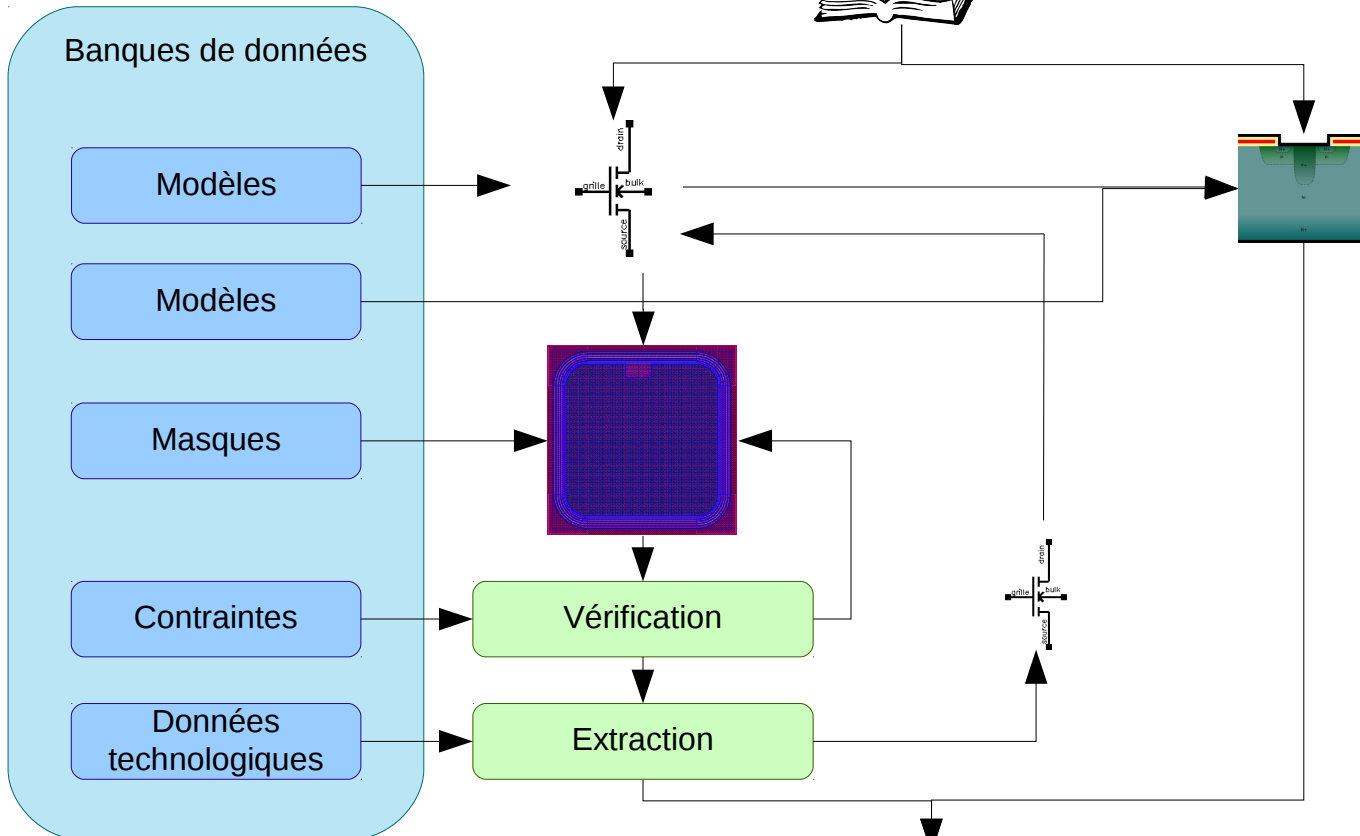
Peut-on améliorer l'assistance à la conception en EP ?

- La plateforme CAPsis
  - Conception assistée d'un système intégré sur silicium
  - Architecture de la plateforme
  - Banque de données
  - Design-kit de modèles par assemblage
  - Génération de masques automatiques
- Mise en application
  - Interrupteur à commutation automatique
  - Structure de test
  - Simulations
  - Masques
  - Prototype
- Conclusion & perspectives

# La plateforme CAPsis



# Conception d'un composant seul

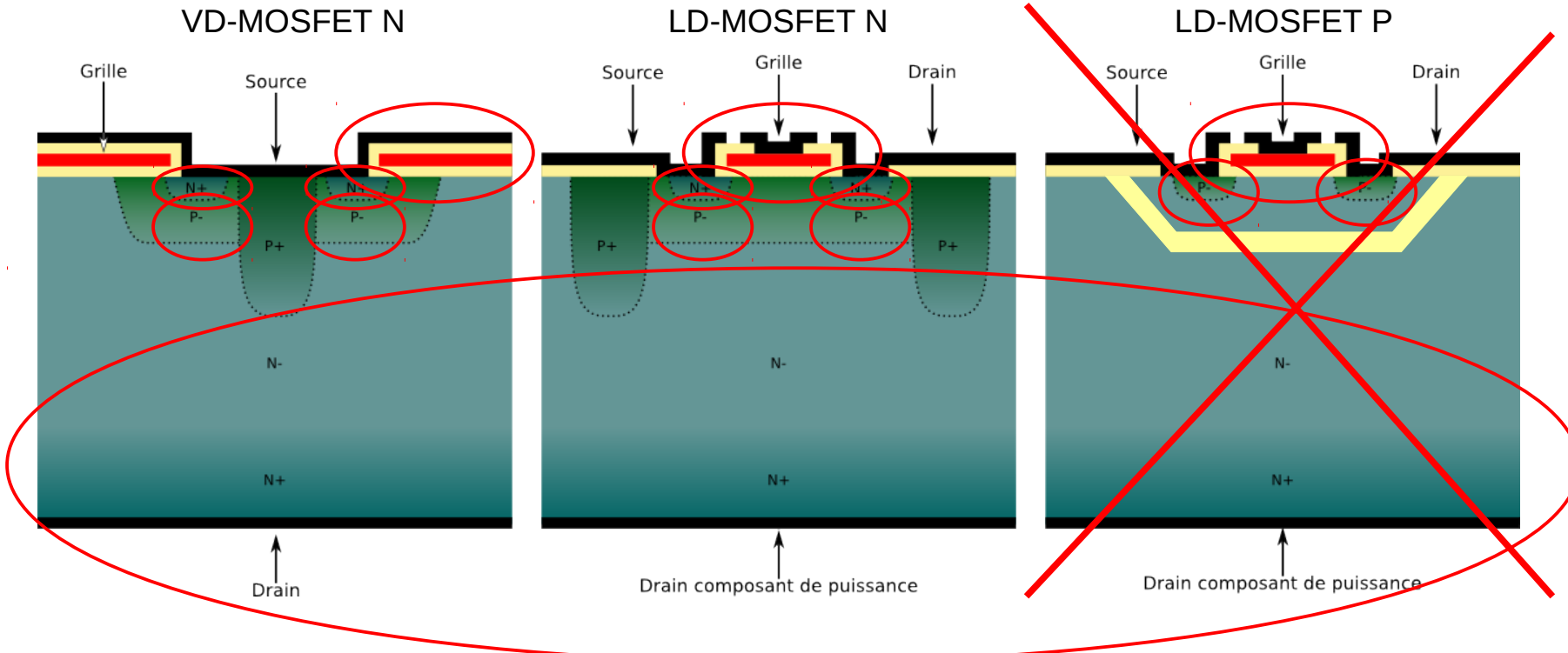


Géographie variable

Géologie variable

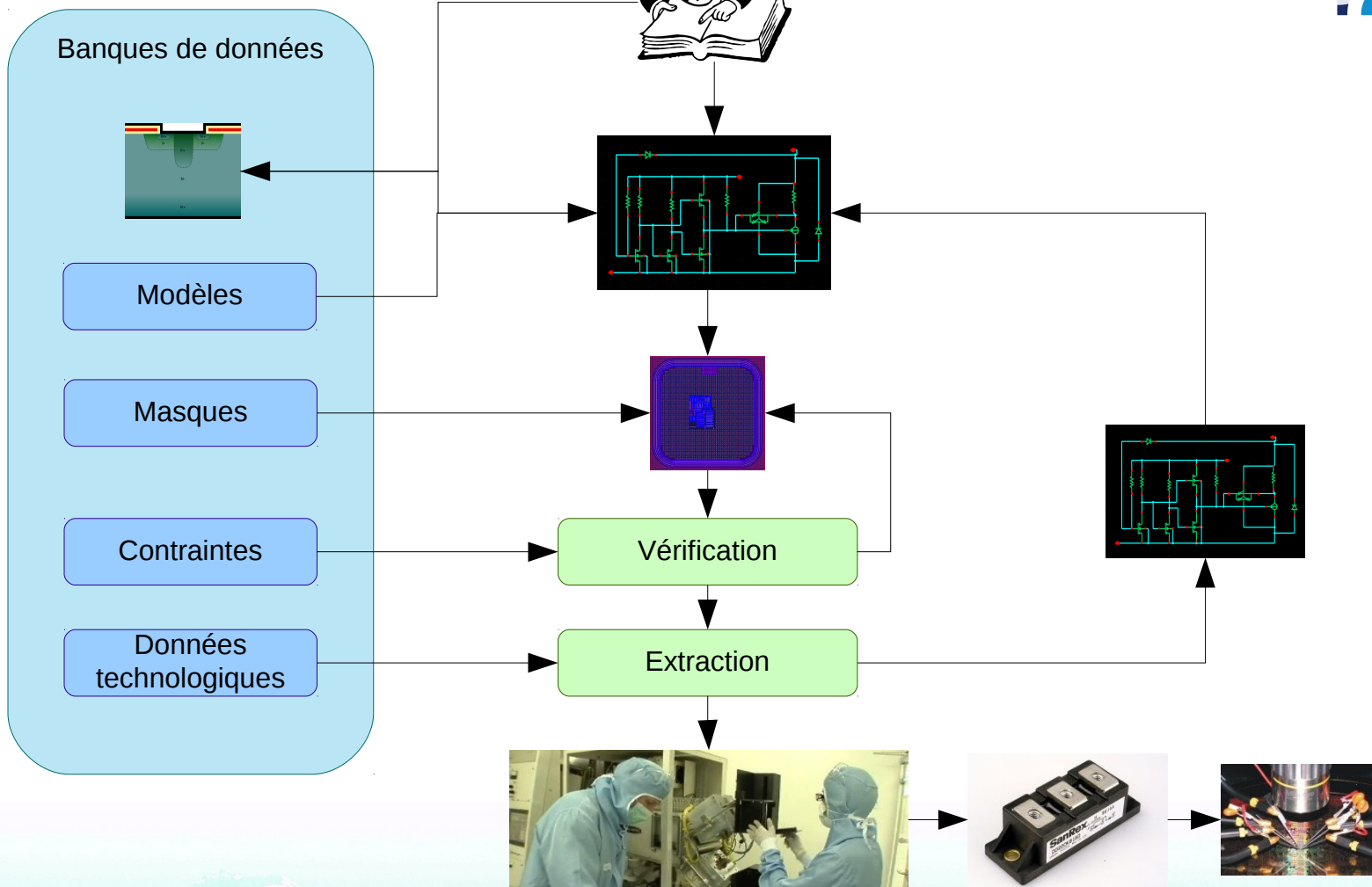
# Contraintes de la technologie monolithique

Sur la base d'un cheminement technologique VD-MOSFET



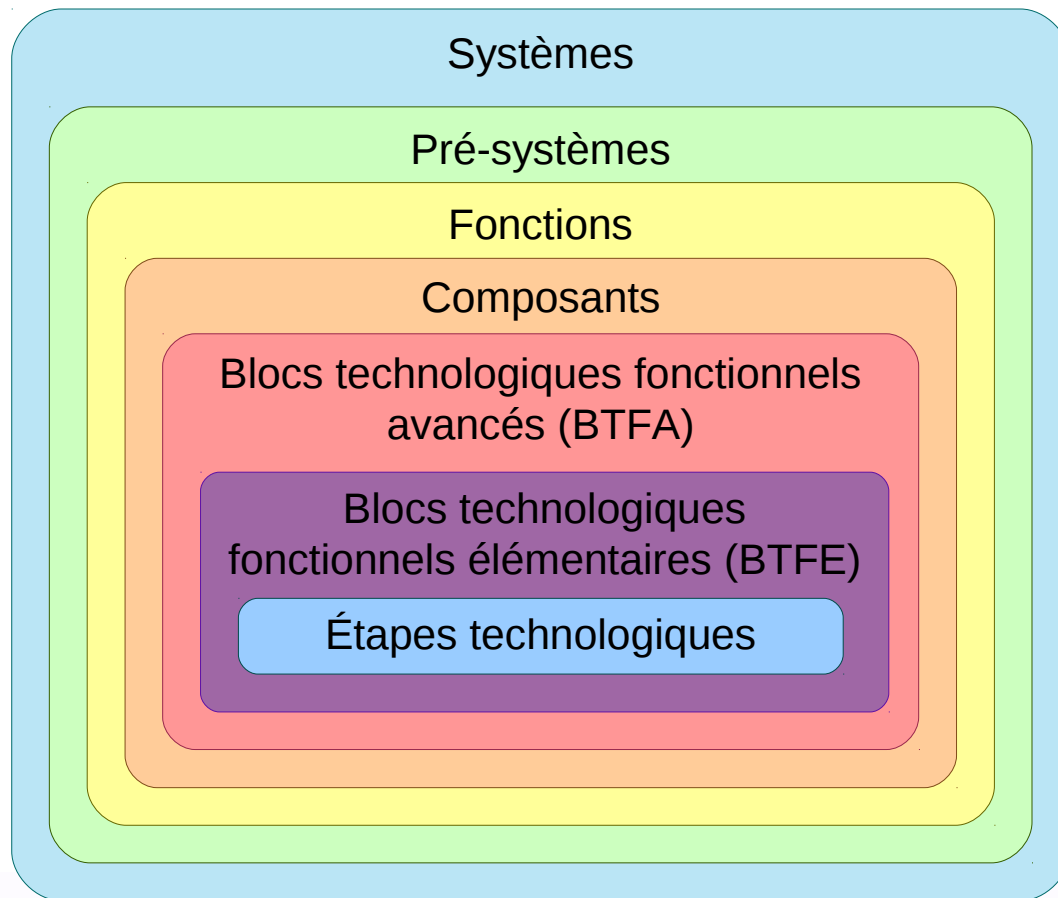
LD-MOSFET P non retenu  
LD-MOSFET N retenu  
Diode laterale  
Résistance : polysilicium ou N+

# Conception composant multi-fonctionnel

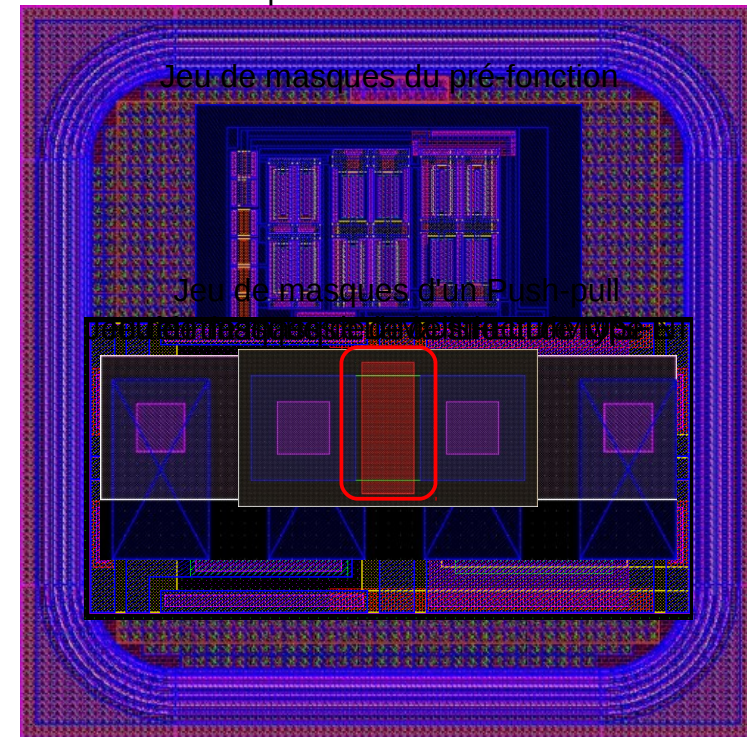


# Architecture retenue

# Banque de données : hiérarchie



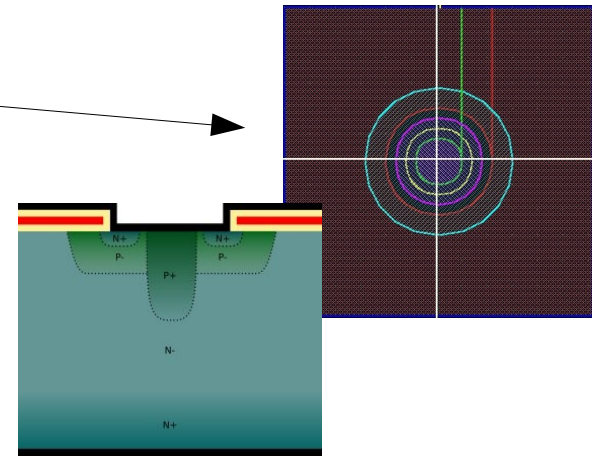
Jeu de masques VD-MOSFET fonctionnel



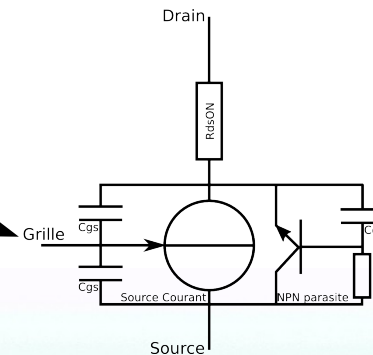
# Banque de données : éléments

Exemple : cellule VD-MOSET (BTFA)

- Masques
- Schématique
- Technologie utilisée
- Technologies compatibles
- Contraintes technologiques
- Paramètres
- Modèles



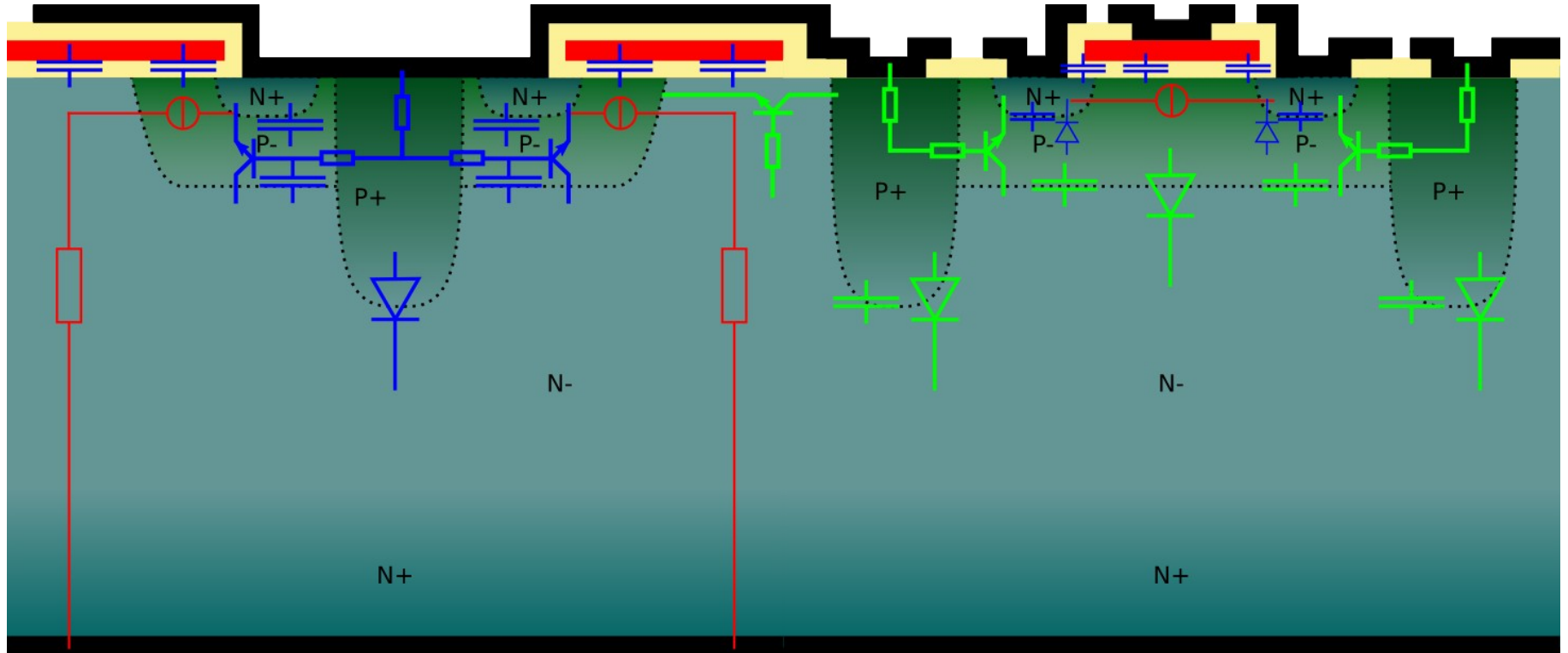
Largeur du canal, épaisseur d'oxyde,...



# Modélisation par assemblage

# Modélisation et couplage

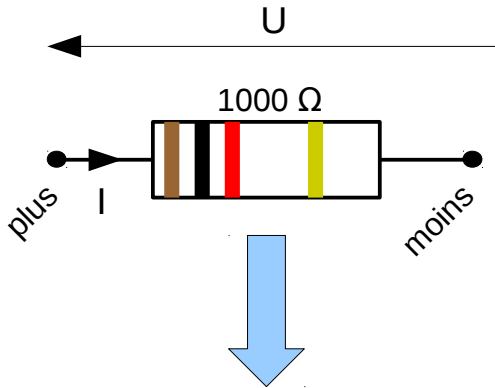
VD-MOSFET N      **Fonctionnels**  
Parasites  
**Environnementaux**      LD-MOSFET N



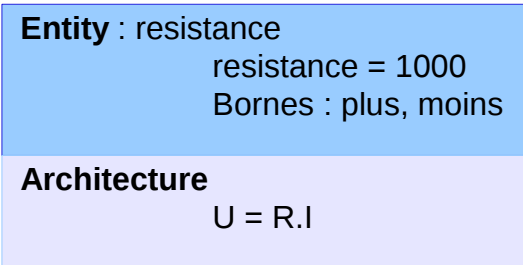
Capitalisation  
Pérennité  
Portabilité



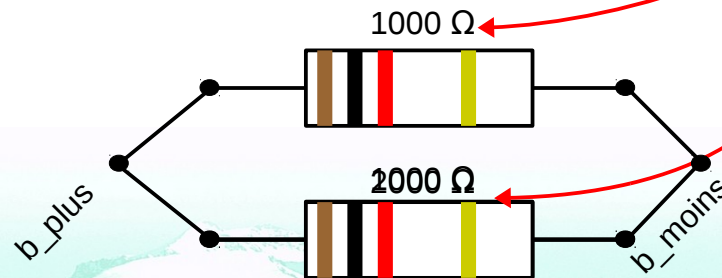
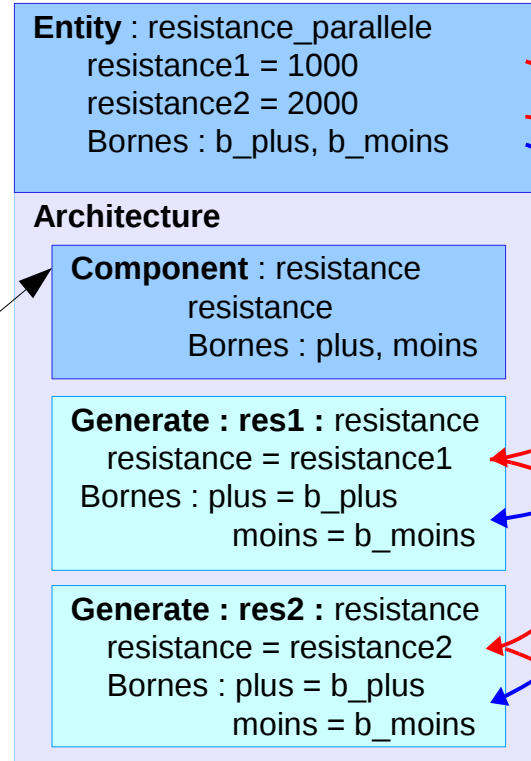
# Assemblage par VHDL-AMS



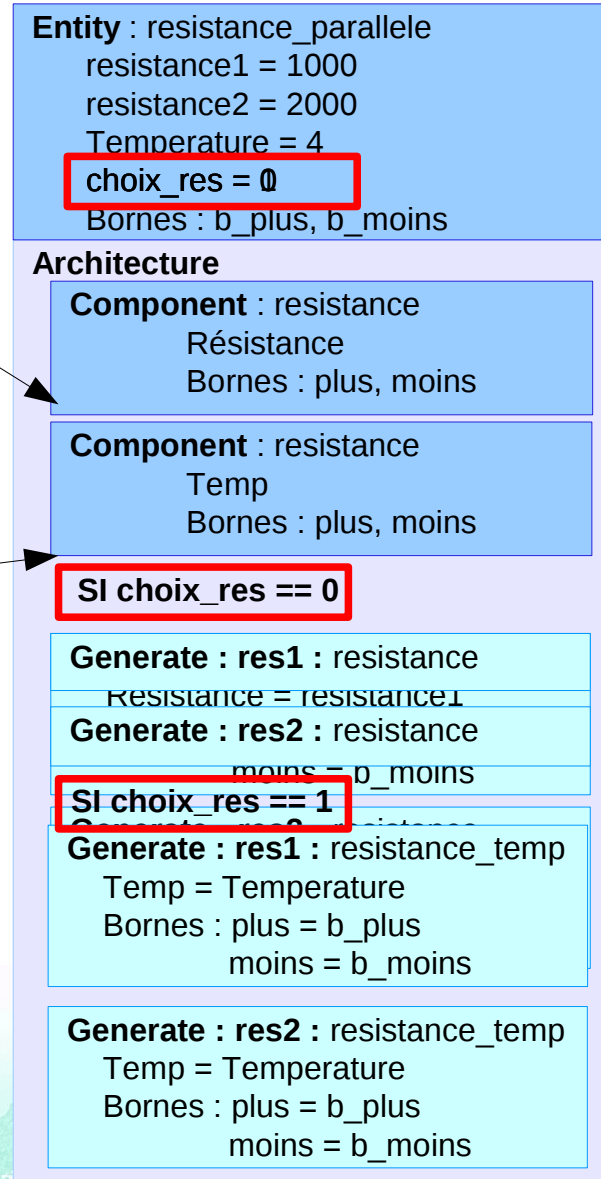
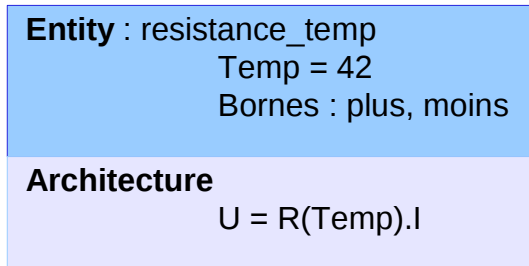
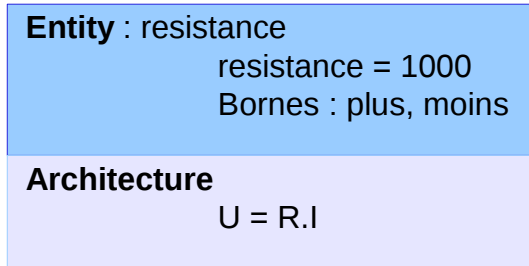
Vue extérieure



Vue intérieure



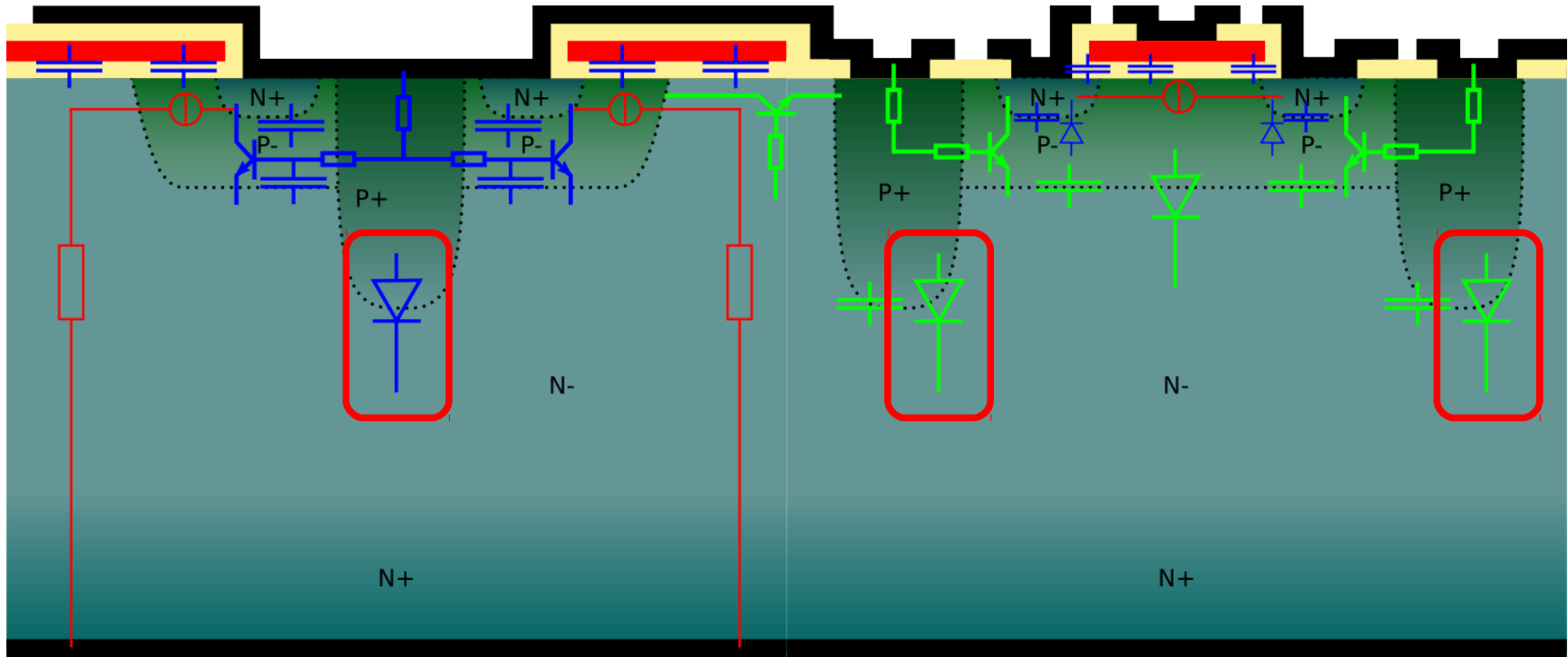
# Assemblage par VHDL-AMS



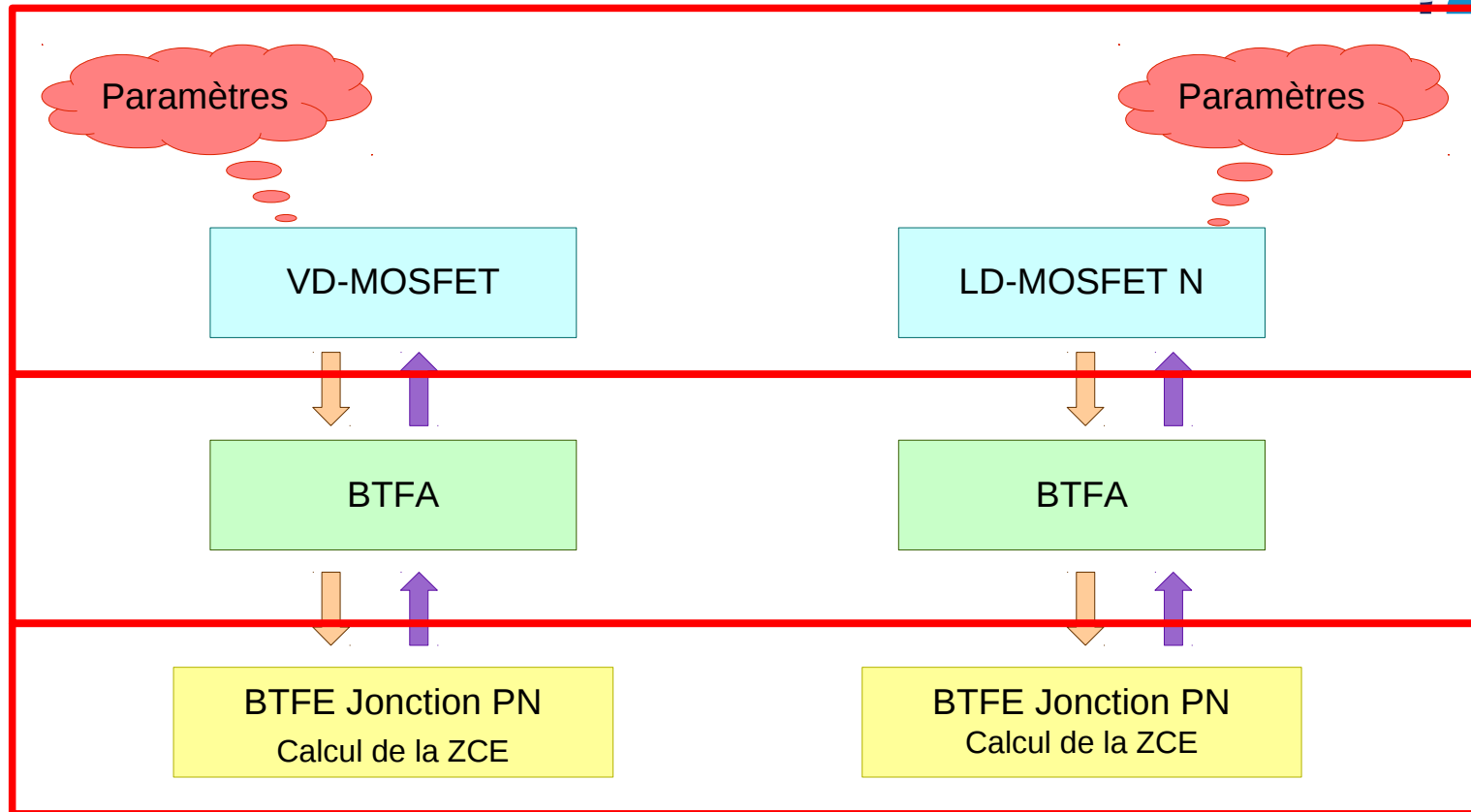
# Problématique de l'assemblage

## VD-MOSFET N

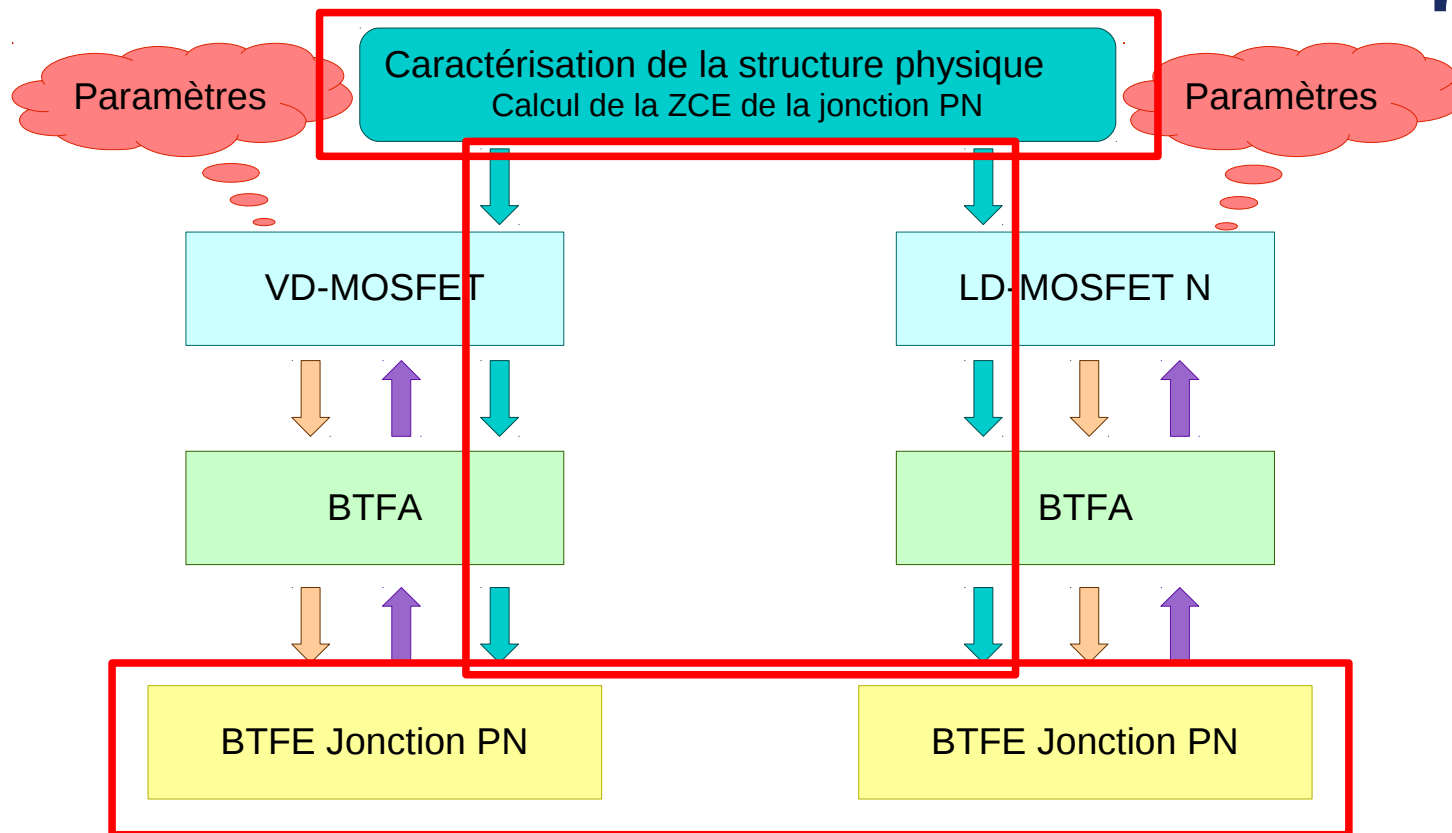
## LD-MOSFET N



# Redondance de calcul



# Suppression de la redondance de calcul



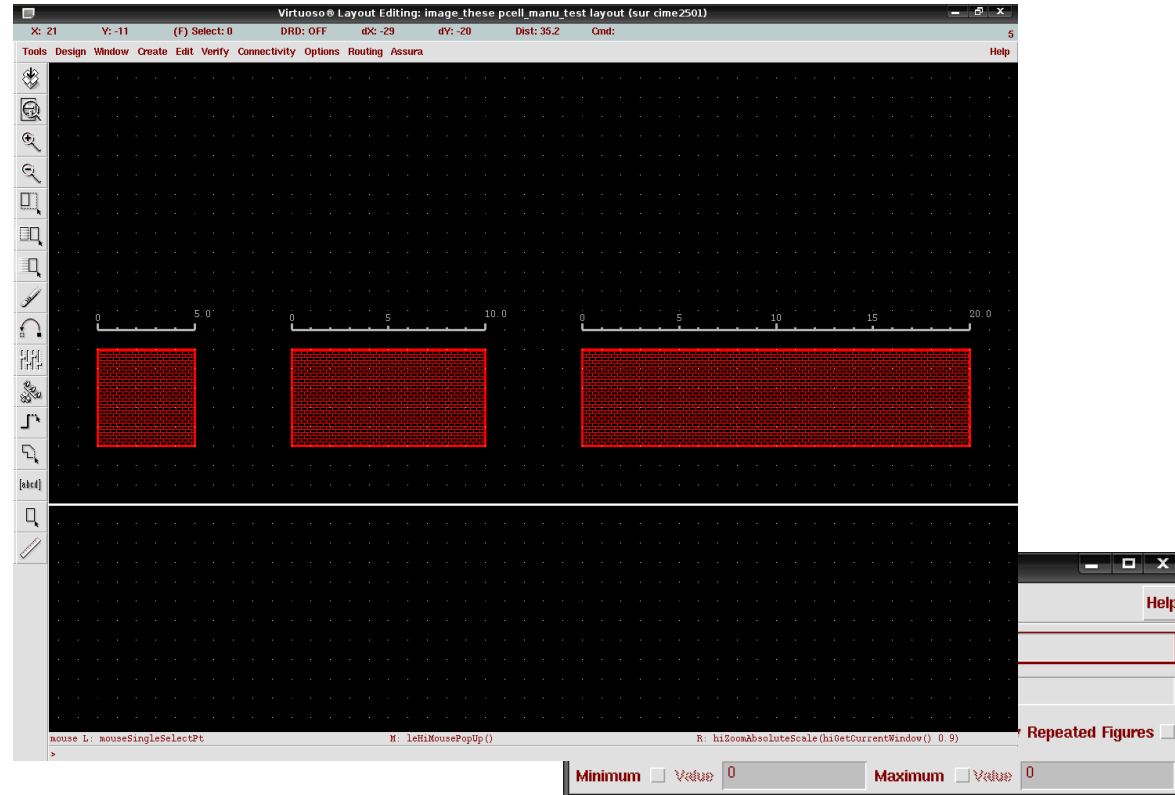
# Synthèse modélisation

- Librairie de modèles
- Structuration
- Assemblage
- Multi-niveaux
- Suppression redondance de calcul

# Génération de masques

# Masques paramétrés

## Création d'un pCell par interface graphique



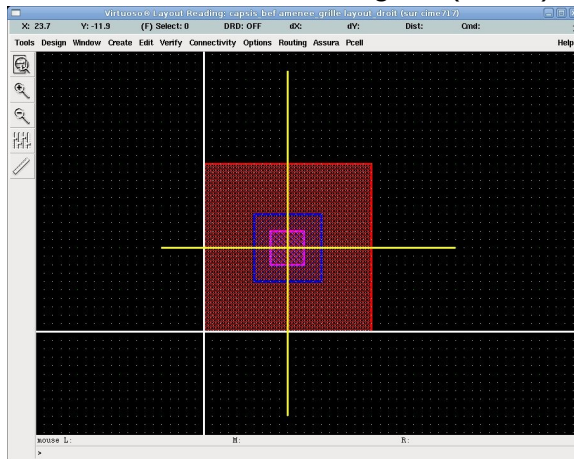
Utilisation du pCell  
Ajout de paramètres au jeu de masque  
Création d'un jeu de masque

Création d'un pCell par un langage de programmation possible

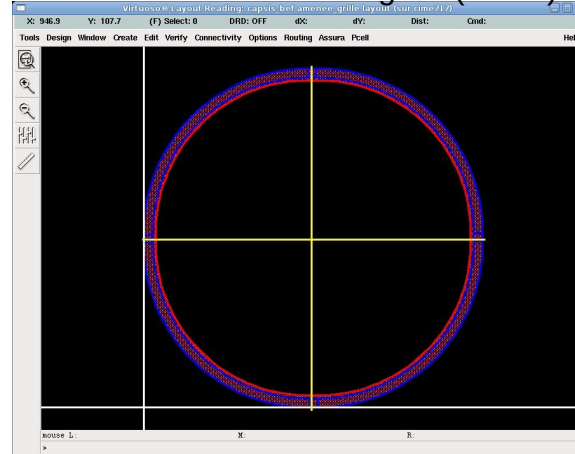


# Illustrations : niveau BTFE/BTFA

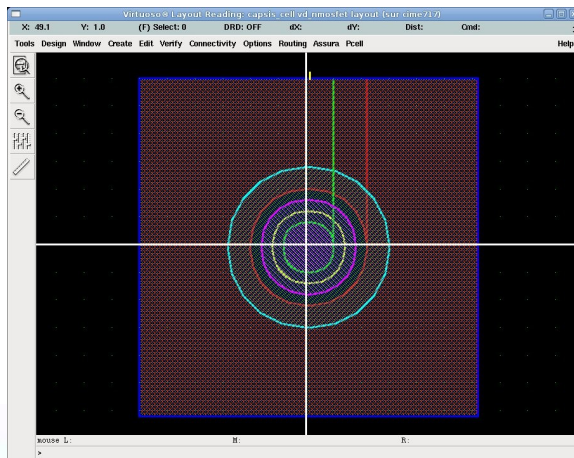
### Amenée de courant de grille (BTFE)



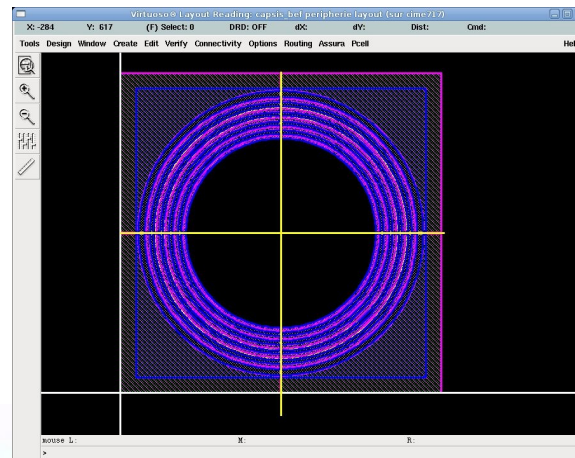
### Amenée de courant de grille (BTFE)



### Cellule VD-MOSFET (BTFA)



### Périphérie (BTFA)

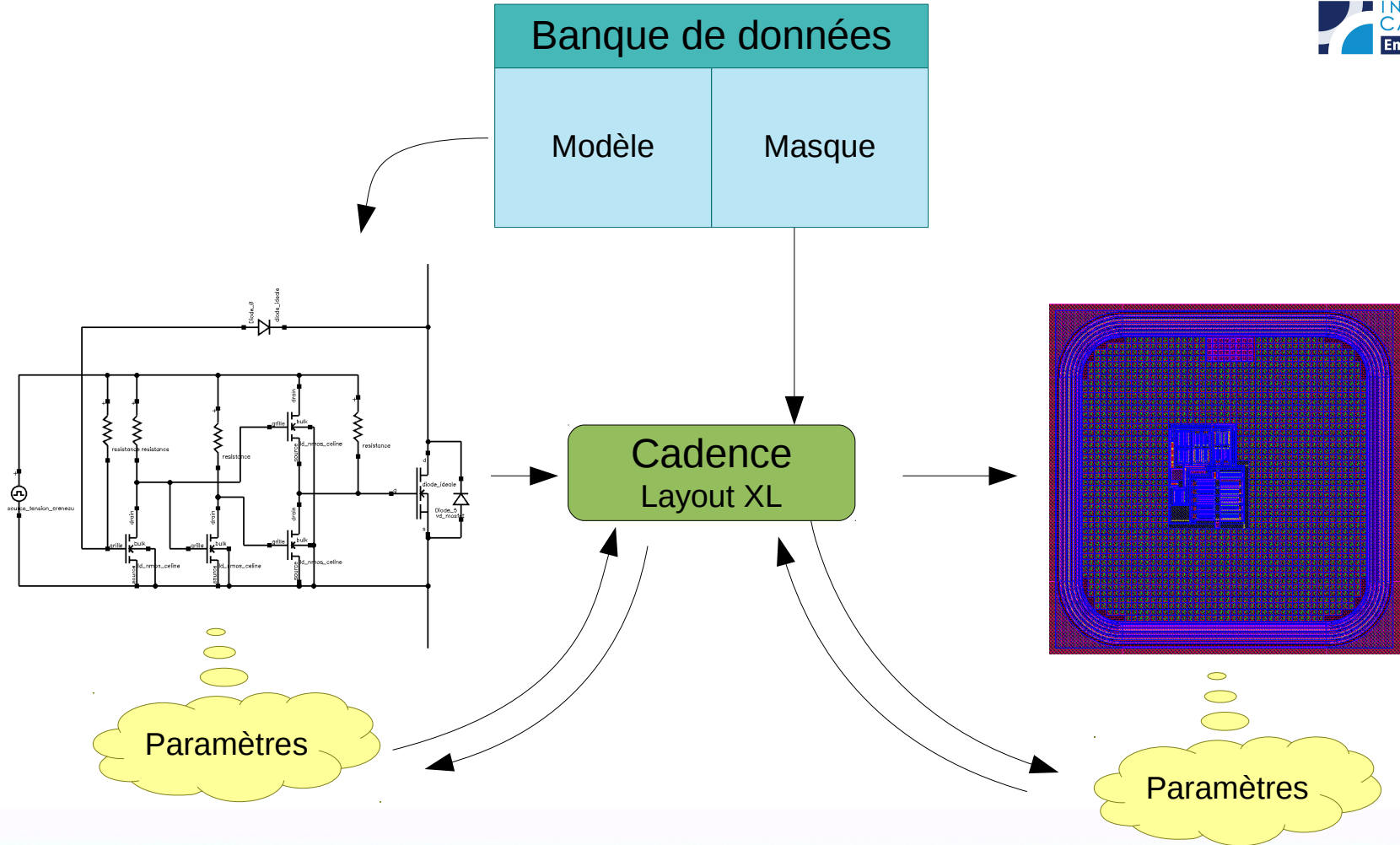


# Illustration : niveau composant

The screenshot displays the Virtuoso Layout Editor interface. The main window shows a MOSFET layout with a blue hatched area representing the gate and a red hatched area representing the source/drain regions. The layout is surrounded by a black border. The status bar at the top indicates coordinates (X: 7872, Y: 1722) and other parameters. The menu bar includes Tools, Design, Window, Create, Edit, Verify, Connectivity, Options, Routing, Assura, and Help. The 'Edit Instance Properties' dialog box is open, showing various parameters for the component. The 'Parameter' tab is selected, and the 'largueur\_puce' parameter is highlighted with a red box.

Parameter	Value
parasite_capacite_level	0.0
fonctionnel_rtison_level	0.0
fonctionnel_diode_level	0.0
cgs_fixe	210.0e-12
ctds_fixe	25.0e-12
cgd_fixe	180.0e-12
rtison_fixe	1.0
iss_diode	100.0e-9
<b>largueur_puce</b>	<b>0.4</b>
hauteur_puce	0.4
hauteur_aux	0.1

# Transferts de données Simu/Masques

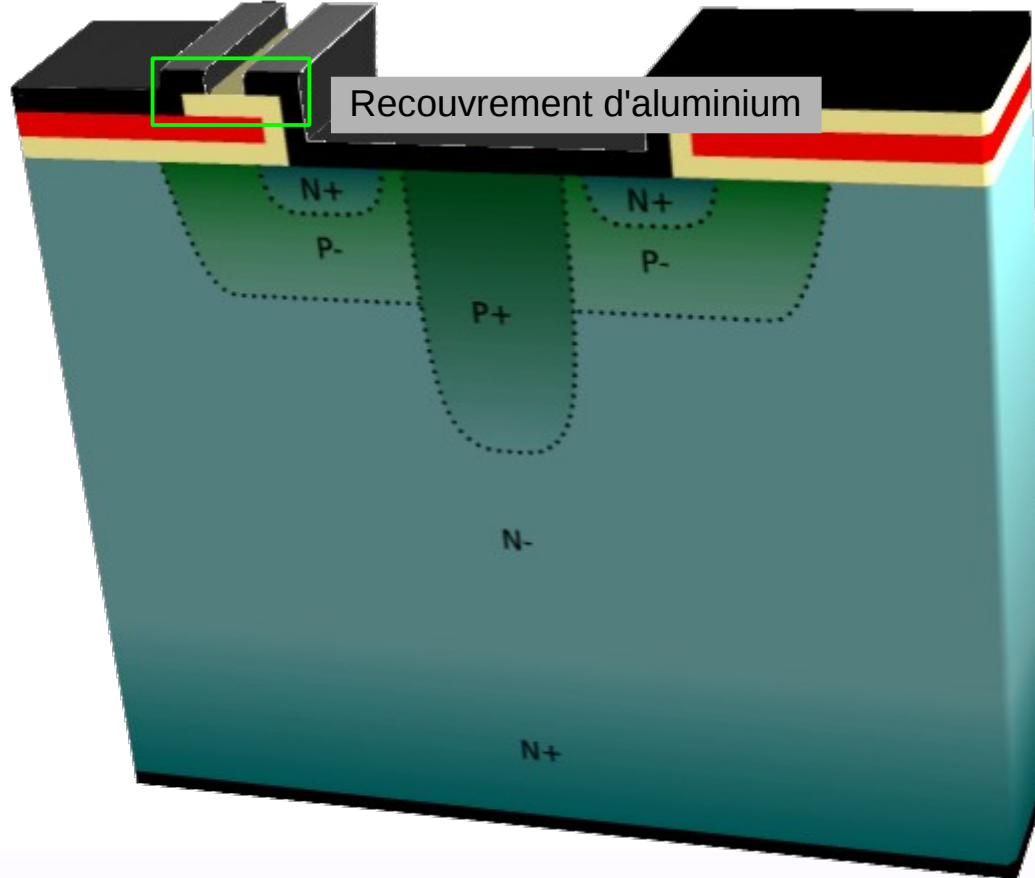


Placements et routage peuvent être non automatiques

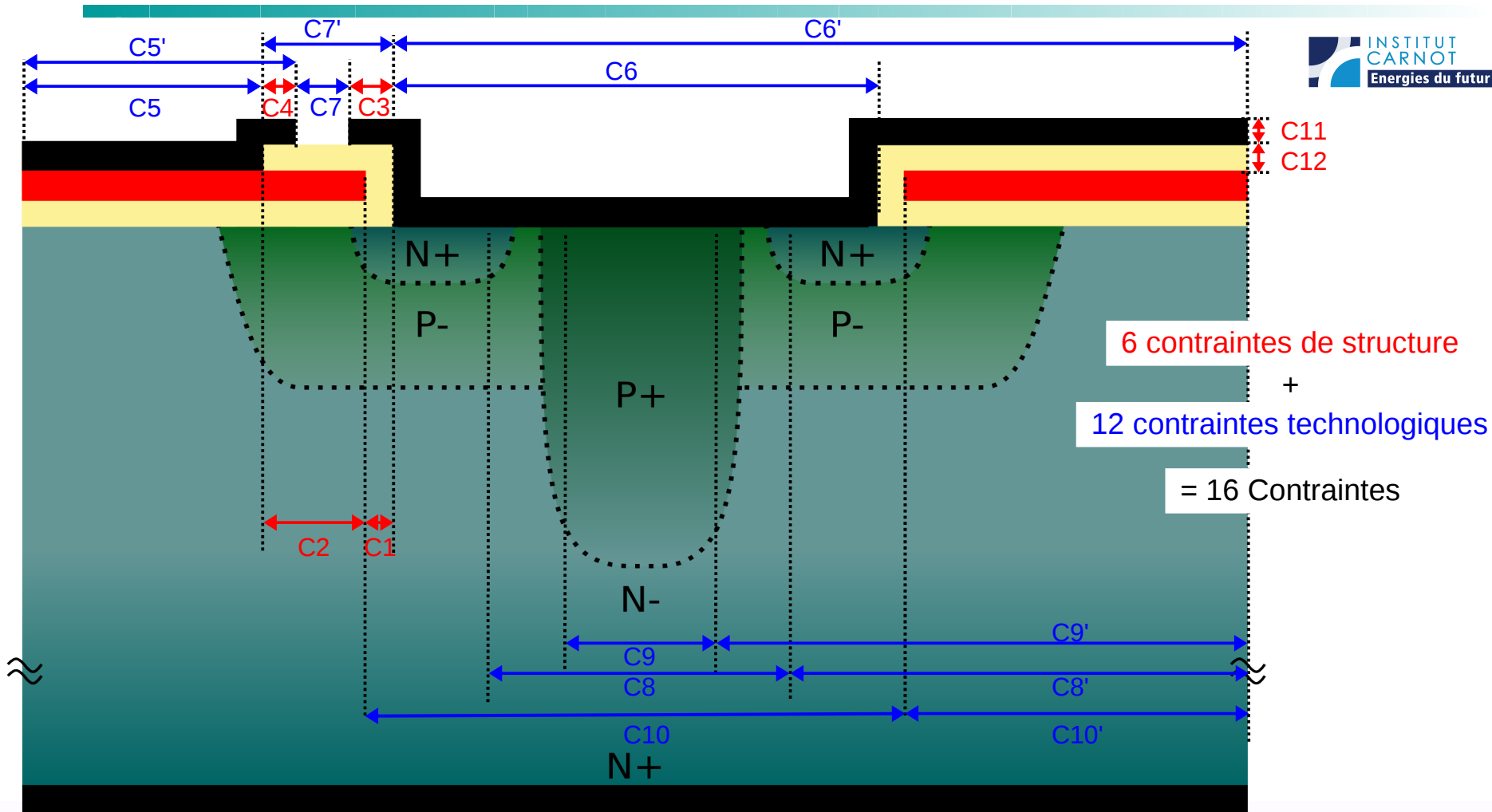
# Contraintes

┌ Ouverture d'aluminium 6 $\mu$ m

- Aluminium
- Polysilicium
- Oxyde



# Contraintes cellule VD-MOSFET



Création du fichier de règles  
Utilisation du DRC de Cadence

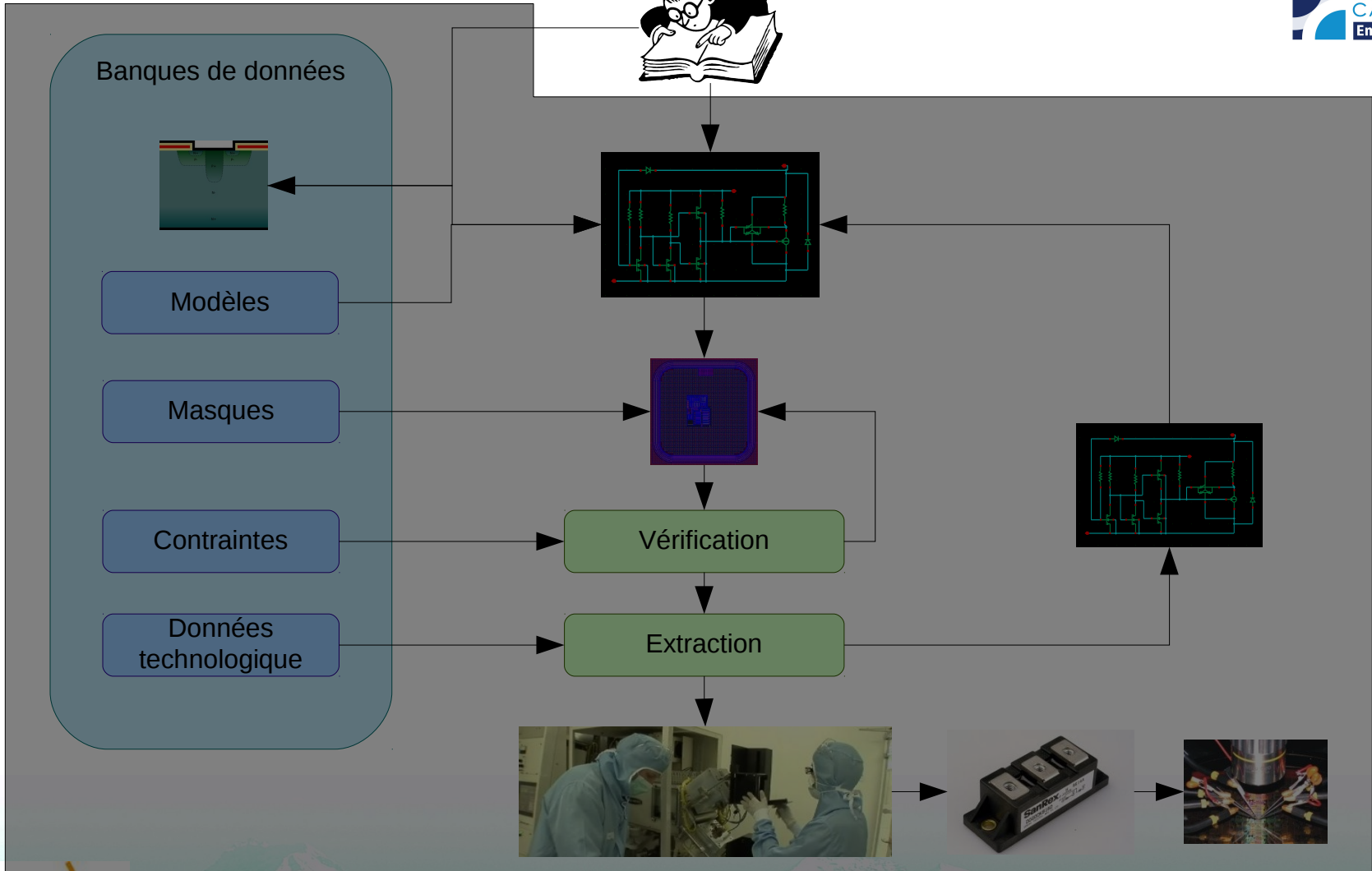
# Synthèse génération de masques

- Création d'une librairie de masques
- Génération de jeu de masques automatiquement
- Transferts bi-directionnels des paramètres
- Vérification automatique des contraintes technologiques et structurelles

# Mise en application

## Interrupteur à commutation automatique

# Cheminement de conception

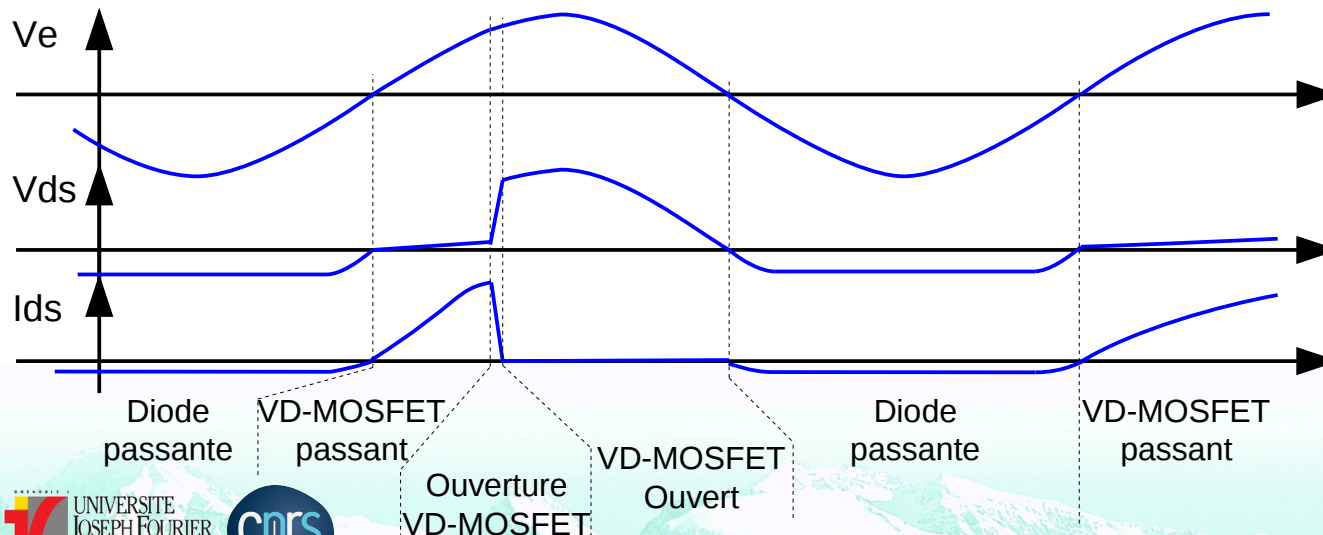
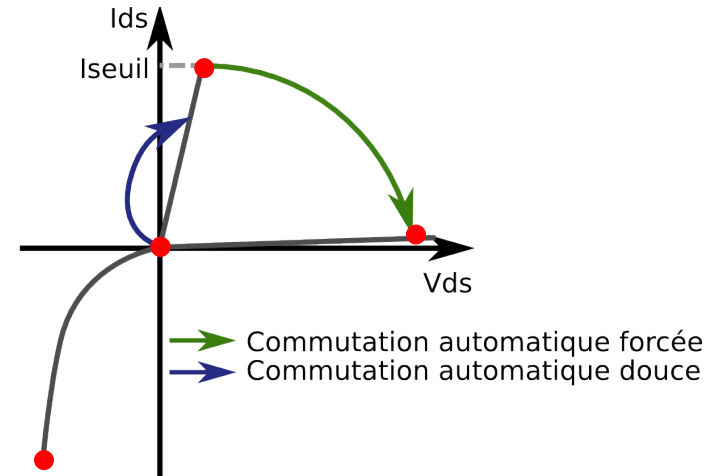
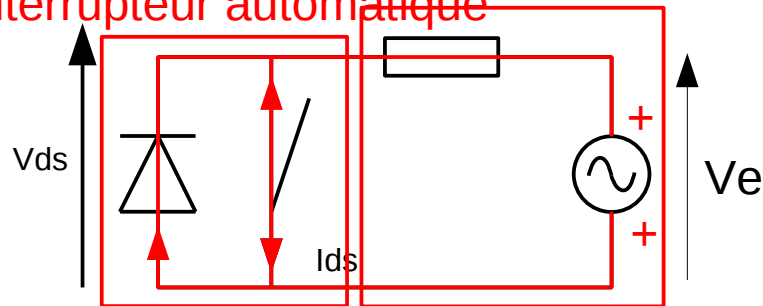




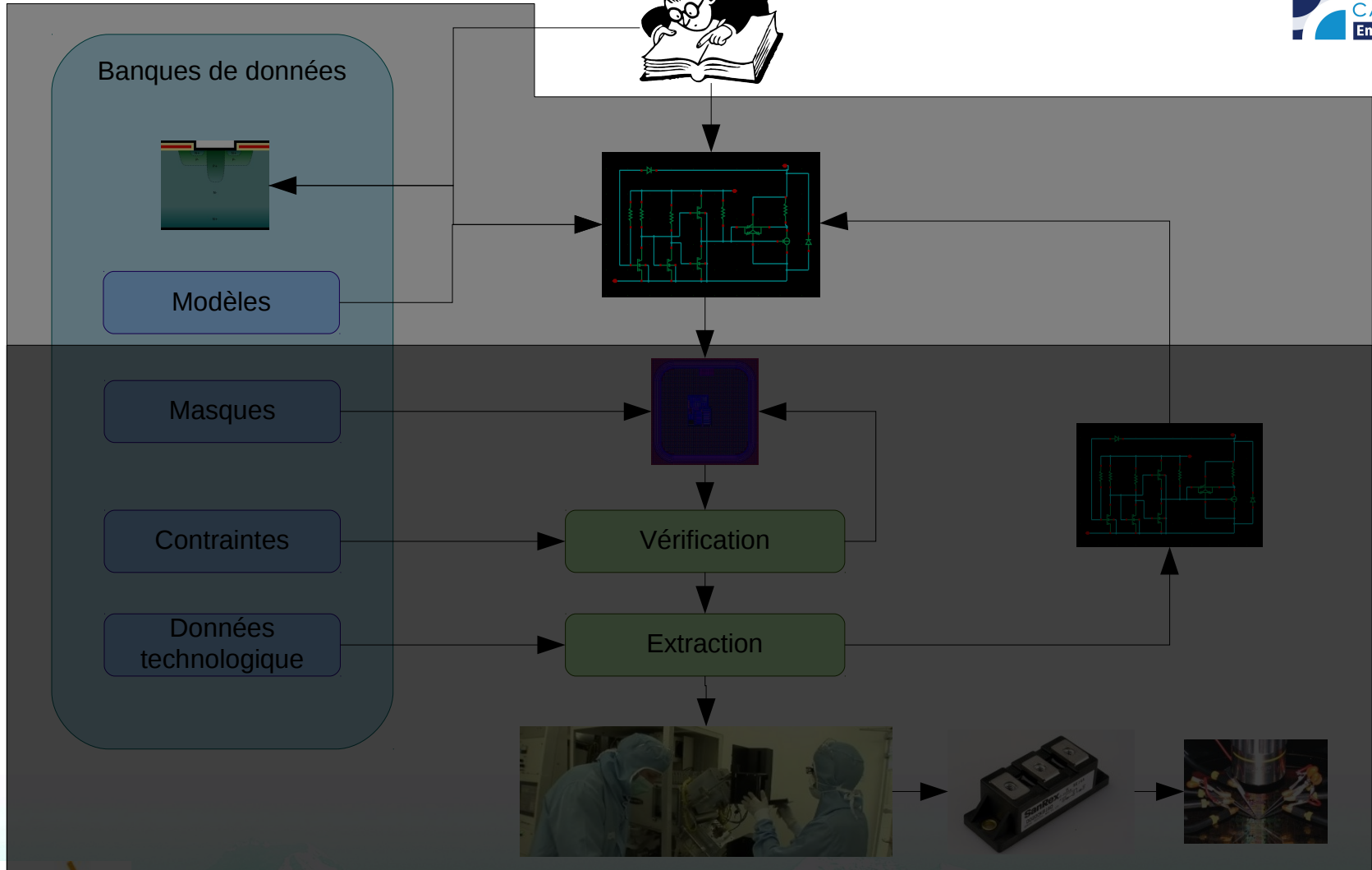


## Caractéristiques de l'interrupteur à commutation automatique

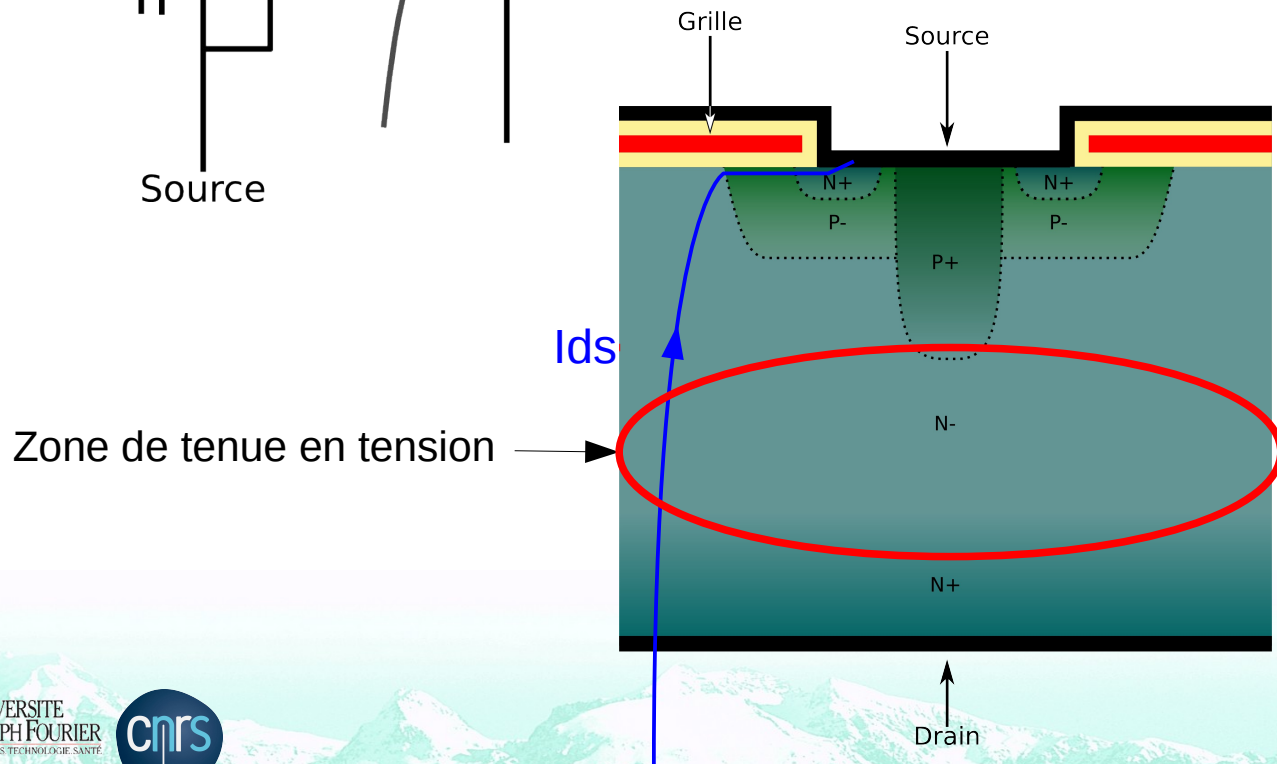
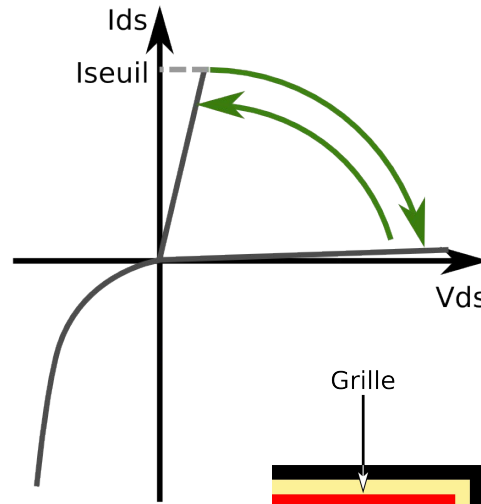
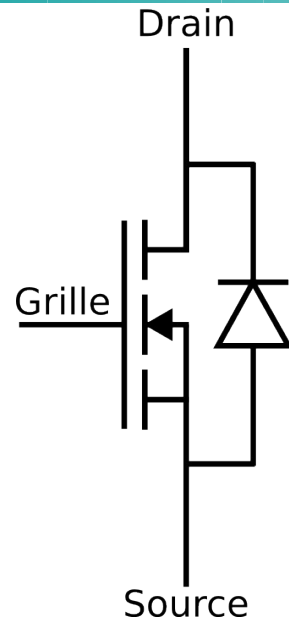
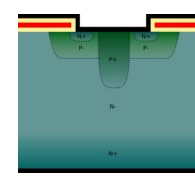
Interrupteur automatique



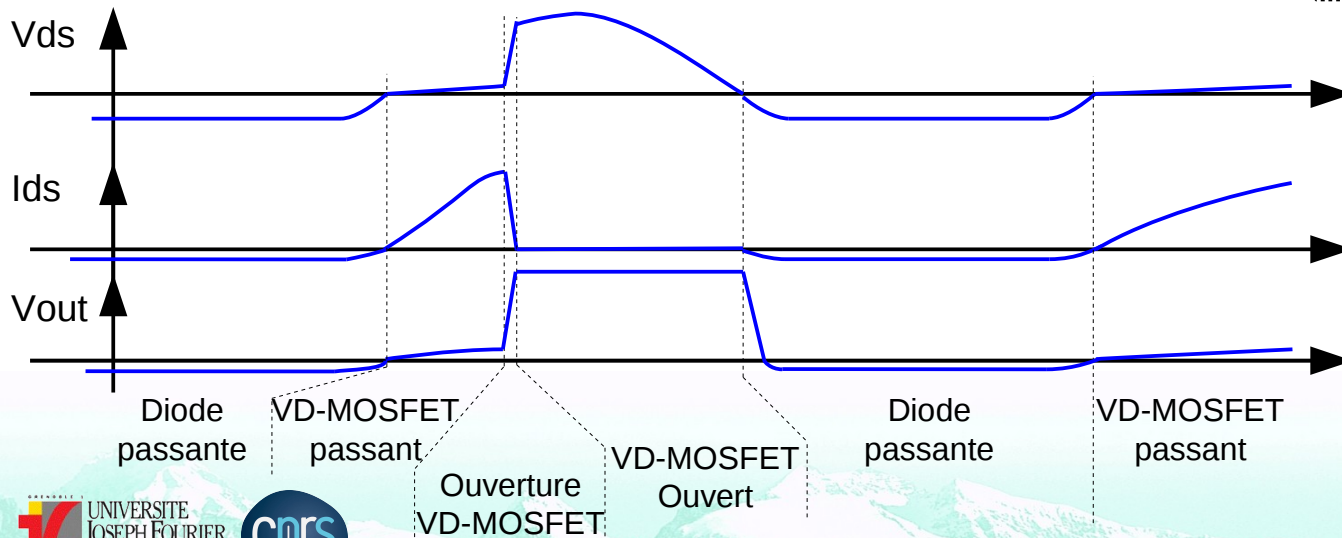
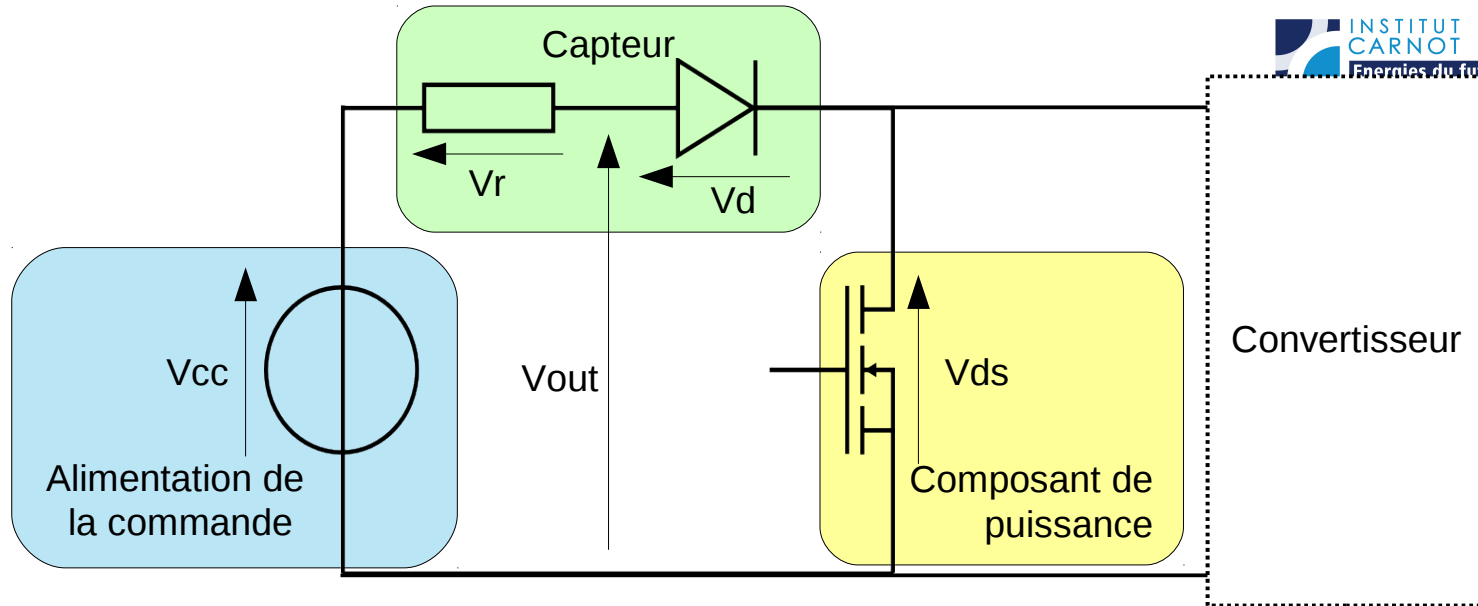
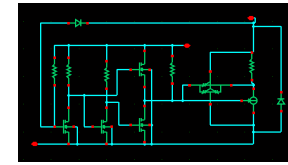
# Cheminement de conception



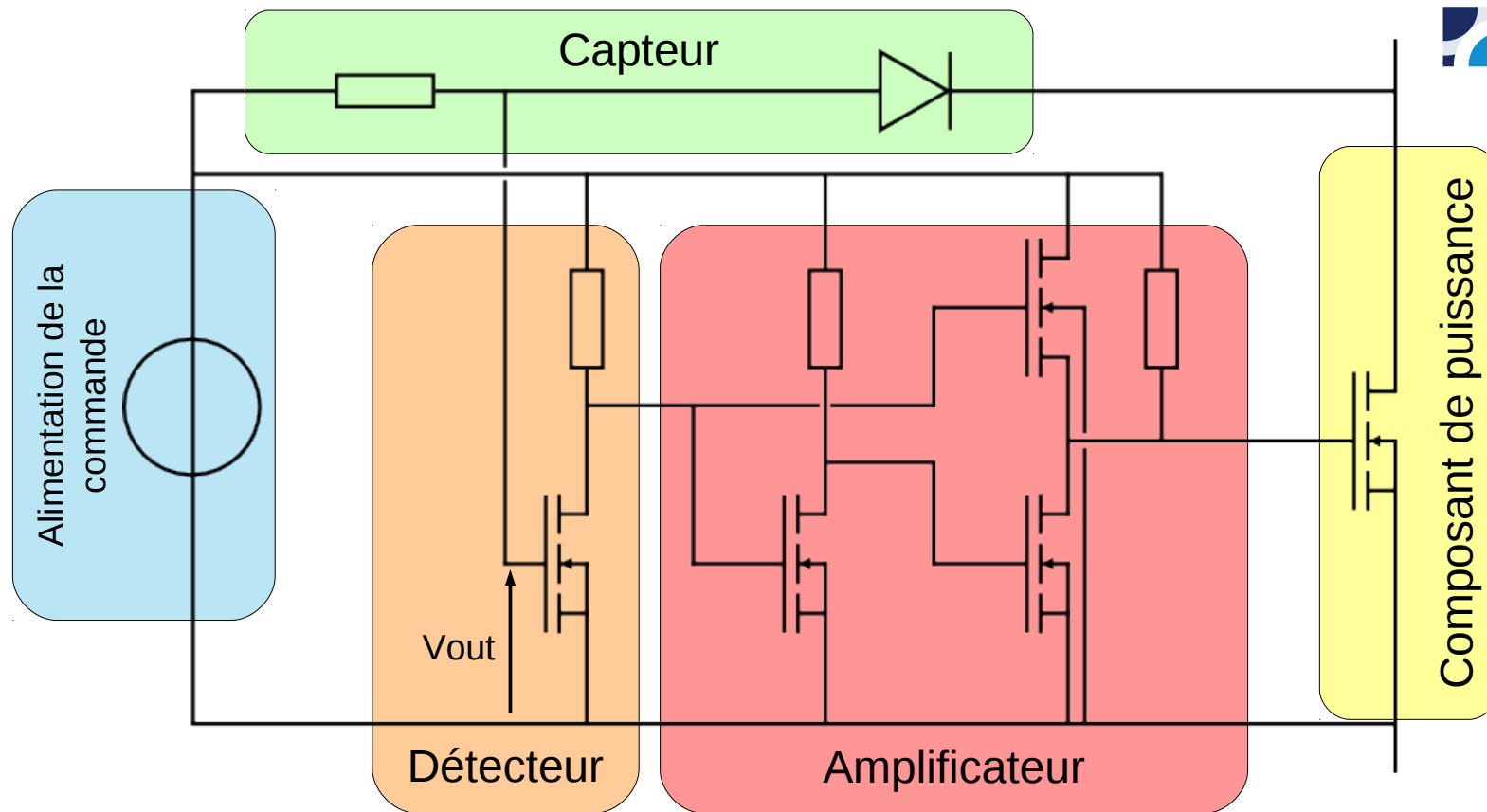
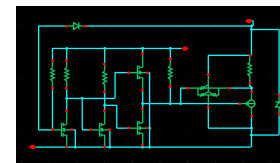
# Choix du cœur de puissance



# Capteur de tension

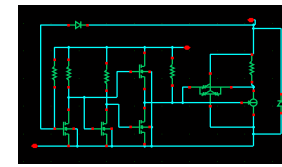


# Émulateur

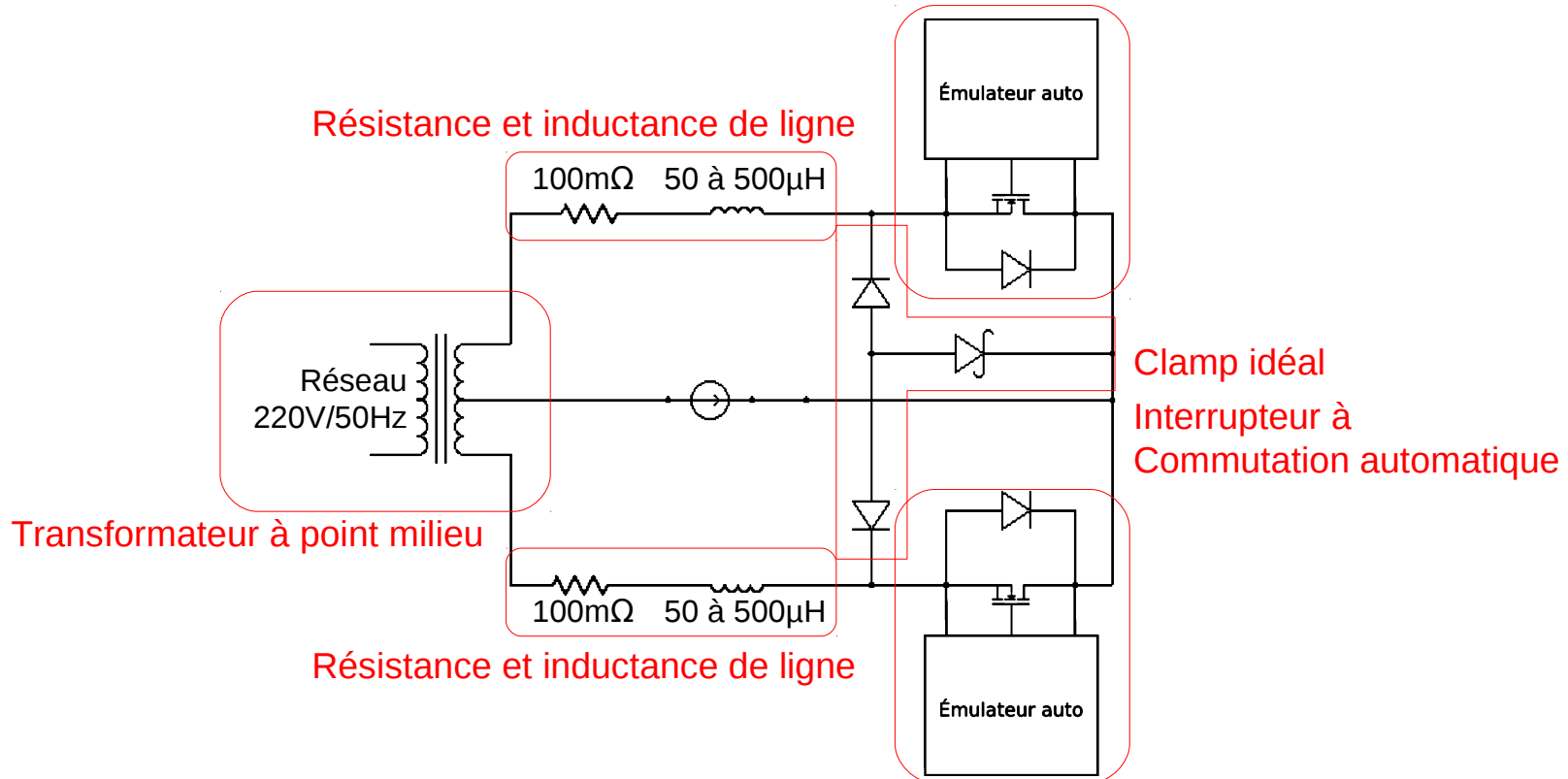


Dimensionnement des éléments : thèse Binh Nguyen  
Alimentation intégrable : thèse Nicolas Rouger

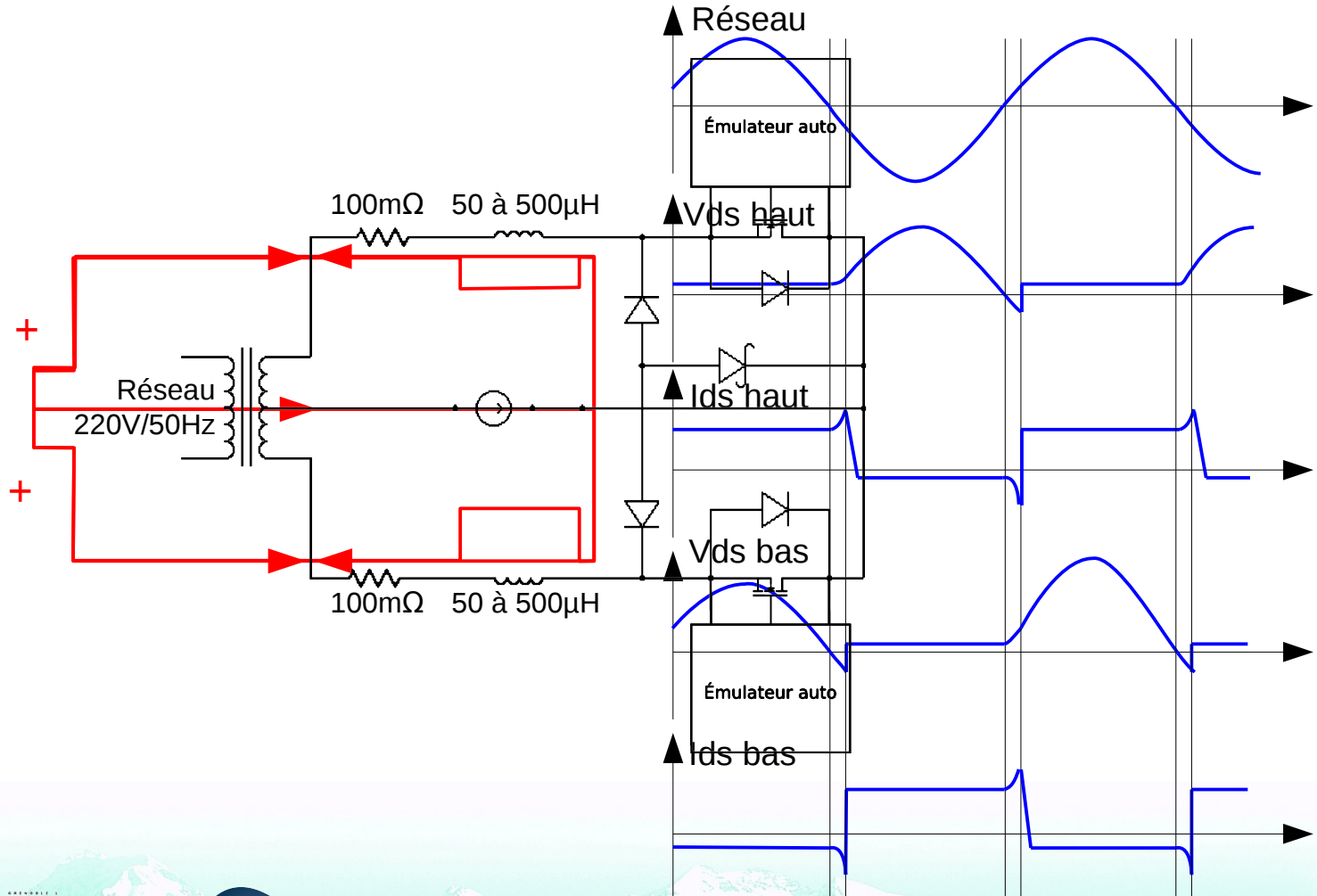
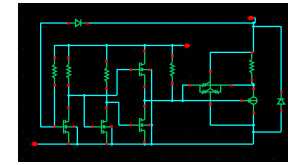
# Structure de simulation : présentation



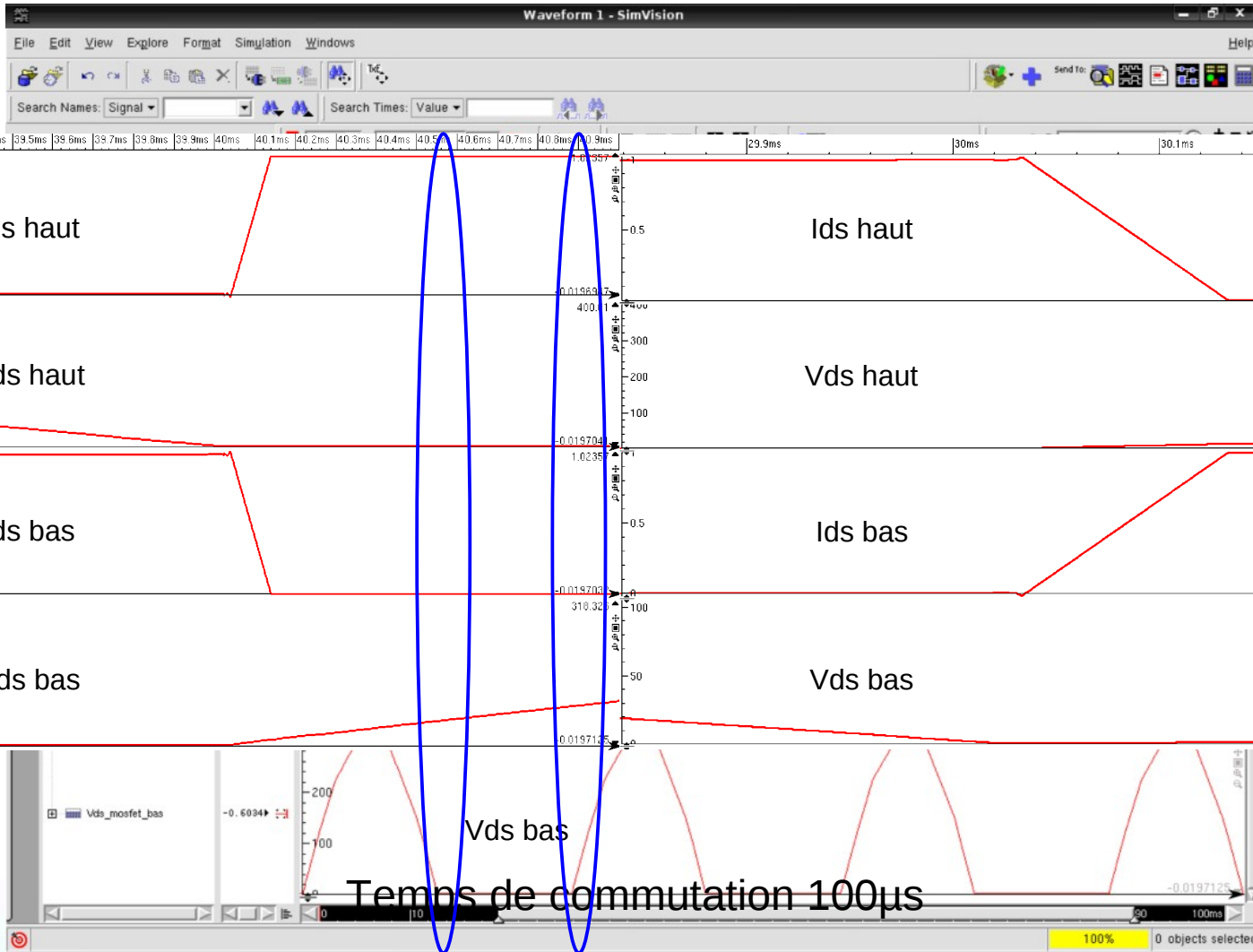
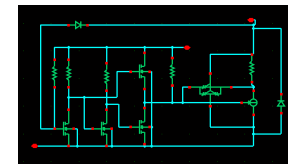
## Redresseur réversible



# Structure de test : fonctionnement

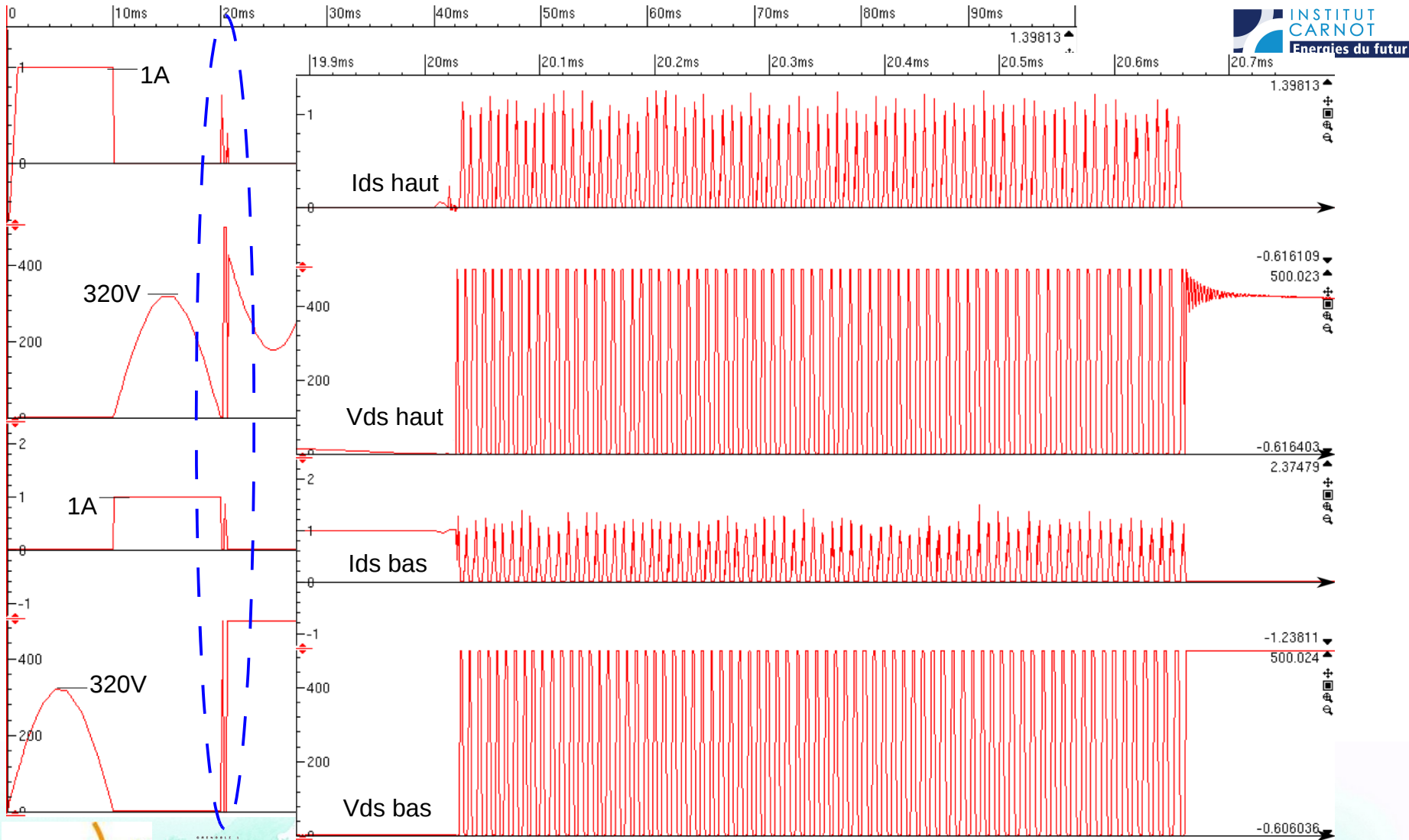
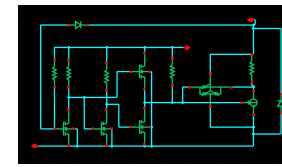


# Simulation des éléments fonctionnels des modèles

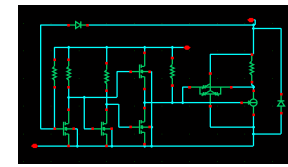




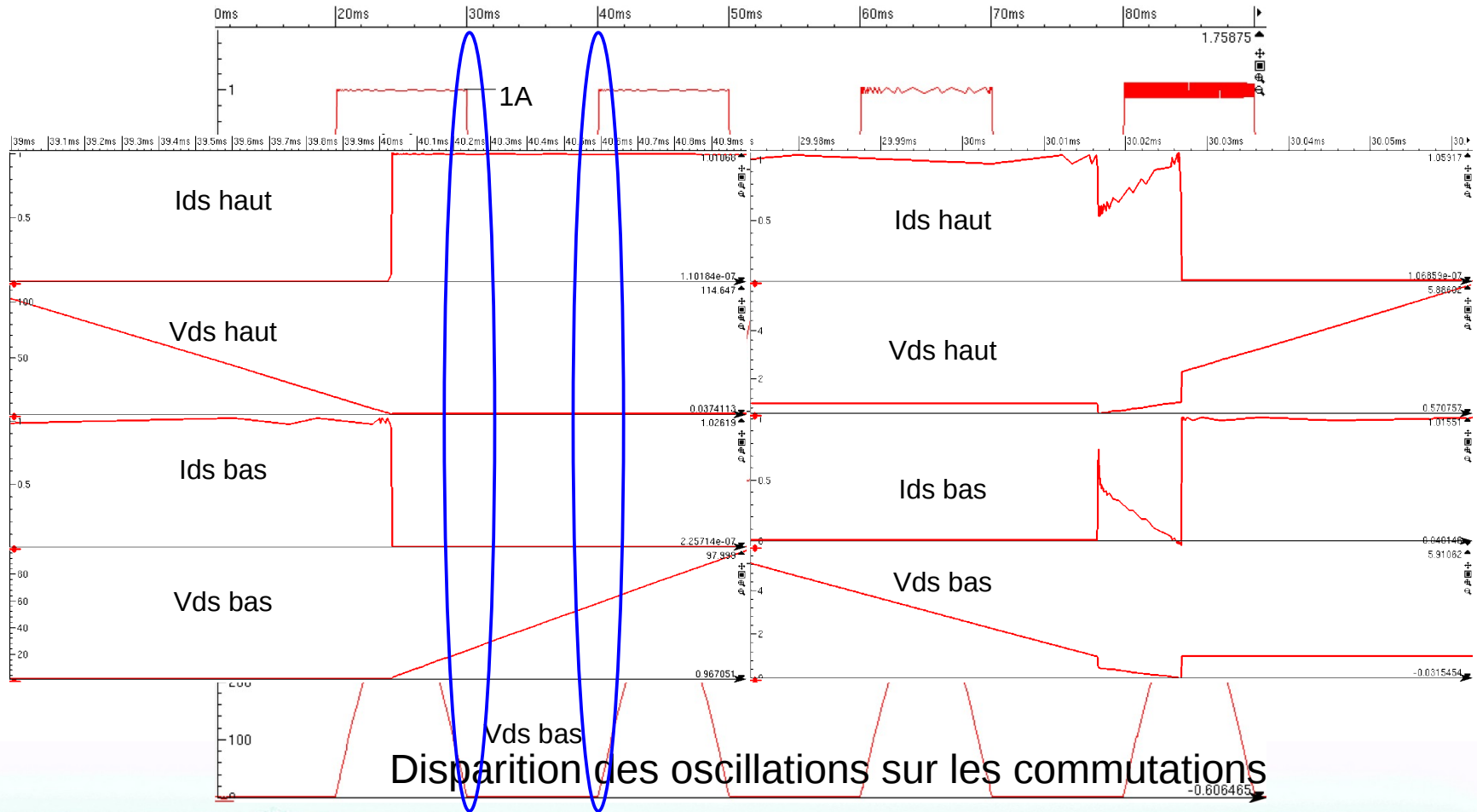
# Simulation des éléments parasites des modèles



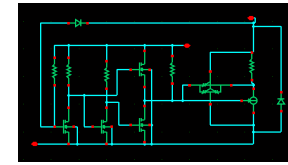
# Simulation des éléments parasites des modèles



Réduction de l'inductance de ligne  $50\mu\text{H} \Rightarrow 50\text{nH}$

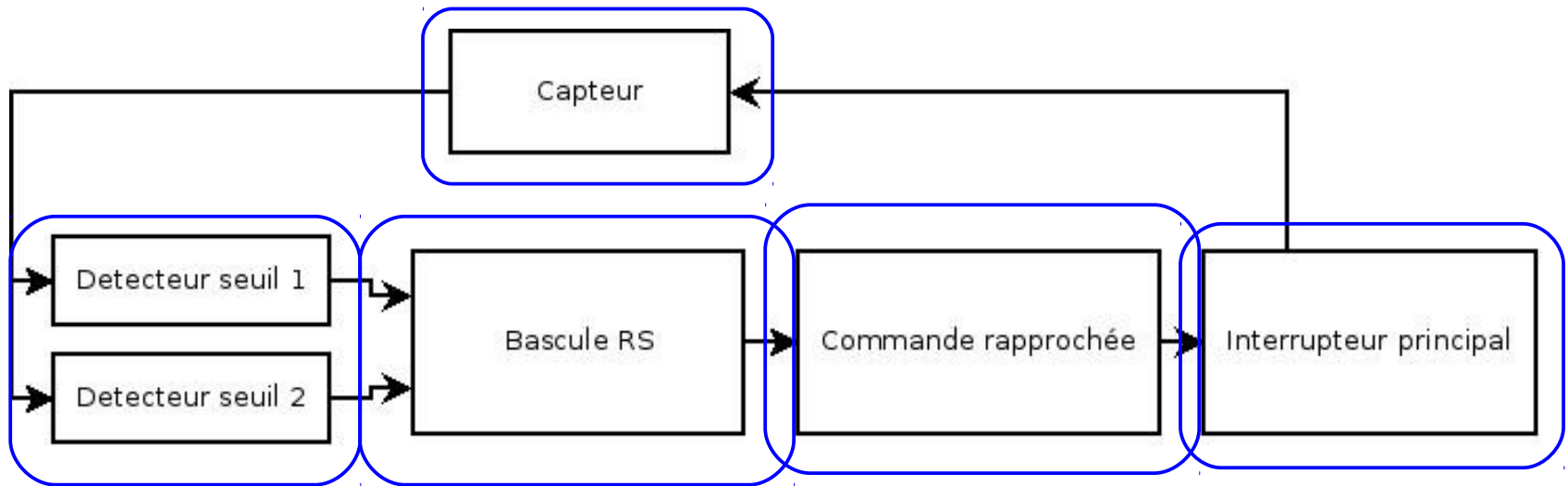
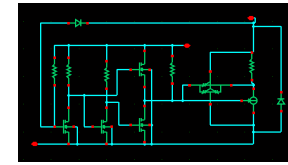


# Source des oscillations

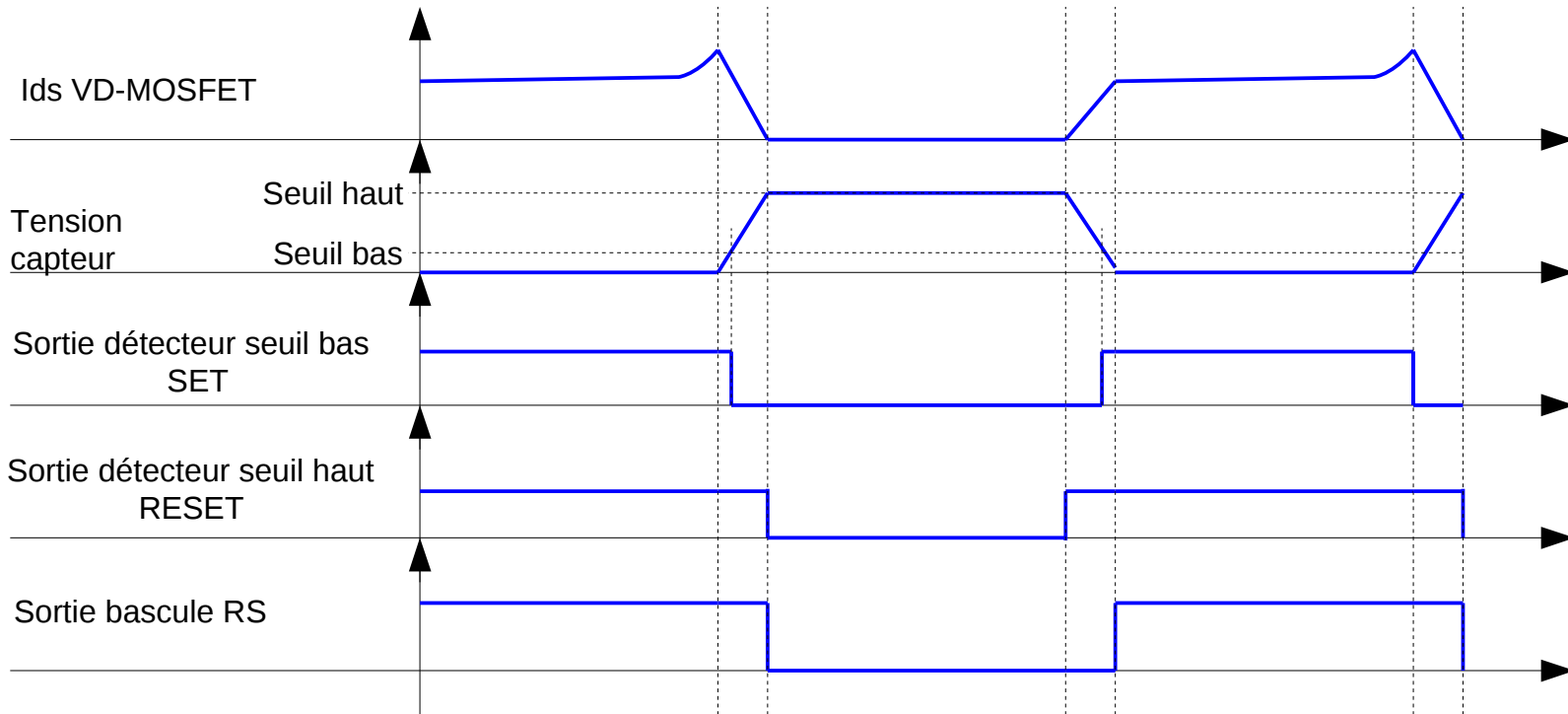
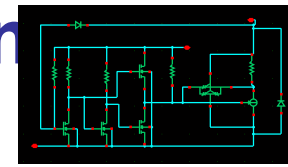


- Problème d'oscillation dû à l'inductance de ligne et aux éléments parasites
- Solution :
  - Temporisation
  - Snubber
  - Hystérésis

# Solution par hystérésis



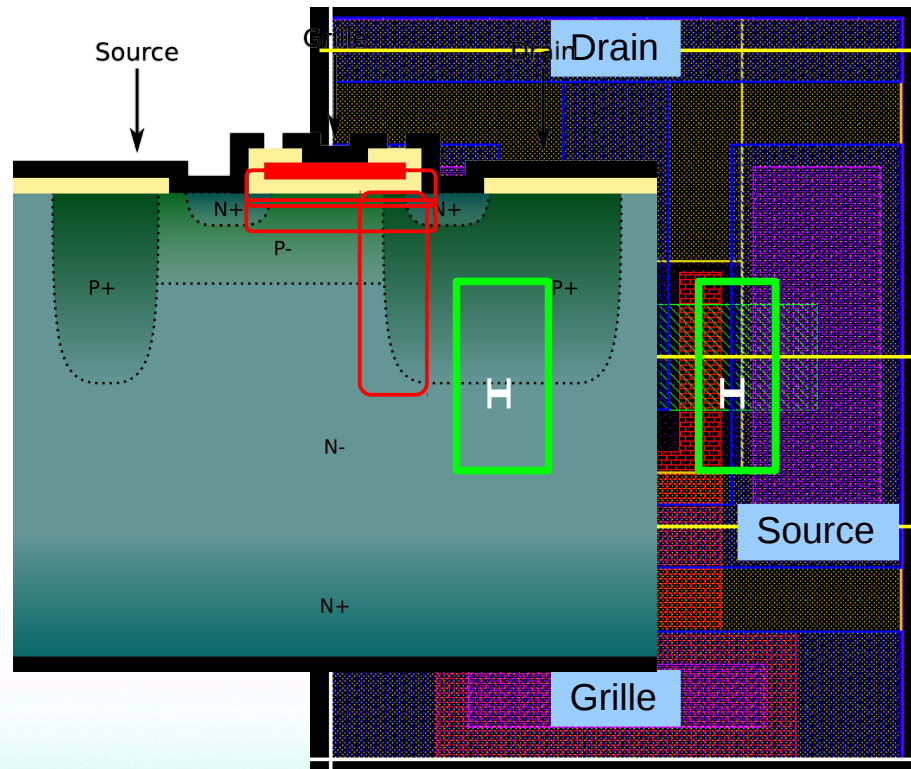
# Fonctionnement de la solution à cycle d'hystérésis



# Détecteur à seuil bas

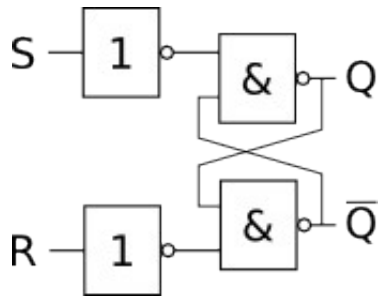
Banques de données

$$V_{th} = \varphi_{ms} + \frac{2,0 \cdot (k \cdot Temp)}{q} \cdot \log\left(\frac{P_m}{n_i}\right) + \frac{\left( \frac{2,0 \cdot q \cdot P_m \cdot \epsilon_{si} \cdot \epsilon_0 \cdot 2,0 \cdot (k \cdot Temp)}{q} \cdot \log\left(\frac{P_m}{n_i}\right) \right)}{\left( \frac{\epsilon_{si} \cdot \epsilon_0}{h_{ox}} \right)}$$

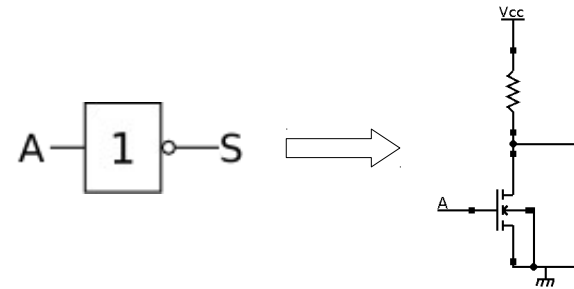


# Intégration de portes logiques

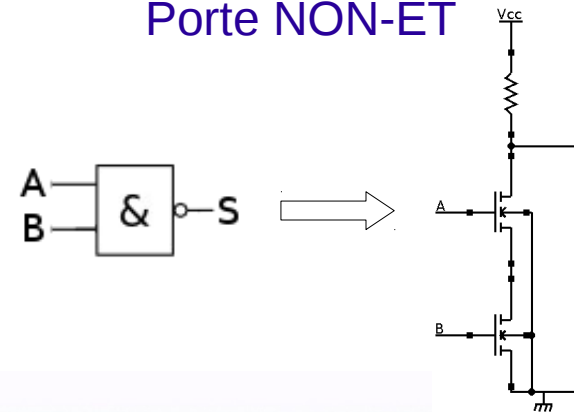
## Diagramme d'une bascule RS



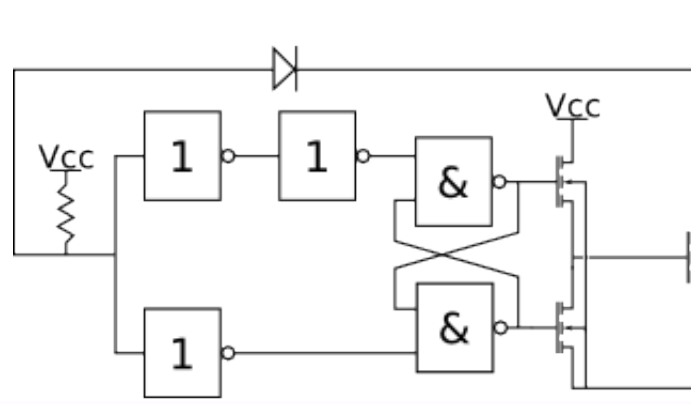
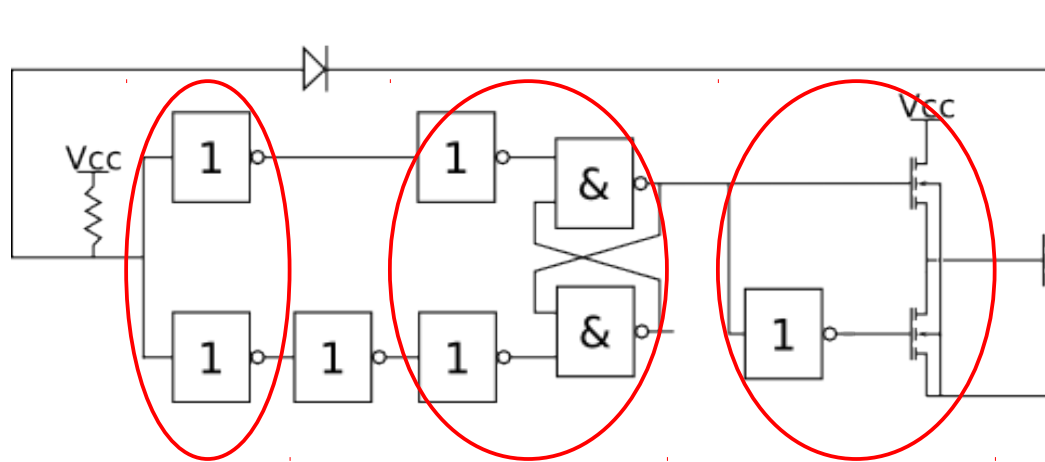
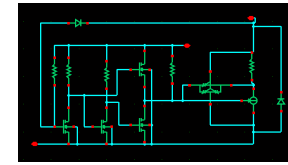
## Porte inverseuse



## Porte NON-ET

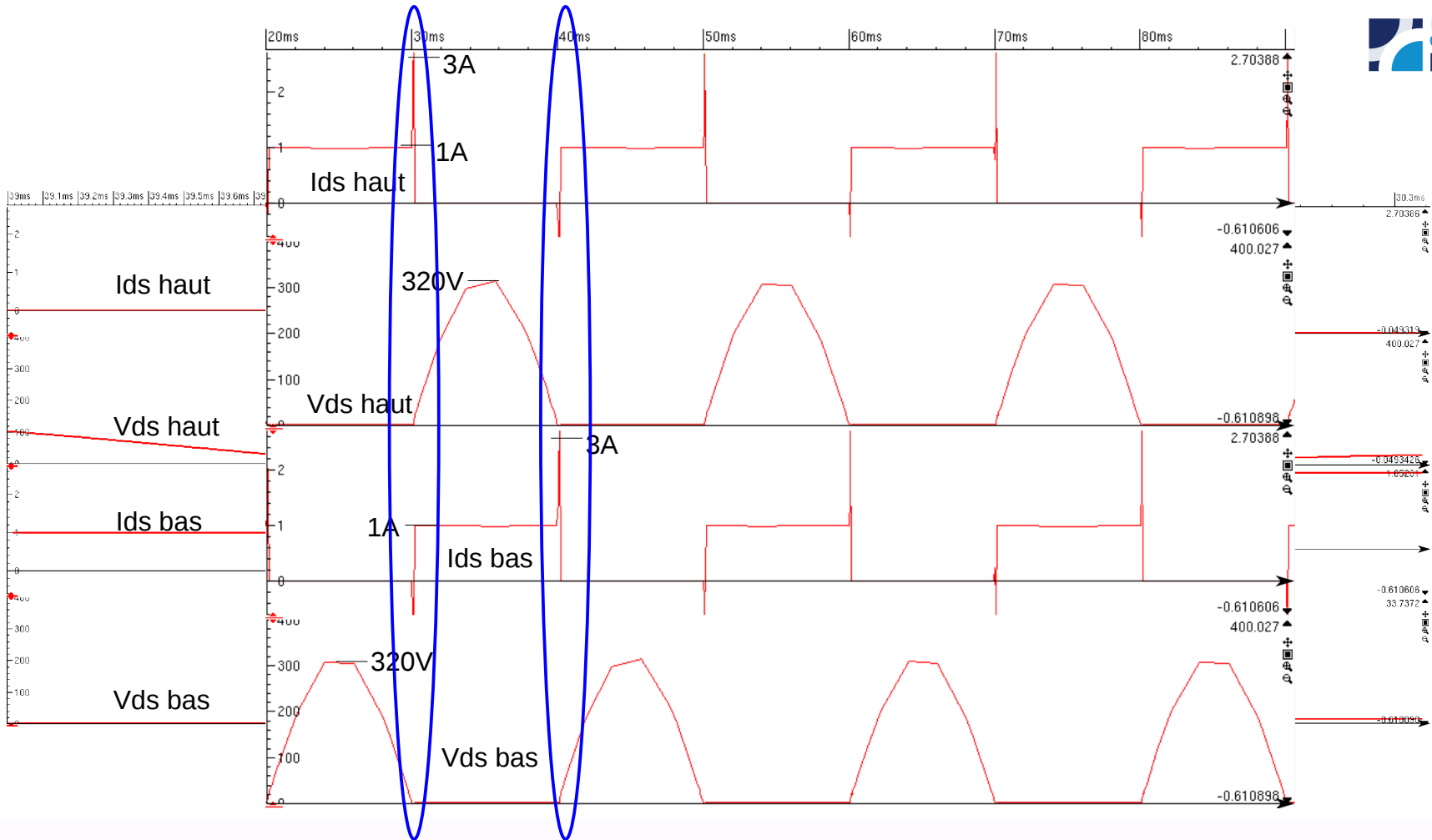
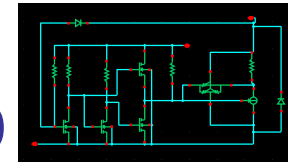


# Schématique logique v2.0

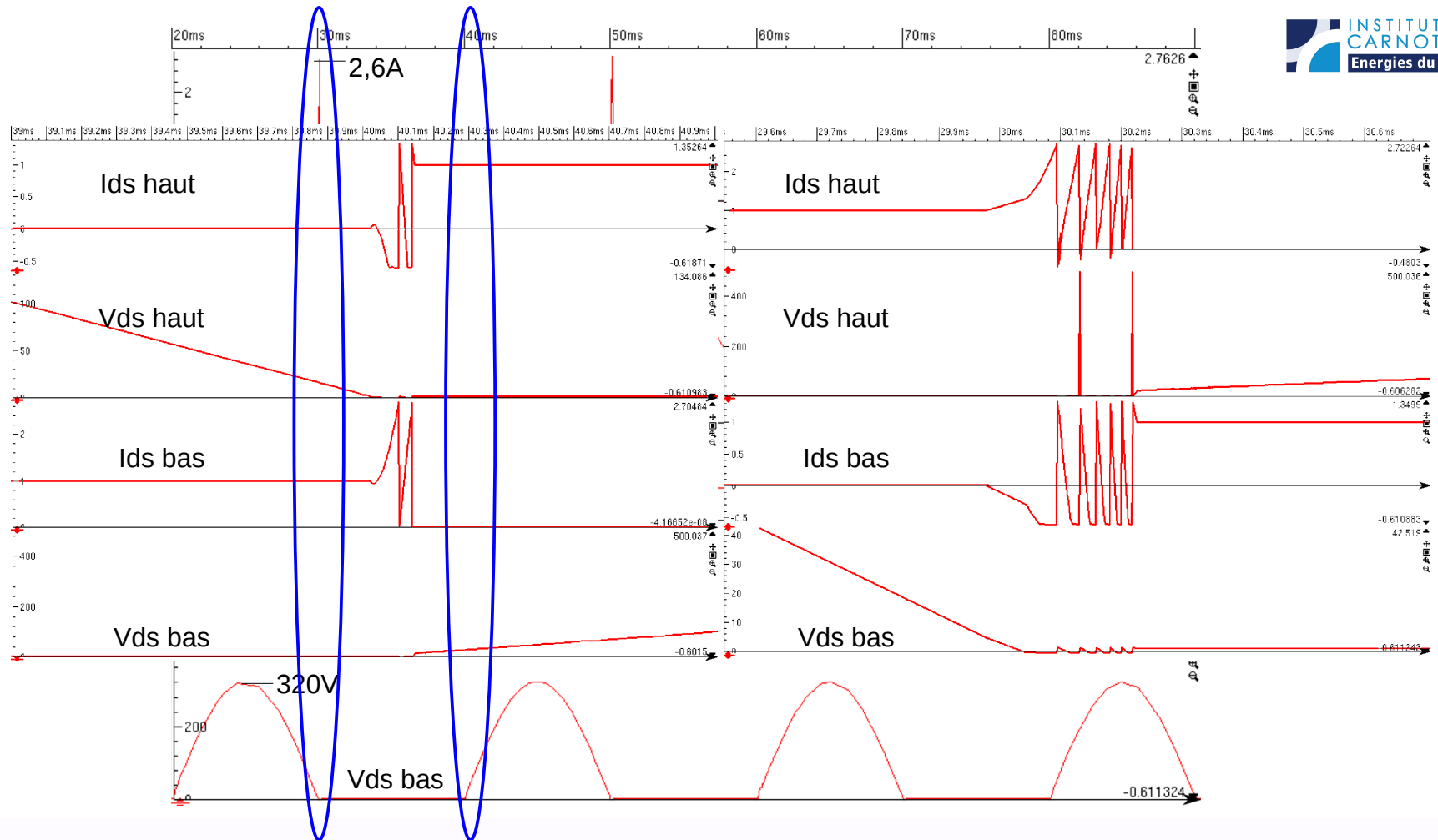
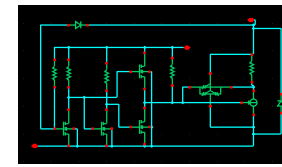




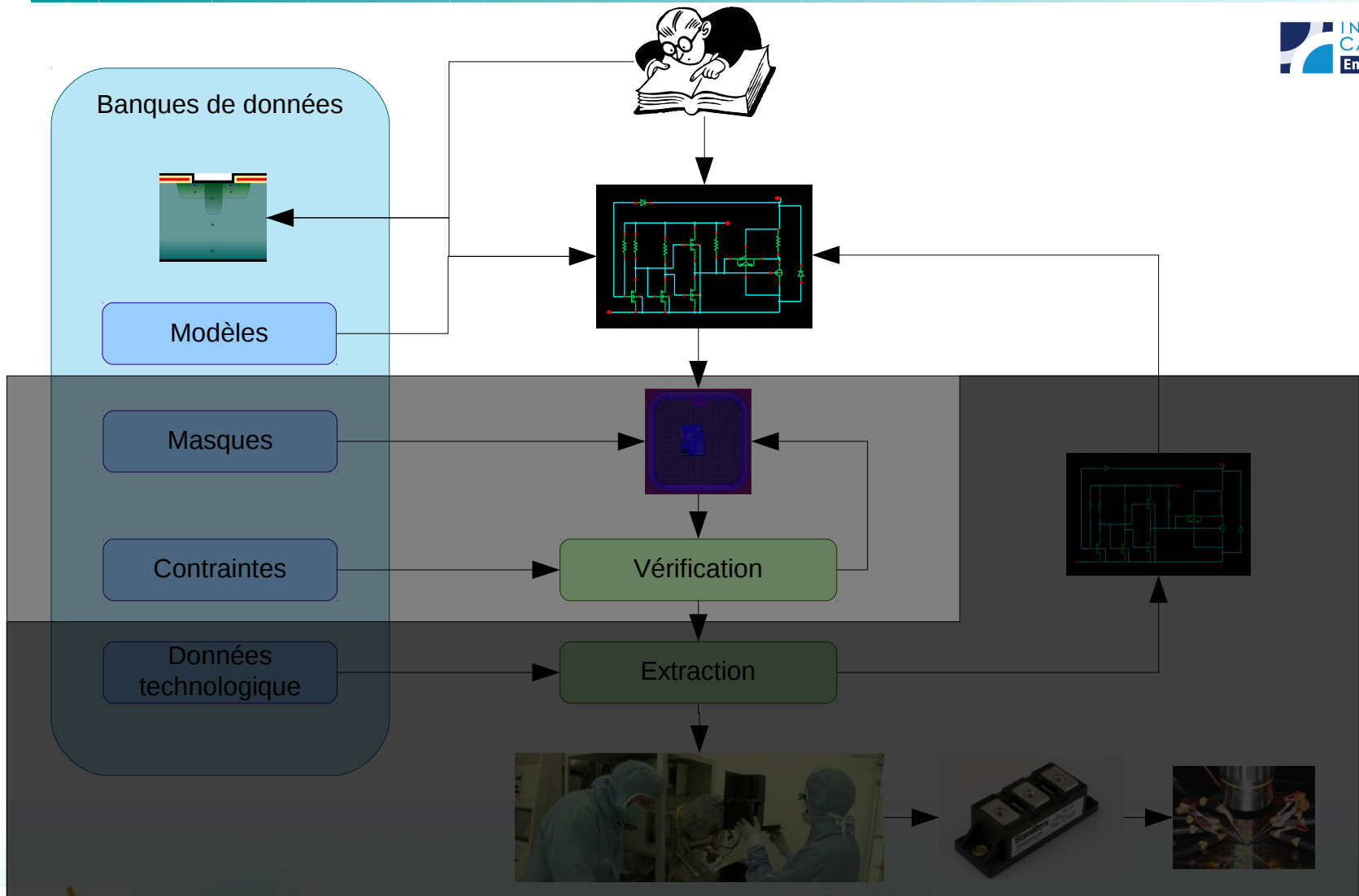
# Simulation des éléments fonctionnels des modèles v2.0



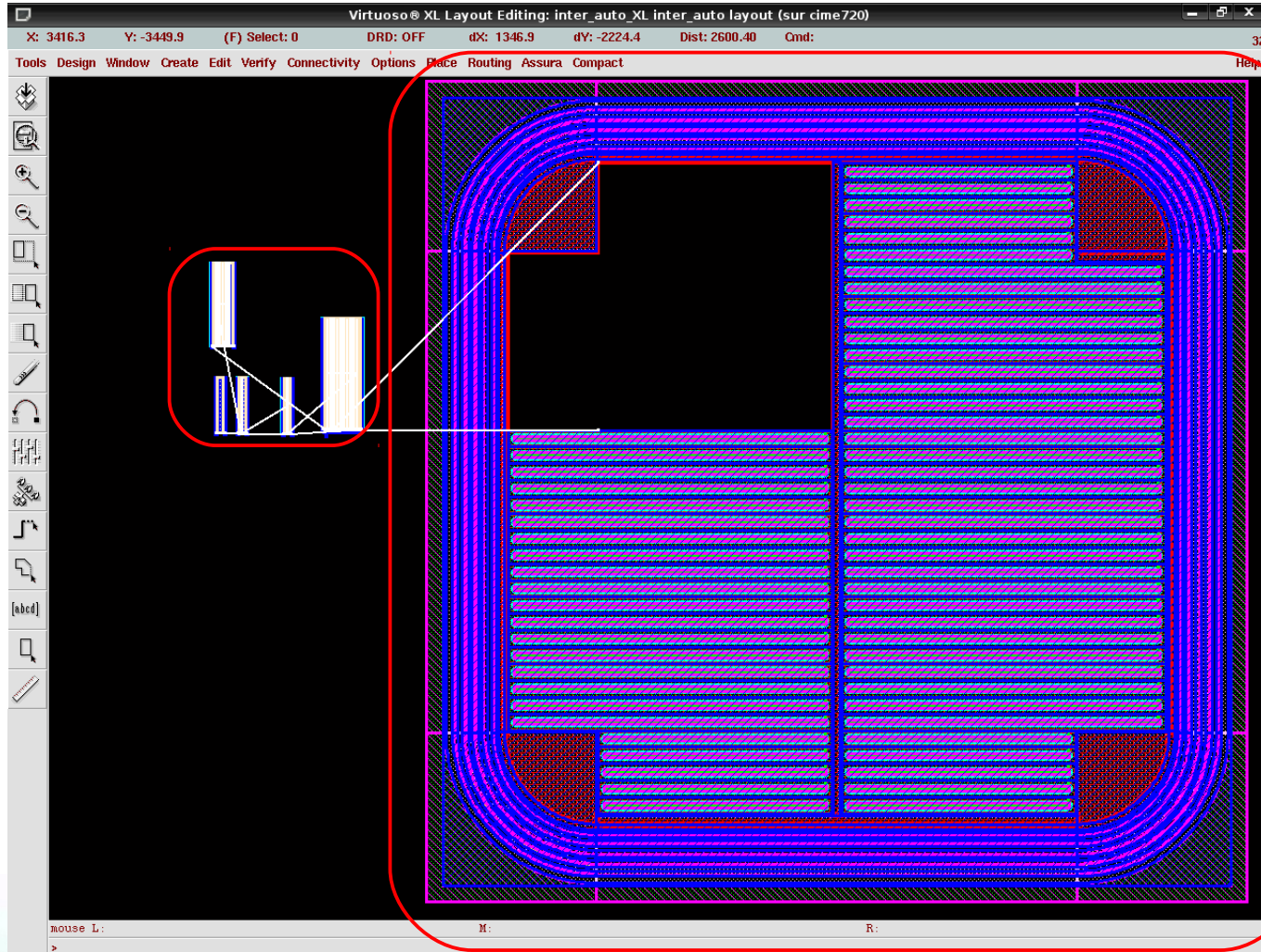
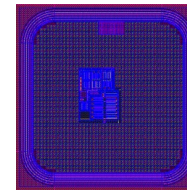
# Simulation des éléments parasites des modèles v2.0



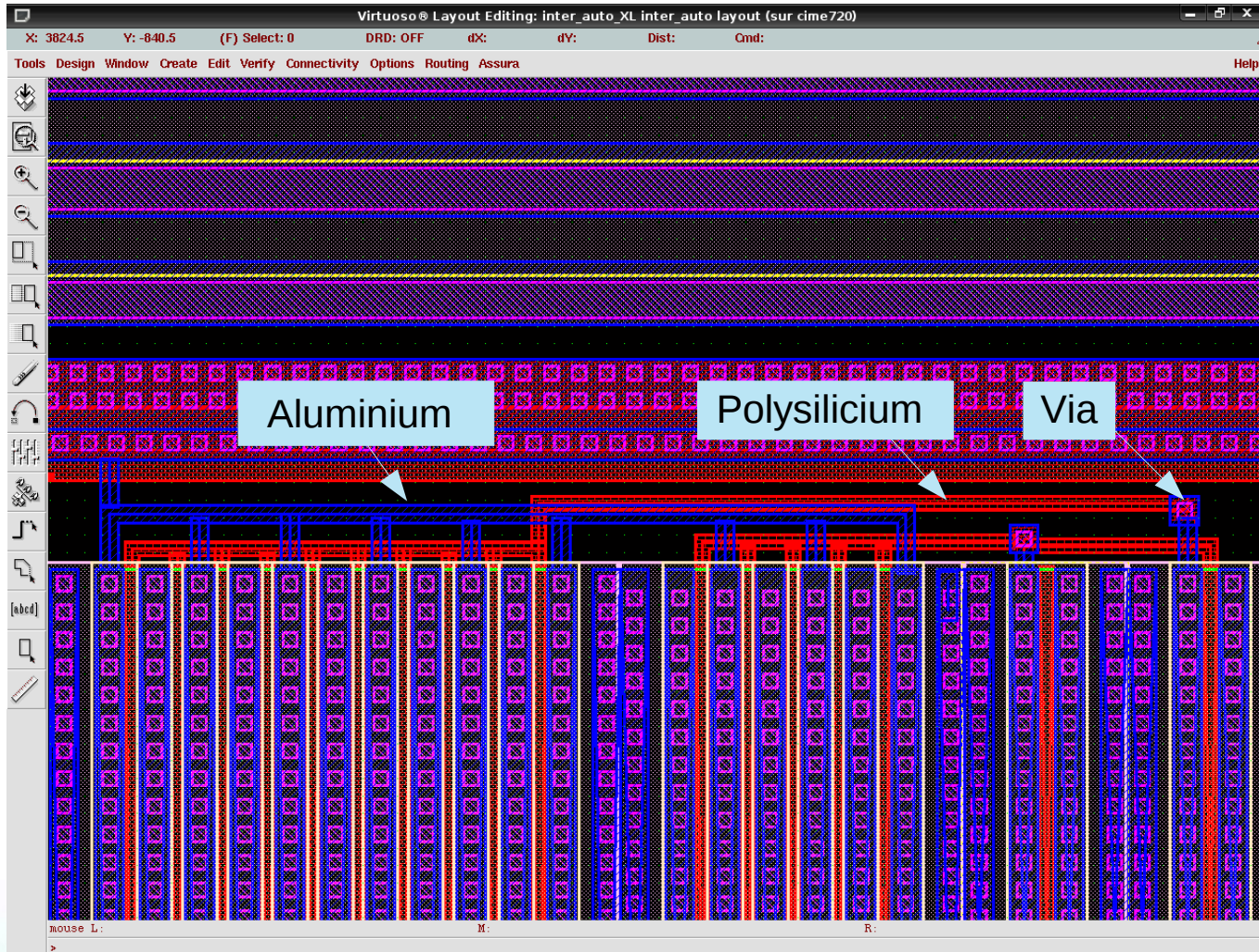
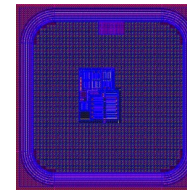
# Cheminement de conception



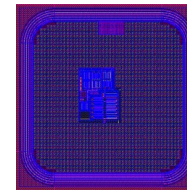
# Génération des masques



# Placement et routage



# Composant final

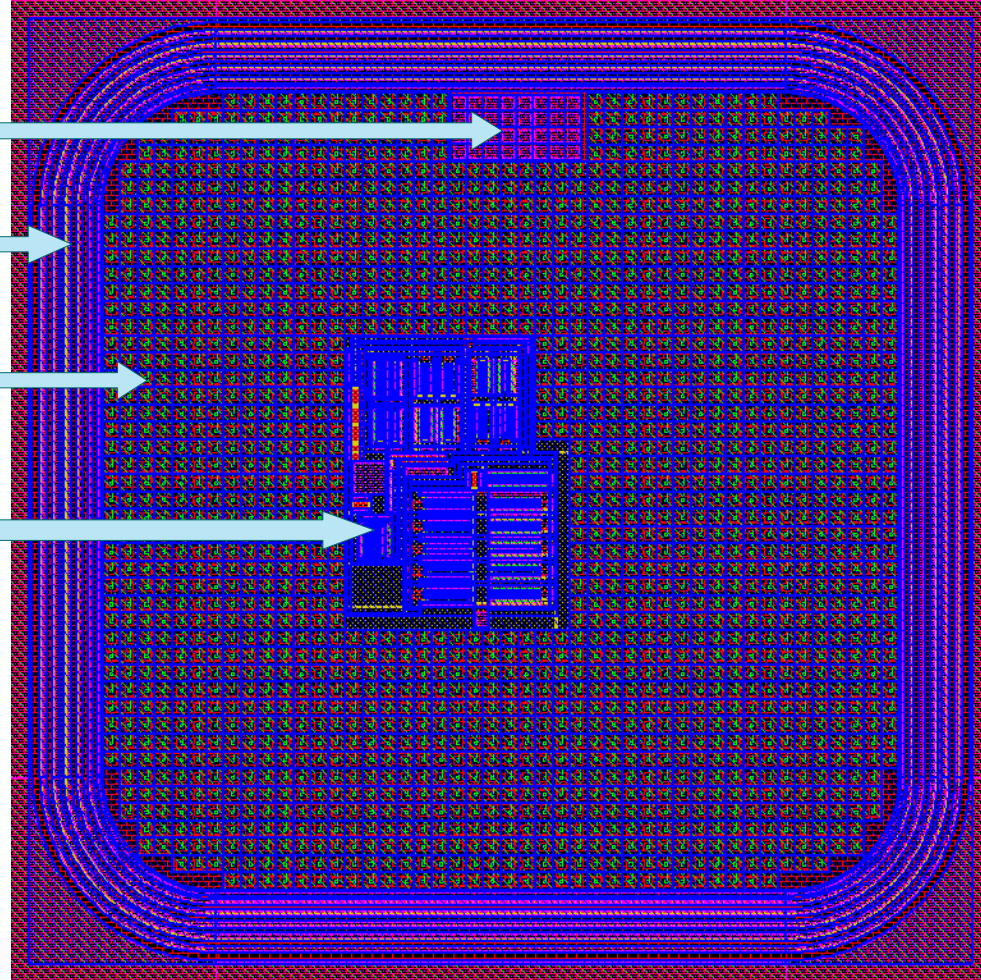


Plôt de contact de grille

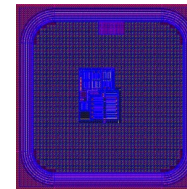
Périphérie

Cellule VD-MOSFET

Émulateur



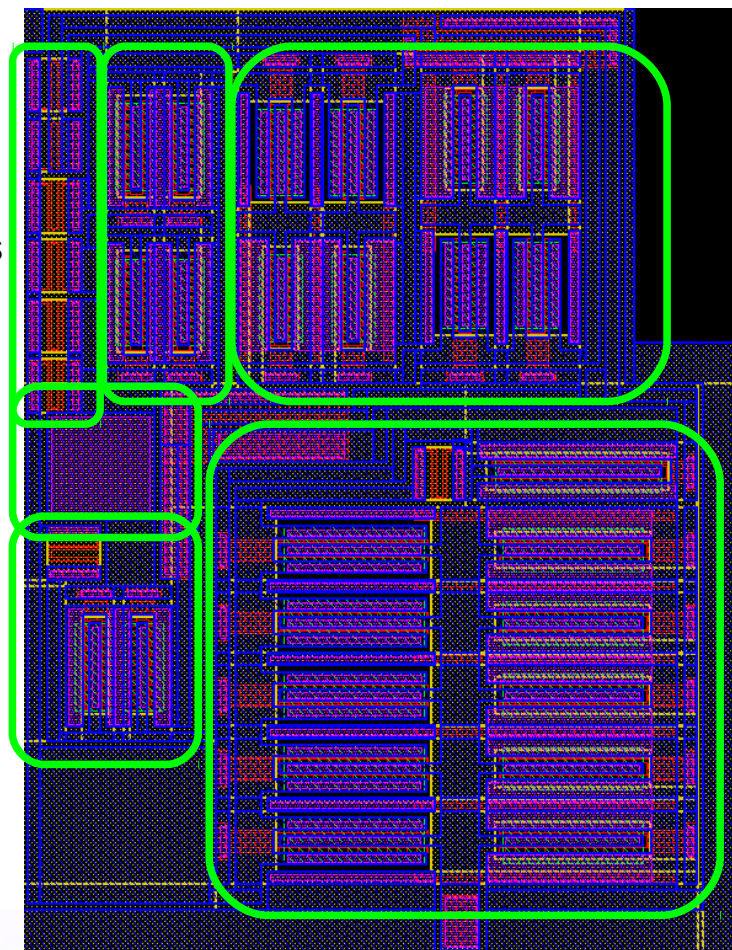
# Émulateur



LD-Resistance de charges

Diode du capteur

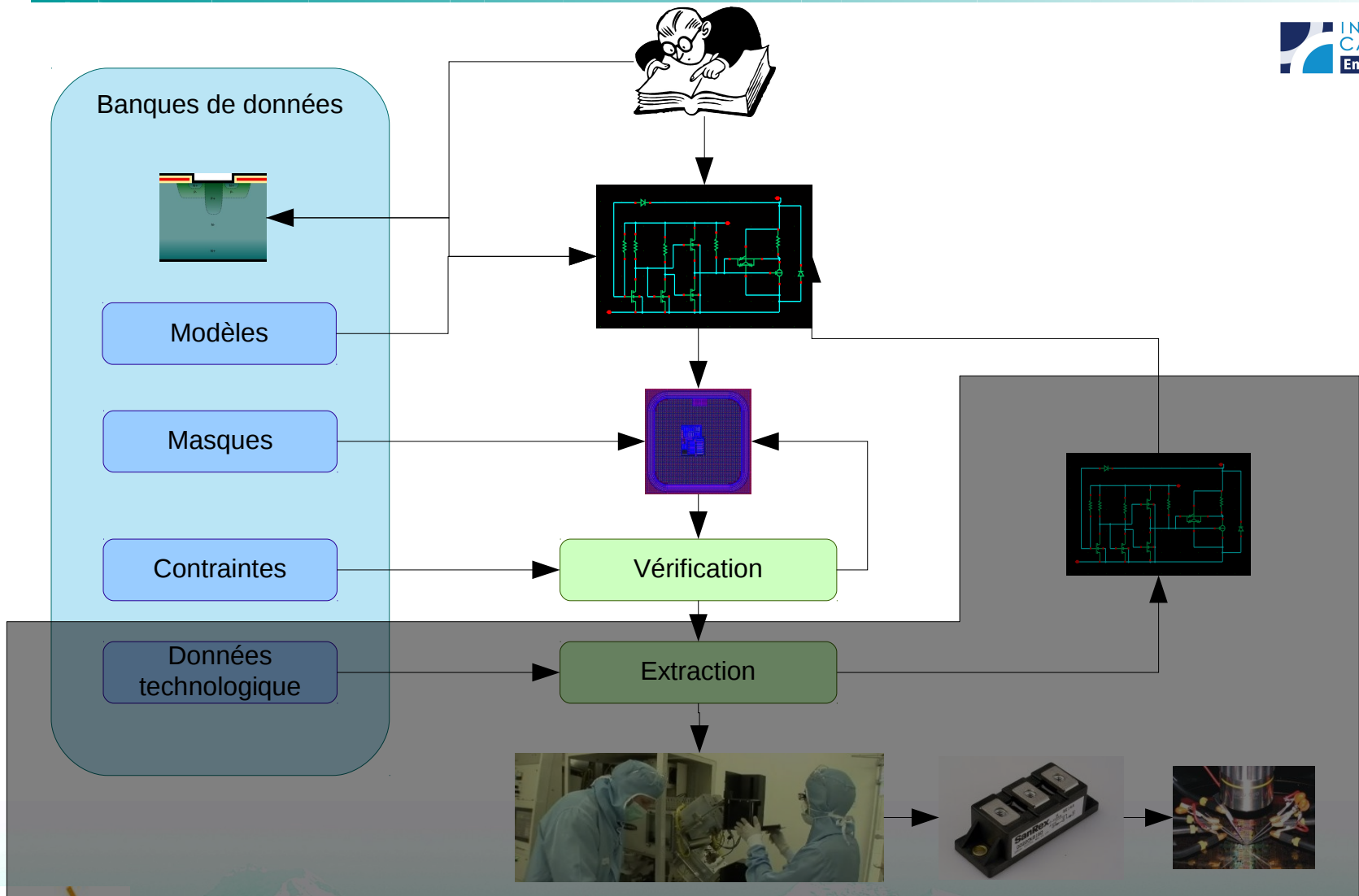
Inverseur a seuil haut



Bascule RS

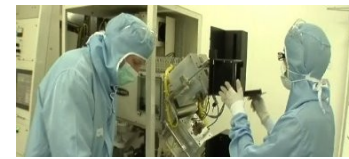
Push-Pull

# Cheminement de conception





# Prototypes réalisés

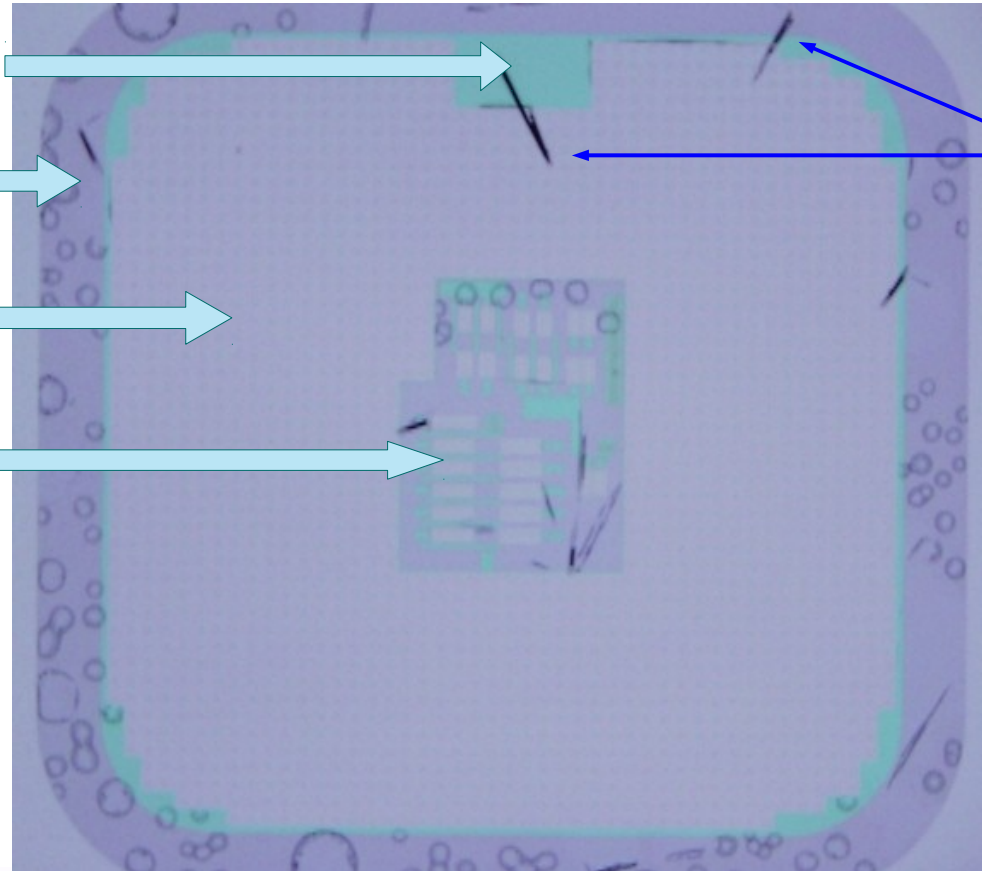


Plôt de contact de grille

Périphérie

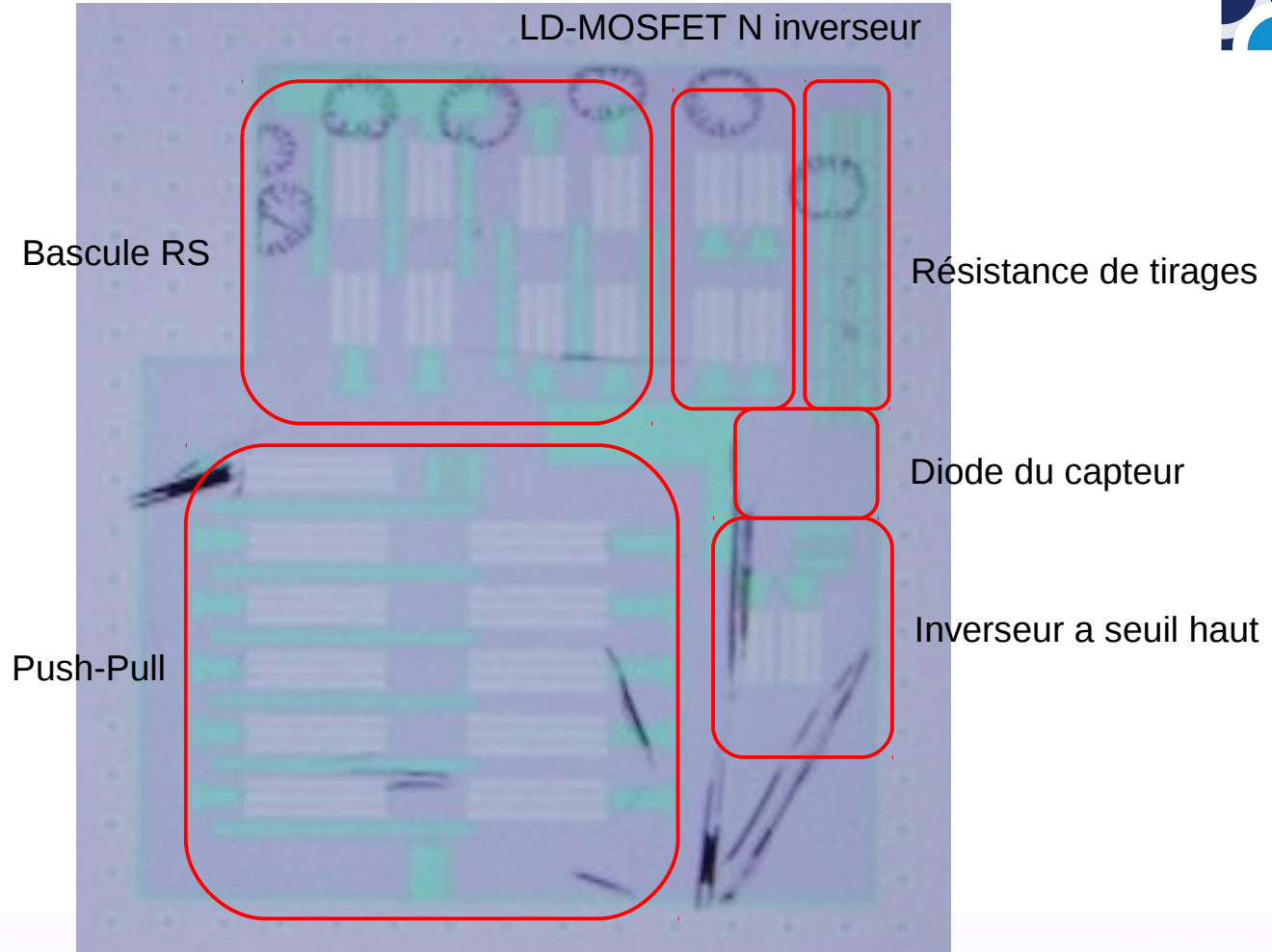
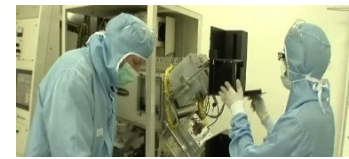
Cellule VD-MOSFET

Émulateur

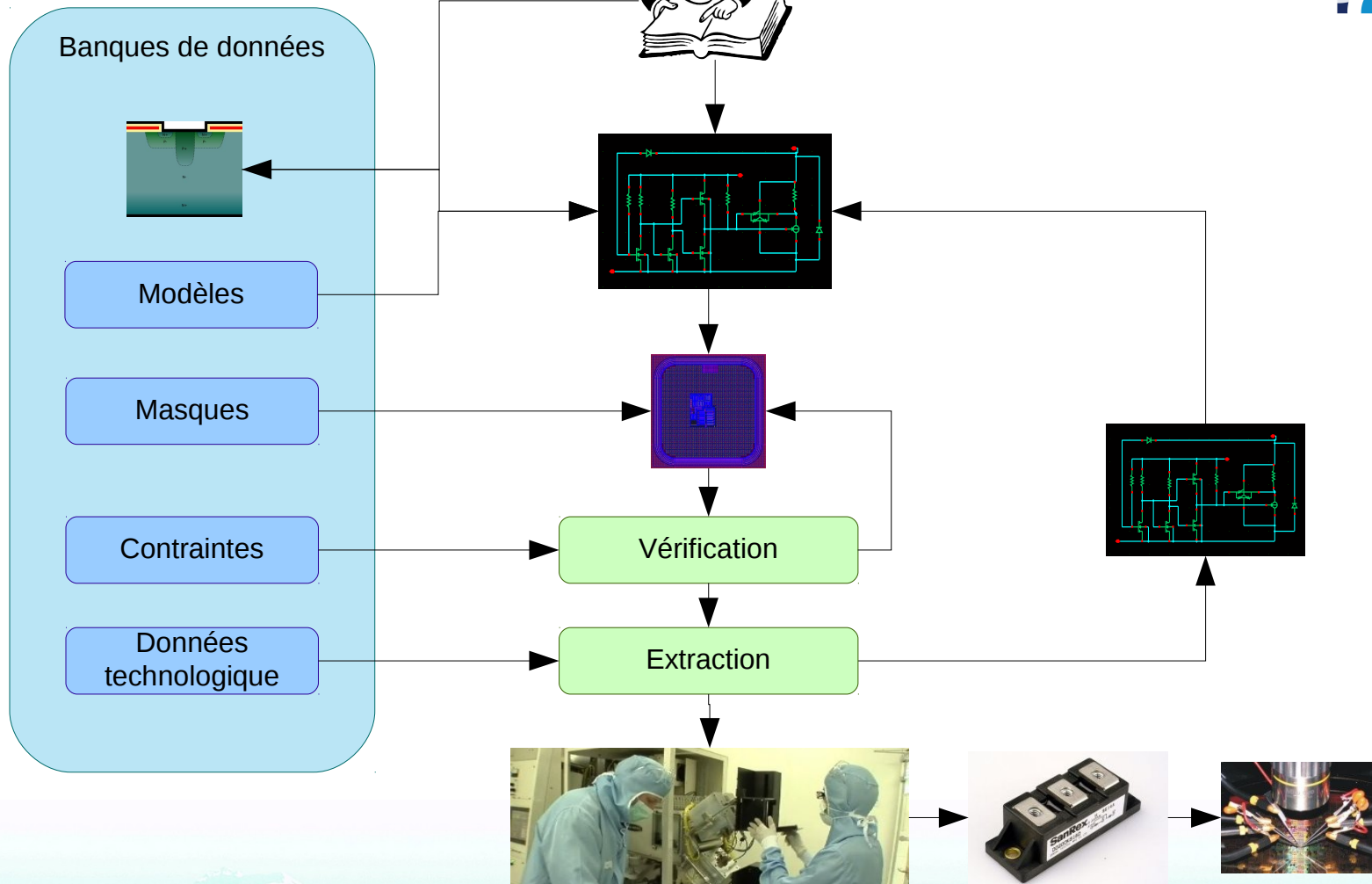


Reste de résine

# Zoom de l'émulateur

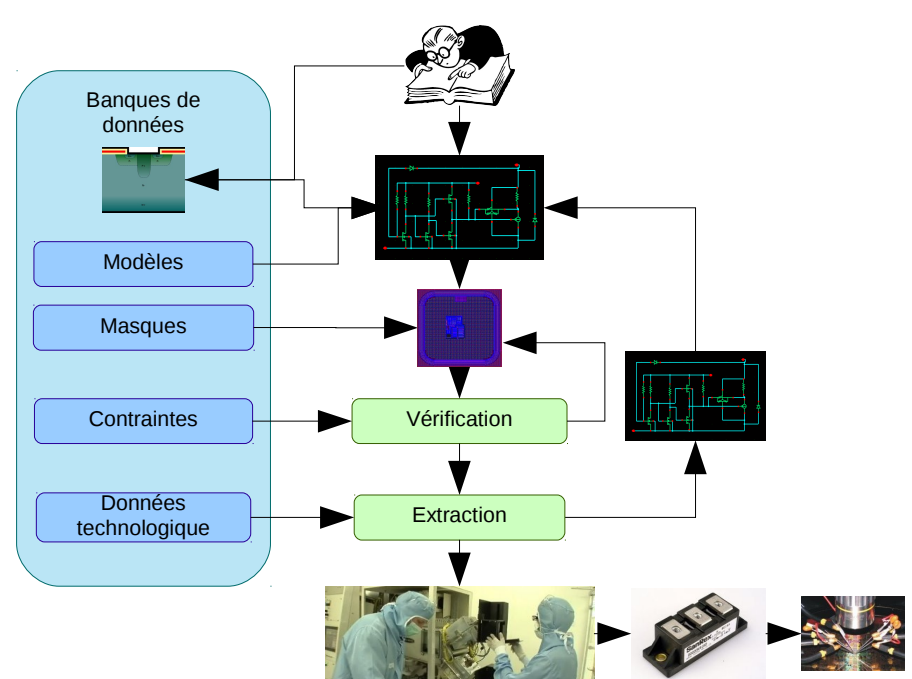
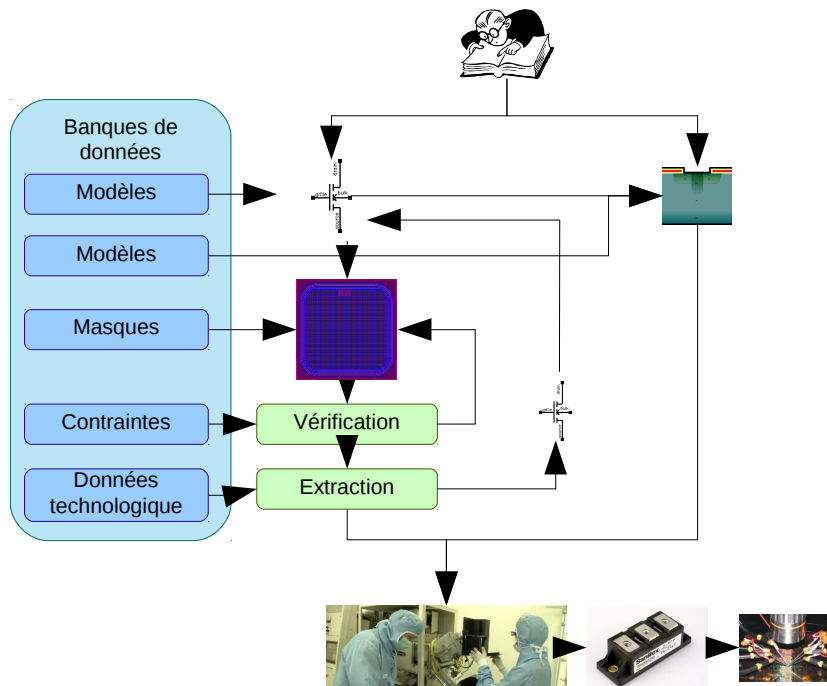


# Cheminement de conception

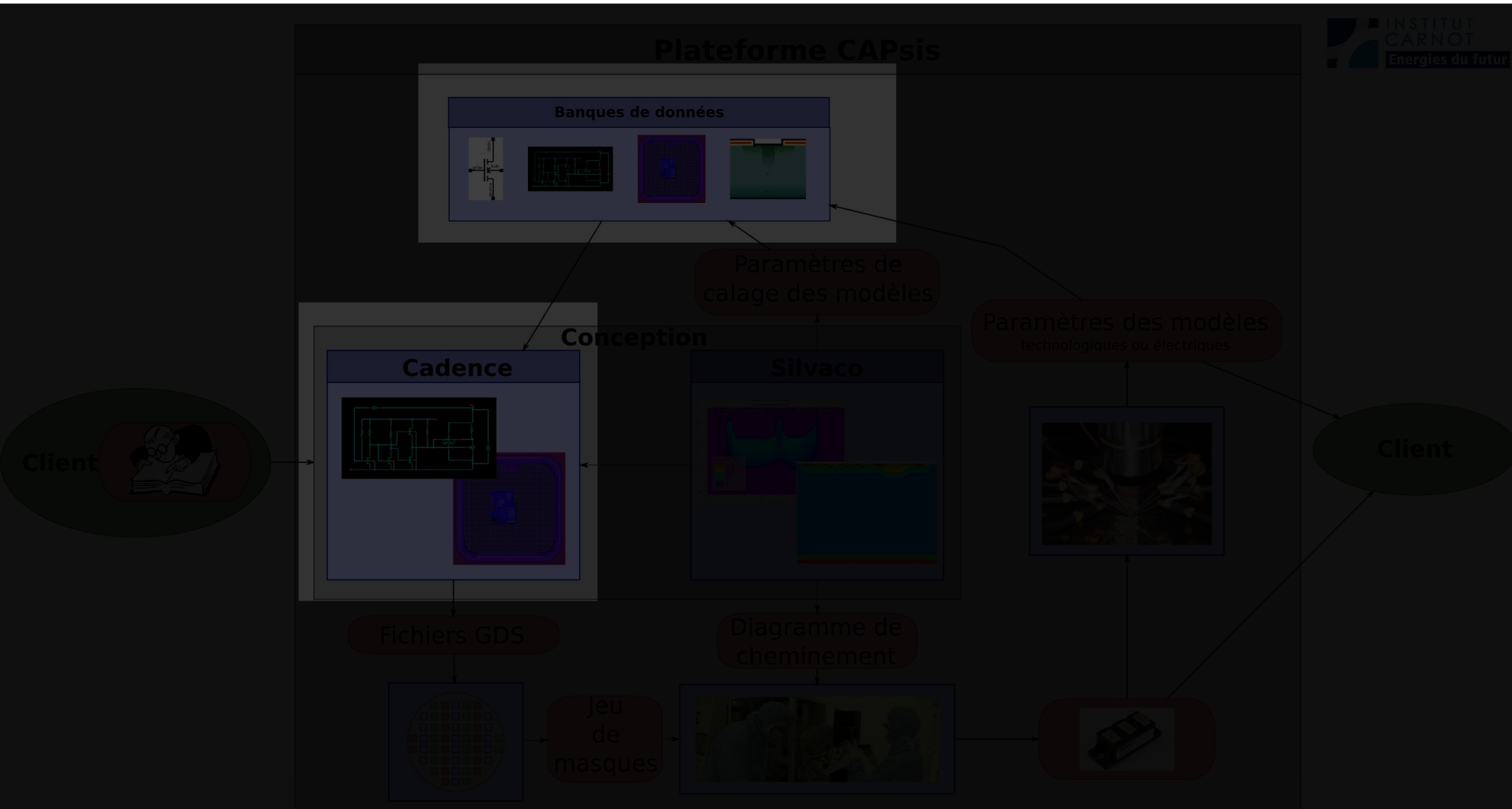


# Conclusions

- Manque d'assistance en conception EP
- Deux démarches de conception plus adaptée



# Conclusion



# Perspectives