Design of an ultra low voltage analog front end for an electroencephalography system
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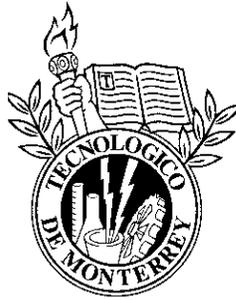
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DESIGN OF AN ULTRA-LOW VOLTAGE ANALOG-FRONT-END FOR AN ELECTROENCEPHALOGRAPHY SYSTEM

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In memory of my grandmother Esther Bautista

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Résumé

Ce travail de thèse présente la conception et le développement d'un circuit intégré frontal analogique (AFE) pour un système d' électroencéphalographie portable. L' AFE est constitué d'un un amplificateur ultra-basse tension et d'un Convertisseur Analogique Numérique (ADC) $\Sigma\Delta$ en Temps Continu (CT). Ce système AFE a été conçu dans une technologie CMOS 0,35μm. Ce circuit de très basse consommation est alimenté avec une tension de seulement 0,5V.

Afin de permettre un véritable fonctionnement en très basse tension, tous les transistors fonctionnent dans la région de faible inversion. Le pré-amplificateur se compose d'un étage d'entrée basé sur une architecture de type cascode replié (OTA-FC) et un d'un étage de sortie basé sur un amplificateur de type "Current Source".

Pour le convertisseur analogique numérique, une architecture de type $\Sigma\Delta$, composée d'un modulateur à temps continu (CT-$\Sigma\Delta$), a été choisi afin d'avoir une consommation de puissance très faible. Le filtre de décimation du convertisseur est basé sur une architecture de filtre à réponse impulsionnelle finie (FIR). Le Modulateur est alimenté avec une tension de seulement 0,5V alors que le filtre numérique nécessite une tension de 1V.

Les résultats de test montrent que l'OTA a un gain de boucle ouverte de 38,8dB pour le premier étage et de 18,6dB pour l'étage de sortie. Cet OTA a une largeurs de bande pour le premier étage et le second étage de 10,23KHz et 6,45KHz, respectivement. Les autres caractéristiques obtenues pour l'OTA sont: bruit de sortie de 1,4$mVrms$@100Hz et consommation de 1,89μW. L' ADC quant à affiche les caractéristiques suivantes: un SNR de 94,2dB, un $ENOB$ de 15,35$bits$, une INL de +0,34/-2,3LSB, et une DNL +0,783/-0,62LSB avec aucun code manquant. Le Modulateur a une consommation de puissance de 7μW. L' AFE proposé dans ce travail possède des caractéristiques qui le place parmi les plus performants comparé aux autres réalisation décrites dans la littérature. Les caractéristiques obtenues pour le circuit permettent d'envisager sont utilisation pour des applications biomédicales de très basse consommation telles que les dispositifs portatifs d'électro-encéphalographie (EEG).

En plus du modulateur de CT-$\Sigma\Delta$ développé en technologies CMOS 0,35μm, un autre modulateur a été conçu utilisant des technologies CMOS 0,13μm, basées sur le temps discret. La simulation affiche un SNR de 92dB et un $ENOB$ de 14.99dB pour une fréquence de sur-échantillonnage (OSR) de 150.

Abstract

In this dissertation a full custom Analog Front End (AFE) integrated circuit (IC) for an Electroencephalography system (EEG) is designed and implemented. The AFE consists of an ultra-low voltage amplifier and a Continuous-Time $\Sigma\Delta$ Analog-to-Digital converter (CT $\Sigma\Delta$ ADC). The AFE was implemented in 0.35 μm CMOS process technology, and it works with a supply voltage of 0.5V.

In order to provide a true low voltage operation, all the transistors are working in the subthreshold region. The proposed preamplifier's topology consists of an input stage based on a folded cascoded amplifier and an output stage based on a current source amplifier.

The CT $\Sigma\Delta$ Modulator was selected to provide a very low power dissipation. The decimation stage is based in a Finite Impulse Response (FIR) filter. The Modulator works with a supply voltage of 0.5V while the FIR stage, which was not optimized, works with a 1V power supply voltage.

Testing results show that the OTA has an open loop gain of 38.8dB and 18.6 dB in its 1st and 2nd stages, respectively. Also, the OTA device has bandwidths in its 1st and 2nd stages of 10.23KHz and 6.45KHz, respectively. Other obtained OTA characteristics are: output noise of 1.4mVrms@100Hz and power dissipation of 1.89μW. The ADC shows the following characteristics: SNR of 94.2dB, ENOB of 15.35bits, INL of +0.34/-2.3 LSB, DNL +.783/-.62 LSB without missing single code. The modulator dissipates only 7μW. The proposed AFE has one of the best performance among all the devices reviewed in today's literature. The AFE's performance make it suitable for biomedical low-power dissipation applications such as portable EEG devices.

In addition to the CT-$\Sigma\Delta$ modulator developed in 0.35μm CMOS technology, an alternative Modulator was designed using a 0.13μm CMOS technology, based on the Discrete Time counterpart. The simulation shows a SNR of 92dB and ENOB of 14.99dB for an oversampling rate (OSR) of 150.

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Acronym list

A

ABCI Ambulatory Brain-Computer Interface

ADC Analog to Digital Converter

AFE Analog-Front-End

AMS Austrian Mikro Systems

ANC Adaptive Noise Cancelling

ASIC Application-Specific Integrated Circuit

B

BCI Brain Computer Interface

BW Bandwidth

C

C_{bs} Bulk to Source Capacitance

C_d Depletion Capacitance

C_G Gate to Bulk Capacitance

CGA Common Gate Amplifiers

C_{gs} Gate to Source Capacitance

CLK Clock

CMFB Common Mode Feedback

CMFF Common Mode Feedforward

CMRR Common Mode Rejection Ratio

CM Common Mode

CNS Central Nervous System

C_{OX} Oxide Capacitance

C_S Source to Bulk Capacitance

CSA Current Source Amplifiers

CT Continuous-Time

D

DAC Digital to Analog Converter

DNL Differential Non-Linearity

DR Dynamic Ratio

DT Discrete Time

E

EEG Electroencephalogram

EMG Electromyogram

ENOB Effective Number of Bits

ERD Event-Retarded Synchronization

F

FC Folded Cascoded

FIFO First In First Out

FIR Finite Impulse Response

FPGA Field-Programmable Gate Array

f_T Frequency response

G

GBW Gain Band-Width

gm transconductance

g_{mb} bulk transconductance

H

H_e Noise Transfer function

H_x Signal Transfer function

I

ICMR Input Common Mode Range

I_D Drain current

I_{DO} Characteristic current

IFSECN International Federation Commite Society of Electroencephalography

INL Integral Non-Linearity

ISI Inter-symbol Interference

K

k Boltzmann constant

K' gain coefficient

L

L Length of a CMOS transistor

M

MC Monte Carlo

MEG Magnetoencephalography

MSB Most Significant Bit

MRI Magnetic Resonance Imaging

N

n Slope factor

NI National Instruments

NMR Nuclear Magnetic Resonance

NRZ Non-Return to Zero

O

OL Overload Level

OSR Oversampling Rate

OTA Operational Transconductance Amplifier

P

P_e Quantization noise power

PET Positron Emission Tomography

PM Phase Margin

PSD Power Spectral Density

PTAT Proportional to Absolute Temperature

Q

q Magnitude of the electrical charge on the electron

R

R Resistance

R_{bi} Effective series bulk resistance

REM Rapid Eye Movements

R_{gi} Effective series gate-metal resistance

RTO Return to Open

RZ Return to Zero

S

S Geometrical shape factor

SAR Successive Approximation Register

SC Switched Capacitor

SCP Slow Cortical Potentials

SINAD Signal, Noise and Distortion

SNDR Signal to Noise-plus-Distortion Ratio

SNR Signal to Noise Ratio

SW Switch

T

T Absolute temperature

U

ULV Ultra Low Voltage

U_T Thermal voltage

V

V_{BS} Bulk to Source Voltage

V_{DS} Drain to Source Voltage

VEP Visual Evoked Potentials

V_G Gate to Bulk Voltage

V_{GS} Gate to Source Voltage

V_S Source to Bulk Voltage

V_T Threshold voltage

V_{TO} Threshold voltage for zero substrate bias

W

W Width of a CMOS transistor

Chapter 1

Introduction

Ce chapitre décrit un système ambulatoire d'interface-cerveau-ordinateur (BCI) et les raisons qui ont motivé ce travail de recherche . Les avantages de l'électroencéphalographie comme système d'enregistrement sont également exposées. Une brève description des différents étages qui sont proposés pour la réalisation de l'interface, ainsi qu'un schéma fonctionnel du système entier sont également présentés. Pour finir ce chapitre détaille le plan du document.

1.1   Motivation

The Brain Computer Interface Systems (BCI) have become in recent years a growing field of research and development. Major efforts are to design interfaces for people with motor disabilities who need better technologies to improve their interaction with the environment. Ambulatory Brain-Computer-Interface (ABCI) helps people to ameliorate this interaction and avoids the need to carry heavy and bulky equipment. Moreover, this technology is also thought that can be used to control different kinds of tools, e.g. industrial machinery.

The formal definition of BCI is illustrated in [1]: "A brain-computer interface is a communication system that does not depend on the brain's normal output pathways of peripheral nerves and muscles". There are different techniques that could be used to monitor brain activity. For example, magnetoencephalography (MEG) is a non-invasive technique of functional imaging, which detects weak magnetic fields associated with the neural synapses. Likewise, positron emission tomography (PET) is a non invasive technique that produce an image of the brain activity. PET is based in nuclear medical image techniques. Another technique is the magnetic resonance imaging (MRI), that produces an image of the brain based on the principles of nuclear magnetic resonance (NMR). MEG, PET and MRI need high level of computer workstation support as well as complex software algorithms. They use huge hardware modules and therefore, these techniques are not used in ABCI applications due to their size and cost.

EEG signals have been well studied, their acquisition and processing are relatively simple and a number of evidences show that individuals can control them. Furthermore, EEG is the most adequate technique to be used as a communication channel in BCI systems. EEG signals could be converted into a command for an application, such as controlling a wheelchair or a keyboard.

The EEG is a semi-invasive technique for recording electrical signals by placing electrodes over the scalp. The electrical biopotentials produced by the brain activity, can be captured by stationary and ambulatory EEG systems. Stationary systems are used mostly in hospitals or clinics; ambulatory systems are used for recording EEG signals throughout a 24 hours span while the patient maintains his normal life.

The EEG signals are mostly used in the detection of brain diseases such as, Parkinsons disease, brain tumors, epilepsy, brain death, narcolepsy, dementia and vertigo. Nowadays, additional techniques to capture and to process EEG signals are used in BCI systems as well.

The necesity of ambulatory EEG for the BCI system and the trends of scaling down the channel in CMOS technology drive the requirement to develop circuits that work at ultra low voltage power supply. Moreover, low power dissipation is essential in this system in order to have longer battery lifetime. In addition, the amplification stage in their analog-front-end (AFE) must have enough gain and low-noise in the base band to amplify the EEG signal (weak signals).

This work develop an ultra-low-voltage low-power AFE for an BCI ambulatory system. The AFE consist of an ultra-low-voltage low-noise high gain amplifier and a micropower Continuous-Time (CT) $\Sigma\Delta$ ADC.

1.2   Proposed ABCI system

Figure 1.1 describes the proposed EEG-based ABCI system in this thesis. The AFE system consists of an ultra-low voltage OTA, and ultra-low-voltage low-power $\Sigma\Delta$ ADC. The signal acquired by electrodes placed over the scalp is amplified by means of the ultra-low-voltage amplifier and then converted into a digital code in order to be processed.

During the processing stage, the interference is subtracted out and an analysis is performed in oder to send an application command via wireless. Some applications include transmission commands to wheelchair, keyboard, cursor or even a machinery control.
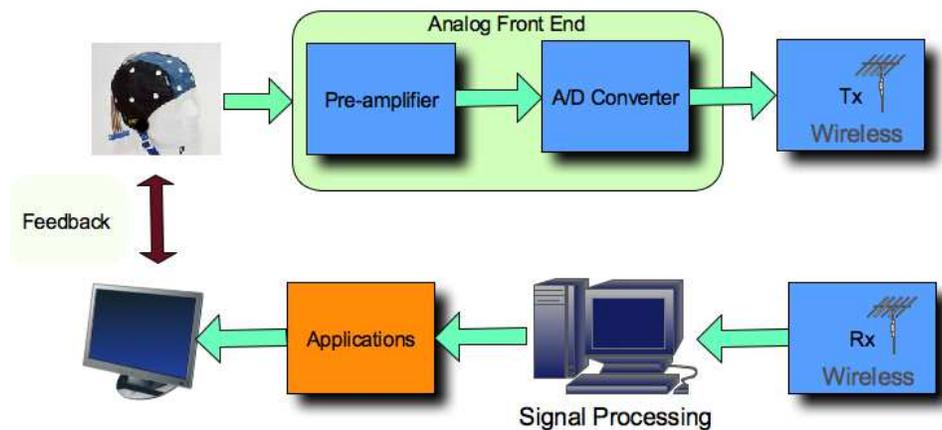
Figure 1.1: Proposed EEG-based ABCI system.

The EEG signal needs to be free from contamination. To achieve this the system

substracts out the power line interference by means of adaptive noise cancelling (ANC) filters. In [2] an architecture based in LMS with adaptive μ iteration gain has been proposed. Not only the power line interference is present in the signal, but also bio-artifacts. Consequently, after the first ANC the signal passes through the bio-artifacts cancellation filters.

This work adresses the AFE development (see figure 1.2). A full custom OTA for EEG signals has been developed and proposed. The AFE works at subtreshold region in order to be a true ultra-low-voltage operation. For the first stage amplification an OTA's topology based in the Folded Cascode OTA is proposed. The ouput amplification stage is based in a Current Source amplifier. The ADC conversion is performed by a $2nd$ order micro-power Continuous-Time (CT) $\Sigma\Delta$ ADC with a 16bits dynamic range. The AFE has been designed to operate at 0.5V.
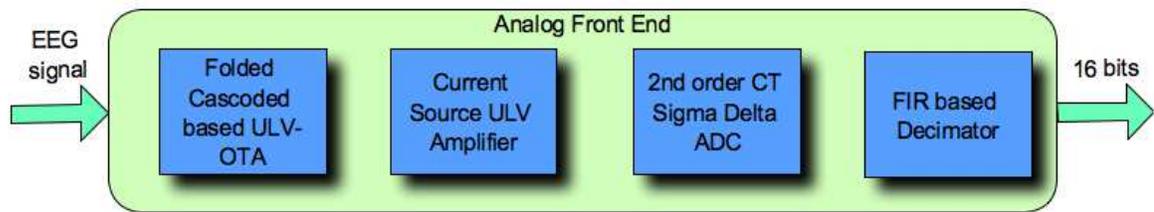
Figure 1.2: Proposed Analog-Front-End

1.3 Thesis Organization

This dissertation is organized as follows. Chapter 2 shows theory of BCI systems and synthetizes previous work in this area. Also, the theory of electroencephalography is presented in this chapter. Chapter 3 illustrates the theory for the CMOS low voltage analog design, and for the Continuous Time $\Sigma\Delta$ Modulators. Also some reported work in the research field of low voltage and low power circuits for AFE is shown. Chapter 4 shows the proposed Analog Front End developed in $0.35\mu m$ CMOS technology. Chapter 5 describes the results of the test of the proposed system. Chapter 6 presents the Discrete Time $\Sigma\Delta$ Modulator based on $0.13~\mu m$ CMOS Techonology. Finally, chapter 7 develops the conclusions of the research.

Chapter 2

An Overview of Brain Computer Interface System

Dans ce chapitre une introduction du système de BCI est présentée d'une façon pédagogique de sorte qu'un lecteur inexpert puisse comprendre. Les sections 2,1 et 2,3 proposent une description détaillée du BCI en décrivant leurs composants principaux, ainsi que leurs caractéristiques. On montre que le BCI n'utilese pas les signaux périphériques des nerfs mais utilisez les signaux électriques évoqués au-dessus du cuir chevelu; le BCI interprète le signal en tant que souhait d'un utilisateur et le convertit en commande. Généralement les systèmes de BCI consistent en trois modules principaux : saisie du signal, traitement des signaux et périphériques de sortie. D'ailleurs, une brève classification des systèmes de BCI est présentée, o le principe d'exécution de chaque système est mis en valeur. La section 2,4 donne la classification de BCI basée sur les dispositifs d'EEG, parmi eux les plus communs sont BCI indépendants et dépendants. Une autre classification proposées des BCI repose sur le signal électrophysiologique qu'ils utilisent. La section 2,5 décrit les signaux et les méthodes d'EEG pour enregistrer ces signaux. L'EEG est la technique la plus appropriée pour une utilisation dans un système BCI. Pour enregistrer les signaux d'EEG du cuir chevelu, une convention appelée 10-20 est utilisée. D'ailleurs, les signaux d'EEG sont classifiés en fonction de leur fréquence, les six groupes principaux sont : Beta, Alpha, Mu, Delta and Theta. L'activité delta a les fréquences les plus basses (0.5Hz à 4Hz), tandis que l'activité gamma a les fréquences plus hautes (35Hz à 100Hz). L'amplitude du signal d'EEG est normalement 50Vpp, cependant, il a des crêtes de 150Vpp et dans quelques activités la tension est aussi basse que 10Vpp. Par conséquent, le système d'acquisition du signal doit pouvoir traiter des signaux de 0.5Hz à 100Hz avec des amplitudes de 10Vpp à 150Vpp. Finalement, la section 2,6 présente l'état de l'art ainsi qu'une brève description des systèmes BCI a proposés par ces groupes de recherche. Les groupes de BCI les plus importants sont: Wadsworth BCI, The Graz BCI, and Kostov and Polak BCI.

Introduction

This chapter presents an insight to the Brain Computer Interface System (BCI). Sections **2.1** to **2.3** expose a detailed description of the BCI. Section **2.4** gives the BCI classification based on the key EEG features. Section **2.5** describes EEG signals and methods for recording these signals. Finally, section **2.6** shows the state-of-the-art literature wich presents a brief description of the BCI proposed by the majors research groups.

2.1 Brain Computer Interface

BCI provides a new communication and control channel, for sending messages and commands from the brain to the external world [1], i.e. the BCI interprets a wish of the user and converts it into a specific command. In order to achive this, brain activity must be monitored. Various methods for monitoring the brain could be used as a channel of communication. They include, functional Magnetic Resonance Imagining (fMRI), Magnetoencephalography (MEG), Positron Emission Tomography (PET) or Electroencephalography (EEG), just to mention some possible applications.

Among these techniques, EEG is the more suitable for BCI application, since it gives continuous and instantaneous recordings of the brain activity. Furthermore, EEG requires relatively simple and inexpensive equipment. Studies have already demonstrated correlations between EEG signals and actual or imagined movements and between EEG signals and mental task [1].

2.2 Functional blocks of a BCI

According to [1], a EEG BCI device consists mainly in the Analog-Front-End (Signal Aqcuisition) for EEG signals, the digital signal processing module, and an output device.

2.2.1 Signal acquisition

The input signals of this module are comming from electrodes placed in the scalp or could be generated by electrodes placed in the surface of the brain. It is common the use of a special electrode cap, in which sensors are placed using the 10-20 system.

The signal acquired is then amplified and digitized. The sampling rates are between 100-400 Hz.

2.2.2 Signal processing

The digitized signals are then subjected to variety of extractions like interference and artifact removal, filtering, voltage amplitude measurements, and spectral analyses among others. In these analysis also the signal features are extracted in order to find the message encoded by the user .

After the signals features are interpreted, the signal is translated into a command. For this purpose, algorithms that use linear techniques (classical statistical analyses) or nonlinear methods (neural networks) could be used [10],[21], [22].

2.2.3 The output device

The most common output device used in the BCIs is the computer screen and the output is the selection of targets, letter, or icons presented on it. Some BCI also provide additional, interim output, such as cursor movement toward the item prior to its selection.

2.3 BCI approaches

There are two classes of BCIs: dependent and independent. A dependent BCI does not use the brain's normal output pathways to carry the message, but activity in these pathways is needed to generate the brain activity that does carry it [1]. In this class of BCI, the user concentrates on few mental task, for example moving the eyes, then the visual evoked potentials (VEP) are recorded by the electrodes placed in the scalp. In this case the output is the EEG, but the EEG signal generation depends on the nerves and muscles that activate the EEG signals.

On the other hand, an independent BCI does not depend in any way on the brain's normal output pathways. The message is not carried by peripheral nerves and muscles, and furthermore, activity in these pathways is not needed to generated the brain activity that does carry the message [1]. In this case the users must learn to regulate their own EEG. For example, change the amplitude on a specific brain activity rythm.

A BCI changes electrophysiological signals from mere reflection of central nervous system (CNS) activity into the intented products of that activity: messages and commands that act on the world. A BCI replaces nervous and muscles and the movements they produce with electrophysiological signals and the hardware and software that translate those signals into actions.

As a replacement for the brain's normal neuromuscular output channels, a BCI also depends on feedback and on adaptation of brain activity based on that feedback. BCI operation depends on the interaction of two adaptive controllers: the user's brain, which produces the signals measured by the BCI, and the BCI itself, which translates these signals into specific command.

2.4   Clasification of BCI

BCIs could be classified in diferents categories, were the more common are: invasive and non-invasive, synchronous and asynchronous, universal and indivdual, online and offline and EEG features. They are here explained.

2.4.1   Invasive and non-invasive BCI

These BCI are based on EEG measured with the electrodes in the scalp. Invasive BCIs records the electrical activity of the brain from the cerebral cortex. Microelectrodes pick up the recording of activity from a single neuron. An example of this invasive method is the cortical neurons.

2.4.2   Synchronous and asynchronous BCI

Almost all the BCI systems work in synchronous mode. The user produce a specific mental task in a predefined time. In an asynchronous mode, the brain activity is analyzed continuously, then the user can freely initiate the specific mental task. The BCI needs to detect when the user tries to control and when the EEG signal does not have a command.

2.4.3 Universal and indivdual BCI

Universal BCIs rely on the assumption that by gathering EEG data from few users it is posible to find a classification function that should be valid for everybody. In individual BCIs, the fact that all the people are diferent, both physiologically and psychologically are need to be considered.

2.4.4 Online and offline BCI

Online BCI extracts the signal, classify the command and control the device in real-time. In offline BCI, the signal is recorded for later processing. This BCI are mostly used to examine electrode position, extraction algorithms, classifiers, etc.

2.4.5 EEG features

BCI systems could be also sorting according to the electrophysiological they use, we have the following groups of signals to be captured: visual evoked potentials, mu and beta rythms, slow cortical potentials, P300 evoked potentials and corticals neurons.

Visual Evoked potentials

In this system the visual evoked potentials (VEP) is recorded from the scalp, over the visual cortex, in order to determine the direction of the eye gaze. VEP systems evaluate the visual nervous system from the eye to the brain.

VEPs communication system depend on the user's ability to control gaze direction. Thus they perform the same function as system that determine gaze direction from the eyes themselves, and can be categorized as dependent BCI systems [1].

Mu and beta rythms

In awake people, primary sensory or motor cortical areas often display EEG activity with frequencies of 8 to $13Hz$ when they are not engaged in processing sensory input or producing motor output. It is called mu rythm when focused over somatosensory cortex, and alpha rythm when focused over visual cortex.

It has been reported that mu and beta rythm amplitudes serve as a very effective input for BCI. The preparation of the movement, followed by an execution produce a power reduction in certain frequency bands. This power reduction is referred to as

Event-Related Desynchronization (ERD). On the other hand, the power increase indicates relaxation, Event-Related Synchronization (ERS).

Slow cortical potentials

Slow cortical potentials (SCP) consists of potentials shifts recorded over the scalp that occur over periods from 0.5 to 10 *seconds*. Negative SCPs are typically associated with movement and other functions involving cortical activation, while positive SCPs are usually associated with reduced cortical activation.

During the first 2 seconds, the system records the initial voltage level. During next 2 seconds, the user tries to increase or decrease the level voltage of the SCP by target selection. The user needs to train 1-2h per day over weeks or months. When they achieve an accuracy of 75%, they are switched to a language support program, which allows a selection from up to 3 letters per minute [10].

P300 evoked potentials

Infrequent or particulary significant auditory, visual, or somatosensory stimuli, typically evoke in the EEG over parietal cortex a positive peak at about $300ms$.

A P300 based BCI has an apparent advantage in that it requires no initial user trainning: P300 is a typical response to a desired choice. However, such technique remind us of limited to letter or symbol selection paradigms. Reference [3] presents a BCI for typing a 5 letter per minute evoked potentials. In that system, the user employ a matrix of symbols of $6X6$, its rows or colums flash alternatively each 125ms in a random order, a complete trial of 12 flashes. The user then selects a symbol by counting how many times the row and column are computed.

Cortical neurons

So far, one user has learned to control neuronal firing rates and uses this control to move a cursor to select icons letters on a computer screen. By using activities to control one dimension of cursor movement and residual EMG to control the other dimension and final selection, communication rates of up to about 3 letters per minute have been achieved. While training has been limited by illness recurrence and medication effects, the results have been encouraging and suggest that more rapid and accurate control should be posible in the future [1].

2.5   Electroencephalography

2.5.1   Electrodes for EEG

The scalp electrodes are the most usual electrodes in rutine EEG recordings. They are commonly made of AgCl with diameters between 4 to 10mm. Other types of electrodes like are made of gold or platinum; however their use is not frequent [4]. AgCl electrodes are very popular among other types because they are easy to handle and place and they have lower resistance compared to the gold or platinum electrodes.

The resistance of an electrode is approximately of hundreds of ohms. In agreement with the EEG international standard, the electrode resistance must be in the order of 100-500 Ω.

The subcutaneous electrodes are made of stainless steel or platinum. Their length is about 10mm and their diameter is 0.5mm. These electrodes have several disadvantages; their positioning is painful, and its resistance is greater than the one for scalp electrodes (10-15 $K\Omega$). Furthermore, this type of electrodes may cause infections [5].

Another type of electrode is the clip electrode. Their properties are similar to those of scalp electrodes. These electrodes are commoly used in the EEG recording to provide a reference [5].

Finally, the depth electrodes are arrays designed specifically for the direct interaction with the brain in order to measure voltages that can not be measured with scalp electrodes. They are placed through the surgical procedures [5].

Figure 2.1 show the types of electrodes for EEG recording.

2.5.2   10-20 system

The International Federation Commite Society of Electroencephalography and Clinical Neurophysiology (IFSECN), recommends a standard to set up electrodes over the scalp. Such standard is known as a 10-20 system. The "10" and "20" refer to the fact that the actual distances between adjacent electrodes are either 10% or 20% of the total front-back or right-left distance of the skull.

The American Society of Clinical Neurophysiology recommends the use of at least 21 electrodes. The electrodes with odd number are placed on the left and electrodes
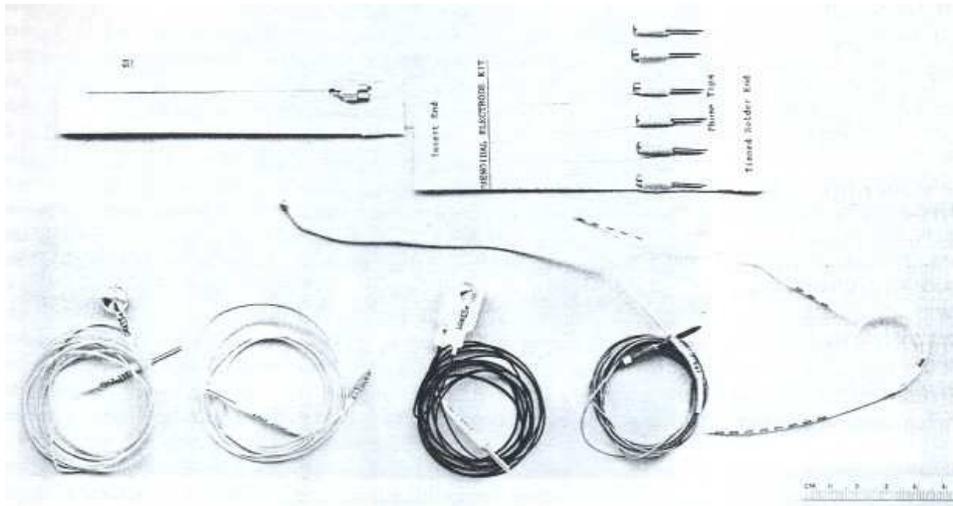
Figure 2.1: Types of electrode for EEG recording. [5]

with even number are placed on the right of the head. The letters specify an anatomical area; e.g. "F" means frontal, the electrodes between the ears are specified by "Cz". The electrodes T3 and T4 of this system are referenced as a T7 and T8 in extended systems; and the electrodes T5 and T6 are referred as a P7 and P8 in the new nomenclature. See figure 2.2
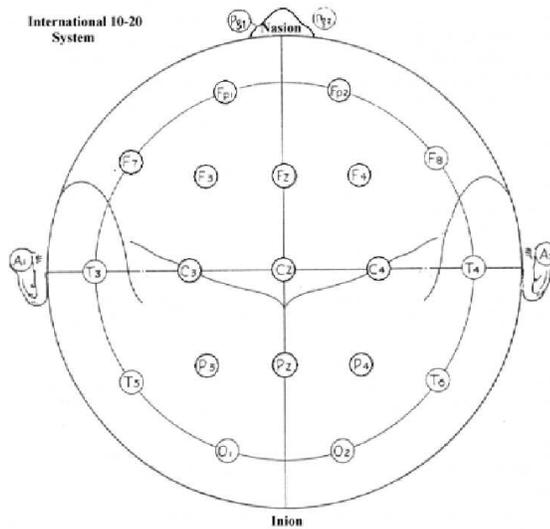
Figure 2.2: EEG electrode 10-20 system. [5]

The EEG helps physicians to study and analyze electrical activity in the brain [6].

2.5.3 Recording scheme

The most popular schemes for brain activity measuments in the 10-20 system are: Bipolar and Referential.

The bipolar scheme performs diferential measurements between pairs of electrodes. The advantage of using recordings of close electrodes is the cancellation of distant electrical events common to both electrodes. Other advantage is the easy localization of focal abnormalitys [6]. In the bipolar scheme, both inputs are connected to active electrodes. Not single electrode is common to all channels. This scheme links pairs of sequential electrodes in longitudinal lines or coronary.

The referential scheme has remarkable advantages over the bipolar. For example, allows a variety of calcualted references like averages references, laplacian references and even customized references for patients. However, the referential scheme also has disadvantages; if the reference is interrupted or has high impedance, the noise will predominate in all the channels [5]. In this scheme, one electrode as a reference is connected to the less negative input of each amplifier. Ideally, for each pair of electrodes in the channels, only one is active. This situation is never achieved since the reference electrode also contribute in the output signal. The most common reference include: A1 and A2, A1 and A2, Cz and the average reference.

2.5.4 EEG signals features

The EEG signals are electrical events with low frequencies recorded by scalp electrodes. The typical amplitude of the signal is around $50\mu V_{pp}$, but also can reach values as high as $150\mu V_{pp}$ (Delta waves) [7].

The EEG is used to detect cerebral abnormalities like Epilepsy, arterial abnormalities, tumors, hemorrhages, cerebral tissue damage, etc.

The age and status of the patient are the only information that is required before starting the EEG analysis. The status of the patient means the general clinical status of conscience in which the patient is; for example, alert, letargic, stupor and semicomatose. It also means the physiological variations of wakefulness and levels of dream that occur during the EEG recording. The electrical activity varies according to the patient's age; i.e. a particular activity that is normal for certain age is completely abnormal for a different age. During the EEG recording, the patient is put under different stimuli, such open and close eyes, flashing light, repetitive movements of the

extremities, sensorial stimulation and hyperventilation [7].

The analysis of EEG signal is complex due the large amount of information that is received by each electrode. Different waves are sorted by their main frequencies and in some cases by their shapes. There are six main groups [8] that are described as follows.

Beta activity

Generally the Beta activity is asociated to signals having frequencies between $13Hz$ and 30 Hz, and voltage levels between $5\mu V$ and 20 μV. Figure 2.3 shows the beta activity. *Beta* wave is related to the reasoning, attention and focusing. It can reach $40Hz$ during the intense mental activity [8].

Activity with frequencies greater than $13Hz$ can be found in adults and normal children. The *Beta* activity is divided into three ranges. The most common is between 18 and 25 Hz, the less common is between 14 and $16Hz$, and finally the uncommon is found between 35 and 40 Hz. In approximately 98 % of the awake adults and normal children the voltage is less than $20\mu V$; in the 70% is less than 10 μV. The *Beta* activity with voltages greater than $25\mu V$ is considered abnormal [5].

The *Beta* activity between 18 to $25Hz$ increases during the rapid eye movements (REM) dream and usually decreases during the depth dream [6].
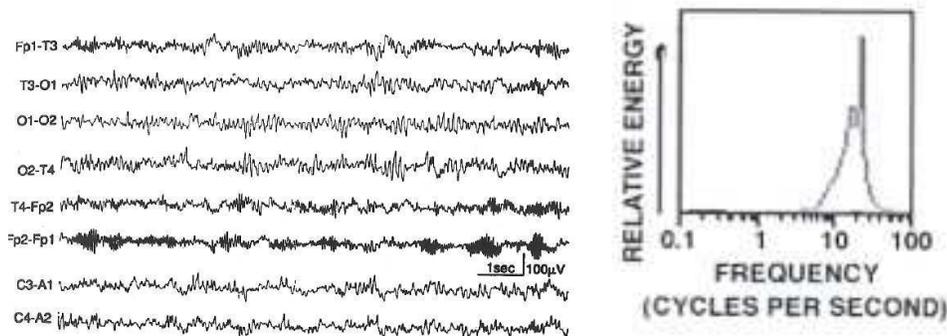
Figure 2.3: Beta activity waves [5] and asociated spectrum [8].

Alpha activity

This activity is related to frequencies between $8Hz$ to $13Hz$, and amplitudes from 30 to 50 μV. The *Alpha* waves had been related with mental relaxation and poor inter-

est in something. This activity has a considereable presence in the occipital and in the frontal cortex areas [8]; however in the occipital area the activity decreases with the age.

The alpha activity has strong relationship with the blood flow and even it is present in anesthesiated patients.

In the 75% of normal adults, *Alpha* activity reach $45\mu V$ in amplitude while for children is uncommon to find voltage levels of less than $30\mu V$ [5].

This activity can be altered through the physiological changes and mental activity such as anxiety.

Mu activity

Mu activity produce a spontaneous signal around 8 to $10Hz$ and is the central rythm of the *Alpha* activity. Figure 2.4 shows the mu activity. It can be meassured in the motor cortex [8]. This activity dissapears in the opposite emisphere to the moving extremity. Its precence is associated to attention and it reinforces when there is no movement [5].
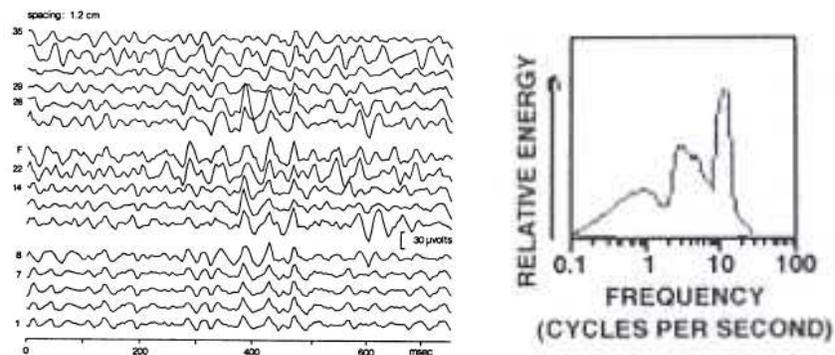
Figure 2.4: Wave [5] and spectrum of Alpha activity [8].

Delta activity

The *Delta* activity has frequencies between $0.5Hz$ and $4Hz$, with variable amplitude. The *Delta* signals are associated to the dream activity and if they are found in the awake patient, it indicates a brain disfunction. It is easy to confuse this activity with artifacts [8].

Gamma activity

The range frequencies in this activity are $35Hz$ to $100\ Hz$. This activity is associated to congnitive functions such as attention, learning and memorization.

Intracraneal recordings of this activity have been reported during the visual, hearing and sensomotor activities [5].

Theta activity

The range frequencies in this activity are 6 and $7Hz$, with an amplitude greater than 20 μV. Figure 2.5 shows the $Theta$ activity The mental stress, like frustation, reinforce the $Theta$ activity in the frontal area. The $Theta$ activity is also associated to the inspiration and depth meditation whose dominant frequency is $7Hz$ [8].
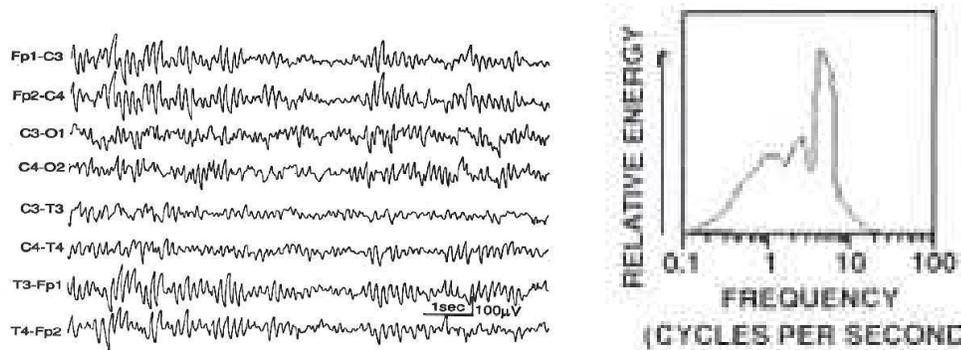
Figure 2.5: Waves [5] and spectrum of Theta activity [8].

2.6   State of the Art

2.6.1   EEG devices

Presently, there is a wide range of stationary and ambulatory EEG systems available. Stationary EEG systems are only used in hospitals due to their size. Their main features are: 16 to 128 channels, sampling frequency of at least of $200Hz$ and 16 to 22 bits of digital resolution. On the other hand, ambulatory systems are used in continuous patient monitoring (24 hours) and their size is similar to a CD player. Their main features are: 16 to 32 channels, sampling frequency of at least $200Hz$, 16 to 22 bits of digital resolution and 0.9 to 1.4 kilograms in weight. Also, some ambulatory systems have integrated wireless communication to transfer data to a server that holds

a database available to physicians. These systems can store data anywhere from 24 to 72 hours. Figure 2.6 shows a stationay and an ambulatory EGG systems.

Figure 2.6: EEG recording systems. Left: Stationary system. Right: Ambulatory system (Grass Telefactor)

Concerning electrode placement, even the specialists require about 20 minutes. Recently EEG caps where the electrodes are pre-positioned according to the 10/20 standard, are used [9].

2.6.2   BCI devices

Here the most important proposed EEG based BCI are presented. The BCI proposed by Wadsworth Center use the self-regulation of the mu or beta rythms, and the proposed by the University of Graz, Kostov and Polak are based on the pattern recognition approach.

Wadsworth BCI.

Wolpaw, McFarland et al. designed a BCI at Wadsworth Center. The BCI proposed is based on the self-regulation of the 8-12Hz mu or the 13-29 Hz beta rythms. People learn to control those signals and use the signals to move a cursor in the one or two dimensions to targets on a computer screen. Figure 2.7 shows how the user increases and decreases the amplitude of a 8-12Hz mu rythm, for moving the cursor to the top and the bottom respectively.

In the system proposed in [10], a 64 EEG channels were used to record signals from 4 subjects, where each channel was referenced to the electrode in the rigth ear.
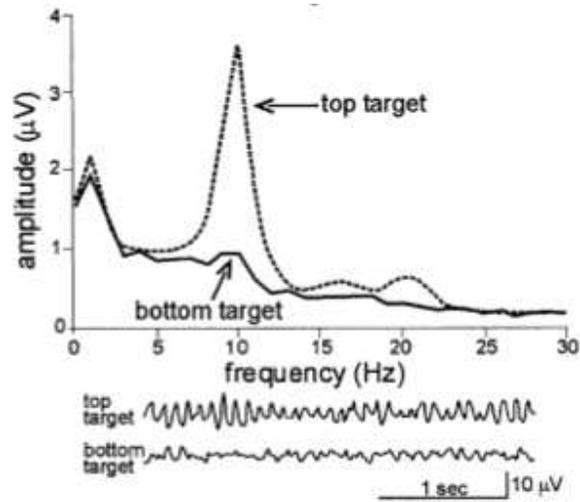
Figure 2.7: Sensorimotor rythm BCI.

The signal was sampled at $128Hz$. The feature extraction was done by autoregressive algorithms. A trainning is needed for periods of 30 min per session having 2-3 sessions per week during 2-3 weeks. This BCI is used to answer simple yes/no questions with accuracies of $> 95\%$, references [11] and [12] are examples of these BCIs. Moreover, some efforts has been made on applications like answering simple questions or basic word processing [13].

Other work has been redirected to the improvement of spatial filters that match the spatial frequencies of the user's mu or beta rhythms, autoregressive frequency analysis that permits more rapid device control [14], [15], [16].

The BCI2000 was also proposed by Wolpaw, and is a general purpose and distributed BCI system. This BCI can describe a wide variety of present and future BCI systems. BCI2000 can incorporate alone or in a combination any brain signals, signal processing methods, output devices, and operating protocols [17].

The Graz BCI.

This BCI was started by Pfurtscheller in the Graz University of Technology. This BCI system is based on the detection of the ERF and ERS of mu and beta rythms during motor imagery.

References [18], [19], [20] show the efforts that had been made on distinguishing between the EEG associated with imagination of different simple motor actions and

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thereby enabling the user to control a cursor or an orthotic device that open and closes a paralyzed hand.

In the BCI proposed in [21], classification of EEG patterns during five mental task has been done. In the standar protocol, the user first participates in an initial session to select a motor imagery paradigm. The timing interval was 5.25 seconds per trial. The EEG signal was recorded by 29 electrodes and digitized by a samplig frequency of $246Hz$. The signal was filtered between $0.5Hz$-$30Hz$.

Kostov and Polak BCI.

Kostov and Polak reported in [22] a BCI control based on the pattern recognition approach, that controls a cursor in one and two dimensions. EEG has been recorded by an array of 28-electrodes arranged according to the 10-20 electrode system. The signal was digitized at 200Hz samplig rate. The features were extracted form C3, C4, P3 and P4 electrodes by means of autoregressive parameters feature extraction. Trainning is needed for about 30 minutes per session.

In the work reported in [23], an autoregressive parameters from 2 to 4 locations are converter to a cursor movements by means of an adaptive logic network.

The principal goal of Kostov BCI is to develop a range of applications by using two dimensional cursor control. The BCI reported by F. Karmali, et al [24] is an application example of this BCI.

2.7   Conclusions

In this chapter an insight of the BCI system was presented. It was stated that BCI does not uses peripherial nerves signals but uses electrical signals evoked over the scalp; the BCI interprets that signal as an user's wish converting it into a command. In general, BCI systems consists in the three main building blocks: signal acquisition, signal processing and the output device. For the BCI system exists a variety of sorting, among them the most common are independent and dependent BCI, and the other type classifies the BCIs according to the electrophysiological signal they use.

The EEG is the more suitable technique to use in the BCI system. For recording the EEG signals from the scalp, a convention called 10-20 is used. Moreover, the EEG signals are classified according their frequency, the six main groups are: Beta, Alpha,

Mu, Delta and Theta. Delta activity has the lower frequencies ($0.5Hz$ to $4Hz$), while Gamma activity has the higher frequencies ($35Hz$ to $100Hz$). The Amplitude of the EEG signal is normally $50\mu V_{pp}$, however, it has peaks of $150\mu V_{pp}$ and in some activities the voltage is as low as $10\mu V_{pp}$. Therefore, the signal adquisition system must be able to process signals from $0.5Hz$ to $100Hz$ with amplitudes from $10\mu V_{pp}$ to $150\mu V_{pp}$.

In the last section of this chapter, the works developed in the most important BCI research groups were presented. The most important BCI groups are: Wadsworth BCI, The Graz BCI, and Kostov and Polak BCI.

Chapter 3

Theoretical Background

Ce chapitre présente les principes théoriques mis en oeuvre dans le développement du système d'AFE (Analog Front End) proposé. Le chapitre commence par une introduction aux techniques de conception de basse tension utilisées dans les technologies CMOS. Dans la section 3,1 des tendances futures des technologies CMOS sont présentées. Cette section présente ensuite les techniques principales de circuits de basse tension: composite transistor, lateral BJT, forward-biased bulk-source et bulk-driven. Si ces techniques fonctionnent en inversion forte, il y a une limitation principale : la tension d'alimentation ne pourrait pas être inférieur à la somme de la tension de seuil des transistors empilés. Par conséquent, la réduction de la tension d'alimentation a pu être possible en polarisant ces circuits dans la region d'inversion faible.

Dans la section 3,2, la théorie de transistors de CMOS fonctionnant dans l'inversion faible est présentée. Dans ce mode de fonctionnement la caractéristique des transistor est exponentiel et les dispositifs ont besoin au moins de 3UT afin d'avoir de bonnes linéarités. Dans la section 3,3, la théorie du bruit dans des dispositifs CMOS est présentée, le bruit flicker et le bruit blanc sont introduits.

Dans les sections 3,4, 3,5 et 3,6, les architectures de CAN sonjt présentées. Le choix de l'architecture en fonction des contraintes du projet est présenté. L'architecture choisie est le CT-$\Sigma\Delta$CAN. Cette architecture est choisie en raison de la faible consommation attendue et de la haute résolution possible. La théorie du modulateur $\Sigma\Delta$ est basé sur les références [25] (sous-sections 3,6,1-3,6,3) et [26] (sous-sections 3,6,4-3,6,7). La section 3,7 présente la situation actuelle des amplificateurs de basse tension et les CAN $\Sigma\Delta$. La section 3,8 conclue ce chapitre.

Introduction

This chapter presents the theory behind the developments of the proposed AFE system. The chapter begins with an overview of the low voltage design techniques used for standard CMOS processes. In section **3.1** the trends in the future CMOS technologies are shown. Moreover, this section presents the main low voltage circuits techniques: the composite transistor, the lateral BJT, the forward-biased bulk-source and the bulk-driven technique. In section **3.2**, the theory of CMOS transistors operating at subthreshold region is presented. In section **3.3**, the therory of noise in CMOS devices is presented, in which the icker noise and white noise are introduced. In sections **3.4**, **3.5** and **3.6**, the ADC architectures, the selection of the ADC architecture and the theory of the selected ADC is respectively presented. The selected architecture is the CT-$\Sigma\Delta$ ADC. It is selected due its good performance for high resolution and low power consumption. The theory of $\Sigma\Delta$ Modulation based upon references [25] (subsections **3.6.1** to **3.6.3**) and [26] (subsections **3.6.4** to **3.6.7**). Finally, section 3.7 illustrate the state-of-the-art in designing low-voltage ampliers and $\Sigma\Delta$ ADCs.

3.1 Low-voltage design techniques for standard CMOS technology

The trends of portable devices justify the necessity of very low voltage power supply and power dissipation systems such as ABCI systems, pacemakers, hearing aids, mobile communications and a wide variety of consumer products. Low power dissipation is essential in these systems to have a long-life battery and is even essential in battery-less systems.

The analog power supply must be at least the sum of the magnitudes of the n-channel and p-channel thresholds [28]. The threshold voltages in future CMOS technologies may not decrease much below the values that are available nowadays. Low-voltage circuits in the future will be incompatible with the standard CMOS technology. Consequently, low-voltage circuit techniques are required to make compatible future CMOS technologies with future low-voltage requirements. Figure 3.1 shows the trends of the threshold voltage from the $1\mu m$ to the $22nm$ CMOS process.

This section address the novel low-voltage circuit techniques that are compatible with todays CMOS technology. Furthermore, this chapter also address the limitation of low-voltage power supply.
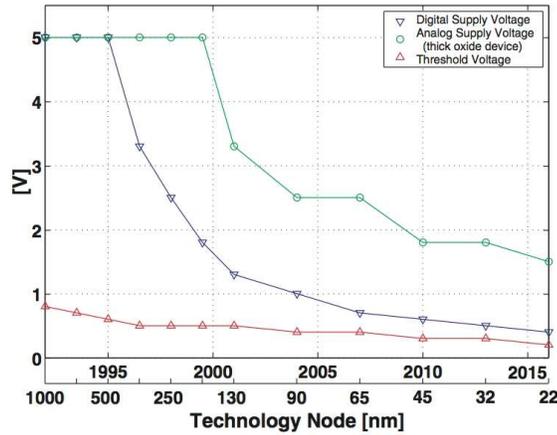
Figure 3.1: Supply voltage and threshold voltage of differents technologies. (Taken from [27])

3.1.1 The Composite Transistor

The composite transistor is based on the regulated-cascode current sink/source [28] and is also known as the self-cascode technique [29] and as the super-transistor [30]. It consists of a cascode configuration and a series feedback loop that increase the small signal output resistance and yet minimizes the voltage drop across the output of the current sink/source.

The composite transistor technique is depicted in the figure 3.2. The transistor T_1 is used as input device, converting the input voltage v_1 into a drain current i_o that flows through the drain to the source of the T_2. To reduce channel-length modulation, V_{DS} of the transistor T_1 must remain stable, this is performed by a feedback that consists of an amplifier (transistor T_3 and I_1) and T_2 used as a follower [30].
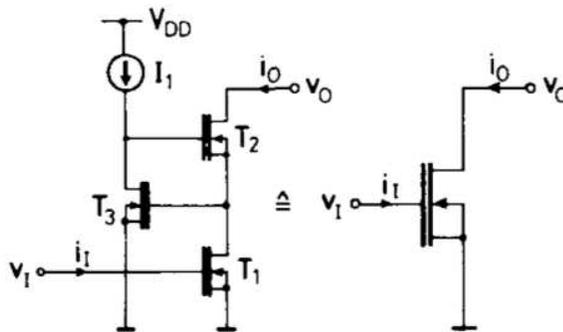
Figure 3.2: Composite transistor. (Taken from [30]).

The composite transistor technique provides a high output impedance with larger

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voltage headroom than the conventional cascode structures. Note that it is not necessary to have different thresholds voltages, $V_{T1} > V_{T2}$ [31]. Moreover, with this technique transistor could be used with minimum sizes obtaining small circuit area while having good frequency response and high dc gain.

3.1.2 The Lateral BJT

This technique is a solution to overcome the threshold limitation. When the voltage in the gate is negative enough (approximately $-V_G > 0.6V$) the I_D-V_S relationship becomes independent of V_G, staying exponential up to much higher values of current, with a slope n equals to U_T. Figure 3.3 shows the cross-section of a NMOS transistor and the current flow in bipolar operation.
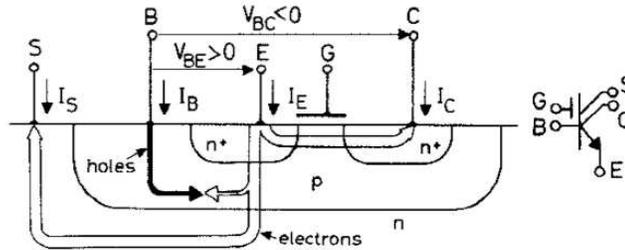
Figure 3.3: Cross-section of a NMOS transistor implemented in a p-well technology and its symbol. (Taken from [32]).

The lateral bjt n-p-n is combined with the vertical n-p-n. Emmiter current I_E is divided into a base current I_B, a lateral collector current I_C, and a substrate collector current I_S. However, emitter current gains can be large ($\beta = I_C/I_B$ and $\beta_s = I_S/I_B$). By minimizing the emmiter area and the lateral base width, and by having the emmiter surrounded by the collector, the ratio I_C/I_S is incremented improving the device performance. The presence of the gate that pushes the flow of diffusion carriers away from the surface might even improve the device with respect to normal lateral bipolars [32].

This solution has added the advantage of much less 1/f noise because current flow in the bulk of the material. Moreover, an additional advantage of the lateral BJT is its low value of v_{CE} which is also important in low voltage analog circuits. However, the lateral BJT requires turn on voltages of $0.6V$ to $0.7V$ which do not provide that much advantage over the MOSFET.

3.1.3 Forward-Biased Bulk-Source

This technique is based in reducing the threshold voltage through a forward bias on the well-source junction. The standard relationship used to predict the reverse bias influence is [33]:

$$V_t = V_{t0} + \gamma[\sqrt{2\phi - V_{BS}} - \sqrt{2\phi}]$$

(3.1)

where V_{t0} is the threshold voltage for zero substrate bias ($V_{BS} = 0V$), γ is the bulk threshold parameter, and ϕ is the strong inversion surface potential of the MOSFET in the well.

Figure 3.4 depicted the cross-section of a CMOS device using this technique which also includes the parasitic vertical BJTs.
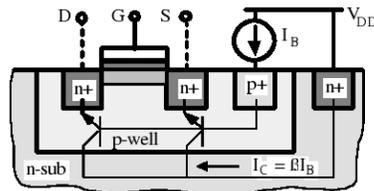
Figure 3.4: Cross-section of forward bias NMOS transistor (Taken from [33]).

The bulk current, I_B, is the base current of the vertical NPN BJTs and appears at the drain or source as ($\beta_F I_B$). Although these currents are dc and β_F is generally small, they are undesirable. The bulk current remains below $100nA$ for bulk-source voltages as high as $0.5V$ [33].

The noise characteristics are identical whether the bulk-source is forward-biased or not.

3.1.4 Bulk-Driven MOSFETs

The bulk-driven MOSFET concept was proposed by A. Guzinski, et. al in 1987, as active components in an OTA differential input stage. The objective of bulk-driven differential amplifier was to improve the linearity and to yield a small g_m. In 1998 a 1V op-amp was designed by P. E. Allen et al using the depletion characteristics of the

bulk-driven MOSFET in order to achieve the low voltage requirements.

Bulk-driven is perhaps the most significative solution to the threshold limitation. A CMOS crosssection diagram illustrating this technique is shown in the figure 3.5.
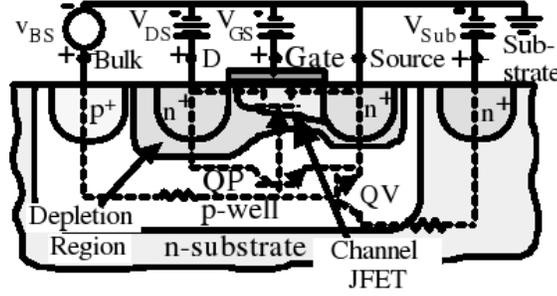
Figure 3.5: Cross-section of bulk-driven MOSFET (Taken from [33]).

Normally, when using a MOSFET as part of an amplifier, the signal is fed in the gate and the bulk is tied to a bias voltage. In bulk-driven MOSFET, the signal is fed into the bulk and the gate is tied to a bias voltage that is sufficient to turn it on. The current flowing from the source to drain is modulated by the reverse bias on the bulk -channel junction. The result is a junction field-effect transistor with the bulk as the signal input. Consequently, the bulk driven configuration illustrates a high-input impedance depletion device that requires no DC bulk-source voltage for current flow [33].

The transconductance characteristics are depicted in the figure 3.59.

The large-signal equation for the bulk-driven MOSFET is [34]:

$$i_D = \frac{K'W}{L}(V_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - v_{BS}} + \gamma\sqrt{2\phi_F} - \frac{n}{2}v_{DS}) \tag{3.2}$$

for $v_{DS} \leq V_{DSsat}$, and

$$i_D = \frac{K'W}{2nL}(V_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - v_{BS}} + \gamma\sqrt{2\phi_F})^2(1 + \lambda v_{DS}) \tag{3.3}$$
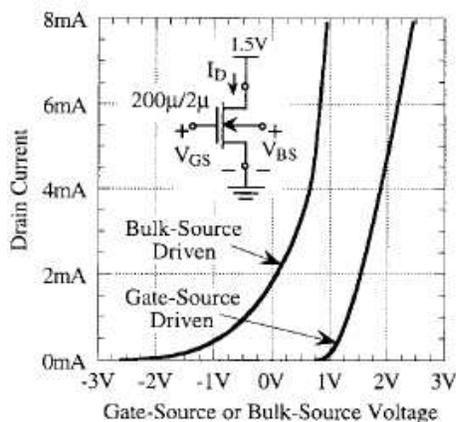
Figure 3.6: Measured linear I_D Vs. V_{BS} for the bulk-driven MOSFET and V_{GS} for the standard MOSFET (Taken from [28]).

for $V_{DS} \geq V_{DSsat}$, where

$$n = 1 + \frac{C_{BC}}{C_{ox}} + \frac{qNFS}{C_{ox}} = 1 + \frac{\gamma}{2\sqrt{\phi_j - V_{BS}}} = 1 + \eta = 1 + \frac{g_{mb}}{g_m} \qquad (3.4)$$

and

$$V_{DSsat} = \frac{v_{GS} - V_T}{n} \qquad (3.5)$$

The small-signal transconductance is given by [34]:

$$g_{mbs} = \frac{\gamma\sqrt{2K'_N(W/L)I_D}}{2\sqrt{2|\phi_F| - V_{BS}}} \qquad (3.6)$$

Advantages of using bulk-driven devices are [35]:

− Bulk-driven differential pairs in op-amps significantly improve the Input Common-Mode Range (ICMR) since it allows an extension in its signal range on the negative side. With an appropiate design, the device can remain saturated over the entire rail-to-rail ICMR.

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– Bulk-driven current mirrors, can eliminate the large voltage drop across the input device. This is because the voltage drop across the input device V_{DS}, which is equal to the bulk-to-source voltage V_{BS}, does not need to be greater than the threshold voltage V_T for proper operation. The cascode configuration, can be used to improve current matching and increase the finite output impedance of the current mirror.

Nevertheless, the bulk-driven also has disadvantages [28]. The main disadvantage is its parasitic input capacitance. This decreases its frequency response as f_T diminishes according to the following equations [34].

$$f_{T,gate-driven} \approx \frac{g_m}{2\pi C_{gs}} \tag{3.7}$$

$$f_{T,bulk-driven} \approx \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})} = \frac{\eta g_m}{2\pi(C_{bs} + C_{bsub})} \tag{3.8}$$

3.1.5 Limitations of circuits in strong-inversion working with low-voltage power supply

The described low voltage techniques show good performance working in strong-inversion region. The composite transistor has, perhaps, the better performance again short channel modulation, while having low $V_{DS(composite)}$, being a good candidate for low-voltage applications. However, the transistors in its feedback loop must remain saturated as possible, having larger $V_{DS(sat)}$.The lateral BJT is a powerful device that could be used to reduce the amount of $1/f$ noise, while having high gain. Nevertheless, using higher gate voltages to turn it on is inevitable. The forward biased technique uses the bulk of the MOSFET to reduce the V_{TH} of the transistor allowing lower $V_{DS(sat)}$. Unfortunately, the V_{BS} activate a parasitic transistor producing undesired currents.

Finally, the bulk-driven technique uses the MOSFET's bulk as input terminal avoing in some degree the threshold limitation. However, the values of the V_{GS} must be at least the V_{TH} of the transistor in order to keep it on the saturation region.

All the presented techniques except the composite transistor, could work in strong-inversion and subthreshold region. Nevertheless, operating at low power supply voltages in strong-inversion brings some important limitations. The first limitation and perhaps the most important is the threshold voltage. In CMOS technology, the power supply must be at least $V_{DD}+V_{SS} \geq V_{tN}+V_{tP}$ such that the circuit work in strong inversion [33].

The second limitation is related to the decreased channel length of today and future submicron CMOS technologies that impact in much larger channel length modulation effect. This results in poor signal gains because the small signal output resistance of the MOSFETs has decreased [33].

The last limitation is the lack of good analog models for deep submicron technologies and for low voltage operation. This results in the use of longer channel lengths than necessary in order to have more reliable models. Consequently, the full perfomance of submicron technologies is not utilized [33].

Due to the trend of scaling the transistors down, techniques for operating circuits at supplies voltages as low as 0.5V are needed. Therefore, the techniques presented working in strong-inversion region are not suitable, since most of them require at least a supply voltage equal to the sum of the threshold voltage of the stacked transistors, in order to work properly. Those limitations generate the necessity to work at subthreshold zones, allowing the reduction of the supply voltage. Some of these techniques could be used as well in subthreshold operation, having advantages over working in strong-inversion. For example, the feedforward technique could be used to reduce the amount of threshold voltage, increasing the inversion level, while at ultra-low voltage supply voltage, the parasitic transistors are not turned on avoing undesired currents.

In conclusion, circuits working in the subthreshold region allow the reduction of power supply voltage, while some of the presented techniques could still be used to improve the performance of the circuits. The pertinent theory of transistors working in the subthreshold region is presented in the next section.

3.2   Subthreshold

When the V_{GS} in the MOS transistor is less than the threshold voltage (V_T), the device works in subthreshold or weak inversion. In the subthreshold region the I_D curve changes from quadratic behavior to exponential behavior.

Some assumptions are needed in order to develop the model. Channel effects are negligible. Generation currents in the drain, channel, and source depletion regions are negligible. Source and drain currents are equal, density of fast surface states and fluctations of surface potentials are all negligible.

Then the Barron's derivation [36] can be easily extended to the case of nonzero

source-to-substrate voltage. For a N-channel transistor:

$$I_D = S\mu U_T^2 (\frac{1}{2}q\epsilon_s n_i)^{1/2} e^{-3\phi/2U_T} \frac{e^{\psi_s/U_T}}{(\psi_s - U_T)^{1/2}} (e^{-V_S/U_T} - e^{-V_D/U_T}) \qquad (3.9)$$

where S is the geometrical shape factor of the transistor (W/L), μ is the mobility of carriers in the channel, U_T is the thermal voltage (kT/q), ϵ_s is the permitivity of the Si, ϕ is the bulk Fermi potential, ψ_s is the surface potential, V_S the source-to-substrate voltage, V_D the drain-to-substrate voltage, V_G is the gate-to-substrate voltage and I_D is the drain current.

Equation 3.9 is valid for:

$$4U_T + \phi + V_S < \psi_s < 2\phi + V_S \qquad (3.10)$$

On the other hand, the surface depletion capacitance C_d can be expressed as:

$$C_d = (\frac{1/2\epsilon_s q n_i}{\psi_s - U_T})^{1/2} e^{\phi/2U_T} \qquad (3.11)$$

Inserting 3.11 into 3.9, yields:

$$I_D = S\mu U_T^2 C_d e^{-2\phi/U_T} e^{\psi_s/U_T} (e^{-V_S/U_T} - e^{-V_D/U_T}) \qquad (3.12)$$

Due to the very slow variation of C_d with ψ_s, I_D shows an exponential behavior on ψ_s/U_T.

Variations of the gate-to-susbtrate voltage V_G are shared between the oxide capacitance per unit area C_{ox} and the semiconductor total surface per unit area C_s. Therefore,

$$\frac{\partial \psi_s}{\partial V_G} = \frac{C_{ox}}{C_{ox} + C_S} = 1 - \frac{C_G}{C_{ox}} \qquad (3.13)$$

where C_G is the gate capacitance per unit area.

According to 3.13, ψ_s is linearly depending on V_G in the range:

$$4U_T + \phi + V_S < \psi_s < 2\phi + V_S - 2U_T \tag{3.14}$$

Then inside this range I_D take the form of:

$$I_{DS} = I_{DO}\frac{W}{L}e^{V_G/nU_T}(e^{-V_S/U_T} - e^{-V_D/U_T}) \tag{3.15}$$

where I_{DO} is the characteristic current, n is the slope factor, U_T is the thermal voltage (kT/q) approximately 26mV at room temperature. The above equation is also applicable for p-channel transistors by changing the signs of V_G, V_S and V_D.

By definition, the gate transconductance can be found from equation 3.16:

$$g_{md} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{1}{nU_T}I_{DS} \tag{3.16}$$

The small signal source conductance can be found from equation 3.17 as:

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{1}{U_T}I_{DO}\frac{W}{L}e^{V_G/nU_T}e^{-V_S/U_T}e^{-V_{DS}/U_T} \tag{3.17}$$

When V_{DS} is less than $3U_T$ the device shows a poor linear behavior. On the other hand when $V_{DS} \gg 3U_T$ the conductance is almost constant [38].

3.3 Noise in CMOS transistors

3.3.1 Thermal noise

Thermal noise in resistances

Random movement of electrons in a conductor produce low voltage fluctuations that can be meassured through the conductor and they are independent of the current that flows into the component. Therefore, the thermal noise spectrum is proportional to the absolute temperature.

The resistance thermal noise model is depicted in the figure 3.7 and its power spectral density (PSD) is:

$$S_v(f) = 4kTR, \quad f \geq 0 \tag{3.18}$$

where $k = 1.38 \times 10^{-23} \ J/^oK$ is the Boltzman constant, T is the absoulte temperature and R is the resistor value. The thermal noise can be assumed as white noise, but it is only flat below $100THz$.
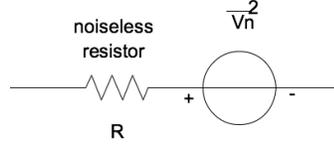
Figure 3.7: Voltage source thermal noise in resistor.

The thermal noise is:

$$\bar{V}_n^2 = 4kTR\Delta_f \tag{3.19}$$

where Δ_f is the frequency bandwidth of interest.

Analyzing the above equation, it can be inferred that the noise is given by $4kTR$, and this quantity is the square of the noise voltage (V^2/Hz).

Figure 3.7 shows that the thermal noise can be modeled by a voltage source in series with an ideal resistance. Figure 3.8 shows the current source noise model in parallel with the ideal resistance.
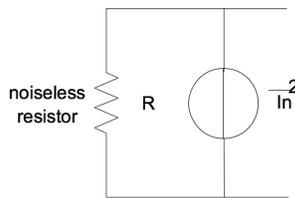
Figure 3.8: Current source thermal noise model.

Equivalent models of figures 3.7 and 3.8 are derived using the Thevenin's or Northon's theorems as follows:

$$\bar{V}_n^2/R^2 = \bar{I}_n^2 \tag{3.20}$$

therefore:

$$\bar{I}_n^2 = 4kT/R \qquad (3.21)$$

3.3.2 Thermal noise in MOSFETs

The channel is the most significative generator of thermal noise in MOSFETs. For long channel MOSFETs in saturatio, the noise can be modeled by a current source between drain and source terminals where its power spectral density (PSD) is:

$$\bar{I}_n^2 = 4kT\gamma g_m \qquad (3.22)$$

Figure 3.9 illustrates the MOSFET noise modelfor long channel transistors.
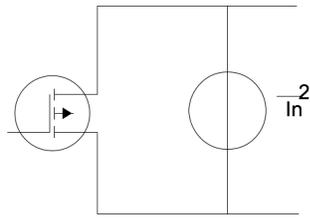
Figure 3.9: Thermal noise circuit model for a MOSFETs operating in saturation.

The γ coeficient for long channel transistors is equal to 2/3.

A MOSFET operating in the ohmic region has also thermal noise. The gate, source and drain materials has a finite resistivity, therefore they induce noise. For a transistor relatively wide, the source and drain resistances are tipically insignificant while the gate resistance is significant.
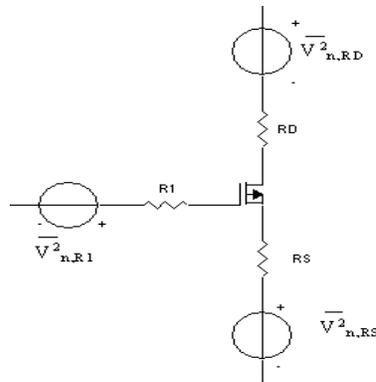
Figure 3.10: Thermal noise circuit model for a MOSFET operating in ohmic.

In figure 3.10, R_1 represents the resistance distributed in the gate, R_D is the drain resistance and R_S is the source resistance.

The thermal noise generated in the channel it is controlled only by the transconductance. The R_G can be diminished by layout techniques.

3.3.3 Flicker noise

The flicker noise is also know as $1/f$ noise. The flicker noise is generated when carriers in movement are either catched or released randomly in networks located at the $Si - SiO_2$ interface and into the gate oxide. As the current in the MOS devices, is a surface current, the MOS transistors are higly suceptible to the defects at the interface having the higher flicker noise among the active semiconductors devices.

The flicker noise can be modeled by a voltage source in series with the gate terminal and its equation it is given by:

$$\bar{V}_n^2 = \frac{K}{C_{OX}WL}\frac{\Delta f}{f}$$

(3.23)

where K is a constant in the order of $10^{-25}V^2F$.

The power spectral density is inversely proportional to the frequency. The inverse dependency on $W \times L$ suggests that in order to diminish the noise in the device its area must be larger.

To quantify $1/f$ with repect to the thermal noise, both PSD are ploted (figure 3.11). The $1/f$ noise corner frequency is the intersection between the thermal noise and flicker noise.

In figure 3.11, f_C is computed by:

$$f_C = \frac{K}{C_{OX}WL}gm\frac{3}{8kT}$$

(3.24)

Generally f_C depends in both transistor size and bias current.
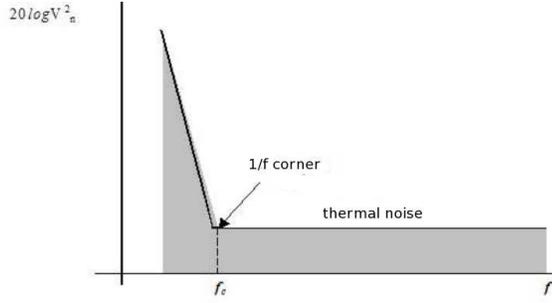
Figure 3.11: Flicker noise corner frequency.

3.3.4 Bulk-Driven noise model

The gain factor referring the channel noise current to the input distinguishes the bulk-driven case from the gate-driven case. Also, the bulk sheet resistance of the bulk-driven MOSFET can contribute to additional thermal noise. The noise considerations for the bulk-driven MOSFET are explicitly described in the bulk-referred mean-square noise voltage expression for the MOSFET [34].

$$\bar{v}^2_{nibulk} = \Big(\frac{8kT(1+\eta)}{3\eta^2 g_m} + \frac{KF}{2fC_{ox}WLK'\eta^2} + 4kT\Big(\frac{1}{N}\Big)^2\Big(\sum_{i=1}^{N} R_{bi} + \frac{1}{\eta^2}\sum_{i=1}^{N} R_{gi}\Big)\Big)\Delta f \quad (3.25)$$

where N is the number of gate fingers whitin an interdigitated MOSFET structure, R_{bi} is the effective series bulk resistance for ith gate channel, R_{gi} is the effective series gate-metal resistance of the ith gate, and $\eta = g_{mb}/g_m$. MOSFET white and flicker noises referred to the bulk terminal are described by the first and second terms, respectively. The last two terms above describe the thermal noise attributed to bulk and gate metal resistance.

In order to minimize bulk-referred noise for the bulk-driven MOSFET, the physical layout of the device should use bulk contacts generously. The contacts should be as close as possible to each gate finger, which minimize the noise contribution of bulk resistance determined by well sheet resistivity of approximately $2500\Omega/square$.

3.4 ADC architectures

This section breafly introduces the most common ADC architectures. Among the most popular we can find the Flash, Pipelined, Successive Aproximations, and Sigma-Delta ADCs. Figure 3.12 illustrates the trade-offs between the resolution and sampling

rates.
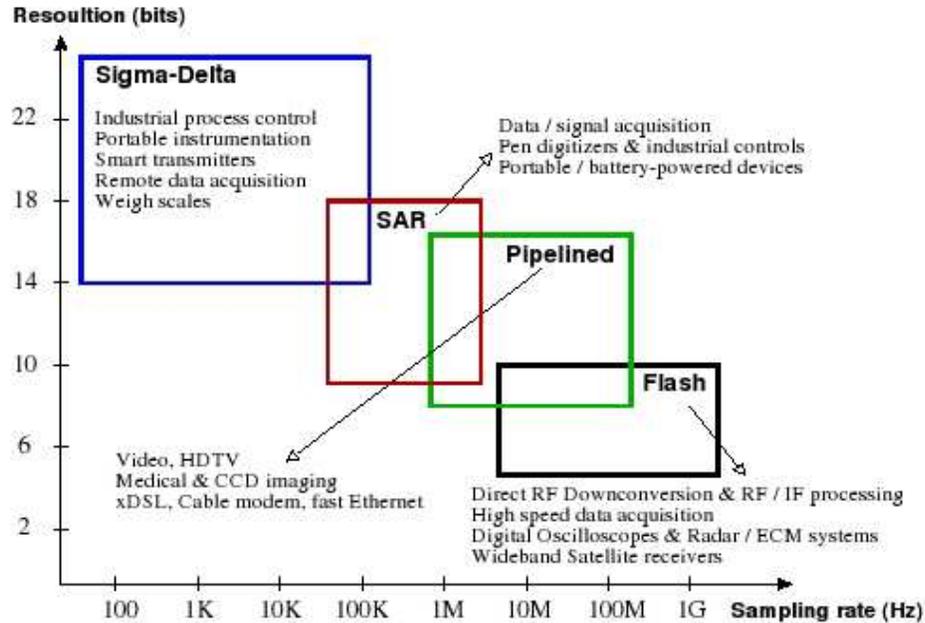
Figure 3.12: Trade-off between resolution and samplig rate.

3.4.1 Flash

The Flash ADC is also known as parallel ADC due to the parallel voltage comparator circuit architecture. This ADC has the fastest speed among all ADC architectures but it has a low resolution. Therefore, this ADC is used in high speed and large bandwidth applications. A schematic of this ADC is shown in the figure 3.13.
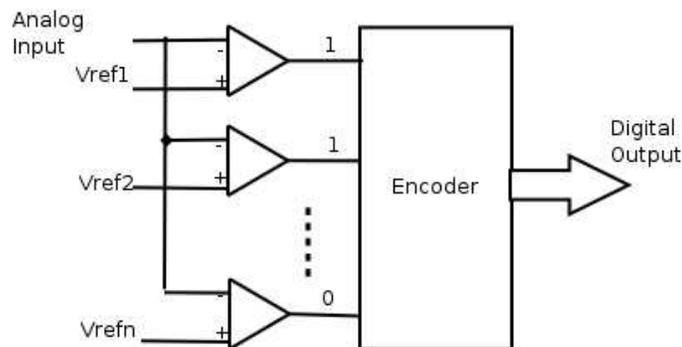
Figure 3.13: Block diagram of a flash ADC

As is depicted in figure 3.13, this architecture needs $2^n - 1$ comparators for a $n - bit$ ADC. For example, if the ADC has a resolution of $10bits$ then 1023 comparators are needed. Each of this comparators has a reference that is provided externally. The values are applied to the possitive terminal of a comparator. Each value is equally spaced by $V_{ref}/(2^n)$.

The flash ADC converts the analog signal into the digital code in one clock cycle that has two phase periods. During the first phase period the signal is sampled and applied to the comparator inputs. After that, during the second phase period, the digital encoding network determines the correct output digital word and stores it in a buffer [37].

Tipically the sampling frequencies can be as large as $1GHz$ for a 6bits word length.

3.4.2   Pipelined

The pipelined ADC consists at least of two low resolution flash ADC. Each stage has a S/H circuit to hold the residue from the previous stage and it is also used at the input of the pipelined ADC to avoid delay skew errors. The pipelined ADC block diagram is shown in figure 3.14.
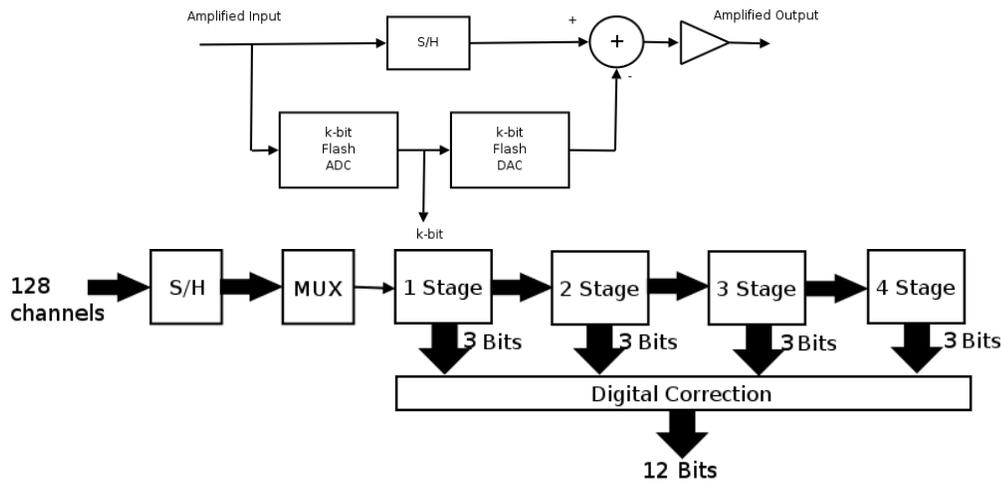
Figure 3.14: ADC pipelined with sample and hold before a Multiplexer and One stage of the pipelined ADC

After the hold cycle, the signal is applied into the low resolution flash ADC in order to generate a binary output. The binary output is converted back to the analog

level and it is substracted out from the input signal. The residue is amplified and applied to the next stage. The segmented binary output from each stage is time-aligned by a shift register.

This ADC has the disadvantages that the time needed to convert a sample is M clock cycles, where M is the number of stages. Pipelined ADC can be used in high speed with low resolution or in low speed with high resolution applications.

3.4.3 Successive approximation register (SAR)

The SAR ADC has been used in many data acquisition and industrial applications. It consists of a comparator, a DAC, and digital control logic. The function of the control logic is to determine the value of each bit in a sequential manner based on the output of the comparator. The figure 3.15 shows a SAR ADC.
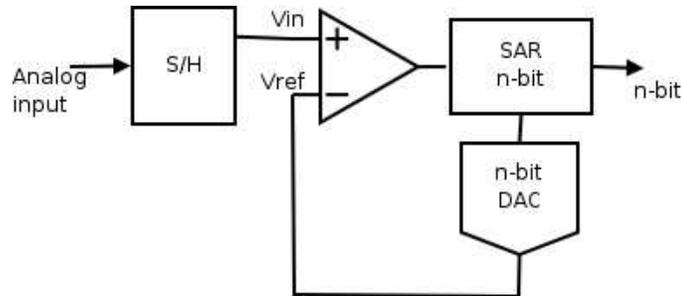
Figure 3.15: Block diagram of a SAR ADC

First the analog signal is sampled. Next, the digital control circuit assumes that MSB is 1 and all other bits of the word are 0. This word is applied to the DAC which provides the comparator with an analog signal of $V_{ref}/2$. If the comparator output is high then MSB is set to 1, otherwise MSB is set to 0. After that, the process continues assuming the next lower bit value equals to 1 and all remaining bits are 0. The value of this bit is determined in the same fashion. The process continues until all the values of the remaining bits have been decided.

For a *Nbits* SAR ADC a single comparator is needed, while the Flash ADC requires $2^N - 1$ comparators. Therefore, this technique produces a large saving in power dissipation compared to the Pipelined or Flash ADC. However, the Flash ADC only needs one clock cycle to convert the signal to a binary output and the SAR ADC needs N clock cycles to convert N bit word.

3.4.4 Sigma-Delta ($\Sigma\Delta$)

The $\Sigma\Delta$ ADC is also called oversampling ADC. Its resolution can be as high as $24bit$ but it is not the fastest ADC.

A $\Sigma\Delta$ ADC consists of two main blocks: the analog $\Sigma\Delta$ modulator and the another one is the digital decimator. The modulator includes an integrator, a comparator and a single bit DAC. The $\Sigma\Delta$ ADC architecture is shown in the figure 3.16.
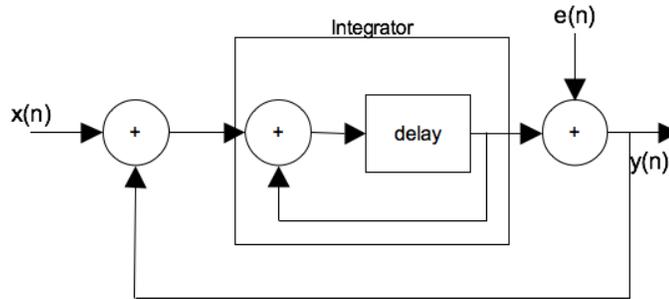
Figure 3.16: Block diagram of a $\Sigma\Delta$ ADC

The operation of $\Sigma\Delta$ ADC is as follows: when the integrator's output is positive, the quatizer feeds back a positive reference signal that is substracted from the input signal, in order to move the integrator output in the negative direction. Similarly, when the integrator output is negative, the quatizer feeds back a negative reference signal that is added to the incoming signal. The integrator therefore accumulates the difference between the input and quantized output signals and tries to maintain the integrator output around zero. A zero integrator output implies that the difference between the input signal and quantized output is zero. In fact, the feedback around the integrator and quantizer forces the local average of quantizer output to track the local average value of the input signal. For inputs around zero, the output oscillates between two levels. The local average of the output can efficiently be computed by a decimator.

The latency of this architecture is much grater than in other architectures.

3.5   Selecting an ADC architecture

For the AFE, an ADC with 16-bit resolution, capable of operating at 0.5V supply voltage and with low power consumption is required.

The Flash ADC would require 65535 comparators, therefore occupying a lot of area and having a large power dissipation. For a pipelined ADC, 4-bit Flash modules are needed. This would require 60 comparators and it would dissipate a moderate amount of power.

We propose a $\Sigma\Delta$ ADC architecture which is more suitable for the BCI applications, since only 2 integrators, and one comparator are required to obtain a 16-bit resolution. Moreover, the Continuous-Time (CT) $\Sigma\Delta$ achieves lower power consumptions than other ADCs with similar resolutions.

3.6 $\Sigma\Delta$ Modulation

The basic $\Sigma\Delta$ modulator consists of a loop filter, a quantizer and a feedback loop. A digital to analog converter inside the feedback loop transfers back the output of the quantizer to a digital signal. The linear $\Sigma\Delta$ modulator models the quantizer with a quantization gain k and a noise source. It is assumed that the DAC inside the feedback loop is ideal. In this system, there are two input signals, $x(n)$ and $e(n)$, and one output signal $y(n)$. The output of the $\Sigma\Delta$ modulator is:

$$Y(z) = H_x(z)X(z) + H_e(z)E(z) \tag{3.26}$$

where $H_x(z)$ represents the signal transfer function and $H_e(z)$ represents the quantization noise transfer function. The signal and noise transfer functions are:

$$H_x(z) = \frac{H(z)}{1 + H(z)} \tag{3.27}$$

$$H_e(z) = \frac{1}{1 + H(z)} \tag{3.28}$$

By properly choosing the loop filter transfer function H(z), the desired signal and noise transfer functions can be obtained within a certain band of interest. If the loop filter transfer function H(z) is designed to have a large gain inside the band of interest and small gain outside the band of interest, then the signal and noise transfer functions

are:

$$H_x(z) = 1 \tag{3.29}$$

$$He(z) = \frac{1}{1 + H(z)} << 1 \tag{3.30}$$

The signal can pass the $\Sigma\Delta$ modulator directly and the noise is greatly reduced inside the band of interest. This is called noise shaping. For example, if an integrator is chosen to be the loop filter, its transfer function is:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3.31}$$

Then the signal and noise transfer functions of the $\Sigma\Delta$ modulator can be calculated as:

$$H_x(z) = z^{-1} \tag{3.32}$$

$$He(z) = 1 - z^{-1} \tag{3.33}$$

The loop filter transfer function, signal and noise transfer functions of the $\Sigma\Delta$ modulator are shown in figure 3.17. It is seen the signal is passed to the output with a delay of a clock cycle, while the quantization noise is passed through a first-order low-pass filter. Combined with the oversampling, the SNR of the ADC can be improved. This is the principle of the first-order low-pass $\Sigma\Delta$ modulator.

In the time-domain, the integrator integrates the difference between the input signal and the feedback output signal of the $\Sigma\Delta$ modulator. The result of the integrator is then fed to the quantizer. The negative feedback tries to minimize the difference between input output signals of the $\Sigma\Delta$ modulator. As a result, the average of the output signal of the $\Sigma\Delta$ modulator is tracking the input signal. This behavior is illustrated in figures 3.18 and 3.19.

It can be seen that the output of the $\Sigma\Delta$ modulator tracks the input signal. In figure 3.18, a single-bit quantizer is used in the $\Sigma\Delta$ modulator. The benefit of using
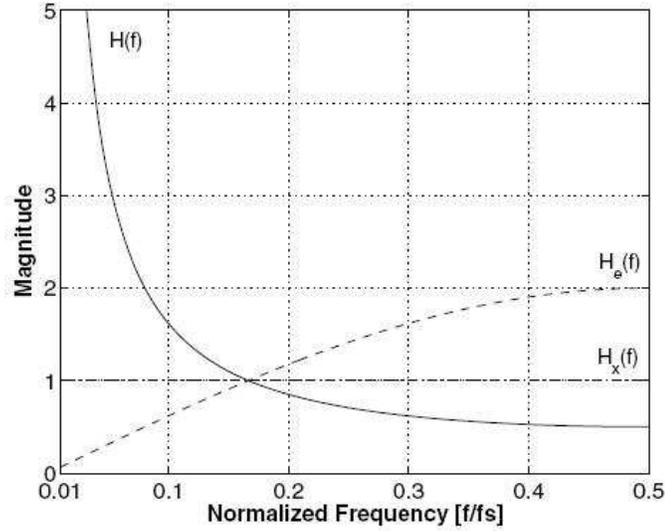
Figure 3.17: Loop filter, signal and noise transfer function of a $\Sigma\Delta$ modulator.

a single bit quantizer is that the single-bit quantizer secures a completely linear behavior. This is, since there are only two output states in the single-bit quantizer and two points define a straight line, therefore, the single-bit quantizer is inherently linear. The single-bit quantizer is widely used in oversampled ADCs applications. The four-bit quantizer generates less quantization noise power compared to the single-bit quantizer, as shown in figure 3.19. As a result, the average value of the output tracks the input signal much closer than the single-bit one.

By applying different loop filters inside the $\Sigma\Delta$ modulator, a high attenuation of quantization noise in a certain frequency band can be obtained. For example, when the loop filter is of second-order given by:

$$H(z) = -\frac{z^{-2}}{1 + z^{-2}} \tag{3.34}$$

Then the signal and noise transfer functions of the $\Sigma\Delta$ modulator are given by:

$$H_x(z) = -z^{-2} \tag{3.35}$$

$$H_x(z) = 1 + z^{-2} \tag{3.36}$$

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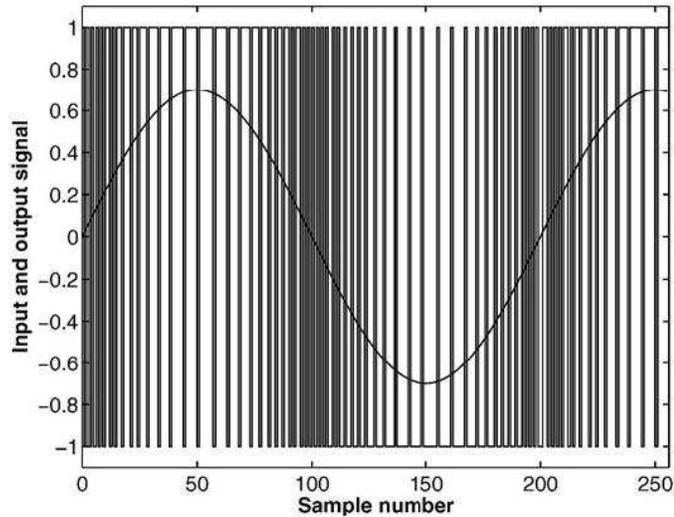
Figure 3.18: Input and output waveforms of a first-order $\Sigma\Delta$ modulator with single bit quantizer.

In this case, the loop filter, signal and noise transfer functions of the $\Sigma\Delta$ modulator are shown in figure 3.20. The quantization noise is suppressed in the frequency band around $f_s/4$. This type of modulator is useful in digitizing signals within a certain frequency range and finds its applications in wireless transceivers.

3.6.1 Performance Metrics for the $\Sigma\Delta$ ADC

For oversampled ADCs, since the operation principles are different from the Nyquist ADCs, different performance metrics are used to evaluate their performance. Some important specifications are discussed as follows.

Signal to Noise Ratio.

The SNR of a converter is the ratio of the input signal power to the noise power measured at the output of the converter. The maximum SNR that a converter can achieve is called peak signal-to-noise-ratio (SNR_p). The noise here should include the quantization and circuit noise.
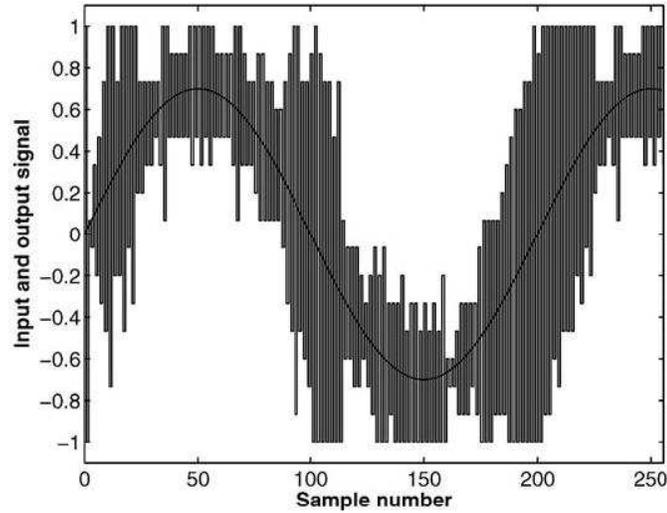
Figure 3.19: Input and output waveforms of a first-order $\Sigma\Delta$ modulator with a four-bit quantizer.

Signal to Noise and Distortion Ratio.

The $SNDR$ of a converter is the ratio of the input signal power to the power of the distortion components and noise measured at the output of the converter. The maximum $SNDR$ that a converter can achieve is called peak signal-to noise-and-distortion-ratio ($SNDR_p$).

Dynamic Range.

The DR is the ratio between the maximum input signal power that can be applied to the input of the converter without significant performance degradation, and the minimum detectable input signal power. A significant performance degradation of a converter is considered as the SNR drops more than $3dB$ below the peak SNR value. The minimum detectable input signal is the input power that the converter has for a SNR of $0dB$.

Overload Level.

The OL is the relative input amplitude where the SNR decreases by $3dB$ below the peak SNR.

These specifications are illustrated in figure 3.21. This figure shows the SNR and $SNDR$ of the $\Sigma\Delta$ modulator versus the amplitude of the signal applied to the input of the converter. Naturally, the SNR increases linearly with the increase of the input amplitude for an ideal converter. When the input signal amplitude is small, the distortion component is immerged in the noise floor of the converter. Therefore, the SNR
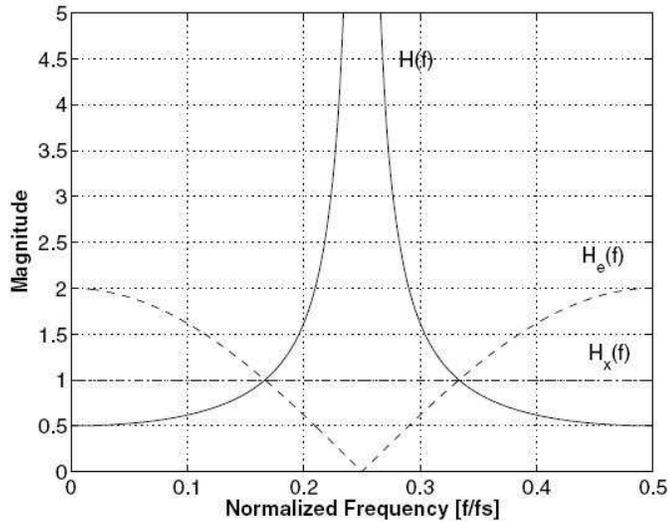
Figure 3.20: Loop filter, signal and noise transfer function of a band pass $\Sigma\Delta$ modulator.

and $SNDR$ curves are merged together. With the increase of the input amplitude, the distortion power becomes larger than the noise power and the $SNDR$ starts to decrease.
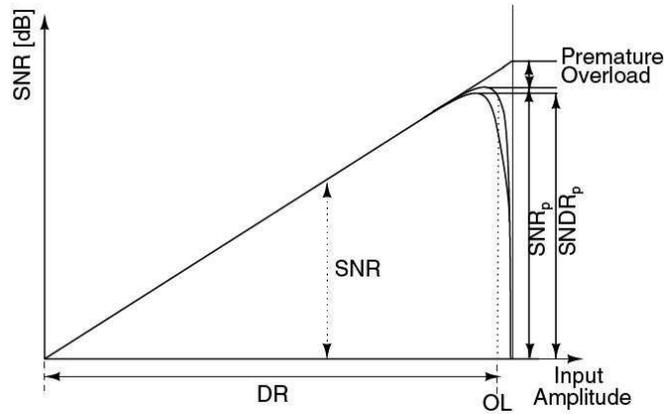
Figure 3.21: Definitions of the performance metrics used to characterize a $\Sigma\Delta$ ADC.

The $SNDR_p$ reflects the linear performance of the converter. Due to the distortion power, the $SNDR_p$ is smaller than the SNR_p for the same converter. After the converter reaches its SNR_p , the performance of the converter degrades drastically due to the overload of the modulator, where instability occurs. The overload is the special characteristics of the $\Sigma\Delta$ modulator. The overload level of a $\Sigma\Delta$ modulator defines the dynamic range of a converter. When the input amplitude is larger than a certain value, the $\Sigma\Delta$ modulator loop becomes unstable and the noise shaping disappears. Large quantization power in the signal band results into a drastic decrease of the SNR. In

the normal operation of the $\Sigma\Delta$ modulator, overload should be avoided.

3.6.2 Traditional $\Sigma\Delta$ ADC Topology

The $\Sigma\Delta$ ADC trades speed with resolution by means of oversampling and noise shaping, as discussed in the previous section. In this section, the single-loop $\Sigma\Delta$modulator is introduced. The relationship between the performance and the topology parameters is also discussed in this section. Then the cascaded $\Sigma\Delta$ modulator is presented. Trade-offs in different topologies are analyzed in detail as follows.

Single-Loop Single-Bit $\Sigma\Delta$ Modulators

The single-loop $\Sigma\Delta$ converter is defined with only one loop in the whole converter. The ability of noise shaping can be improved by increasing the order of the loop filter. Figure 3.22 shows a block diagram of a first-order single loop $\Sigma\Delta$ modulator. By inserting another integrator inside the loop a second-order $\Sigma\Delta$ modulator can be obtained as shown in figure 3.23.
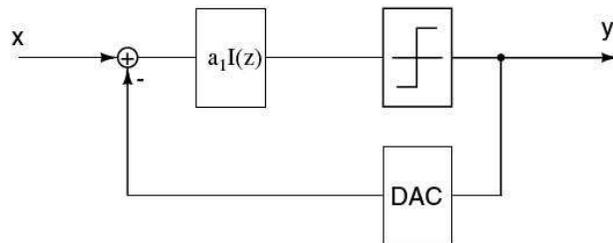
Figure 3.22: The first-order single-loop $\Sigma\Delta$ modulator.
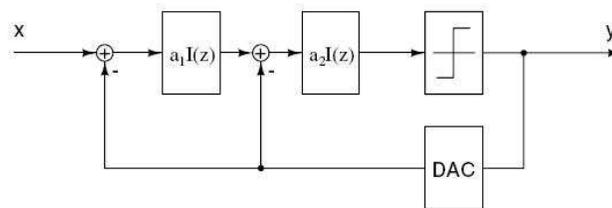
Figure 3.23: The second-order single-loop $\Sigma\Delta$ modulator.

Similarly, by inserting more integrator stages inside the loop, a higher-order $\Sigma\Delta$ modulator can be synthesized. Figure 3.24 shows a general block diagram of the n-th order single loop $\Sigma\Delta$ modulator. Consequently, as illustrated in figure 3.25 the noise transfer functions become steeper in the signal band for higher-order $\Sigma\Delta$ modulators. The signal transfer function of an ideal n-th order $\Sigma\Delta$ modulator can be expressed as:

$$H_x(z) = z^{-n} \tag{3.37}$$

$$H_e(z) = (1 - z^{-1})^n \tag{3.38}$$
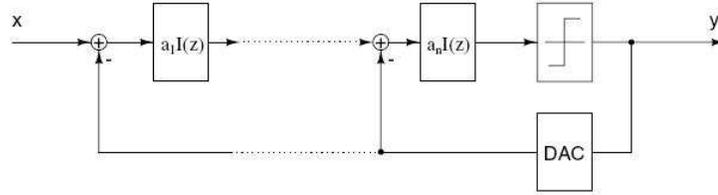
Figure 3.24: General block diagram of the $n-th$ order single-loop $\Sigma\Delta$ modulator.
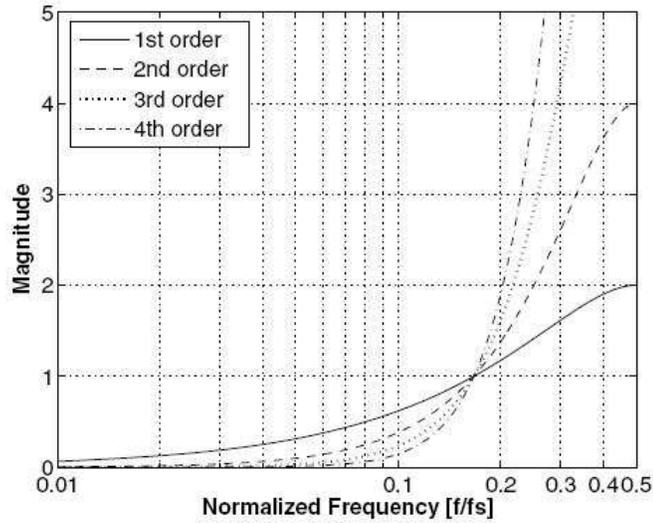
Figure 3.25: Ideal noise transfer functions of $\Sigma\Delta$ modulator.

The signal transfer function is only a n-th order delay and the noise transfer function is a $n-th$ order high-pass filter. The total quantization noise power inside the signal band is:

$$P_e = \int_{-f_s/2}^{f_s/2} S_e(f)|H(f)|^2 df \tag{3.39}$$

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$$P_e = \int_{-f_b}^{f_b} S_e(f)|1 - z^{-1}|^2 df \qquad (3.40)$$

$$P_e = \int_{-f_b}^{f_b} \frac{\Delta^2}{12 f_s} |\frac{j2\pi f}{f_s}|^{2n} df \qquad (3.41)$$

$$P_e = (\frac{\Delta}{2})^2 \frac{1}{3\pi(2n+1)} (\frac{\pi}{OSR})^{2n+1} \qquad (3.42)$$

Then the SNR_p of the $n-th$ order $\Sigma\Delta$ modulator can be calculated as:

$$SNR_p = \frac{3\pi}{2}(2^B - 1)^2(2n+1)(\frac{OSR}{\pi})^{2n+1} \qquad (3.43)$$

where B is the number of bits in the quantizer. This is the theoretical performance of an ideal $n-th$ order single-loop $\Sigma\Delta$ modulator. Compared to the first-order $\Sigma\Delta$ modulator, the noise shaping ability of the $n-th$ order $\Sigma\Delta$ modulator is greatly improved. However, the $\Sigma\Delta$ modulator loop can be unstable when the order is greater than two. The reason is that the higher loop-gain of the high-order loop filter causes an overload in the quantizer. Loop coefficients, $a_1...a_i$, are introduced to ensure the stability of a high order $\Sigma\Delta$ modulator. The constant a_i in front of the integrator is called the loop coefficient of this stage. Then the transfer function of the quantization noise is:

$$H_e(z) = \frac{1}{1 + k \sum_{i=1}^{n} \prod_{j-i}^{n} a_j(\frac{z^{-1}}{1-z^{-1}})^{n-i+1}} \qquad (3.44)$$

The amplitude of the noise transfer function can be approximated as:

$$|H_e(z)| \approx \frac{|1 - z^{-1}|^n}{k \sum_{i=1}^{n} a_i} \qquad (3.45)$$

Then the SNR of the $\Sigma\Delta$ modulator can be calculated as:

$$SNR_p = SNR_{p(ideal)}(k \prod_{i=1}^{n} a_i)^2 \qquad (3.46)$$

The quantization gain k is not determined for the single-bit quantizer, since it only responds to the polarity of the input signal. As a result, the gain of the last integrator is irrelevant to the operation of the $\Sigma\Delta$ modulator. In other words, the last loop coefficient can be chosen to have any value without affecting the performance of the $\Sigma\Delta$ modulator. For a single-bit $\Sigma\Delta$ modulator, the quantization gain k can be combined with the last integrator gain.

Normally the product of all coefficients is smaller than unity to ensure stability. Compared to the ideal $\Sigma\Delta$ modulator, the SNR degrades due to the introduction of the loop coefficients. By properly choosing the loop coefficients, the high order $\Sigma\Delta$ modulator can be made stable for the whole input range. However, the steepness of the noise transfer function is smother than the ideal one, which means that the noise shaping ability is degraded.

According to equation 3.43 and 3.46, the noise shaping ability of a $\Sigma\Delta$ modulator is determined by the following factors: oversampling ratio (OSR), order of the noise shaping (n), number of bits (B) of the quantizer and loop coefficients (a_i).

Oversampling ratio.

The SNR of the $\Sigma\Delta$ ADC can be increased by $(2n + 1)3dB$, or $n + 0.5bits$ by doubling the oversampling ratio, where n denotes the order of the loop filter. It is tempting to raise the oversampling ratio to increase the SNR of the $\Sigma\Delta$ modulator. However, it is restricted by the speed limit of the circuit and the power consumption. In practice, for the same performance, it is preferred to lower the oversampling ratio. Another driving force is the everincreasing bandwidth requirement, which also needs to lower the oversampling ratio. For high bandwidth converters, the oversampling ratio should be kept as low as possible. A lot of efforts have been made at the system level to lower the oversampling ratio and maintain the same performance.

Order of the loop filter.

The SNR of the converter can be increased by increasing the order of the loop filter n. However, while increasing the order of the loop filter, the stability problem is the prior concern. Smaller loop coefficients are then introduced to maintain the stability of the converter. Consequently, the noise shaping ability is compromised. Moreover, more circuits are also required to expand the order of the loop filter. Practically the order of the loop filter should be less than five.

Number of bits of the quantizer.

For the intrinsic linearity of the single-bit quantizer and the single-bit DAC in the feedback loop, many $\Sigma\Delta$ ADCs employ a single-bit quantizer. However, increasing the number of bits in the quantizer increases the SNR of the converter significantly. For each additional bit in the quantizer, the SNR of the converter increased by $6dB$. Moreover, by employing a multibit quantizer, the loop stability can also be improved and loop coefficients can be enlarged. Thus more powerful noise shaping ability is obtained. The linearity of the multibit DAC in the feedback loop directly affects the linearity of the converter. Since the feedback loop is connected directly to the input of the $\Sigma\Delta$ modulator, any non-linearity in the DAC can not be distinguished from the input signal and will be shown in the output. Therefore, the accuracy of the DAC should be at least as good as the $\Sigma\Delta$ converter in order not to degrade the performance of the $\Sigma\Delta$ converter.

Loop coefficients.

Loop coefficients are introduced to stabilize the $\Sigma\Delta$ modulator. However, they degrade the SNR of the $\Sigma\Delta$ modulator if not selected properly. The larger coefficients are, the better noise shaping ability can be achieved, and the higher the risk is to get instability for the $\Sigma\Delta$ modulator. A tarde off between the stability and the SNR exists which need to be considered. Figure 3.26 shows the output spectrum of single-loop single-bit $\Sigma\Delta$ modulator from the first-order to the fourth-order. In the first-order $\Sigma\Delta$ modulator, large idle tones are found in the spectrum of the output, therefore, modulators of this kind should be avoided.

3.6.3   Cascade Modulators

The augmentation of the loop filter to orders higher than two in single-stage modulators results in architectures which are prone to instability and thus they suffer from reduced scaling coefficients and reduced performance than an ideal higher order filter. As an alternative, cascaded or MASH (multistage noise shaping) topologies can
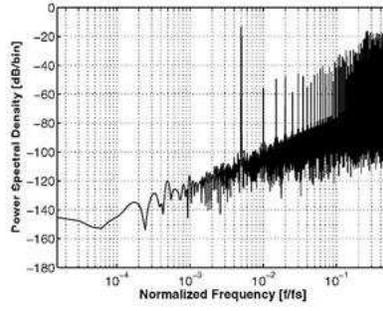
(a) Output spectrum of a first-order single-loop single-bit Σ-Δ modulator.
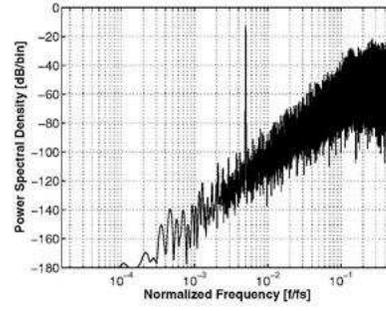
(b) Output spectrum of a second-order single-loop single-bit Σ-Δ modulator.
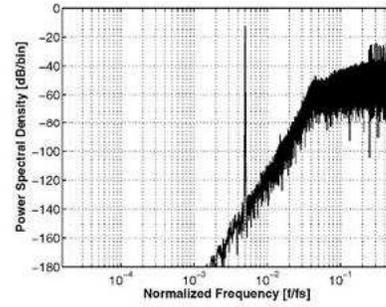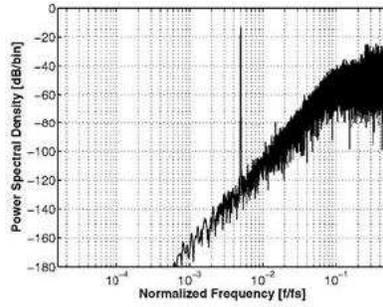
Figure 3.26: Figure (a) to (d): ouput spectrum of first-order to fourth-order single loop single-bit $\Sigma\Delta$ modulators.

combine high order noise shaping with the stability of low order single-stage modulators. They typically consist of several stages of lower-order $\Sigma\Delta$ modualtors, where each higher stage receives a representation of the quantization noise of the previous stage as its input. With an appropriate recombination of all digital outputs the quantization noise of all but the last stage can be canceled. An illustrative implementation of a general cascaded $\Sigma\Delta$ modulator with M stages is shown in figure 3.27. There, $H_i(z)$ are loop filters of order N_i, the quantizers have a $B_{int}|i - bit$ resolution and the DF_i are the digital recombination logic.

The operation principle is easily understood as follows: by modeling the quantizer of the ith stage as additive noise $e_i(n)$, the outputs of an exemplary two-stage cascaded modulator become:

$$y_1(n) = STF_1 u_1(n) + NTF_1 e_1(n) \tag{3.47}$$

$$y_2(n) = STF_2 u_2(n) + NTF_2 e_2(n) \tag{3.48}$$
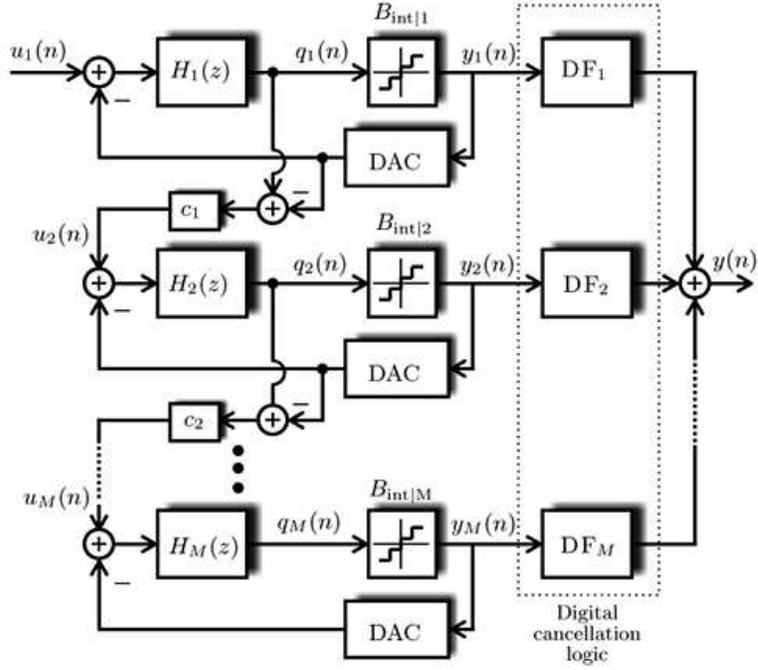
Figure 3.27: Cascade ΣΔ modulators.

For the input of the second-stage follows from figure 3.27:

$$u_2(n) = -c_1 e_1(n) \tag{3.49}$$

Thus, the overall output yields:

$$y(n) = y_1(n)DF_1 + y_2(n)DF_2 \tag{3.50}$$

$$y(n) = STF_1 u_1(n)DF_1 + NTF_1 e_1(n)DF_1 + c_1 STF_2(-e_1(n))DF_2 + c_1 NTF_2 e_2(n)DF_2 \tag{3.51}$$

The first objective of the digital cancellation logic is to eliminate the quantization noise of the first stage $e_1(n)$, which yields the condition:

$$DF_1 NTF_1 = c_2 DF_2 + STF_2 \tag{3.52}$$

$$DF_1 = STF_2|_d, DF = 1/c_1 NTF_1|_d \tag{3.53}$$

where the suffix $|d$ stands for an equivalent digital implementation of an analog transfer function. Doing so, the output of the cascaded modulator becomes:

$$y(n) = STF_1 STF_2|_d u_1(n) + 1/c_1 NTF_1|_d NTF_2 e_2(n) \quad (3.54)$$

Interestingly, apart from the interstage coupling coefficient c_1, (3.54) shows the ideal noise-shaping of second-stage cascaded $\Sigma\Delta$ modulator, because through the digital cancellation logic all but the last quantization noise is canceled completely. The quantizer error of the last stage is attenuated by a noise-shaping function of an order equal to the number of integrators N_{casc} in the overall cascade.

$$NTF_{casc} = \frac{(1 - z^{-1})^{N_{casc}}}{\prod_{i=1}^{M} c_i}, N_{casc} = \sum_{i=1}^{M} N_i \quad (3.55)$$

Thus, only the interstage coupling coefficients c_i, which prevent a possible overload of the input of the higher stages, decrease the performance below the ideal value. From 3.55 the integrated in-band noise of cascaded $\Sigma\Delta$ modulators can be derived to:

$$IBN_{casc} = \frac{\pi^{2N_{casc}}}{2N_{casc} + 1} \frac{\Delta_M^2}{12} \frac{1}{OSR^{2N_{casc}+1} \prod_{i=1}^{M-1} c_i^2} \quad (3.56)$$

where M is the total number of cascaded stages, N_i the order of the ith stage, c_i the interstage connection scalings, while ΔM is the quantizer step width of the last stage.

Principally, any stable single-loop $\Sigma\Delta$ modulator can be used as one stage in a cascaded modulator. But in practice there exist some restrictions: first, due to their intrinsic, unconditional stability, mostly first-order and second-order single-loop modulators are employed; by that, first stage first order modulators are avoided due to the tonal problems and an increased sensitivity to nonidealities.

3.6.4   Modulator Loop Filter Stability and Scaling

The above presented architectures provide the possibility to implement a noise-transfer and signal-transfer function with a certain filter characteristic. But together with considering about the loop filter implementation, the finding of such loop filter is of major interest.

The well-known drawback of single-loop single-bit $\Sigma\Delta$ modulators with orders higher than two is their tendency to instability. Thereby, stability is defined as a modulator condition, where all internal state variables, which are the integrator outputs, remain bounded over time. One measures to ensure stable operation in a possibly unstable control loop is the reduction of the loop-gain by appropriate filter scaling. The out-of-band gain of the ideal noise-transfer function increases heavily for increasing loop filter order N. Consequently, it starts to overload the quantizer input, which yields a significantly decreased effective quantizer gain kq.

Thus, after having chosen a certain filter characteristic through one specific architecture, and after having designed an optimized noise-transfer function, the analysis of stability is of major importance. Therefore, several methods can be used, beyond others simulation or calculation. While simulations are surely the final prove for performance, stability, and other effects like pattern noise, calculations give the starting point for the loop filter and can even provide a closer insight into the behavior of the chosen $\Sigma\Delta$ modulator: the method of root-locus plots has been adopted for that purpose in single-loop, single-bit $\Delta\Sigma$ modulators. Therefore, the unknown quantizer gain kq has been used as the variable gain of the root locus, which was found to be not defined in the case of a single-bit quantizer.

In the following, the STF of a third-order modulator with distributed feedback with $H(z) = I(z) = 1/(z-1)$ is exemplarily considered. From the open loop transfer function, the root-locus plot can be derived and is shown in figure 3.28 The scaling coefficients have been illustratively varied from no scaling toward an optimal set of scaling coefficients for a third-order, single-bit $\Sigma\Delta$ modulator.

Obviously, three poles start at dc ($z = \{1, 0\}$) for $kq = 0$. The real pole tends to $-\infty$, but actually it will always be on the real axis inside the unit circle. This is due to the effect of a stable limit cycle. The possible instability arises from the conjugate complex pair of poles, which leave the unit circle for small quantizer gains kq and enter it at a critical gain $kq, crit$: without scaling ($a_i = 1$), this pole pair never gets into the stable area, i.e., the modulator will not work. For smaller scaling coefficients, the branches of the root-locus plot are bent into the unit circle, and a conditional stability is achieved, if the quantizer gain is larger than the critical gain. On the other hand, a high single-bit quantizer gain corresponds to small quantizer input signals and thus to a limitation of the quantizer input, since the output is fixed to the reference $\pm\Delta/2$.

A feasible enhancement of this linear examination is the calculation of the quantizer gain kq in the case of zero input signal, i.e., $kq0$.
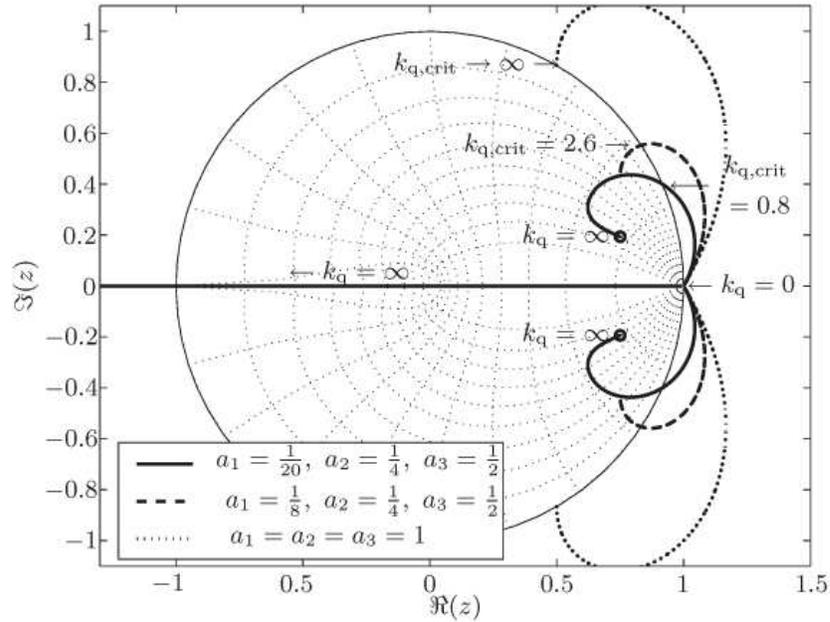
Figure 3.28: The first-order single-loop $\Sigma\Delta$ modulator.

This calculation can only be formally done for orders $N \leq 2$, while for higher order loop filters numerical methods have to be used. The determination of $kq0$ together with the critical gain $kq, crit$ then yields an estimate, if the modulator is conditionally or unconditionally stable or even completely unstable. The modulator will be:

- Completely unstable, if one of its poles is out of the unit circle for $kq = kq0$, i.e., if the quantizer gain for zero input signal causes poles outside the unit circle

- Unconditionally stable, if the locus of its poles is completely inside the unit circle for $kq \leq kq0$, i.e., if for all input amplitudes larger than zero all poles remain inside the unit circle

The given root-locus method is a linear approach to a strongly nonlinear system. Thus, this conditional stability and the finding of optimal scaling coefficients must be confirmed by behavioral simulations, and is usually based on two requirements: first, the modulator input signal has to be bounded into a specific interval, and second, the scaling has to prevent the noise-transfer function from peaking at high frequencies. As a rule of thumb, in it has been proposed to limit the out-of-band gain of the noise-transfer function of single-bit, single-loop modulators to 1.5.

3.6.5 CT ΣΔ Modulator

The Continuous Time ΣΔ Modulator was first mentioned in [39]. Here the signal is directly applied to the input of the modulator. The modulator consists of (see figure 3.29) a continuous time filter $H(s)$, that can be implemented as an active RC-filter using opertational amplifiers, operational transconductances amplifiers (OTA), gmC-filters or LC resonator structures; a quantizer that can be a sampled or a latched circuit, which is clocked at the modulator's samplig frequency f_s; and finally to close the loop a DAC, that can be a non-return to zero, a return to zero or a return to open type.
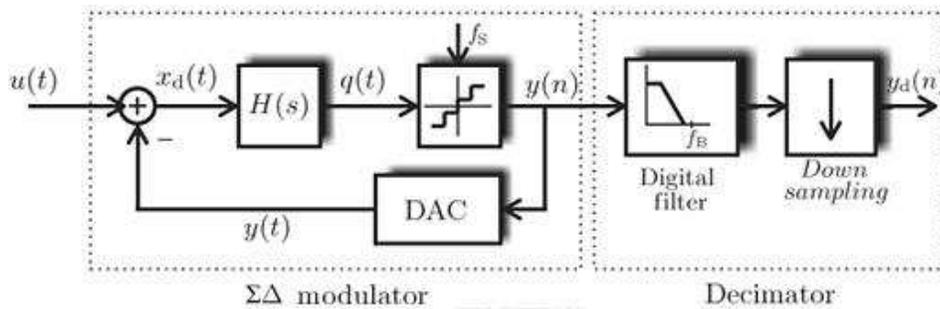
Figure 3.29: Continuous Time ΣΔ Modulator

The main diferences between Discrete Time (DT) modulators and CT modulators are attributed to the working principle.

Probably the key advantage of CT modulators over their DT counterpart, is that the sampling operation takes place inside the ΣΔ loop, in contrast to DT modulators, where a S/H circuit is placed at the input of the converter. In particular, if a large conversion bandwidth is desired, high-performance DT ΣΔ modulators are more difficult to design because of the stringent requirements on the fast, high-precision sample and hold building block.

Beyond this favorable feature of noise-shaped S/H errors, the shift of the sampling operation behind a continuous-time filter in the forward, signal path results in some degree of implicit antialiasing filtering. This can be the most emphasizing argument for choosing a continuous-time ΣΔ implementation.

Another performance limitation arises from the fact that the noise generated by the nonzero on-resistance of the switches and that of the amplifier is sampled together with the input signal. The overall accuracy of a switched-capacitor ΣΔ modulator is provided by using a small time constant compared to the clock period, therefore, a noise

cut-off frequency must be several times larger than the sampling frequency. Accordingly, a large amount of thermal noise is fold back into the signal band, constituting a fundamental resolution limit in SC $\Sigma\Delta$ modulators. Further performance limitations are introduced by the finite and signal-swing dependant on-resistances of the switches, glitch-induced errors and the generated digital switching noise.

Timing errors of the sampling clock have a significant impact on the DT modulator sampling operation.

Consequently, a common benefit that comes along with the sampled nature of the DT counterpart is its relaxed sensitivity to timing variations or delays within the feedback path, both of which are a strong performance limitation in CT modulators.

CT modulators dissipate lower power than the DT counterpart, since the sampling occurs only at the comparator stage.

3.6.6   DT to CT conversion of $\Sigma\Delta$ Modulators

A straight forward design procedure of a CT $\Sigma\Delta$ modulator loop filter should start with a DT loop filter $H(z)$. This way, design and simulation of the ideal CT $\Sigma\Delta$ modulator can be done in discrete-time to speed-up the overall design procedure. Consequently, it is highly recommended to start the CT modulator design with the synthesis of a DT modulator showing the required performance and to proceed with a DT-to-CT conversion in order to obtain the equivalent CT modulator.

The most common methods for this transformation are: the modified Z-transform or the impulse-invariant transformation.

The Impulse Invariant Transformation

Principally the DT-to-CT approach is based on the clocked internal quantizer of the CT modulator, which makes it a kind of DT system at this point. Following a DT-to-CT equivalence is achieved in equation 3.30, if the input to both quantizers $u(t)$ and $u(n)$ are the same at the sampling instants.

$$q(n) = q(t)|_{t=nTs} \tag{3.57}$$
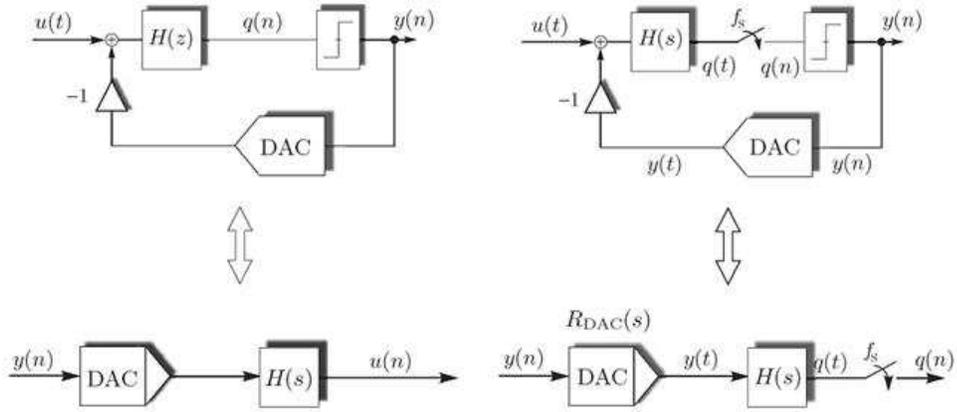
Figure 3.30: Loop filter representation for DT and CT modulators. Left: DT modulator. Right: CT modulator

Thus, the output bitstreams of both modulators and therefore the noise-performance are identical. In fig. 3.30, it is important to realize that the digital-to-analog converter in the feedback of the CT modulator acts as a discrete-to-continuous converter: while its input is a DT sample $y(n)$, its output is a continuous waveform $y(t)$, whose shape depends on the DAC transfer function RDAC(s). The above condition for the loop filter equivalence translates directly into:

$$\mathcal{Z}^{-1}\{H(z)\} = \mathcal{L}^{-1}\{R_{DAC}(s)H(s)\}|_{t=nTs} \tag{3.58}$$

In the time domain this leads to the condition:

$$h(n) = [r_{DAC} * h(t)|_{t=nTS}] = \int_{-\infty} \infty r_{DAC(\tau)}h(t-\tau)d_\tau|_{t=nTs} \tag{3.59}$$

where $r_{DAC}(t)$ as the impulse response of the specific DAC. This transformation between DT and CT domain is called the impulse-invariant transformation, because it makes the open-loop impulse responses equal at the sampling instances.

This transformation enables the design of a CT loop filter $H(s)$, which together with a specific DAC transfer function $RDAC(s)$, matches exactly the noise-shaping behavior of a DT loop filter $H(z)$. For a given architecture, the actual transformation can be performed using equation 3.59 for a specific loop filter arrangement.

Modified Z-Transform

Another method for establishing the CT loop filter is the modified Z- transform. This approach is based on the general Z- transform but extended, such that the discrete system behavior can be calculated at all instants of time, which is particularly important for mixed-signal, sampled-data systems with delay or multirate sampled systems.

In order to determine the equivalent CT loop filter for a certain modulator architecture with a certain feedback DAC pulse shape, the DT loop transfer function is computed and compared with the original DT loop filter function, in the same way as shown during the impulse invariant transformation. $H(s)$ will be multiplied with the desired DAC impulse response $RDAC(s)$ and according to the equation 3.60, the modified Z -transform is adopted on it.

$$H(z) = \sum_i \mathcal{Z}_{m_i}\{H(s)R_{DAC(s)}\} \tag{3.60}$$

The variable delay factor m_i is the key parameter of the modified Z -transform. The value m_i is normalized to the sampling period and bounded between $0 < m_i < 1$, whereas the extremes 0 confirm to the previous sample instant and 1 to the next. In general, for every time instance, in which the CT loop filter function changes its behavior, an additional delay factor is introduced. For example, this means for an ideal NRZ-DAC pulse:

- The first time instant is the rising edge of the DAC pulse at $t = 0$, which results in $m_1 = 1$- 0 $/TS = 1$.

- The second time instant is the falling edge at $t = 1\ TS$. Thus m_2 yields $m_2 = 1$-$TS/TS = 0$.

Next, each loop filter term is transferred with respect to all time instances m_i according to the table 3.1. Finally, a coefficient comparison with the original DT loop filter function leads to the wanted CT coefficients k_i.

3.6.7 DACs in CT $\Sigma\Delta$ Modulation

A wide variety of DAC pulses exists. Here the more common DACs, NRZ and RZ, are addressed. These DACs generate a rectangular pulse.

S-domain	$\mathcal{Z}_m$-domain equivalents
$\left(\frac{1}{s^2}\right)$	$\frac{mTs}{z-1} + \frac{Ts}{(z-1)^2}$
$\left(\frac{1}{s(s+s_k)}\right)$	$\frac{1}{s_k}\left(\frac{1}{z-1} - \frac{e^{s_k mTs}}{z-e^{-s_k Ts}}\right)$
$\left(\frac{1}{s^3}\right)$	$\frac{Ts^2}{2}\left(\frac{m^2}{z-1} + \frac{s_k Ts}{(z-1)^2} + \frac{2}{(z-1)^3}\right)$
$\left(\frac{1}{s^2(s+s_k)}\right)$	$\frac{1}{s_k^2}\left(\frac{s_k mTs-1}{z-1} + \frac{s_k Ts}{(z-1)^2} + \frac{e^{-s_k mTs}}{(z-e^{-s_k Ts})}\right)$
$\left(\frac{1}{s^4}\right)$	$\frac{Ts^3}{6}\left(\frac{m^3}{z-1} + \frac{3m^2+3m+3}{(z-1)^2} + \frac{6m+6}{(z-1)^3} + \frac{6}{(z-1)^4}\right)$
$\left(\frac{1}{s^3(s+s_k)}\right)$	$\frac{1}{s_k^3}\left(\frac{s_k^2 m^2 T_s^2/2 - s_k mTs+1}{z-1} + \frac{s_k^2 T_s^2(m+1/2)-s_k Ts}{(z-1)^2} + \frac{s_k^2 Ts^2}{(z-1)^3} - \frac{e^{-s_k mTs}}{z-e^{-s_k Ts}}\right)$

Non-Return to Zero DAC

The non-return to zero (NRZ) DAC produces an output pulse duration of $\beta = 1 + \alpha$, where β and α are normalized with respect to the sampling clock period T, i.e. the pulse is mantained during all the period. The amplitude of the pulse is quantized in two levels.

The major drawback is the intersymbol interference.
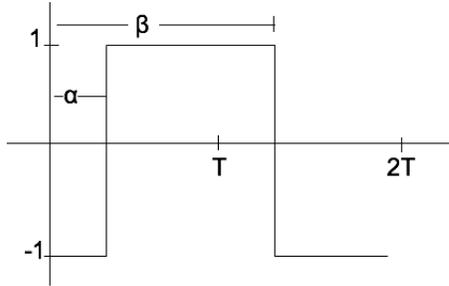
Figure 3.31: NRZ pulse.

Return to Zero DAC

The return to zero (RZ) DAC produce a pulse of $\beta < 1 + \alpha$, where β and α are normalized with respect to T. By using this DAC, the intersymbol interference is avoided, because before each input signal enters, the output DAC resets to a constant DC value.
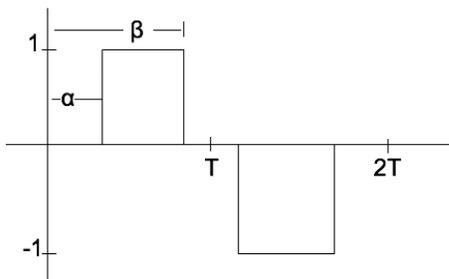
Figure 3.32: RZ pulse.

3.7 State-of-the-Art in CMOS Amplifiers and $\Sigma\Delta$ ADC

3.7.1 Low voltage amplifiers

Different techniques have been developed for low-voltage operation such as, charge-pump, low V_{TH}, bulk-forward biased, bulk-driven and devices working in weak inversion.

Amplifiers with bulk as input with supply voltage down to 0.8V has been reported in [35], [40], [41] and [42]. In [35] and [40] a complementary bulk-driven differential pairs are used in order to achieve rail-to-rail input operation. These amplifiers extensively uses bulk forward bias in order to reduce the transistor's threshold voltage. References [41] and [42] show amplifiers working at $0.6V$ supply voltage with transistors operating in weak inversion and having a bulk-driven differential input.

Recently two amplifiers working in subthreshold region with 0.5V power supply have been reported in [43]. The called Body-Input OTA, shown in figure 3.33, uses the bodies of a PMOS transistors as input terminals, and has an input common mode voltage of $0.25V$ in order to reduce the V_{TH} and increase the inversion level. The input transconductance is provide by the gm_b. A common mode feedback circuit has been added in order to perform the CM operation. Two stages are connected in cascade in order to achive higher gain. The open loop gain for this topology is $52dB$ with a BW of 2.5 MHz.

Another low voltage configuration called Gate-Input OTA is reported in [43]. This OTA is able to work 0.5V rail-to-rail, having a $62dB$ DC gain and $75\mu W$ of power dissipation. Figure 3.34 illustrates the circuit diagram of this device.

Reference [44] reports a more compact solution for gate-input OTA CM operation.
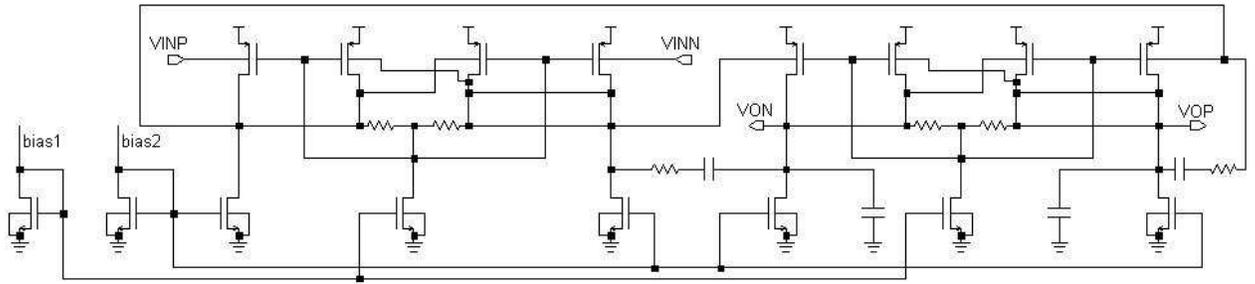
Figure 3.33: Ultra Low Voltage body-input OTA
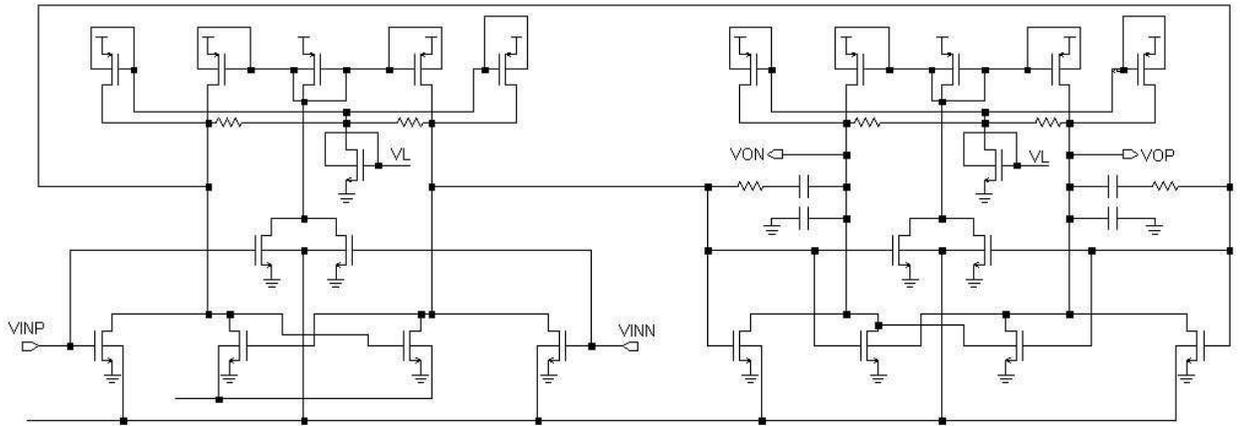
Figure 3.34: Ultra Low Voltage gate-input OTA

The proposed OTA has an intrinsic common-mode rejection. This OTA has an open loop gain of $55dB$ and BW of 8.7 MHz. Figure 3.35 shows the schematic diagram of this device.

Some other related OTAs are reported in [46], [47] and [48]. These OTAs are based in the gate-input and body-input OTA, contributing with different CMFF schemes.

A summary of these OTA specifications are shown in the table 3.2.

3.7.2 $\Sigma\Delta$ ADCs

Most of the ADCs used in bio-potential signal conversion are based upon the Sigma-Delta $\Sigma\Delta$ architecture [49],[50]. The $\Sigma\Delta$ ADC handles higher resolutions than pipelined or flash ADCs considering the same level of complexity. Table 3.3 illustrate some specifications of $\Sigma\Delta$ that are proposed for biomedical systems.

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Figure 3.35: CT ΣΔ Modulator

Table 3.2: Low-voltage amplifiers specification.

Supply	Gain	BW	Consumption	Noise	Process	Ref
0.5V	52dB	2.5MHz	110μW	280$\frac{nV}{\sqrt{Hz}}$@10KHz	0.18μm	[43] (body)
0.5V	62dB	10MHz	75μW	225$\frac{nV}{\sqrt{Hz}}$@10KHz	0.18μm	[43] (gate)
0.5V	55dB	8.7MHz	77μW	157$\frac{nV}{\sqrt{Hz}}$@10KHz	0.18μm	[44]
0.5V	61dB	41MHz	510μW	28$\frac{nV}{\sqrt{Hz}}$@10KHz(in)	0.18μm	[45]
0.5V	65dB	550KHz	28μW	675$\frac{nV}{\sqrt{Hz}}$@10KHz (in)	0.18μm	[47]
0.5V	90dB	100KHz	1.5μW	–	0.35μm	[48]

References [55] and [56] report an ultra-low voltage third order CT ΣΔ Modulators. Reference [55] propose a Return to Open (RTO) architecture in order to allow the realization of return-to-zero signaling feedback DAC with ultra-low supply voltage. The RTO is needed to avoid inter-symbol interference (ISI). The OTA of the modulators are based in Body-Input OTA and the comparator is a gate-clocked that uses the body as an input terminal. Figure 3.36 shows the modulator which works with power supply voltages of 0.5V.

Reference [57] presents a fourth order CT ΣΔ modulator, with a $4bit$ internal quantizer operating at $300MHz$. The integrators are resonators and this modulator achieves a resolution of 11$bits$.

Reference [58] describes a low voltage low noise third order modulator where $G_m - C$ integrators are implemented by a simple inverter and capacitors. This modulator achieves a SNR of $77dB$ with a 1.5V supply voltage.

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Table 3.3: DT ΣΔ ADC specification.

Supply	Resolution	OSR	Consumption	Process	Ref
1.5V	12 bits	5MHz	.85mW	0.18 μm	[49]
3V	12 bits	50KHz	2.1mW	0.8 μm	[50]
5V	10.5 bits	1.63MHz	60mW	0.8 μm	[51]
1.1V	14 bits	16KHz	.5mW	0.35 μm	[52]
2.5V	16 bits	–	.065mW	4 μm	[53]
1.8V	10 bits	1MHz	.4mW	0.18 μm	[54]
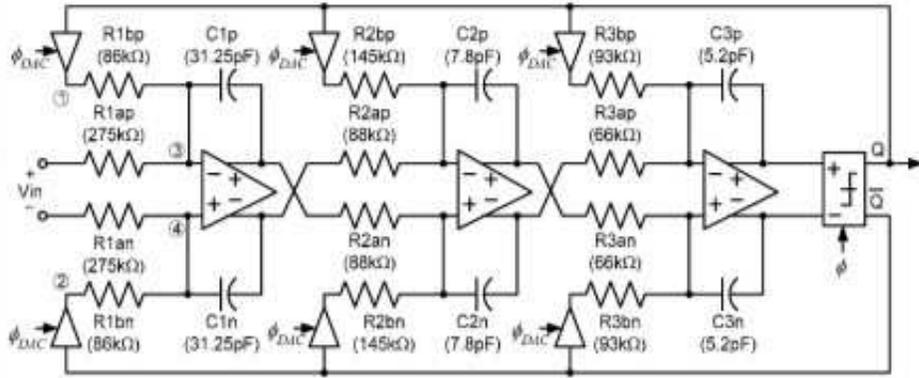
Figure 3.36: CT ΣΔ Modulator

Table 3.4 summarizes key specifications of low-voltage low-power CT ΣΔ ADCs.

Table 3.4: CT ΣΔ ADC specification.

Supply	SNDR	BW	Consumption	Process	Ref
0.5V	74dB	25KHz	$300\mu W$	$0.18\mu m$	[55]
0.5V	81dB	25KHz	$300\mu W$	$0.18\mu m$	[56]
1.5V		15MHz	$70mW$	$0.13\mu m$	[57]
1.5V	74dB	600KHz	$6mW$	$90nm$	[58]

3.8 Conclusions

In this chapter, the theoretical background was adress. In the first section, the trends in the future CMOS technologies were shown. Moreover, this section presented the main low voltage circuits techniques: the composite transistor, the lateral BJT,

the forward-biased bulk-source and the bulk-driven technique. However, if these techniques are operating in strong-inversion, there is a main limitation, the supply voltage could not be lower than the sum of the threshold voltage of the stacked transistors. Concluding, that operating these circuits in subthreshold region, the reduction of the supply voltage could be possible.

In section **2**, the theory of CMOS transistors operating at subthreshold region was presented, in where was stated that the drain current behavior is exponential, and that the devices needs at least $3U_T$ in order to have good linearity. The therory of noise in CMOS devices was presented in section **3**, in which the flicker noise and white noise were introduced.

In sections **4**, **5** and **6**, the ADC architectures, the selection of the ADC architecture and the theory of the selected ADC were respectively presented. The selected architecture is the CT-$\Sigma\Delta$ ADC. It was selected due its good performance for high resolution and low power consumption.

Finally, the state-of-the-art was presented in section **7**. A summary table of the most promising circuits was presented in this section.

Chapter 4

A 0.35μm CMOS Analog Front End Design

Le chapitre 4 présente l'analyse et les résultats de simulation de l'AFE proposé, ainsi que son implémentation dans la technologie 0,35μm CMOS. L'AFE consiste en trois étages, le premier étage est l'amplificateur opérationnel de Transconductance Ultra-Bas-Tension (ULV) (OTA), le second étage est le modulateur de CT $\Sigma\Delta$ (modulateur Sigma-Delta à temps continu) du second degré et le dernier étage est le filtre numérique de décimation du convertisseur. Les étages analogiques (pré-amplificateur et modulateur) sont optimisé pour fonctionner avec une tension aussi basse que 0,5V. D'autre part, l'étage numérique (filtre de décimation) fonctionne quant à lui avec une tension d'alimentation de 1V. Cette différence de tension d'alimentation a nécésité la conception d'un module d'interface, entre le modulateur et le Decimateur, pour interpréter le bitstream "0" ou "1") issu du modulateur par le Decimateur. Cette interface est conçue en utilisant un simple inverseur CMOS avec une tension de seuil de 0,3V. L'étage de decimation est basée sur un filtre FIR de 64 coeffcients.

Dans la section 4,1 la description détaillée ainsi que les résultats de simulation de l'OTA ultra basse tension proposé sont présentés. Cet OTA est une contribution originale, qui permet un fonctionnement avec une faible puissance consommée compatible avec les contraintes imposée par un système BCI embarqué. Les simulations montrent que l'amplificateur proposé est très approprié pour des applications biomédicales, en raison de sa faible dissipation de puissance et de son gain élevé. Dans cette section les circuits de polarisations sont également présentés. Ces circuits sont utilisés pour rendre le fonctionnement de l'OTA indépendant les variations de process et de température.

La section 4,2 présente le modulateur temps continu de basse tension (CT) $\Sigma\Delta$ CAN. Dans un premier temps, le choix du modulateur est présenté. Puis, l'analyse du modèle idéal du modulateur CT-$\Sigma\Delta$ est présentée : obtention d'un SNR de 98dB en utilisant un sur-échantillonnage (OSR) de 150. Dans la sous-section 4,2,2, le circuit du modulateur est détaillé. L'OTA utilisé pour l'étage d'intégrateur est basé sur l'amplificateur actuel de source de courant (CSA). Le comparteur de type D-latch à bit unique est présenté, suivi par la description du convertisseur numérique-analogique

de type "retour au zéro" (RZ-CNA). Le decimateur basé sur une architecture de filtre FIR est détaillé dans la dernière partie de cette sous-section. En sous-section 4,2,3, les résultats de simulation sont donnés, en particulier un SNR de $92dB$ est obtenu. Finalement, dans la section 4,3 les conclusions sur la conception de l'AFE sont présentées.

Introduction

This chapter presents the analysis and the simulation results of the proposed Analog Front End (AFE) implemented using the $0.35\mu m$ CMOS technology process.

Figure 4.1 illustrates all the blocks that integrate the whole system. The first stage is the Ultra-Low-Voltage (ULV) Operational Transconductance Amplifier (OTA) and the second stage is the second order CT $\Sigma\Delta$ Modulator.
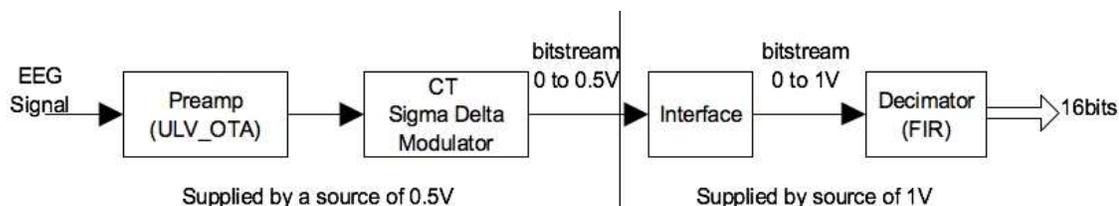
Figure 4.1: Proposed Analog-Front-End

The preamplifier and the modulator are able to operate with a 0.5 of supply voltage. The last two stages of the AFE operates with a supply voltage of 1V. Moreover, an interface module, between the Modulator and Decimator, is necessary to interpret the bitstream (either "0" or "1") by the Decimator. This interface is designed using a simple inverter with a threshold voltage of 0.3V. The decimator stage is based on a FIR filter using 64 coefficients

In the following sections, the AFE will be explained in more detail.

4.1   Ultra-Low-Voltage Amplifier

Differential pairs are commonly used as input stages in voltage amplifiers. In the case of an ULV-OTA the tail current must be removed in order to have more voltage headroom [44], however a Common Mode Feedforward (CMFF) must be added to improve the Common Mode (CM) operation and CM rejection ratio (CMRR). The CMFF module is a transconductor whose differential transconductance is ideally zero. This

method is shown in figure 4.2.

The ULV amplifier configurations reported in the literature are based on current source amplifiers (CSA). Here, we propose a two-stage topology which is able to operate with 0.5 supply voltage where the first stage is similar to the folded cascode (FC) OTA and the output stage is a CSA to achive greater output swing.

Figure 4.2: ULV OTA block diagram.

4.1.1   First OTA stage

A configuration similar to FC was chosen for the first stage and a CSA for the output stage of the ultra-low voltage OTA's design. The proposed circuit is shown in figure 4.3.

Figure 4.3: Ultra Low Voltage OTA

The main difference between the classical FC and the proposed configuration is that the former has a stack of 4 transistor (figure 4.4) at its output, to obtain a high

output resistance while the proposed topology only has a stack of 3 transistors. Assuming that all the devices are working in saturation ($V_{DS_{sat}} \geq 0.1V$), and using 4 transistors, an ultra-low voltage supply produces an extremly reduced ouput swing. Hence, to increase the output swing and have relatively higher gains 3 transistors are stacked. Nevertheless, an extra stage is needed to improve the ouput swing.

Figure 4.4: Classical Folded Cascode OTA configuration.

In the proposed topology, a differential PMOS pair is used as input ($M1_a$ and $M1_b$) in order to reduce the noise, the bulks of the transistors are forward biased to reduce the V_{TH}, increase the inversion level [43] and set the output common mode. The $V_{cm,o}$ is set to $V_{DD}/2$ to have maximum output swing. Since the EEG signal has small offset ($\sim 1 \ \mu V$), the input transistors are always on.

Transistors M3a and M3b consitute two symmetric common gate amplifiers (CGA). The current sources M_{2a} and M_{2b} provide the current bias to the CGA and are also the current sources for the differential input. Both CGAs have an active load (current source) composed by M_{4a} and M_{4b}. Bulks of M_4 are connected to the gate and bulks of all the NMOS are conected to a biasing circuit that generates a voltage of $VDD/2$ in order to reduce the V_{TH}.

Due to I_{tail} has been removed from the design in order to provide voltage headroom, devices M_5, M_6 and capacitors C_{c1a}, C_{c1b} are added to perform CM operation and achieve good CMRR.

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The small signal model of the OTA is shown in figure 4.5. Using nodal analyzis we have:
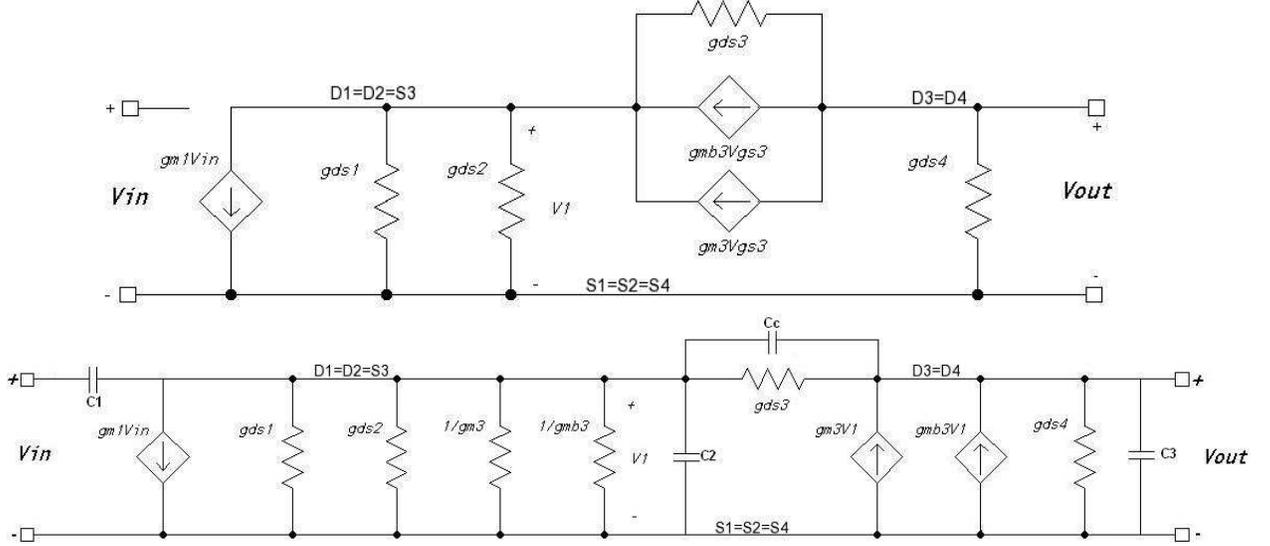

Figure 4.5: OTAs small signal model

$$-g_{m1}V_{in} = (g_{ds1} + g_{ds2} + g_{mb3} + g_{m3} + g_{ds3})V_1 - g_{ds3}V_{out} \qquad (4.1)$$

$$-(g_{m3} + g_{mb3} + g_{ds3})V_1 + (g_{ds3} + g_{ds4})V_{out} = 0 \qquad (4.2)$$

By solving for V_{out}/V_{in} the DC gain of this stage is obtained:

$$A_{v_1} = \frac{-g_{m1}(g_{ds3} + g_{m3} + g_{mb3})}{g_{ds3}(g_{ds1} + g_{ds2}) + g_{ds4}(g_{ds1} + g_{ds2} + g_{ds3} + g_{m3} + g_{mb3})} \qquad (4.3)$$

assuming that $(g_{ds1} + g_{ds2}) >> (g_{m3} + g_{mb3} + g_{ds3})$ then the DC-gain becomes

$$A_{v_1} = \frac{-g_{m1}(g_{ds3} + g_{m3} + g_{mb3})}{(g_{ds1} + g_{ds2})(g_{ds3} + g_{ds4})} \qquad (4.4)$$

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By decreasing the current in the CGA, the output resistance increases, enhancing the gain of this stage, A_{v_1}. However, the unit gain-bandwidth (GBW) is reduced.

The input referred white and flicker noise for this stage is:

$$\overline{V}^2_{n_{in}} = 2\overline{V}^2_{n_1} + 2\left(\frac{g_{m2}}{g_{m1}}\right)^2 \overline{V}^2_{n_2} + 2\left(\frac{g_{m3}}{g_{m1}}\right)^2 \overline{V}^2_{n_3} + 2\left(\frac{g_{m4}}{g_{m1}}\right)^2 \overline{V}^2_{n_4} \tag{4.5}$$

and

$$\overline{V}^2_{n_i} = \frac{2q}{I_D}\left(\frac{nkT}{q}\right)^2 + \frac{K_F}{C^2_{ox}W_i L_i f} \tag{4.6}$$

where i is the number of the device, $k = 1.38 \times 10^{-23} J/^oK$ is the Boltzman constant, n is the slope factor, I_D is the drain current, T is the temperature, K_F is the flicker noise process dependent constant, C_{ox} is the oxide capacitance, f is the frequency and W_i, L_i are the transistor dimensions. The first expression of the equation 4.6 denotes the white noise and the second the flicker noise.

The frequency behavior of the proposed ULV-OTA can be obtained by analyzing the figure 4.5, including the capacitors. C_1 includes C_{gd1}, C_2 includes C_{gd2}, C_{bd2}, C_{gs3} C_{bs3} and C_3 includes C_L, C_{gd3}, C_{bd3}, C_{gd4}, and C_{bd4}.

$$-(g_{m1}-sC_1)V_{in} = (g_{ds1}+g_{ds2}+g_{mb3}+g_{m3}+g_{ds3}+s(C_2+C_c))V_1-(g_{ds3}+sC_c)V_{out} \tag{4.7}$$

$$-(g_{m3} + g_{mb3} + g_{ds3} + sC_c)V_1 + (g_{ds3} + g_{ds4} + s(C_3 + C_c))V_{out} = 0 \tag{4.8}$$

By solving for $V_{out}(s)/V_{in}(s)$ gives:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{-g_{m1}(g_{ds3} + g_{m3} + g_{mb3} + sC_c)}{K}\right)\left(\frac{1}{1 + as + bs^2}\right) \tag{4.9}$$

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where

$$a = A/K$$

$$b = B/K$$

and

$$A = (g_{ds3} + g_{ds4})C_2 + (g_{ds1} + g_{ds2} + g_{ds4})C_c + (g_{ds1} + g_{ds2} + g_{ds3} + g_{m3} + g_{mb3})C_3,$$

$$B = C_3C_2 + C_3C_c + C_2C_c,$$

$$K = g_{ds3}(g_{ds1} + g_{ds2}) + g_{ds4}(g_{ds1} + g_{ds2} + g_{ds3} + g_{m3} + g_{mb3})$$

the poles can be obtained from,

$$p_1 = -\frac{K}{A}$$

$$p_2 = -\frac{A}{B}$$

assuming that $C_c \gg C_3$, $C_3 \gg C_2$ then the dominant pole is:

$$p_1 = -\frac{g_{ds3} + g_{ds4}}{C_c} \tag{4.10}$$

assuming that $(g_{ds1} + g_{ds2}) \gg g_{ds4}$ the nondominant pole is given by:

$$p_2 = -\frac{g_{ds1} + g_{ds2}}{C_3} \tag{4.11}$$

Then BW defined as $Av|p_1|$ is:

$$BW = \frac{g_{m1}(g_{m3} + g_{mb3} + g_{ds3})}{(g_{ds1} + g_{ds2})C_c} \tag{4.12}$$

In the design, g_{m1} is set larger than g_{m2} and g_{m4}, in order to reduce the total input referred noise. Only the noise of the first stage is computed, since the gain is high enough to overcome the equivalent noise of the output stage.

The transistor dimensions of the first amplifier's stage are shown in the table 4.1.

Table 4.1: OTA transistors dimensions.

Device	W (μm)	L (μm)
$M1_{a,b}$	604	0.35
$M2_{a,b}$	80	0.35
$M3_{a,b}$	10	0.35
$M4_{a,b}$	70	0.35
$M5_{a,b}$	2	0.35
$M6$	28	0.35

The EEG signal has frequencies from $0.5Hz$ to $100Hz$, therefore the amplifier must have a bandwidth larger than $100Hz$. The simulation shows that the first stage has a differential open loop gain for this stage is $53dB$ with a BW of $5.2MHz$ and PM of 91.7^o. The open loop gain is shown in figure 4.6.
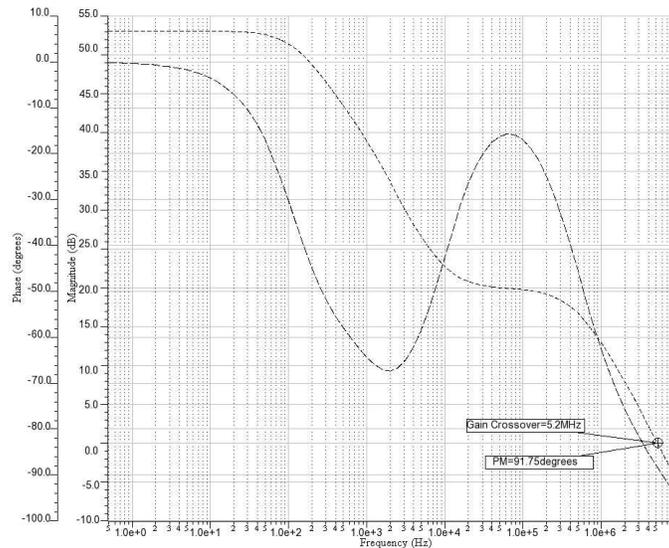

Figure 4.6: First stage open loop gain.

By adding the CMFF a CMRR of $44dB@10Hz$ and $36.8dB@100Hz$ was achieved.

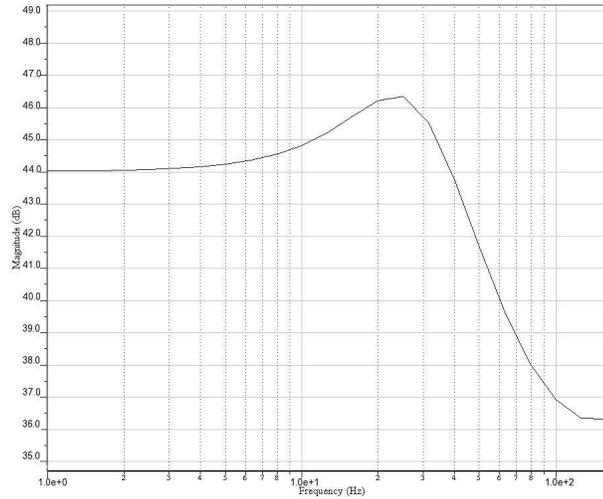Figure 4.7 shows the CMRR curve for the frequency range from 1 to 100Hz.

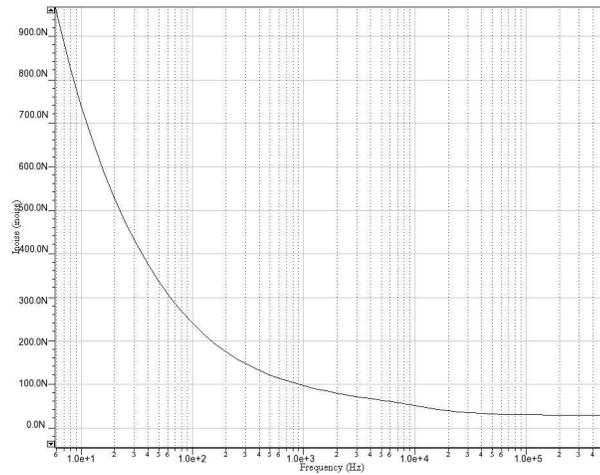Figure 4.7: Common mode rejection ratio.

Figure 4.8: Total Input referred noise.

Figure 4.8 illustrates the OTA's input referred noise in the frequency range of 1 to $100KHz$. The simulation uses typical $0.35\mu m$ CMOS models and shows just $240nV/\sqrt{Hz}$ of input referred noise at $100Hz$.

Figure 4.9 shows the OTAs first stage layout where each transistor is labeled and requiring and overall area of 175×113 μm^2.
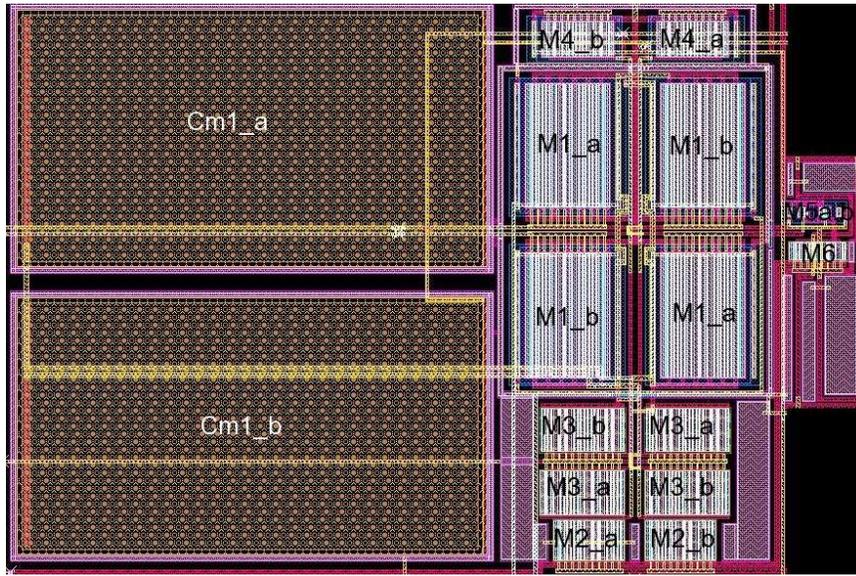
Figure 4.9: First stage OTA's layout.

4.1.2 Output OTA stage design

The second stage follows a tandem configuration with the first stage and is used to achive higher gains while maximizing the output swing.

Devices M_{7a} and M_{7b} are used as input transistors. The bulk of these devices fixes the output common mode operation to $V_{DD}/2$. Transistors M_8 are current sources. Figure 4.10 shows the diagram of the Common Source Amplifier (CSA) working in the subthreshold region.
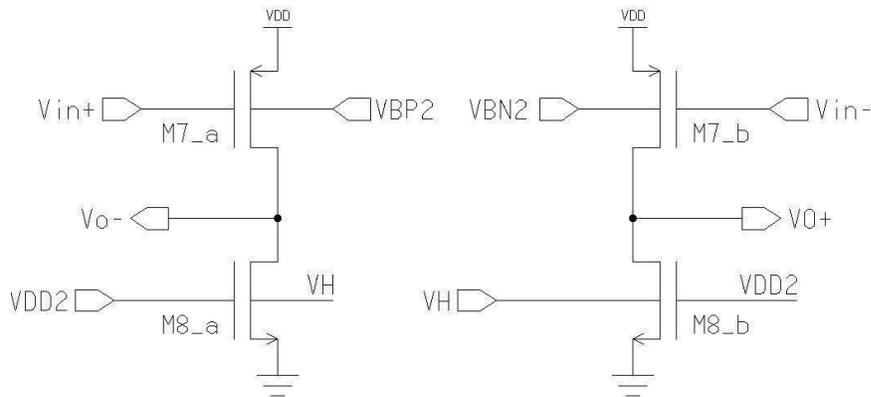

Figure 4.10: Output OTA.

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The gain of this stage is obtained by analizing the small signal model (figure 4.11):
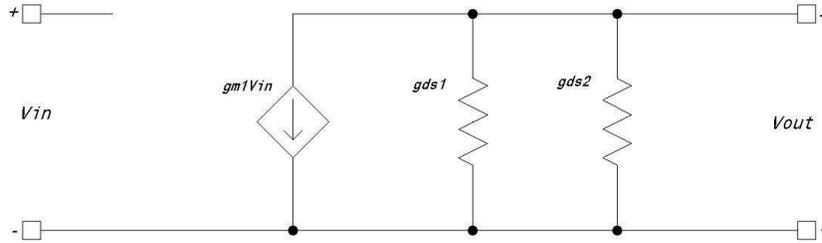

Figure 4.11: Output OTAs small signal model

$$0 = g_{m7}V_{in} + (g_{ds7} + g_{ds8})V_{out} \tag{4.13}$$

Solving for V_{out}/V_{in} the voltage gain is obtained as follows:

$$A_{v_2} = \frac{-g_{m7}}{g_{ds7} + g_{ds8}} \tag{4.14}$$

The whole amplifier gain is:

$$A_{v_{out}} = A_{v_1} \times A_{v_2} \tag{4.15}$$

The transistors' size of the output stage are shown in table 4.2.

Table 4.2: OTA's output stage transistors' dimensions.

Device	W (μm)	L (μm)
$M7_{a,b}$	597	0.35
$M8_{a,b}$	5	0.35

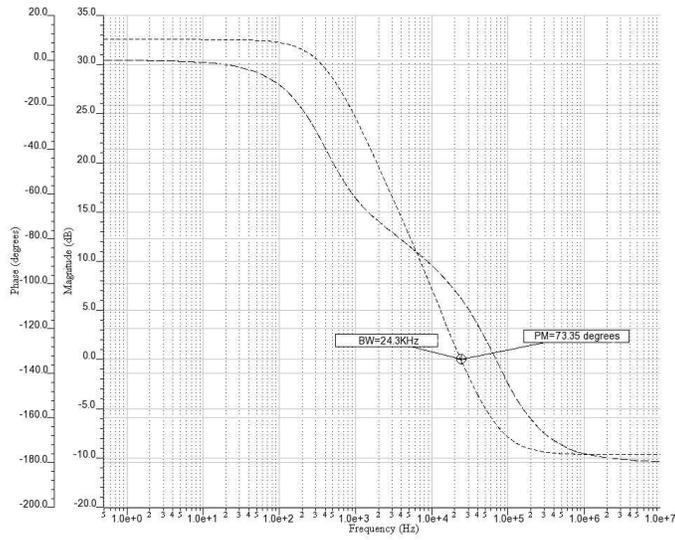The simulation shows a gain of $32.5dB$ with a BW of $24.34KHz$ and a PM of 73° (figure 4.12).

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Figure 4.12: Output stage open loop gain.

Figure 4.13 shows the voltage output swing of the output stage, where a $400mV$ output voltage swing is observed.
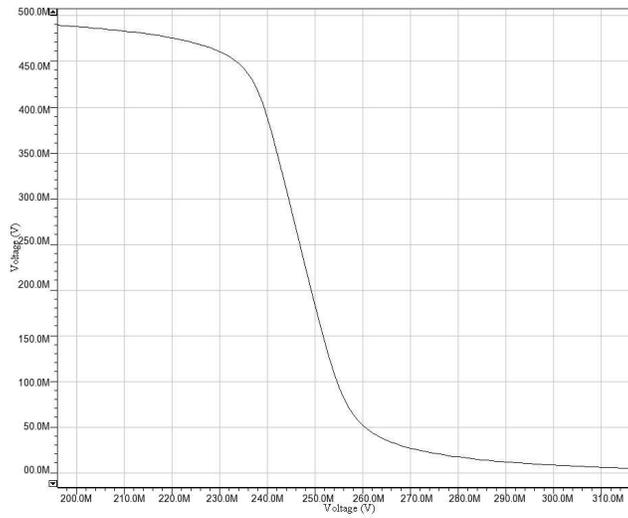

Figure 4.13: Ouput stage output voltage swing.

The layout of the output amplifier stage is shown in figure 4.14 whose dimensions are $94\mu m \times 113\mu m$.
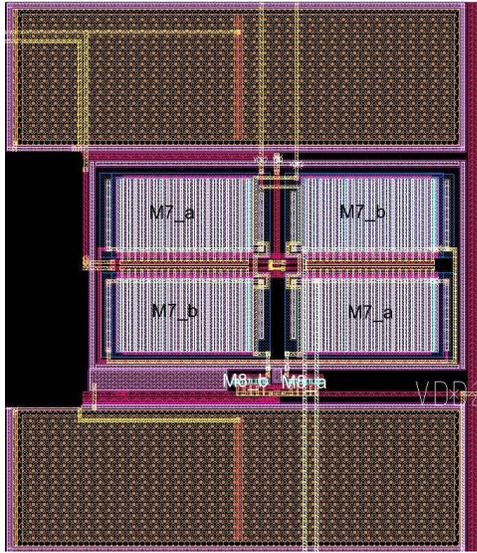
Figure 4.14: Output stage OTA's layout.

4.1.3 Biasing Circuits

Biasing circuits are developed in order to set the DC operational point of both amplifiers. For the first amplifier stage, three circuits are developed. Amplifier's biases VL and $Vptat$ keep a constat gain over process-temperature variations. Through terminals V_{OCMP} and V_{OCMN}, V_{OCMP2} and V_{OCMN2}, V_{ocm} is set. Figure 4.15 shows all the building blocks of the amplifier, including the biasing stages. The circuits for VL and $VOCM$ are based on reference [43].
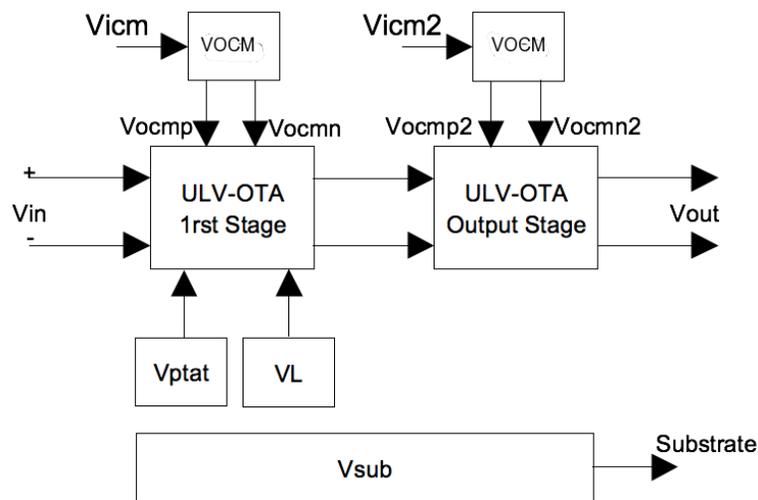

Figure 4.15: Biases diagram.

Vptat **biasing**

The *Vptat* bias circuit generates a voltage that is proportional to the absolute temperature. The generated voltage feeds the first stage OTA's current source. The circuit is based in the well known PTAT bipolar circuit reported in [59].

To compare the behaviour of the CMOS in weak inversion (equation 3.15) and the bipolar transistor, we use the Ebers-Moll model as follows:

$$I_C = I_S(e^{V_{BE}/U_T} - e^{V_{BC}/U_T}) \tag{4.16}$$

The comparison shows that the CMOS operating in weak inversion is equivalent to the bipolar transistor. Then as described in [60], bipolar transistor can be substituted by CMOS transistor working in subthreshold regim (see figure 4.16).
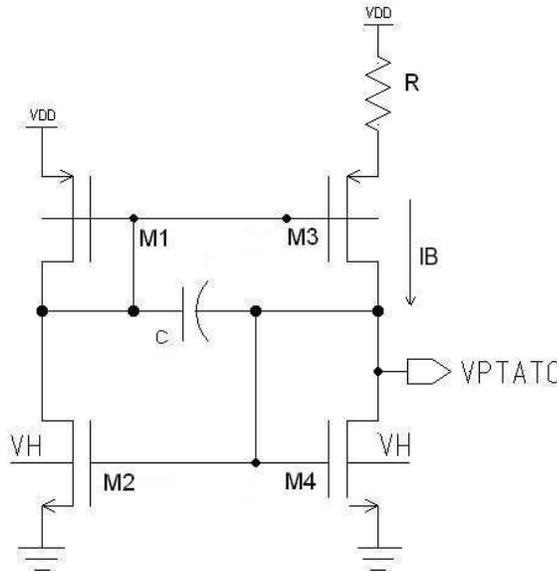

Figure 4.16: PTAT circuit.

The circuit has been built by two current mirrors $M_1 - M_3$ and $M_2 - M_4$. The current through M_1 is the same than the current of M_2 and I_B is the same current flowing through M_3 and M_4. Therefore:

$$I_B = \frac{S_4}{S_2} I_2 \tag{4.17}$$

and

$$V_{GS1} = V_{GS3} + I_B R \tag{4.18}$$

substituting I_B and I_2 by its characteristic equation:

$$I_S S_3 e^{(V_{GS3}-Vth)/U_T} = S_4/S_2 e^{(V_{GS3}-Vth+I_B R)/U_T} \tag{4.19}$$

solving for I_B,

$$I_B = n \frac{KT}{qR} ln(\frac{S_2}{S_4} \frac{S_3}{S_1}) \tag{4.20}$$

The I_B current is then reflected to the current source of the amplifier through the gate of M_4.
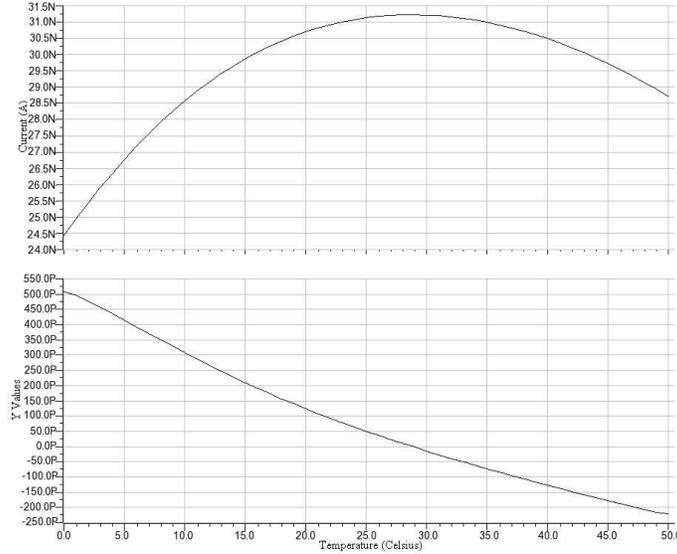

Figure 4.17: IPTAT behaviour.

Figure 4.17 illustrates the I_{PTAT} simulation where, a temperature sweep shows the variation of the I_{ptat} with an average of $dIref/dT = 85pA/^oC$. This simulation results on a fractional temperature coeficient (TFc) of $2741ppm/^oC$.

The figure 4.18 shows the Vptat's layout which measures $45\mu m \times 76.6\mu m$.
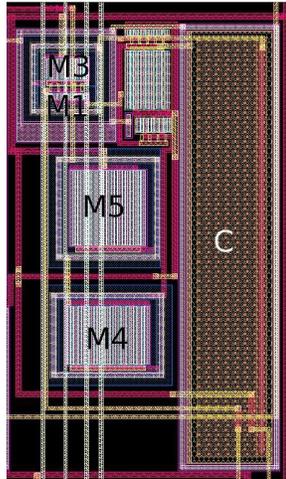
Figure 4.18: Vptat layout.

VL biasing

The VL biasing circuit (figure 4.23) provides a constant current over process-temperatures variations.
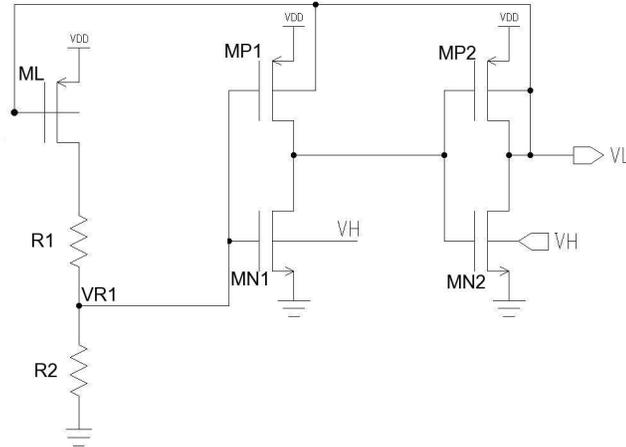
Figure 4.19: VL bias circuit.

This biasing circuit is build by a replica of the IL source (transistors M_4), and two inverters. Transistor ML is the replica of transistor M_4 from the first OTA stage circuit. The current generated by ML creates a voltage in the node V_{R1} of $150mV$. The voltage needed in the gate-bulk is also 150mV. The threshold voltage of the inverters are set to $150mV$.

The circuit dynamically adapts the voltage level trough the bulks of the PMOS in-

verters and the gate-bulk of the current source. If a variation in temperature or process produces a decrease in the IL current, the V_{R1} decrease as well, producing a decrease at the ouput of the second inverter (VL). This voltage produces a higher current in ML devices. When the changes in process or temperature produce an increase in the IL, V_{R1} increases and VL increases, reducing the current IL.
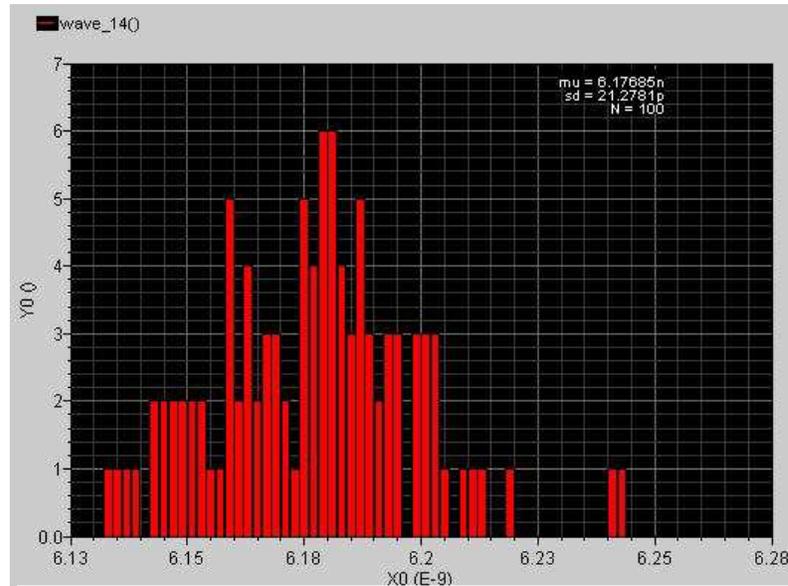
Figure 4.20: IL histogram for a process variation simulation.

A 100 run Monte Carlo (MC) simulation of process was performed in order to obtain the variability of the I_L against the process variations. Using typical CMOS models a I_L of $6.17nA$ is calculated. In the MC simulation, an average of $6.176nA$ is obtained with a standard deviation of $21.26pA$. The results are shown in figure 4.20.

The dimensions of the VL bias circuit are $102.5\mu m \times 34.5\mu m$. The layout is shown in figure 4.21.

Figure 4.21: VL bias layout

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$VOCM$ **biasing**

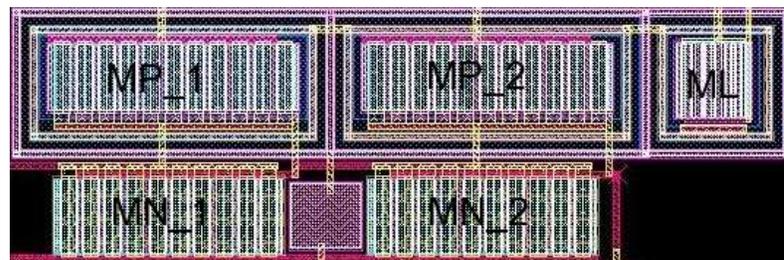The $VOCM$ biasing circuits (figure 4.22) sets the outputs common mode voltage (V_{ocm}) to the Amplifiers FC and CSA. The desired value of V_{ocm} is 250mV ($VDD/2$).

Replica of both, amplifiers and two inverters, are used in the figure 4.22. The switching voltage of the inverters is 250mV. If V_{ocm} is lower than $VDD/2$ then the output $VOCM$ (250mV typically) will be lower than $250mV$, reducing the PMOS V_{th} of the input devices; and the current in the same devices increases, increasing the V_{ocm}.

A capacitor C_1 is used to stabilize the circuit. The input DC voltage in the replica amplifier is set to ground.
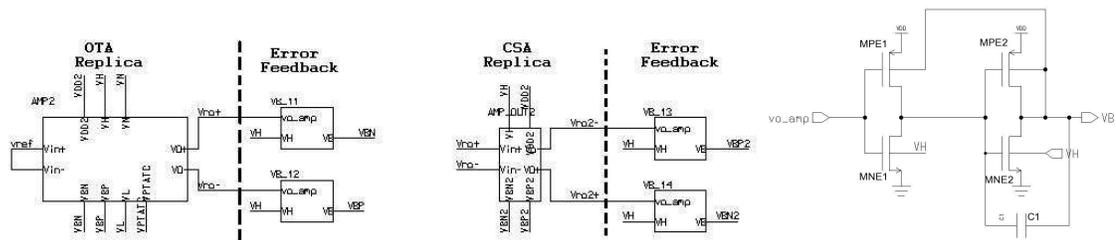

Figure 4.22: VOCM biasing circuits. Left: Circuit for setting the $V_{o,cm}$. Right: Error Feedback circuit.
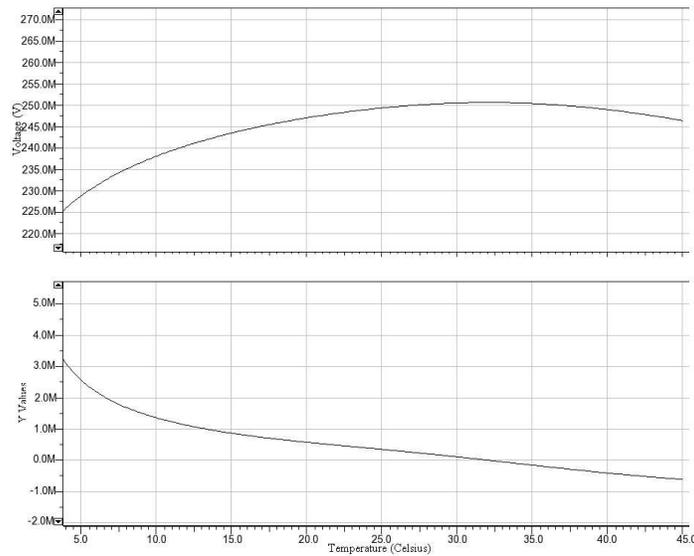

Figure 4.23: V_{ocm} variation against process variation.

The figure 4.23 shows the V_{ocm} simulation where a temperature sweep from 0 to

45^oC illustrates an average of $dVref/dT = 43\mu V/^oC$ providing a Fractional Temperature coefficient, FTc, of $1736ppm/^oC$.
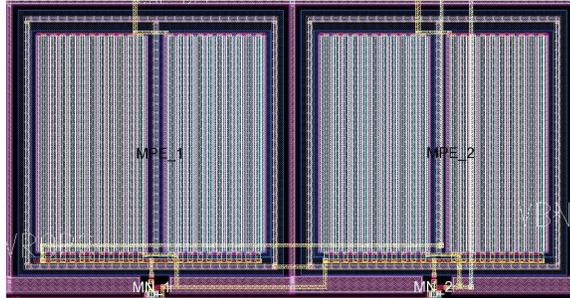
Figure 4.24: Error amplifier layout.

Figure 4.24 shows the error amplifier layout which has dimensions of $118\mu m$ by $60\mu m$.

$Vsub$ biasing

In order to reduce the V_{th} of the NMOS devices, a substrate voltage of $250mV$ is needed. The $Vsub$ biasing circuit (figure 4.25) dinamically adapts the substrate voltage trough process-temperature variations.
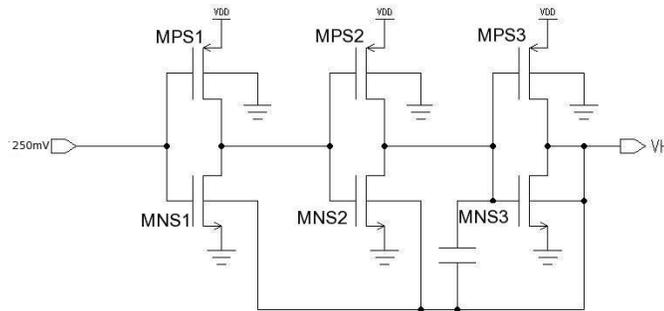
Figure 4.25: Substrate bias circuit.

This circuit is formed by three identical inverters whose switching voltage is set to $250mV$. If a variation in the process and/or temperature cause an increase in the V_{th} of the NMOS devices, the switching voltage of the inverters decreases causing an increase in the output of the first inverter and $Vsub$ increases. As $Vsub$ feeds the bulks of all the NMOS devices, the V_{th} of those devices will decrease.

The stability of this circuit is controlled by the capacitor.

Figure 4.26 shows the layout of the $Vsub$ circuit whose dimensions are $205\mu m$ by $77\mu m$.

Figure 4.26: Vsub layout.

Ultra-Low-Voltage amplifier performance

A simulation of whole OTA amplifier including its biasing circuits was performed using Spectre of Cadence® software.
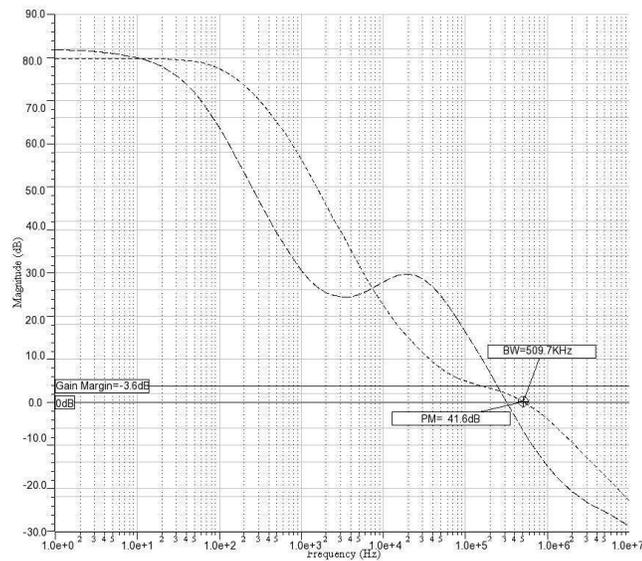

Figure 4.27: Ultra-Low-Voltage amplifier open loop gain.

The simulation shows a differential nominal gain of $80dB$ with a BW of $510KHz$ and a PM of 41.6^o. Figure 4.27 shows the frequency response simulation in magnitude and phase from $1Hz$ to $100MHz$. Moreover, a CMRR of $44dB$ with an input referred

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noise of $240nV/\sqrt{Hz}$ was obtained for the device.
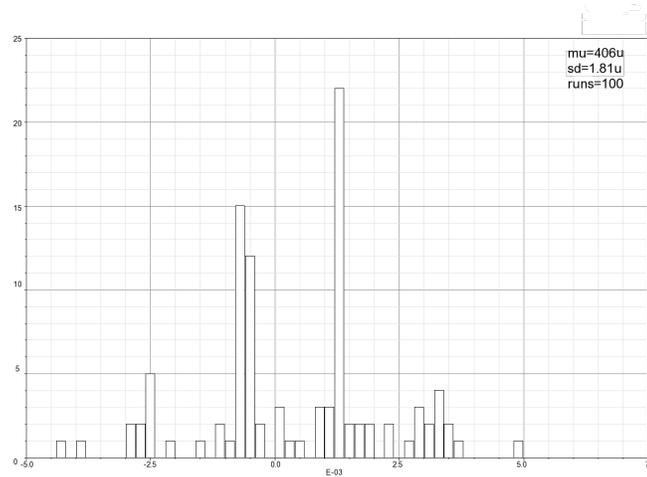
Figure 4.28: Ultra-Low-Voltage amplifier offset.

The figure 4.28 illustrates an histogram that describes the ULV-OTA's offset voltage, in which the value obtained was $406\mu V$. Moreover, the simulated power dissipation was only $1.9\mu W$.

The simulation results are summarized in table 4.3.

Table 4.3: OTA performance summary.

Parameters	
Open loop gain	$80dB$
Bandwidth	$510KHz$
Phase Margin	41.6^o
Input Offset Voltage	$406\mu V$
CMRR	$44dB@10Hz$
	$36.8dB@100Hz$
Input Referred Noise	$240nV/\sqrt{Hz}$
Power Dissipation	
only OTA-core	$1.9\mu W$
OTA+biases	$4\mu W$

The simulations results clearly shows that the proposed OTA has an excellent performance and achieves the requirements of low power consumption while having a high gain in the band of interest being appropriate for its usage in portable EEG devices.

The ULV-OTAs layout is shown in figure 4.29, were each stage of the amplifer has been framed. The total dimensions of the OTA device including its biasing circuits are $260\mu m$ by $480\mu m$.
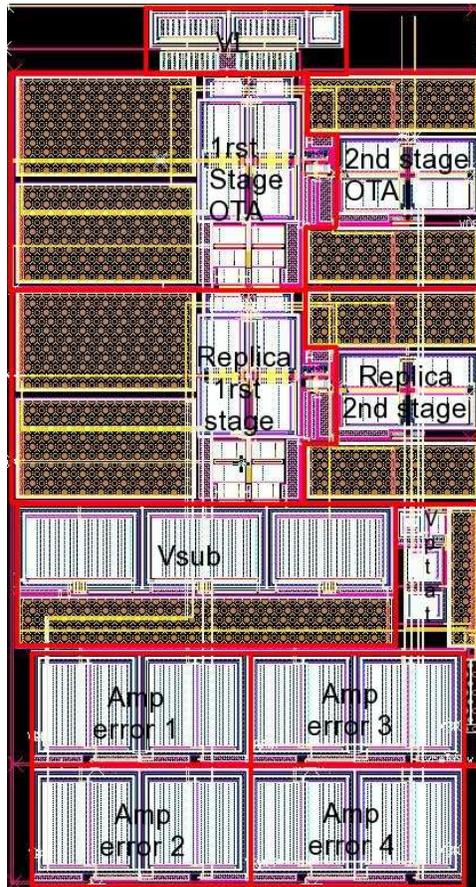
Figure 4.29: ULV-OTA layout

4.2   Low-voltage low-power CT $\Sigma\Delta$ ADC

The CT $\Sigma\Delta$ ADC combines an excellent balance between performance, size and ultra-low voltage applications. Also, while reducing amplifier parameters such as settling time and bandwidth does not degrade the AC performance.

By decreasing the supply voltage, the amplifier's bandwidth is reduced. That makes the use of CT $\Sigma\Delta$ ADC suitable in ultra-low-voltage applications.

4.2.1   Ideal Model

Starting from the desired 16-*bit* of resolution, the CT $\Sigma\Delta$ ADC was designed. The SNR is computed as follows:

$$DR^2 = 3(2^{2B-1}) \tag{4.21}$$

$$DR^2 = 3(2^{2*16-1}) \tag{4.22}$$

Hence $DRdB$ is equal to 98.09dB. For computing the OSR for first, second and third order devices, a small Matlab script was developed using the following equation:

$$M = (\frac{2}{3}\frac{DR^2\pi^{2L}}{2L+1})^{\frac{1}{2L+1}} \tag{4.23}$$

where M represents the estimation of the OSR for each case.

Table 4.4 shows the results of the equation 4.23 for a first, second and third order.

Table 4.4: OSR for first to third modulator's order.

Modulator's order	OSR
1rst	2417
2nd	150
3rd	48

For a first order modulator an OSR of 2417 is needed, given a relatively high samplig frequency for the $0.35\mu m$ CMOS ultra-low-voltage system. For the second and third order devices, better sampling frequencies are required. Although for the third order modulator, the lowest sampling frequency is needed, this frequency implies the uses of higher value of resistances and capacitances, generating more thermal noise (see section **3.2.1**) and taking up more area. For that reason, a second order modulator was choosen for the AFE. Table 4.5 illustrates the values of resistances and the occupied area (if implemented in a high resistance poly) . These values assume capacitances, C_1 and C_2, of $60pF$ and $50pF$ respectively.

A CT second order $\Sigma\Delta$ modulator ideal model (figure 4.30) was designed and simulated using the Matlab toolbox [62] in order to calculate its coeficients. Using the

Table 4.5: Resistors values for second and third modulator's order.

Order	R_1	R_{D1}	R_2	R_{D2}
2nd	5 $M\Omega$	2.5 $M\Omega$	665.4$K\Omega$	865.43$K\Omega$
	15,000μm^2	7,500μm^2	1,996μm^2	2,596μm^2
3rd	15.64 $M\Omega$	7.78 $M\Omega$	2.08$M\Omega$	9.34$M\Omega$
	46,920μm^2	23,334μm^2	6,240μm^2	28,020μm^2

second order model in the Z-domain the modulator coefficients a={0.223, 0.77, 0.074} and c={0.111,1.001} were obtained such that the Modulator transfer function becomes:.
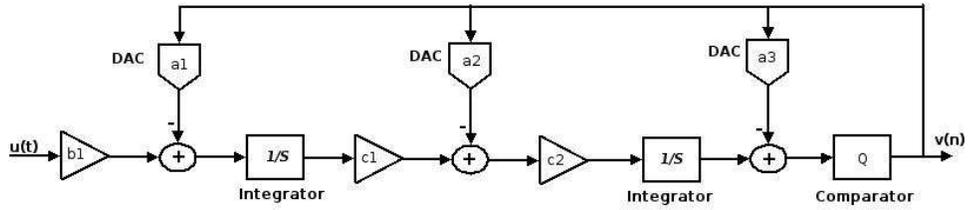
Figure 4.30: Modulator's ideal model.

$$\frac{z^2 - 2z + 1}{z^2 - 1.225z + 0.4415} \tag{4.24}$$

The modulator was simulated using a 15% delay. The obtained bitstream and its respective power spectral density is shown in figure 4.31. A SNR peak of 95dB and a maximum input stable signal of -1.71dB were estimated, according to figure 4.32.
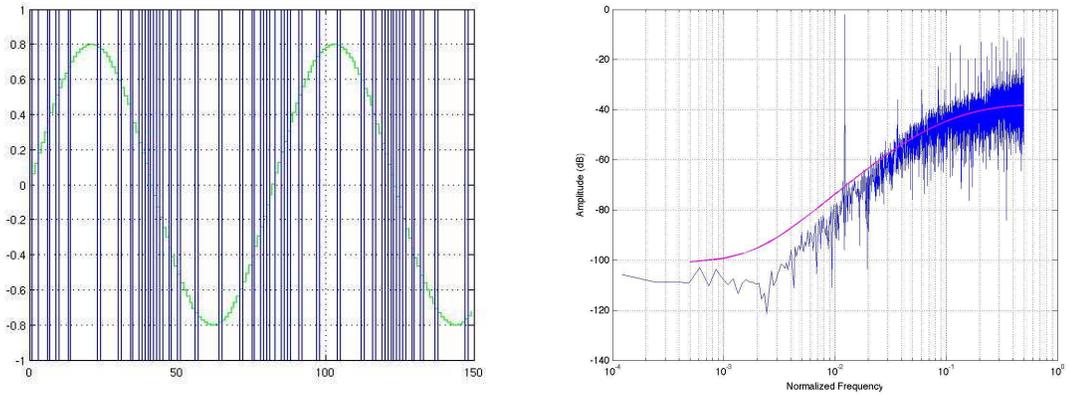
Figure 4.31: Left: Bitstream; Rigth:Bitstream's PSD.
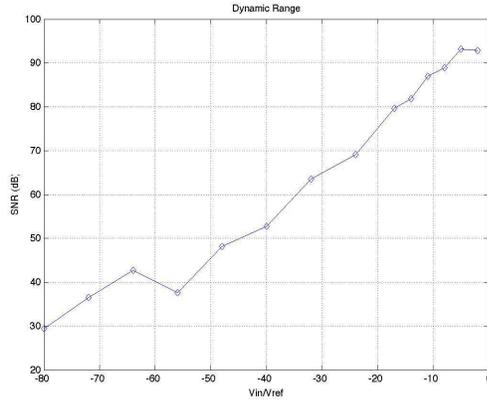
Figure 4.32: Modulator's dynamic range.

4.2.2 Circuit Model

The Modulator building blocks are shown in figure 4.33. The resistors and capacitors are calculated as:

$$C_i = \frac{1}{a_i R_i f_s} \qquad (4.25)$$
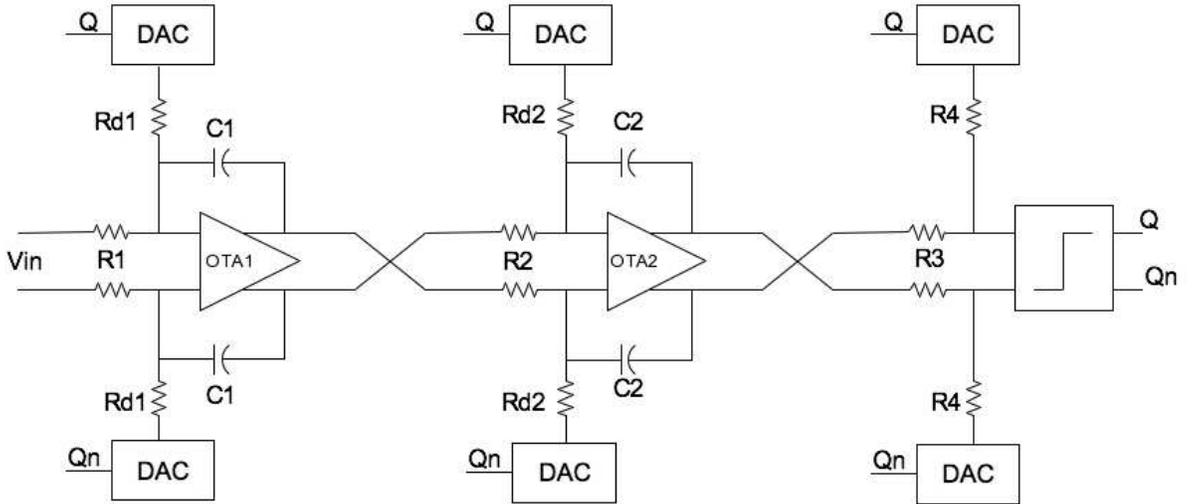
Figure 4.33: CT $\Sigma\Delta$ Modulator

The maximum value of the resistance is determinated by the maximum thermal noise allowed. As the DAC used is a RZ DAC the equation that models the noise is:

$$V_{neq,RTZ}^2 = V_{ni}^2 + V_{nDAC}^2 \left(\frac{R_i}{R_{DAC}}\right)^2 + V_{n,OTA}^2 \left(\frac{R_i}{R_i||R_{DAC}}\right)^2 \qquad (4.26)$$

The values of capacitances and resistances for the modulator are shown in table 4.5

Amplifier

A current source Amplifier based OTA has been choosen for the ADC' integrator (figure 4.34) in order to have greater output swing and wider BW than the FC based OTA. For maximal output swing a V_{ocm} of VDD/2 is selected. This topology has not inherent CM operation, therefore, a CM network is added. The amplifier is designed to work at $0.5V$ supply voltage.
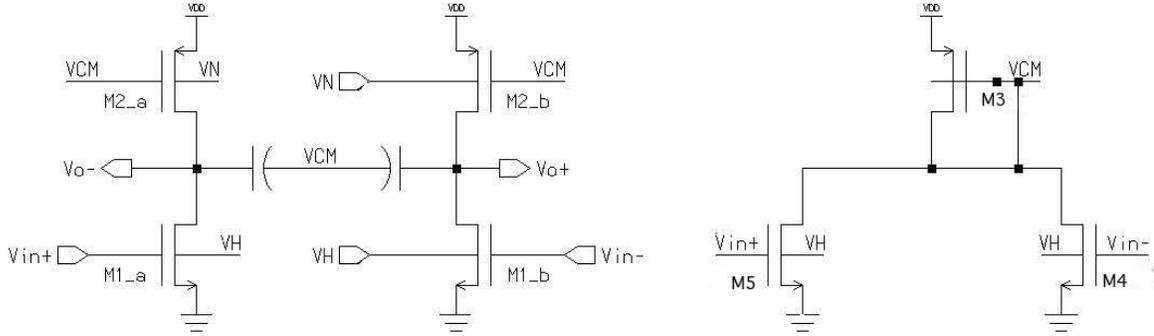

Figure 4.34: Current source amplifier based OTA for a $\Sigma\Delta$ ADC.

A pseudo-differential pair NMOS (transistors M_{1a} and M_{1b}) is used as input devices. The V_{icm} in these devices is set to VDD/2 in order to keep them on, and the nominal value of the bulk, VDD/2, reduces the threshold voltage and increases the level of inversion. Transistors M2 are active loads (current sources) whose bulks allows to control V_{ocm} and thus V_{th} reduces to a nominal value of $100mV$. Transistors M3, M4 and capacitors C_{cm} form a feedforward network that performs a common mode operation.

Figure 4.35 shows the small signal model where the open loop gain equation is calculated as:

$$0 = g_{m1}V_{in} + (g_{ds1} + g_{ds2})V_{out} \qquad (4.27)$$

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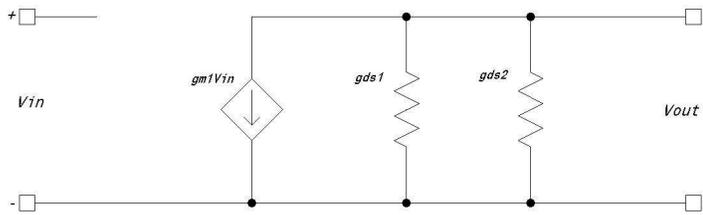
Figure 4.35: Output OTAs small signal model

Solving for V_{out}/V_{in}:

$$A_v = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} \tag{4.28}$$

The transistors dimensions of the OTA used for the simulation are shown in table 4.6.

Table 4.6: Transistor dimensions of the OTA

Device	W (μm)	L (μm)
$M1_{a,b}$	693	0.35
$M2_{a,b}$	698	0.35
$M3$	789.9	0.35
$M4_{a,b}$	482	0.35
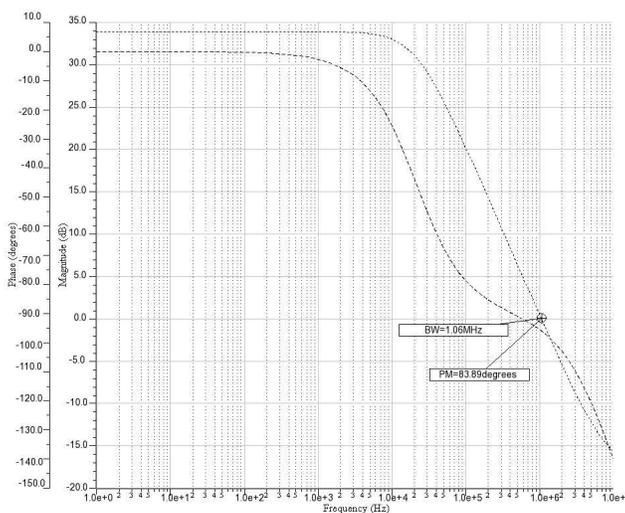
Figure 4.36: ADCs amplifier open loop gain.

Figure 4.36 illustrates the bode plots representing the OTA frequency response in open loop for magnitude and phase. The differential open loop gain of the OTA is $34dB$ with a BW of $1.063MHz$ and PM of 83°. Moreover, figure 4.37 shows the CMRR plot for the amplifier which displays $72dB$ from $1Hz$ to $2MHz$.
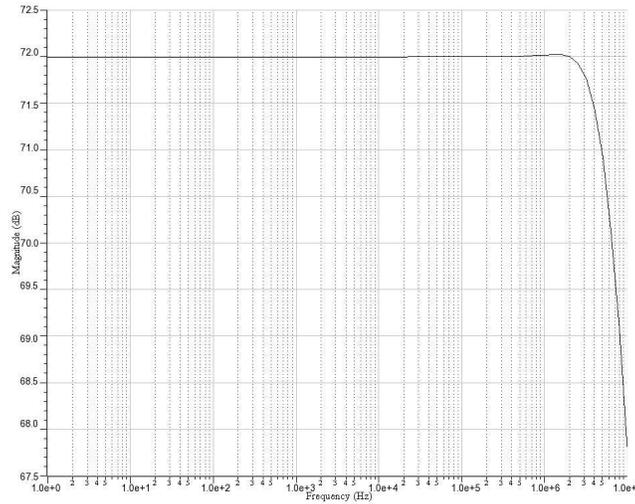
Figure 4.37: ADCs amplifier common mode rejection ratio.
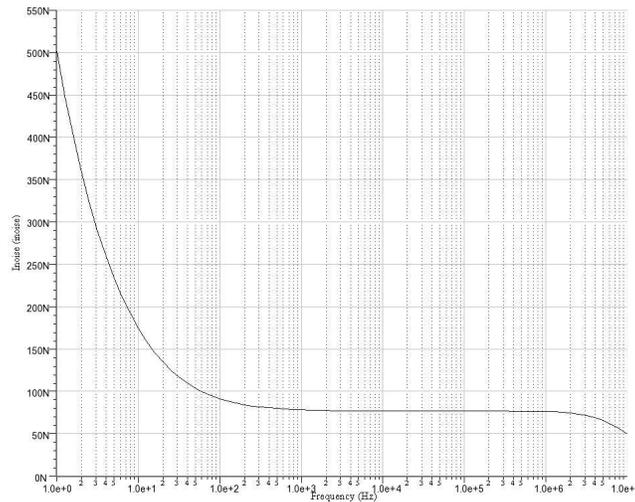
Figure 4.38: ADCs amplifier input referred noise.

The noise and offset performance are shown in figures 4.38 and 4.39, respectively. The amplifier has an input referred noise of $90nV/\sqrt{Hz}$ and an offset of $1mV$.
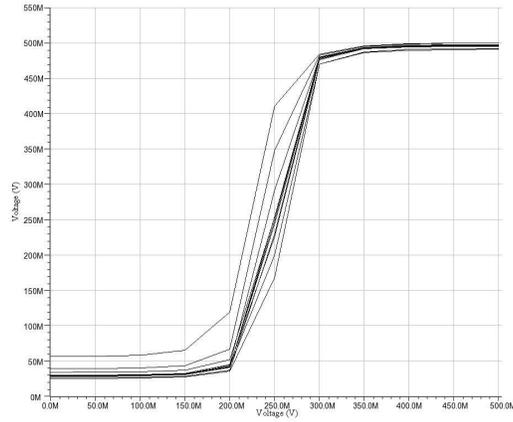
Figure 4.39: ADCs amplifier offset.

Finally, figure 4.40 shows the amplifier's layout, whose dimensions are $130\mu m$ by $89.5\mu m$.
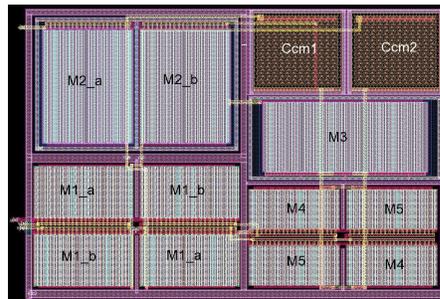
Figure 4.40: Amplifier's layout

The Modulator's OTA device performance is summarized in table 4.7.

Table 4.7: Summarized results of the Modulator's OTA.

Parameter	Value
Gain	$34dB$
BW	$1.06MHz$
PM	83°
CMRR	$72dB$
Offset	$1mV$

Comparator

A single bit quantizer latch-based was implemented for the ADC design, as shown in figure 4.41. The quantizator consists of a sampling stage, a comparation stage and a latch stage.

When the clock is low, the signal is sampled by the switches M_{s1} and M_{s2}, made by NMOS transistors; then the signal is compared by the latch type comparator. PMOS transistors of comparator are tied to ground in order to reduce the transistors threshold voltage.

The output of the comparator is valid when the clock is high. Moreover, the signal is latched by the D type Flip-Flop during all the clock period.
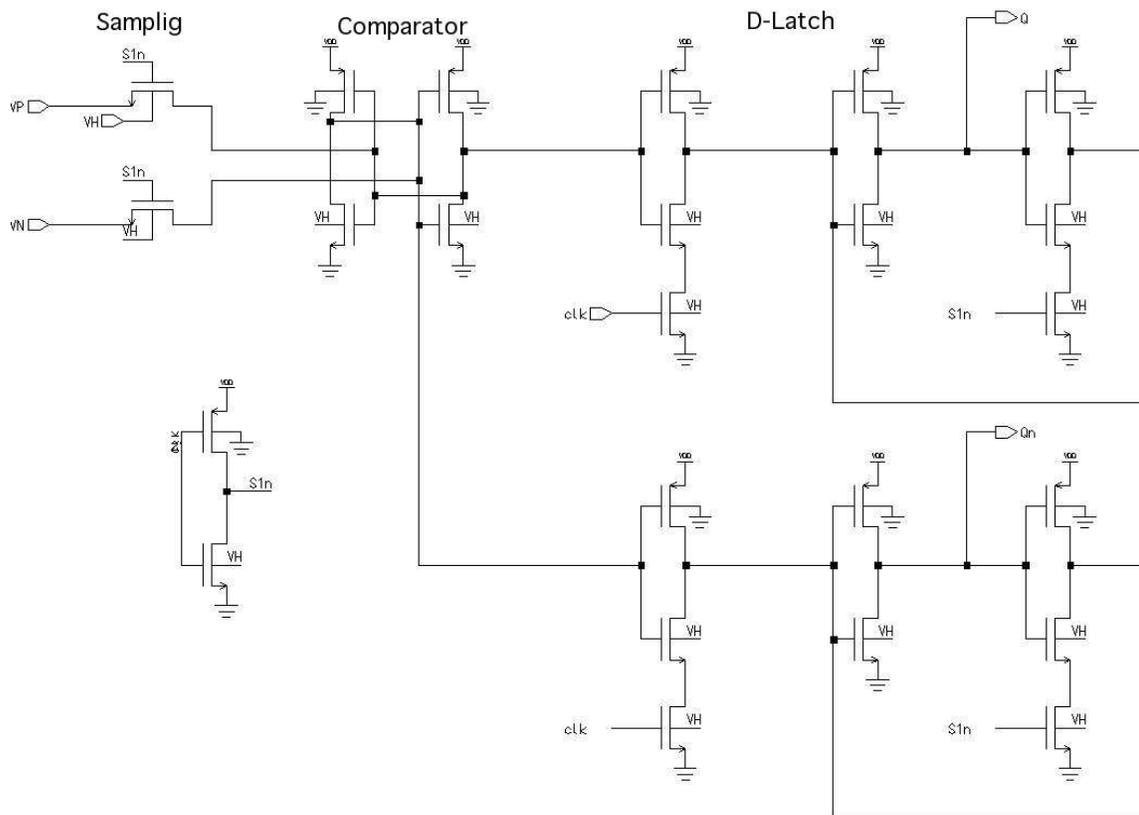
Figure 4.41: Single bit quantizer

Figure 4.42 shows the comparator's layout whose dimensions are 34 μm by 98μm.
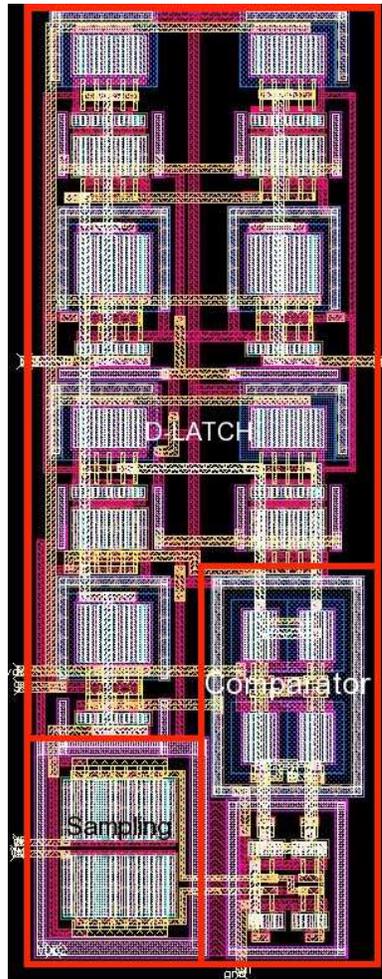
Figure 4.42: RZ DAC's layout.

Return to Zero Digital to Analog Converter

As mentioned earlier, the RZ DAC avoids the intersymbol interference, therefore, reducing the distortion. The RZ DAC is made by a series of switches (figure 4.43) where NMOS transistors are used to transfer VDD/2 and ground; while PMOS are used to transfer VDD.

When the clock is low, the RZ DAC is active. At the active phase of the DAC two values, 0V and 0.5V, will be dependent of the Quatizators output.

At the inactive RZ DAC phase, i.e. when the clock is high, a constant value of VDD/2 appers at its output.

Figure 4.44 shows the layout of the comparator whose dimensions are $32\mu m$ by
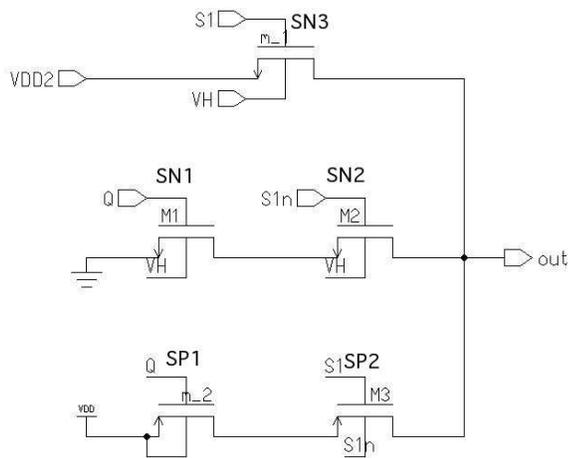
Figure 4.43: Return to zero DAC

$28.5\mu m$.
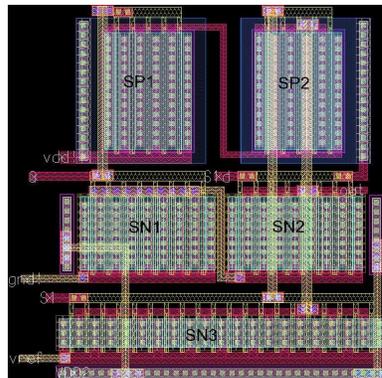
Figure 4.44: RZ DAC's layout.

Decimator

The bitsream needs to be applied to a low pass filter in order to reduce the quantization noise and return the modulated signal to the band base . This stage is called decimator.

Here the bitstream is applied to a low pass FIR of 64 coeficients. The representation diagram is shown in figure 4.45. The biststream is first loaded into a shift register of 64bits. When the register is full, each loaded bit is multiplied by a coefficient of the FIR and all the resulted data is added. The desired output appers at $Y(n)$.
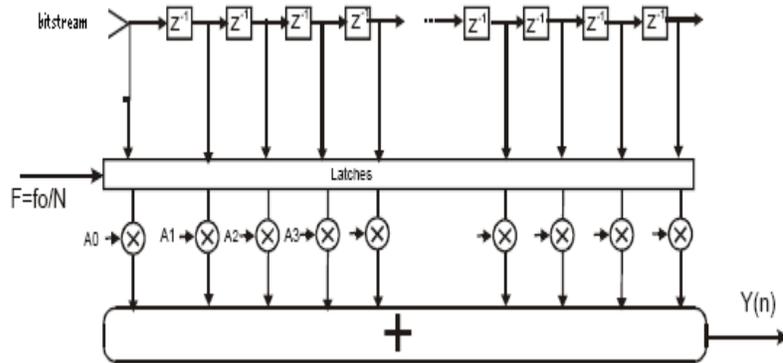
Figure 4.45: FIR diagram.

In order to avoid the multiplication stage, an alternative solution is adopted. Thanks to the nature of the bitstream is easy to simplify this stage, by chossing a positive coefficient or negative coefficient if the value of the bit loaded is 1 or 0 respetively. Figure 4.46 illustrates this solution.
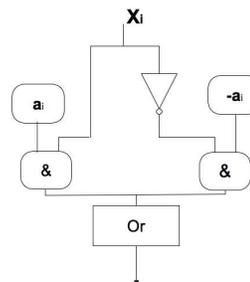
Figure 4.46: Multiplication diagram model.

The FIR was programmed in VHDL and later synthetized in Cadence. Figure 4.47 shows the resulted diagram where the first bistream is latched in a shift register, then, the frequency is reduced by a factor of 64 and finally the coefficients are selected and added.
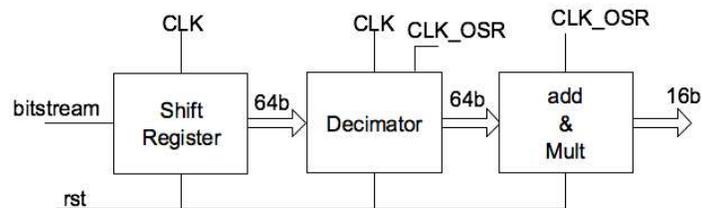
Figure 4.47: FIR based decimator architecture.

4.2.3 ADC performance

For simulating the ADC, a sinusoidal signal of 100Hz of $190mV_{pp}$ has been applied to the input of the ADC giving an SNR of $92dB$. The figure 4.48 shows the obtained bitsream PSD from the simulation.
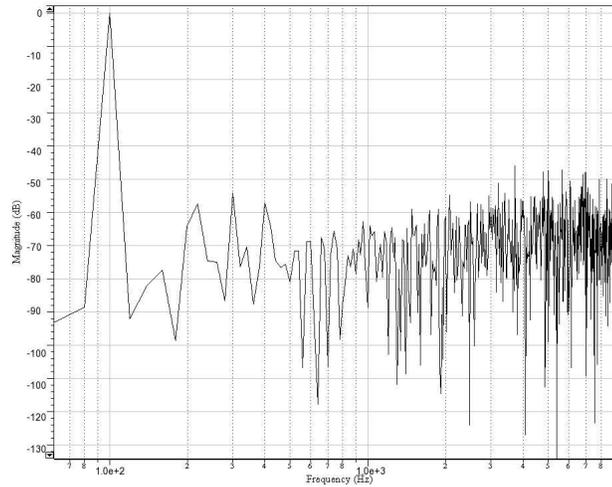
Figure 4.48: ADCs noise shape.

Figure 4.49 shows the layout of the CT-$\Sigma\Delta$ modulator whose dimensions without taking into account the capacitors are $480\mu m$ by $410\mu m$.
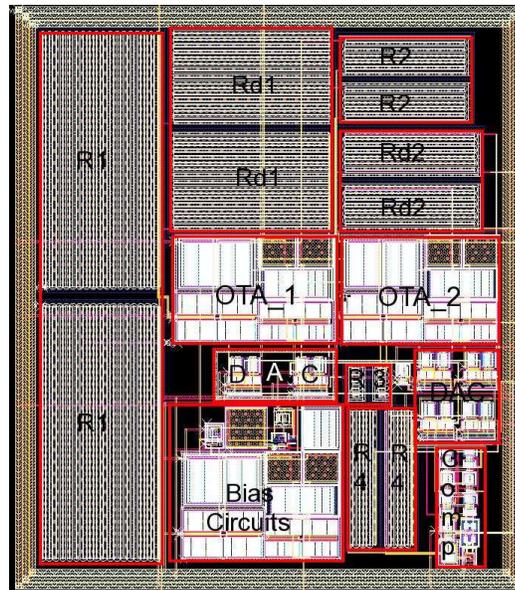
Figure 4.49: CT $\Sigma\Delta$ Modulator.

The table 4.8 summarize the results of the $CT\text{-}\Sigma\Delta$ modulator.

Table 4.8: Modulator performance summary.

Parameter	Value
SNR	$95dB$
ENOB	$15.48bits$
Max input peak	$-1.71dB$
Power dissipation	$7\mu W$

The simulations results show that the Modulator has an excellent performance achieving $15.5bits$ while it dissipates only $7\mu W$, being an excellent candidate to be implemented in portable EEG devices.

4.3   Conclusions

In this chapter a novel amplifier's topology able to work at supply voltage of 0.5V was presented. The simulations shown that the proposed amplifier is very suitable to be implemented in biomedical applications, because of its high gain and low power dissipation.

Moreover, this chapter also presented the proposed CT-$\Sigma\Delta$ Modulator, that works at supply voltage of 0.5V. The modulator achieves in simulation a resolution of $16bits$ while dissipating only $7\mu W$, which is excellent for biomedical micropower tasks.

The $0.35\mu m$ AMS CMOS technology was used to develop the AFE circuit; this technology was made to operate with a maximum of 3.3V supply voltage. Nevertheless, a circuit capable to operate with a supply voltage of 0.5V was developed.

The proposed FIR operates with a supply voltage of 1V; however, by replacing the cells that AMS provides by full custom cells, with special polarization in the substrate, the FIR will be able to operate with a polarization voltage of 0.5V.

Then, based on the excellent performance of the AFE shown by the simulation, the ASIC was fabricated. Figure 4.50 shows a photo of the AFE's ASIC. The FIR filter occupies the half of the space, while the ULV-OTA and the Modultor occupies the other half. The total dimensions of the AFE are $852\mu m$ by $1542\mu m$.
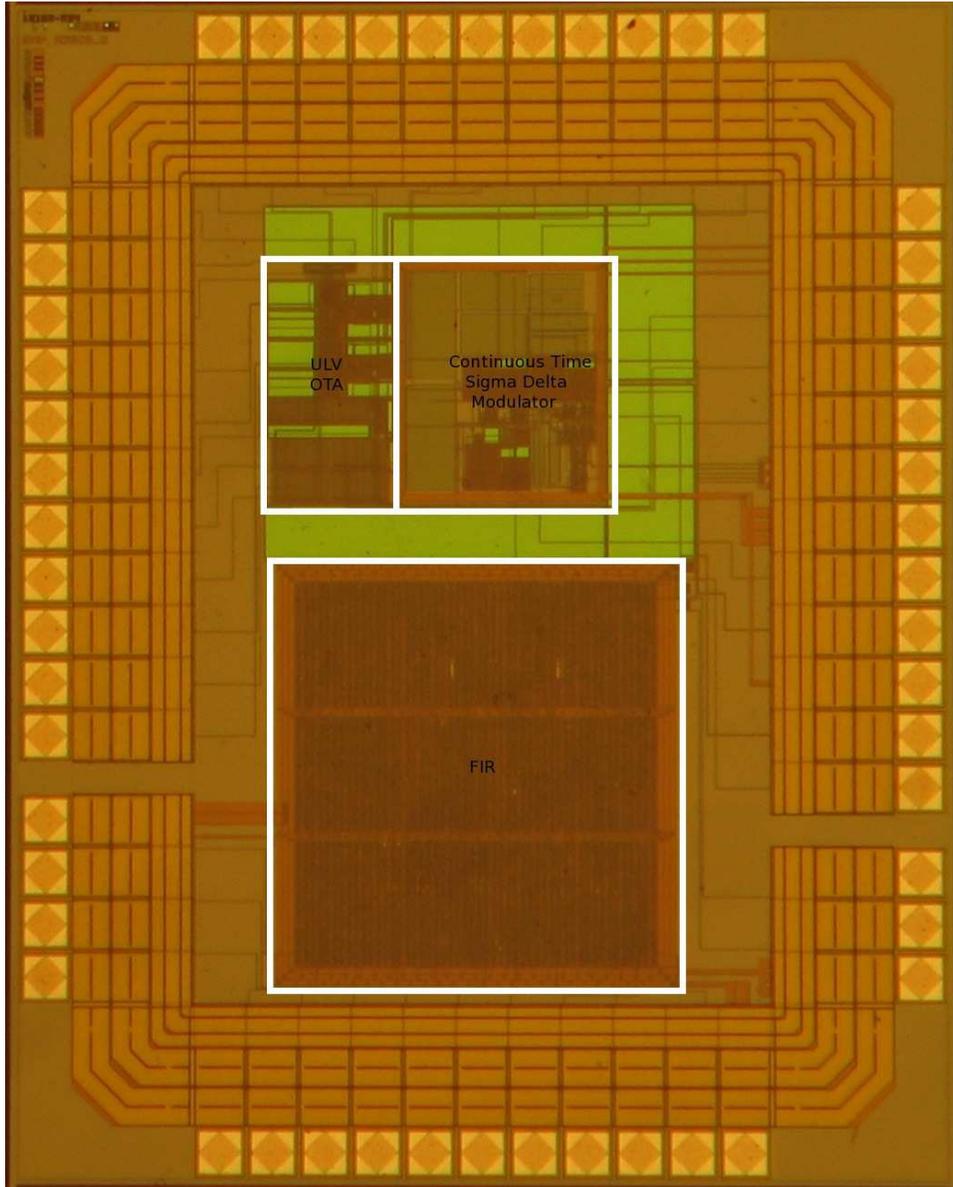
Figure 4.50: AFE's ASIC

Chapter 5

Analog Front End Test

Ce chapitre détaille le procédé de mesure et la carte de test développée pour les test des circuits prototypes. Plusieurs mesures peuvent être faites sur l'ASIC, test de l'ULV-OTA, du modulateur de $\Sigma\Delta$ avec ou sans le filtre FIR. La section 5,1 présente la fonction globale de la carte de test, et l'explication de chaque module. Dans la section 5,2 la configuration de la carte de test pour tester l'ULV-OTA est présentée.

La section 5,3 présente la configuration pour le bitstream du modulateur et le meassurement du mot 16 bit.

Dans la section 5,4 présente les résultat de mesure de l'ASIC pour vérifier son fonctionnement. En sous-section 5,4,1 les caractéristiques de gain de boucle ouverte, de largeur de bande, d'offset, de bruit en sortie e de puissance dissipée par l'OTA sont présentés. Le gain global d'ULV-OTA n'a pas été mesuré, puisque le V_{pp} inférieur réalisable du signal d'entrée était $500\mu V$. Avec cette valeur dans le signal d'entrée, la sortie de l'ULV-OTA est saturée. Alors le gain de boucle ouverte a été mesuré dans chaque étage séparément. En sous-section 5,4,2 les résultats de test du CAN sont présentés. Le modulateur a été testé en utilisant un signal du sinus de $50Hz$. Les caractéristiques mesurées sont le rapport signal sur bruit (SNR), le nombre de bits effectifs, signal maximum d'entrée et dissipation de puissance. En plus des tests du modulateur, le modulateur a été testé avec le filtre FIR, obtenant des caractéristiques d'INL, et de DNL identiques aux caratéristiques estimées par simulation. De plus le convertisseur ne présente pas de code manquant. Enfin dans la section 5,5 les conclusions sont données. Deux tableaux sont présentées afin de comparer les résultats obtenus en simulation et en test.

Introduction

This chapter describes the test and the results obtained from the system that was proposed in the previous chapters. Section **5.1** explains the global function of the test card, section **5.2** and **5.3** show the special cases of the test card configuration for the ULV-OTA and the CT-ΣΔ ADC. Finally, section **5.4** presents the ASIC meassurements to verify its performance.

5.1   Test board

The test board was designed to test the ULV-OTA, to perform the test and analysis of the bitstream's CT-ΣΔ Modulator and to test the complete CT-ΣΔ ADC (the modulator plus the decimation filter). The figure 5.1 shows a photograph of the test card board.

Figure 5.1: Test card circuit.

The overall function of the test card is described in the diagram of the figure 5.2. At the time the test card is initialized, a 16 *bits* signal predefined by the user (eg. sinusoidal, white noise, etc.) is charged in the signal generation module. This module consists of a $64K \times 16$ SRAM and a 16 *bits* DAC. Moreover, in this step the test type is selected via two multiplexers. Two 16 *bits* buffers perform the function of the external multiplexer and the second multiplexer is programmed into the FPGA.

Once the test card is configured with the desired test and the signal is loaded, the card sends the signal to the ASIC. Thus, depending on the selected test configuration,

that signal could be the signal from ULV-OTA, the bitstream or the 16 *bits* signal from the ASIC's ADC. The FIFO sends the signal to the computer via the NI PCI 6533 aquisition card, where the signal is displayed and processed by an user interface developed in LabView.
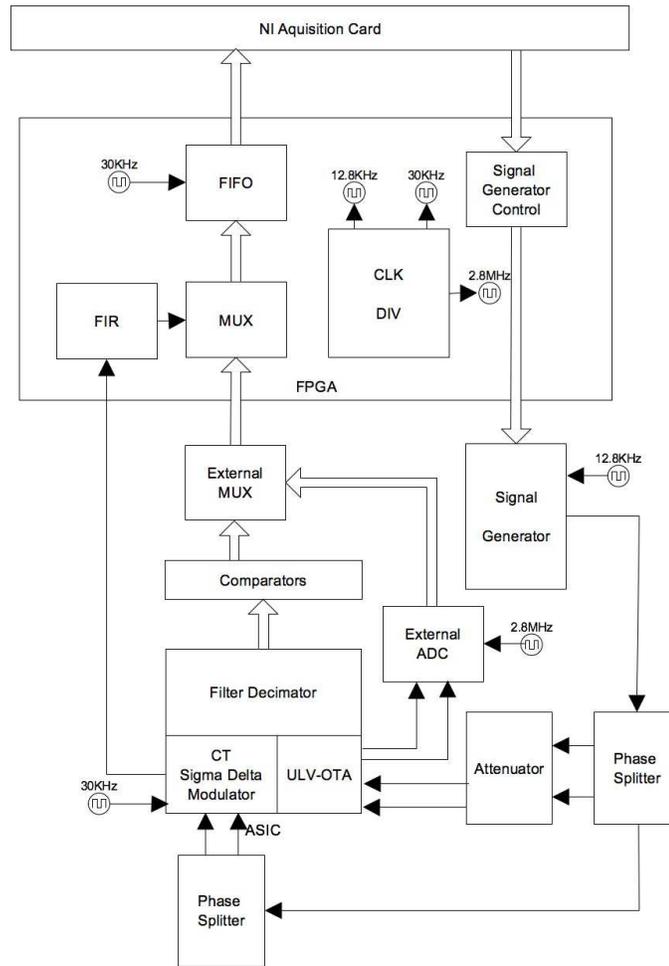
Figure 5.2: Blocks diagram of the test card

5.2 Ultra-low voltage amplifier Test configuration

This test supports both, first and second ULV-OTA stage open loop gains and band widths, output referred noise, and offset meassurements. Additional flexibility is provided through the possibility of changing manually the jumpers, and then modifying the testing functions for the ULV-OTA stages. The figure 5.3 shows the test card's block diagram and information flow configurations for this test.
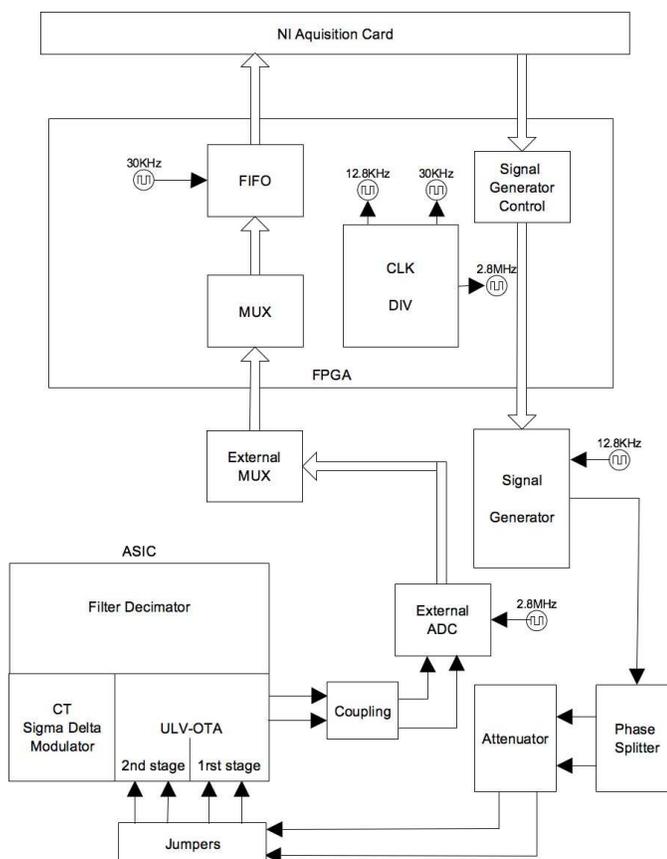
Figure 5.3: ULV-OTA test and information configuration.

When the card is activated, the signal is loaded into the signal generation module and in the case of open loop gain and band width meassurement, a frequency sweep from $50Hz$ to $50KHz$ signal is selected. For the noise meassurement both ULV-OTA inputs are tied to ground.

The signal generator gives a single phase signal, however, the proposed ULV-OTA is a fully differential OTA, which means that positive and negative phases are needed. Therefore, a single differential ouput unity gain op-amp phase splitter is placed after the signal generator. The output of the splitter is then reduced by an array of resistances in order to achieve values of hundreds of μ-volts.

After the ULV-OTA, an analog signal conditioning stage is placed to isolate and couple the ULV-OTA ASIC's output with the external ADC. The 16 *bit* signal is taken by the FIFO, that has a sampling rate of 454KHz, and then it is sent to the PC.

5.3 CT ΣΔ ADC Test

Here two test set up configurations are available: the modulator or the modulator plus the decimation filter. With the modulator test, the bitstream is analyzed, while the modulator plus the filter test gives both, the INL and DNL meassurements.

5.3.1 CT ΣΔ Modulator Test

This test set up allows the analysis of the bitstream and its PSD. The SNR, SINAD and ENOB result from this test analysis.

A sinusoidal signal is loaded in the signal generation module, as a first step in the board test set up configuration. The CT-ΣΔ modulator is feed by the phase splitter stage that has a unitary gain and an output common mode of $0.25V$. The modulator works with a clock of 30 KHz and voltage levels of 0 and $0.5V$.
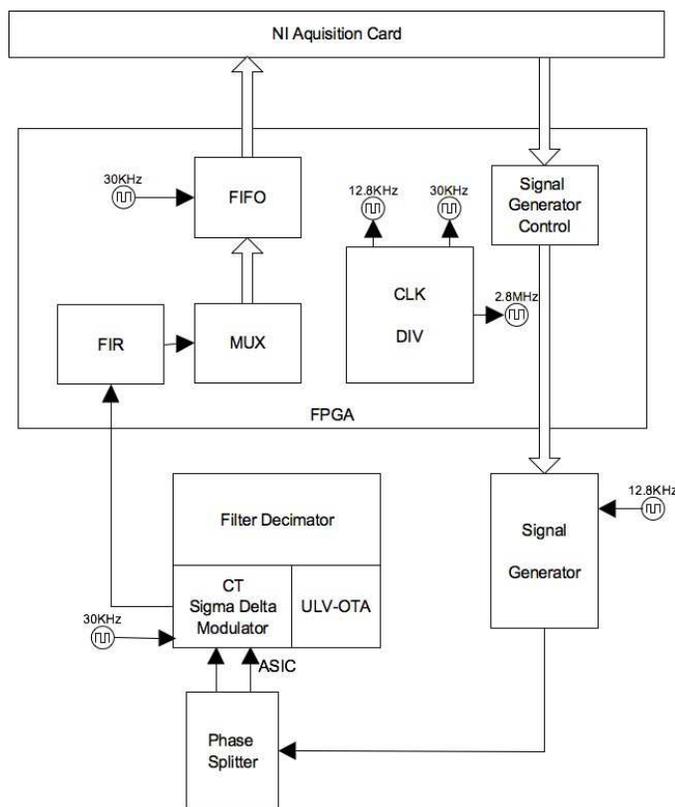
Figure 5.4: Modulator test and information configuration.

The modulator's output bitstream has a low value of $0V$ and a high value of $.5V$.

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Nevertheless, the FPGA recognizes a high value as a $3.3V$. In order to, communicate the ASIC with the FPGA, a simple comparator is placed to pull up the bitstream values.

The FIFO, working at $30KHz$, receives the bitstream and sends it to the PC via the NI card.

The FIR filter could be programmed in the FPGA, such that a programmable filter could be tested. Figure 5.4 illustrates the block and information diagram of this test.

5.3.2   Modulator with Decimation filter Test

In this test the INL, DNL and the Histogram are meassured from the ASIC's ADC (Modulator + FIR) .

As in the other configurations, the signal is first loaded, in this case a sinewave. Then the ADC is fed by the unity gain phase splitter, whose output common mode voltage is $250mV$. In this test set up the ADC works with a clock of $30KHz$.

The ASICs FIR ouput is taken by the FPGA. However, the high value of the FIR is $1V$ and the low value is $0V$ while the FPGA needs a high value input of $3.3V$. For that reason, an array of comparators is placed between the FIR's output and the FPGA input, in order to pull up the high value of the FIR. Finally the signal is received by the FIFO and it is sent to the PC via the NI card.

Figure 5.5 illustrates the block and information diagram for this test set up.

5.4   Test results

The following section presents the results obtained from the test set ups explained previously. First, the ULV-OTA results are presented in subsection **5.4.1** and second, the ADC results are presented in subsection **5.4.2**.

5.4.1   ULV-OTA test results

For testing the open loop gain of both stages, a sweep signal from $50Hz$ to 50 KHz was used. For the first stage, the signal was reduced by an array of resistors to
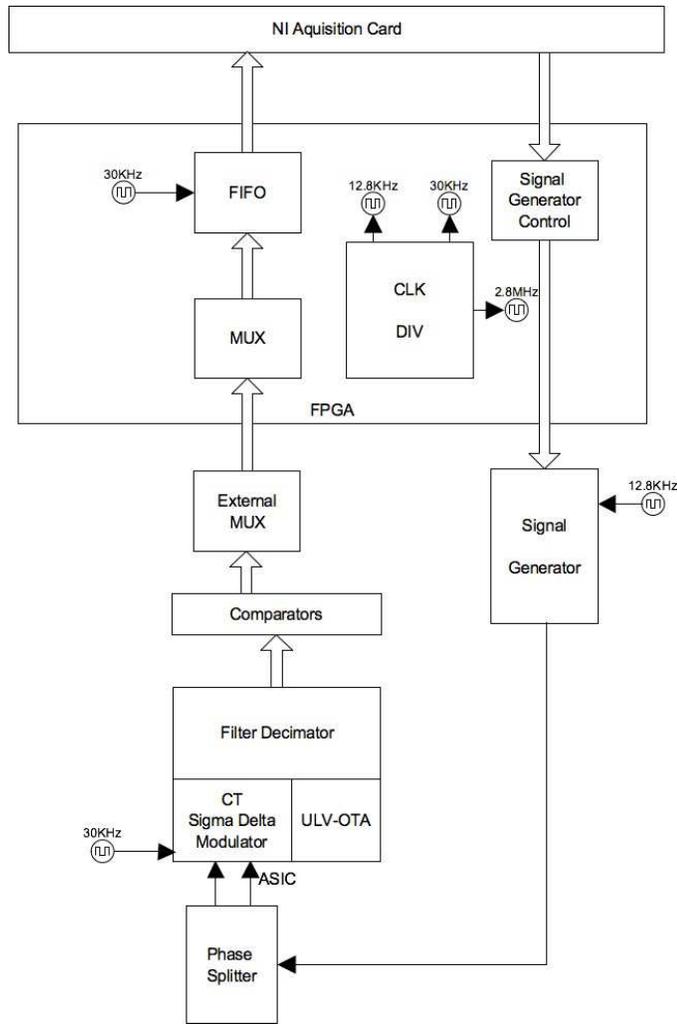
Figure 5.5: Modulator with FIR test and information configuration.

a level of $200\mu V$, having an input common mode voltage of $0V$.

The messured open loop gain was $38.8dB$ with a bandwidth of $10.23KHz$. The figure 5.6 shows the meassured gain for the first stage. The meassured offset for this stage was $400\mu V$.

The figure 5.7 shows the meassured output referred noise. For this test, both inputs were tied to ground and then the noise was meassured at the ouput of the first stage. The ULV-OTA has a noise of $1.4mV rms$ in band of interest (0.5Hz to $100Hz$)f.

For meassuring the open loop gain of the second stage, a frequency sweep from $50Hz$ to $50KHz$ with a $250mV$ input common mode was used.
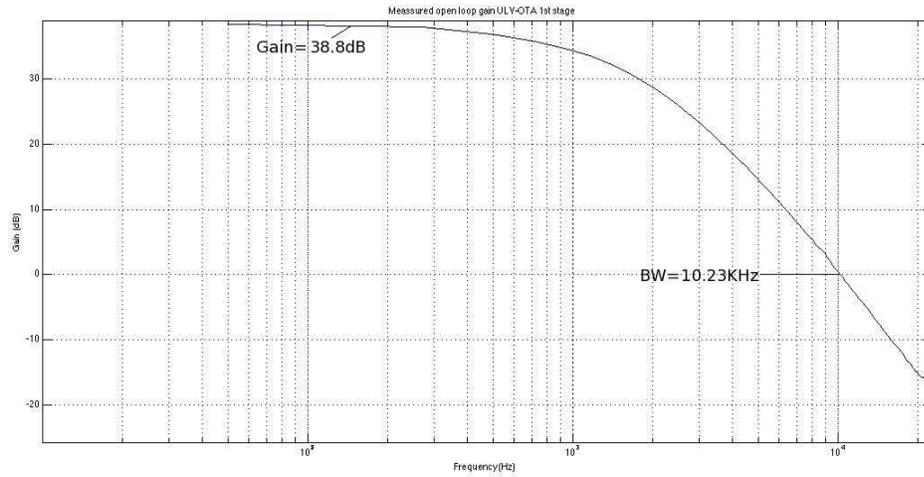
Figure 5.6: ULV-OTA first stage open loop gain.
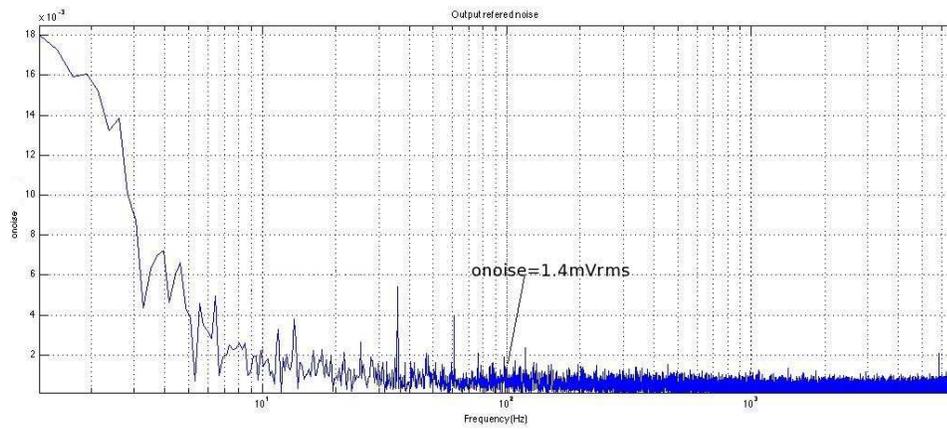
Figure 5.7: Output referred noise.

The figure 5.8 shows the meassured open loop gain for the second stage, where the gain was $18.6dB$ and the bandwidth was $6.45KHz$.

The output swing was also measured since this stage was designed to improve it. The figure 5.9 shows the meassured output swing of the second stage. The CH1 represents the x-axis while the CH2 represents the y-axis. A $300mV$ ouput swing with 2% of distortion was obtained.

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Figure 5.8: ULV-OTA second stage open loop gain.
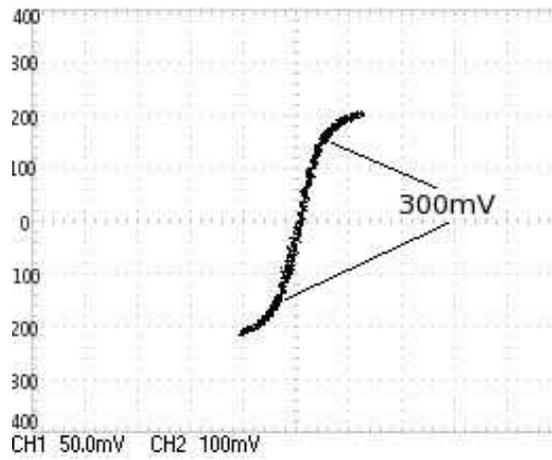
Figure 5.9: Output swing.

5.4.2 ADC test results

In this test a sinusoidal signal of $50Hz$ with $440mV_{pp}$ and $250mV$ input common mode has beed applied to the CT-$\Sigma\Delta$ modulator.

The meassured bitstream is shown in the figure 5.10. However, since the signal in time domain doesn't have information, the PSD of the bistream has been estimated.

From the figure 5.11 the meassured SNR is $94.2dB$ the ENOB is 15.35 $bits$ and the SINAD is $94.38dB$.

The figure 5.12 shows the meassured dynamic range of the modulator. The max-

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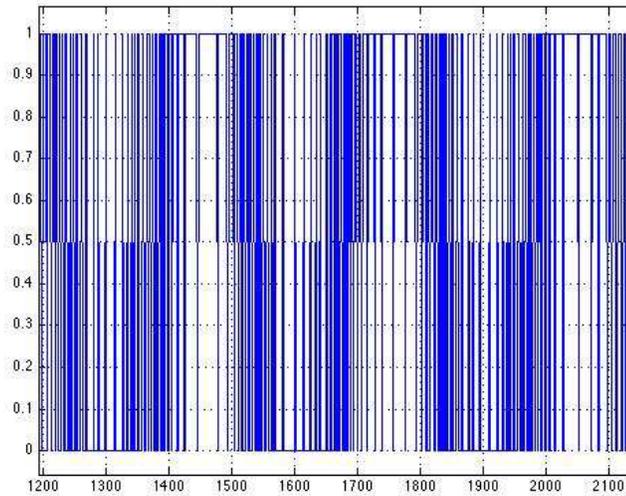
Figure 5.10: Bitstream.
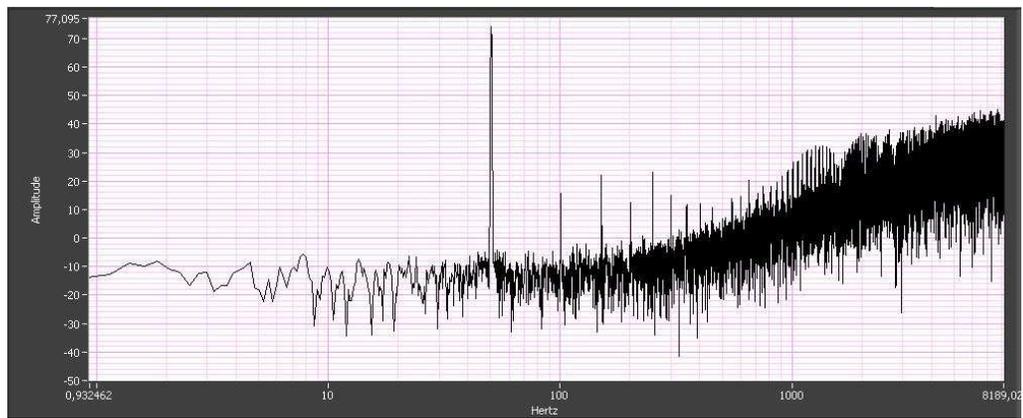
Figure 5.11: PSD of the bitstream.

imum peak is presented at an input signal of -1.11dB and the minimum input signal is -70.69dB.

Finally, the modulator plus the FIR filter were tested, meassuring its DNL and INL. The figure 5.13 shows this meassurement. A DNL of +.783 / -.62 LSB with non missing code, and an INL of +.34 / -2.31 LSB were obtained.
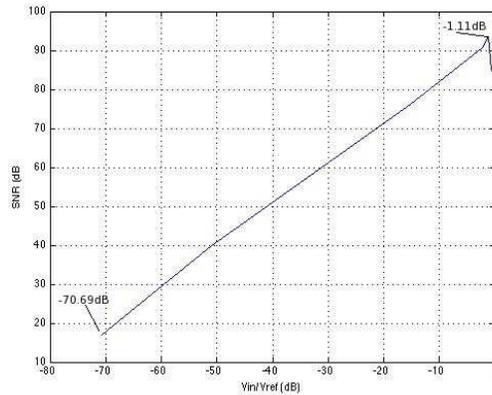
Figure 5.12: CT ADC dynamic range.

5.5   Conclusions

In this chapter the detailed development of the full custom test board was presented. The test board is able to test the proposed ULV-OTA, the $\Sigma\Delta$ Modulator with or without the FIR filter.

Tables 5.1 and 5.2 present a comparison summary of the meassurement results for the ULV-OTA and the modulator, respectively.

For the ULV-OTA measurements of open-loop gain, bandwidth, offset, ouput noise and power dissipation were done. However, the overall ULV-OTA gain was not measured, since the lower achievable V_{pp} of the input signal was $500\mu V$. With this value in the input signal, the output of the ULV-OTA is saturated. Then open-loop gain was measured in each stage.

From table 5.1, is possible to see that the open-loop-gain and bandwidth from simulation and test differ by a significant amount. This is caused, perhaps, by the I_{ptat} circuit. Power dissipation and offset seem to match better to the simulation results.

The modulator was tested using a $50Hz$ sine signal. The measurements performed were Signal to Noise Ratio, Effective Number of Bits, Maximum input peak, Power Dissipation. The test results of the modulator match perfectly with the simulation results showing an excellent design of the $\Sigma\Delta$ Modulator.

In addition to the presented test of the modulator, the modulator was tested in
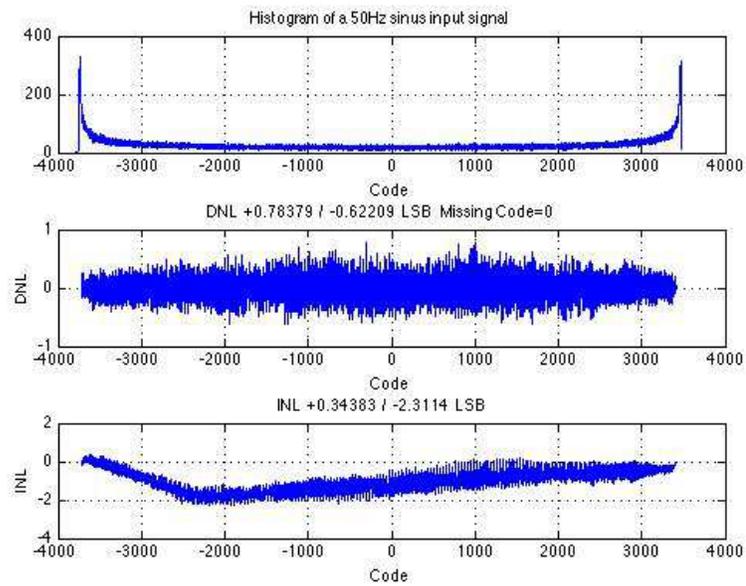
Figure 5.13: Histogram, DNL and INL.

combination with the FIR filter, obtaining excellents measurements of INL, DNL and without any missing code.

Table 5.1: ULV-OTA comparison summary.

Parameters	Measurement	Simulation
Supply Voltage	0.5V	0.5V
Open loop gain		
1rst stage	$38.8dB$	$53dB$
2nd stage	$18.6dB$	$32.5dB$
Bandwidth		
1rst stage	$10.23KHz$	$5.2MHz$
2nd stage	$6.45KHz$	$24.34KHz$
Offset	$400\mu V$	$406\mu V$
Output Noise	$1.4mVrms@100Hz$	$9mVrms@100Hz$
Power Dissipation	$2\mu W$	$1.89\mu W$

Table 5.2: CT$\Sigma\Delta$ modulator comparison summary.

Parameter	Meassurement	Simulation
Supply Voltage	0.5V	0.5V
SNR	$94.2dB$	$95dB$
ENOB	$15.35bits$	$15.48bits$
Max input peak	-1.11dB	-1.71dB
INL	+.34/-2.31 LSB	–
DNL	+.78/-.62 LSB	–
Missing Code	0	–
Power Dissipation	$7\mu W$	$7\mu W$

Chapter 6

A $0.13\mu m$ CMOS Discrete-Time $\Sigma\Delta$ Modulator

Dans ce chapitre la conception d'un modulateur Sigma Delta en temps discret (DT-$\Sigma\Delta$) développé en technologie de $0{,}13\mu m$ CMOS de STMicroeletronics fonctionnant à la tension d'alimentation de 0,5V est présenté. Le modulateur en temp discret a été choisi malgrès ses inconvénients (en particulier consommation plus imporante) par rapport au modulateur en temps continu parce que, dans cette technologie la réalisation de résistances de fortes valeurs s'est avérée demander une surface de silicium inconsidérée.

Dans la section 6,1 le modèle idéal de modulateur est analysé et simulé. Un SNR de $98dB$ avec un OSR de 150 est atteind. La section 6,2 détaille la réalisation du circuit au niveau transistor pour chaque bloc du modulateur. Cette section commence par le circuit général du modulateur, suivi de la présentation de l'OTA. Dans ce modulateur une configuration semblable au cascode OTA est utilisée. En sous-section 6,2,2 les circuits de polarisation de l'OTA sont présentés. Ces circuits agissent en même temps comme réaction de mode commun (CMFF) et en tant que circuits de contre-réaction de mode commun (CMFB). La sous-section 6,2,3 présente le circuit de commutateur et en sous-section 6,2,4 le comparateur de D-latch est présenté.

La section 6,3 présente les résultats de simulation du modulateur de DT-$\Sigma\Delta$. Enfin dans la section 6,4 les conclusions sur la conception de ce modulateurs sont présentées. Dans cette première conception, il n'a pas été pris en considération la compensation des dérives, les erreurs d'appariement, ni les effets non-idéaux des commutations.

Introduction

This chapter presents a ULV-Discrete Time (DT) $\Sigma\Delta$ Modulator developed in a $0.13\mu m$ CMOS tecnology by STMicroelectronics. This process is a multi-well technology that allows NMOS and PMOS isolated substrates, having available design architectures that the $0.35\mu m$ CMOS process would not allow, due to the necessity of connectivity the NMOS substrates to the same potential. However, the $0.13\mu m$ CMOS process is a deep submicron digital technology that does not have a special layer to make high resistances. For example a resistor of $2.5M\Omega$ occupies an area of $9,804\mu m^2$ using 0.13 μm process while in 0.35 μm CMOS technology it occupies just $7,500\mu m^2$. Therefore, if the CT $\Sigma\Delta$ modulator, reported in section **4**, is implemented in this technology the circuit will occupy excessive area having much higher cost. Hence, a DT $\Sigma\Delta$ modulator was selected to use $0.13\mu m$ CMOS technology.

The chapter presents the ideal modulator model in section **6.1**, the analysis of the modulator circuit in section **6.2** and the simulation results in section **6.3**.

6.1 Ideal Model

A second order modulator was choosen due to its good stability. The figure 6.1 shows the architecture of the modulator.
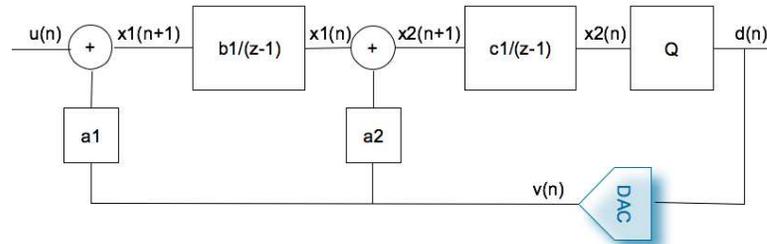
Figure 6.1: Second order DT $\Sigma\Delta$ Modulator.

The modulator is designed for a desired $16bits$ of resolution for which the SNR can be evaluated as follows:

$$SNR = 6.02ENOB + 1.76 \tag{6.1}$$

SNR is then $98dB$ and an OSR of 150 is needed.

In order to compute the modulator's coeficients the $\Sigma\Delta$ Matlab Toolbox [62] was used. The obtained coefficients are $\{a_1 = 0.2673,\ a_2 = 0.2309,\ b_1 = 0.2673$ and $c_1 = 0.3\}$. The a_i coefficients are the DAC's coefficients and the b_1 and c_1 are scaling coefficients.

The figure 6.2 show the bitstream of the ideal model simulated with the $\Sigma\Delta$ Matlab Toolbox. In this simulation the techonology limitations are not took into account. The figure 6.3 shows the PSD of the bitstream.
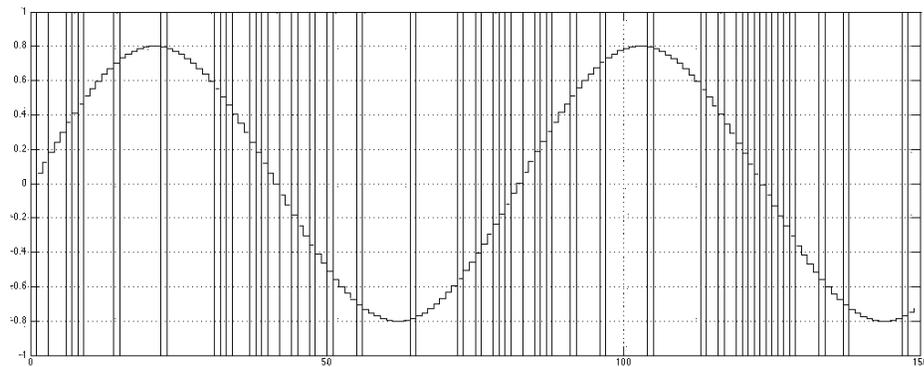
Figure 6.2: Bitstream of the ideal model.
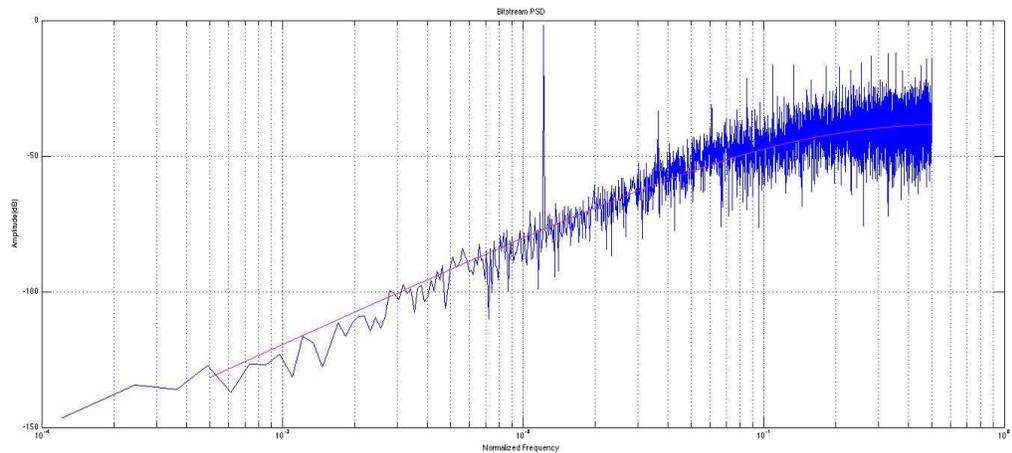
Figure 6.3: Bitstream's PSD.

In figure 6.4 the dynamic range is shown, where the maximum input is -1.71dB

with a SNR of $92dB$.
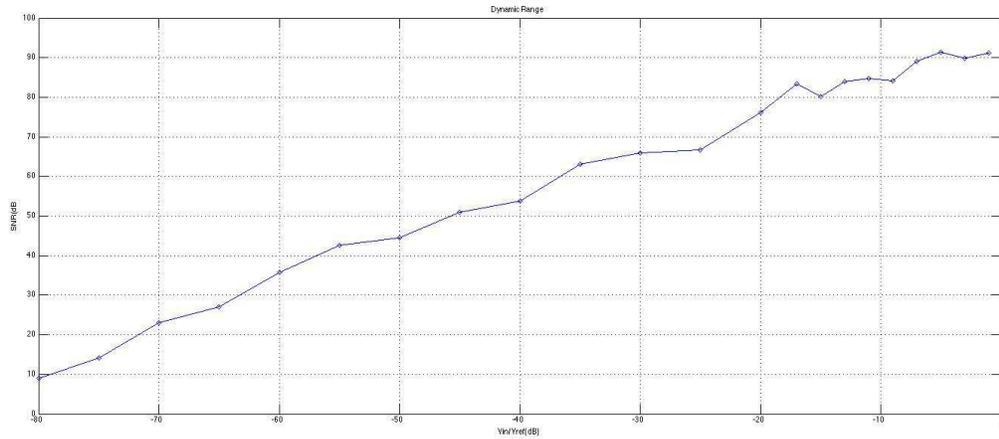
Figure 6.4: Modulator's dynamic range.

6.2   Modulator's Circuit

The figure 6.5 shows the schematic circuit of the modulator. In order to calculate the value of the capacitances, the difference equations of the modulator (eqs. 6.2 and 6.9) must be solved.
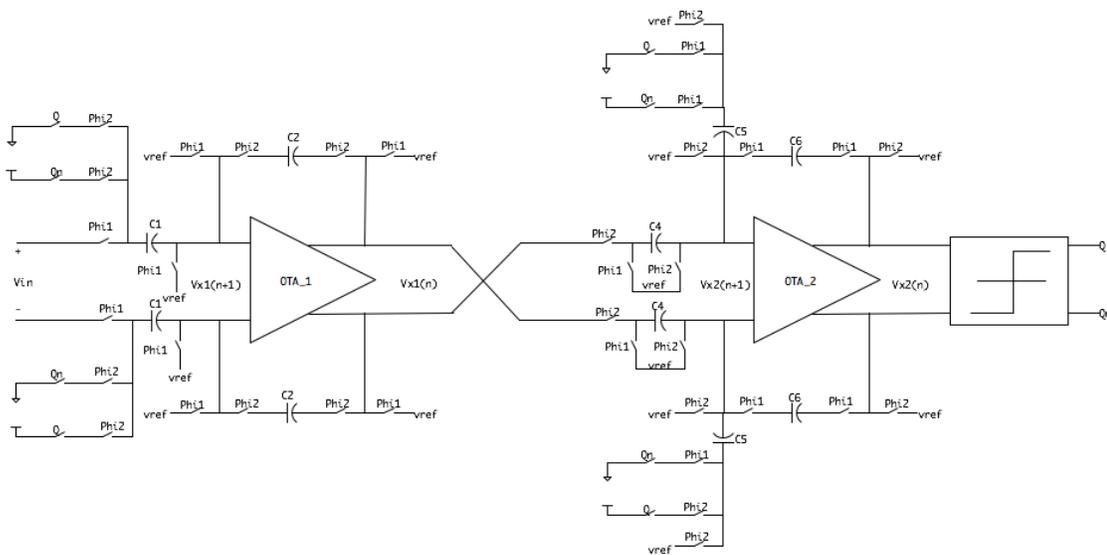
Figure 6.5: ADC circuit model.

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For computing the values of C_1 and C_2 we have:

$$x_1(n+1) = x_1(n) + b_1 u(n) - a_1 v(n) \tag{6.2}$$

where $x_1 = V x_1 / 1V$, $u = (Vin - 0.25V)/0.25V$ and $v = 2v_d - 1$.

Substituting,

$$V x_1(n+1) = V x_1(n) + b_1 \frac{V_{in} - .25}{.25} - a_1 [2v_d - 1]1V \tag{6.3}$$

$$V x_1(n+1) = V x_1(n) + \frac{b_1 V_{in}}{.25} - 2a_1 v_d 1V \tag{6.4}$$

$$V x_1(n+1) = V x_1(n) + 1.096 V_{in} - .5346 V v_d \tag{6.5}$$

$$V x_1(n+1) = V x_1(n) + \frac{2C_1}{C_2} V_{in} - \frac{2C_1}{C_2} V_{DD} v_d \tag{6.6}$$

Then,

$$\frac{2C_1}{C_2} = 1.092 \tag{6.7}$$

or

$$\frac{2C_1}{C_2} 0.5 = .5346 \tag{6.8}$$

Making C_1 equal to $1pF$, C_2 is $1.87pF$.

For obtaining the values of C_4, C_5 and C_6 we have,

$$x_2(n+1) = x_2(n) + c_1 x_1(n) - a_2 v(n) \tag{6.9}$$

Substituting,

$$V x_2(n+1) = V x_2(n) + \frac{2V_{in}}{3} - .2309[2v_d - 1]1V \tag{6.10}$$

$$V x_2(n+1) = V x_2(n) + \frac{2C_4 V_{in}}{C_5} - \frac{2C_6 V_{DD}}{C_5} v_d + .2309V \tag{6.11}$$

Then,

$$\frac{2C_4}{C_5} = 2/3 \tag{6.12}$$

or

$$\frac{2C_6}{C_5} 0.5 = .4618 \tag{6.13}$$

Making C_5 equal to $2pF$, C_4 is $0.666pF$ and C_6 is $.923pF$.

6.2.1 Ultra-low voltage OTA

A modified version of the OTA proposed in chapter **4** is now described. The first stage is based in the FC-OTA and the second stage is based in the CSA topology. As the tail current were removed for the design, a common mode feedforward (CMFF) and common mode feedback (CMFB) circuits are added.

First stage OTA

The core of this topology is similar to the 0.35 μm ULV-OTA. The main differences arise in the input device (NMOS) and in the added gain boost circuit. The proposed circuit is shown in figure 6.6.
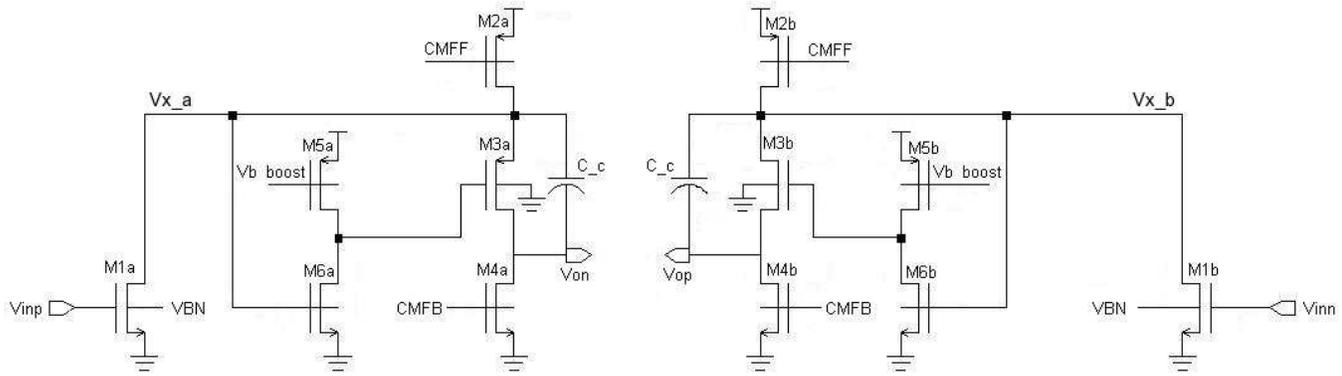
Figure 6.6: First stage ULV-OTA.

A pseudo-differential input NMOS pair is used as input ($M1_a$ and $M1_b$). The bulks of the input devices are forward biased in order to reduce the V_{TH} and increase the inversion level. Transistors $M3_a$ and $M3_b$ constitute two symmetric CGA whose bulk is forward biased. The gate of these transistors is fed by the ouput of the gain boost circuit. This circuit allows an increase in r_{out} to about $r_{out}A_{boost}$.

Transistors $M2_a$ and $M2_b$ are the current sources for the CGA and for the input devices. The gate of these transistors are fed by the CMFF circuit. Both CGAs have an active load performed by transistors $M4_a$ and $M4_b$, its gate are used to set the V_{ocm}. The desired V_{ocm} is $V_{DD}/2$ in order to have maximum output swing.

The small signal model of the proposed OTA is shown in figure 6.7.
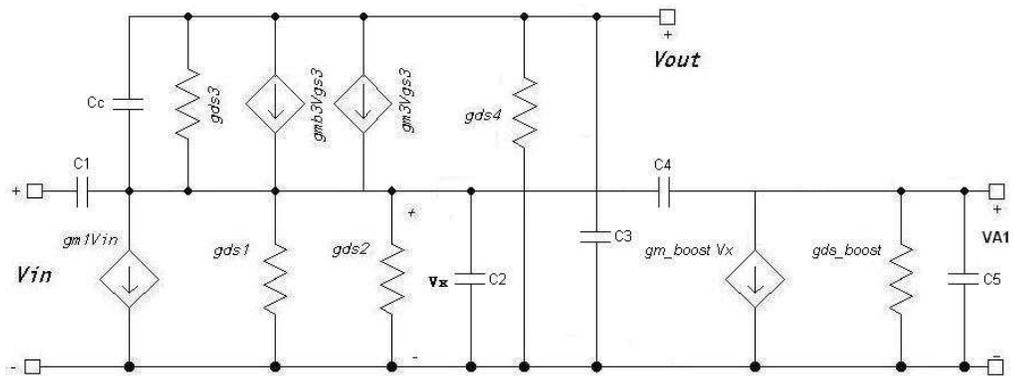
Figure 6.7: OTAs small signal model

The r_{out} is given by :

$$r_{out} = ((r_{ds3} + r_e + (gm_3 + gm_{b3})r_{ds3}r_e)||r_{ds4})gm_{boost}r_{boost} \quad (6.14)$$

Where r_e is $1/(g_{ds1} + g_{ds2})$, then:

$$r_{out} = \frac{g_{ds1} + g_{ds2} + g_{ds3} + gm_3 + gm_{b3}}{g_{ds4}(g_{ds1} + g_{ds2} + g_{ds3} + gm_3 + gm_{b3}) + g_{ds3}(g_{ds1} + g_{ds2})}(\frac{gm_{boost}}{g_{dsboost}}) \quad (6.15)$$

The gain is therefore:

$$A_v = \frac{-gm_1 gm_{boost}(g_{ds3} + gm_3 + gm_{b3})}{(g_{ds4}(g_{ds1} + g_{ds2} + g_{ds3} + gm_3 + gm_{b3}) + g_{ds3}(g_{ds1} + g_{ds2}))g_{dsboost}} \quad (6.16)$$

where g_{mboost} and $g_{dsboost}$, are g_{m6} and $g_{gs5} + g_{ds6}$ respectively.

The frequency response of the OTA is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{-g_{m1}(g_{ds3} + g_{m3} + g_{mb3} + sC_c)}{K + As + Bs^2}\right)\left(\frac{g_{m6} - sC_6}{g_{ds5} + g_{ds6} + sC_5}\right) \quad (6.17)$$

where

$a = A/K$

$b = B/K$

and

$A = (g_{ds3} + g_{ds4})C_2 + (g_{ds1} + g_{ds2} + g_{ds4})C_c + (g_{ds1} + g_{ds2} + g_{ds3} + g_{m3} + g_{mb3})C_3,$

$B = C_3C_2 + C_3C_c + C_2C_c,$

$$K = g_{ds3}(g_{ds1} + g_{ds2}) + g_{ds4}(g_{ds1} + g_{ds2} + g_{ds3} + g_{m3} + g_{mb3})$$

the dominant pole is therefore,

$$p_1 = -\frac{g_{ds3} + g_{ds4}}{C_c}$$

and the GBW defined as $A_v|p_1|$ is:

$$GBW = \frac{g_{m1}(g_{m3} + g_{mb3})}{(g_{ds1} + g_{ds2})(g_{ds5} + g_{ds6})C_c} \tag{6.18}$$
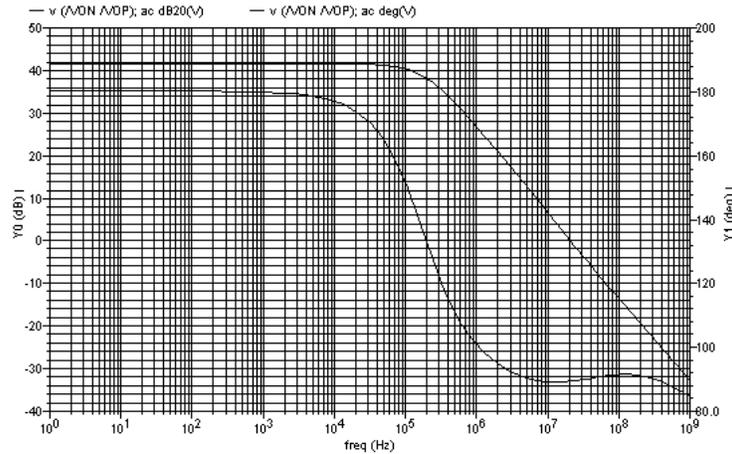
Figure 6.8: First stage pen loop gain.

Figure 6.8 shows the simulated open loop gain for this stage. The obtained gain was $42dB$ with a BW of 20MHz and a phase margin of 90°.

ULV-OTA second stage

As we mention before, this output stage is cascaded after the first stage in order to achive higher gain while maximizing the ouput swing.

Devices NMOS M_{7a} and M_{7b} are used as input transistors. Transistors M_8 are current sources; and their gates are connected to the CMFB output circuit, in order to set the V_{ocm} in $V_{DD}/2$. Figure 6.9 shows the diagram of the Current Source Amplifier
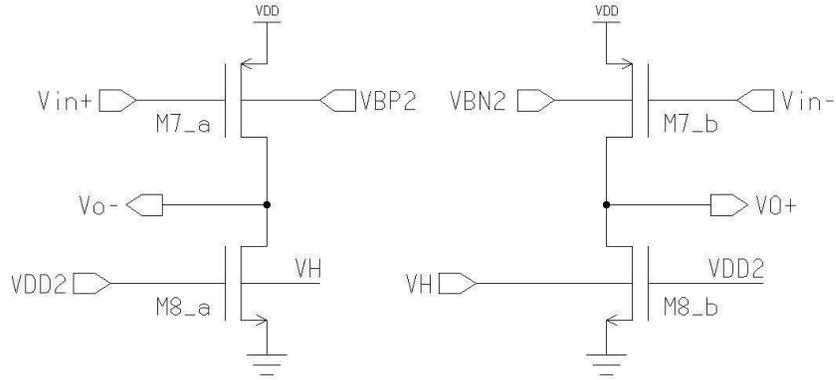
Figure 6.9: ULV-OTA second stage.

(CSA).

The gain of this stage is obtained by analyzing the small signal model (figure 6.10):
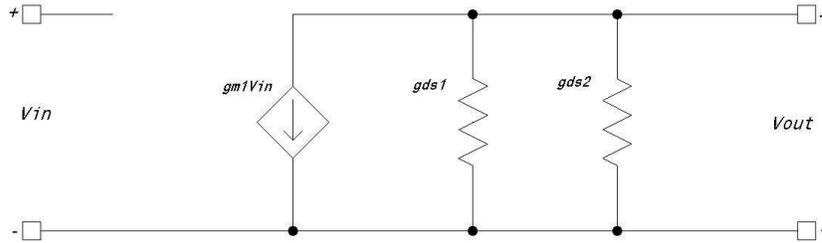
Figure 6.10: Output OTAs small signal model

$$0 = g_{m7}V_{in} + (g_{ds7} + g_{ds8})V_{out} \tag{6.19}$$

Solving for V_{out}/V_{in} we obtain the voltage gain as follows:

$$A_{v_2} = \frac{-g_{m7}}{g_{ds7} + g_{ds8}} \tag{6.20}$$

The simulated open loop gain is $25.8dB$ with a BW of $14MHz$ and PM of 92.5^o. The simulation is shown in figure 6.11.
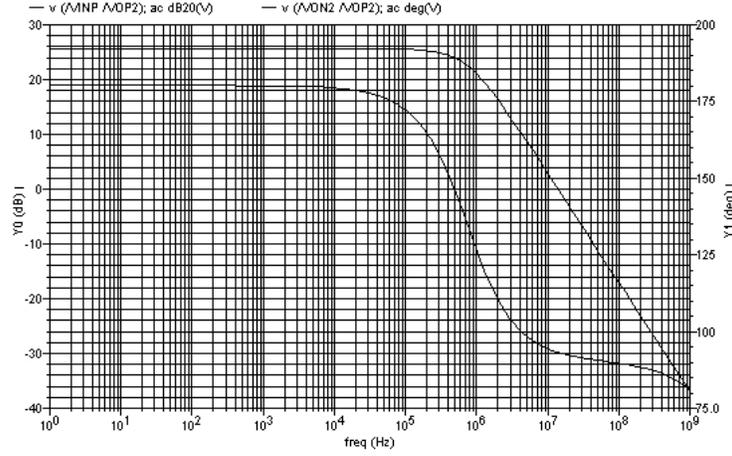
Figure 6.11: Open loop gain and phase of the second stage.

The whole amplifier gain is:

$$A_{v_{out}} = A_{v_1} \times A_{v_2} \tag{6.21}$$

The transistors dimensions of the ULV-OTA used for the simulations are shown in the table 6.1.

Table 6.1: ULV-OTA transistors dimensions.

Device	W	L	Device	W	L
$M1_{a,b}$	1.2 μm	.4μm	$M7_{a,b}$	1.18 μm	.4μm
$M2_{a,b}$	119.45 μm	.4μm	$M8_{a,b}$	10 μm	.4μm
$M3_{a,b}$	9 μm	.4μm			
$M4_{a,b}$	.43 μm	.4μm			
$M5_{a,b}$	5 μm	.4μm			
$M6_{a,b}$	.8 μm	.4μm			

The figure 6.12 shows the gain and phase plots of the whole proposed amplifier. A gain of $66dB$ is obtained with a BW of 600MHz.

The figure 6.13 shows the montecarlo simulation for obtaining the offset. The obtained offset is $1.18mV$.

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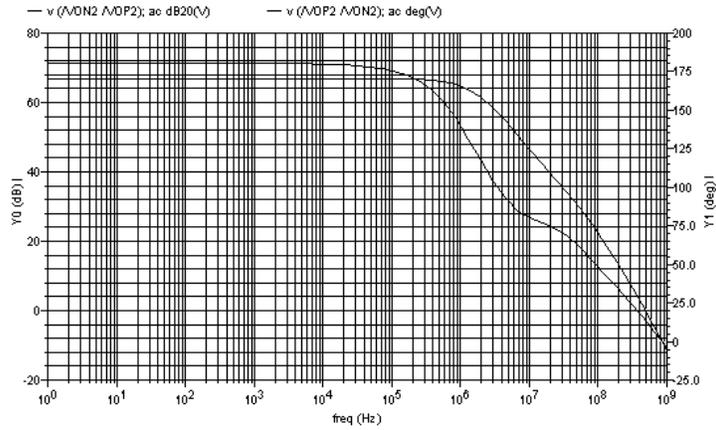
Figure 6.12: Open loop gain and phase.
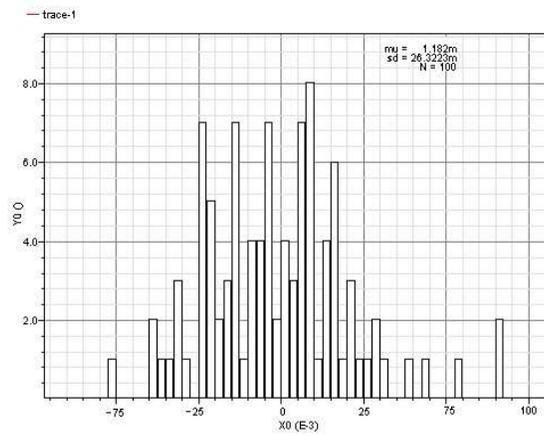
Figure 6.13: Simulated Offset.

The results are summarized in table 6.2.
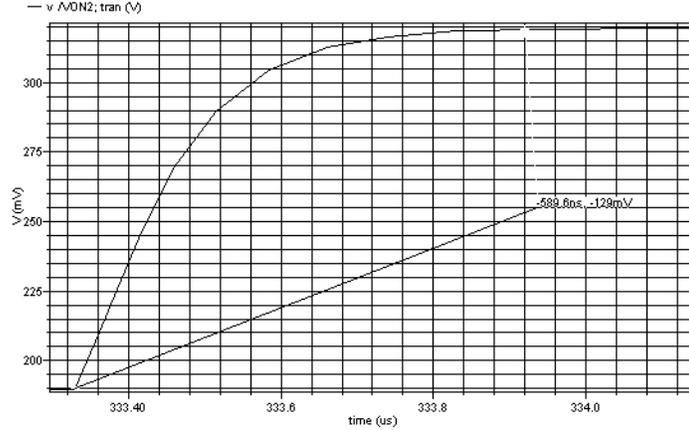
Figure 6.14: Amplifer settling time.

Table 6.2: ULV-OTA comparison summary.

Parameters	Value
Open loop gain	$66dB$
Bandwidth	$600MHz$
Offset	$1.18mV$

6.2.2 Biasing Circuits

The circuits here presented are used to set the DC operational point of the amplifier and they also are used as CMFF and CMFB circuits.

For the first stage to circuits are developed, a CMFF and CMFB circuit while for the second stage only a CMFB circuit has been developed.

Switched Capacitor Common Mode Feedback Circuit

A Switched Capacitor (SC) common mode feedback (CMFB) circuit is used to stabilize the ouput common mode voltage. Figure 6.15 shows the SC-CMFB circuit.

The SC CMFB circuit consists of a C_c and C_s capacitors, and eight switches controled by two clocks with non-overlaping phases.

In the SC CMFB the V_{ocm} represents the desired biasing output common mode voltage, $V_{desired}$ represents the desired biasing voltage for the OTA current sources $M4_i$ for getting the V_{ocm}.

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During the active phase ϕ_1, C_s is charged with $V_{ocm} - V_{desired}$; when phase ϕ_2 is active, the charges are redistributed between C_s and C_c.
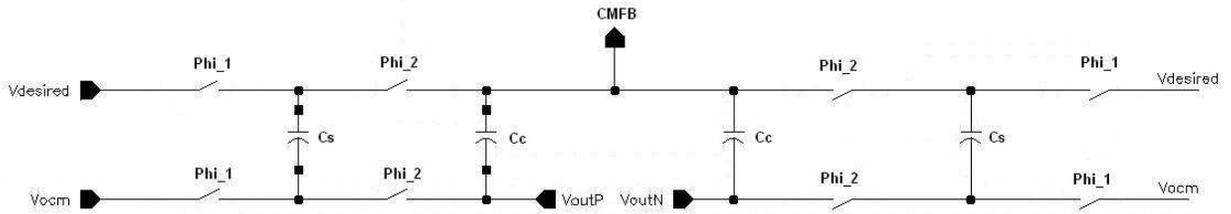
Figure 6.15: SC-Common mode feedback circuit.
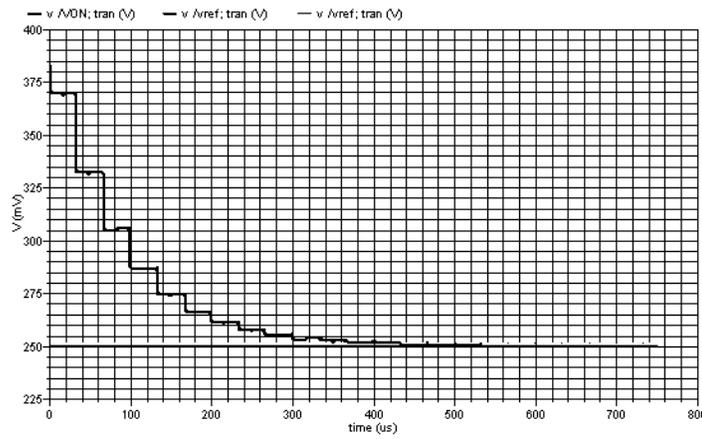
Figure 6.16: First stage output common mode.

The convergence for CMFB of the first stage is shown in figure 6.16.

Figure 6.17 shows the CMFB convergence for the second amplifier stage.

The convegence for both stages occurs at $416\mu S$.
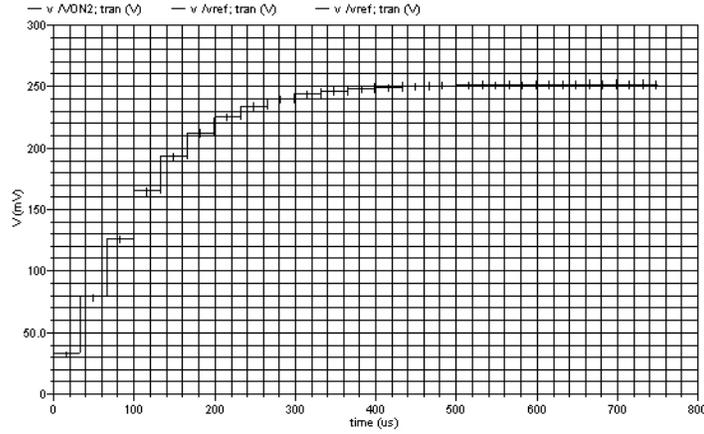
Figure 6.17: Second stage output common mode.

Common mode Feedforward Circuit

As the I_{tail} has been removed, a common mode feedforward circuit is needed for performing the CM operation. Figure 6.18 shows the circuit.
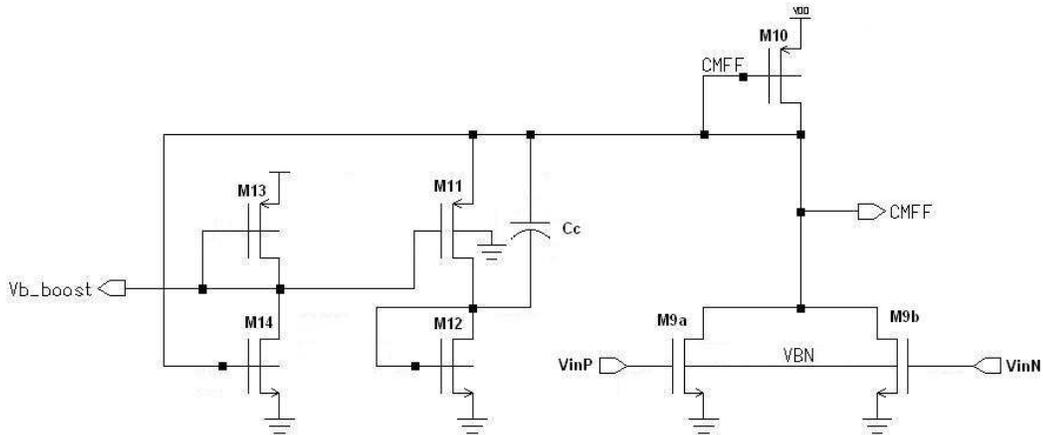
Figure 6.18: Common mode Feedforward circuit.

The circuit performs a transconductor whose differential transconductance is zero. The output current of this transconductor is substracted out from the output current of the ULV-OTA. The circuits then performs a feedforward cancellation path.

The current of this circuits is fed in the ULV-OTA by means of the device M_{10} and M_{13}.

The devices should be one half of the ULV-OTA input devices.

6.2.3 Switch

The switch is performed by a simple transmission gate circuit, that is shown in figure 6.19.
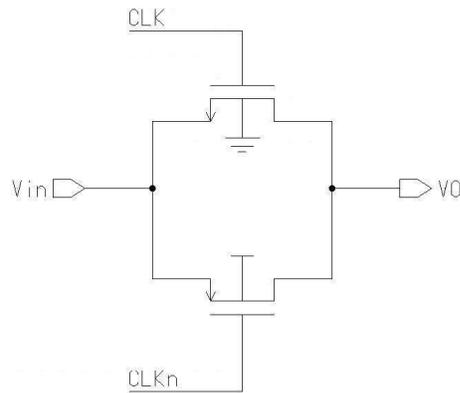
Figure 6.19: Transmission gate circuit used as CMOS switch.

6.2.4 Comparator

Figure 6.20 shows the latch based comparator. The comparator consists of a sampling stage, performed by switches S_1 and S_2, a bulk-driven comparator stage and a D-latch.

When the CLK is high, the switches S_1 and S_2 are sampling the input signal. Then when the CLK is low the signal is compared, having a valid output. Finally the signal is feed into the D-latch. The latch works with a delayed version of the CLK's high value.
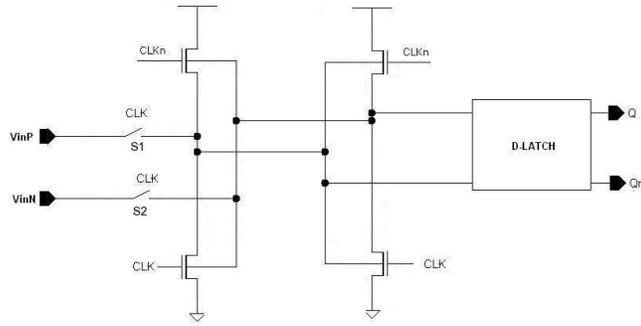
Figure 6.20: Quatizer using D-latch.

6.3 DT-$\Sigma\Delta$ Modulator performance

The results are summarized in the table 6.3.

Table 6.3: DT-$\Sigma\Delta$ Modulator performance.

Parameters	
SNR	$92dB$
ENOB	14.99 $bits$
Max. input peak	-1.7 dB

The achived SNR was 92dB with an OSR of 150. However by incrementing the OSR a higher SNR could be obtained.

6.4 Conclusions

In this chapter the design of a DT-$\Sigma\Delta$ Modulator developed in a $0.13\mu m$ CMOS technology by STMicroeletronics working at supply voltage of 0.5V was presented. The DT Modulator was selected over its CT counterpart, because, if an architecture similar to the proposed in chapter **4** is implemented, more area is needed incrementing enormously the cost.

The ideal modulators was simulated, showing a good performance of the DT Modultor. As a result of the good behavior of the modulator, a circuit was designed. In this first design, it has not been considered the compensation of the skew effects, mismatch contributions, non-ideal switching effects. However, preliminary results show the viability of developing this modulator architecture using a supply voltage of 0.5V.

Chapter 7

Conclusions and Future work

Conclusion

Dans ce travail, la faisabilité de la réalisation de circuits très basse tension, utilisant une technologie CMOS 0,35μm alimentés en seulement 0,5V alors que la technologie demande en fonctionnement standard 3,3 volts, pour un EEG utilisant une technologie CMOS a été étudiée. En particulier, un amplificateur très basse tension (ULV-OTA) et un modulateur $\Sigma\Delta$ à temps continu (CT-$\Sigma\Delta$) avec leurs circuits de polarisation ont été développés.

Dans ce travail de thèse, nous avons proposé une architecture originale pour l'ULV-OTA. L'ULV- OTA a été optimisé pour le traitement des signaux d'EEG et se compose de deux étages. La premier étage est basée sur un circuit cascode replié (FC-OTA) et le second étage est basé sur un amplificateur de courant (CSA) qui a été ajouté pour maximiser la dynamique de sortie du signal. Le tableau 7,1 résume les performances obtenue à partir des mesures et des simulations.

Un incrément dans la tension de grille des dispositifs M_2, provoquée par le circuit polarisé d'Iptat, est probablement la cause de la dégradation du gain du premier étage.

Bien que les résultats de mesures ne soient pas parfaitement conformes aux simulations pour le pré-amplificateur, les performances obtenues pour l'ULV-OTA proposé peuvent être comparée aux meilleures réalisations décrites dans l'état de l'art. Dans le tableau 7,2, les résultats de simulation de ce travail sont comparés à l'état de l'art. En particulier, la puissance consommée est une des plus faible comparée aux autres réalisations.

En ce qui concerne l'ADC, on a proposé une architecture CT-$\Sigma\Delta$ du second ordre. Ce modulateur fonctionne avec un OSR de 150 et atteint un rapport signal à bruit (SNR) de 94.2dB. Le modulateur a été conçu pour fonctionner avec une tension

d'alimentation de 0,5V. Le modulateur a été optimisé pour des signaux d'EEG, tel que le signal d'entrée doit être entre 0,5Hz et 100Hz. Le filtre de décimation composé d'un filtre FIR, n'a pas été optimisé pour fonctionner à 0,5V, toutefois il fonctionne avec une tension de 1V.

Le tableau 7,3 résume les résultats obtenus pour les simulation et les mesures. Les résultats de test sont très proches de ceux prédits par la simulation. Les résultats de l'ULV-OTA et très bonnes caractéristiques obtenus pour le modulateur CT-$\Sigma\Delta$, montrent qu'il est possible de mettre en uvre les circuits en très bas tension en cette technologie avec quelques restrictions sur la largeur de bande et la vitesse. Les performances obtenus pour le circuit de traitement AFE proposé sont très approprié pour les dispositif biomédicaux basse consommation comme les dispositif portatif d'EEG. Le tableau 7,4 permet de comparer les résultats obtenus pour le convertisseur avec l'état de l'art.

En plus de cet ASIC développé en technologie CMOS 0,35μm, un modulateur $\Sigma\Delta$ de temps discret a été conçu et simulé utilisant une technologie CMOS 0,13μm. Un modulateur du second degré a été choisi, ayant un OSR de 150 obtenant un SNR de 92dB.

La topologie de l'OTA dans les modulateurs est semblable à celle proposée en le chapitre 4. Cette topologie a obtenue une largeur de bande plus grande et un temps de stabilisation réduit. Il présente donc des caractéristiques compatibles avec contraintes de réponse de l'intégrateur.

Le modulateur de DT-$\Sigma\Delta$ a été seulement simulé et les résultats sont donnés dans le tableau 7,5.

Les contributions principales de ce travail de recherches sont :

- Un OTA topologie de très faible tension de alimentation.

- Des circuits de polarisation.

- Une carte de test dédiée.

- Un modulateur CT-$\Sigma\Delta$ de très basse puissance

- Un modulateur DT-$\Sigma\Delta$ de très faible tension d'alimentation

7.1 Conclusions

In this work, the implementation feasibility of ultra-low voltage circuits for an EEG using a $0.35\mu m$ CMOS technology has been studied. Particulary an ULV-OTA and a CT $\Sigma\Delta$ modulator with their bias circuits were developed.

A novel architecture for the ULV-OTA was proposed in this thesis. The ULV-OTA was customized for processing of EEG signals and consists of two stages. The first stage is based on a FC-OTA and the second stage is based on a CS-Amplifier which was added to increase the output swing of the signal.

Table 7.1 shows a comparative performance parameters obtained from meassurements and simulations.

Table 7.1: ULV-OTA comparison summary.

Parameters	Measurement	Simulation
Supply Voltage	0.5V	0.5V
Open loop gain		
1rst stage	$38.8dB$	$53dB$
2nd stage	$18.6dB$	$32.5dB$
Bandwidth		
1rst stage	$10.23KHz$	$5.2MHz$
2nd stage	$6.45KHz$	$24.34KHz$
Offset	$400\mu V$	$406\mu V$
Output Noise	$1.4mVrms@100Hz$	$9mVrms@100Hz$
Power Dissipation	$2\mu W$	$1.89\mu W$

An increment in the gate voltage of the M_2 devices, provoked by the Iptat bias circuit, could be the cause of the gain degradation in the first stage.

Even though the measurements do not match with the simulation results, the performance of the proposed ULV-OTA can be compared with previously reported devices. In table 7.2, the simulation results of this work are compared with the state-of-the-art. The power dissipation performance is one of the best compared with the latest reported devices.

For the ADC, a 2nd order CT-$\Sigma\Delta$ architecture was proposed. The CT $\Sigma\Delta$ modulator works with a 150 OSR and achieves a SNR of $94.2dB$. The modulator was designed to operate with $0.5V$ of supply voltage. The modulator was customized for EEG signals, such that the input signal must be between $0.5Hz$ and $100Hz$. The FIR

Table 7.2: Low-voltage amplifiers specification comparison.

Supply	Gain	BW	Consumption	Noise	Process	Ref
0.5V	52dB	2.5MHz	$110\mu W$	$280\frac{nV}{\sqrt{Hz}}$@10KHz	$0.18\mu m$	[43] (body)
0.5V	62dB	10MHz	$75\mu W$	$225\frac{nV}{\sqrt{Hz}}$@10KHz	$0.18\mu m$	[43] (gate)
0.5V	55dB	8.7MHz	$77\mu W$	$157\frac{nV}{\sqrt{Hz}}$@10KHz	$0.18\mu m$	[44]
0.5V	61dB	41MHz	$510\mu W$	$28\frac{nV}{\sqrt{Hz}}$@10KHz(in)	$0.18\mu m$	[45]
0.5V	58dB	13.5MHz	$.085\mu W$	$-$	$0.18\mu m$	[46]
0.5V	65dB	550KHz	$28\mu W$	$675\frac{nV}{\sqrt{Hz}}$@10KHz (in)	$0.18\mu m$	[47]
0.5V	90dB	100KHz	$1.5\mu W$	$-$	$0.35\mu m$	[48]
0.5V	80dB	510KHz	$2\mu W$	$240\frac{nV}{\sqrt{Hz}}$	$0.35\mu m$	This work

based decimation filter, was not optimzed to work at 0.5V, however it operates at low voltage of $1V$.

The table 7.3, shows the results obtained from the simulation and from the test. There is a high coherency among the results showing that the modulator has a good performance.

Table 7.3: CT$\Sigma\Delta$ modulator comparison summary.

Parameter	Meassurement	Simulation
Supply Voltage	0.5V	0.5V
SNR	$94.2dB$	$95dB$
ENOB	$15.35bits$	$15.48bits$
Max input peak	$-1.11dB$	$-1.71dB$
INL	$+.34/-2.31$ LSB	$-$
DNL	$+.78/-.62$ LSB	$-$
Missing Code	0	$-$
Power Dissipation	$7\mu W$	$7\mu W$

The results of the ULV-OTA and the excellent performance of the CT-$\Sigma\Delta$ modulator, show that it is possible to implement ultra low voltage circuits in this technology with some restrictions in bandwidth and speed. Moreover, the results show that the proposed AFE is very suitable for biomedical low-power dissipation as a portable EEG device. A comparison among the proposed modulator with other reported modulators is shown in table 7.4, where is possible to see that the performance of our modulator.

In addition to the ASIC developed in $0.35\mu m$ CMOS technology, a Discrete-Time $\Sigma\Delta$ modulator was designed and simulated using a $0.13\mu m$ CMOS technology. A sec-

Table 7.4: CT $\Sigma\Delta$ ADC specification comparison.

Supply	SNDR	BW	Consumption	Process	Ref
0.5V	74dB	25KHz	$300\mu W$	$0.18\mu m$	[55]
0.5V	81dB	25KHz	$300\mu W$	$0.18\mu m$	[56]
1.5V		15MHz	$70mW$	$0.13\mu m$	[57]
1.5V	74dB	600KHz	$6mW$	$90nm$	[58]
0.5V	94.2dB	100Hz	$7\mu W$	$0.35\mu m$	This work

ond order modulator was selected, having an OSR of 150 and obtaining a SNR of $92dB$.

Table 7.5: DT-$\Sigma\Delta$ Modulator performance.

Parameters	Simulation
SNR	$92dB$
ENOB	$14.99\ bits$
Max. input peak	$-1.7\ dB$

The OTA's topology in the modulator is similar to the one proposed in chapter 4. This topology, obtained a higher bandwidth and settling time, therefore, it is a good candidate to be used in the modulator's integrator device.

The DT $\Sigma\Delta$ modulator was simulated only and the results appear in table 7.5.

The main contributions of this research work are:

- Ultra-low voltage OTA novel topology

- Biasing circuits

- Full Custom Test board

- An ultra-low voltage low power CT-$\Sigma\Delta$ Modulator

- An ultra-low voltage DT-$\Sigma\Delta$ Modulator

7.2 Future Work

As the ULV-OTA did not achieve the expected results, an analysis and evaluation of other Iptat circuit are suggested. Moreover, some improvements in the CM feedfor-

ward path could be done.

Once the test of the amplifier match the expected parameters, a multichannel AFE must be designed.

Future analysis for higher order CT $\Sigma\Delta$ modulator must be done in order to reduce the OSR.

In a short term, the layout for the DT $\Sigma\Delta$ modulator and its test card must be developed.

Other work to continue with this development are:

- Add a digital processing algorithms for artifacts removal

- Add a transceiver

- Include a programmable gain amplifier in the overall device

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