Techniques d’impression et matériaux semiconducteurs pour l’électronique plastique

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Techniques d'impression et materiaux semiconducteurs pour l'électronique plastique

-

Stamping Techniques and Semiconducting Materials for Plastic Electronics

Soutenue le 18 octobre 2005 devant la commission d'examen composée de :

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Chapter 1

Introduction

Nous vivons dans une société ou l'image est un important vecteur de communication. Au cours de l'histoire, l'homme n'a cessé d'améliorer les supports physiques permettant de projeter et de diffuser l'information contenue dans ces images. Les récents progrès de l'électronique ont permis de rendre ce moyen de communication plus vivant, réactif à la demande de l'observateur. De nombreux supports permettent aujourd'hui une réactualisation rapide du contenu visuel permettant ainsi une mise à jour constante de l'information véhiculée. Ces systèmes de projection d'images font un usage intensif de matériaux semi-conducteurs dits "classiques" tel que le silicium mono-cristallin. En raison de leur inhérente fragilité, ces types de semi-conducteurs inorganiques ont des propriétés mécaniques qui se prêtent mieux à la fabrication de circuits sur substrats rigides ayant des propriétés chimiques compatible avec les procédés à haute température nécessaires à la production de systèmes optoélectroniques performants.

Pour permettre la fabrication de tels systèmes électroniques sur supports souple, de nouveaux matériaux et techniques de fabrication doivent être inventés. Ces nouvelles méthodes ont pour ultime but la création d'une gamme nouvelle de dispositifs électroniques sur des substrats ayant des propriétés chimiques et mécaniques variées, pouvant entre autre être légers, flexibles et peu onéreux. Le développement de matériaux semi-conducteurs ayant des propriétés biochimiques adéquates permettra aussi d'ajouter des fonctionnalités inédites à ces systèmes électroniques "souples" qui sont aujourd'hui difficilement réalisables avec les techniques et matériaux couteux utilisés en micro-électronique conventionnelle. Ces recherches déboucheront dans un futur proche sur la commercialisation d'écrans souples avec des produits destinés au marché public par le biais de nombreux secteurs de diffusions tels que: la téléphonie, la télévision, la publicité, l'architecture, la mode. De plus, de nouvelles applications naîtront à la demande de l'industrie aéronautique, automobile, spatiale et de l'armée.

La première partie de ce travail de recherche concerne le développement de nouvelles techniques de fabrication qui permettront la fabrication, à bas coups, sur de grandes surfaces, de ces circuits électroniques souples. Nous verrons à travers de nombreux exemples de prototypes que

ces nouvelles techniques représentent une alternative intéressante aux techniques de lithographie “classiques” développées par l’industrie de la micro-électronique. La deuxième partie de cette thèse sera portée sur une étude plus “fondamentale” d’un semi-conducteur organique ayant des propriétés électroniques très prometteuses : le rubrene. Par le biais de nouvelles méthodes de fabrication, que nous avons spécifiquement développées pour tester ce matériau à l’état cristallin, nous verrons comment nous avons réussi à enrichir les connaissances scientifiques relatives aux phénomènes de transport de porteurs dans les matériaux organiques.

Le corps de ce document est rédigé en anglais afin de permettre une meilleure diffusion de ces résultats de recherche.

Part I

Stamping Techniques for Micro and Nanofabrication

Chapter 2

Overview of Stamping Techniques: Methods and Applications

2.1 Introduction

There is considerable interest in methods for building structures that have micron or nanometer dimensions. Historically, research and development in this area has been driven mainly by the needs of the microelectronics industry. The spectacularly successful techniques that have emerged from those efforts – photolithography, electron beam lithography, *etc.* – are extremely well suited to the tasks for which they were principally designed: forming structures of radiation sensitive materials (*e.g.* photoresists or electron beam resists) on ultraflat glass or semiconductor surfaces. Significant challenges exist in adapting these methods for new emerging applications and areas of research which require patterning of unusual systems and materials (*e.g.* those in biotechnology, plastic electronics, etc.), structures with nanometer dimensions (*i.e.* below 50-100 nm), large areas in a single step (*i.e.* larger than a few square centimeters) or non-planar (*i.e.* rough or curved) surfaces. These established techniques also have the disadvantage that they involve high capital and operational costs. As a result, some of the oldest and conceptually simplest forms of lithography – embossing, molding, stamping, writing, etc. – are now being re-examined for their potential to serve as the basis for nanofabrication techniques that can avoid these limitations.[1] Considerable progress has been made in the last few years, mainly by combining these approaches or variants of them with new materials, chemistries and processing techniques. This chapter highlights some recent advances in high resolution printing methods, in which a 'stamp' forms a pattern of 'ink' on a surface that it contacts. It focuses on approaches whose capabilities, level of development and demonstrated applications indicate a strong potential for widespread use, especially in areas where conventional methods are unsuitable.

Contact printing involves the use of an element with surface relief (*i.e.* the 'stamp') for transferring material applied to its surface (*i.e.* the 'ink') to locations on a substrate that it

contacts. The printing press, which represents one of the earliest manufacturable implementations of this approach, was due to Gutenberg and first appeared in the 15th century. The general approach has been since used almost exclusively for producing printed text or images with features that are one hundred microns or larger in their minimum dimension. The resolution is determined by the nature of the ink and its interaction with the stamp and/or substrate, the resolution of the stamp, and the processing conditions that are used for printing or for converting the pattern of ink into a pattern of functional material. This chapter focuses on (i) printing techniques that are capable of micron and nanometer resolution and (ii) their use for fabricating key elements of active electronic or optical devices and subsystems. It begins with an overview of some methods for fabricating high resolution stamps. It then illustrates two different ways that these stamps can be used to print patterns of functional materials. Applications that highlight the capabilities of these techniques and the performance of systems that are constructed with them are also presented.

2.2 High Resolution Stamps

The printing process can be separated into two parts: fabrication of the stamp and the use of this stamp to pattern features defined by the relief on its surface. These two processes are typically quite different, although it is possible in some cases to use patterns generated by a stamp to produce a replica of that stamp. The structure from which the stamp is derived, which is known as the 'master', can be fabricated with any technique that is capable of producing well defined structures of relief on a surface. This 'master' can then be used directly as the stamp, or it can be used to produce stamps via molding or printing procedures. It is important to note that the technique for producing the 'master' does not need to be fast or low in cost. It also does not need to possess many other characteristics that might be desirable for a given patterning task: it is used just once to produce a 'master' which is directly or indirectly used to fabricate stamps. Each one of these stamps can then be used many times for printing. In a common approach for the high resolution techniques that are the focus of this chapter, an established lithographic technique, such as one of those developed for the microelectronics industry, defines the master. Figure 2.1 schematically illustrates typical processes.

Here, photolithography patterns a thin layer of resist on a silicon wafer. Stamps are generated from this structure in one of two ways: by casting against this master or by etching the substrate with the patterned resist as a mask. In the first approach, the master itself can be used multiple times to produce many stamps, typically using a light or heat-curable prepolymer. In the second, the etched substrate serves as the stamp; additional stamps can be generated either by repeating the lithography and etching, or by using the original stamp to print replica stamps. For minimum lateral feature sizes greater than ∽1-2 microns, contact or proximity mode photolithography with a mask produced by direct write photolithography represents a

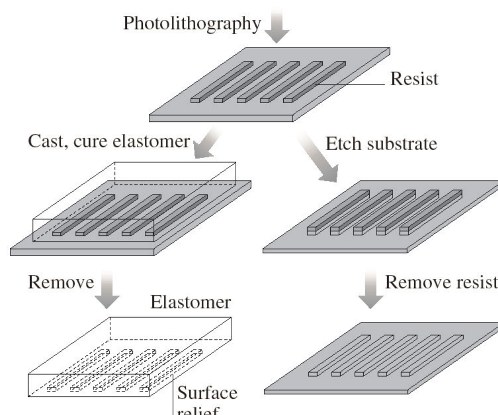


Figure 2.1: Schematic illustration of two methods for producing high resolution stamps. The first step involves patterning a thin layer of some radiation sensitive material, known as the resist, on a flat substrate, such as a silicon wafer. It is convenient to use an established technique, such as photolithography or electron beam lithography, for this purpose. This structure, known as the 'master', is converted to a stamp either by etching or by molding. In the first case, the resist acts as a mask for etching the underlying substrate. Removing the resist yields a stamp. This structure can be used directly as a stamp to print patterns or to produce additional stamps. In the molding approach, a prepolymer is cast against the relief structure formed by the patterned resist on the substrate. Curing (thermally or optically) and then peeling the resulting polymer away from the substrate yields a stamp. In this approach, many stamps can be made with a single 'master' and each stamp can be used many times.

convenient method to fabricate the master. For features smaller than ∽2 microns, several different techniques can be used,[2] including: (i) projection mode photolithography,[3] (ii) direct write electron beam (or focused ion beam) lithography,[4,5] (iii) scanning probe lithography[6–9] or (iv) laser interference lithography.[10] The first approach requires a photomask generated by some other method, such as direct write photolithography or electron beam lithography. The reduction (typically 4x) provided by the projection optics relaxes the resolution requirements on the mask and enables features as small as ∽90 nm when deep ultraviolet radiation and phase shifting masks are used. The costs for these systems are, however, very high and their availability for general research purposes is limited. The second method is flexible in the geometry of patterns that can be produced and the writing systems are highly developed: 30-50 nm features can be achieved with commercial systems,[11] and < 10 nm features are possible with research tools, as first demonstrated more than 25 years ago by Broers *et al*.[12] The main drawback of this method is that it is relatively slow and it is difficult to pattern large areas. Like projection mode photolithography, it can be expensive. The third method, scanning probe lithography, is quite powerful in principle, but the tools are not as well established as those for other approaches. This technique has atomic resolution, but its writing speed can be lower and the areas that can be patterned are smaller than electron beam systems. Interference lithography provides a pow-

erful, low cost tool for generating periodic arrays of features with dimensions down to 100-200 nm; smaller sizes demand ultraviolet lasers and patterns with aperiodic or non-regular features are difficult to produce.

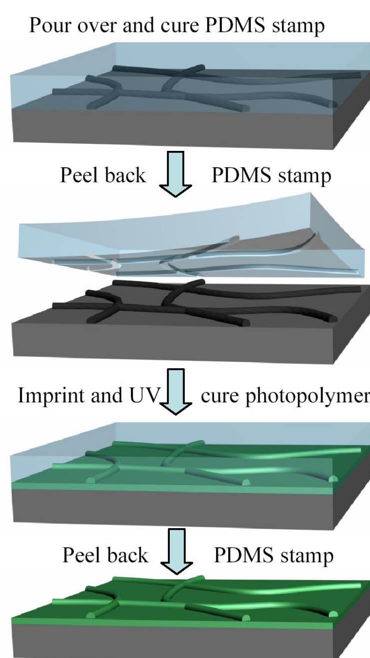


Figure 2.2: Schematically illustrates a process for examining the ultimate limits in resolution of soft lithographic methods. The approach uses a SWNT master to create a PDMS mold with nanoscale relief features. Soft nanoimprint lithography transfers the relief on the PDMS to that on the surface of an ultraviolet curable photopolymer film.

In order to evaluate the ultimate resolution limit of the soft lithography methods, masters having relief structures in the single nanometer range must be fabricated. A simple method, presented in figure 2.2, uses a sub-monolayer coverage of single walled carbon nanotubes (SWNT) grown, by established chemical vapor deposition techniques, on an ultra flat silicon wafer. The SWNT, which have diameters (*i.e.* heights and widths) in the 0.5-5 nm range, are molded on the bottom surface of a PDMS stamp generated by casting and curing against this master. Such a mold can be used to replicate the relief structure into a variety of photocurable polymers in a kind of soft nanoimprinting technique.[13–15] A single mold can be used multiple times without significant degradation. The resolution of this process can be exceedingly high: resolution approaching the single nanometer scale range (comparable to a few bond lengths in the polymer backbone) as can be seen in figure 2.3.[16] These results demonstrate extreme efficiency of these basic soft lithographic procedures for generating and using elastomeric elements. The ultimate limits are difficult to predict, due to substantial uncertainties surrounding the polymer physics and chemistry that dominates in the nanometer regime.

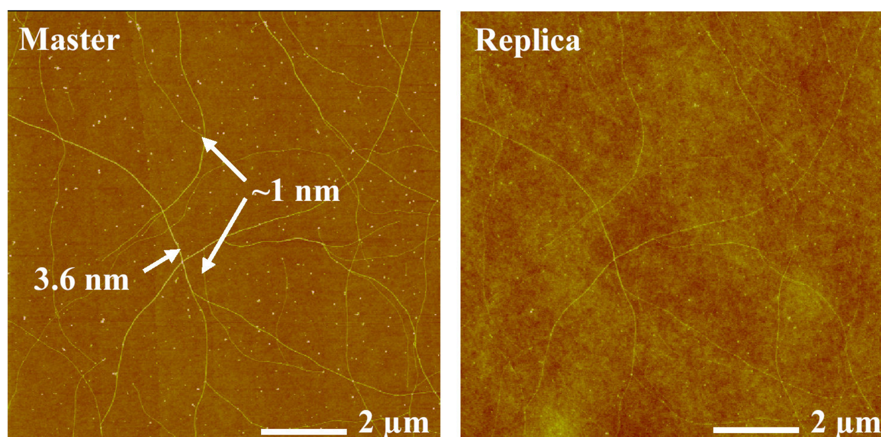


Figure 2.3: Atomic force micrographs (left picture) of a 'master' that consists of a sub-monolayer of single walled carbon nanotubes (SWNTs; diameter between 0.5 and 5 nm) grown on a SiO_2/Si wafer. The right atomic force micrograph shows a replica of the relief structures in poly(urethane). These results indicate effective operation of a PDMS stamp for soft imprint lithography at the single nanometer scale.

2.3 Microcontact Printing

Microcontact printing (μCP)[17] is one of several soft lithographic techniques – replica molding, micromolding in capillaries, microtransfer molding, near-field conformal photolithography using an elastomeric phase-shifting mask, etc. – that have been developed as alternatives to established methods for micro- and nanofabrication.[18–22] μCP use an elastomeric element (usually polydimethylsiloxane – PDMS) with high resolution features of relief as a stamp to print patterns of chemical inks. It was mainly developed for use with inks that form self-assembled monolayers (SAMs) of alkanethiolates on gold and silver. The procedure for carrying out μCP in these systems is remarkably simple: a stamp, inked with a solution of alkanethiol, is brought into contact with the surface of a substrate to transfer ink molecules to regions where the stamp and substrate contact. The resolution and effectiveness of μCP relies on conformal contact between the stamp and the surface of the substrate, rapid formation of highly ordered monolayers,[23] and autophobicity of the SAM, which effectively blocks the reactive spreading of the ink across the surface.[24] It can pattern SAMs over relatively large areas ($\backsim$up to 0.25 ft^2 have been demonstrated in prototype electronic devices) in a single impression.[25] The edge resolution of SAMs printed onto thermally evaporated gold films is on the order of 50 nm, as determined by lateral force microscopy.[26] Microcontact printing has been used with a range of different SAMs on various substrates.[18] Of these, alkanethiolates on gold, silver and palladium[27] presently give the highest resolution. In many cases, the mechanical properties of the stamp limit the sizes of

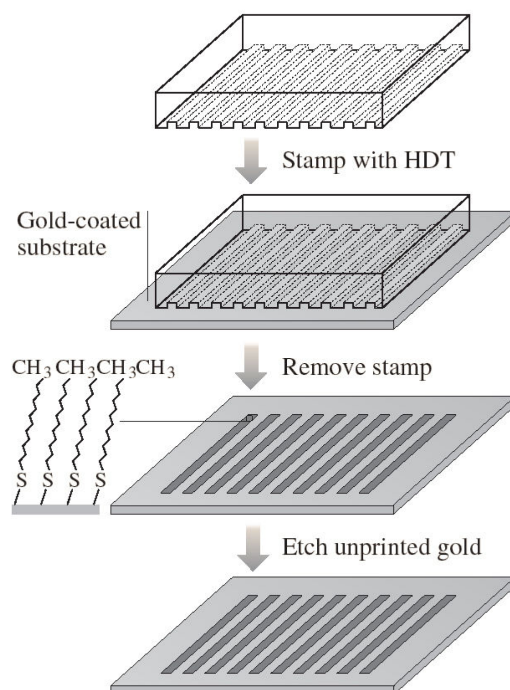


Figure 2.4: Schematic illustration of microcontact printing. The first step involves 'inking' a 'stamp' with a solution of a material that is capable of forming a self assembled monolayer (SAM) on a substrate that will be printed. In the case illustrated here, the ink is a millimolar concentration of hexadecanethiol (HDT) in ethanol. Directly applying the ink to the surface of the stamp with a pipette prepares the stamp for printing. Blowing the surface of the stamp dry and contacting it to a substrate delivers the ink to areas where the stamp contacts the substrate. The substrate consists of a thin layer of Au on a flat support. Removing the stamp after a few seconds of contact leaves a patterned SAM of HDT on the surface of the Au film. The printed SAM can act as a resist for the aqueous based wet etching of the exposed regions of the Au. The resulting pattern of conducting gold that can be used to build devices of various types.

the smallest features that can be achieved: the most commonly used elastomer (Sylgard 184, Dow Corning) has a low modulus which can lead to mechanical collapse or sagging for features of relief with aspect ratios greater than $\backsim$2 or less than $\backsim$0.05. Stamps fabricated with high modulus elastomers avoid some of these problems.[28,29] Conventional stamps also are susceptible to in-plane mechanical strains that can cause distortions in the printed patterns. Composite stamps that use thin elastomer layers on stiff supports are effective at minimizing this source of distortion.[30] Methods for printing that avoid direct mechanical manipulation of the stamp can reduce distortions with conventional and composite stamps.[25] This approach has proven to be effective in large area flexible circuit applications that require accurate multilevel registration.

The patterned SAM can be used either as a resist in selective wet etching or as a template in

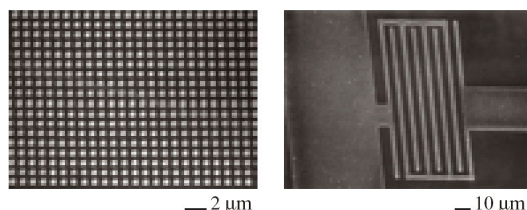


Figure 2.5: Scanning electron micrographs of typical structures formed by microcontact printing a self-assembled monolayer ink of hexadecanethiol onto a thin metal film followed by etching of the unprinted areas of the film. The left frame shows an array of Au (20 nm thick) dots with ∽500 nm diameters. The right frame shows a printed structure of Ag (100 nm thick) in the geometry of interdigitated source/drain electrodes for a transistor in a simple inverter circuit. The edge resolution of patterns that can be easily achieved with microcontact printing is ∽50-100 nm.

selective deposition to form structures of a variety of materials: metals, silicon, liquids, organic polymers, and even biological species. Figure 2.4 schematically illustrates the use of μCP and wet etching to pattern a thin film of Au. Figure 2.5 shows SEM images of nanostructures of gold (20 nm thick, thermally evaporated with a 2.5 nm layer of Ti as an adhesion promoter) and silver (∽100 nm thick formed by electroless deposition using commercially available plating baths)[31] that were fabricated using this approach. In the first and second examples, the 'masters' for the stamps consisted of photoresist patterned on silicon wafers with projection and contact mode photolithography respectively. Placing these masters in a dessicator for ∽1 h with a few drops of tridecafluoro-1,1,2,2-tetrahydrooctyl-1-trichlorosilane forms a silane monolayer on the exposed native oxide of the silicon. This monolayer prevents adhesion of the master to PDMS (Sylgard 184) that is cast and cured from a 10:1 mixture of prepolymer and curing agent. Placing a few drops of a ∽1 mM solution of hexadecanethiol (HDT) in ethanol on the surface of the stamps, and then blowing them dry with a stream of nitrogen prepares them for printing. Contacting the metal film for a few seconds with the stamp produces a patterned self-assembled monolayer (SAM) of HDT. An aqueous etchant (1 mM $K_4Fe(CN)_6$, 10 mM $K_3Fe(CN)_6$ and 0.1 M $Na_2S_2O_3$) removes the unprinted regions of the silver.[32] A similar solution (1 mM $K_4Fe(CN)_6$, 10 mM $K_3Fe(CN)_6$, 1.0 M KOH and 0.1 M $Na_2S_2O_3$) can be used for etching the bare gold.[33] The results of Figure 2.5 show that the roughness on the edges of the patterns is ∽50-100 nm. The resolution is determined by the grain size of the metal films, the isotropic etching process, slight reactive spreading of the inks and edge disorder in the patterned SAMs.

The structures of Figure 2.5 were formed on the flat surfaces of silicon wafers (left image) and glass slides (right image). An attractive feature of μCP and certain other contact printing techniques is their ability to pattern features with high resolution on highly curved or rough surfaces.[22,34,35] This type of patterning task is difficult or impossible to accomplish with photolithography due to its limited depth of focus and the difficulty in casting uniform films of photoresist on non-flat surfaces. Figure 2.6 shows, as an example, a straightforward approach

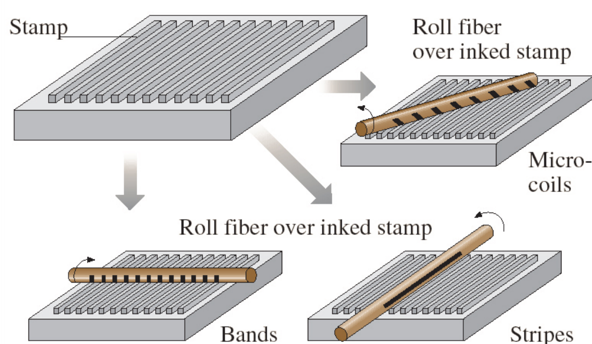


Figure 2.6: Schematic illustration of a simple method to print lines on the surfaces of optical fibers. Rolling a fiber over the inked stamp prints a pattern onto the fiber surface. Depending on the orientation of the fiber axis with the line stamp illustrated here, it is possible, in a single rotation of the fiber, to produce a continuous microcoil, or arrays of bands or stripes.

for high resolution printing on the highly curved surfaces of optical fibers. Here, simply rolling the fiber over an inked stamp prints a pattern on the entire outer surface of the fiber. Simple staging systems allow alignment of features to the fiber axis; they also ensure registration of the pattern from one side of the fiber to the other.[20]

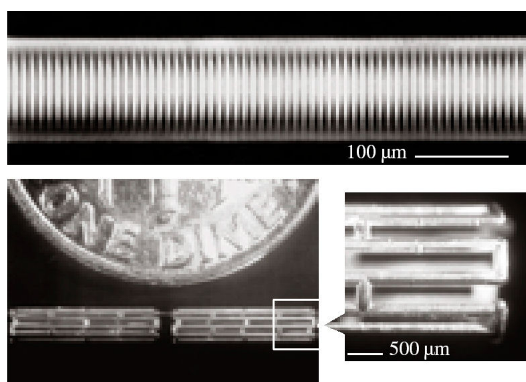


Figure 2.7: Optical micrographs of some three dimensional microstructures formed by microcontact printing on curved surfaces. The top frame shows an array of 3 micron lines of Au (20 nm) / Ti (1.5 nm) printed onto the surface of an optical fiber. This type of structure can be used as an integrated photomask for producing mode-coupling gratings in the core of the fiber. The bottom frames show a free standing metallic microstructure formed by (i) microcontact printing and etching a thin (100 nm thick) film of Ag on the surface of a glass microcapillary tube, (ii) electroplating the Ag to increase its thickness (to tens of microns) and (iii) etching away the glass microcapillary with concentrated hydrofluoric acid. The structure shown here has the geometry and mechanical properties of an intravascular stent, which is a biomedical device commonly used in balloon angioplasty.

Figure 2.7 shows 3 micron wide lines and spaces printed onto the surface of a single mode optical fiber (diameter 125 μm). The bottom frame shows a free standing metallic structure with the geometry and mechanical properties of an intravascular stent, which is a biomedical device that is commonly used in balloon angioplasty procedures. In this latter case μCP followed by electroplating generated the Ag microstructure on a sacrificial glass cylinder that was subsequently etched away with concentrated hydrofluoric acid.[36] Other examples of microcontact printing on non-flat surfaces (*i.e.* low cost plastic sheets and optical ridge waveguides) appear in the applications section of this chapter.

2.4 2D and 3D Dimensional Nanofabrication with Conformable Photomasks

PDMS rubber stamps can be used as soft photomasks since they are transparent to ultraviolet (UV) light with wavelengths greater than 300 nm. A first method, known as near field phase shift lithography involves exposure of a thin (*i.e.* $\lesssim$ micrometer) photoresist layer to UV light that passes through an elastomeric phase mask while the mask is in conformal contact with the resist.[37,38]

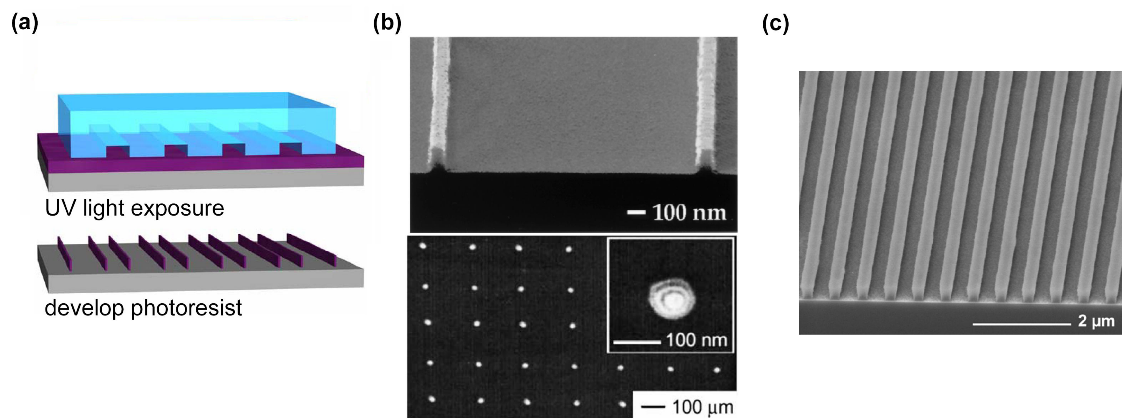


Figure 2.8: Part **(a)** shows a schematic illustration of the procedures for laminating a PDMS stamp on a relatively thin ($\lesssim$ micrometer) photoresist and generating patterns with nanometer scale after UV exposure. Part **(b)** shows the photoresist lines and dots patterned with one and two exposures, respectively. Part **(c)** shows dense photoresist lines and spaces formed when the stamp relief structure periodicity is close to the wavelength of the UV light ($\backsim$365 nm) used for exposure. In this special case, the stamp acts as an amplitude mask and produces a pattern in photoresist that has a one to one correspondence with the relief features on the stamp.

Figure 2.8a schematically illustrates the method. This approach requires only a phase mask and a simple handheld UV lamp to generate structures with dimensions as small as 50 nm over

large areas (limited by the size of the molded stamp).[39] By carefully choosing the height of the relief features in the master, a sharp minimum appears in the intensity of light at the step edges of relief (when the phase is modulated by π). Developing away the exposed regions of the resist (when a positive resist is used) yields line patterns at the edges of the relief features mask.

Figure 2.8b shows high resolution scanning micrographs of narrow line and dot patterns obtained by one or two exposures in this manner.[40] If the distance between the edges of the stamp relief features is reduced to a value close to the light wavelength, the two nulls in the near field intensity of the light add together. The transparent stamp then can serve as a sub-wavelength amplitude type photomask such that patterns molded in the stamps are reproduced in the photoresist layer in a one to one correspondence. Figure 2.8c illustrates this capability with 300 nm lines and spaces in a photoresist layer generated with a stamp that has similar features of relief.

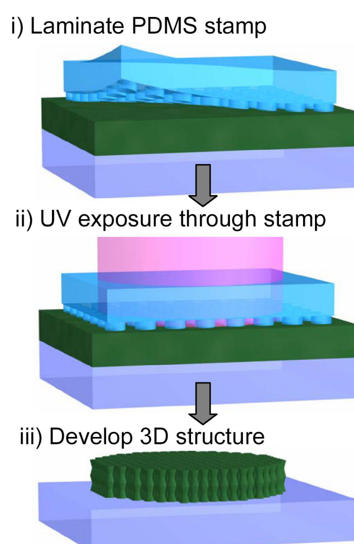


Figure 2.9: Schematic illustration of the process for fabricating 3D periodic nanostructures using the pattern of intensity formed by passage of light through a PDMS phase mask with sub-wavelength features of relief. **(i)** The stamp is first brought into intimate contact with the surface of a substrate coated with a relatively thick (several micrometers) transparent layer of a photopolymer. **(ii)** A laser beam or a regular UV mercury lamp source exposes this polymer through the photomask. **(iii)** The mask is peeled away and the unexposed regions of the photopolymer are removed by a developing step to create 3D polymer nanostructures.

As light propagates away from the surfaces of masks of this type, the intensity varies with position not only in the plane of the mask but also perpendicular to it. In the case of a mask with a grating geometry, this phenomenon is known as the Talbot effect. With thick transparent photoresists, one can exploit this effect to generate complex three dimensional nanostructures.[41] Figure 2.9 schematically illustrates the method when a coherent laser beam source is used for

exposure. The variation of the intensity can be accurately predicted using a coupled wave or finite element analysis.

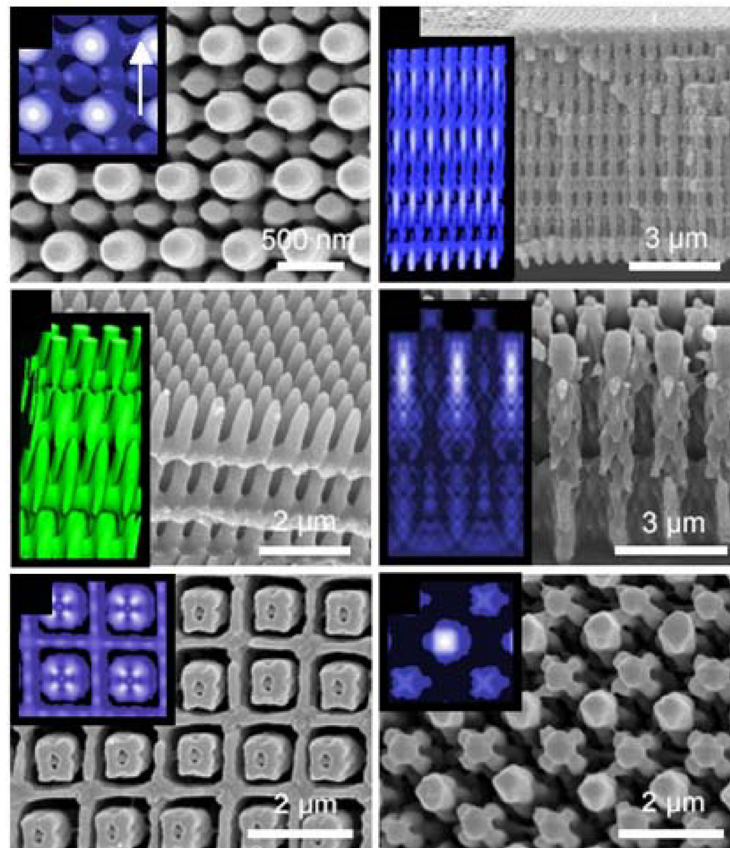


Figure 2.10: Scanning electron micrographs of representative 3D structures generated using a soft photomask element. The top left inset images show the computed intensity models obtained from the addition of the intensity of the diffracted light beams. The precise fit between the experimental results and the mathematical models is remarkable.

Figure 2.10 shows various high resolution scanning electron micrographs of complex three dimensional periodic structures generated using this method. Supercritical drying during the developing step avoids the destructive effects of surface tension on these fragile structures. These fine 3D structures have been successfully incorporated into a variety of microfluidic systems for filtering, mixing and other applications.

2.5 Nanotransfer Printing

Nanotransfer printing (nTP) is a more recent high resolution printing technique which uses surface chemistries as interfacial 'glues' and 'release' layers (rather than 'inks' as in μCP) to control the transfer of solid material layers from relief features on a stamp to a substrate.[42–44] This approach is purely additive (*i.e.* material is only deposited in locations where it is needed) and it can generate complex patterns of single or multiple layers of materials with nanometer resolution over large areas in a single process step. It does not suffer from surface diffusion or edge disorder in the patterned 'inks' of μCP nor does it require post-printing etching or deposition steps to produce structures of functional materials. The method involves four components: (i) a stamp (rigid, flexible, or elastomeric) with relief features in the geometry of the desired pattern, (ii) a method for depositing a thin layer of solid material onto the raised features of this stamp, (iii) a means for bringing the stamp into intimate physical contact with a substrate and (iv) surface chemistries that prevent adhesion of the deposited material to the stamp and promote its strong adhesion to the substrate. nTP has been demonstrated with SAMs and other surface chemistries for printing onto flexible and rigid substrates with hard inorganic and soft polymer stamps. Figure 2.11 presents a set of procedures for using nTP to pattern a thin metal bilayer of Au/Ti with a surface transfer chemistry that relies on a dehydration reaction.[42] The process begins with fabrication of a suitable stamp. Elastomeric stamps can be built using the same casting and curing procedures described for μCP. Rigid stamps can be fabricated by (i) patterning resist (*e.g.* electron beam resist or photoresist) on a substrate (*e.g.* Si or GaAs), (ii) etching the exposed regions of the substrate with an anisotropic reactive ion etch and (iii) removing the resist, as illustrated in Figure 2.1. For both types of stamps, careful control of the lithography and the etching steps yields features of relief with nearly vertical or slightly re-entrant sidewalls. The stamps typically have depths of relief > 0.2 μm for patterning metal films with thicknesses < 50 nm.

Electron beam evaporation of Au (20 nm; 1 nm/s) and Ti (5 nm; 0.3 nm/s) generates uniform metal bilayers on the surfaces of the stamp. A vertical, collimated flux of metal from the source ensures uniform deposition only on the raised and recessed regions of relief. The gold adheres poorly to the surfaces of stamps made of GaAs, PDMS, glass or Si. In the process of Figure 2.11, a fluorinated silane monolayer acts to reduce further the adhesion when a Si stamp (with native oxide) is used. The Ti layer serves two purposes: (i) it promotes adhesion between the Au layer and the substrate after pattern transfer, and (ii) it readily forms a $\backsim$3 nm oxide layer at ambient conditions which provides a surface where the dehydration reaction can take place. Exposing the titanium oxide (TiO_x) surface to an oxygen plasma breaks bridging oxygen bonds, thus creating defect sites where water molecules can adsorb. The result is a titanium oxide surface with some fractional coverage of hydroxyl (-OH) groups (titanol).

In the case of Figure 2.11, the substrate is a thin film of PDMS (10-50 μm thick) cast onto a sheet of poly(ethylene terephthalate) (PET; 175 μm thick). Exposing the PDMS to an oxygen

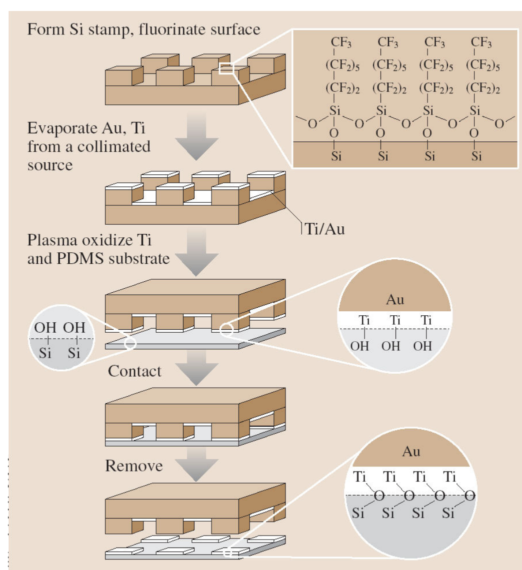


Figure 2.11: Schematic illustration of nanotransfer printing procedures. Here, interfacial dehydration chemistries control the transfer of a thin metal film from a hard inorganic stamp to a conformable elastomeric substrate (thin film of polydimethylsiloxane (PDMS) on a plastic sheet). The process begins with fabrication of a silicon stamp (by conventional lithography and etching) followed by surface functionalization of the native oxide with a fluorinated silane monolayer. This layer ensures poor adhesion between the stamp and a bilayer metal film (Au and Ti) deposited by electron beam evaporation. A collimated flux of metal oriented perpendicular to the surface of the stamp avoids deposition on the sidewalls of relief. Exposing the surface Ti layer to an oxygen plasma produces titanol groups. A similar exposure for the PDMS produces silanol groups. Contacting the metal coated stamp to the PDMS results in a dehydration reaction that links the metal to the PDMS. Removing the stamp leaves a pattern of metal in the geometry of the relief features.

plasma produces surface (-OH) groups (silanol). Placing the plasma oxidized, Au/Ti-coated stamp on top of these substrates leads to intimate, conformal contact between the raised regions of the stamp and the substrate, without the application of any external pressure. (The soft, conformable PDMS is important in this regard.) It is likely that a dehydration reaction takes place at the (-OH)-bearing interfaces during contact; this reaction results in permanent Ti-O-Si bonds that produce strong adhesion between the two surfaces. Peeling the substrate and stamp apart transfers the Au/Ti bilayer from the raised regions of stamp (to which the metal has extremely poor adhesion) to the substrate. Complete pattern-transfer from an elastomeric stamp to a thin elastomeric substrate occurs readily at room temperature in open air with contact times of less than 15 seconds. When a rigid stamp is employed, slight heating is needed to induce transfer. While the origin of this difference is unclear, it may reflect the comparatively poor contact when rigid stamps are used; similar differences are also observed in cold welding of gold films.[45]

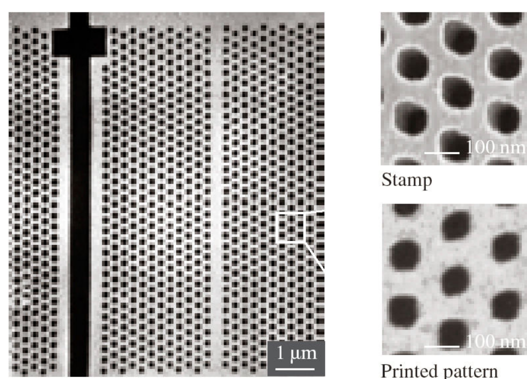


Figure 2.12: Scanning electron micrograph (SEM) of a pattern produced by nanotransfer printing. The structure consists of a bilayer of Au(20 nm)/Ti (1 nm) (white) in the geometry of a photonic bandgap waveguide printed onto a thin layer of polydimethylsiloxane on a sheet of plastic (black). Electron beam lithography and etching of a GaAs wafer produced the stamp that was used in this case. The transfer chemistry relied on condensation reactions between titanol groups on the surface of the Ti and silanol groups on the surface of the PDMS. The frames on the right show SEMs of the Au/Ti coated stamp (top) before printing and on the substrate (bottom) after printing. The electron beam lithography and etching used to fabricate the stamp limit the minimum feature size (∽70 nm) and the edge resolution (∽5-10 nm) of this pattern.

Figure 2.12 shows scanning electron micrographs of a pattern produced using a GaAs stamp generated by electron beam lithography and etching. The frames on the right show images of the metal coated stamp before printing (top) and the transferred pattern (bottom). The resolution appears to be limited only by the resolution of the stamp itself, and perhaps by the grain size of the metal films. Although the accuracy in multilevel registration that is possible with nTP has not yet been quantified, its performance is likely similar to that of embossing techniques when rigid stamps are used.[46]

A wide range of surface chemistries can be used for the transfer. SAMs are particularly attractive due to their chemical flexibility. Figure 2.13 illustrates the use of a thiol terminated SAM and nTP for forming patterns of Au on a silicon wafer.[43] Here, the vapor phase co-condensation of the methoxy groups of molecules of 3-mercaptopropyltrimethoxysilane (MPTMS) with the -OH terminated surface of the wafer produces a SAM of MPTMS with exposed thiol (-SH) groups. PDMS stamps can be prepared for printing on this surface by coating them with a thin film (∽15 nm) of Au using conditions (thermal evaporation 1.0 nm/s; ∽10^{-7} torr base pressure) that yield optically smooth, uniform films without the buckling that has been observed in the past with similar systems.[47] Nanocracking that sometimes occurs in the films deposited in this way can be reduced or eliminated by evaporating a small amount of Ti onto the PDMS before Au deposition and/or by exposing the PDMS surface briefly to an oxygen plasma. Bringing this coated stamp into contact with the MPTMS SAM leads to

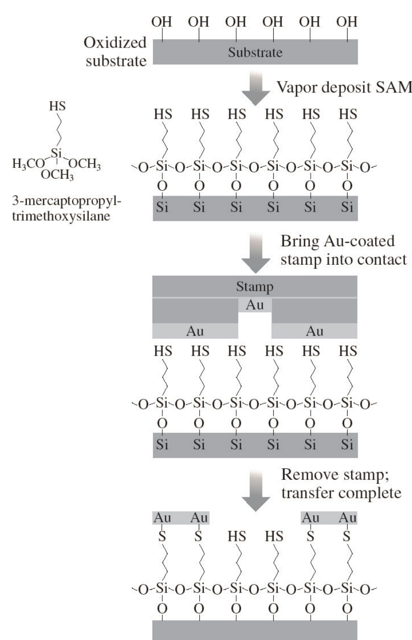


Figure 2.13: Schematic illustration of steps for nanotransfer printing a pattern of a thin layer of Au onto a silicon wafer using a self-assembled monolayer (SAM) surface chemistry. Plasma oxidizing the surface of the wafer generates -OH groups. Solution or vapor phase exposure of the wafer to 3-mercaptopropyl-trimethoxysilane yields a SAM with exposed thiol groups. Contacting an Au-coated stamp to this surface produces thiol linkages that bond the gold to the substrate. Removing the stamp completes the transfer printing process.

the formation of sulfur-gold bonds in the regions of contact. Removing the stamp after a few seconds efficiently transfers the gold from the raised regions of the stamp (Au does not adhere to the PDMS) to the substrate. Covalent bonding of the SAM 'glue' to both the substrate and the gold leads to good adhesion of the printed patterns: they easily pass Scotch tape adhesion tests. Similar results can be obtained with other substrates containing surface -OH groups. For example, Au patterns can be printed onto ∽250 μm thick sheets of poly(ethylene terephthalate) (PET) by first spin casting and curing (130 ^{o}C for 24 h) a thin film of an organosilsesquioxane on the PET. Exposing the cured film (∽1 μm thick) to an oxygen plasma then air produces the necessary surface (-OH) groups.

Figure 2.14 shows some optical micrographs of typical printed patterns in this case.[43] Similar surface chemistries can guide transfer to other substrates. Alkanedithiols, for example, are useful for printing Au onto GaAs wafers.[44] Immersing these substrates (freshly etched with 37% HCl for ∽2 min. to remove the surface oxide) in a 0.05 M solution of 1,8-octanedithiol in ethanol for 3 h produces a monolayer of dithiol on the surface. Although the chemistry of this system is not completely clear, it is generally believed that the thiol end groups chemically bond

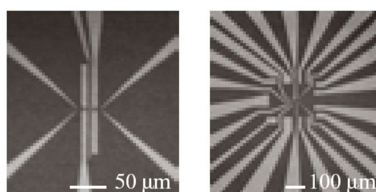


Figure 2.14: Optical micrographs of patterns of Au (15 nm thick) formed on plastic (left frame) and silicon (right frame) substrates with nanotransfer printing. The transfer chemistries in both cases rely on self-assembled monolayers with exposed thiol groups. The minimum feature sizes and the edge resolution are both limited by the photolithography used to fabricate the stamps.

to the surface. Surface spectroscopy suggests the formation of Ga-S and As-S bonds. Contacting an Au-coated PDMS stamp with the treated substrate causes the exposed thiol endgroups to react with Au in the regions of contact. This reaction produces permanent Au-S bonds at the stamp/substrate interface (see insets in Figure 2.4 for idealized chemical reaction schemes).

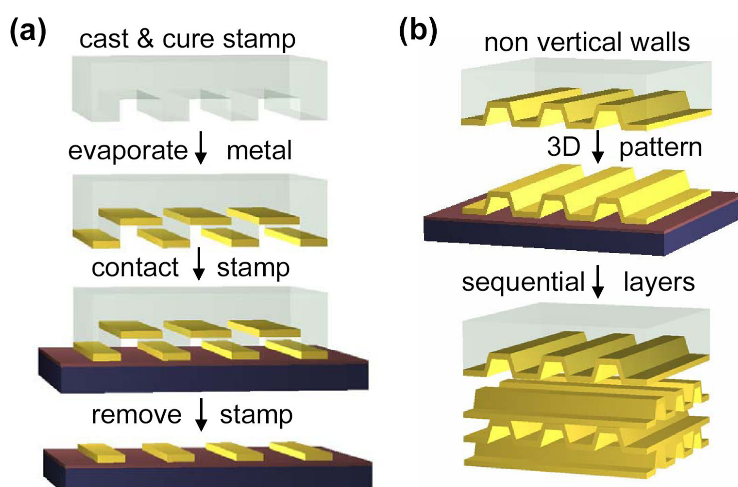


Figure 2.15: Schematic illustration of the nanotransfer printing (nTP) process for fabricating high resolution 2D or 3D patterns of thin metals. Part **(a)** schematic schematically illustrates the process for generating 2D metal patterns. A metal coated stamp (formed using a collimated electron beam evaporator) is brought into intimate contact with the surface of a substrate. Chemical bonding or surface energy differences enable the transfer of the metal from the raised area of the stamp to the substrate. Part **(b)** illustrates schematically the process for generating continuous 3D structures when the stamp relief side walls are not vertical. Successive cold welding of gold films on top of each other yields complex multilayers structures.

Figure 2.15 schematically illustrates two different nTP procedures that enable the transfer of discontinuous or continuous 3D metal patterns (depending on the side wall orientation of the stamp relief patterns).[48]

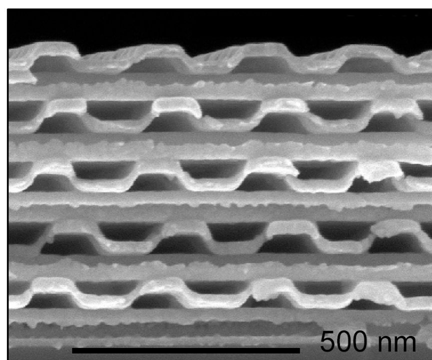


Figure 2.16: Scanning electron micrographs of three dimensional metal structures obtained by nano-transfer printing gold metal films. Part **(a)** shows closed gold nano-capsules. Part **(b)** shows free-standing L structures obtained using a stamp coated with a steeply angled flux of metal. Part **(c)** shows a multilayer 3D structure obtained by the successive transfer and cold welding of continuous gold nano-corrugated films.

The integrity of the nanotransfer printed free standing 3D metal structures is remarkable (see Figure 2.16) but depends critically on the careful optimization of the metal evaporation conditions and stamp & substrate surface chemistries as we will see in the following chapter. Similar metal transfer techniques have been developed in other research groups.[49,50]

2.6 Applications: Unconventional Electronic Systems

Although conventional patterning techniques, such as photolithography or electron beam lithography, have the required resolution, they are not appropriate because they are expensive and generally require multiple processing steps with resists, solvents and developers that can be difficult to use with organic active materials and plastic substrates. Microcontact and nanotransfer printing are both particularly well suited for this application. They can be combined and matched with other techniques, such as ink jet or screen printing, to form a complete system for patterning all layers in practical plastic electronic devices.[51] We have focused our efforts partly on unusual electronic systems such as flexible plastic circuits and devices that rely on electrodes patterned on curved objects such as microcapillaries and optical fibers. We have also explored photonic systems such as distributed feedback structures for lasers and other integrated optical elements that demand sub-micron features. The sections below highlight several examples in each of these areas.

A relatively new direction in electronics research seeks to establish low cost plastic materials, substrates and printing techniques for large area flexible electronic devices, such as paper-like displays. These types of novel devices can complement those (*e.g.* high density memories,

high speed microprocessors, etc.) that are well suited to existing inorganic (*e.g.* silicon) electronics technologies. High resolution patterning methods for defining the separation between the source and drain electrodes (*i.e.* channel length) of transistors in these plastic circuits are particularly important because this dimension determines current output and other important characteristics.[52]

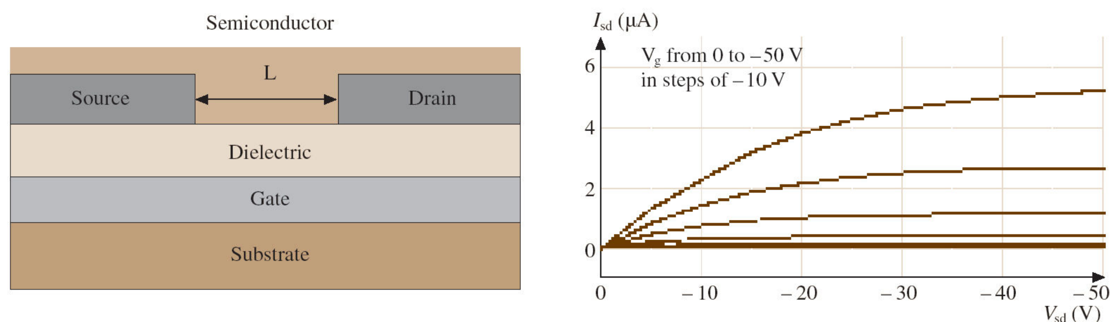


Figure 2.17: Schematic cross sectional view (left) and electrical performance (right) of an organic thin film transistor with microcontact printed source and drain electrodes. The structure consists of a substrate (PET), a gate electrode (indium tin oxide), a gate dielectric (spin cast layer of organosilsesquioxane), source and drain electrodes (20 nm Au and 1.5 nm Ti), and a layer of the organic semiconductor pentacene. The electrical properties of this device are comparable to or better than those that use pentacene with photolithographically defined source/drain electrodes and inorganic dielectrics, gates and substrates.

Figure 2.17 schematically illustrates a cross sectional view of a typical organic transistor. The frame on the right shows the electrical switching characteristics of a device that uses source/drain electrodes of Au patterned by μCP, a dielectric layer of an organosilsesquioxane, a gate of indium tin oxide (ITO) and a PET substrate. The effective semiconductor mobility extracted from these data is comparable to those measured in devices that use the same semiconductor (pentacene in this case) with inorganic substrates and dielectrics, and gold source/drain electrodes defined by photolithography. Our recent work[31,53] with μCP in the area of plastic electronics demonstrates: (i) methods for using cylindrical ‘roller’ stamps mounted on fixed axles for printing, in a continuous reel-to-reel fashion, high resolution source/drain electrodes in ultrathin gold and in silver deposited from solution at room temperature using electroless deposition, (ii) techniques for performing registration and alignment of the printed features with other elements of a circuit, over large areas, (iii) strategies for achieving densities of defects that are as good as those observed with photolithography, when the patterning is performed outside of cleanroom facilities, (iv) methods for removing the printed SAMs to allow good electrical contact of the electrodes with organic semiconductors deposited on top of them, and (v) materials and fabrication sequences that can efficiently exploit these printed electrodes for working organic TFTs in large scale circuits.

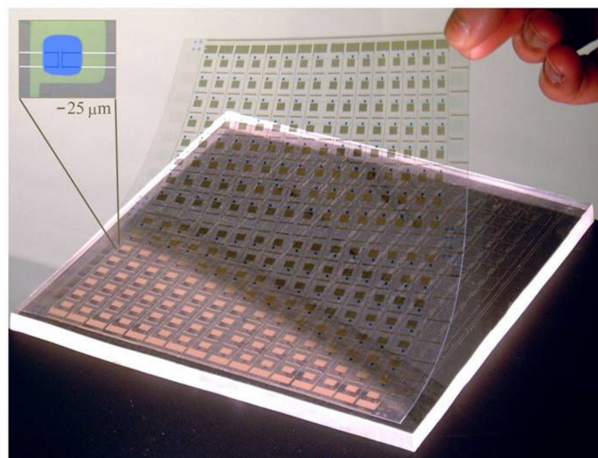


Figure 2.18: Image of a flexible plastic active matrix backplane circuit whose finest features (transistor source/drain electrodes and related interconnects) are patterned by microcontact printing. The circuit rests partly on the elastomeric stamp that was used for printing. The circuit consists of a square array of interconnected organic transistors, each of which acts locally as a voltage controlled switch to control the color of an element in the display. The inset shows an optical micrograph of one of the transistors.

Figure 2.18 provides an image of a large area plastic circuit with critical features defined by μCP. This circuit is a flexible active matrix backplane for a display. It consists of a square array of interconnected transistors, each of which serves as a switching element that controls the color of a display pixel.[25,54] The transistors themselves have the layout illustrated in Figure 2.17, and they use similar materials. The semiconductor in this image is blue (pentacene), the source/drain level is Au; the ITO appears green in the optical micrograph in the inset. Part of the circuit rests on the stamp that was used for μCP. The smallest features are the source and drain electrodes ($\backsim$15 μm lines), the interconnecting lines ($\backsim$15 μm lines) and the channel length of the transistor ($\backsim$15 μm). This circuit incorporates 5 layers of material patterned with good registration of the source/drain, gate and semiconductor levels.

The simple approach illustrated in Figure 2.19 to perform the printing.[25] Just before use, the surface of the stamp is cleaned using a conventional adhesive roller lint-remover; this procedure removes dust from the stamp in a convenient manner that does not contaminate or damage its surface. Inking the stamp and placing it face up on a flat surface prepares it for printing. Matching crosshair alignment marks on the corners of one edge of the stamp with those patterned in the ITO brings the substrate into registration with the stamp. During this alignment, features on the stamp are viewed directly through the semi-transparent substrate. By bending the PET sheet, contact with the stamp is initiated on the edge of the substrate that contains the crosshair marks. Gradually unbending the sheet allows contact to progress across the rest of the surface. This procedure for printing is attractive because it avoids distortions that can arise

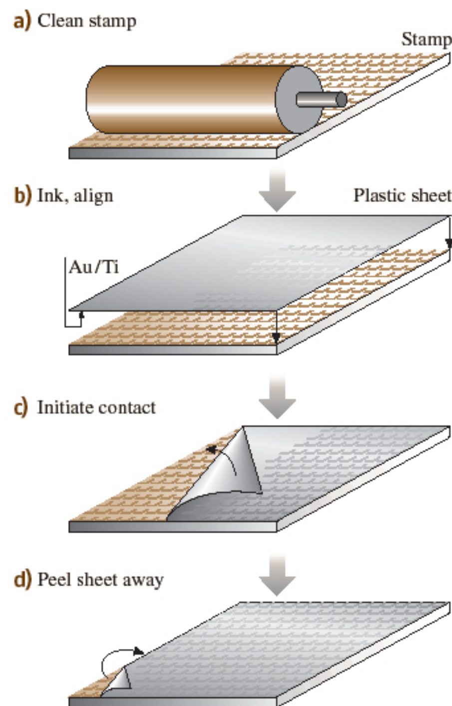


Figure 2.19: Schematic illustration of fabrication steps for microcontact printing over large areas onto plastic sheets. The process begins with cleaning the stamp using a conventional adhesive roller lint remover. This procedure effectively removes dust particles. To minimize distortions, the stamp rests face up on a flat surface and it is not manipulated directly during the printing. Alignment and registration are achieved with alignment marks on one side of the substrate and the stamp. By bending the plastic sheet, contact is initiated on one side of the stamp; the contact line is then allowed to progress gradually across the stamp. This approach avoids formation of air bubbles that can frustrate good contact. After the substrate is in contact with the stamp for a few seconds, the plastic substrate is separated from the stamp by peeling it away beginning in one corner. Good registration (maximum cumulative distortions less than 50 microns over an area of 0.25 square feet) and low density of defects can be achieved with this simple approach. It is also well suited for use with rigid composite stamps designed to reduce even further the level of distortions.

when directly manipulating the flexible rubber stamp. It also minimizes the number and size of trapped air pockets can form between the stamp and substrate. Careful measurements performed after etching the unprinted areas of the gold show that, over the entire 6”×6” area of the circuit, (i) the overall alignment accuracy for positioning the stamp relative to the substrate (*i.e.* the offset of the center of the distribution of registration errors) is ∽50-100 μm, even with the simple approach used here, and (ii) the distortions in the positions of features in the source/drain level, when referenced to the gate level, can be as small as ∽50 μm (*i.e.* the full width at half maximum of the distribution of registration errors). These distortions represent the cumulative

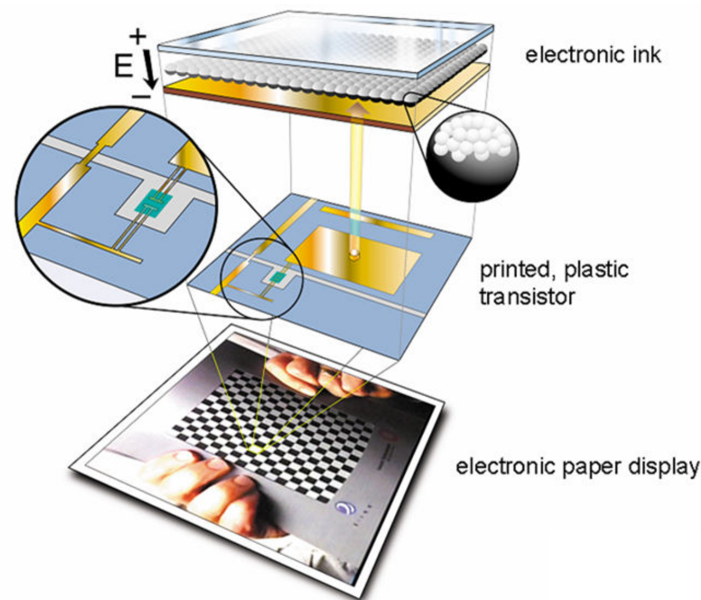


Figure 2.20: Schematic exploded view of the components of a pixel in an electronic paperlike display (bottom frame) that uses a microcontact printed flexible active matrix backplane circuit (illustration near the bottom frame). The circuit is laminated against an unpatterned thin sheet of electronic ink (top frame) that consists of a monolayer of transparent polymer microcapsules (diameter ∽100 microns). These capsules contain a heavily dyed black fluid and a suspension of charged white pigment particles (see right inset). When one of the transistors turns on, electric fields develop between an unpatterned transparent frontplane electrode (indium tin oxide) and a backplane electrode that connects to the transistor. Electrophoretic flow drives the pigment particles to the front or the back of the display, depending on the polarity of the field. This flow changes the color of the pixel, as viewed from the front of the display, from black to white or vica versa.

effects of deformations in the stamp and distortions in the gate and column electrodes that may arise during patterning and processing of the flexible PET sheet. The density of defects in the printed patterns is comparable to (or smaller than) that in resist patterned by contact mode photolithography, when both procedures are performed outside of a cleanroom facility (*i.e.* when dust is the dominant source of defects).

Figure 2.20 shows an 'exploded' view of a paperlike display that consists of a printed flexible plastic backplane circuit like the one illustrated in Figure 2.18 laminated against a thin layer of 'electronic ink'.[25,55] The 'electronic ink' is composed of a monolayer of transparent polymer microcapules that contain a suspension of charged white pigment particles suspended in a black liquid. The printed transistors in the backplane circuit act as local switches which control electric fields that drive the pigments to the front or back of the display. When the particles flow to the front of a microcapsule, it appears white; when they flow to the back, it appears black.

Figure 2.21: Electronic paperlike display showing two different images. The device consists of several hundred pixels controlled by a flexible active matrix backplane circuit formed by microcontact printing. The relatively coarse resolution of the display is not limited by material properties or by the printing techniques. Instead, it is set by practical considerations for achieving high pixel yields in the relatively uncontrolled environment of the chemistry laboratory in which the circuits were fabricated.

Figure 2.21 shows a working sheet of active matrix electronic paper that uses this design. This prototype display has several hundred pixels and an optical contrast that is both independent of viewing angle and significantly better than newsprint. The device is $\backsim$1 mm thick, it is mechanically flexible and weighs $\backsim$80% less than a conventional liquid crystal display of similar size. Although these displays have only a relatively coarse resolution, all of the processing techniques, the μCP method, the materials and the ’electronic inks’ are suitable for the large numbers of pixels that are required for high information content electronic newspapers and other systems. Like μCP, nTP is well suited to forming high resolution source/drain electrodes for plastic electronics. nTP of Au/Ti features in the geometry of the drain and source level of organic transistors and with appropriate interconnects on a thin layer of PDMS on PET yields a substrate that can be used in an unusual but powerful way for building circuits: soft, room temperature lamination of such a structure against a plastic substrate that supports the semiconductor, gate dielectric and gate levels yields a high performance circuit embedded between two plastic sheets.[42,56] Details of this lamination procedure are presented elsewhere.

The left frame of Figure 2.22 shows the current-voltage characteristics of a laminated n-channel transistor that uses the organic semiconductor copper hexadecafluorophthalocyanine (n-type) and source/drain electrodes patterned with nTP. The inset shows an optical micrograph of the printed interdigitated source/drain electrodes of this device. The right frame of Figure 2.22 shows the transfer characteristics of a laminated complementary organic inverter circuit whose electrodes and connecting lines are defined by nTP. The p-channel transistor in this circuit used pentacene for the semiconductor.[42]

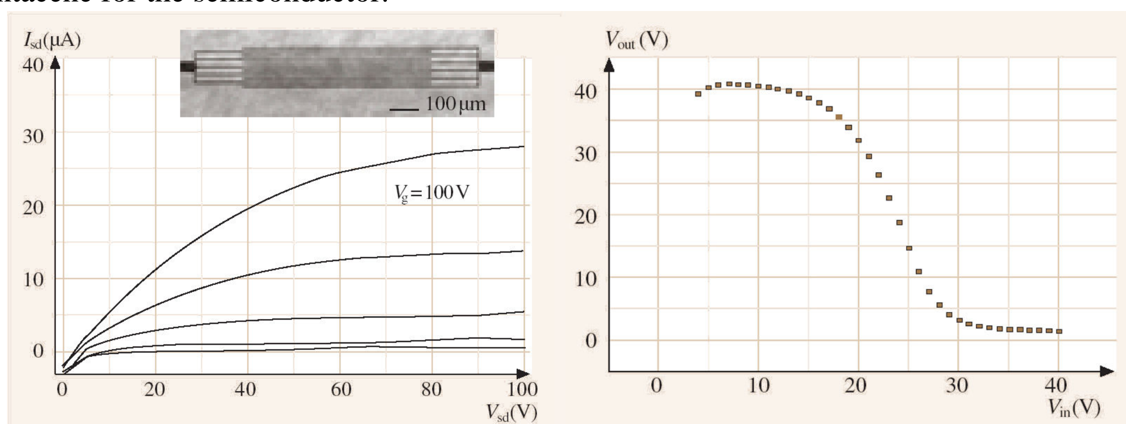


Figure 2.22: The frame on the left shows current-voltage characteristics of an n-channel transistor formed with electrodes patterned by nanotransfer printing that are laminated against a substrate that supports an organic semiconductor, a gate dielectric and a gate. The inset shows an optical micrograph of the interdigitated electrodes. The frame on the right shows the transfer characteristics of a simple CMOS inverter circuit that uses this device and a similar one for the p-channel transistor.

In addition to high resolution source/drain electrodes, it is possible to use nTP to form complex multilayer devices with electrical functionality on plastic substrates.[43] Figure 2.23 shows a metal/insulator/metal (MIM) structure of Au (50 nm), SiN_x (100nm; by plasma enhanced vapor deposition, PECVD), Ti (5 nm) and Au (50 nm) formed by transfer printing with a silicon stamp that is sequentially coated with these layers. In this case, a short reactive ion etch (with CF_4) after the second Au deposition removes the SiN_x from the sidewalls of the stamp. nTP transfers these layers in a patterned geometry to a substrate of Au(15 nm)/Ti(1 nm)-coated PDMS(50 μm)/PET(250 μm). Interfacial cold welding between the Au on the surfaces of the stamp and substrate bonds the multilayers to the substrate. Figure 2.11 illustrates the procedures, the structures (lateral dimensions of 250 μm $\times$ 250 μm, for ease of electrical probing) and their electrical characteristics. These MIM capacitors have performance similar to devices fabricated on silicon wafers by photolithography and lift-off. This example illustrates the ability of nTP to print patterns of materials whose growth conditions (high temperature SiN_x by PECVD in this case) prevent their direct deposition or processing on the substrate of interest (PET in this case). The cold welding transfer approach has also been exploited in other ways for patterning components for plastic electronics.[50,57]

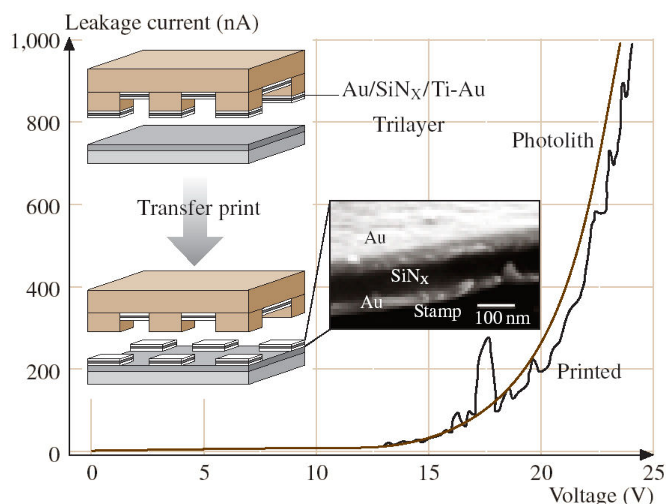


Figure 2.23: Multilayer thin film capacitor structure printed in a single step onto a plastic substrate using the nanotransfer printing technique. A multilayer of Au/SiN_x/Ti/Au was first deposited onto a silicon stamp formed by photolithography and etching. Contacting this stamp to a substrate of Au/PDMS/PET forms a cold weld that bonds the exposed Au on the stamp to the Au-coating on the substrate. Removing the stamp produces arrays of square (250 μm × 250 μm) metal/insulator/metal capacitors on the plastic support. The dashed line shows the measured current-voltage characteristics of one of these printed capacitors. The solid line corresponds to a similar structure formed on a rigid glass substrate using conventional photolithographic procedures. The characteristics are the same for these two cases. The slightly higher level of noise in the printed devices results, at least partly, from the difficulty in making good electrical contacts to structures on the flexible plastic substrate.

Another class of unusual electronic/optoelectronic device relies on circuits or circuit elements on curved surfaces. This emerging area of research was stimulated primarily by the ability of μCP to print high resolution features on fibers and cylinders. Figure 2.24 shows a conducting microcoil printed, with μCP using the approach illustrated in Figure 2.4, on a microcapillary tube. The coil serves as the excitation and detection element for high resolution proton nuclear magnetic resonance of nanoliter volumes of fluid that are housed in the bore of the microcapillary.[58] The high fill factor and other considerations lead to extremely high sensivitity with such printed coils. The bottom frame of Figure 2.24 shows the spectrum of an ∽8 nL volume of ethylbenzene. The narrow lines demonstrate the high resolution that is possible with this approach. Similar coils can be used as magnets,[59] springs[36] and electrical transformers.[60]

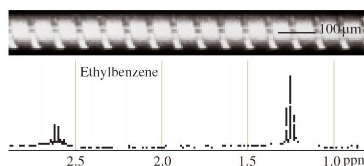


Figure 2.24: The top frame shows an optical micrograph of a continuous conducting microcoil formed by microcontact printing onto a microcapillary tube. This type of printed microcoil is well suited for excitation and detection of nuclear magnetic resonance spectra from nanoliter volumes of fluid housed in the bore of the microcapillary. The bottom frame shows a spectra trace collected from an ∽8 nL volume of ethyl benzene using a structure similar to the one shown in the top frame.

Figure 2.25 shows an optical micrograph and electrical measurements from a concentric cylindrical microtransformer that uses a microcoil printed on a microcapillary tube with a ferromagnetic wire threaded through its core. Inserting this structure into the core of a larger microcapillary that also supports a printed microcoil completes the transformer.[60] This type of device shows good coupling coefficients up to relatively high frequencies. Examples of other optoelectronic components appear in fiber optics where microfabriated on-fiber structures serve as integrated photomasks[20] and distributed thermal actuators.[22]

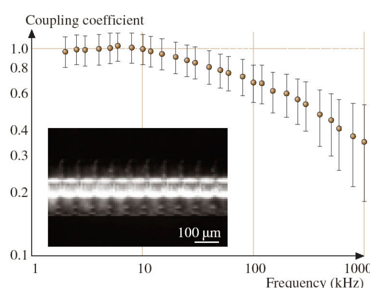


Figure 2.25: The inset shows a concentric microtransformer formed using microcoils printed onto two different microcapillary tubes. The smaller of the tubes (outer diameter 135 microns) has a ferromagnetic wire threaded through its core. The larger one (outer diameter 350 microns) has the smaller tube threaded through its core. The resulting structure is a microtransformer that shows good coupling coefficients at frequencies up to ∽1 MHz. The graph shows its performance.

2.7 Conclusions

This chapter provides an overview of various soft lithography printing techniques that are capable of micron and sub-micron resolution. It also illustrated some applications where these methods may provide attractive alternatives to more established lithographic method. The growing

interest nanoscience and nanotechnology makes crucial the development of new methods for nanofabricating the relevant test structures and devices. The simplicity of these techniques together with the interesting and subtle materials science, chemistry, and physics associated with them, make this a promising area for basic and applied study.

Chapter 3

Improved Surface Chemistries, Thin Film Deposition Techniques and Stamp Designs for Nanotransfer Printing

As we have seen in the previous chapter, nanotransfer printing (nTP) represents an additive approach for patterning thin layers of solid materials with nanometer resolution. The surface chemistries, thin film deposition techniques and stamp designs are all important for the proper operation of this method. In this chapter we will present some details concerning processing procedures and other considerations needed for patterning two and three dimensional nanostructures with low density of defects and minimal distortions.

3.1 Introduction

Lithographic techniques that use rubber stamps provide simple means to generate patterns with lateral dimensions that can be much smaller than one micron. These soft lithographic printing methods are useful for fabricating devices such as diodes,[61] photoluminescent porous silicon pixels,[62] organic light-emitting diodes[63] and thin-film transistors.[64] and a wide range of other devices in electronics and photonics, as well as biotechnology. The printed inks typically consist of soft organic materials such as proteins,[65] dendrimers, colloids or molecules that form self-assembled monolayers.[17,66] Recent work demonstrates that similar stamps can print thin solid inks (*i.e.* polymer, metal or inorganic films) of functional materials.[42,44,50,67] Such methods are purely additive in their operation. They do not suffer from loss of resolution due to etching steps or to surface spreading or vapor phase transport of the inks. One approach, referred to as nanotransfer printing, uses soft or hard stamps to print single or multiple layers of solid films.[42,43,48,49] It can form complex two or three dimensional[48] structures with minimum feature sizes well below 100 nm with edge resolution of 5-10 nm. The method has

been used to build plastic[42] and molecular electronic devices[68,69] and subwavelength photonic elements.[43] This chapter presents some improved surface chemistries, thin film deposition techniques and advanced stamp designs for high fidelity nanotransfer printing of metal films with elastomeric stamps made of poly(dimethylsiloxane) (PDMS). Some of these procedures are also important for a non-invasive electrical probing technique that uses thin metal films on PDMS elements.[56,70,71] The stamp designs are useful for a range of other soft lithographic methods. Nanotransfer printing (nTP) relies on the transfer of a solid material ink from the structured surface of a stamp to a substrate. Figure 3.1 shows representative procedures for printing thin Au patterns. The process begins with deposition of the Au coating. In the case of figure 3.1, a collimated flux of Au oriented perpendicular to the surface of a stamp forms a discontinuous coating on the raised and recessed regions. Contacting this stamp to a substrate that supports a self-assembled monolayer (SAM) designed to bond to the Au (e.g. a thiol terminated SAM) leads to strong adhesion between the Au and the substrate. Removing the stamp, to which the Au only weakly adheres, transfers the Au on the raised regions of the stamp to the substrate. This purely additive printing approach offers exceptionally high resolution for two dimensional patterning. With specially designed stamps it is possible to transfer complex three dimensional nanostructures. The printing steps can be repeated to build up patterned multilayer stacks.[48]

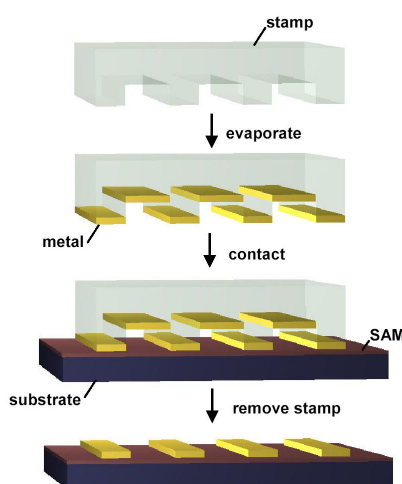


Figure 3.1: Schematic illustration of steps for nanotransfer printing. A collimated flux of material oriented perpendicular to the surface of a high resolution stamp forms a discontinuous coating. (Au is illustrated here. Other materials are possible.) Contacting this coated stamp to a substrate leads to chemical reactions at the interface between the metal and the substrate. (A self assembled monolayer (SAM) provides the necessary chemistry.) These reactions bond the metal to the substrate; removing the stamp (to which the metal only weakly adheres) transfers the metal on the raised regions of the stamp to the substrate. Continuous coatings are also possible. In this case, the transfer process yields certain classes of three dimensional structures.

3.2 Surface Chemistry and Thin Film Deposition Effects on Nanotransfer Printing.

The ability to perform nTP depends critically on processing conditions that enable robust coatings to be deposited on the stamps and to be transferred from them to substrates without damage. These challenges are significant when relatively brittle materials are printed with the types of elastomeric stamps that have been used in traditional soft lithography. Although nTP is compatible with rigid stamps, elastomeric ones are attractive because they are easy to fabricate and because they readily form intimate 'wetting' contacts with a wide range of substrates without applied pressure. It is therefore important to develop processing conditions for using these types of stamps to fabricate defect free patterns by nTP. The following focuses on printing of Au films onto either silicon wafers (with their native oxide) coated with a bilayer of Ti/Au (2nm/20nm) or onto GaAs wafers coated with a monolayer of octanedithiol. In the former case, cold welding between the freshly evaporated Au layers on the stamp and substrate guides the transfer of the metal patterns.[43,50] In the latter case, Au-S bonds facilitate transfer.[44] In both systems, contact between the stamp and substrate for a few seconds is sufficient to induce bonding. The coating and deposition conditions are chosen to ensure that the strength of adhesion between the metals and the stamps is small compared to the adhesive bonds that form to the substrate during contact.

The stamps use bilayer PDMS designs described elsewhere.[72] These stamps are placed on glass slides immediately before depositing the Au; they remain on these slides throughout the course of the printing process. Rigid backings help to eliminate damage to the coatings that can otherwise be introduced during manipulation of the stamps. Electron beam evaporation of thin Au (20 nm) onto the stamps at relatively high rates (1 nm/s) yields smooth, electrically continuous coatings that are free of the rippling observed in other work.[47] Figures 3.2a-c show field emission scanning electron micrographs (SEMs) and atomic force micrographs (AFMs) of typical patterns that result from nTP by cold welding onto a silicon substrate (similar results are obtained with the GaAs system). Although printing in this manner successfully forms high resolution patterns over large areas, figure 3.2a-c show that nanoscale cracking in the Au can occur. Imaging of coated stamps before printing (Figure 3.2d) indicates that the nanocracking is already present at that stage of the process.

Contacting and removing the stamp from the substrate, when carried out carefully with stamps mounted on glass slides for support, does not seem to alter significantly the density or length scale of these cracks. This type of defect is often present when only Au is used; it is somewhat less frequently observed when Ti (1-2 nm) is used as an interfacial wetting layer between the Au and PDMS. The morphology and density of these nanocracks seem to be only weakly related to the physical properties (modulus, thermal expansion coefficient, etc.) of the PDMS stamps. (We noticed that evaporated Au films on in situ heated PDMS stamps present identical film structure with a similar density of nano-cracks.) In fact, similar nanocracking is present in 20 nm Au coatings deposited in the same manner onto bare silicon wafers with their

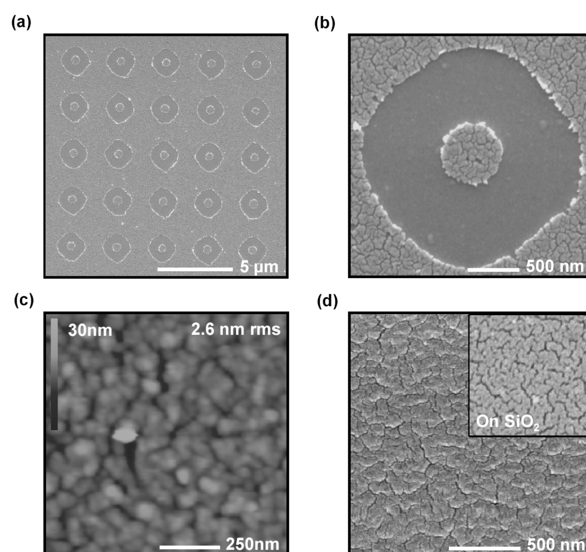


Figure 3.2: **(a)** & **(b)** Scanning electron micrographs and atomic force micrograph **(c)** of transfer printed patterns of Ti/Au (2 nm/20 nm). **(d)** SEM of a stamp (SiO_2 wafer surface in the inset) coated with Ti/Au (2 nm/20 nm).

native oxide (Figure 3.2d inset). In this case, a thin adhesion promoting layer of Ti (1-2 nm) deposited before the Au eliminates the cracks. Collectively, these observations suggest that it is the composition and deposition conditions for the metal layers that primarily controls the presence of cracks, rather than the physical properties of the stamps, the methods for printing or the transfer bonding of the metals.

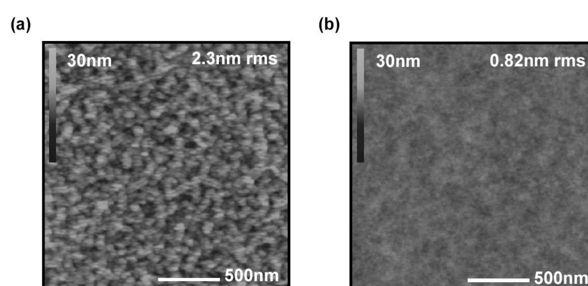


Figure 3.3: Atomic force micrographs of an evaporated Ti/Au metal layer on the surface of PDMS/gelest stamps. The top frame corresponds to Ti/Au (2 nm/20 nm) deposited directly onto the untreated surface of the stamp. The second frame illustrates results obtained when the stamp is exposed to a short (13 s) oxygen plasma before deposition of the metals. Crack free patterns of smooth (root mean squared roughness of <1 nm) gold films can be obtained in this manner.

We exploit this fact for nTP by first exposing PDMS to an oxygen plasma to create a silica-like surface layer[73,74] and then depositing Ti (2 nm at 0.3 nm/s) and Au (20 nm at 1 nm/s). These procedures yield smooth metal coatings that are free of cracks. See figure 3.3 & 3.4d. The time and conditions of the plasma treatment and the thickness of the Ti control the degree of adhesion of these coatings to the PDMS (*i.e.* reducing the oxygen plasma or thickness of Ti reduces the adhesion). Strong adhesion is useful for applications in soft contact lamination, where the coatings remain on the PDMS in the final device geometry. For nTP, the adhesion should be as weak as possible to facilitate transfer. Sufficiently poor adhesion of coatings that are free of nanocracks can be obtained by minimizing the duration of the oxidation step and the thickness of the Ti layer. Figure 3.4a-b shows the results.

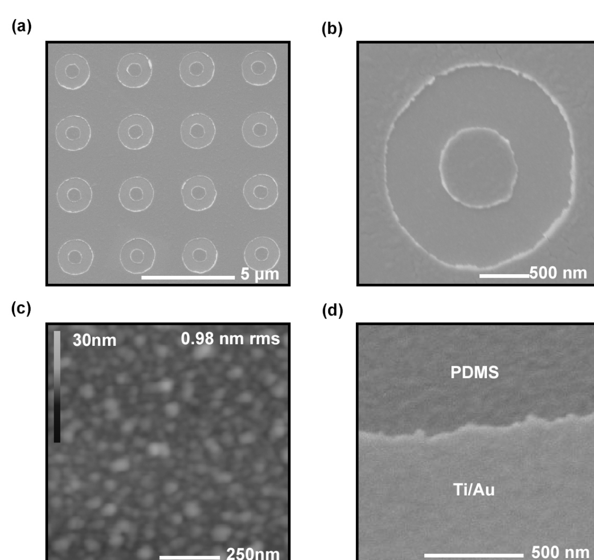


Figure 3.4: **(a)** & **(b)** Scanning electron micrographs and atomic force microscope (AFM) image **(c)** of a pattern printed with optimized conditions. **(d)** Scanning electron micrographs of the surface of a stamp coated with Ti/Au (2 nm/20 nm). The results indicate that nanotransfer printing can reliably form Au patterns that are smooth and crack free (as observed with AFM and scanning electron microscopy).

X-ray photoelectron spectroscopy (XPS) indicates that patterns printed in this manner are often coated with an ultrathin layer of PDMS-like material. We speculate that this layer improves the physical toughness of the printed films, thereby aiding in the formation of defect free patterns. Its thickness and extent of coverage is a sensitive function of the processing conditions. Figure 3.5 summarizes XPS measurements on transferred patterns of Ti/Au before and after exposure to a brief reactive ion etch (RIE) (60 s using an Uniaxis 790 Plasma-Therm Reactive Ion Etching system in an oxygen flow of 10 standard cubic centimeter per minute and 30 sccm of CF_4 at a chamber pressure of 30 mTorr with a 50 W RF power). The disappearance

of the Si(2p) peak and intensity increase of the Au(4f) peaks indicate that these coatings can be removed by this type of etching. Similar results are obtained with wet etching (5 min immersion in a boiling hydrogen peroxide solution).

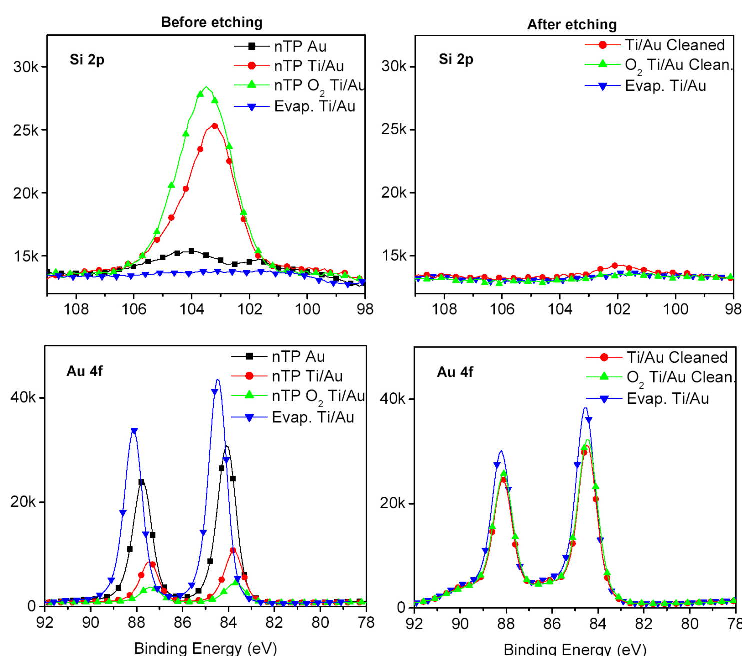


Figure 3.5: X-ray photoelectron spectroscopy of nanotransfer printed patterns of Ti/Au. The data were collected before (left side spectra) and after (right side spectra) treatment of the patterns with a reactive ion etch to remove residual organics from the surfaces of the printed films. The results show that these organics, which originate from the poly(dimethylsiloxane) stamps and are present as ultrathin films (∽ 2 nm thick, depending on processing conditions), can be removed effectively by dry etching. The Au and Si peaks intensity confirm that the cleanness of the RIE cleaned gold patterns is comparable to freshly evaporated Ti/Au film onto a bare silicon wafer (here included for comparison purposes).

Figure 3.6a shows AFM images of transferred coatings before and after exposure to the RIE. The etching induces little or no change in the morphology of the film. AFM analysis of a step edge (Figure 6b) caused by RIE etching through a mask indicates that these coatings are approximately 2 nm thick (with a one or two nanometer variation depending on the conditions for the plasma oxidation step). XPS experiments indicate that some Ti transfers to the substrate. If needed this ultra-thin layer can be briefly etched away in a HF:H2O 1:10 solution which does not damage the Au film.

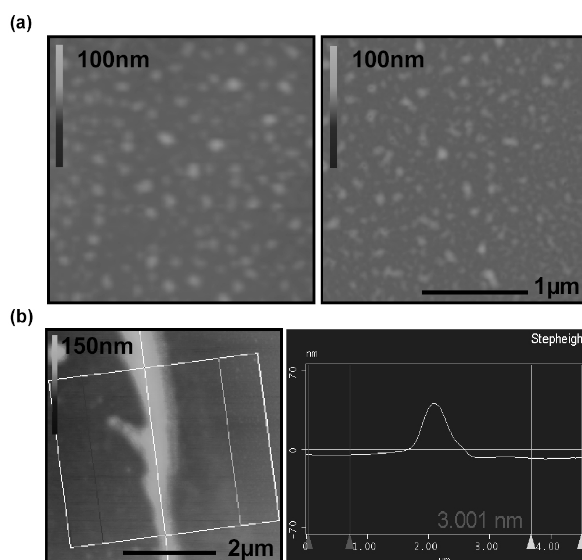


Figure 3.6: (a) Atomic force micrographs of patterns of Au/Ti formed by nanotransfer printing with optimized procedures. The images show representative areas of patterns before and after exposure to a reactive ion etching step that removes residual organics from the surfaces of the metal films. **(b)** Atomic force micrograph and cross section analysis of a the transferred silica-like coating etched by RIE through a membrane, the thickness of the residual organic layer is measured to be $\backsim$ 3 nm ($\pm$1 nm). The line cut represents the average of many line scans collected across the step.

3.3 Two and Three Dimensional Printing Using Optimized Stamp Relief Profiles.

Three dimensional nanostructures result from nanotransfer printing of ink coatings deposited not only on the raised and recessed regions of the stamps but also on their sidewalls. Figure 3.7 shows SEMs of some representative structures formed in this manner using the processing approaches described in the previous section. The top frames show an array of sealed nanocapsules formed by printing a continuous, conformal coating of Ti/Au (1.5 nm/15 nm) on a stamp that has an array of holes (*i.e.* arrays of cylindrical depressions, 500 nm diameters and 300 nm deep on its surface. Using a stamp with the inverse geometry (*i.e.* arrays of posts) produces the crossed nanochannel system shown in the middle frames. Structures with an ‘L’ geometry result from printing with a stamp that has surface relief in the geometry of an array of lines and is coated using a steeply angled flux of metal. The mechanical integrity of these features is remarkable. The ability to print structures of this sort depends critically on processing conditions that enable robust crack free coatings to be formed and transferred.

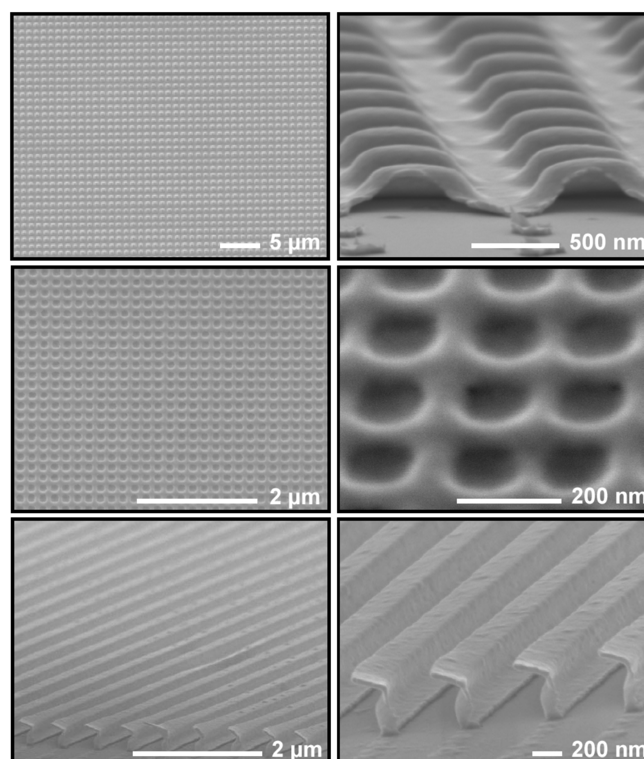


Figure 3.7: Scanning electron micrographs of representative three dimensional structures formed by nanotransfer printing. The left and right images show low and high magnification views, respectively. The top frames show arrays of sealed nanocapsules; the middle frames show a square grid of crossed nanochannels; the bottom frames show free standing 'L-shaped' beams.

For the three dimensional structures of Figure 3.7, sloping sidewalls on the stamp help to enable continuous ink coatings. To print two dimensional patterns with sharp, well defined edges vertical or re-entrant sidewalls must be used with a deposition flux collimated normal to the surface of the stamp. The sensitivity of printed two dimensional patterns to stamp geometry and deposition conditions can be reduced by incorporating sharply re-entrant features of relief near the contact surface of the stamp. Figure 3.8a schematically illustrates this approach. Fabrication of the necessary stamps begins by spin coating a silicon wafer with a layer of liftoff resist followed by conventional positive photoresist. Exposing and developing this bilayer resist removes selectively the positive resist in the areas that are exposed. The same developer also removes exposed or unexposed liftoff resist. The resulting structure consists of a pattern of the positive resist in the geometry of the photomask. By proper selection of development conditions, the liftoff resist can be removed completely in the exposed regions and to a small extent in the unexposed regions underneath the remaining positive resist. The latter effect yields a small undercut at the edges of the positive resist. For the experiments described here, the thickness

of the liftoff resist was ∽100 nm and the degree of undercut was ∽100 nm. Casting and curing PDMS against this type of master in the usual way generates stamps with 'T' shaped tops. The elastomeric nature of the PDMS enables stamps with these geometries to release nondestructively from the master. Figure 3.8b shows an SEM image of the relief structure on a typical stamp that has been coated with Au. A shadowed region beneath the overhang at the top of the stamp is visible.

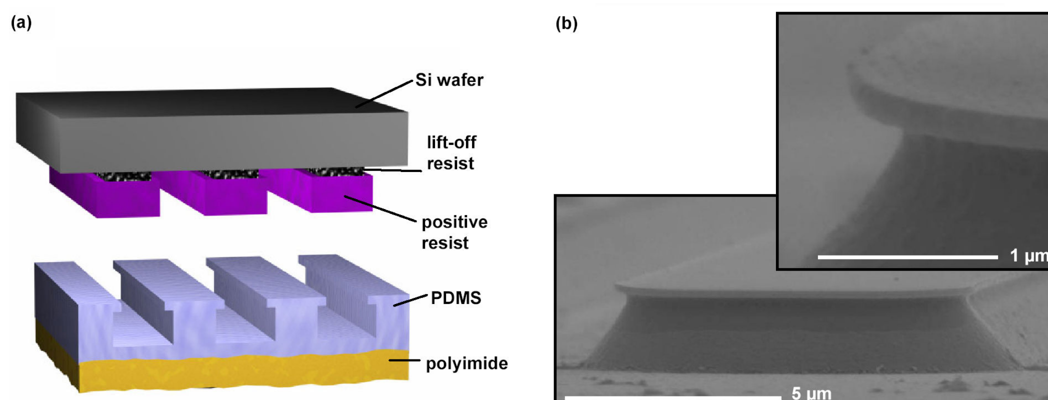


Figure 3.8: Schematic illustration (part **(a)**) of re-entrant stamps designed for high fidelity, two dimensional nanotransfer printing. A pattern of photoresist with an underlying layer of liftoff resist forms a master for generating PDMS stamps that have reentrant profiles. Such designs prevent the deposition of metal onto the relief sidewalls near the top surfaces of the stamps, even when these sidewalls are steeply sloped. The scanning electron micrograph in part **(b)** illustrates this effect; it shows a reentrant stamp with a thin layer of Au evaporated using a collimated flux oriented perpendicular to the surface of the stamp. A shadowed area that is free of Au is visible underneath the protruding reentrant feature of the stamp.

Figure 3.9 presents an AFM image of an edge region of a pattern produced by nTP with a stamp of this type. It also shows an image of a similar pattern generated with a stamp that has the same sidewall geometry, but without the sharply re-entrant structure associated with the liftoff resist. These results illustrate that the optimized stamp design eliminates the raised region at the edge of the Au feature printed with the conventional stamp. The liftoff masters and associated stamps could be used multiple times without damage.

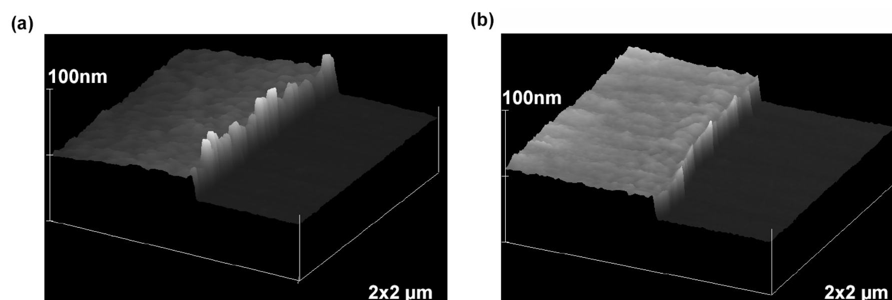


Figure 3.9: Atomic force microscope images of the edges of nanotransfer printed patterns of Au/Ti on GaAs. The edges in the patterns defined with unoptimized stamps (top) are rougher and have greater relief than those generated with reentrant stamps (bottom). The improved edges in the latter case derive mainly from the ability of the reentrant structure to prevent deposition of Au/Ti on the top parts of the sidewalls of the sloping relief features on the normal stamp.

3.4 Tough, Flexible Stamps that Use Thin Polymer Backings.

As we have described previously, placing thin elastomeric stamps against glass slides enhances their structural rigidity, thereby minimizing in-plane deformations that can lead to cracks in the solid inks during manipulation of the stamps before and during printing. This stamp design also reduces distortions that can frustrate accurate multilevel registration.[75] A disadvantage is that the thick glass backings make it difficult to bend the stamps. Bendability is important because it allows stamp-substrate contact to be established in a gradual, controlled manner that avoids trapped air pockets.[76] It also enables easy separation, by peeling, of stamps from their master or from a substrates. Although thin glass backing layers enable bending, they can be mechanically fragile and require the application of an uniform pressure on their backing for printing on uneven substrate.[21] Replacing the glass sheets with thin films of polymers that have a relatively high modulus yields composite stamps that (i) are easy to use for printing, molding, and other soft lithographic techniques, (ii) avoid in-plane deformations that can damage solid ink coatings for nanotransfer printing and (iii) lead to pattern distortions that are sufficiently low for micron-level pattern registration over large areas.* To demonstrate this concept, we built large area composite stamps using thin (5∽10 μm) PDMS layers with sheets of polyimide (Kapton® E 25 μm thick, DuPont) as backing layers. We typically also included with these stamps a thick (∽10 mm) PDMS flat or a second polyimide film separated by another thin (∽4 μm) PDMS layer, to facilitate handling and to avoid the curling that can occur after separation from the master (due to shrinkage of the PDMS and/or mismatch in the thermal expansion coefficients of the PDMS and the polyimide). Figure 3.10 shows a schematic illustration and a cross sectional SEM.

*U.S. Patent No. 60/565,604 on "*Composite Patterning Devices for Soft Lithography*"

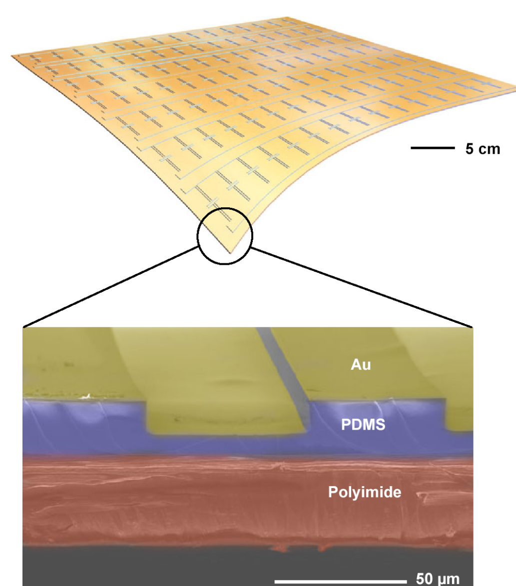


Figure 3.10: Schematic illustration (top) and cross sectional scanning electron micrograph (bottom) of a composite stamp. The structure consists of a thin layer of poly(dimethylsiloxane) bonded to a thin layer of polyimide. The resulting stamp is mechanically robust and flexible, and it is easy to use for printing. It has a relatively high in-plane modulus (5.3 GPa, defined mainly by the polyimide) that helps to reduce distortions that can occur in printing. The polyimide backing layer also decreases the tendency of the stamp to make unwanted contact with the substrate due to mechanical sagging in its recessed regions.

For this example, the relief layout corresponds to the source/drain level of an active matrix circuit for electronic paper displays. It consists of 256 interconnected transistors arranged in a square array over an area of 16×16 cm.[40] We quantified the distortions in these composite stamps by measuring with a microscope the misalignment at each transistor location between two successive prints, between one print and the stamp used to print and between a stamp and its master. Figure 3.11 shows distortions that correspond to measurements of positions of features on the stamp compared to those on its master. These results include corrections for overall translational and rotational misalignment and isotropic shrinkage (280 ppm for stamps cured at 80 ^{o}C and 60 ppm for those cured at room temperature). The Matlab® algorithm used to perform these corrections is included in the Appendix A. The residual distortions are close to the estimated accuracy ($\backsim$ 1 μm) of our measurement method. They include the cumulative effects of (i) fabricating and releasing the stamp from its master (ii) printing (wetting the stamp) on an uneven substrate (the master has some relief features $\backsim$ 9 μm thick).

Another attractive feature of the composite stamps is that they have a reduced tendency to sag mechanically in the recessed regions, which can cause unwanted stamp-substrate contact.[77]

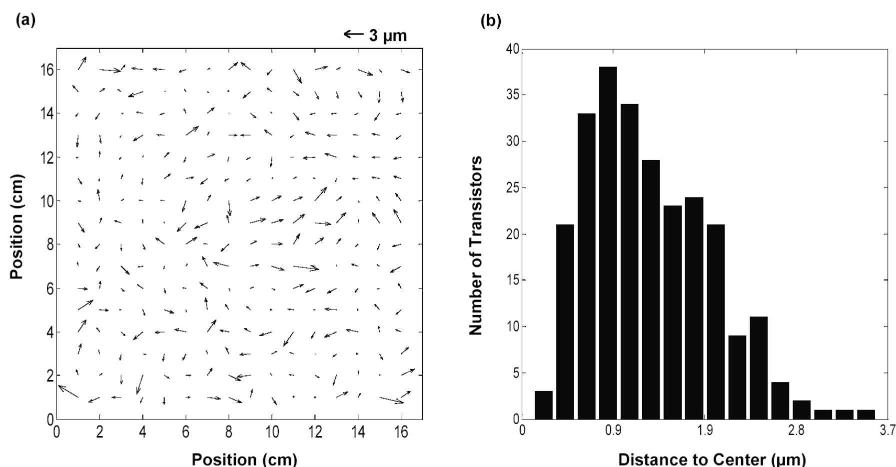


Figure 3.11: Distortion measurements collected at 256 points equally spaced across a 16 × 16 cm stamp that has the layout of the source/drain level of an active matrix backplane circuit for an electronic paper display. The top frame shows a vector diagram of misalignments between the stamp (which uses a composite design) and its master. (Overall translational and rotational misalignments are subtracted.) The bottom frame shows a histogram plot of the lengths of the vectors illustrated in the top frame. The median distortion is less than 1 micron. This value is better, by ∽25 times, than results observed by us with conventional single component stamps of poly(dimethylsiloxane) that have the same layout.

As an example, in the case of 60 μm wide lines separated by 60 μm (500 nm relief height), recessed areas of a regular single element PDMS stamp sag completely. No sagging is observed for the same relief geometry on a PDMS/polyimide/PDMS/polyimide (25/25/60/25 μm) composite stamp. Figure 3.12 shows top view optical micrographs that illustrate these results. The color uniformity in the recessed area of the composite stamp (Figure 3.12b) suggests that the bowing is almost zero. Finite element modeling of the composite structure indicate that the kapton backing efficiently reduces the tendency of the stamp for sagging when the residual PDMS layer is thin (Details concerning the sagging behavior of PDMS stamps are given in the Appendix B).

3.5 Conclusions

The surface chemistries, thin film deposition techniques and stamp designs presented in this chapter enable patterning, with high fidelity and low defect density, two and three dimensional nanostructures by nanotransfer printing. The successful fabrication of self-supporting discontinuous 3D metal nanostructures, in particular, demonstrates the efficiency of some of these procedures. The morphology of the transferred patterns is, however, highly sensitive to the

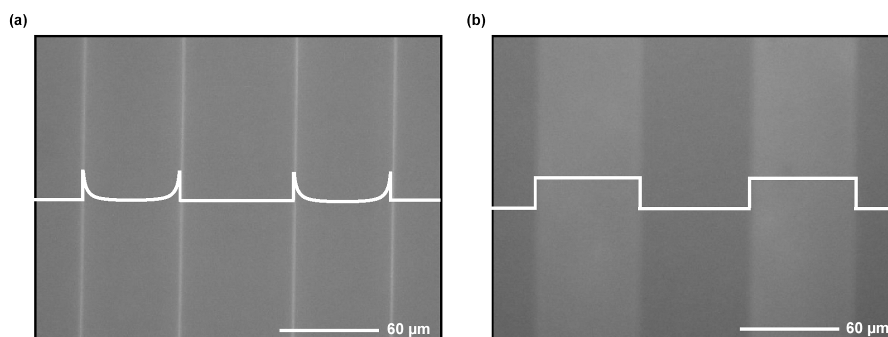


Figure 3.12: Optical micrographs (parts **(a)** and **(b)**) of stamps placed against glass slides, obtained by imaging through the stamps. The lines schematically illustrate the shape of the relief (500 nm height) on the stamp after contact. Part (a) indicates complete sagging of the recessed regions of a conventional single component poly(dimethylsiloxane) (PDMS) stamp. Part **(b)** shows a similar image of a composite stamp that uses the same PDMS chemistry, but in a thin film ($\backsim$ 25 μm) geometry supported by a thin (25 μm) polyimide sheet. This stamp shows no evidence of sagging.

preparation of the stamp surface prior to metallization. For example, in some cases the plasma oxidation treatment can form low density shallow (10 nm deep) small diameter (30 nm) depressions on the surface of the stamp. This effect leads to small gold bumps on the surface of the transferred film. See Figure 3.6a. In other cases, excessive plasma treatment leads to a failure interface upon transfer that is cohesive at a depth of some microns below the surface of the stamp. Careful process control can eliminate these effects. It is likely that similar optimization through study of surface chemistry will be required for printing of materials other than those explicitly described here. The low level of distortions observed in easy-to-use, flexible composite stamp designs indicates that the printing method, in its current form, can meet the requirements of applications in plastic electronics and in many areas of subwavelength and integrated optics. These features suggest that nTP may represent a versatile tool for patterning, in a purely additive fashion, materials with nanometer resolution.

3.6 Experimental Section

Printing Procedures. Metal evaporation was performed with a Temescal electron beam system (BJD 1800) and deposition rates of 0.3 nm/s for Ti and 1 nm/s for Au. Pressures during evaporation were typically $\backsim 3 \cdot 10^{-6}$ Torr or less. A deposition rate monitor was installed in position such that the rates could be established and stabilized before exposing the stamps or substrates to the flux of metal. The printing was performed in open air shortly after deposition. The stamps typically come into intimate contact with the substrates without applied pressure. In some cases small pressure applied by hand initiated contact at one edge, which then proceeded naturally

across the stamp-substrate interface. Peeling the stamp away from the substrate after contact for a few seconds completed the printing. The stamps used either glass slides or thin sheets of polyimide as structural supports to prevent unwanted in-plane strains during processing or printing.

3.6.1 Fabrication of Stamps with Re-Entrant Sidewalls

Masters with sharply re-entrant profiles used positive photoresist (S1818; Shipley, www.shipley.com) and liftoff resist (LOR1A ; MicroChem, www.microchem.com). Test grade $\backsim$ 450 μm thick silicon wafers (Montco Silicon Technologies, www.silicon-wafers.com) were cleaned with acetone, iso-propanol and de-ionized water and then dried on a hotplate at 150 °C for 10 min. In the first step, LOR 1A resin was spin-coated at 3000 rpm for 30 s and then pre-baked on a hotplate at 130 °C for 5 min. Next, the S1818 resin was spin-coated at 3000 rpm for 30 s and baked on a hotplate at 110 °C for 5 min. The resulting bilayer film ($\backsim$ 1.7 μm thick) was exposed (λ= 365 nm, 16.5 mW/cm^2 for 7 s) with an optical contact aligner (Suss Microtech MJB3) using a chromium on glass mask, and then developed (MF-319; Shipley, www.shipley.com) for 75 s. This development removed all of the S1818 resist that was photoexposed. It also removes, in a roughly isotropic manner, the LOR1A in both the exposed and unexposed regions. The result is a pattern of S1818 on LOR1A with regions of bare substrate in the exposed areas and slight undercuts at the edges of the patterns. Standard soft lithographic procedures of casting and curing PDMS against these patterns produce stamps with the desired sharply re-entrant features.

3.6.2 Fabrication of Stamps with Flexible Polymer Backings

Masters were prepared with conventional contact mode photolithography (features larger than 2 μm) or electron beam lithography (features smaller than 2 μm). The masters for the large area stamps were formed by direct write photolithography using procedures described elsewhere.[25] PDMS (Sylgard 184 from Dow Corning, www.downcorning.com) or h-PDMS (VDT-731, Gelest Corp., www.gelest.com) were mixed and degassed, poured over the masters and cured in a oven at 80 °C. In some cases, the curing of the 184 PDMS material was performed at room temperature, by using twice as much curing agent as recommended by the vendor of this material. Kapton® polyimide films 100E (DuPont, www.dupont.com/kapton) were plasma oxidized using an Uniaxis 790 Plasma-Therm Reactive Ion etching system in an oxygen flow of 20 standard cubic centimeter per minute at a pressure of 30 mTorr for 3-5 min with a 100 W RF power. A few drops of h-PDMS were dispensed onto the surface of the master and then the kapton sheet was slightly bent and brought into contact with the master (plasma treated side facing down). Air bubble formation was prevented by slowly bringing down the full sheet of plastic from the center toward the edges. Rolling a glass cylinder over the surface of the sheet

reduced the thickness of the PDMS layer to 5-10 μm.

3.6.3 Instrumentation

AFM images were recorded using a Dimension 3100 microscope in tapping mode. The images were analyzed using the Nanoscope IV v5.12b18 software package (Digital Instruments, Santa Barbara, CA). SEM images were recorded using a Philips XL30 Field-Emission Environmental Scanning Electron Microscope (ESEM-FEG) in high vacuum mode. All images were recorded with an accelerating voltage of 5 keV and a gun-sample distance of 10 mm. XPS spectra were obtained using a Kratos Axis Ultra photoelectron spectrometer using Al KR radiation (15 kV, 225 W, base pressure $\backsim 5{\cdot}10^{-10}$ Torr). High-resolution spectra of the Si(2p) and Au(4f) core levels were collected at a pass energy of 40 eV with a 1.0 mm^2 spot size. The binding energies were normalized and corrected by referencing the C(1s) binding energy to 284.5 eV. High-resolution spectra backgrounds were corrected using a linear fitting function for the baseline.

Chapter 4

Dry Transfer Printing Techniques with High Resolution Molded Rubber Stamps

4.1 Deposition and Patterning of High-Performance Semiconductors on Flexible Substrates

As we have seen in the previous chapters, high performance printed circuits on large area flexible substrates represents a new form of electronics that could have wide ranging applications in sensors, displays, medical devices and other areas. Fabricating the required transistors on plastic substrates represents a challenge to achieving these 'macroelectronic' systems. We have seen that the patterning of some of the passive circuit elements could be realized using various soft lithography methods. It is worth mentioning that most of these methods have focused on the patterning or transfer of metal or liquid 'ink' materials. But the deposition and patterning of high performance semi-conducting materials on flexible substrates remain an unsolved issue.

Some approaches that have been explored over the last several years are based on modified, low temperature versions of the types of process steps used to fabricate conventional silicon based thin film transistors (TFTs) on glass/quartz substrates.[78] The high temperatures associated with the directional solidification processes developed for producing single-crystal silicon films (*i.e.*, zone-melting recrystallization of Si films on SiO_2 using a cw laser, a focused lamp, an electron beam, or a graphite-strip heater) make this approach unsuitable for use with plastic substrates.[79] Laser based approaches have achieved some limited degree of success, although uniformity, throughput and use with low cost plastics represent topics of continuing work.[80,81] Direct full wafer transfer of preformed circuits onto plastic substrates can yield the necessary devices, but this approach is difficult to scale to large areas and it does not retain printing type fabrication sequences that might be important for low cost, large area macroelectronics.[82] Organic semiconductor materials provide an alternative path to flexible electronics; here the organic based electronic materials can be naturally integrated, via room temperature deposition,

with a range of plastic substrates.[83,84] Known organic semiconductors, however, enable only modest device mobilities. Even high quality single crystals of these materials have mobilities in the range of 1-2 $cm^2/V{\cdot}s$ and $\backsim$ 10-20 $cm^2/V{\cdot}s$ for *n* and *p*-type devices, respectively.[85–87] Innovative techniques such as fluidic self assembly separate the high temperature steps for producing high mobility materials from the low temperature processing that is required for building devices on plastic substrates.[88] These methods do not, however, allow efficient control of the organization or location of the deposited objects.

4.2 Dry Transfer Printing of Inorganic Semiconductor Micro-Structures and Carbon Nanotubes

In order to address these issues, an efficient room temperature dry transfer printing technique, with potentially excellent registration capability,[89] has been invented.* This new soft-lithography method, called Dry Transfer Printing (DTP), is capable of transferring thin solid objects such as well defined 'pieces' of semiconducting elements. This technique has been successfully used to deposit on plastic substrates a range of high quality semiconductors, including single crystal Si ribbons,[90] Ga-As and InP wires[91] and single-walled carbon nanotubes.[92]

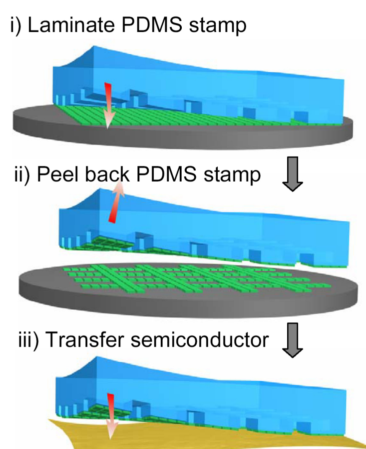


Figure 4.1: Schematically illustrates Dry Transfer Printing (DTP) of semiconducting elements from a 'mother' wafer to a substrate. **(i)** A PDMS stamp is brought into intimate with the top surface of nanometer thick semiconducting elements. **(ii)** Surface adhesion forces enable the transfer of these elements from the surface of a substrate to the PDMS stamp. **(iii)** The semiconducting elements are then transferred onto a target substrate coated with an adhesive layer.

*International Patent No. 11/145,574 on "*Methods and Devices for Fabricating and Assembling Printable Semiconductor Elements*"

Figure 4.1 schematically presents the concept. Soft stamps (made out of PDMS) are used to pick-up, selectively, individual solid objects from one substrate and then to transfer those objects onto another target substrate.

With the help of theorists from the department of Theoretical and Applied Mechanics at the University of Illinois at Urbana-Champaign, we are studying the detailed mechanism of adhesion and release from soft elastomeric stamps. This analysis is out of the scope of this thesis report, so only the experimental results are briefly presented in the Appendix B. Further details concerning the underlying theory can be found in the a *Langmuir* article that we recently published in collaboration with Pr. Hsia and Pr. Huang.[93] A second article, with a more advanced analytical model taking into consideration the local Van Der Waals forces which are present at the interface between the stamp and the semi-conducting elements (or a flat substrate), is currently in preparation.

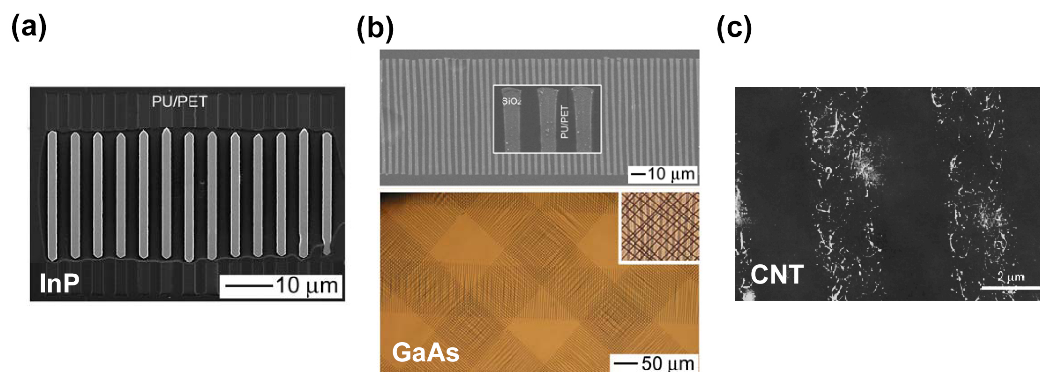


Figure 4.2: Nanoscale semi-conducting elements transferred onto poly(urethane) coated poly(ethylene-terephtalate) (PET) plastic substrates. Part **(a)** shows a high resolution scanning micrograph of transferred Indium-Phosphorus (InP) wires. Part **(b)** shows high resolution scanning micrographs and optical images of transferred GasAs wires. Part **(c)** shows single walled carbon nanotubes (SWNT) transferred stripes. In this case the PET substrate is coated with poly(methyl-methacrylate) (PMMA).

This new DTP method has been applied to several kind of semiconductors. Figure 4.2a shows, as an example, a high resolution scanning electron micrographs of indium phosphide (InP) ribbons transferred by DTP, from a bulk wafer, onto the surface of a poly(ethylene-terephtalate) (PET) plastic substrate coated with a thin poly(urethane) layer. Figure 4.2b shows similar results for the case of gallium arsenide (GaAs) wires.[91,94] The bottom inset optical images show a cross patterned array of these elements obtained by successive dry transfer printings. A similar approach can be used for individual single walled carbon nanotubes (SWNTs). Figure 4.2c shows, for example, an atomic force micrograph (AFM) of the surface of a poly(methyl-methacrylate) (PMMA) coated PET substrate on which SWNTs have been transfer printed. In this case, the stamp was inked by direct spin coating of the SWNTs on the

stamp.[92]

The transfer, by dry printing, of high performance semiconducting elements (such as Si, InP or GaAs which are all grown at high temperature) to a low cost plastics (of the type that would be incompatible with the high temperature growth procedures for the semiconductors) could be extremely useful for the fabrication of flexible, high performance electronic devices. This approach has the potential to lead to new consumer electronic systems such as electronic-paper, flexible ultra large street display panels and lightweight steerable antenna systems for military applications. It is primarily for these application possibilities that we recently developed a dry transfer printing (DTP) technique. This method was first successfully applied to the fabrication of some of the highest performance electronic circuit devices on plastic substrates.[90]

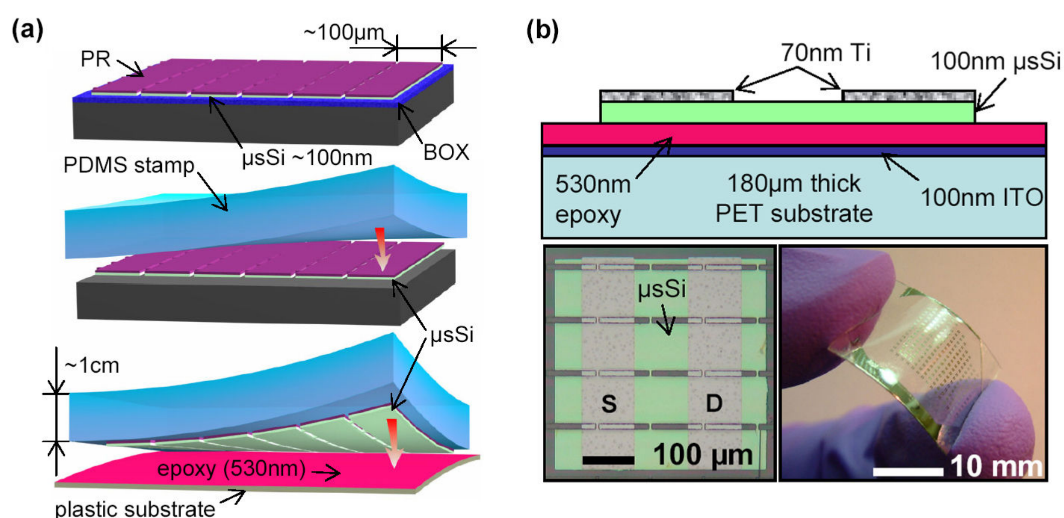


Figure 4.3: Schematic illustration of steps for transferring microstructured silicon (μs-Si) ribbons from a 'mother' wafer to a plastic substrate. **(a)** Conventional lithographic and dry (SF_6 plasma) etching procedures define μs-Si on the top surface of a Silicon On Insulator (SOI) wafer. After wet etching the underlying SiO_2, these objects are picked-up from the surface of the SOI using a flat PDMS stamp. Then they can be dry transfer printed onto a plastic substrate coated with a thin epoxy film. **(b)** Device structure schematic of a high performance thin film transistor built on an ITO coated (100 nm) PET substrate. The bottom insets show high and low magnification optical images of a $\backsim$10$\times$10 mm device array. Each device uses 4 interconnected microstrips (95 μm wide) of 100 nm thick single crystal silicon. The device channel width is W=400 μm and the length is L=100 μm.

Figure 4.3a illustrate the steps used to fabricate high performance single crystal silicon devices on a flexible plastic substrate. The detailed process is given, at the end of this chapter, in the experimental section. Figure 4.3b presents a schematic illustration of this bottom gate device configuration together with high and low magnification optical images of an array of high performance micro-structured silicon (μs-Si) elements (ribbons in this case) transferred onto a

poly(ethyleneteraphtalate) (PET) trasnparent substrate using the DTP method.

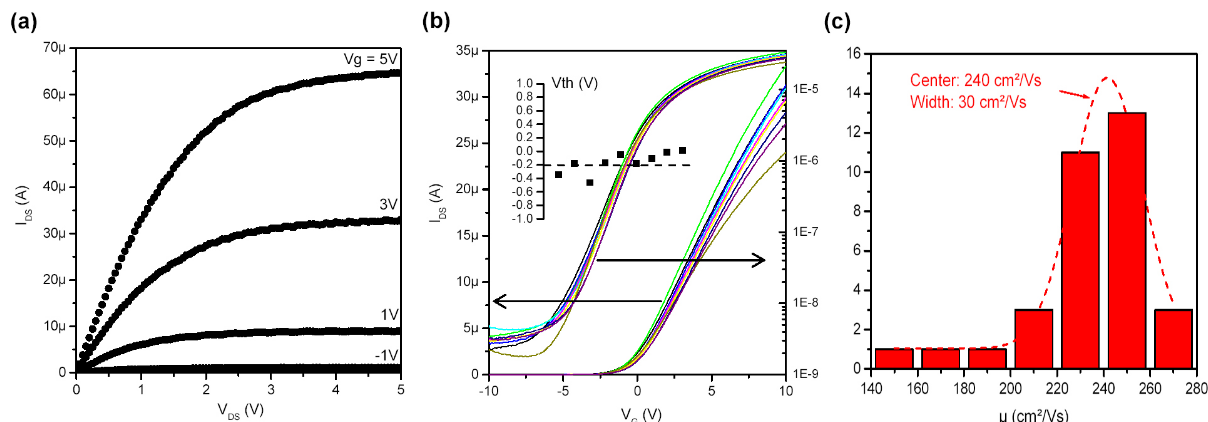


Figure 4.4: Electrical characterization of the High performance thin film transistor devices on PET substrate. Part **(a)** shows current-voltage (I-V) characteristics of one of the devices. Part **(b)** shows on a linear (left axis) and logarithm (right axis) plot several transfer characteristics of the transistors measured at a drain-source bias V_{DS}=0.5 V. The threshold voltage values of these devices are displayed on the inset plot. Part **(c)** shows the distribution of the devices'field effect mobilities.

Figure 4.4a presents the current-voltage characteristics of a device that show an effective device mobility of 140 $cm^2/V{\cdot}s$ in the saturation regime and 260 $cm^2/V{\cdot}s$ in the linear regime, as evaluated by application of standard field effect transistor models that ignore the effects of contacts.[95] Figure 4.4b presents transfer characteristics of several devices, plotted on linear (left axis) and logarithmic (right axis) scales. The plot in the inset shows that the threshold voltages have a narrow distribution near 0 V. Small ($<$ 4% in current for a $\pm$10 V cycle) hysteresis in the transfer characteristics indicates a low density of trapped charges at the interface between the silicon (with native oxide) and the epoxy dielectric. The small values ($\backsim$ 13 $V{\cdot}nF/dec{\cdot}cm^2$) of the normalized subthreshold slopes confirm the good quality of this interface, which may be governed primarily by the interface between the silicon and its native oxide. Figure 4.4c shows the distribution of the linear effective mobilities of the devices. A Gaussian fit indicates a center value of 240 $cm^2/V{\cdot}s$ with a standard deviation of 30 $cm^2/V{\cdot}s$. The performance of these devices are excellent, some of the low values can be associated with slight defects in the electrodes or other components of the devices.

The mechanical flexibility and robustness of these devices were investigated by performing frontward and backward bending tests. Figure 4.5a top inset presents a high-resolution scanning electron micrograph of solution cast ribbons illustrating the remarkable flexibility of the thin Si objects. The bottom inset shows a picture of the setup used to bend the devices. A relatively thick ($\backsim$180 μm) plastic substrate was used in order to maximize the strain induced in the devices when the plastic sheet is bent. Figure 4.5b top inset shows the small ($\lesssim$ 1%) linear vari-

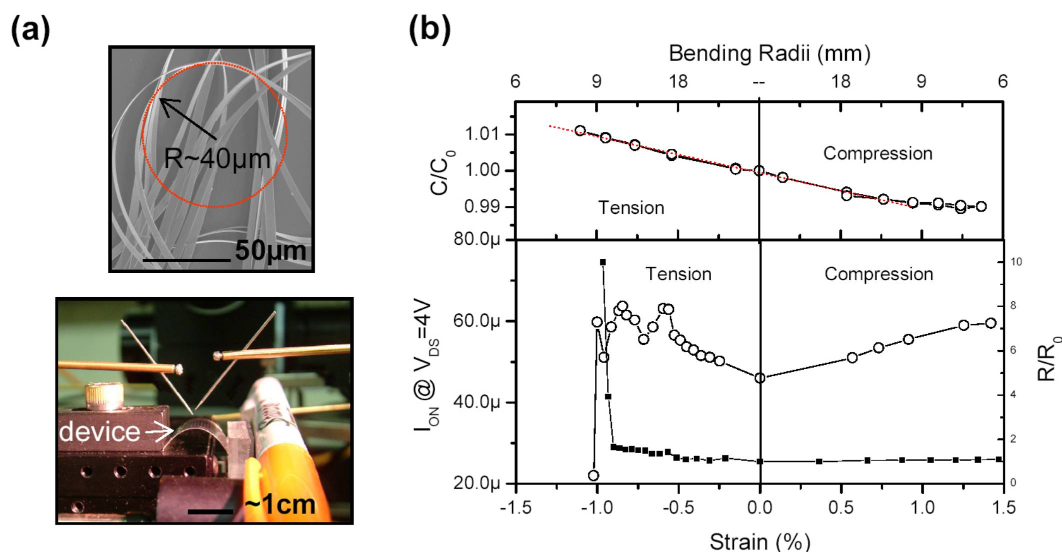


Figure 4.5: Bending test of the devices built on a 180 μm thick PET plastic substrate. Part **(a)** left inset shows a high resolution SEM pictures of μs-Si ribbons solution deposited on the surface of a silicon wafer. The right inset shows a picture of the precision mechanical stage used to frontward (and backward) bend the plastic circuit. Part **(b)** shows the variation of the dielectric capacitance value together with the device saturation current when the plastic circuits are subject to compressive or tensile mechanical strain. The ITO normalized resistivity is plotted on the right axis.

ation of the epoxy dielectric capacitance when subject to tensile and compressive strains. The bending radius and strain values where computed using a finite element model of the buckling sheet. Comparisons of the bending profiles of the buckling sheet (for several bending radius) to the profiles obtained with the finite element method confirmed the accuracy of the simulations. The second inset presents the variation of the saturation current of a device measured for a gate and drain bias voltages of both 4 V. The maximum value of the tensile strain at which the device can be operated seems to be limited by the failure of the ITO gate electrode (which fails a tensile strain value of $\backsim$ -0.9%). The devices operate well even at compressive strains as high as 1.4%. This level of bendability is comparable to that recently reported for organic transistors based on pentacene. The failure mechanism of our silicon devices and the effects of fatigue for repeated bending are the subject of current study. Takahiro *et al.* demonstrated that micro-size single crystal silicon objects etched from the top layer of a SOI wafer can withstand remarkably high tensile stress (>6%).[96] The cause of the modest variation in output current with strain requires further investigation. The known variation in mobility with strain contributes (but does not fully account for) these changes. Devices of the type that we describe here might, in fact, enable new opportunities to investigate the charge transport in mechanically strained silicon at strain values not easily reached when bulk Si wafers are bent.[97]

4.3 Conclusion and Future Outlook

The fabrication techniques presented in this chapter have considerable value for applications in nanoscience and nanotechnology, partly because of the simplicity and availability of the materials and equipments on which they rely. They will continue to facilitate research in these areas, particularly for those who do not have access to the more costly conventional lithography patterning systems. We speculate that the dry transfer printing methods will be applicable to solid materials that have dimensions outside the range (smaller and larger) than those illustrated here. Their capability for transferring high performance semi-conducting materials, to virtually any substrate, without compromising their integrity, performance and alignment have been demonstrated with the fabrication of high performance thin film transistors on plastic substrates. Although the use of these techniques has been confined mostly to research laboratories, they are beginning to migrate into prototype industrial lines for the fabrication of large area display panels. Work in this direction, as well as toward the development of new techniques, will be the focus of future efforts.

4.4 Experimental Section: Dry Transfer Printing of μs-Si Devices

First, photolithography defined on the surface of a silicon-on-insulator wafer (Soitec unibond SOI with a 100 nm top Si layer and 145 nm buried oxide) a layer of photoresist. This resist served as a mask for dry etching the top silicon layer of the SOI wafer with a SF_6 plasma (Plasmatherm RIE system, 40 sccm SF_6 flow with a chamber base pressure of 50 mTorr, 100 W RF power for 25 s). A concentrated HF solution etched the buried oxide and freed (but does not completely float off) the Si objects from their substrate. A flat piece of poly(dimethylsiloxane) (PDMS) was then brought into conformal contact with the top surface of the wafer and then carefully peeled back to pickup the interconnected array of ribbons. The interaction between the photoresist and the PDMS was sufficient to bond the two together for removal, with good efficiency. An Indium-Tin-Oxide (ITO; thickness $\backsim$ 100 nm) coated poly(ethyleneteraphtalate) (PET; thickness $\backsim$ 180 μm) plastic sheet served as the device substrate. Washing it with acetone & isopropopanol, rinsing it with deionized water and then drying it with a stream of nitrogen cleaned its surface. Treating the ITO with a short oxygen plasma (Plasmatherm RIE system, 20 sccm O_2 flow with a chamber base pressure of 100 mTorr, 50 W RF power for 10 s) promotes adhesion between it and a spin cast dielectric layer of epoxy (3000 RPM for 30 s of Microchem SU8-5 diluted with 66% of SU8-2000 thinner). This photo sensitive epoxy was pre-cured at 50 ^{o}C on a hot plate during $\backsim$ 1 min. Bringing the PDMS with the μs-Si on its surface into contact with the warm epoxy layer and then peeling back the PDMS led to the transfer of the μs-Si to the epoxy. Evidently, the bonding forces between the silicon and the soft epoxy layer (some of which are mechanical, due to the flow of epoxy around the μs-Si edges) are stronger

than those between the photoresist and the PDMS stamp. The epoxy layer was fully cured at 100 °C for 5 min, exposed to UV light from the back side of the transparent substrate for 10 s and then post baked at 115 °C for 5 min to crosslink the polymer. The photoresist mask (which, conveniently, prevents contamination of the top surface of the Si during the transfer steps) was dissolved with acetone and the sample was then abundantly rinsed with deionized water. Source and drain electrodes used Ti ($\backsim$ 70 nm; Temescal e-beam evaporator) deposited on the top Si surface. Etching (1:1:10 HF:H2O2:DI for $\backsim$ 2 s) through a photoresist mask (Shipley S1818) patterned on the Ti defined the geometry of these electrodes. The last step of the fabrication involves dry etching (SF_6 using the RIE parameters given above) through a photoresist mask to define islands of silicon at the locations of the devices.

Part II

Organic Semiconductors

In the previous part we have seen various novel printing techniques that will enable the commercialization of large area plastic electronic systems. The second part will be focused on the study of a promising organic semiconducting material for such kind of applications. We will begin this second part with an overview of recent studies of charge transport in organic semiconductor and the characterization of these materials. As a rather large number of articles have been published in this field, due to the potentially high commercial impacts of these researches, we will limit our overview to single crystals made out of low-molecular-weight materials.

Then we will present a new methodology for probing charge transport in fragile semiconductors in a non-invasive, reversible fashion. The critical advance demonstrated here involves the construction of three terminal probes (source/drain electrode, gate dielectric and gate electrode) entirely on the surface of a flexible elastomer, polydimethysiloxane (PDMS). These stamps are laminated against independently grown organic crystals (rubrene) to yield field effect transistors (FETs) in which the crystal surface is unexposed to any conventional processing. The strength of our approach is reflected in the characteristics of these FETs. More importantly, these probes have revealed new physics through the large in-plane, field effect mobility anisotropy in rubrene; an observation that is only possible because we are able to sequentially probe charge transport on the same crystal surface in different directions. This observation, though long predicted, is seen for the first time at the surface of organic crystals and attests to the sensitive, reversible and inherently non-invasive nature of the methodology presented here.

Then we went further and improved the stamp structure to obtain new record high performance characteristics - mobilities and normalized sub-threshold slopes - in both n- and p-channel organic transistors. These results follow directly from the implementation of a new device design that incorporates a thin free space layer as a gate dielectric. When combined with high quality single crystal organic semiconductors, this design yields the ultimate in OFET performance, limited only by polaronic transport on the pristine free surface of the crystal. It avoids completely all of the detrimental (and typically unknown) interactions (doping, trapping, dipole formation, *etc.*) that occur at the interface between a conventional solid material dielectric and a semiconductor.

Finally we will report on the molecular resolution scanning tunnelling microscope (STM) measurements on single crystals of the organic semiconductor rubrene. These images reveal the real space position and orientation of rubrene molecules at the surface that has been used for fabrication of high-mobility rubrene field-effect transistors. Current-voltage characteristics, measured with the STM, reveal nearly ideal rectifying p-type behaviour without dangling-bond related surface transport channels that are observed in inorganic semiconductors such as silicon. It is shown that the STM can be used as a tool for molecular scale modification of the rubrene surface; this opens up the possibility of the nanoscale patterning the conducting channels in organic transistors and related devices.

Chapter 5

Overview of Organic Semiconductor Devices

5.1 From Conducting Polymers to Organic Single Crystal Semiconductors

Traditionally, organic materials are considered as insulators having relatively poor electrical characteristics. As a matter of fact, these materials are commonly used to insulate standard copper wires. But in the 1970s, Heeger *et al.* found that polyethylene molecules could become good conductors by doping.[98] In order to conduct electricity, *i.e.* transport electrical charges, the polymer must be congugated. The main backbone of the polymer must have single carbon-carbon bonds followed by multiple C-C bonds. Su, Schrieffer and Heeger developed a simple tight-binding model, the Su-Schrieffer-Heeger (SSH) model, to explain the hopping of the charge carriers along the backbone of polyacetylenes. Since this discovery, the conducting polymers have received increasing attention from the research community and industry. Heeger *et al.* also demonstrated that the conductivity of these polymers could be greatly enhanced by doping the materials with charged particles such as ions. Then, the researches in this field quickly focused on the study of more complex polymers and small molecules having π delocalized electrons on benzene or thiophene rings.[99]

The organic field-effect transistors (OFETs), whose electrical characteristics are modulated by an electrical field, have been first described in 1987.[101] These devices are key building blocks for applications such as low-end electronic displays that we have presented in the first part. Most of the recent researches in this field have focused on the development of optimized fabrication techniques and materials in order to achieve high performance and good stability over time of the device electrical characteristics of the built devices. Polymers and shadow evaporated small molecules represent good candidate for the fabrication of plastic electronics circuits as they can be deposited on large area flexible substrate with a rather low manufacturing

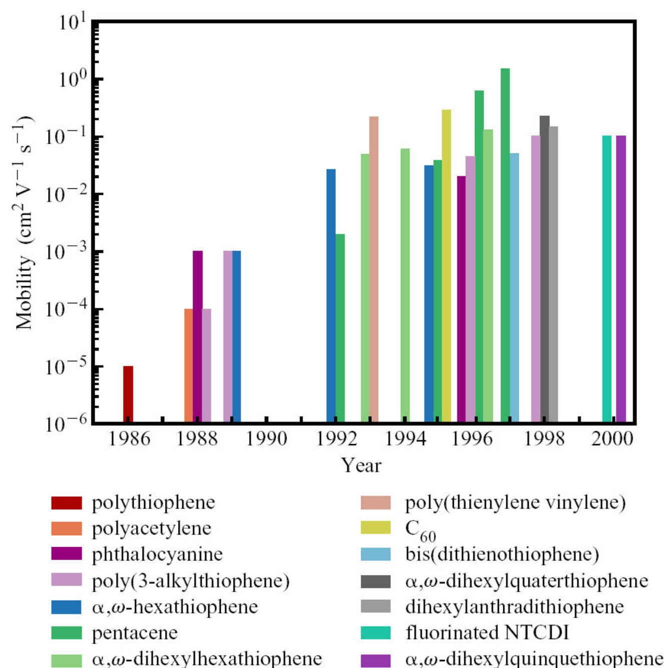
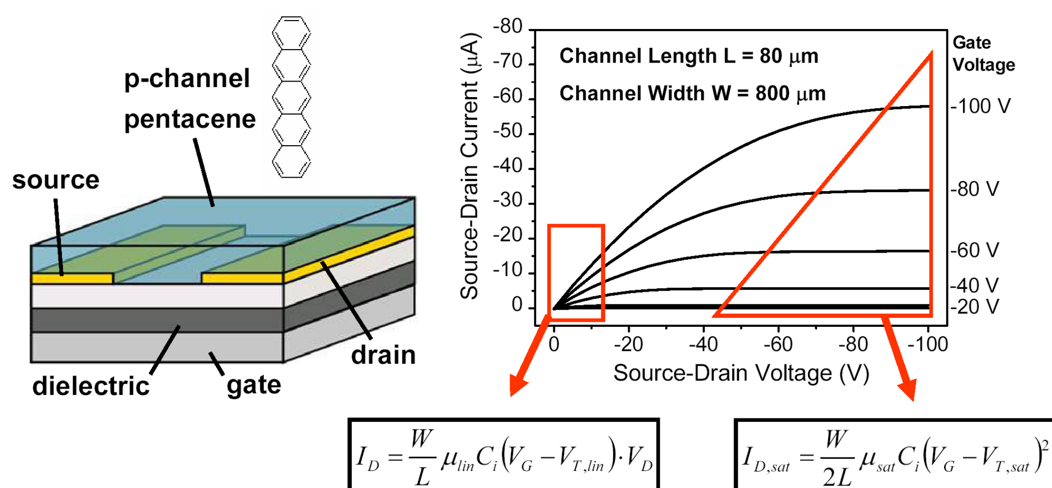


Figure 5.1: Semilogarithmic plot of the highest field-effect mobilities (μ) reported for OTFTs fabricated from the most promising polymeric and oligomeric semiconductors versus year from 1986 to 2000.[100]

cost. Significant progresses have been made since the invention of the first OFET, but the best to date devices have performances lower or equal to the amorphous silicon devices commonly used by the industry to drive the pixels of flat panel displays (See Figure 5.1).

The typical OFET device fabrication is extremely simple and very similar to the amorphous silicon thin film devices. In order to avoid the unintentional degradation of the organic semiconductor during the device fabrication process, the organic semiconductor is usually deposited at the end of the process. The source, drain, gate electrodes and a dielectric are typically prefabricated on a flat substrate, such as a silicon wafer, resulting in a so-called ‘bottom gate’ structure (see Figure 5.2). The current flowing between the drain and source electrodes is modulated by the applied gate voltage. When no gate voltage is applied, the source-drain current is very low and the transistor is normally off. With an increase in the gate voltage other the device threshold voltage, a layer of mobile charges can accumulate at the interface between the semiconductor and insulator. The current increase and the transistor enter in the on state. From the output, we can see that if a higher source-drain voltage is applied, the device gradually enters the saturation regime where the source-drain current becomes independent of the drain bias. This saturation behaviour is in digital circuits where the device is used as an electrical switch.



$$I_D = \frac{W}{L}\mu_{lin}C_i\left(V_G - V_{T,lin}\right)\cdot V_D$$

$$I_{D,sat} = \frac{W}{2L}\mu_{sat}C_i\left(V_G - V_{T,sat}\right)^2$$

Figure 5.2: Typical pentacene field effect transistor fabricated on a pre-oxidized silicon wafer. The current-voltage output characteristics (IV) of the device are modeled using standart long channel field effect transistor equations.

Although the output electrical characteristics of these OFETs devices seem to be well modelled with basic transistor equations, the underlying conduction mechanism is far from being well understood. After several decades of intensive research our understanding of the charge transport in conjugated polymers and small-molecule organic semiconductors remains incomplete. Complexity of the transport phenomena in these systems is due to the polaronic nature of charge carriers[102] and the strong interaction of small polarons with defects. For the emerging field of organic electronics,[103] it is especially important to develop an adequate model of the polaronic transport at room temperature. As we will see, organic single crystals represent ideal systems for this kind of studies.

5.2 Organic Single Crystal Growth

Most of the single crystals used so far for the fabrication of organic FETs have been grown from the vapor phase in a stream of transport gas, in horizontal reactors (glass or, better, quartz tube).[104,105] In the Physical Vapor Transport (PVT) method, the starting material is placed in the hottest region of the reactor, and the crystal growth occurs within a narrow temperature range near its cold end (see Figure 5.3). For better separation of larger and, presumably, purer crystals from the rest of re-deposited material along the tube, the temperature gradient should be sufficiently small (typically, 2-5 ^oC/cm). Several ultra-high-purity gases have been used as a carrier agent,[106] the highest mobility of tetracene-based devices was realized with argon, whereas the best rubrene FETs fabricated so far have been grown in pure H_2.[107,108] In the latter case, hy-

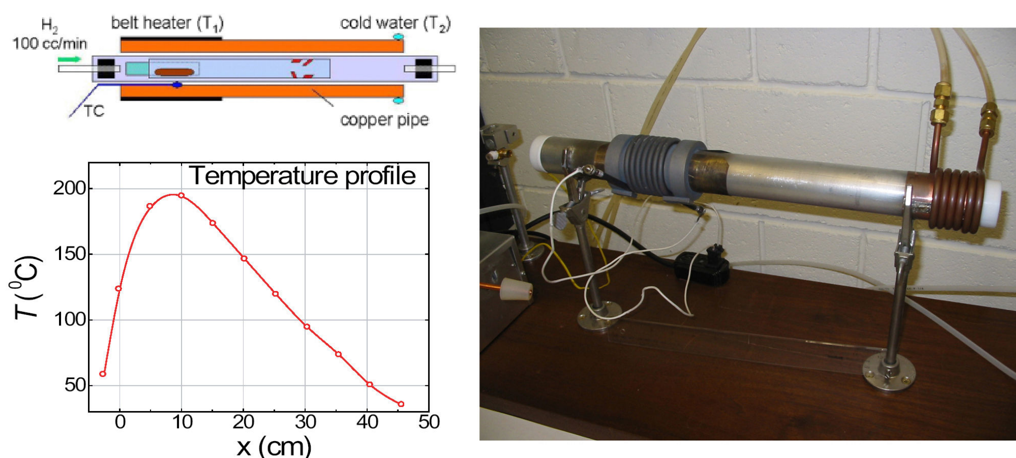


Figure 5.3: Schematic and optical image of a typical crystal growth system. Organic material sublimes at temperature T1, is transported through the system by the carrier gas and recrystallizes in the cooler end of the reactor. Heavy impurities (with a vapor pressure lower that that of the pure organic compound) remain at the position of the source material. Light impurities (with a vapor pressure higher than that of the pure organic compound) condense at a lower temperature, *i.e.* at a different position from where the crystals grow. Therefore, the crystal growth process also results in the purification of the material. *(Image from Vitaly Podzorov)*

drogen has been chosen after comparison of the field-effect characteristics of rubrene crystals grown in Ar, N_2, and H_2 atmospheres. It is unclear at present how exactly the transport gas affects the crystal quality; uncontrollable variations of the crystal quality might be caused by the residual water vapor and oxygen in the reactors. Photoinduced reactions with O_2 are known for most organic molecules[109] and the products of these reactions can act as traps for charge carriers. To minimize possible photo-activated oxidation of organic material, the reactors should be pumped down to a reduced pressure P $\backsim 10^{-2}$ mbar prior to the crystal growth, and the growth should be performed in the dark.

Several factors affect the growth process and the quality of the crystals. Important parameters are, for instance, the temperature in the sublimation zone (T_{sblm}) and the gas flow rate. Many other factors can also play a role: *e.g.*, acoustical vibrations of the reactor in the process of growth might affect the size, shape, and quality of the crystals. For each material and each reactor, the optimal parameters have to be determined empirically. At least in one case (the rubrene-based OFETs[108]), it has been verified that the slower the growth process, the higher the field-effect mobility. For this reason, the temperature of sublimated organic material was chosen close to the sublimation threshold. The crystal growth in this regime proceeds by the flow of steps at a very low rate (5×10^{-7} cm/s in the direction perpendicular to the a-b plane), and results in a flat surface with a low density of growth steps.[105] As an example, sublimation of 300 mg of starting material can take up to 48 hours at T_{sblm} = 300 ^{o}C.[108] Another important

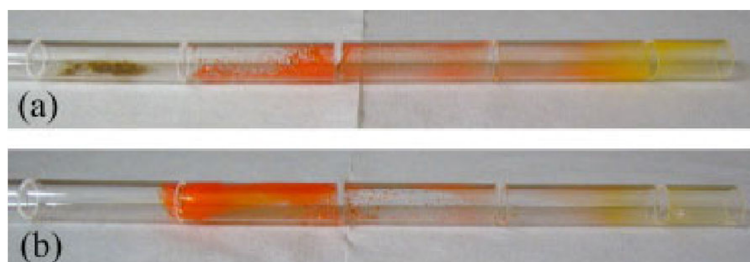


Figure 5.4: **(a)** Result after first regrowth of as-purchased organic material. Purified crystals are visible in the middle; the dark residue present where the source material initially was and the light (yellow) material visible on the right are due impurities. **(b)** At the end of the second regrowth no dark residue is present at the position of the source material, which demonstrate the purifying effect of the growth process.[87]

parameter is the purity of the starting material. As the crystal growth process also results in the chemical purification of the material, several re-growth cycles may be required for improving the field-effect mobility, with the grown crystals used as the starting material for the subsequent re-growth. The number of required re-growth cycles depends strongly on the purity of starting material. Figure 5.4 illustrates the need for several re-growth cycles in the process of the growth of tetracene crystals. Despite the nominal 98 % purity of the starting tetracene (Sigma-Aldrich), a large amount of residue left in the sublimation zone after the first growth cycle is clearly visible (Figure 5.4a); this residue is not present at the end of the second growth cycle (Figure 5.4b). A word of caution is appropriate: in the authors' experience, different batches of as-purchased material, though being of the same nominal purity, might leave different amount of residue. Clearly, the better purity of the starting material, the fewer re-growth cycles are required for a high FET mobility: rubrene OFETs with $\mu > 5$ cm^2/Vs have been fabricated from the 'sublimed grade' material (Sigma-Aldrich) after only 1∽2 growth cycles.[108]

Most of the organic crystals grown by the physical vapor transport are shaped as elongated 'needles' or thin platelets (see figure 5.5). The crystal shape is controlled by the anisotropy of inter-molecular interactions: for many materials, a larger crystal dimension corresponds to the direction of the strongest interactions and, presumably, the strongest overlap between p-orbitals of adjacent molecules. For this reason, the direction of the fastest growth of needle-like rubrene crystals coincides with the direction of the highest mobility of field-induced carriers (see Sec. 3). For platelet-like crystals, the larger facets are parallel to the a-b plane. Typical in-plane dimensions range from a few square millimeters for rubrene to several square centimeters in the case of anthracene. The crystal thickness also varies over a wide range and, in most cases, can be controlled by stopping the growth process at an early stage. For example, the thickness of the tetracene crystals grown for 24 hours ranges between 10 mm and 200 mm,[110] but it is possible to harvest several crystals of sub-micron thickness by stopping the growth process after 30 minutes.

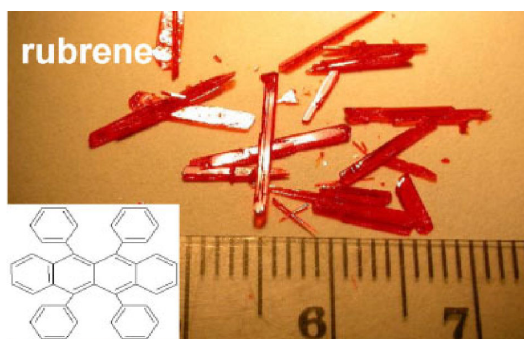


Figure 5.5: Result of rubrene crystal growth. Most of the organic crystals grown by the physical vapor transport are shaped as elongated 'needles' or thin platelets. *(Image from Vitaly Podzorov)*

5.3 Field Effect Transistor Devices

The fabrication of the field-effect structure on the surface of organic crystals poses a challenge, because many conventional fabrication processes irreversibly damage the surface of van-der-Waals-bonded organic crystals by disrupting molecular order, generating interfacial trapping sites, and creating barriers to charge injection. For example, sputtering of an insulator onto the crystal creates such a high density of defects on the organic surface that the field-effect is completely suppressed. Up to date, two techniques for single-crystal OFET fabrication have been successfully used: (a) electrostatic 'bonding' of an organic crystal to a prefabricated source/drain/gate structure, and (b) direct deposition of the contacts and gate insulator onto the crystal surface. In this section, we address the technical aspects of these fabrication processes.[87]

5.3.1 Electrostatic Bonding Technique

In this approach, the transistor circuitry (both gate and source/drain electrodes) is fabricated on a separate substrate, which, at the final fabrication stage, is electrostatically bonded to the surface of an organic crystal. The source/drain/gate structure is fabricated on the surface of a heavily doped (n-type or p-type) Si wafer, covered with a layer of thermally grown SiO_2 (typically, 0∽2 mm thick). The conducting Si wafer serves as the gate electrode, and the SiO_2 layer plays the role of the gate insulator. The source and drain gold contacts are deposited on top of the SiO_2 layer, and, as a final step, a sufficiently thin organic crystal is electrostatically bonded to the source/drain/gate structure. It has been found that the reactive ion etching (RIE) of the contact/SiO_2 surface in the oxygen plasma prior to the OMC bonding improves significantly the characteristics of tetracene OFETs:[106] the RIE cleaning reduces the spread of mobilities,

the field-effect threshold voltage, and the hysteresis of transfer characteristics. The RIE cleaning also significantly improves adhesion of freshly grown tetracene crystals to SiO_2 surface. The technique works best for very thin crystals (1 mm thick) that adhere spontaneously to the substrate, but it can also be applied (with a lower success yield) to much thicker crystals by gently pressing on the crystal to assist the adhesion process. Figure 5.6 shows a picture of a rubrene FET fabricated with the technique of electrostatic adhesion to SiO_2.

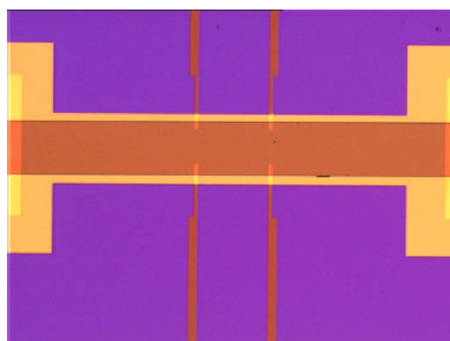


Figure 5.6: Optical microscope picture of a single-crystal rubrene FET, fabricated by electrostatic bonding. The crystal, which has a rectangular shape, overlaps with the source and drain contacts (at the left and right edge of the picture) and with four small contacts in the center, used to perform 4-probe electrical measurements. The purple area consists of a Ta_2O_5 layer sputtered on top of the substrate prior to the crystal bonding, which, for wider crystals, serves to confine the electrically active region of the FET.[106]

5.3.2 Parylene Dielectric

High performance OFETs devices can also be realized by direct evaporation, through a shadow mask, of the source and drain electrodes directly on the top surface of a rubrene single crystal.[108] Then, a thin electrically insulating parylene film is deposited on top to form the gate insulator. Unexpectedly, the exposed channel area of the organic semiconductor is not significantly damaged during this deposition process provided that the sample if sufficiently far away ($\geq$ 35 cm) from the pyrolysis zone of the parylene reactor. To avoid any gate leakage, the parylene film needs to be relatively thick ($\backsim$1 μm thick) in order to efficiently cover all defects present on the crystal top surface. The device fabrication is completed by shadow evaporating a top gate electrode. An optical image of such a device is presented on figure 5.7 together with its electrical characteristics. Analysis of the transfer curves slope indicate field-effect mobilities as high as $\backsim$8 cm^2/V$\cdot$s for the best devices. In these devices, the threshold voltage depend on the applied gate bias indicating that their is a built in, electrostatically inducted, channel. The variation of the device field effect mobilities with the applied source-drain bias indicates that the transistor operation is limited by the quality of the interface between the semiconductor and the deposited

parylene dielectric.

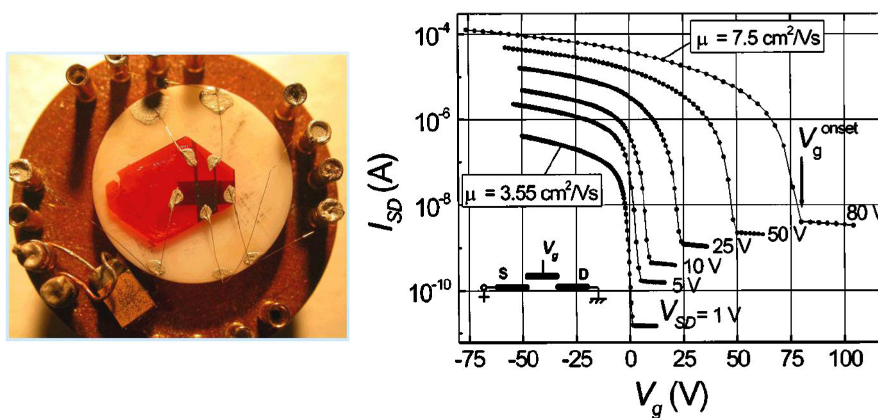


Figure 5.7: Optical microscope picture of a single-crystal rubrene FET using parylene as a gate dielectric. Electrical contact to the shadow silver electrodes are realized using silver paint.[108]

Chapter 6

Reversible Probing of Charge Transport in Organic Crystals

We introduce a novel method to fabricate high-performance field effect transistors on the surface of free-standing organic single crystals: the transistors are constructed by laminating a monolithic elastomeric transistor stamp against the surface of a crystal . This method, which eliminates exposure of the fragile organic surface to the hazards of conventional processing, enables fabrication of rubrene transistors with charge carrier mobilities as high as $\backsim$ 15 cm^2/V·s and sub-threshold slopes as low as 2 V·nF/decade·cm^2. Multiple re-lamination of the transistor stamp against the same crystal does not affect the transistor characteristics; we exploit this reversibility to reveal anisotropic charge transport at the basal plane of rubrene.

Basic scientific interest and potential applications in large-area, flexible electronic systems motivate research in the field of organic semiconductors.[55,111–113] Despite a substantial body of work aimed at understanding charge transport in these materials,[106–108,114–117] a well-developed, microscopic description is still lacking. It is for this reason that studies of organic single crystals, in which grain boundaries are eliminated and concentration of charge traps is minimized, are important. A primary experimental difficulty is that the field-effect structures which are needed for these measurements require fabrication steps that can disrupt molecular order and bonding, generate interfacial trapping sites, create barriers to charge injection and cause other unwanted changes to these fragile molecular systems.[118] There is, therefore, a strong need for non-destructive, reversible methods to fabricate field effect transistors (FETs) based on single crystals of organic semiconductors in a way that reveals intrinsic properties and removes processing-related effects.

6.1 The Soft 'Transistor Stamp' for Probing Organic Single Crystals

In our technique, the transistor circuitry (the source/drain/gate electrodes and gate dielectric) is fabricated on a flexible elastomeric substrate, which, at the final stage, is bonded to the surface of organic crystal by van der Waals forces. In this respect, our technique is similar to fabrication of organic FETs by laminating an organic crystal against a silicon wafer with pre-deposited electrodes.[106,115] The main advantage of both elastomeric and Si-based stamp techniques is obvious: they eliminate the need for deposition of metals and dielectrics directly onto a very fragile organic surface. The elastomeric technique, however, compares favorably with the Si-based technique in two important aspects. Firstly, in contrast to Si-based substrates that require very thin ($\backsim 1\ \mu$m) and bendable crystals (which are prone to strain-induced defects), the elastomeric stamps are compatible with much thicker (up to a few mm) and rigid crystals: the flexible elastomeric surface and the ductile Au contacts adjust easily to the crystal shape. Secondly, the elastomeric stamp technique is non-destructive and reversible: the contact between the stamp and organic crystals can be re-established many times without affecting the transistor characteristics. We exploit this experimental capability to explore the dependence of the field effect mobility on the orientation of the transistor channel relative to the crystallographic axes, and observed for the first time a strong anisotropy of the field-effect mobility within the *a*-*b* plane of single crystals of rubrene.

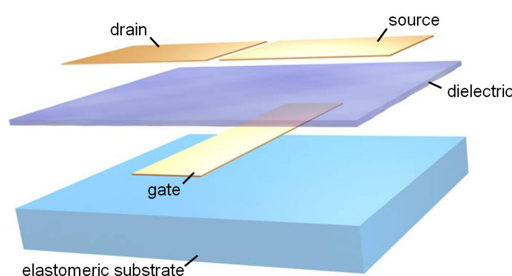


Figure 6.1: Schematic view of a transistor stamp with gate, dielectric, and source and drain electrodes sequentially deposited onto a PDMS substrate.

Figure 6.1 shows the transistor stamps used and outlines the steps of device fabrication. A flexible elastomer, polydimethylsiloxane (PDMS), is used as a substrate on which the transistor stamp is constructed. Gate and source/drain electrodes (Ti/Au) are evaporated through shadow masks and are separated by an additively transferred thin film (2-4 μm) of PDMS.[119] The flexibility of the both the dielectric and substrate (and therefore all the gold electrodes in these transistor stamps) enables assembly of devices through simple lamination of the organic crystal and elastomeric stamp surface. Slight pressure applied to one edge of the crystal initiates contact with the stamp (Figure 6.2); van der Waals forces then spontaneously cause a 'wetting'

front to proceed across the surface of the crystal (Figure 6.2 central frame). The low free-surface energy of PDMS favors the progression of such a wetting front[120,121] across the flat surfaces of organic crystals. The absence of interference fringes (as observed through a high-resolution optical microscope) suggests an atomic-scale, intimate contact of the semiconductor with the electrodes[56,122] and the elastomeric gate dielectric,[123] consistent with electrical measurements described below.

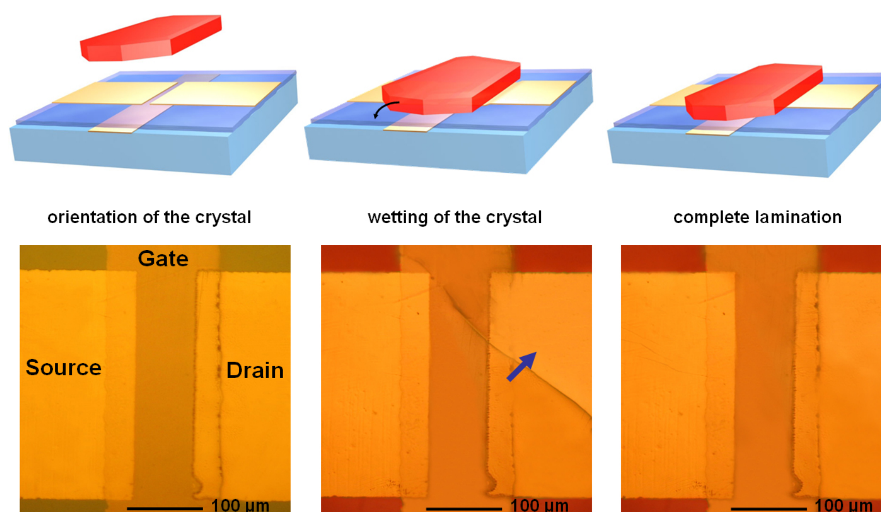


Figure 6.2: Transistor fabrication by lamination of an organic crystal against the transistor stamp. Initiating contact (first frame) between these two surfaces results in a 'wetting' front that progresses across the semiconductor-stamp interface (second frame), until the entire crystal is in intimate contact with the stamp (final frame). The right insets show optical micrographs of three stages of this process. The arrow in the middle inset marks the progression of the wetting front.

The ease of this assembly process and its inherently noninvasive nature enables systematic analysis of the semiconducting properties of pristine organic crystals. The present work focuses on high-purity crystals of rubrene (Figure 6.3a), synthesized using a physical vapor transport technique.[105,107] This material forms an orthorhombic crystal with herringbone molecular packing. Figure 6.3b shows the relative orientation of rubrene molecules in the basal (a-b) plane of the crystal; the lattice constants along a and b axes are 14.4 and 7.2 Å, respectively. Slower crystal growth along the c-axis results in the formation of thin platelets, 0.2-1.0 mm thick and 2-3 mm wide, with the natural large-area flat facet being the (001) a-b plane. The FETs are built by lamination on these surfaces. Images collected through crossed polarizers indicate that the crystals grown in this fashion are single crystalline (Figure 6.3c).[124] The natural facets of the crystals match the crystallographic directions obtained from Laue diffraction profiles (Figure 6.3d).

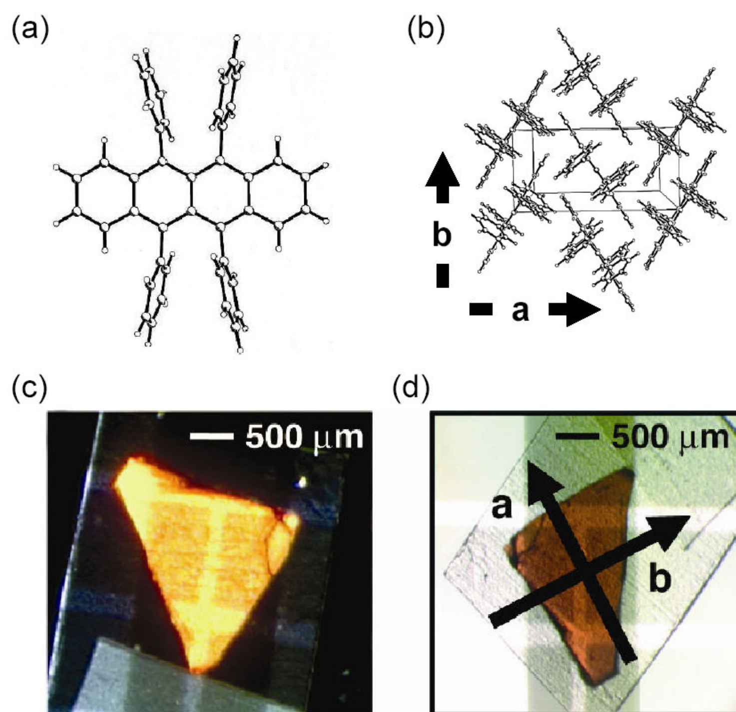


Figure 6.3: **(a)** Molecular structure of rubrene. **(b)** Orthorhombic, crystallographic structure of a single crystal of rubrene shows the enhanced π-π overlap along the *b* direction and reduced overlap along the a direction. **(c)** Optical micrograph of a sample viewed through crossed polarizers **(d)** Natural facets on the crystal surface correspond well to the crystallographic data and enable easy identification of the *a* and *b* axes confirmed by Laue diffraction.

6.2 Charge Transport in a Rubrene Single Crystal

Figure 6.4a shows current-voltage characteristics of a representative device. Strong field effect modulation of the channel conductance is observed, with on/off current ratios as high as 10^6 (measured between V_G= -100 V and 20 V). By fitting the data to linear and saturation regime standard FET equations (22), two-probe mobilities μ= 3-9 $cm^2/V{\cdot}s$ were obtained for different rubrene crystals. The highly ohmic current-voltage characteristics at low source-drain bias (Figure 6.4a inset), together with nearly equal values of the mobility extracted from the linear and saturation regimes, are consistent with a relatively low Schottky barrier to hole injection and thus low contact resistance. Transfer characteristics of such devices yield sub-threshold slopes ∽3-5 V/decade (corresponding to the intrinsic sub-threshold slope 2-4 $V{\cdot}nF/decade{\cdot}cm^2$)[107] and show near threshold-less operation and weak gate voltage dependence of the channel mobility. Minor hysteresis observed in forward and reverse scans suggest a low density of deep traps at the interface. These excellent transistor characteristics result from the high quality of the laminated rubrene-PDMS interface and the high purity rubrene crystals.

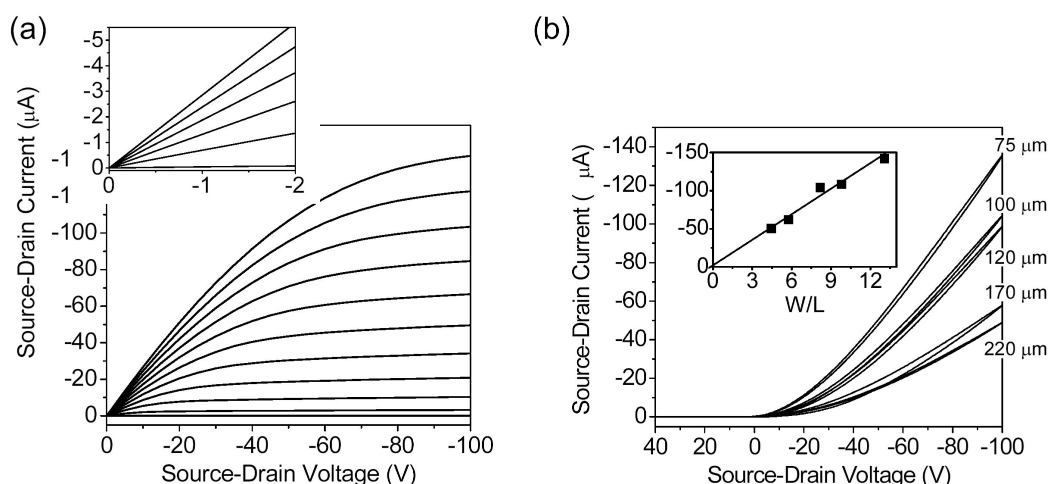


Figure 6.4: **(a)** Current-voltage characteristics of laminated rubrene-transistor stamp assemblies (L= 75 μm, W= 980 μm, Ci= 0.67 nF/cm^2). Typical FET behavior, with well resolved linear and saturation current regimes, is observed. The channel is normally 'off' and turns on at successively more negative gate voltage (from +20 to -100 V). The graph in the inset shows the behavior at low V_{SD}. Highly ohmic behavior is evident at all gate voltages. **(b)** Transfer characteristics measured at V_{SD}= -100 V in the same region of one single crystal by forming, one after another, contacts with transistor stamp structures that define different channel lengths (L= 220, 170, 120, 100 and 75 μm, W= 980 μm). Similar mobilities and sub-threshold slopes are seen for all devices (3.4 $\pm$ 0.3 cm^2/V·s and 2.5 $\pm$ 0.3 V·nF/decade·cm^2 respectively). As a result, the inset shows linear scaling of saturation currents with *W/L*.

Because the adhesion of the PDMS elastomer to the organic is driven primarily by van der Waals forces and not by irreversible bond formation, separation of the elastomeric stamp from the organic crystal does not degrade the crystal surface provided these forces are weaker than the intermolecular bonding. This is the case for rubrene: there are no substantial changes in channel conductance even upon multiple re-lamination of the stamp. This reversibility is important because, unlike previous efforts,[106–108,115] it enables different high-performance transistor structures, each with different electrode configurations, to be assembled sequentially on the same region of the crystal surface. Figure 6.4b shows, as an example, data collected from a set of devices with different channel lengths assembled one after another on a single small region of the crystal surface. Variations of the device characteristics (mobility, etc.) were within 15%. As a result, the saturation current observed in Figure 6.4b inset shows the expected width/length (W/L) scaling.

6.3 Anisotropy of the Charge Transport at the Basal Plane of a Rubrene Single Crystal

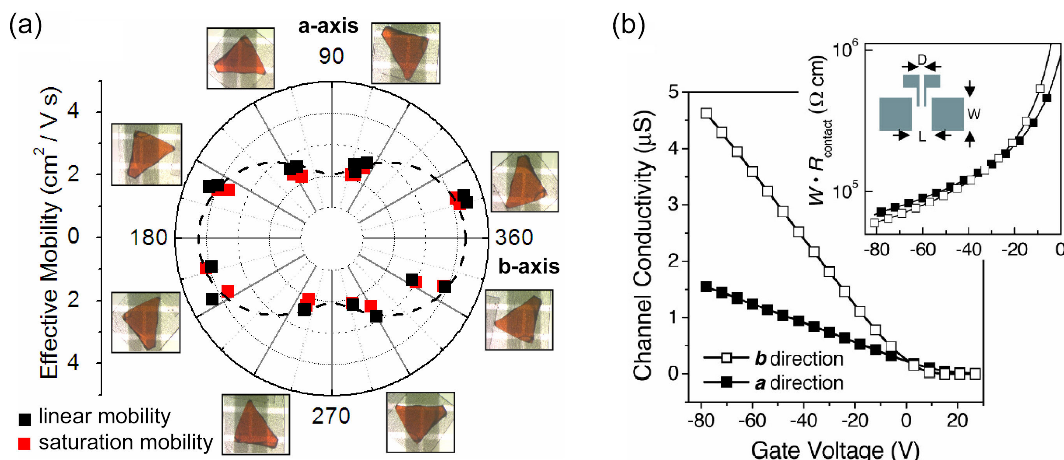


Figure 6.5: **(a)** Polar plot of the mobility at the rubrene *a*-*b* surface (angle measured between the *b* axis and the conducting channel). The linear and saturation mobilities (black and red squares respectively) are similar and are seen to be coincident after each full 360° rotation. The maximum and minimum mobility values occur along *b* (180° and 360°) and a (90° and 270°) axis, respectively. The dotted line shows the fitted in plane transformation of the mobility tensor. **(b)** Four-probe conductivity as a function of gate voltage along the *b* and *a* axes. Intrinsic mobilities measured along the *b* and *a* axes are 15.4 cm^2/V·s and 4.4 cm^2/V·s respectively. The inset plots the contact resistance along the *a* and *b* direction.

By performing experiments with the same source/drain configuration but with different angular orientations of the crystal relative to the channel, it is possible to examine mobility anisotropy. Figure 6.5a presents results of such measurements, in which the crystal was rotated and re-laminated through 720°, in a step-wise fashion. After each rotation the 2-probe mobility was measured in both linear and saturation regime to exclude the contact effects. Reproducibility of the results after two full 360° rotations demonstrates that re-lamination does not damage the crystal surface. The effective two-probe mobilities for charge transport along the crystallographic *a* and *b* axes differ at least by a factor of two, with the highest mobility along the *b* axis. The angular dependence of the mobility variation is consistent with tensor transformation rules for an orthorhombic crystal (Figure 6.5a, dashed line).[125] All investigated samples showed similar behavior (6 samples taken from different crystal and transistor stamp syntheses) and highlighted the non-invasive nature of this technique.

To completely eliminate the contact effects and to extract intrinsic hole mobilities, we utilized stamps with a four-probe configuration of electrodes (Figure 6.5b, inset).[107,108,126] In this experiment, the potential difference between two voltage contacts located inside the channel,

V_{4W}, was measured as a function of gate voltage simultaneously with the source-drain current, I_{SD}. The conductivity, $\mu = I_{SD}/V_{4W}$, is plotted as a function of V_G for the transport along the *a* and *b* crystallographic directions (Figure 6.5b). The slope of the $\mu(V_G)$ dependences in the linear regime is proportional to the intrinsic hole mobility μ_{4W} in rubrene.[126]

Intrinsic hole mobiliy $\mu_{4W} = \frac{D}{W \cdot C_i} \frac{\partial \sigma}{\partial V_G}$

with D: distance between the voltage probes
W: channel width
C_i: capacitance of the gate dielectric
V_G: gate volatge bias

Again, this mobility is dramatically different along the *a* and *b* axis (4.4 $cm^2/V \cdot s$ and 15.4 $cm^2/V \cdot s$, respectively). Contact resistance $R_{contact}$ extracted from this data (Figure 4b inset) vary with V_G in a similar fashion along both crystallographic directions. These results show that the observed mobility anisotropy in the two-probe measurements indeed reflects the specific crystal structure.

Contact resistance $R_{contact} = \frac{V_{SD}}{I_{SD}} - \frac{L}{D} \frac{V_{4W}}{I_{SD}}$

While it is known that organic single crystals are highly anisotropic,[114] manifestations of these effects in field effect experiments have not been previously reported. Our observation that the maximum mobility is realized for hole transport along the *b* axis is qualitatively consistent with molecular packing in the rubrene crystal (Figure 6.3a), for which one might expect a stronger overlap of the electronic π-orbitals along the *b* axis (Figure 6.3b). The different lattice constants along the *a* and *b* axes (14.4 Å versus 7.2 Å) and the anisotropic character of inter- and intra-molecular vibrational modes are also likely to contribute to the observed anisotropy. Qualitatively, our finding agrees with the theoretically predicted mobility anisotropy in molecular crystals based on differences in transfer integrals along different crystallographic axes;[127] however, for a more quantitative analysis, polaronic effects in rubrene and other polyacenes should be included.[128]

These results suggest that future field-effect experiments at organic crystal surfaces should consider mobility anisotropy, and highlight the importance of controlling the orientation of the organic crystal relative to the FET channel. More broadly, the reversible lamination of transistor stamps, demonstrated in this report, provides simple two- and four-probe stamps that could be effectively used to extract spatial channel characteristics in a single grain, as well as across the grain boundary of organic semiconductors.[129] The reversible formation of the interface between the PDMS dielectrics and organic surface allows for a reliable interpretation of these results and enables a better understanding of charge transport in organic semiconductor. More generally this technique could facilitate studies of operation-induced changes in transport prop-

erties by providing access to interfaces that are irreversibly embedded in conventional devices.

6.4 Experimental section

6.4.1 Materials and Methods:

Casting and curing Sylgard 184 PDMS (Dow Corning; 1:10 w/w, cross linker and base) against a cleaned Si wafer (treated with (Tridecafluoro-1,1,2,2-tetrahydrooctyl)trichlorosilane (Gelest, Inc.) to produce a non-stick surface) yields a flat substrate for the transistor stamps. Evaporating (2 nm (0.3 nm/s) / 20 nm (1 nm/s) / 3nm (0.3 nm/s) of Ti/Au/Ti respectively (Temescal BDJ-1800 electron beam evaporator), onto this substrate (briefly treated with an oxygen plasma) through a shadow mask defines the gate electrode (electrode width = 1.0 – 1.5 mm). Separately, PDMS was diluted in trichloroethylene (1:3 or 1:4 w/w), spin-cast (5000 rpm) onto a PDMS substrate that had been treated with oxygen plasma and (Tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane and cured at 120 °C for 6 hours on a hotplate. This process yields PDMS films with thicknesses between 2 and 4 microns. Oxygen plasma treatment of the PDMS dielectric surface and the gate electrode substrate for 10 s, followed by laminating these two surfaces together forms irreversible bonds (condensation reaction between titanol and hydroxy groups) that effect transfer of the PDMS dielectric to the gate electrode substrate. Samples that showed imperfect transfer (bubbles or ripples) were discarded. Source-drain electrodes were evaporated through shadow masks (Ti/Au; 2 nm/20 nm respectively) on top of the dielectric to complete the fabrication of the transistor stamp. Careful control of the fabrication processes results in electrode and dielectric surfaces with low surface roughness (root mean squared values of 0.6 nm for both surfaces, as measured by atomic force microscopy). Lamination of the stamp (under ambient conditions and in air) against the surface of a freshly grown rubrene crystal produces a complete transistor. The rear side of the rubrene crystal was mounted on a piece of scotch tape for ease of handling.

6.4.2 Transistor Characterization:

A single transistor stamp typically supported several pairs of source/drain electrodes for a range of transistor channel widths (W) and lengths (L) with a common gate and gate dielectric. The capacitance of the dielectric (0.2-0.8 nF/cm2, depending on the thickness of the film) was determined by measurements on capacitor test structures formed near the active region of the stamps (HP 4284A Precision LCR meter, 100 Hz, 2 V bias). We observed very small leakage through these dielectrics (1-5 nA/mm^2 at 1 MV/cm); they exhibited small or negligible frequency dependence in their capacitance over the range investigated (less than 3% variation between 50 Hz and 1 MHz). Current-voltage measurements were collected using a semiconductor parameter analyzer (Agilent 4156C). These measurements show characteristic transistor behavior with

well resolved linear and saturation regimes. Transfer characteristics for these devices were obtained at V_{SD}= +20 V (linear regime) and V_{SD}= -100 V (saturation regime) and show almost thresholdless behavior. They yield sub-threshold slopes 3-5 V/decade which correspond to intrinsic (scaled by the dielectric capacitance) sub-threshold slopes of 2-4 V·nF/decade·cm^2.

Chapter 7

'Air-Gap' Stamps

7.1 Background: Need for a New Test Structure

Study of intrinsic transport properties in single crystal organic semiconductors has the potential to yield fundamental insights into the behavior of plastic transistors for flexible electronics.[78,130–132] The organic field effect transistors (OFETs) that facilitate these studies are, however, complex structures whose properties depend on interactions between the semiconductor, gate dielectric and electrodes.[31,111,133] Carrier trapping, charge doping, molecular reorientation, dipole formation and a range of possible chemical interactions are among the many phenomena that can occur at the semiconductor/dielectric interface to degrade device performance.[107,108,110,134,135] We introduce an unusual device design that avoids these effects entirely by replacing the standard solid dielectric layer with a thin free space gap that can be filled with air, nitrogen, other gases or even vacuum. When combined with high-quality organic crystals, this design reveals the ultimate in OFET performance, determined solely by the intrinsic (not limited by disorder) polaronic transport on the pristine surface of the crystals. We demonstrate this approach by building *p* and *n* channel devices with performance characteristics – mobilities and normalized sub-threshold slopes – that establish new record values for organic transistors.

Unlike the effects associated with electrical contacts, which can be subtracted from the device response by four point probing or channel length scaling analysis, it is difficult or impossible to predict or account for interactions between a semiconductor and a conventional material dielectric.[115,136] The free space dielectric simply eliminates these effects by eliminating the dielectric insulating material. It is uniquely well suited to the study of organic semiconductors, which do not possess the types of dangling bonds or surface states that are present in many inorganic materials.

7.2 The 'Air-Gap' Stamp

7.2.1 Fabrication of the Air-Gap Stamp

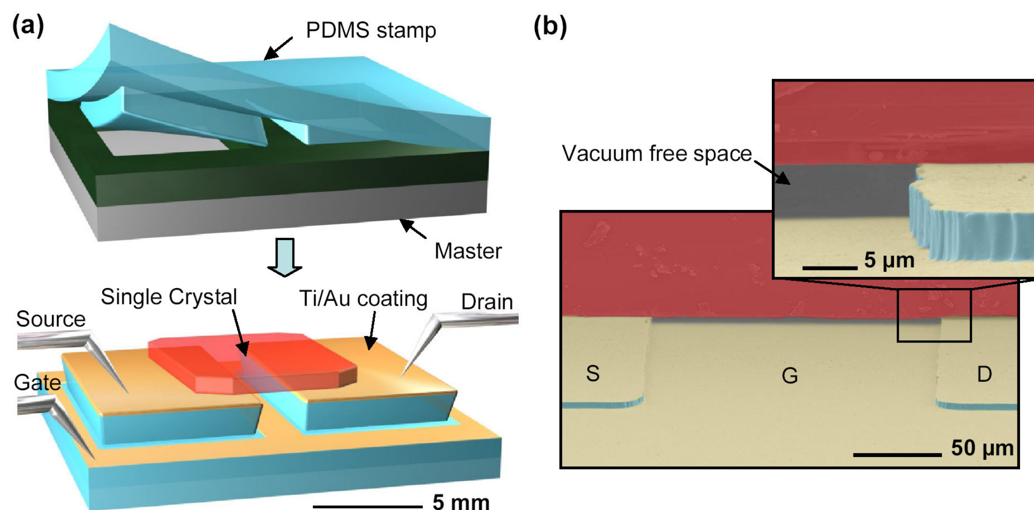


Figure 7.1: Organic single crystal transistors with free space gate dielectrics. **(a)** Schematic illustration of steps for producing the device. **(b)** Scanning electron micrograph of such a device that uses a single crystal of rubrene.

Figure 7.1a schematically illustrates the steps for building these devices. Casting and curing a pre-polymer of poly(dimethylsiloxane) (PDMS; Sylgard 184, Dow Corning Corp.) against a pattern of photoresist (SU8, Microchem Corp.) on a silicon wafer defines an elastomeric element with relief features in the geometry of the resist. Coating this element with a collimated flux of metal generates electrically isolated electrodes on the raised and recessed regions. This single processing step defines source and drain (raised regions) electrodes together with a self-aligned gate (recessed region) electrode. The size of the electrodes and their separation are limited only by the resolution of soft lithographic casting and curing procedures: dimensions as small as a few tens of nanometers are possible.[19] Gently placing a single crystal sample on the surface of such an element leads to soft, van der Waals contacts to the source/drain electrodes. The crystal itself forms a free standing bridge that spans the gap between these electrodes. The thin space between the bottom surface of the crystal and the gate electrode plays the role of the gate dielectric. This space can be filled with any gas (e.g. air) or by vacuum, depending on experimental conditions implemented during or after device assembly. Figure 7.1b shows a scanning electron micrograph of a rubrene single crystal laminated on top of a Ti/Au (2 nm/20 nm) coated elastomeric element. The dielectric is vacuum in this case.

7.2.2 Characterization of the Stamp Electro-Mechanical Properties

These transistors rely critically on acceptable electrical behavior of this unusual type of gate dielectric. The low (3 V/μm) dielectric strength of most gases together with the low modulus (2-5 MPa) of the elastomer might suggest that devices with this design would be suitable only for very low electric field operation. Our results show, however, that this inference is incorrect for two reasons. First, the breakdown fields for air gaps which are much narrower than the mean free path of an air molecule can be exceptionally high owing to suppression of the avalanche phenomena that generate discharges in unrestricted geometries.[137] We observed, in agreement with Paschen’s law for atmospheric pressures, breakdown voltages greater than 100 V with air gaps as narrow as 1.8 μm. In fact, breakdown of the PDMS (rather than the air) caused by fringing fields at the edges of the device can limit the operating voltages. Second, even relatively large electric fields applied to gaps with these dimensions are insufficient to deform the elastomer.

7.2.2.1 Stamp mechanical distortion when subjects to electrostatic forces

The high aspect ratio of the built test structures enabled us to perform the finite element simulations using a simple 2D plane model approximation. Figure 7.2 shows a magnified view of the different sub-domains of the modeled system (the defined model is actually larger, it is here cropped to highlight the contour definition of the modeled air gap cavities).

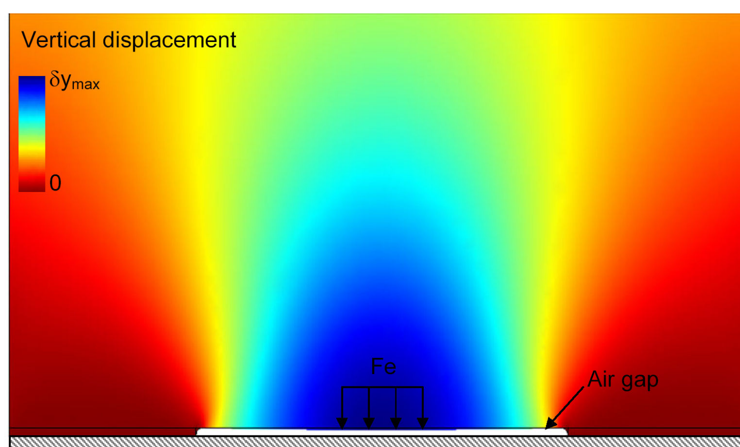


Figure 7.2: Finite element plane model of the electro-mechanical compression of the air gap structure.

A non-slip boundary condition was assumed at the interface between the PDMS stamp and the metal coated glass slide. The PDMS material was assumed to be isotropic with a Young’s modulus of 3 MPa and a Poisson ratio of 0.48. The pressure values of the electrostatic forces

were computed on each point of the PDMS 'roof' boundary using an analytical expression:

$$Fe/A = \frac{\epsilon_0 V_0^2}{2(h-\delta y)^2}$$

with: $\epsilon_0 = 1$: air or vaccum dielectric constant
V_0 : applied gate bias voltage
h : initial air gap thickness
δy : local variation of the air gap thickness

The simulations results (Figure 7.3a indicate that gate biases of 100 V compress air gaps thicker than 3 μm (50 μm wide) by less than ∽ 4 nm. We verified experimentally these finite element modeling results by measuring the variation of the air capacitor when a high voltage bias is applied between a metal coated glass slide (laminated on the stamp) and the soft PDMS 'roof' electrode. Figure 7.3b demonstrate that test structures with air gaps even as thin as ∽ 1.8±0.03 μm exhibit tiny variations in capacitance ($< 0.2\%$) for bias voltages up to 40 V (limited by the instrument output voltage capability). As a result, we can assume (with a very good approximation) that the air-gap stamp has a constant dielectric value which is independant of the applied voltage on the FET gate electrode.

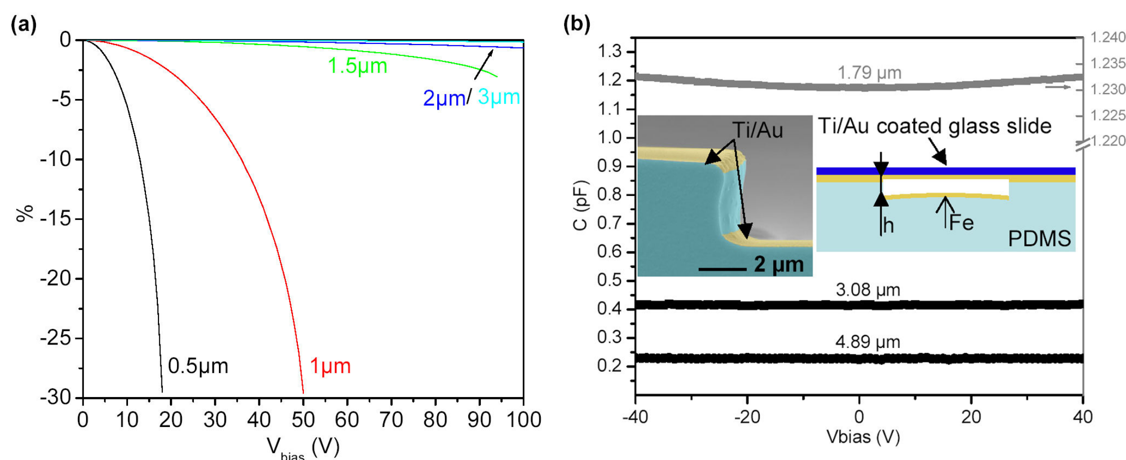


Figure 7.3: **(a)** Compression of the air gap cavity subject to compressive electrostatic pressure forces (W= 50 μm). **(b)** Capacitance-voltage dependences measured for different air dielectric thicknesses for the test structures with 50 μm × 1.8 mm in-plane dimensions. The 1.79 μm results are plotted using the expended vertical axis to give more details on the capacitance variations. The voltage-independent capacitance and the ability to withstand high voltages are two important features for applications as gate dielectrics.

7.2.2.2 Finite element modeling of the electrostatic fringes fields

The magnitude of the capacitance, which includes contributions from fringing fields that pass through the elastomer, can be accurately predicted by finite element modeling of the electrostatics. Similarly, we used a simple 2D plane model (plane strain assumption) to simulate the influence of the electrostatic forces on the soft PDMS structure. Figure 7.4 shows a magnified view of the different elements of the modeled systems (again the defined model is actually larger). A dielectric constant of 1 was used for the air material and 2.8 for the PDMS areas located on both sides and underneath the air cavity. The bottom boundary of the air gap was grounded and the top boundary assigned a fixed potential V0. All the other boundaries of the systems where assigned a neutral boundary condition (continuity of the electric field). The capacitor values were computed (integrated in each sub-domain) using a stored energy method: $C = 2 \cdot We/V_0^2$. Values computed in the vicinity of the air gap area were within 1% of values obtained using a standard plane capacitor model confirming the accuracy of the used integral method.

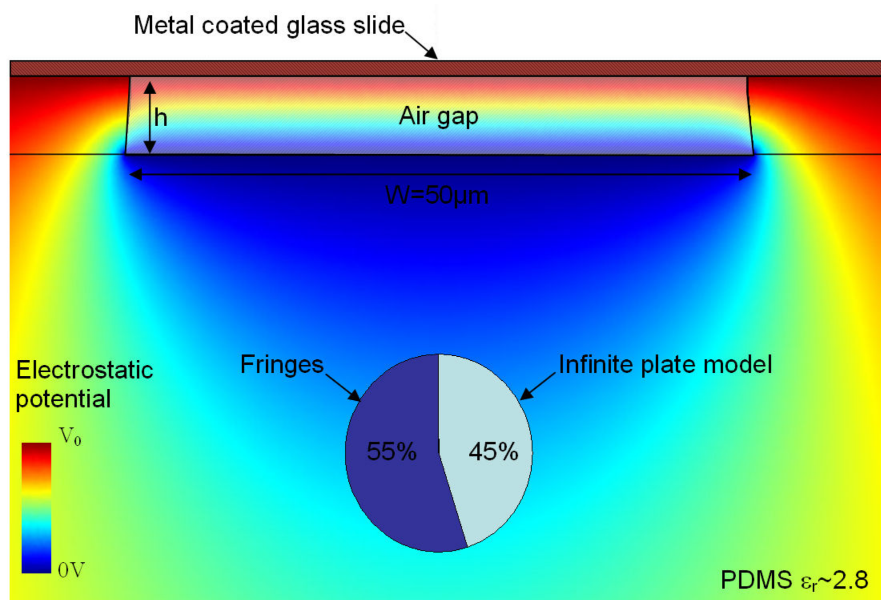


Figure 7.4: Finite Element Modeling of the electrostatic fringes fields

Ultra long test structures were specifically designed to create a measurable amplitude of the cavity capacitance. Figure 7.5 shows that the experimental results obtained with a HP4155A capacitance meter are in good agreement with FEM simulations (taking into consideration the influence of the fringing fields).

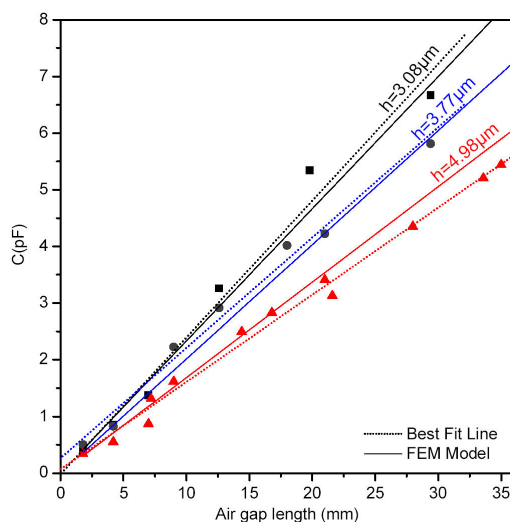


Figure 7.5: Experimental capacitance measurements and finite element modeling of air-gap capacitors increasing linearly with the test structure length (50 μm wide).

For voltages probed in the experiments described here, moderate fields are achieved, corresponding to charge doping at the surface of the organic crystal up to 60 nC/cm^2 or the carrier density up to $4{\cdot}10^{10}$ cm^{-2} ($2{\cdot}10^{-4}$ holes/molecule). It is possible to operate at fields that are ten times larger than these values. The main limitations are breakdown in the PDMS and onset of deformation in the elastomer, which can distort the empty space dielectric in a way that depends non-linearly on the electrostatic and surface forces. This deformation can, in some cases, lead to runaway collapse of the empty space. High modulus materials can eliminate this effect.

7.3 TCNQ and Rubrene Field Effect Transistor Devices

We built transistors with a wide range of channel dimensions and dielectric thicknesses using single crystals of two different molecules: TCNQ and rubrene.

7.3.1 Single Crystal TCNQ Devices

Figure 7.6a shows the molecular structure and crystal packing of TCNQ,[138] which grows with large flat facets oriented perpendicular to the c-axis of the crystal. The device geometry and transistor characteristics, obtained using a 4 point probe transistor geometry[107] and free space dielectric thickness of 4.7±0.1 μm, appear in Figure 7.6b.

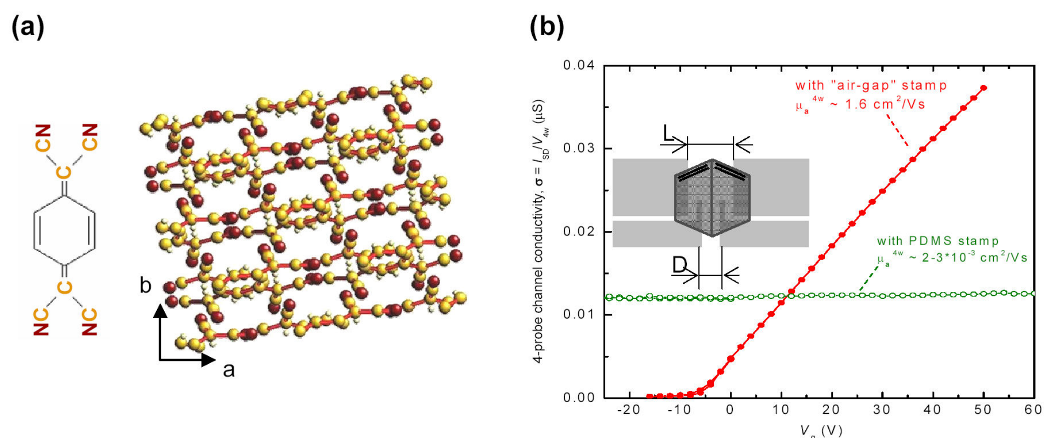


Figure 7.6: **(a)** Molecular structure and crystal packing in TCNQ. **(b)** Gate-dependent channel conductivity along *a*-axis of a TCNQ crystal measured by laminating it on top of elastomeric transistor elements that use vacuum and PDMS as gate dielectrics. Intrinsic carrier mobilities in these devices are 1.6 and 2∽3·10^{-3} cm^2/V.s, respectfully. The vacuum device has a channel length (L) of 1 mm, a channel width (W) of 1.15 mm, a dielectric thickness (d) of 4.7 μm and the distance between voltage probes (D) of 0.39 mm. The PDMS device used L= 1 mm, W= 1.3 mm, D= 0.25 mm, and d∽5 μm.

Here, transport occurs in the *a*-*b* plane. The conductivity of the channel, $\sigma = I_{DS}/V_{4W}$ (I_{DS} is the source-drain current, V_{4W} is the potential difference between the voltage probes),increases with increasing positive gate bias, V_G, consistent with n-type behavior. It represents the first n-channel single crystal organic transistor. The free space dielectric is critical to the successful operation of the device. Attempts to use conventional solid dielectric materials (PDMS, parylene, laminated PET and others) resulted in negligibly small mobilities and on/off ratios. A typical result for the case of PDMS dielectric appears in Figure 7.7b. We attribute the poor performance to trapping and doping due to the interactions between the dielectric and TCNQ, which has a very high electron affinity.[139] Doping associated with the PDMS dielectric leads to a relatively large “off” conductivity and small “on/off” ratio.

Analysis of the response of the device using standard methods for the linear regime yields a gate voltage independent intrinsic carrier mobility of 1.6±0.1 cm^2/V·s and a normalized subthreshold slope of 1.5±0.1 V·nF/decade·cm^2. These values are better by a substantial margin than those of the best thin film organic n-channel transistors.[140] Despite the anisotropic shape of the molecules and their packing in the crystal, the transport characteristics depend only very weakly on orientation of the *a* and *b*-axes of the crystal relative to the transistor channel (as determined by multiple measurements on a large number of TCNQ crystals). The absence of anisotropy is consistent with our observation that at room temperature, the conductivity of TCNQ transistors is still thermally activated and governed by a trap-and-release mechanism.[132]

7.3.2 Single Crystal Rubrene Devices

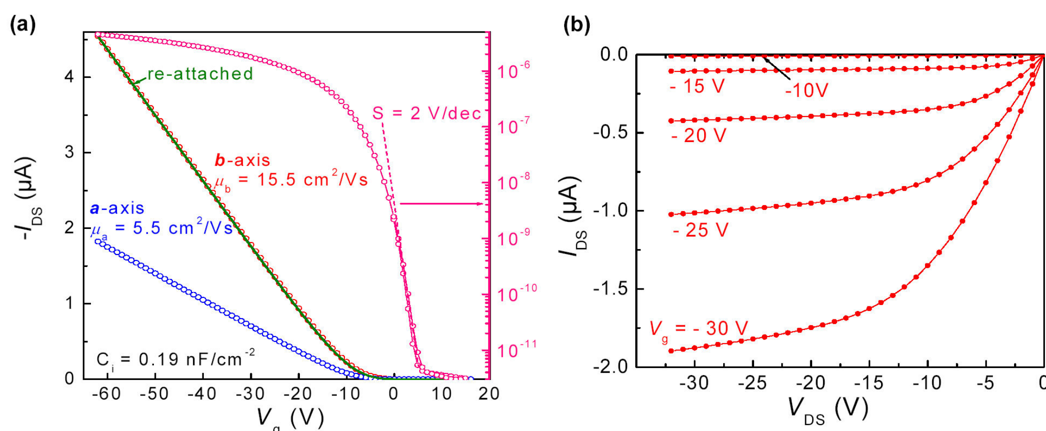


Figure 7.7: Rubrene field effect transistor that uses air as the gate dielectric, with source/drain electrodes oriented along the *a* and *b*-axis of the single crystal. **(a)** The transfer characteristics have been measured at the source/drain voltage V_{DS}= -5 V after the crystal was laminated (circles), peeled back and re-attached (solid line). The transfer characteristic along *b*-axis is also shown in semi-log plot (right axis) (L= 149 μm, W= 1 mm, d= 4.7 μm). **(b)** Current-voltage characteristics measured along *b*-axis (L= 196 μm, W= 1mm, d= 4.7 μm).

Figure 7.7a presents transfer characteristics of rubrene transistors formed with air dielectrics (thickness 4.7±0.1 μm) on the large, flat crystal surfaces that expose the *a*-*b* plane. Effective device mobilities are 13±1 cm^2/V·s along the *b*-axis and 5.5±0.5 cm^2/V·s along the *a*-axis, and on/off ratios are greater than 10^6. These devices, like those built with TCNQ, show no measurable hysteresis (instrument limited change of $\leq$ 0.2% in current for a 60 V cycle). They also exhibit little or no degradation of the transfer characteristics after detaching and then re-attaching a crystal onto the elastomeric element, or during measurements for periods of many hours, and storage for days. The devices behave like ideal long channels transistors[141] with very good quadratic scaling of the saturation current with gate voltage (Figure 7.7b). Linear and saturation regime effective mobilities are similar (within ∽ 10%), indicating a good carrier injection at the laminated source contact.

Four point probing structures allow separate measurement of the contact resistance and the channel resistance.[107,108] The results reveal intrinsic mobilities as high as 20±2 cm^2/V·s for transport along the *b*-axis.[132] As expected for Schottky contacts, the resistivity decreases with increasing gate bias and increases with decreasing temperature in accordance with the thermionic emission model (Figure 7.8 inset).[140] A semi-log plot of the resistance as a function of temperature can be fit by two linear segments corresponding to the change (at ∽ 175 °K) of

charge transport conduction mechanism from the intrinsic polaronic to trap dominated.[132] At low temperature, the transport in the channel is thought to be dominated by trapping processes, which might be responsible for the larger slope of the contact resistance vs 1/T dependence.

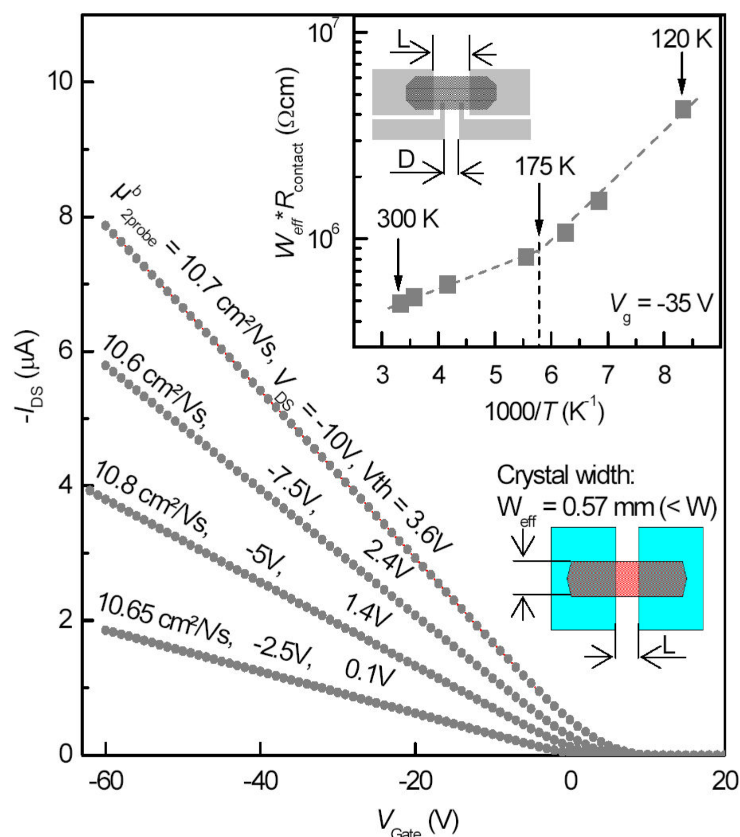


Figure 7.8: Transfer characteristics along the b-axis measured at different V_{DS}= -10 to -2.5 V (L= 149 μm, Weff= 0.57 mm, d= 3 μm). The inset shows an Arrhenius plot of the normalized contact resistance (Weff·Rcontact) for transport along the b-axis (L= 0.75 mm, Weff= 1.25 mm, D= 0.25 mm, Ci= 0.2 nF/cm^2).

The transport characteristics of the conducting channel depend critically on the properties of the rubrene crystals and, in particular, on the interface between the rubrene and air. Atomic force microscope measurements reveal mono-molecular steps (heights of $\backsim$ 1.5$\pm$0.1 nm) on the a-b plane with a preferred orientation along the b-axis (Figure 7.9a inset). These steps may affect the transport: it is expected that the effect of steps should become increasingly important at stronger gate fields when the carriers are pulled closer to the crystal surface.[141] Our observation that the mobilities along both a and b directions are independent of the gate induced electric field over a wide range of Vg (Figure 7.9a) suggests that the effect of steps is minor

in the case of the studied crystals with a relatively low density of steps. The high quality of the rubrene/air-dielectric interface clearly manifests itself in the sub-threshold device behavior. Figure 7.9b presents the temperature dependence of the drain current as a function of gate voltage in the sub-threshold region (the inset). As expected, the subthreshold swing increases linearly with temperature for transistors measured along the *a* or *b*-axis of the rubrene.[95] At room temperature, the normalized subthreshold swings along the *b*-axis varied typically from 0.4 to 0.8 V·nF/decade·cm^2, with a 'best' value of 0.38±0.04 V·nF/decade·cm^2. These subthreshold slope values correspond to remarkably low densities of surface states, (4.2 - 8.4)·10^{10} cm^2·eV^{-1}. This simple estimate neglects the depletion capacitance.[95]

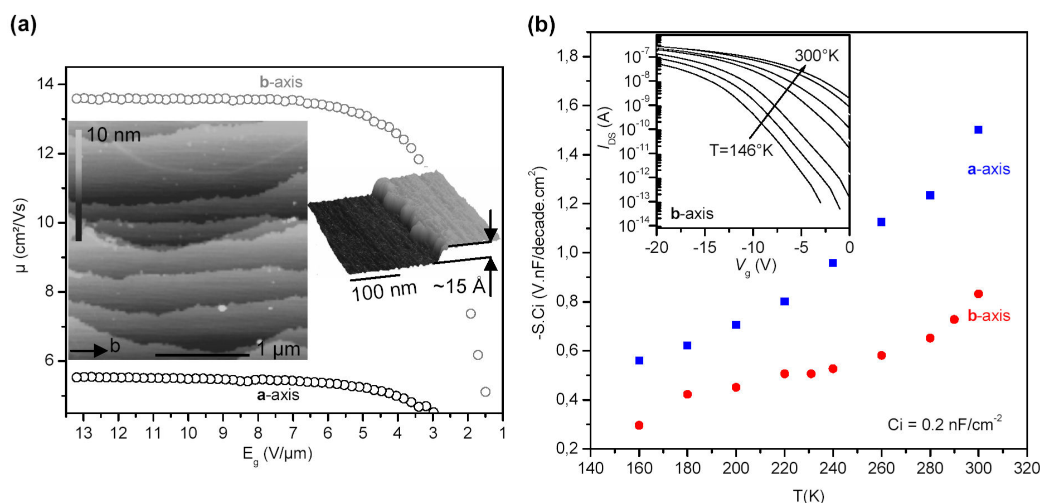


Figure 7.9: Semiconductor-gate dielectric interface characterization. **(a)** Variation of the linear regime carrier mobility along the *a* and *b*-axis of a rubrene single crystal as a function of the gate electric field measured in an air gap transistor. The inset shows low and high resolution AFM images of the *a*-*b* plane surface of a rubrene crystal. **(b)** Variation of the normalized subthreshold swing with temperature for a rubrene crystal along *a* and *b*-axis. The inset shows on a semi-log plot the transfer characteristics measured along the *b*-axis at different temperatures.

7.4 Conclusion

Laminated single crystal organic transistors with vacuum dielectrics represent perhaps the most straightforward route to artifact free measurements of the intrinsic gated transport in this class of materials. The results presented here demonstrate many features of this approach, including its successful use with two classes of small molecule organics to yield n and p channel devices with exceptionally good properties. Temperature dependent measurements and surface analytic studies reveal some basic aspects of transport, contacts and semiconductor/dielectric properties.

The approach also provides (i) sufficiently high resolution for transport studies on nanometer length scales, (ii) reversible device assembly for studies of device reliability and (iii) direct access to the accumulation channel for sensing applications. These areas represent fruitful directions for research.

7.5 Experimental Section:

7.5.1 Building the Transistors:

Casting and curing a liquid prepolymer against a ‘master’ with suitable relief structures in photoresist defines a soft rubber element. Collimated deposition of a metal coating produces, in a single step, source/drain electrodes and a self-aligned gate electrode on this element with geometries defined by the master. Laminating an organic single crystal on top of this structure completes the fabrication of a transistor whose gate dielectric is defined by the free space, or gap, below the bottom surface of the crystal and the top surface of the gate electrode. The electric measurements of the FETs characteristics have been carried out using Keithley SourceMeters K2400 and Electrometers K6512 and K617.

7.5.2 Preparing the Masters:

SU-8 photo resist was spin coated at 3000-5000 RPM, pre-baked at 120 ^{o}C for 5 min, exposed to UV light for 8 s ($\backsim$ 160 mJ/cm^2), post-baked at 95 ^{o}C for 3 min, and then developed for $\backsim$ 20 s in SU-8 developer.

7.5.3 Preparing the Stamps:

PDMS (Sylgard 184 from Dow Corning, www.downcorning.com) was mixed and degassed, poured over the masters and cured in an oven at 80 ^{o}C. Immediately before loading the stamp in an e-beam chamber, its surface was plasma oxidized using an Uniaxis 790 Plasma-Therm Reactive Ion etching system in an oxygen flow of 20 standard cubic centimeter per minute at a pressure of 30 mTorr for 20 s with a 10 W RF power. The 2$\pm$0.4 nm of Ti (0.3 nm/s) and 20$\pm$4 nm of Au (1 nm/s) were sequentially evaporated with a Temescal electron beam system (BJD 1800). Pressures during evaporation were typically $\backsim 3{\cdot}10^{-6}$ Torr or less.

Chapter 8

Scanning Tunnelling Microscopy of a Rubrene Single Crystal

8.1 Surface and Bulk Analysis of a Semi-Conducting Organic Single Crystal

Single crystal organic semiconductors represent ideal systems not only for studying basic science associated with transport of polaronic charge carriers but for investigating the upper limits of mobilities in thin film organic devices for flexible displays and other emerging electronic applications. The field effect transistors provide an important tool to explore the transport of field-induced charge carriers at the surface of organic semiconductors.[87] Special care, however, must be taken during the device fabrication to avoid degradation of the critical interface between the semiconductor and the dielectric.[86,135] High material purity, excellent crystalline quality and nanoscale morphological smoothness are among the characteristics of this interface that are crucial to obtain high performance devices[108,131] that can enable studies of intrinsic phenomena.

Detailed surface measurements of organic semiconductors at the active interfaces of conventional transistors are difficult or impossible to perform due to the inaccessibility of the semiconductor/dielectric interface to many classes of useful probes.[142–145] A new method for building transistors on the pristine surfaces of bulk single crystals uses free space dielectrics (*i.e.* vacuum or air) to eliminate completely any contact or processing of the active surface of the semiconductor. This technique, which provides a reversible ability to assemble and dissemble the devices repetitively, recently enabled observation of intrinsic transport and transport anisotropy in rubrene.[85,132] In this paper, we report on the scanning tunnelling microscope (STM) measurements of the critical interface between the semiconductor and the gate dielectric (air, in this case) in these devices. The results reveal directly, with molecular resolution, the position and orientation of the molecules on rubrene surface. These measurements represent the first real space molecular resolution images of the surface of a single crystal organic semiconductor.

When combined with atomic force microscope (AFM) images, the electrical measurements of point-contact Schottky diodes between the rubrene surface and the STM tip, and X-ray diffraction analysis, the results provide important insights into the physical and structural properties of the rubrene surface. We also demonstrate the feasibility of molecular scale modification of rubrene surface by moving the rubrene molecules with the STM tip. This capability could be valuable as an engineering tool for unusual classes of devices that rely on structured interfaces.

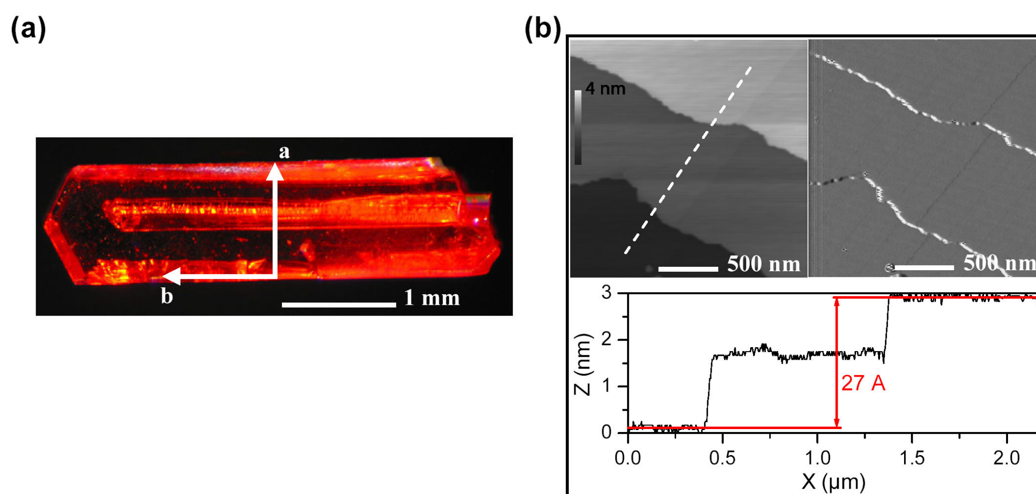


Figure 8.1: **(a)** Optical micrograph of a rubrene single crystal. The directions of the a and b crystal axes are determined by X-Ray Diffraction. **(b)** Atomic Force Microscope micrographs of the surface of the sample. A cross section line shows the presence of molecular steps with 27±.5 Å heights.

High quality single crystals of rubrene were grown by physical vapour transport in hydrogen.[87,104] Figure 8.1a shows an optical image of a typical crystal with an elongated hexagonal plate shape. The orientation of the crystal axis was determined by X-ray diffraction using a Cu Kα radiation. Figure 8.2 shows the two-θ X-Ray (45 kV, 40 mA, 2 s per angle step) intensity data collected on this crystal. The polar plots show that, as typically observed for crystals belonging to the orthorhombic pyramidal point group,[146] the c axis is normal to the top surface (slow-growing face) and that the b axis is parallel to the long side of the crystal. The crystal lattice values determined from these measurements are similar to those published in the literature: a = 14.49 Å, b = 7.21 Å, c = 26.92 Å.[147] The vertical distance measured by AFM between 3 terraces (see Figure 8.1b bottom inset) is in good agreement with the c axis crystal lattice parameter. This result confirms that there are 3 layers of molecules in the rubrene orthorhombic packing which belongs to the Aea2 (former Aba2) space group. AFM images of the surface revealed flat terraces separated by steps (Figure 8.1b). Images acquired at various locations indicate that the terrace plains are parallel to each other, suggesting that the samples are single crystalline.

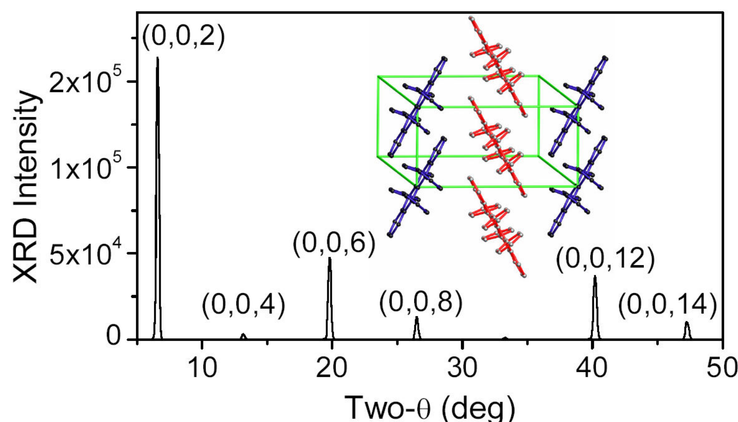


Figure 8.2: X-Ray Diffraction Two-θ plot of the sample with an inset that shows schematically the molecular organization of the rubrene molecules in the crystal a-b plane. The extracted orthorhombic cell lattice dimensions are a= 14.49 Å, b= 7.21 Å, c= 26.92 Å.

8.2 Surface Imaging at the Molecular Scale

The STM enables the direct examination of the molecular packing at the organic surface. For the measurements, the sample was mounted onto a metal plate using silver paint and left overnight for the paint to dry. STM analysis was performed with a PicoScan STM ("Molecular Imaging" USA) equipped with a low-current scanning head. The Pt-Ir (80:20) tip was mechanically cut from a commercial wire with 0.25 mm diameter. The STM images were recorded in both "current" and "constant height" modes. Molecular scale images were collected at the negative tip-polarity between -1 V to -2 V. At higher negative voltages, we observed a destabilization of tunnelling regime, probably due to desorption of molecules induced by the strong electric field in the tunnelling gap. At positive voltages, we were unable to generate any tunnelling current, for reasons described in detail below.

Figure 8.3a shows typical STM images of the rubrene surface. Two flat terraces separated by ∽2 nm height step are visible in the left and right parts of the image. The large terrace in the right part reveals parallel rows extending along the direction of preferential crystal growth. The average Z-corrugation of the rows is estimated to be about ∽1.5 Å. The detailed shape of the step between the terraces can change slightly during the scanning, which suggests the tip-induced detachment of molecules from the step edge as described below. Some detached molecules appear on top of the terrace (shown by white arrow in figure 8.3a). This tip-induced detachment of the molecules leads to instability in the tunnelling gap and the loss of resolution in the left part of image in figure 8.3a. In general, we were able to resolve molecular rows on top of all single terraces. Several topographic images acquired at different areas indicate that the orientation of molecular rows is spatially uniform. Figure 8.3b shows a blow-up with

molecular resolution. The periods between the repeated double-row features and between the rubrene molecules within the rows are ∽14 Å and ∽7 Å, respectively. Comparison with the lattice parameters obtained by X-ray diffraction confirmed that we were imaging the *a*-*b* plane of the crystal. The parallelogram drawn in Figure 8.3b shows the unit cell in the *a*-*b* plane of rubrene crystal. Figure 8.3c shows a larger scale image together with a cross section profile along a single row of molecules in the direction of *b* axis. These observations are important because they indicate an atomically clean interface and single crystal molecular organization at the active interface of transistors that use the as-grown surfaces of rubrene crystals and air dielectrics.

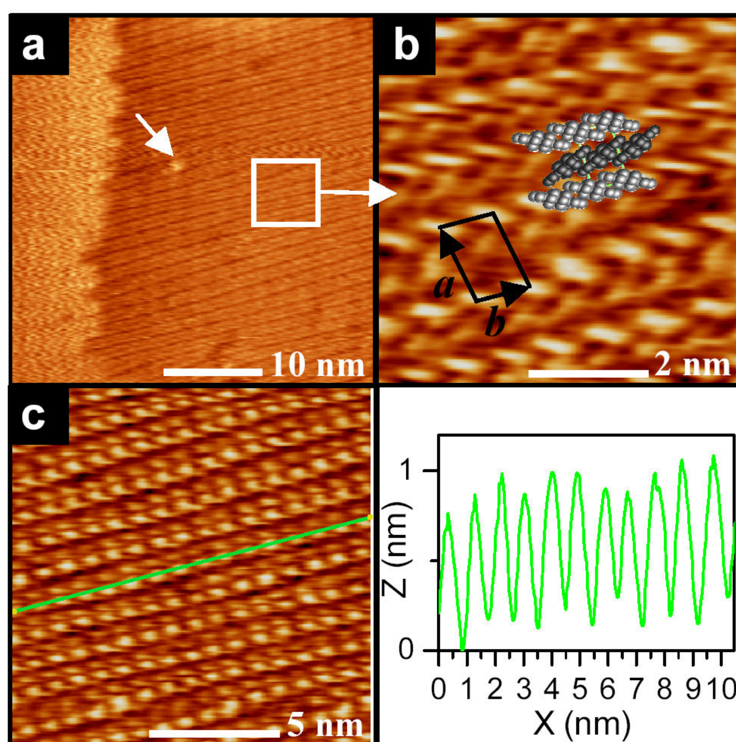


Figure 8.3: Scanning Tunnelling Microscopy Images of the rubrene surface. **(a)** Typical large-scale STM image of the rubrene crystal surface in the constant current mode (Vt= -1.065 V, It= 29 pA). **(b)** A smaller scale image (Vt= -1.138 V, It= 29 pA) reveals the herringbone organization of the rubrene molecules in the *a*-*b* plane. **(c)** Larger scale image and cross section profile along a single row of molecules in the *b*-axis direction of the crystal.

8.3 Rectifying Behaviour of a Rubrene Single Crystal

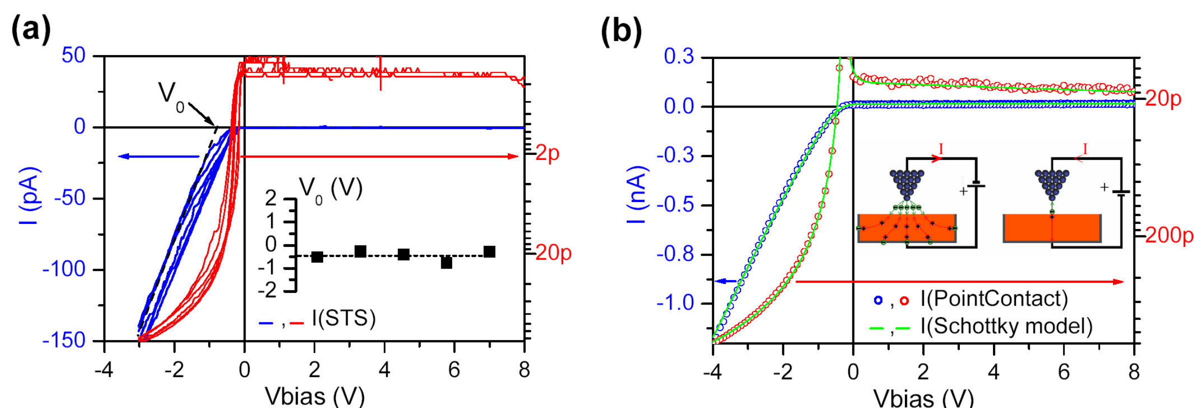


Figure 8.4: Scanning Tunnelling Spectroscopy and Electrical Measurements on the rubrene single crystal surface. **(a)**, Current-Voltage tunnelling spectra of the MIS tunnel diode presented on a linear (left) and logarithmic (right) plot showing the perfectly rectifying behaviour of the p-type rubrene semiconductor. The inset plot shows the extracted turn-on voltages from the tunnelling spectra. **(b)** Current-Voltage characteristic of a rubrene point contact diode (dots) fitted with the Schottky model (line). The inset schematic illustrates the carrier injection mechanism at the tip and bottom electrode of the point contact diode.

Figure 8.4a shows a set of current-voltage traces obtained with the STM tip located above an ordered region of molecular rows presented in figure 8.3c. In these I-V measurements the feedback loop of the STM is disabled, so that after an initial voltage and current (and thus tip height) are set (It= 10 pA, Ut= -1.1 V), the subsequent variations of the voltage are not followed by vertical movement of the tip. Rather, the tip remains at the initial height and the change in current resulting from the change in voltage is recorded. As can be seen, the I-V curves of the MIS tunnelling diode formed between the organic surface and the tip are almost linear at $U < 0$; at positive polarity the measured current is equal to zero. The turn-on voltages of the diodes are in good agreement with measurements made on a bulk point contact Schottky diode (Figure 8.4c, the point contact diode was made using a 12 μm tip diameter tungsten carbide probe tip from Signatone). This result suggests that the STM tip comes into close contact with the rubrene during the scan. The nearly zero (< 0.35 pA/V) ohmic "leakage" current in the reverse bias regime ($U > 0$) indicates the absence of a dangling-bond related surface transport channel.[148] In contrast to the Si point contact diodes, where transport through the dangling-bond surface states is typically observed, the rubrene diodes shows extremely good current blocking behaviour up to the reverse voltage biases ∽20 V. These results suggest the absence of dangling bonds at the surface and a low density of deep traps, which is consistent with the previously observed sharp normalized subthreshold swing for rubrene field effect transistors using air as a gate dielectric.[85] In the forward regime ($U < 0$), the current of the diodes is linearly limited by

the very high resistivity of the rubrene crystal. A bulk conductivity of ∽0.4 nS was extracted from the point contact diode after fitting the I-V characteristic using a standard Schottky exponential model (assuming a thermionic current emission, a serial resistance Rs, a parallel leakage resistance Rp and a reverse current Ir) (Eq.(8.1)).[95]

$$I = I_s[e^{\frac{V-R_sI}{nkT}} - 1] + \frac{V - R_sI}{R_p} - I_r \tag{8.1}$$

$$with\ I_s = 2.1\,pA,\ n = 5.5,\ R_s = 2.65\,G\Omega,\ R_p = 3\,T\Omega,\ I_r = 13\,pA$$

These results indicate the *p*-type rectifying behaviour of rubrene single crystal where positive carriers are injected (from the bottom contact) as schematically illustrated in Figure 8.4b inset. Only positive carriers transit through the bulk ; electrons, which transit in the crystal with much lower mobilities, are probably trapped.[149]

8.4 Nano-Patterning of the Surface of a Rubrene Crystal

In addition to molecular scale structural and electronic characterization, it is possible to use the STM tip as a tool for moving molecules across the rubrene surface. Figure 8.5 illustrates how local modification of the rubrene surface can be performed via a layer-by-layer stripping with the tip. In particular, a selected area of 50x50 nm^2 was scanned 30 times with tunnelling parameters of Ut= -1.138 V and It= 29 pA.

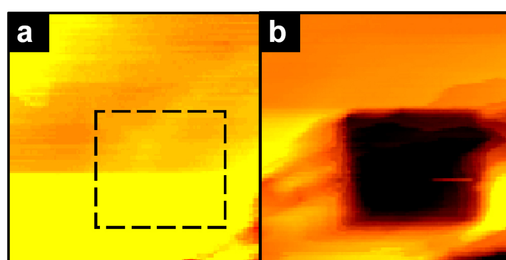


Figure 8.5: Local modification of the rubrene surface by a layer-by-layer "stripping" with the STM tip. The rubrene surface is shown before and after the tip-induced modification performed within a square marked by dash line in part a. This selected area was scanned ten times (It= 29 pA; Ut= -1.138 V; 200×200 nm^2). The modification creates a ∽100 Å deep depression and, at the same time, some material is displaced from the modified area.

The image in figure 8.5b shows a large (200×200 nm^2) scan of the same area immediately after the surface modification. As shown in cross section in figure 8.6e, the modification creates

an approximately ∽150 Å deep depression and, at the same time, some material is displaced from the modified area. The time evolution of molecular steps inside the depression can be seen in consequent "current" STM images in figures 8.6a-d. The cross-sectional profiles taken from corresponding "constant current" STM images (Figure 8.6e) allow to estimate how the depth of the depression changes during the scanning. This high-precision of modification of the organic surface could be useful for a range of basic and applied studies.

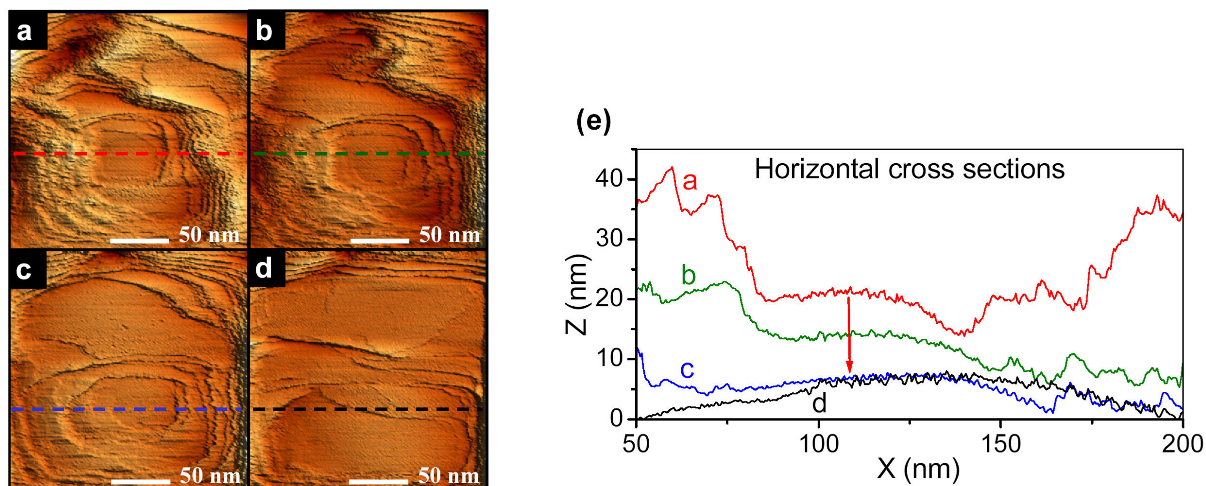


Figure 8.6: **(a** to **d)** 200×200 nm^2 consequent STM "current" images showing the time evolution of the molecular steps in an artificially created square depression in the rubrene crystal (It= 29 pA; Ut= -1.138V). The "current" regime of imaging is used for enhancement of contrast of the steps. **(e)** Cross-section profiles a,c,c&f along the dashed line taken from corresponding STM images recorded in "constant current" mode. The field induced surface flattening due to desorption of rubrene molecules is clearly visible.

8.5 Conclusion

In summary, the molecular resolution images of the surface of a bulk organic semiconductor have been observed. Although the conducting molecular crystals have been imaged in the past,[150] similar measurements have been previously unsuccessful for semiconducting samples because of their poor transport characteristics. The data on rubrene illustrate the extremely high quality of the crystal surface and directly reveal the morphology and electrical properties of the active interfaces of transistors fabricated with these materials. The ability to manipulate, on the molecular scale, the morphology of the crystal surface could be useful for future device applications or fundamental studies. Beyond the scope of this semiconductor analysis, we speculate that the surface of rubrene crystals might becomes a reference organic surface for STM analy-

sis. The presence of large molecularly-flat terraces on the crystal a-b planes together with the fact that no surface preparation (such as flaming or cleaving) is necessary to achieve molecular resolution makes this surface ideally suited for such studies.

Chapter 9

Conclusion and perspectives

In this thesis report, we have presented an overview of various 'soft lithography' techniques which have considerable value for applications in nanoscience and for the fabrication of plastic electronic systems. We speculate that the dry transfer printing method will be quickly adopted by the industry and used to manufacture the next generation of high performance distributed electronic devices on low cost, large area, plastic substrates. It's capability for transferring high performance semi-conducting materials, to virtually any substrate, without compromising their integrity, performance and alignment is unique. The successful operation of the technique has been demonstrated with the fabrication of the highest (to date) performance thin film transistors on plastic substrates.

Although this technique enables the fabrication of very high performance devices on plastic substrates, its successful application to an industrial fabrication line has not yet been demonstrated. Work in this direction is the focus of current efforts.

Organic semiconductors deposited by simple means, such as thermal evaporation, might still represent good candidates for the manufacturing of plastic electronic devices, such as electronic papers, requiring only moderate operation speed. We have seen that the rubrene organic semiconductor might represent an interesting candidate for such kind of applications. Futher research need to be carried to enable the fabrication of thin film devices from this material.

We wish that the 'Air-Gap' stamp technique that we have presented will be useful to other research groups as a "quick and clean" mean for evaluating the performance of their organic semiconducting materials. And finally, we hope that the results that we have presented on the surface analysis and charge carrier transport at the surface of rubrene single crystal have convinced the reader that interesting fundamental science researches need to be further pursued to gain a better understanding of complex organic semiconducting materials.

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Appendix A

Matlab® Code for Substracting Overall Translational and Rotational Misalignments

A.1 Matlab® Code

```
file_name = '4_PDMSKapOnMast.txt';
J=8; %Nb of horizontal patterns
LPatX = 56e3; %width of pattern array in um
LPatY = 56e3; %height of pattern array in um
kptoum = 100/105; %factor of conversion from pixel to um (100 um / nb pixels)
Nbar = 17; %N of bar in gaussien plot


%Load raw data
str_scan = '';
for j = 1:J
    str_scan = [str_scan,'%g %g '];
end
fid = fopen(file_name,'r');
a = fscanf(fid,str_scan,[2*J inf]); % It has J cols with X and Y values
a = a'
fclose(fid);
ss = size(a);
I = ss(1) %nb of rows

%Create Raw data matrix
for i = 1:I
    for j=1:J
        A{i,j}=[(j-1)*LPatX/(J-1) + kptoum*a(i,2*j-1)-LPatX/2 ;
                (I-i)*LPatY/(I-1) + kptoum*a(i,2*j)-LPatY/2];
    end
```

```
end

%Horizontal lignes y=a*x+b
for i = 1:I
    Sx=0;
    Sy=0;
    Sxy=0;
    Sx2=0;
    Sy2=0;
    for j = 1:J
        Sx=Sx + A{i,j}(1);
        Sy=Sy + A{i,j}(2);
        Sxy=Sxy + A{i,j}(1)*A{i,j}(2);
        Sx2=Sx2 + A{i,j}(1)*A{i,j}(1);
        Sy2=Sy2 + A{i,j}(2)*A{i,j}(2);
    end
    Lh{i}=[ (J*Sxy-Sx*Sy)/(J*Sx2-Sx*Sx) , (Sy*Sx2-Sx*Sxy)/(J*Sx2-Sx*Sx) ];
end

%Average slope am
am=0;
for i=1:I
    am = am+Lh{i}(1);
end
am = am/I;
%Angle of rotation alpha
alpha = atan(am);

%Vertical lignes x=c*y+d
for j = 1:J
    Sx=0;
    Sy=0;
    Sxy=0;
    Sx2=0;
    Sy2=0;
    for i = 1:I
        Sx=Sx + A{i,j}(1);
        Sy=Sy + A{i,j}(2);
        Sxy=Sxy + A{i,j}(1)*A{i,j}(2);
        Sx2=Sx2 + A{i,j}(1)*A{i,j}(1);
        Sy2=Sy2 + A{i,j}(2)*A{i,j}(2);
    end
    Lv{j}=[ (I*Sxy-Sx*Sy)/(I*Sy2-Sy*Sy) , (Sx*Sy2-Sy*Sxy)/(I*Sy2-Sy*Sy) ];
end

%Rotate raw data by -alpha
Rot=[cos(-alpha),-sin(-alpha);
     sin(-alpha),cos(-alpha)];
 for j = 1:J
```

```
76      for i = 1:I
            B{i,j}=Rot*A{i,j};
        end
    end

81  %Horizontal lignes y=a*x+b
    for i = 1:I
        Sx=0;
        Sy=0;
        Sxy=0;
86      Sx2=0;
        Sy2=0;
        for j = 1:J
            Sx=Sx + B{i,j}(1);
            Sy=Sy + B{i,j}(2);
91          Sxy=Sxy + B{i,j}(1)*B{i,j}(2);
            Sx2=Sx2 + B{i,j}(1)*B{i,j}(1);
            Sy2=Sy2 + B{i,j}(2)*B{i,j}(2);
        end
        Lhm{i}=[ (J*Sxy-Sx*Sy)/(J*Sx2-Sx*Sx) , (Sy*Sx2-Sx*Sxy)/(J*Sx2-Sx*Sx) ];
96  end

    %Vertical lignes x=c*y+d
    for j = 1:J
        Sx=0;
101     Sy=0;
        Sxy=0;
        Sx2=0;
        Sy2=0;
        for i = 1:I
106         Sx=Sx + B{i,j}(1);
            Sy=Sy + B{i,j}(2);
            Sxy=Sxy + B{i,j}(1)*B{i,j}(2);
            Sx2=Sx2 + B{i,j}(1)*B{i,j}(1);
            Sy2=Sy2 + B{i,j}(2)*B{i,j}(2);
111     end
        Lvm{j}=[ (I*Sxy-Sx*Sy)/(I*Sy2-Sy*Sy) , (Sx*Sy2-Sy*Sxy)/(I*Sy2-Sy*Sy) ];
    end

    %Calculate ref grid
116 dx = (Lvm{J}(2)-Lvm{1}(2))/(J-1);
    dy = (Lhm{I}(2)-Lhm{1}(2))/(I-1);
    %dx = 80000;
    %dy = -80000;
    for i = 1:I
121     for j = 1:J
            Gref{i,j}(1)=(j-1)*dx-(Lvm{J}(2)-Lvm{1}(2))/2;
            Gref{i,j}(2)=(I-i)*dy-(Lhm{I}(2)-Lhm{1}(2))/2;
        end
```

```
    end
126
    %Display ref grid and raw data
    subplot(2,3,1);
    hold on
    for i = 1:I
131     for k = 1:J
            Xm(k)=A{i,k}(1);
            Ym(k)=A{i,k}(2);
            Xr(k)=Gref{i,k}(1);
            Yr(k)=Gref{i,k}(2);
136     end
        plot(Xm,Ym,':rs','MarkerEdgeColor','k','MarkerFaceColor','g','MarkerSize',10)
        plot(Xr,Yr,':rs','MarkerEdgeColor','k','MarkerFaceColor','b','MarkerSize',5)
    end
    hold off
141 title('Raw Data on Ref grid');

    %Display quiver plot with raw data
    drms=0;
    for i = 1:I
146     for j = 1:J
            U(i,j)=A{I-i+1,j}(1)-Gref{i,j}(1);
            V(i,j)=A{I-i+1,j}(2)-Gref{i,j}(2);
            Xq(i,j)=Gref{i,j}(1);
            Yq(i,j)=Gref{i,j}(2);
151     end
    end
    subplot(2,3,4);
    quiver(U,V)
    title('Distortion on raw data');
156 xlabel(['rot angle ', num2str(alpha*180/pi), ' d']);

    %Calculate shift
    Tx=0;
    Ty=0;
161 for i = 1:I
        for j = 1:J
            Tx= Tx + B{i,j}(1)-Gref{i,j}(1);
            Ty= Ty + B{i,j}(2)-Gref{i,j}(2);
        end
166 end
    Tx = -Tx/(I*J);
    Ty = -Ty/(I*J);

    %Shift raw data
171 for j = 1:J
        for i = 1:I
            B{i,j}=[B{i,j}(1)+Tx;B{i,j}(2)+Ty];
```

```
        end
    end
176
    %Horizontal lignes y=a*x+b
    for i = 1:I
        Sx=0;
        Sy=0;
181     Sxy=0;
        Sx2=0;
        Sy2=0;
        for j = 1:J
            Sx=Sx + B{i,j}(1);
186         Sy=Sy + B{i,j}(2);
            Sxy=Sxy + B{i,j}(1)*B{i,j}(2);
            Sx2=Sx2 + B{i,j}(1)*B{i,j}(1);
            Sy2=Sy2 + B{i,j}(2)*B{i,j}(2);
        end
191     Lhm{i}=[ (J*Sxy-Sx*Sy)/(J*Sx2-Sx*Sx) , (Sy*Sx2-Sx*Sxy)/(J*Sx2-Sx*Sx) ];
    end

    %Vertical lignes x=c*y+d
    for j = 1:J
196     Sx=0;
        Sy=0;
        Sxy=0;
        Sx2=0;
        Sy2=0;
201     for i = 1:I
            Sx=Sx + B{i,j}(1);
            Sy=Sy + B{i,j}(2);
            Sxy=Sxy + B{i,j}(1)*B{i,j}(2);
            Sx2=Sx2 + B{i,j}(1)*B{i,j}(1);
206         Sy2=Sy2 + B{i,j}(2)*B{i,j}(2);
        end
        Lvm{j}=[ (I*Sxy-Sx*Sy)/(I*Sy2-Sy*Sy) , (Sx*Sy2-Sy*Sxy)/(I*Sy2-Sy*Sy) ];
    end

211 %Display quiver plot with ajusted data
    drms=0;
    for i = 1:I
        for j = 1:J
            U(i,j)=B{I-i+1,j}(1) - Gref{i,j}(1);
216         V(i,j)=B{I-i+1,j}(2) - Gref{i,j}(2);
            drms = drms
                    + ( (B{I-i+1,j}(1) - Gref{i,j}(1))^2
                    +   (B{I-i+1,j}(2) - Gref{i,j}(2))^2 )^0.5;
            Xq(i,j)=Gref{i,j}(1);
221         Yq(i,j)=Gref{i,j}(2);
        end
```

```
    end
    drms = drms/(I*J);
    subplot(2,3,2);
226 quiver(U,V)
    title('Distortion␣on␣ajusted␣data');
    xlabel(['rms␣=␣', num2str(drms)]);

    %---------------------------------------------------------------------------
231 %Rotate camera after shifting
    Rstep=60;
    Rmax=pi/5000;
    rms_min = 1000;
    for r = 0:Rstep
236 rcam= -(Rstep/2-r)*(Rmax)/Rstep+Rmax/2-Rmax/2;
    C=B;
    for i = 1:I
        for j = 1:J
            rU=B{i,j}(1)-Gref{i,j}(1);
241         rV=B{i,j}(2)-Gref{i,j}(2);
            vU=rU*cos(rcam)-rV*sin(rcam);
            vV=rU*sin(rcam)+rV*cos(rcam);
            C{i,j}(1)=Gref{i,j}(1)+vU;
            C{i,j}(2)=Gref{i,j}(2)+vV;
246     end
    end

    %Horizontal lignes y=a*x+b
    for i = 1:I
251     Sx=0;
        Sy=0;
        Sxy=0;
        Sx2=0;
        Sy2=0;
256     for j = 1:J
            Sx=Sx + C{i,j}(1);
            Sy=Sy + C{i,j}(2);
            Sxy=Sxy + C{i,j}(1)*C{i,j}(2);
            Sx2=Sx2 + C{i,j}(1)*C{i,j}(1);
261         Sy2=Sy2 + C{i,j}(2)*C{i,j}(2);
        end
        Lh{i}=[ (J*Sxy-Sx*Sy)/(J*Sx2-Sx*Sx) , (Sy*Sx2-Sx*Sxy)/(J*Sx2-Sx*Sx) ];
    end

266 %Average slope am
    am=0;
    for i=1:I
        am = am+Lh{i}(1);
    end
271 am = am/I;
```

```
    %Angle of rotation alpha
    alpha = atan(am);

    %Rotate raw data by -alpha
276 Rot=[cos(-alpha),-sin(-alpha);
         sin(-alpha),cos(-alpha)];
     for j = 1:J
         for i = 1:I
             C{i,j}=Rot*C{i,j};
281      end
    end

    %Horizontal lignes y=a*x+b
    for i = 1:I
286     Sx=0;
        Sy=0;
        Sxy=0;
        Sx2=0;
        Sy2=0;
291     for j = 1:J
            Sx=Sx + C{i,j}(1);
            Sy=Sy + C{i,j}(2);
            Sxy=Sxy + C{i,j}(1)*C{i,j}(2);
            Sx2=Sx2 + C{i,j}(1)*C{i,j}(1);
296         Sy2=Sy2 + C{i,j}(2)*C{i,j}(2);
        end
        Lhm{i}=[ (J*Sxy-Sx*Sy)/(J*Sx2-Sx*Sx) , (Sy*Sx2-Sx*Sxy)/(J*Sx2-Sx*Sx) ];
    end

301 %Vertical lignes x=c*y+d
    for j = 1:J
        Sx=0;
        Sy=0;
        Sxy=0;
306     Sx2=0;
        Sy2=0;
        for i = 1:I
            Sx=Sx + C{i,j}(1);
            Sy=Sy + C{i,j}(2);
311         Sxy=Sxy + C{i,j}(1)*C{i,j}(2);
            Sx2=Sx2 + C{i,j}(1)*C{i,j}(1);
            Sy2=Sy2 + C{i,j}(2)*C{i,j}(2);
        end
        Lvm{j}=[ (I*Sxy-Sx*Sy)/(I*Sy2-Sy*Sy) , (Sx*Sy2-Sy*Sxy)/(I*Sy2-Sy*Sy) ];
316 end

    %Calculate ref grid
    %dx = (Lvm{J}(2)-Lvm{1}(2))/(J-1);
    %dy = (Lhm{I}(2)-Lhm{1}(2))/(I-1);
```

```
321 for i = 1:I
        for j = 1:J
            Gref2{i,j}(1)=(j-1)*dx-(Lvm{J}(2)-Lvm{1}(2))/2;
            Gref2{i,j}(2)=(i-1)*dy-(Lhm{I}(2)-Lhm{1}(2))/2;
        end
326 end

    %Calculate shift
    Tx=0;
    Ty=0;
331 for i = 1:I
        for j = 1:J
            Tx= Tx + C{i,j}(1)-Gref2{i,j}(1);
            Ty= Ty + C{i,j}(2)-Gref2{i,j}(2);
        end
336 end
    Tx = -Tx/(I*J);
    Ty = -Ty/(I*J);

    %Shift raw data
341 for j = 1:J
        for i = 1:I
            C{i,j}=[C{i,j}(1)+Tx;C{i,j}(2)+Ty];
        end
    end
346
    %Calculate rms distortion
    drms=0;
    for i = 1:I
        for j = 1:J
351         drms = drms
                    + (  (C{i,j}(1)-Gref2{i,j}(1))^2
                    + (   C{i,j}(2)-Gref2{i,j}(2))^2  )^0.5;
        end
    end
356 drms = drms/(I*J);
    if drms < rms_min
        rms_min = drms;
        rcam_opt = rcam;
    end
361
    lrcam(r+1)=rcam*180/pi;
    ddercam(r+1) = drms;

    end %r...
366
    %Display camera rotation influence
    subplot(2,3,5);
    plot(lrcam,ddercam)
```

```
    title('Camera rotation');
371 xlabel(['Camera rot = ', num2str(rcam_opt*180/pi), ' d']);


    %-----------------------------------------------------------------------
    %Rotate camera by optimized rotation value
376
    rcam= rcam_opt;
    C=B;
    for i = 1:I
        for j = 1:J
381         rU=B{i,j}(1)-Gref{i,j}(1);
            rV=B{i,j}(2)-Gref{i,j}(2);
            vU=rU*cos(rcam)-rV*sin(rcam);
            vV=rU*sin(rcam)+rV*cos(rcam);
            C{i,j}(1)=Gref{i,j}(1)+vU;
386         C{i,j}(2)=Gref{i,j}(2)+vV;
        end
    end

    %Horizontal lignes y=a*x+b
391 for i = 1:I
        Sx=0;
        Sy=0;
        Sxy=0;
        Sx2=0;
396     Sy2=0;
        for j = 1:J
            Sx=Sx + C{i,j}(1);
            Sy=Sy + C{i,j}(2);
            Sxy=Sxy + C{i,j}(1)*C{i,j}(2);
401         Sx2=Sx2 + C{i,j}(1)*C{i,j}(1);
            Sy2=Sy2 + C{i,j}(2)*C{i,j}(2);
        end
        Lh{i}=[ (J*Sxy-Sx*Sy)/(J*Sx2-Sx*Sx) , (Sy*Sx2-Sx*Sxy)/(J*Sx2-Sx*Sx) ];
    end
406
    %Average slope am
    am=0;
    for i=1:I
        am = am+Lh{i}(1);
411 end
    am = am/I;
    %Angle of rotation alpha
    alpha = atan(am);

416 %Rotate raw data by -alpha
    Rot=[cos(-alpha),-sin(-alpha);
         sin(-alpha),cos(-alpha)];
```

```
 for j = 1:J
     for i = 1:I
421          C{i,j}=Rot*C{i,j};
     end
end

%Horizontal lignes y=a*x+b
426 for i = 1:I
     Sx=0;
     Sy=0;
     Sxy=0;
     Sx2=0;
431  Sy2=0;
     for j = 1:J
          Sx=Sx + C{i,j}(1);
          Sy=Sy + C{i,j}(2);
          Sxy=Sxy + C{i,j}(1)*C{i,j}(2);
436       Sx2=Sx2 + C{i,j}(1)*C{i,j}(1);
          Sy2=Sy2 + C{i,j}(2)*C{i,j}(2);
     end
     Lhm{i}=[ (J*Sxy-Sx*Sy)/(J*Sx2-Sx*Sx) , (Sy*Sx2-Sx*Sxy)/(J*Sx2-Sx*Sx) ];
end
441
%Vertical lignes x=c*y+d
for j = 1:J
     Sx=0;
     Sy=0;
446  Sxy=0;
     Sx2=0;
     Sy2=0;
     for i = 1:I
          Sx=Sx + C{i,j}(1);
451       Sy=Sy + C{i,j}(2);
          Sxy=Sxy + C{i,j}(1)*C{i,j}(2);
          Sx2=Sx2 + C{i,j}(1)*C{i,j}(1);
          Sy2=Sy2 + C{i,j}(2)*C{i,j}(2);
     end
456  Lvm{j}=[ (I*Sxy-Sx*Sy)/(I*Sy2-Sy*Sy) , (Sx*Sy2-Sy*Sxy)/(I*Sy2-Sy*Sy) ];
end

%Calculate ref grid
for i = 1:I
461  for j = 1:J
          Gref2{i,j}(1)=(j-1)*dx-(Lvm{J}(2)-Lvm{1}(2))/2;
          Gref2{i,j}(2)=(i-1)*dy-(Lhm{I}(2)-Lhm{1}(2))/2;
     end
end
466
%Calculate shift
```

```
Tx=0;
Ty=0;
for i = 1:I
    for j = 1:J
        Tx= Tx + C{i,j}(1)-Gref2{i,j}(1);
        Ty= Ty + C{i,j}(2)-Gref2{i,j}(2);
    end
end
Tx = -Tx/(I*J);
Ty = -Ty/(I*J);

%Shift raw data
for j = 1:J
    for i = 1:I
        C{i,j}=[C{i,j}(1)+Tx;C{i,j}(2)+Ty];
    end
end

%Display quiver plot
drms=0;
n=0;rms_max=0;
for i = 1:I
    for j = 1:J
        U4(I-i+1,j)=C{i,j}(1)-Gref2{i,j}(1);
        V4(I-i+1,j)=C{i,j}(2)-Gref2{i,j}(2);
        rms = ( (C{i,j}(1)-Gref2{i,j}(1))^2 + (C{i,j}(2)-Gref2{i,j}(2))^2 )^0.5;
        drms = drms + rms;
        n=n+1;
        lrmsx(n) = C{i,j}(1)-Gref2{i,j}(1);
        lrmsy(n) = C{i,j}(2)-Gref2{i,j}(2);
        lrms(n) = rms;
        if rms > rms_max
            rms_max = rms;
        end
    end
end
drms = drms/(I*J);
subplot(2,3,3);
quiver(U4,V4)
title('Distortion with optimized camera rotation');
xlabel(['rms min = ', num2str(drms)]);

%Gaussien graph
gauss(Nbar+1)=0;
for i = 1:I*J
    gauss(round(lrms(i)*Nbar/rms_max)+1) = gauss(round(lrms(i)*Nbar/rms_max)+1)+1;
end

Gi = 1:1:Nbar+1;
```

```
    subplot(2,3,6);
    bar(Gi,gauss);
    title('Dispersion␣plot');
    xlabel('rms␣(um)');
521 set(gca,'Xlim',[0,Nbar]);
    set(gca,'XTick',0:Nbar/4:Nbar)
    set(gca,'XTickLabel',{'0',
        num2str(round(10*rms_max*1/4)/10),
        num2str(round(10*rms_max*2/4)/10),
526     num2str(round(10*rms_max*3/4)/10),
        num2str(round(10*rms_max*4/4)/10)})
```

A.2 Typical Program Outputs

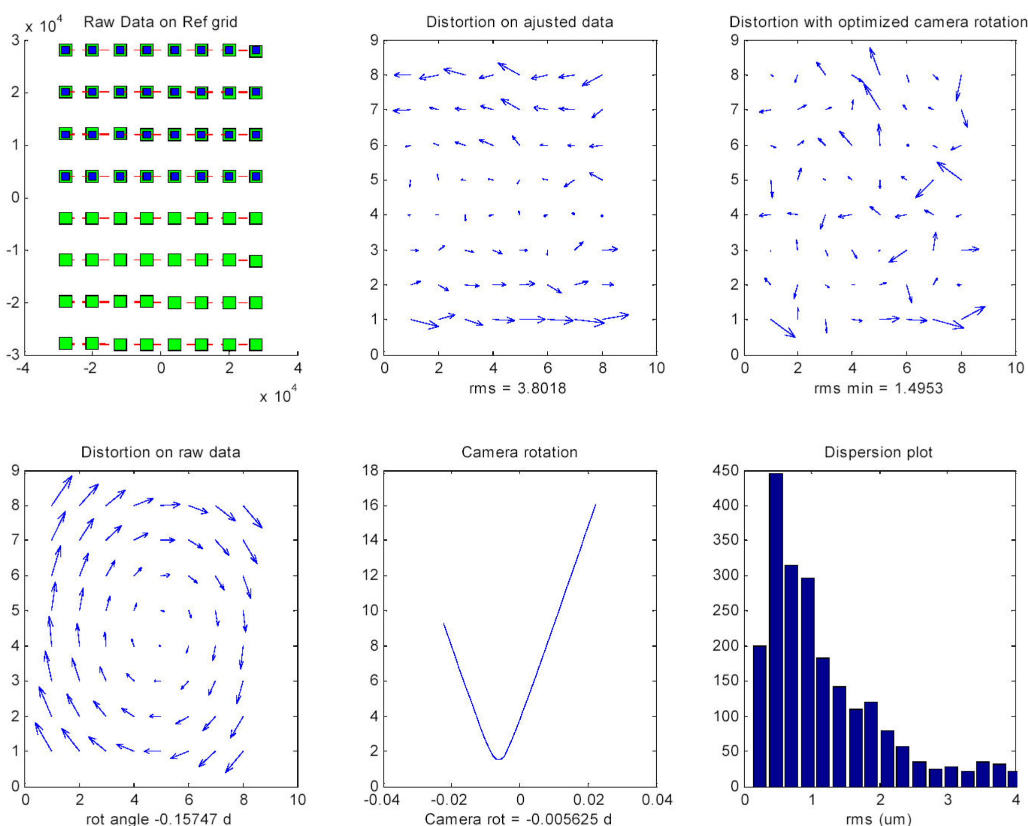

Figure A.1: In this experiemnt, the stamp was laminated on its master with an overall rotation offset of -0.15^o. The center of rotation was located close to the middle of the sample area.

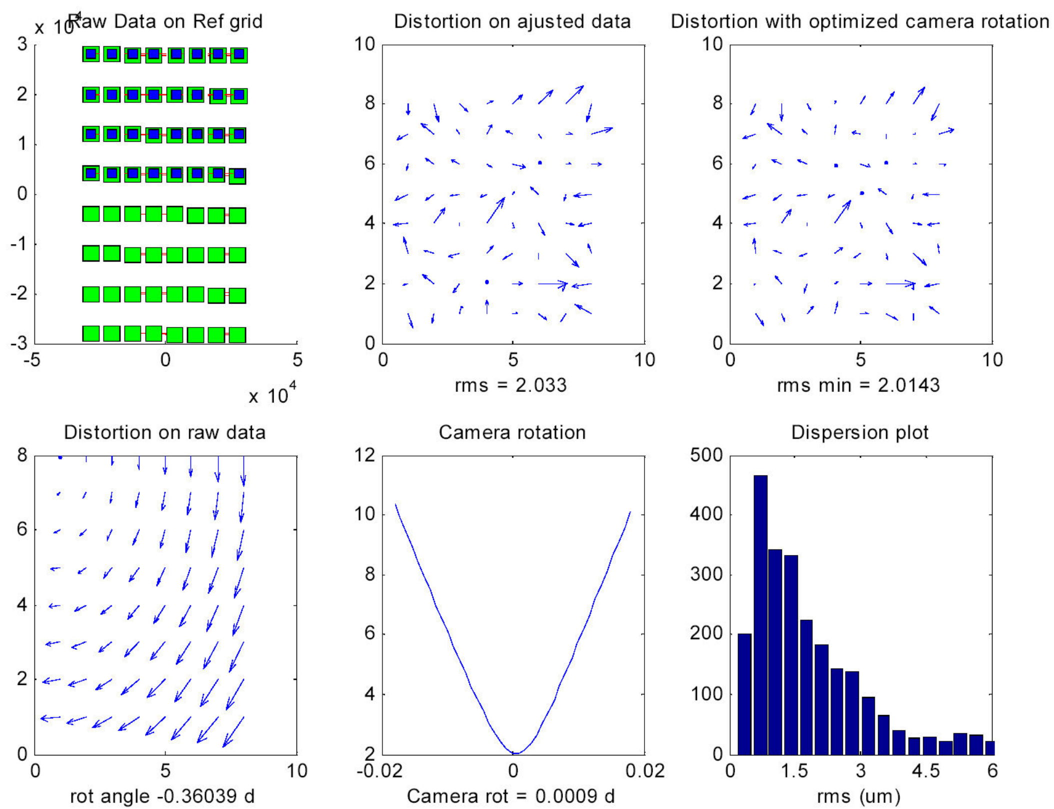

Figure A.2: In this experiemnt, the stamp was laminated on its master with an overall rotation offset of -0.36^o. The center of rotation was located close in the top left of the sample area.

Appendix B

Adhesion and Collapse of Soft Elastomeric Stamps

In all soft lithographic methods, the elastomeric stamps are brought into contact with solid substrates or elements. The low modulus and low surface energy of the elastomers that are typically used for the stamps (*e.g.* polysdimethylsiloxaned, PDMS) allow atomic-scale conformal contacts to be established without the application of external pressure. The basic mechanisms governing this critically important contact process and the issues that can lead, in certain cases, to mechanical collapse of the stamp relief features are not well known.

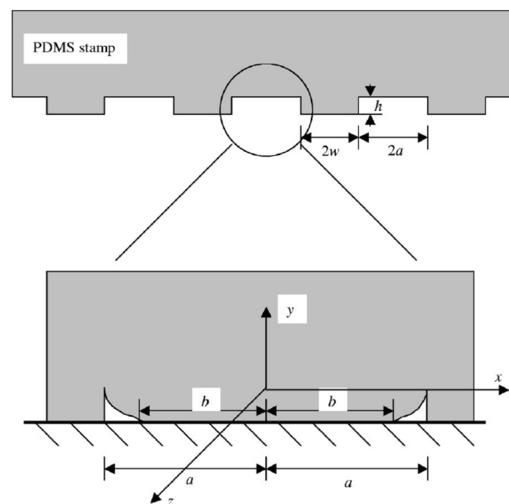

Figure B.1: (a) Schematics of the PDMS stamp specimens used in the experiments, and **(b)** details of a collapsed groove with a contact region -b≤x≤b.

In order to understand this process more fully, we conducted both experimental study and modeling of an idealized structure with a simple pattern. We used periodic rectangular grooves

and flat punches, as schematically shown in Figure B.1. The material used to fabricate the experimental specimens is PDMS (Dow Corning, Sylgard 184). The dimension of the grooves (punches) in the out-of-plane direction (z direction) is very large compared to the in-plane dimensions, w and a. In the current study, a was fixed at 500 mm, w ranged from 50 mm to 5 mm; while the dimension in the z direction, *e.g.*, the length of grooves, is of the order of several centimeters. Such geometric arrangement usually guarantees the plane strain condition during deformation. Moreover, we choose the height of the punches h, ranging from a few hundred nanometers to a few micrometers, to be much smaller than w or a (h/a is always less than 0.01). A wide range of the a/w ratio and several values of h have been considered in the experimental measurements. The experiments were conducted by placing the patterned stamps on a substrate of a silicon wafer with a native silica glass layer. The degree of collapse was then examined and measured using optical microscopy. In all cases, we observed that the grooves collapsed onto the substrate. A fully collapsed groove is schematically shown in figure B.1b.

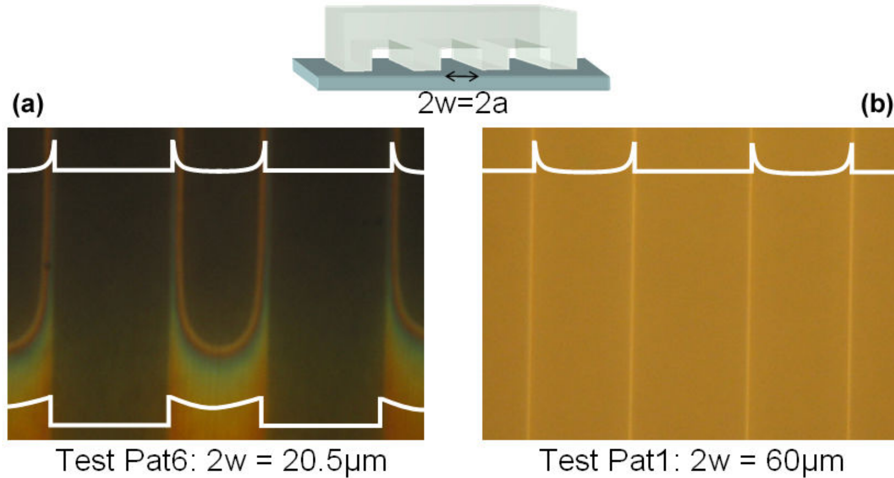

Figure B.2: Optical micrograph of typical collapsing front **(a)** and fully collapsed front **(b)** in a PDMS stamp (h=0.5 μm). The white contaours are the displacement profiles of the stamp surface at partly collapsed and fully collapsed locations.

Optical microscopy videos show that once a groove collapse occurs at any location, it will progress rapidly with a front roughly normal to the long dimension (*i.e.*, normal to z axis in figure B.1b) across all grooves. An optical micrograph of a typical collapsing front of a stamp is shown in figure B.2a.

Furthermore, the contact part of the collapsed region always takes a significant portion of the groove, *i.e.*, the ratio b/a in Figure B.1b is always rather large (>0.7). We experimentally measured b (or the noncontact width L=a-b) for many different combinations of a/w and h. The measurement results are shown in Figure B.4 as discrete data points. One key question is what the driving force is for the groove collapse in PDMS stamps. It has been postulated that

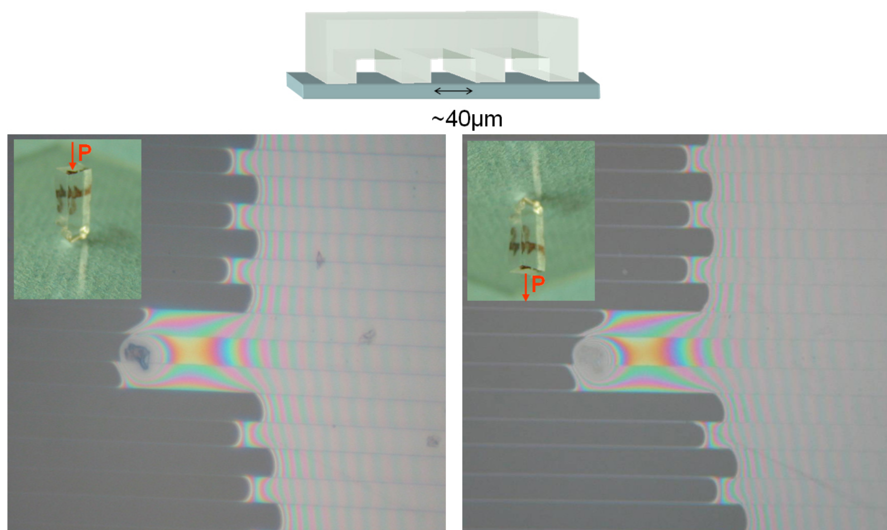

Figure B.3: Optical micrograph of collapsing in a PDMS stamp laminated against a glass slide. The first frame shows the sample looking through the PDMS stamp while the second frame shows the same sample upside down (this time looking through the glass substrate).

the collapse is a result of the gravitational force, *i.e.*, the self-weight of the stamps. Hui et al.* and Sharp et al.† provided an analysis based on this assumption to evaluate the forces needed to cause the groove collapse (see Eq.B.1).

$$y_{max} = \frac{4\sigma_{\infty}}{\pi E^{*}}(w+a)cosh^{-1}[\frac{a\pi}{2(w+a)}] \tag{B.1}$$

with σ_{∞}: remote stress on the stamp due to a compressive load on the top
$E^{*} \equiv E/(1-\nu^{2})$
E: Stamp Young's modulus
ν: Stamp Poisson's ratio ($\nu \backsim 0.5$)
$2a, 2w$: Stamps' roof and punch widths

However, in our experiments, we have at times turned the experimental setup up-side down, such that the gravitational force acts to prevent grooves collapse. But the grooves still collapsed with the same proportion of the contact area in the grooves as can be seen on Figure B.3. Finite element analysis of the stamps also shows that the required 'gravitational force' to collapse the stamps would be more than 30 times higher than the weight of the stamps. These evidences indicate that the driving force for groove collapse is not the gravitational force, but is likely to be interfacial adhesion between PDMS stamp and the substrate. We have developed a model

Langmuir*, **18, 1394 (2002)
†*Langmuir*, **20**, 6430 (2004)

based on the postulation that the groove collapse is caused by interfacial adhesion. The details of this analytical model is presented in a Langmuir article.‡

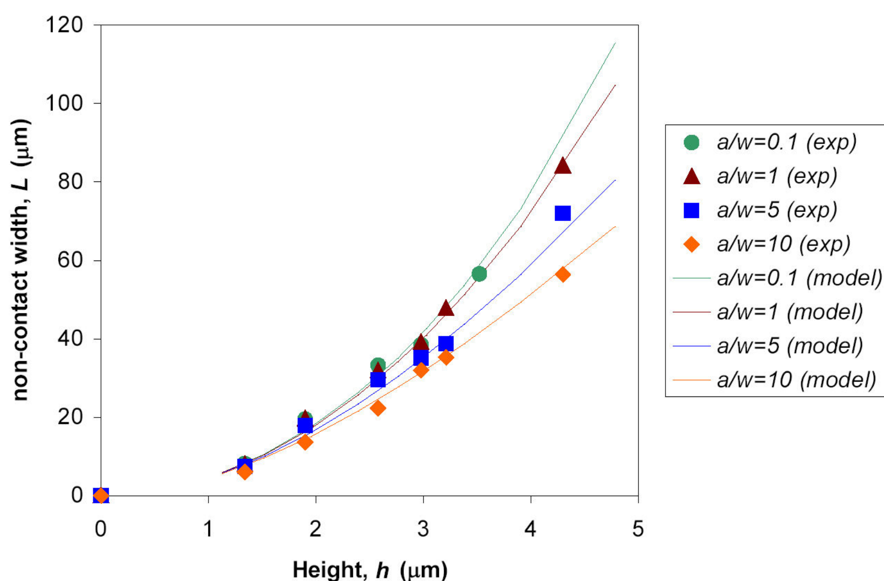

Figure B.4: Experimental measurements (individual data points) and model predictions (solid lines) of the non-contact width L of fully collapsed grooves as a function of groove height h for a wide range of *a/w*.

The solid lines in Figure B.4 are the model predictions of the noncontact width L=*a*-*b* as a function of the groove depth h for a wide range of *a/w*. In generating these curves, the value of G is determined from the experimental data for *a/w=1*, and that value is then used to plot the curves for all other *a/w* values. Figure B.4 demonstrates that our model predictions exhibit excellent agreement with experimental measurements for a wide range of the ratio of groove width over punch width, *a/w*, and for all values of punch height h tested in the experiment. It should be pointed out that if the driving force for groove collapse were the self-weight of the stamps, the noncontact width L versus groove height h curve would be linear. This assertion can be confirmed both by the formula in Hui et al.'s paper (Eq. B.1) and by finite element analysis that we carried out with FEMLAB®. However, the L versus h curve would be qualitatively different, *i.e.*, the curve would be nonlinear if the driving force is interfacial adhesion. In fact, it can be shown from the model that L is proportional to h^2 in the limiting case of *a/w*→0.11 Results presented in Figure B.4, both the experimental measurements and the model prediction, provide convincing evidence that the driving force for groove collapse is indeed interfacial adhesion.

‡*Langmuir*, **21**, 8058 (2005)

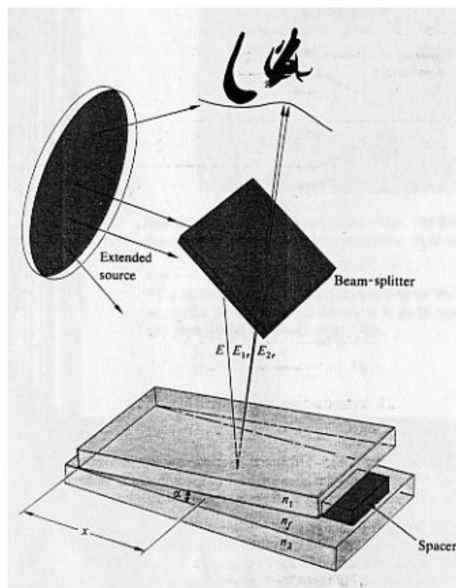

Figure B.5: Basic experimental setup to produce and observe Fizeau fringes. From Klein and T. E. Furtak, Optics (Wiley, New York, 1986).

In order to get a better understanding of the local adhesion forces which are causing the sagging of the stamp recessed areas, we then decided to investigate the shape of the sagging profile. The imaging of a cross section of the stamp would be unpractical as it is rather difficult to obtain a clean cross section of a PDMS elastomer. So, we decided to develop an optical method based on Fizeau's interferences (See Figure B.5).

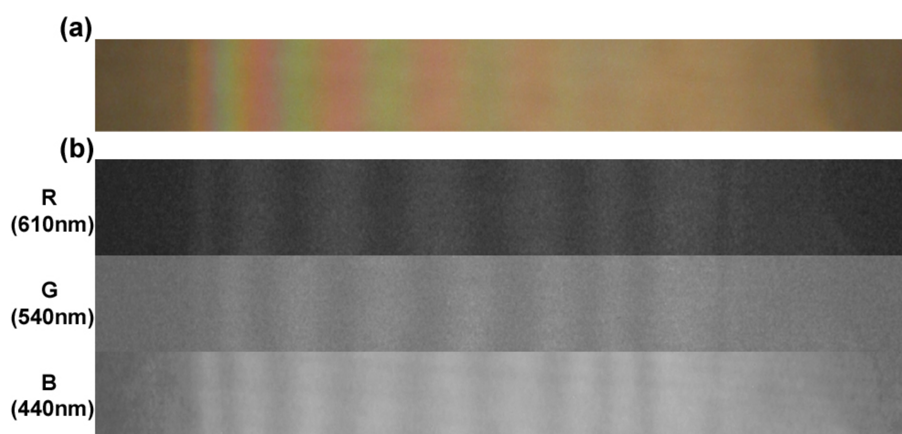

Figure B.6: White-light **(a)** and filtered **(b)** fringes observed in the sagging area of a PDMS stamp laminated against a flat silicon wafer.

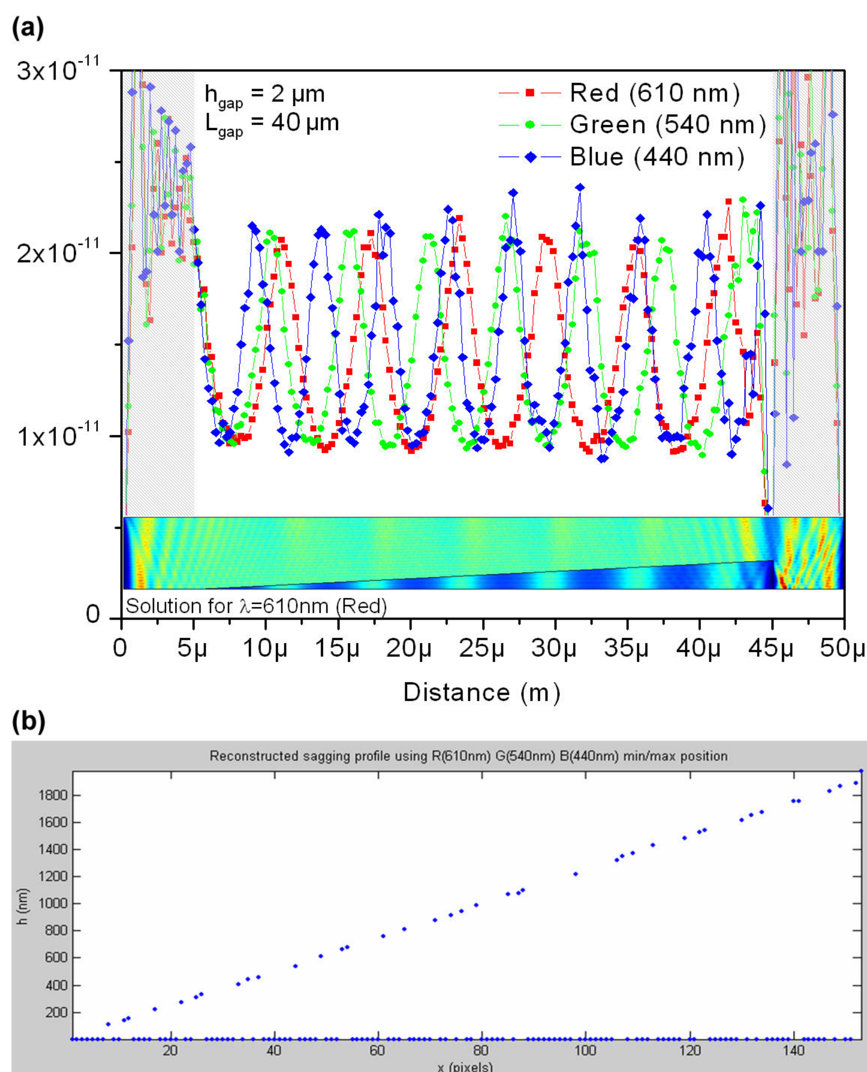

Figure B.7: **(a)** Finite element simulation results of the Fizeau fringes obtained using the 'electromagnetics' module of FEMLAB®. **(b)** Reconstructed (with a Matlab® script) profile using the light intensity data obtained with the FEM simulations.

When the sagging profile of a PDMS stamp laminated against a flat silicon wafer is observed under a high resolution microscope, local interferences fringes are observed (See Figure B.6a). The analysis of such diffraction patterns is rather difficult when the light source wavelength is unknown. But, the light of the optical microscope can be filtered with a narrow band optical filter in order to obtain a quasi monochromatic light source. Using three different narrow band optical filters with center wavelengths located into the visible range, it is possible to record images of the light intensity map using a regular CCD camera mounted on the microscope head (Figure B.6b).

With the help of a Matlab script, it is possible to filter and extract the variation of the light intensity and to reconstruct the sagging profile of the PDMS stamp. In order to verify the accuracy of this idea, we simulated the optics of the system using FEMLAB. Figure B.7a presents the results of these simulations in the case of a linear sagging profile (standard Fizeau fringes). This set of data was then used as a benchmark to verify the correctness of the Matlab script. The reconstructed sagging profile presented in Figure B.7b is in good agreement with the original arbitrary chosen profile confirming the accuracy of the method.

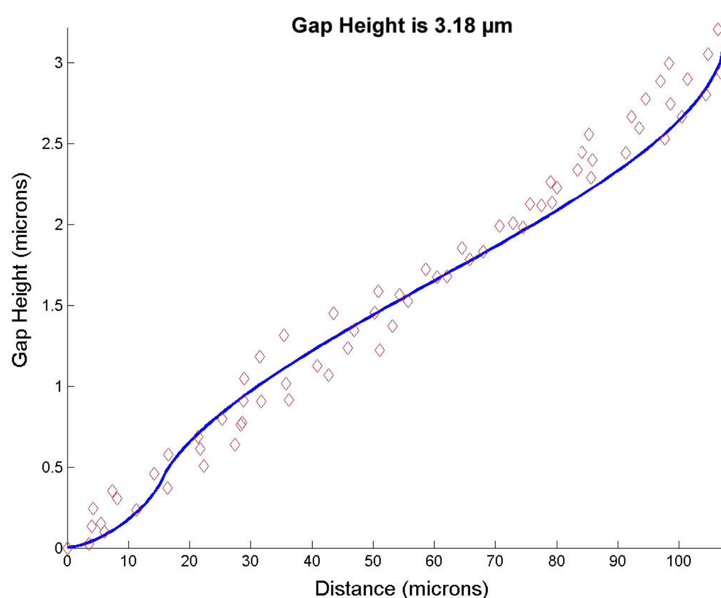

Figure B.8: Reconstructed experimental (marks) and theroitical model (solid line) of the sagging profile of a PDMS stamps with 3.18μm relief line features (*2w=2a*) laminated ontop of a silicon wafer.

Figure B.8 shows preliminary measurements of the sagging profile of a PDMS sample laminated against a flat silicon wafer. The new analytical model taking into consideration the local Van Der Waals adhesion forces seems to be in shart agreement with these experimental results. Further experiments are under progress to confirm these preliminary results.

Appendix C

List of Written and Oral Communications

List of written communications

[1] Menard, E., Bilhaut, L., Zaumseil, J. and Rogers, J. A. Improved surface chemistries, thin film deposition techniques, and stamp designs for nanotransfer printing. *Langmuir* **20**, 6871–6878 (2004).

[2] Jeon, S., Menard, E., Park, J. U., Maria, J., Meitl, M., Zaumseil, J. and Rogers, J. A. Three-dimensional nanofabrication with rubber stamps and conformable photomasks. *Advanced Materials* **16**, 1369–1373 (2004).

[3] Menard, E., Lee, K. J., Khang, D. Y., Nuzzo, R. G. and Rogers, J. A. A printable form of silicon for high performance thin film transistors on plastic substrates. *Applied Physics Letters* **84**, 5398–5400 (2004).

[4] Menard, E., Nuzzo, R. G. and Rogers, J. A. Bendable single crystal silicon thin film transistors formed by printing on plastic substrates. *Applied Physics Letters* **86**, 093507 (2005).

[5] Zhu, Z. T., Menard, E., Hurley, K., Nuzzo, R. G. and Rogers, J. A. Spin on dopants for high-performance single-crystal silicon transistors on flexible plastic substrates. *Applied Physics Letters* **86**, 133507 (2005).

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[7] Sun, Y., Kim, H. S., Menard, E., Kim, S., Chen, G., Adesida, I. and Rogers, J. A. Gigahertz operation in mechanically flexible transistors on plastic substrates and their integration into several types of logic gates (submitted).

[8] Lee, H. H., Menard, E., Tassi, N. G., Rogers, J. A. and Blanchet, G. B. Fabrication of large-area stamps, moulds, and conformable photomasks for soft lithography. *Proceedings of the I MECH E Part N Journal of Nanoengineering and Nanosystems* **N1**, 1–6 (2004).

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[13] Menard, E., Marchenko, A., Podzorov, V., Gershenson, M. E., Fichou, D. and Rogers, J. A. Surface imaging and rectifying behaviour of a semi-conducting organic single crystal at the molecular scale. *Nature Materials* (in press).

[14] Hsia, K. J., Huang, Y., Menard, E., Park, J. U., Zhou, W., Rogers, J. and Fulton, J. M. Collapse of stamps for soft lithography due to interfacial adhesion. *Applied Physics Letters* **86**, 154106 (2005).

[15] Huang, Y., Zhou, W., Hsia, K. J., Menard, E., Park, J. U., Rogers, J. A. and Alleyne, A. G. Stamp collapse in soft lithography. *Langmuir* **21**, 8058–8068 (2005).

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[17] Menard, E. and Rogers, J. Nanofabrication techniques with high resolution molded rubber stamps. In Busnaina, A. A. (ed.) *Handbook of Nanomanufacturing* (CRC Press, 2005).

List of oral communications

[1] Menard, E., Meitl, M., Zaumseil, J., Sundar, V. C., Acharya, B. and Rogers, J. Additive nanofabrication with a stamp: applications in organic electronics. *7th European Conference on Molecular Electronics* Avignon, France (September 10, 2003).

[2] Menard, E., Sun, Y., Khang, D. Y., Zhu, Z. T., Lee, K. J., Nuzzo, R. G. and Rogers, J. A printable form of single crystal silicon for high performance thin film transistors on plastic. *62nd Device Research Conference* University of Notre Dame, South–Bend, IN (June 21, 2004).

[3] Menard, E., Marchenko, A., Gershenson, M. E., Fichou, D. and Rogers, J. Fundamental science of transport and surface characterization of single crystal organic semiconductors. *Material Research Laboratory External Advisory Committee* Material Research Laboratory, Urbana, IL (April 5, 2005).

[4] Menard, E., Sun, Y., Khang, D. Y., Zhu, Z. T., Ahn, J., Meitl, M., Hur, S. H., Gaur, A. and Rogers, J. Materials and patterning techniques for flexible electronic systems. *Nanotechnology Workshop* Beckman Institute, Urbana, IL (May 5, 2005).

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[6] Menard, E., Marchenko, A., Podzorov, V., Gershenson, M. E., Rogers, J. A. and Fichou, D. Nanoscale morphology and transport of a single crystal organic semiconductor. *8th European Conference on Molecular Electronics* Bologna, Italy (June 29, 2005).