Etude d'un Convertisseur Analogique-Numérique à grande dynamique à base de portes logiques supraconductrices

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Michel MAIGNAN

DRFMC/SPSMS/Dispositifs Supraconducteurs

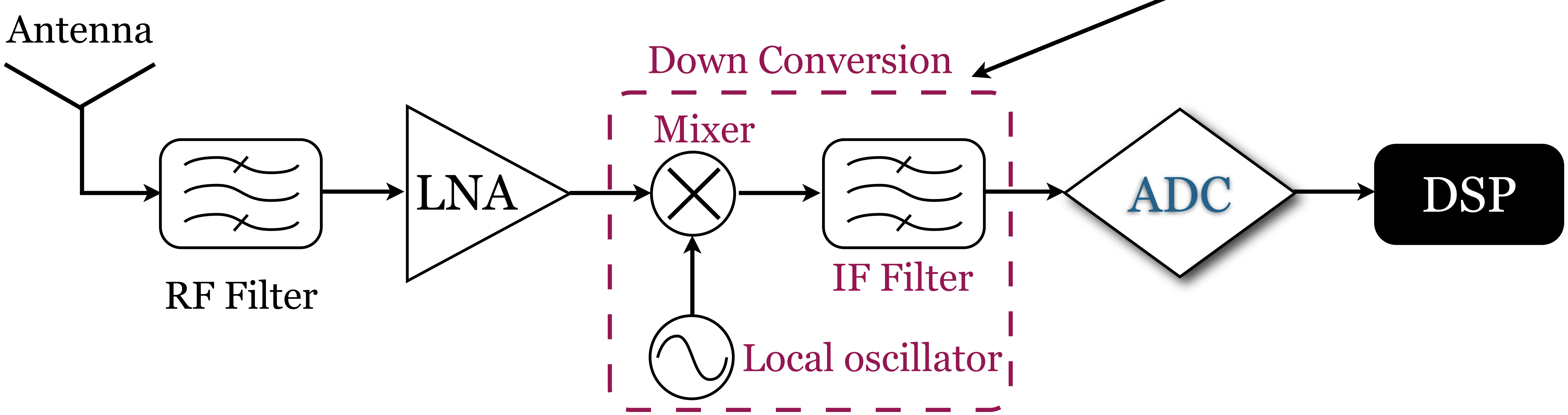
Plan de l’exposé

- Introduction
- Rappels sur le CAN et l‘Electronique supraconductrice
- Etude de la structure du CAN en NbN
- Implémentation et comparaison de la technologie NbN et Nb
- Conclusions et perspectives

Contexte

Space Telecommunications

Bit Rate Information Increasing → Bandwidth and Carrier Increasing → Noise Increasing in Analog Parts



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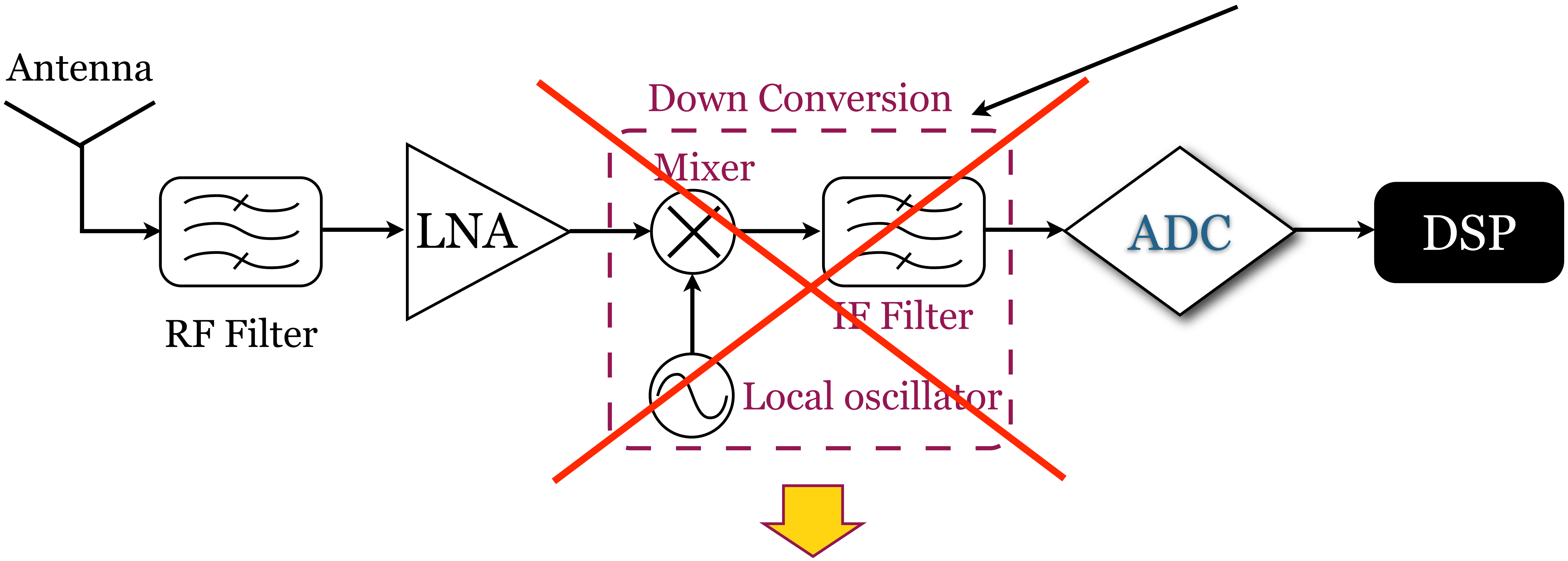
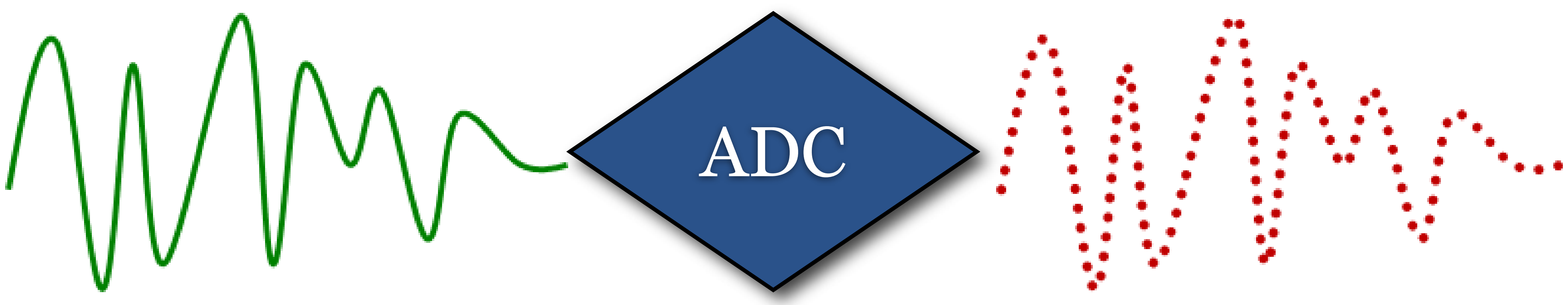


Digitalization of RF signals for Software Defined Radio (SDR) systems

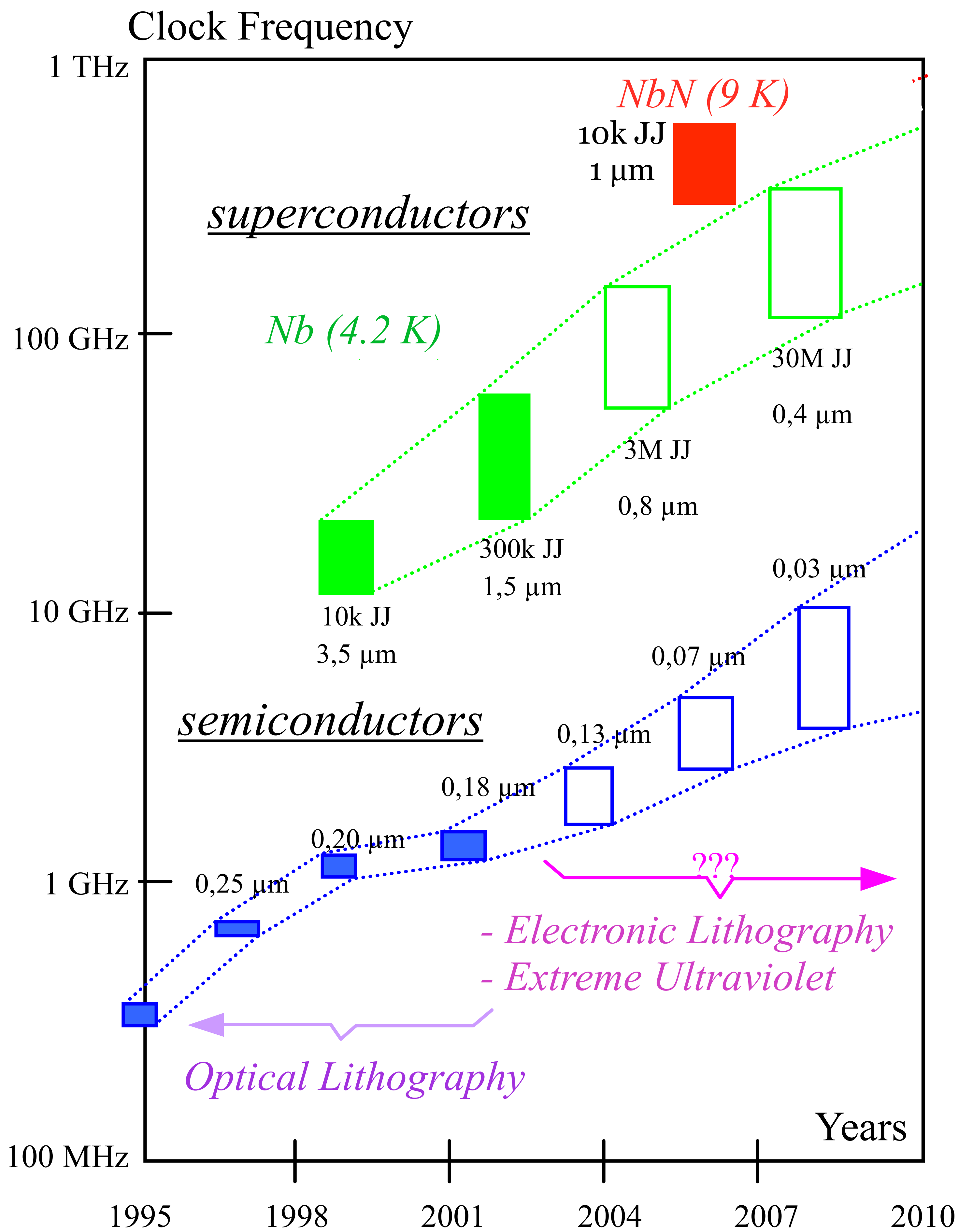


SNR ~90 dB

Signal-to-**N**oise **R**atio

Pourquoi la logique RSFQ?

Rapid Single Flux Quantum logic based on Josephson junctions



✓Superconductor transmission lines

Very small dispersion
Very small attenuation
Very small dissipation

✓Switching time about 1-3 picoseconds

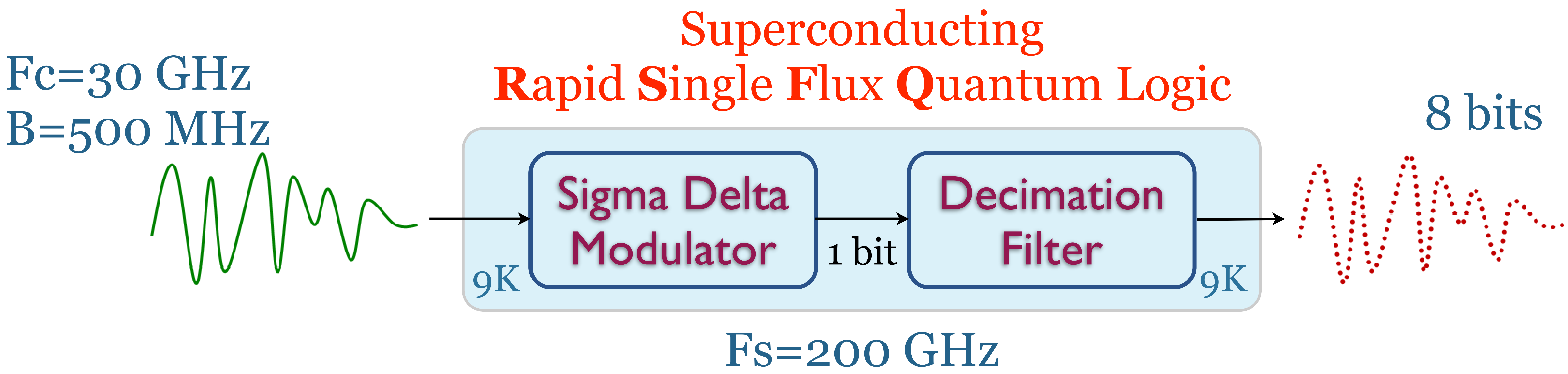
High Frequency (0.5-1 THz)

✓Power consumption of 2 orders lower then a CMOS transistor considering the cryocooler power

High Bit Rate

Objectif

Analog-to-Digital Converter based on ∑Δ Architecture



✓Niobium Nitride (NbN) superconductor (Tc=16 K)

New technology:

✓ **Self-shunted Josephson junctions NbN/Ta_XN/NbN**

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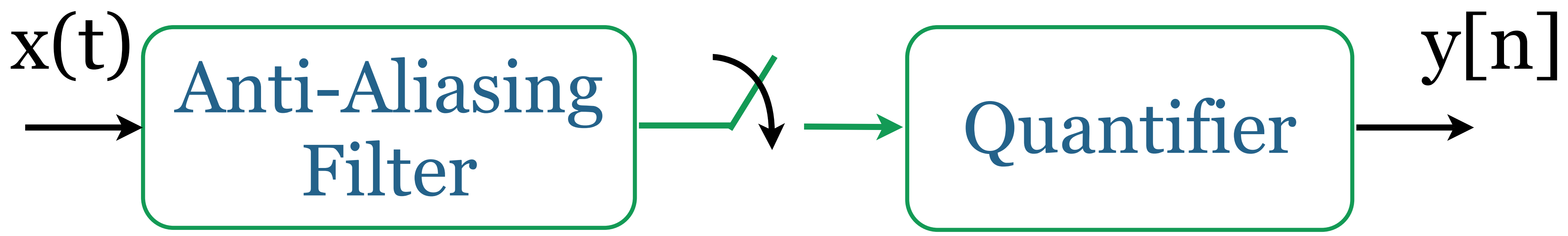
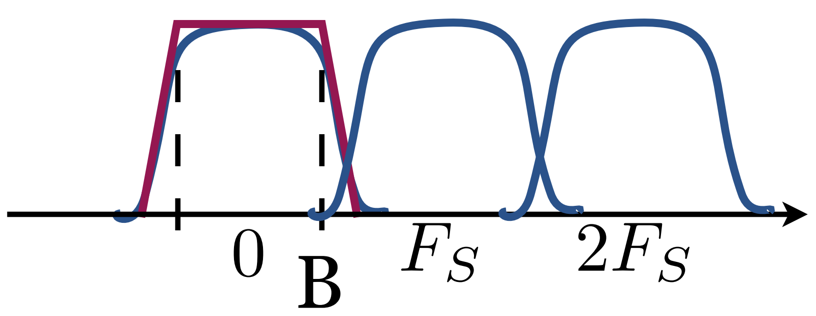
La modulation Sigma-Delta

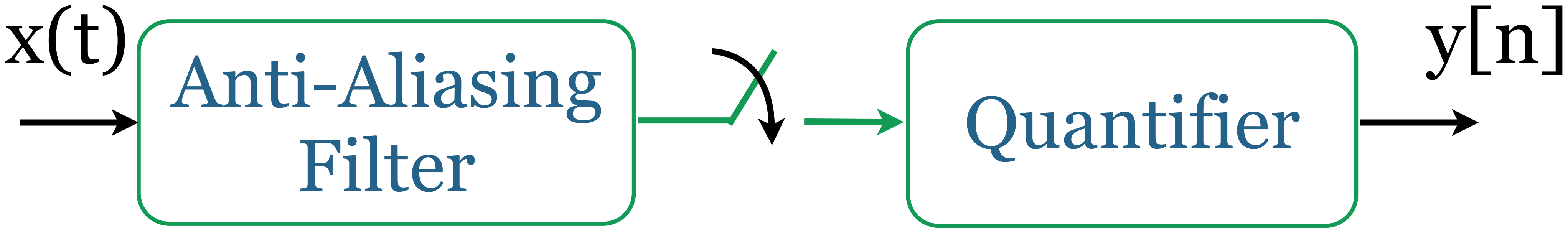
Fs=2B (Nyquist Sampling)

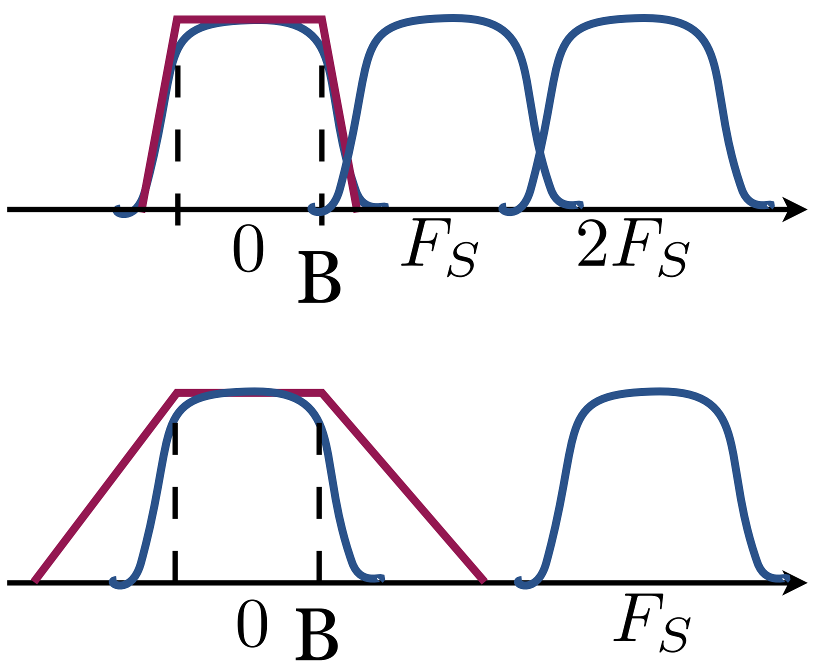




La modulation Sigma-Delta

✓Oversampling : Fs>2B





Less selective filter

La modulation Sigma-Delta

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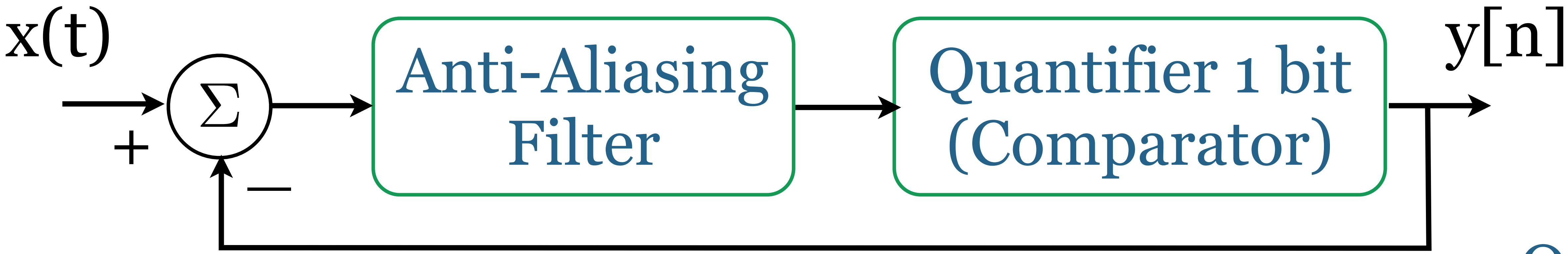
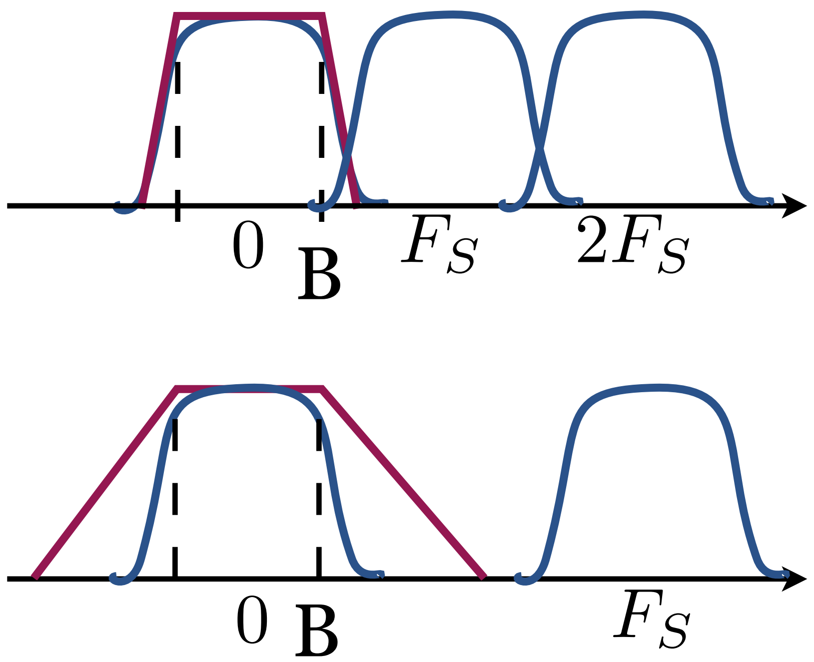


1 bit

✓ Noise shaping



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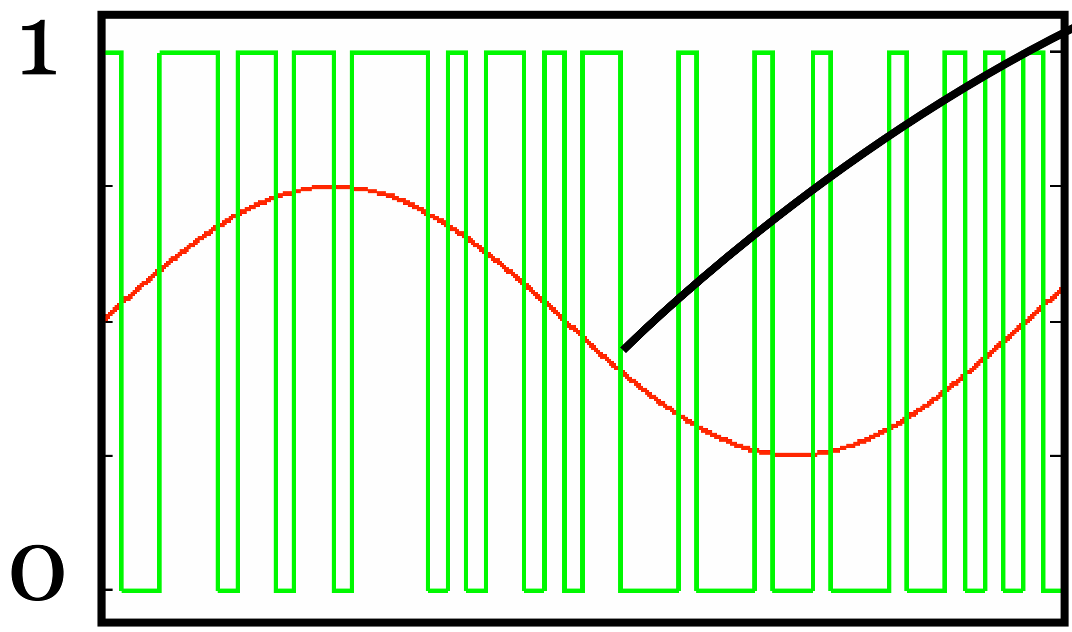
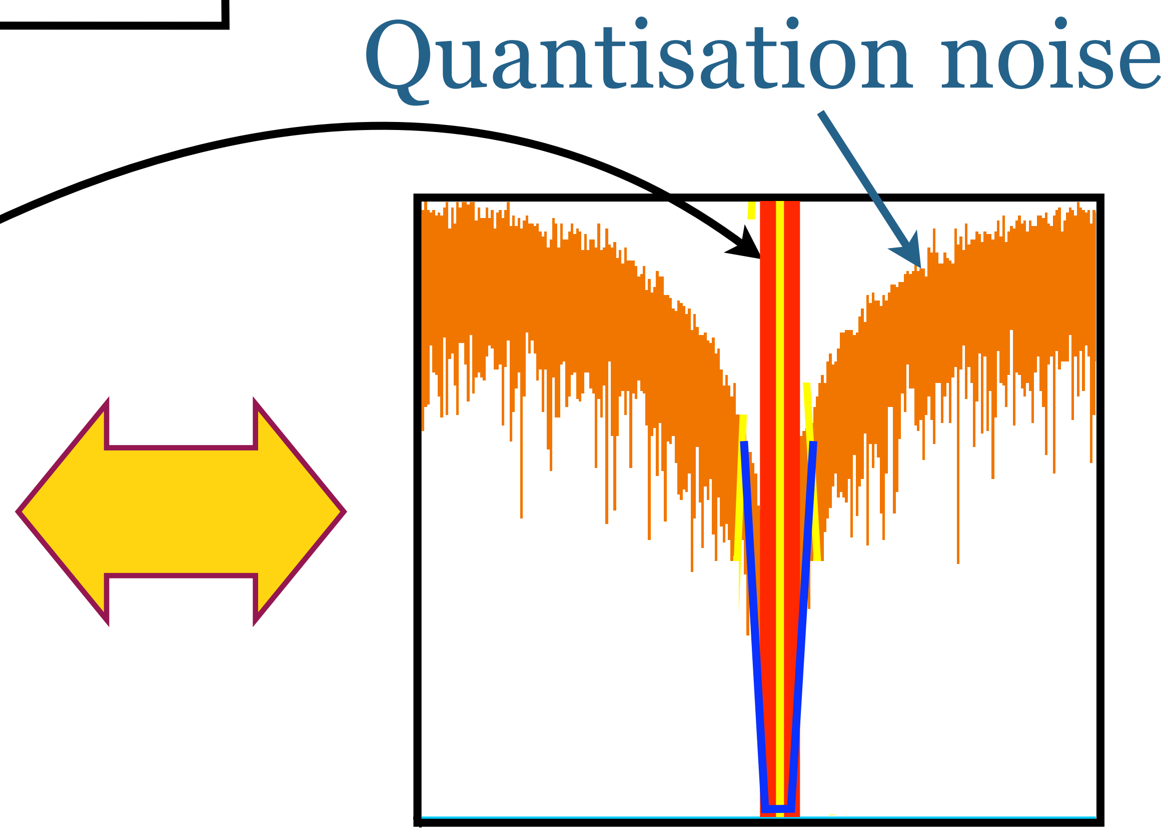


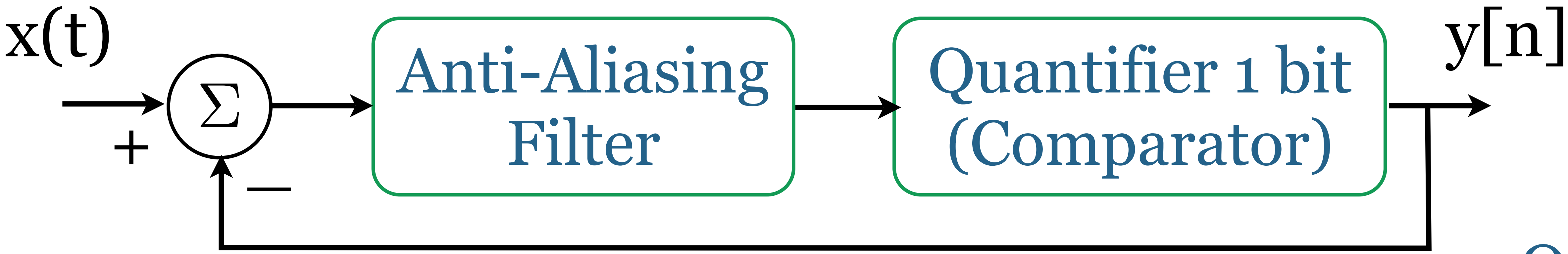
Time domain



Frequency domain

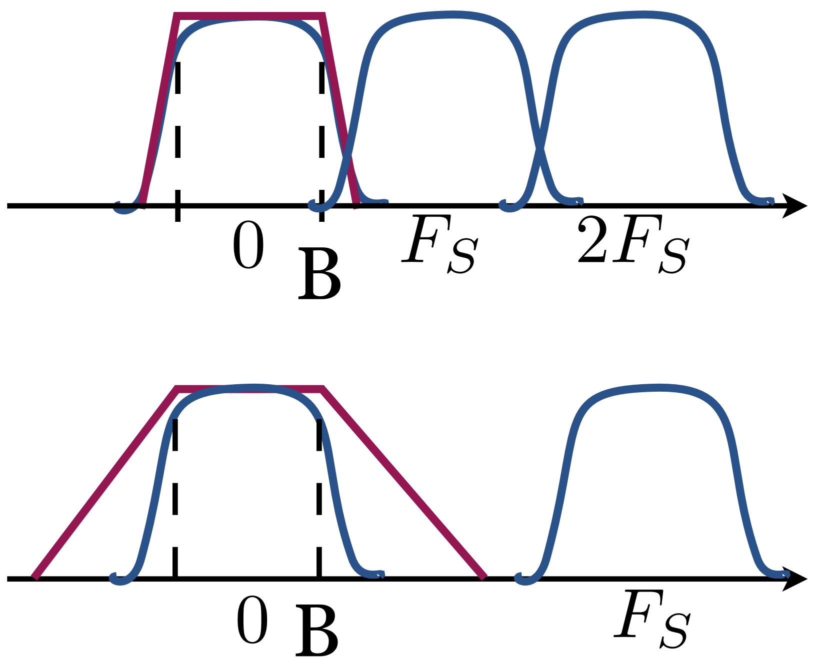
La modulation Sigma-Delta

✓**Oversampling : Fs>2B**



✓ **Noise shaping**

Quantisation noise



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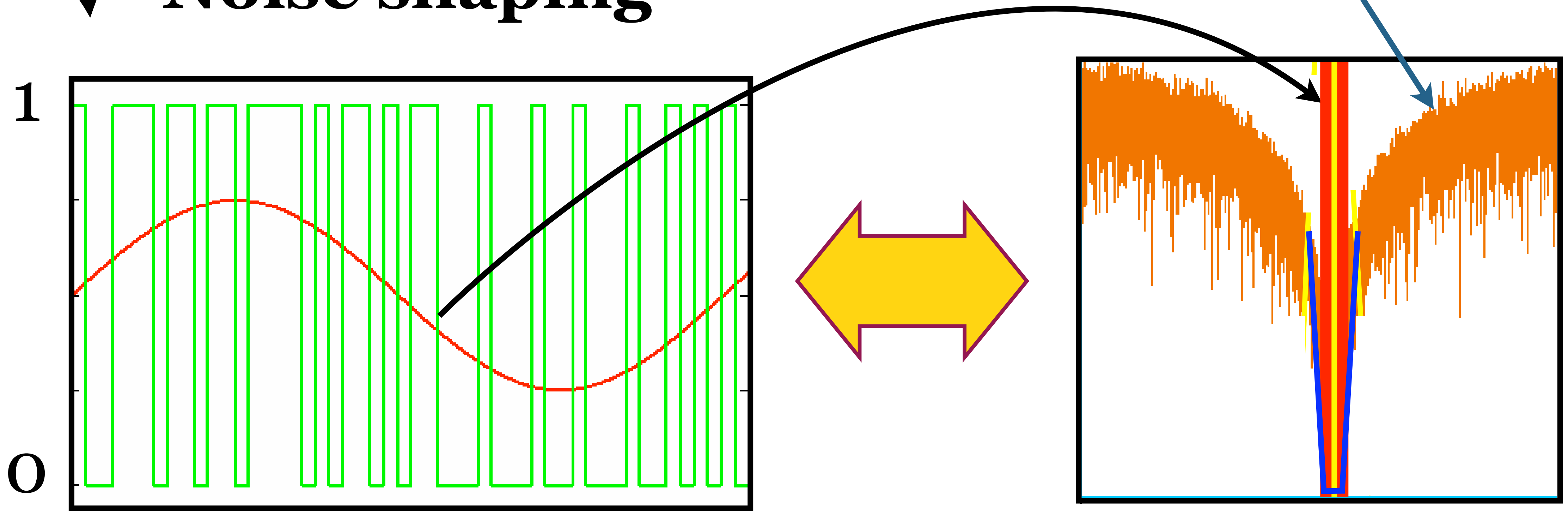

Time domain

Frequency domain

Transfert Function Order ➡ Modulator Order (l) ↗

$$H(s) = \frac{Y(s)}{X(s)}$$

Oversampling Ratio (OSR) ↗

OSR=Fs/2B

➡ SNR **S**ignal-to-**N**oise **R**atio ↗

Le filtre de décimation

Increases the resolution of the conversion

Resolution 1 ⟶ M bits ➡ **Decimation Factor** ⟶ $N = 2^M$

Mean over N bits of the modulator output

Sigma-Delta Modulator 1 Bit Output

Time

0 1 0 1 1 1 0 0 1 0 1 0 1 1 0 1 0 1 0 1 1 0

9 bits at *1* over 16 bits

$$\frac{9}{16} = 0.5625$$

Decimation Filter Output

1 0 0 1

Sinc Filter

$$H(f) = \left[\frac{sinc(Nf/f_S)}{sinc(f/f_S)}\right]^{k}$$

The filter order (*k*) must be higher than the modulator order (*l*)

$$k = l + 1$$

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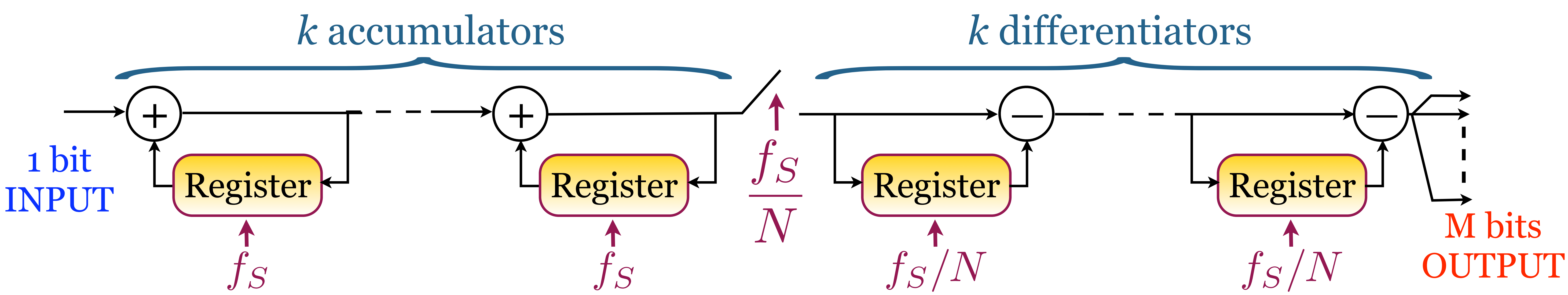
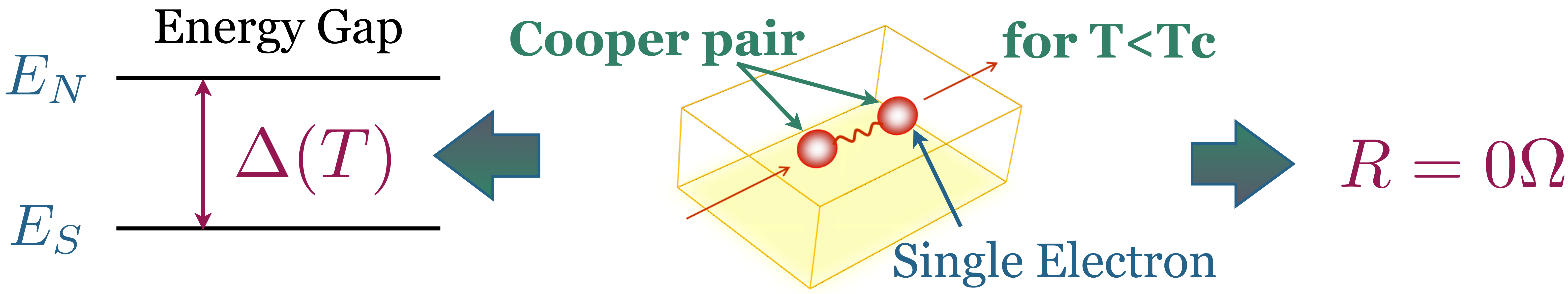
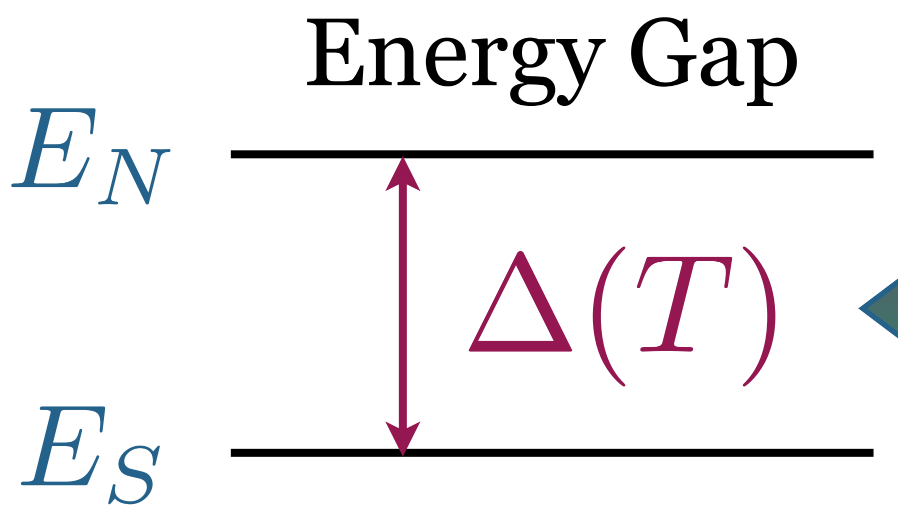
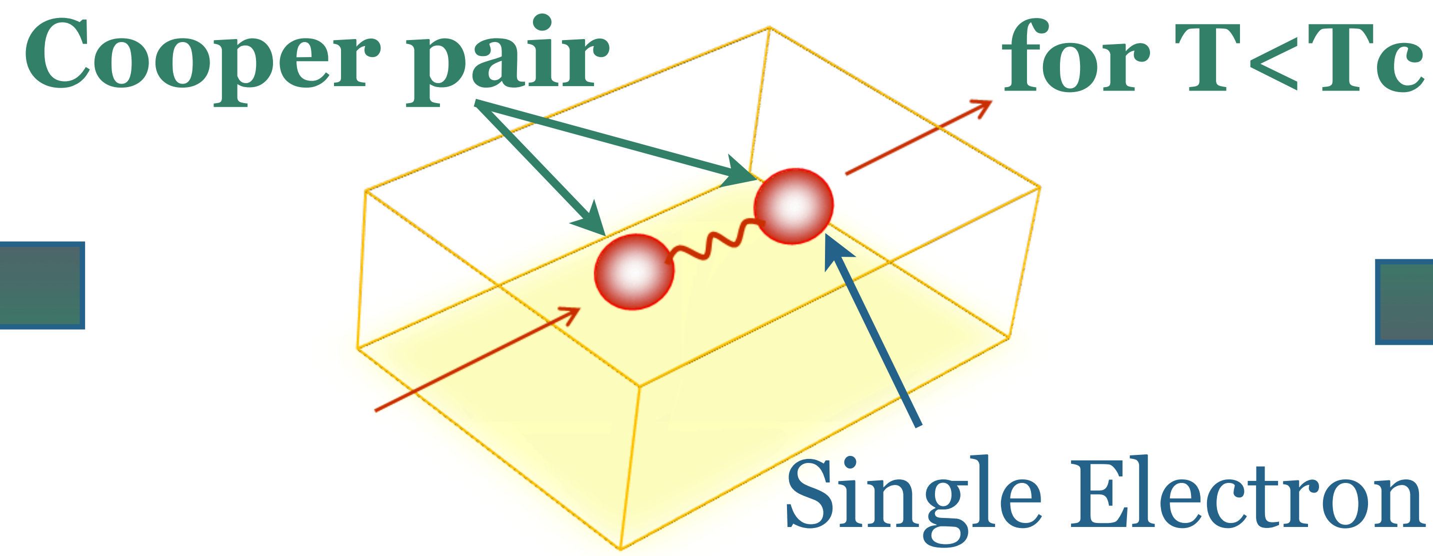


Lignes supraconductrices

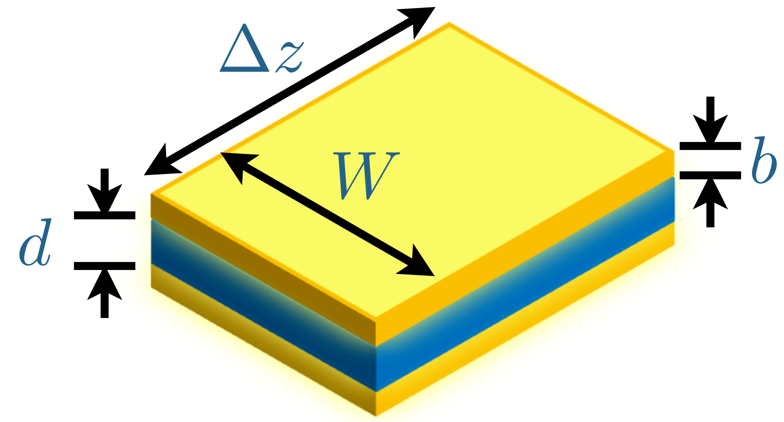


Lignes supraconductrices

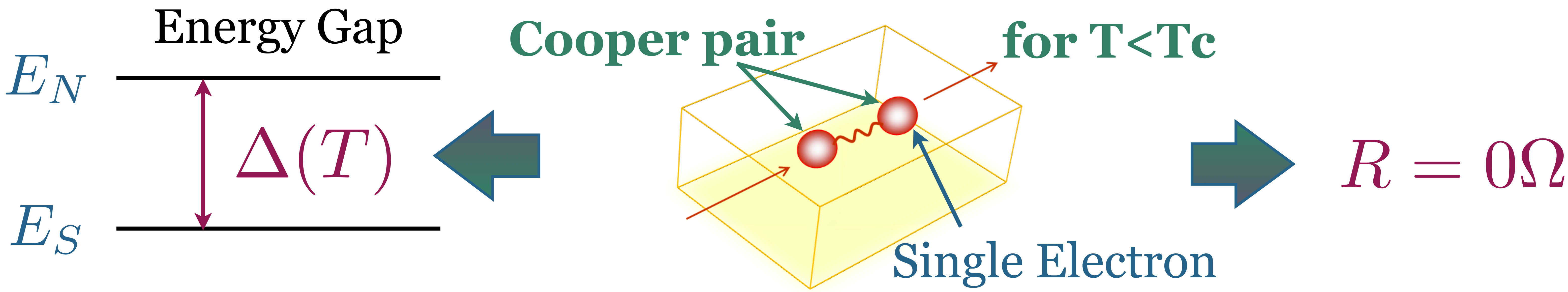


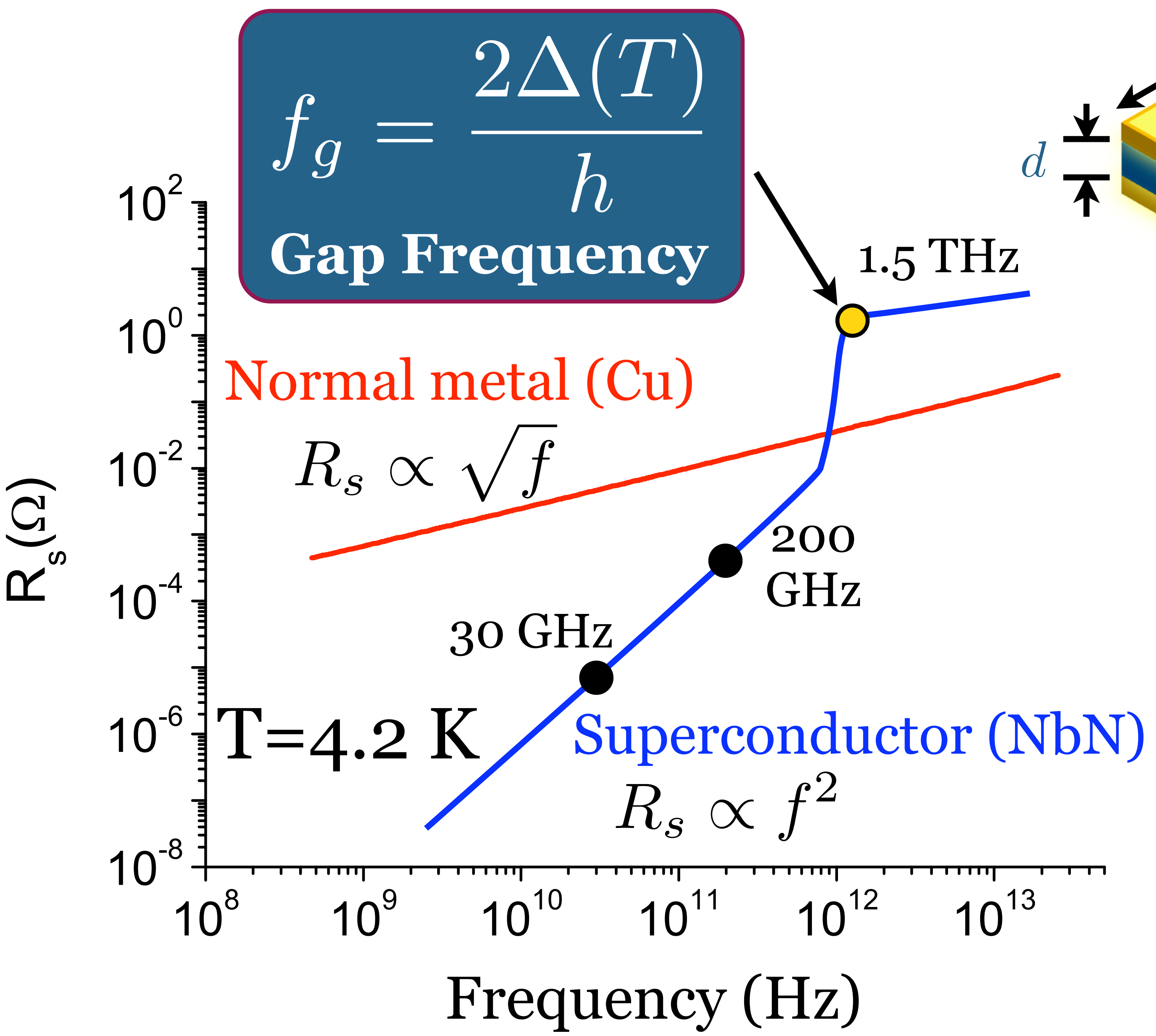


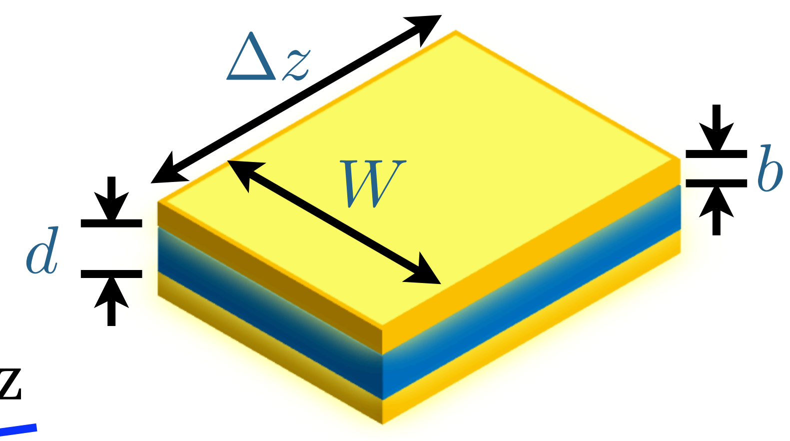
$R = 0\Omega$



Lignes supraconductrices







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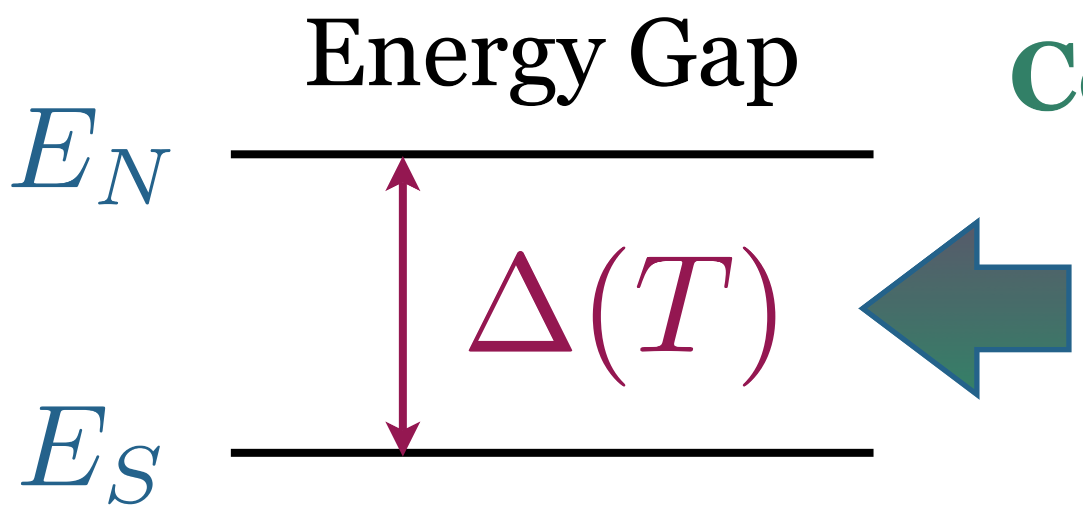
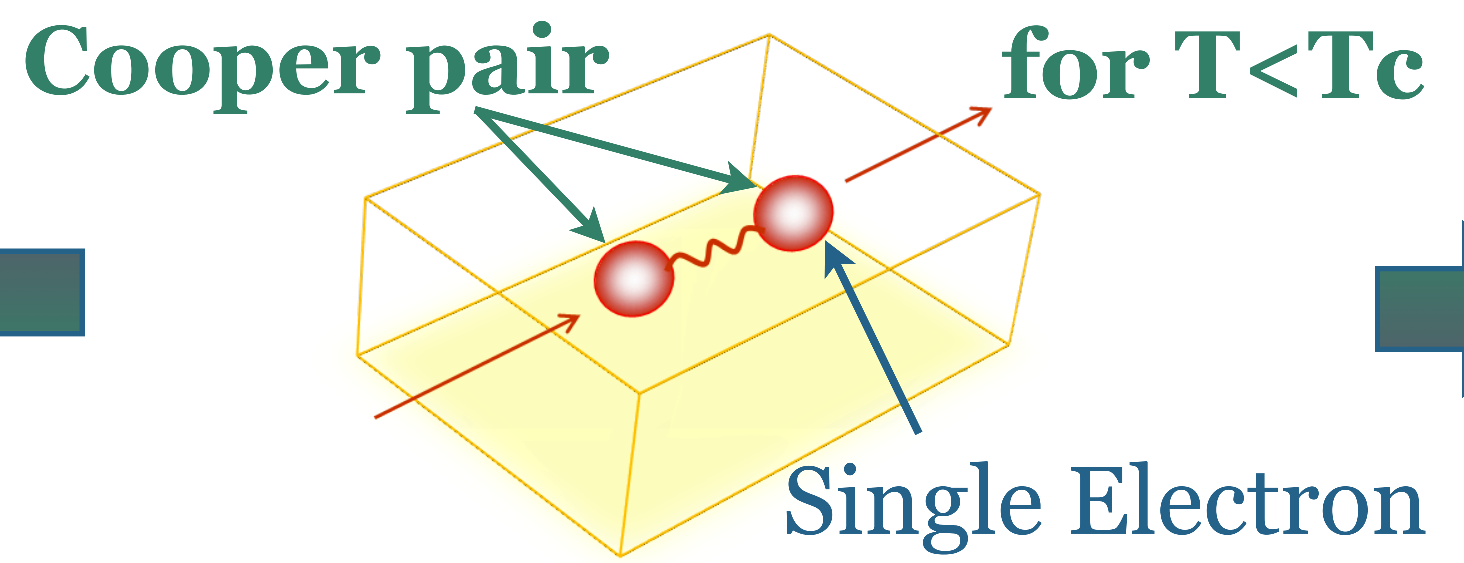
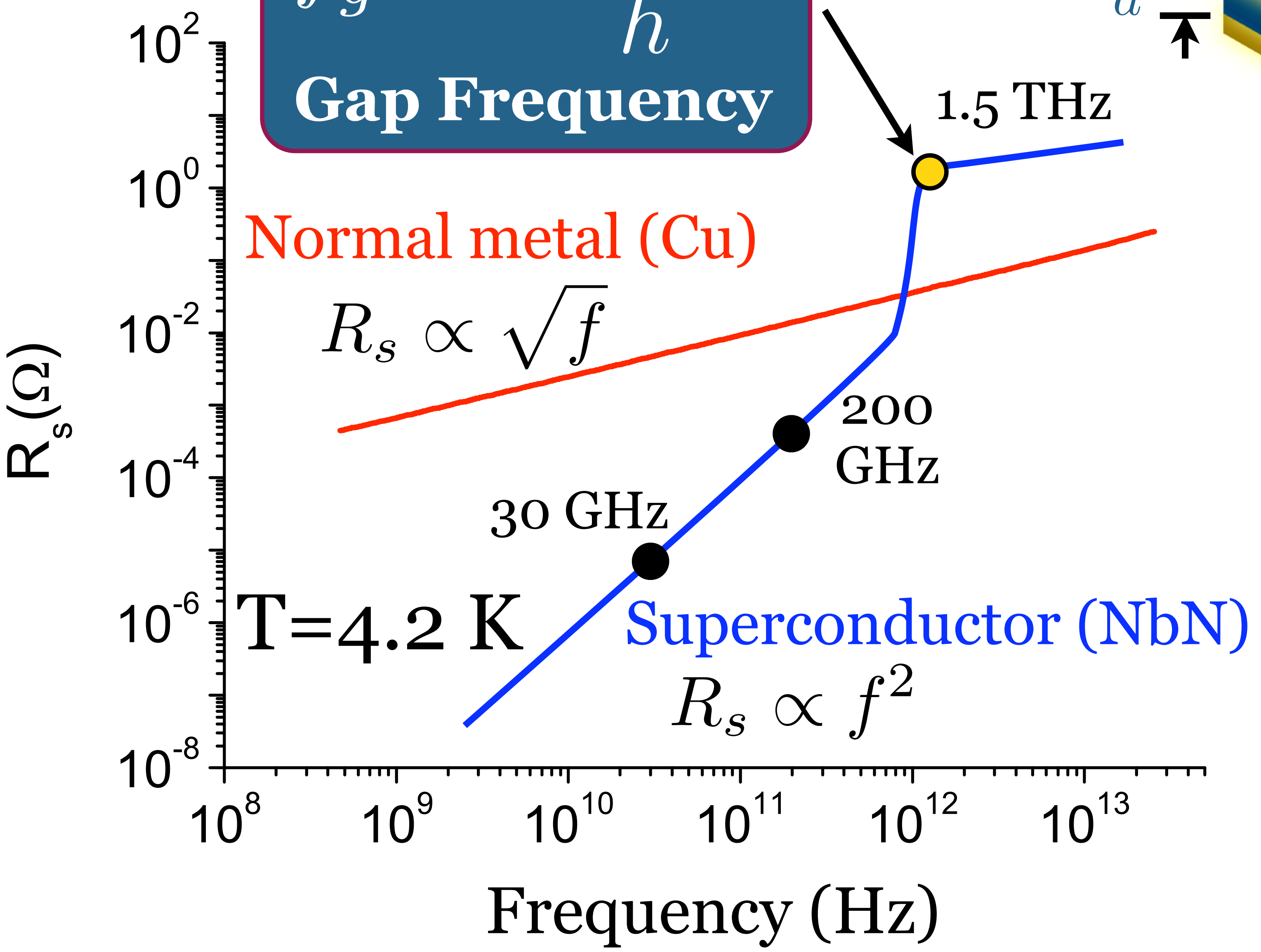


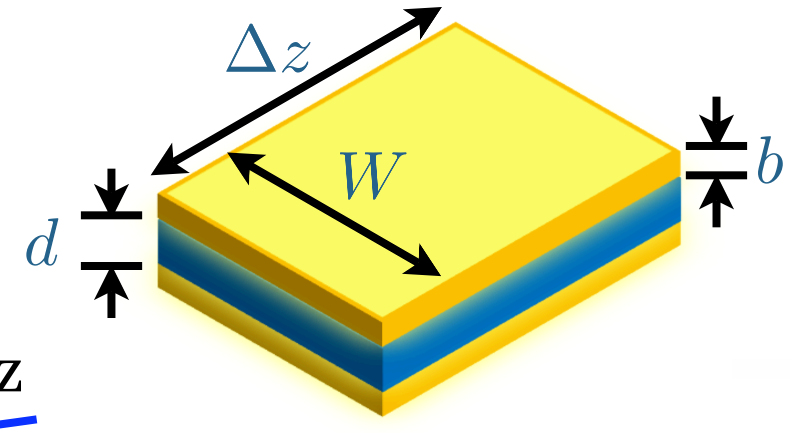


$R = 0\Omega$

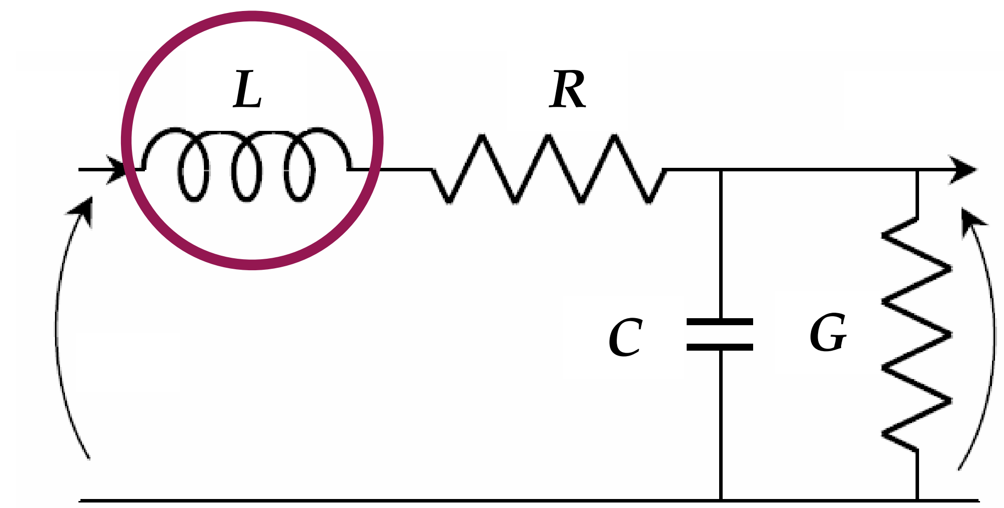
$$f_g = \frac{2\Delta(T)}{h}$$

Gap Frequency





Equivalent Transmission Line circuit

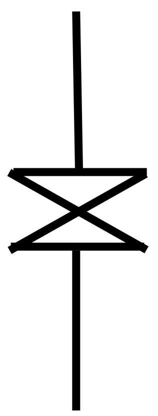


$$L(w, d, b, \boxed{\lambda_L})$$

$$\lambda_L(T) = \lambda_L(0)[1 - (T/T_C)^4]^{-1/2}$$

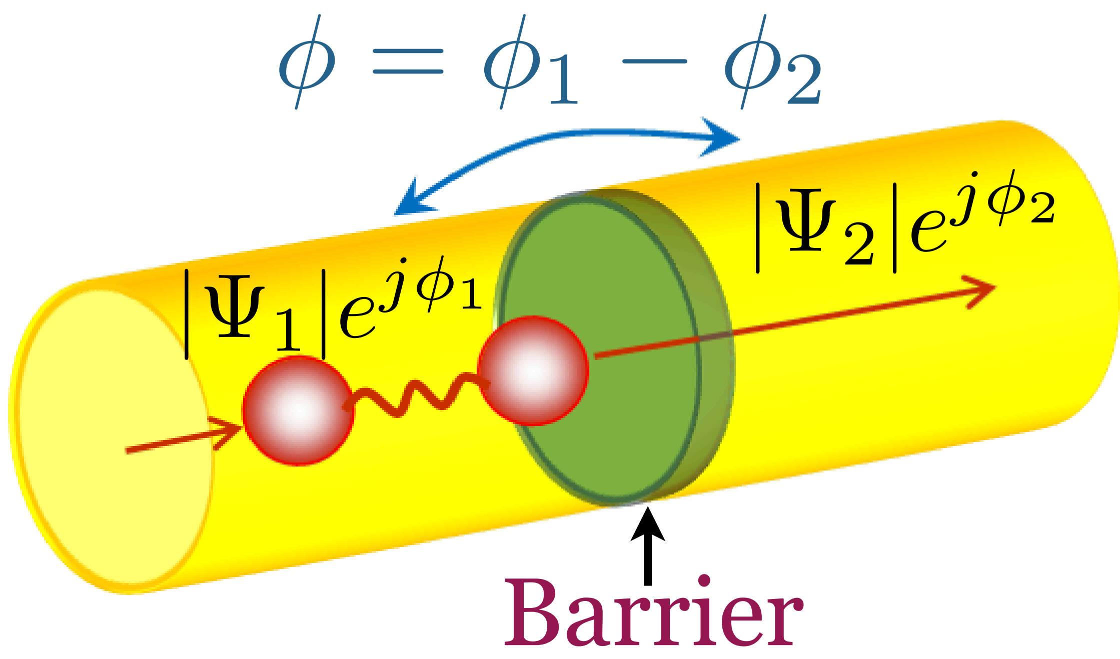
London Penetration Depth

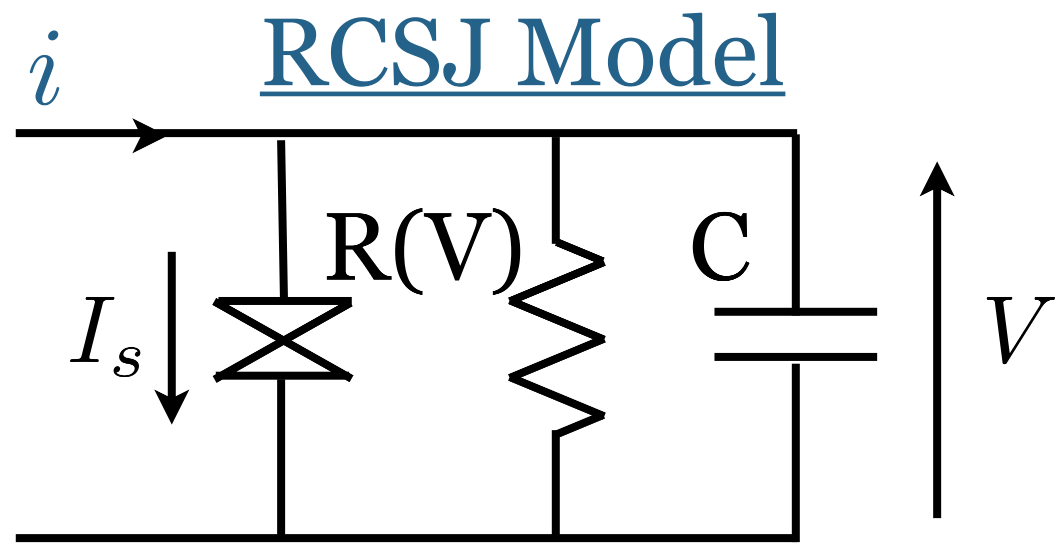
La jonction Josephson (JJ)



$$I_s = I_c \sin\phi$$

$$V = \frac{\Phi_0}{2\pi}\frac{d\phi}{dt}$$



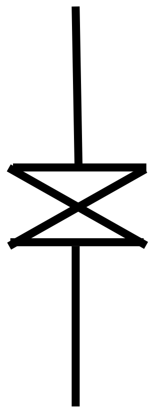


$$i = \beta_c\ddot{\phi} + \dot{\phi} + \sin\phi$$

$$\beta_c = \frac{2\pi I_C R(V)^2 C}{\Phi_0}$$

Stewart-McCumber Factor

La jonction Josephson (JJ)



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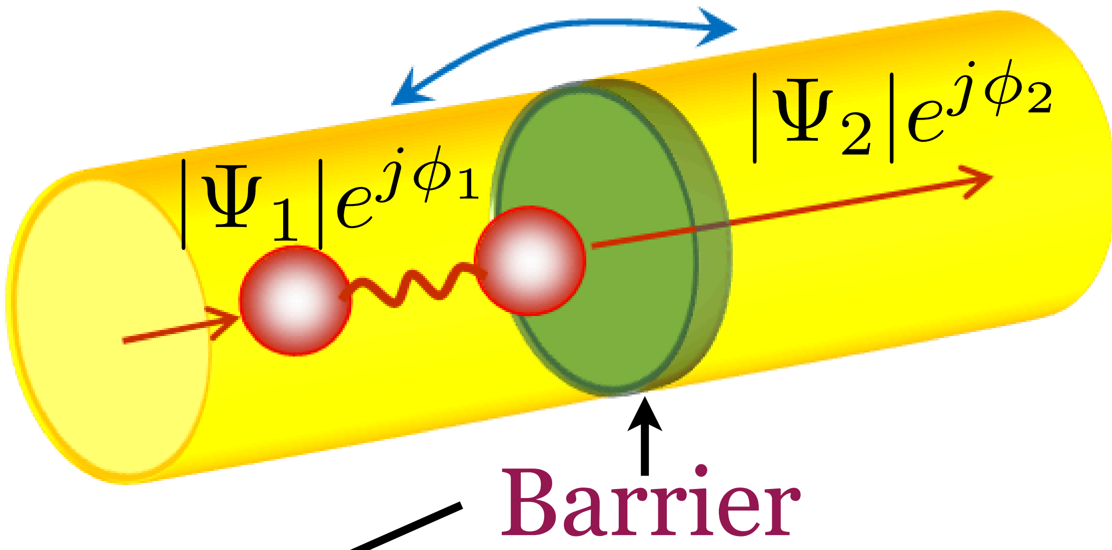
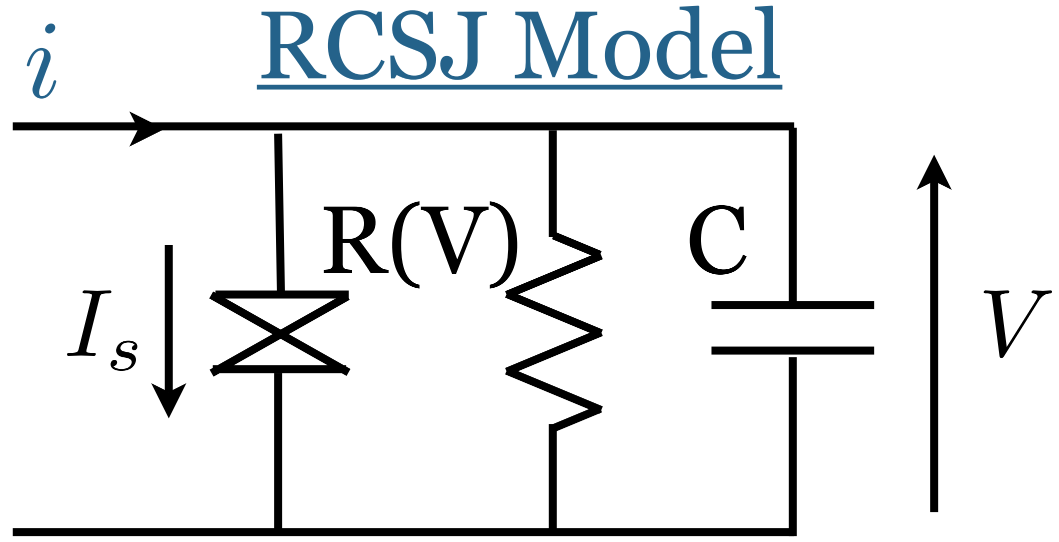


RCSJ Model



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Superconductor-Insulator-Superconductor

(Tunnel Effect)

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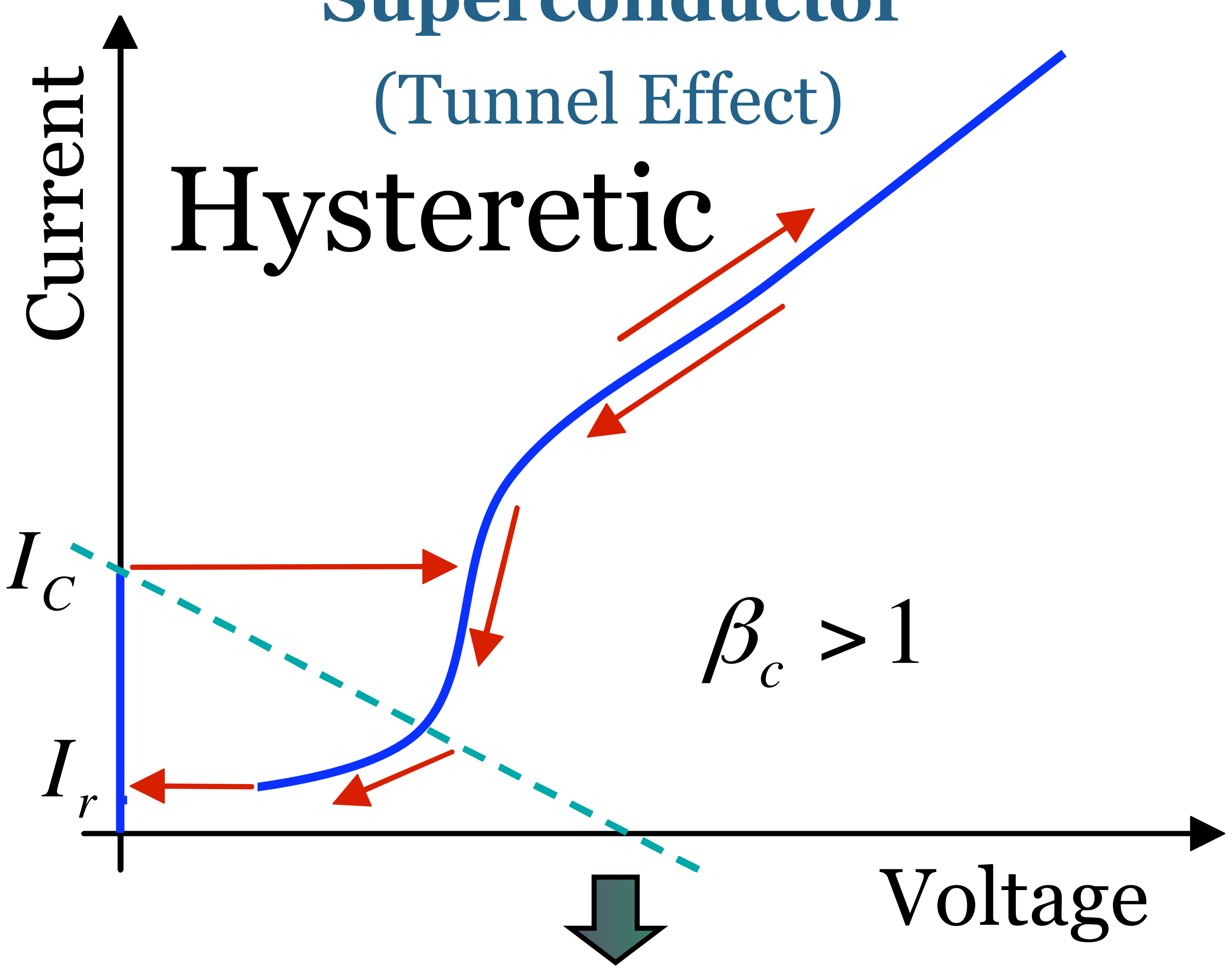
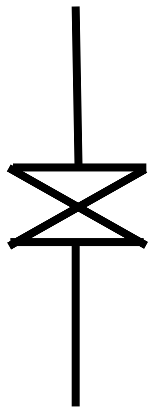


***Latching** Logic*

La jonction Josephson (JJ)



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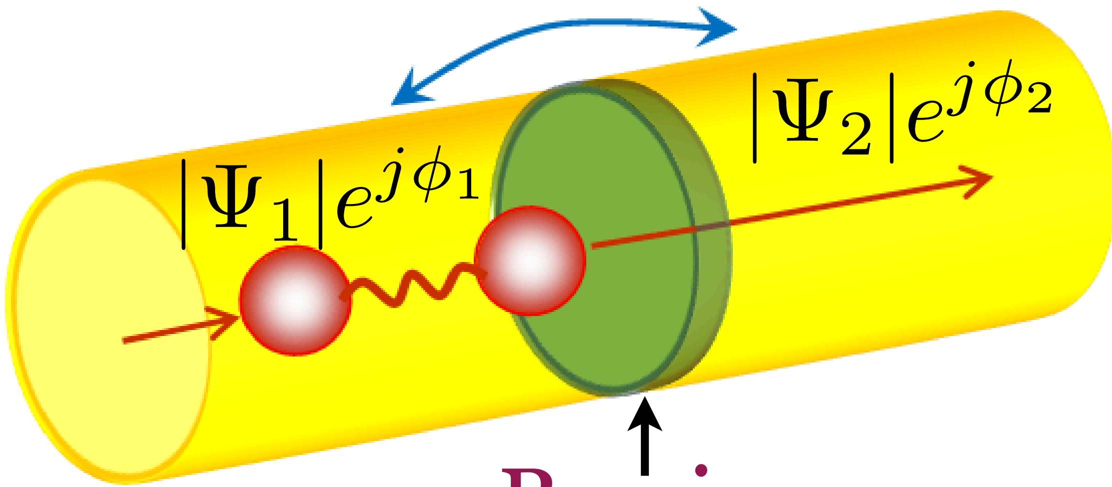
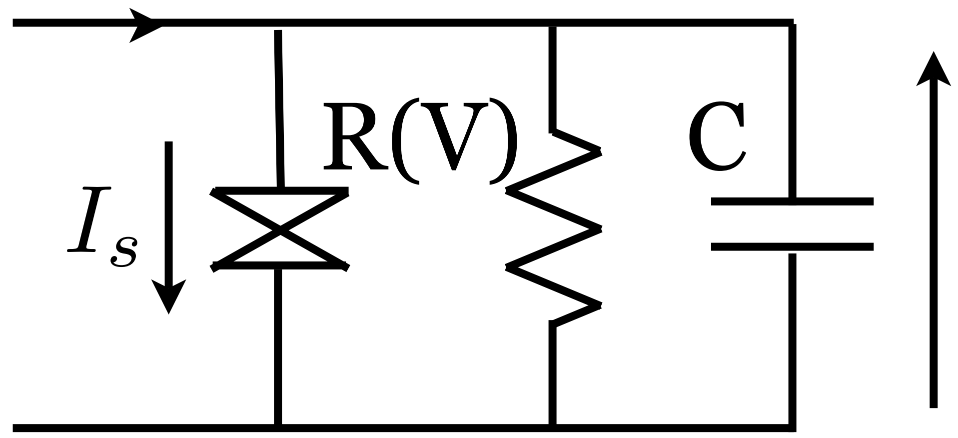


Barrier

RCSJ Model



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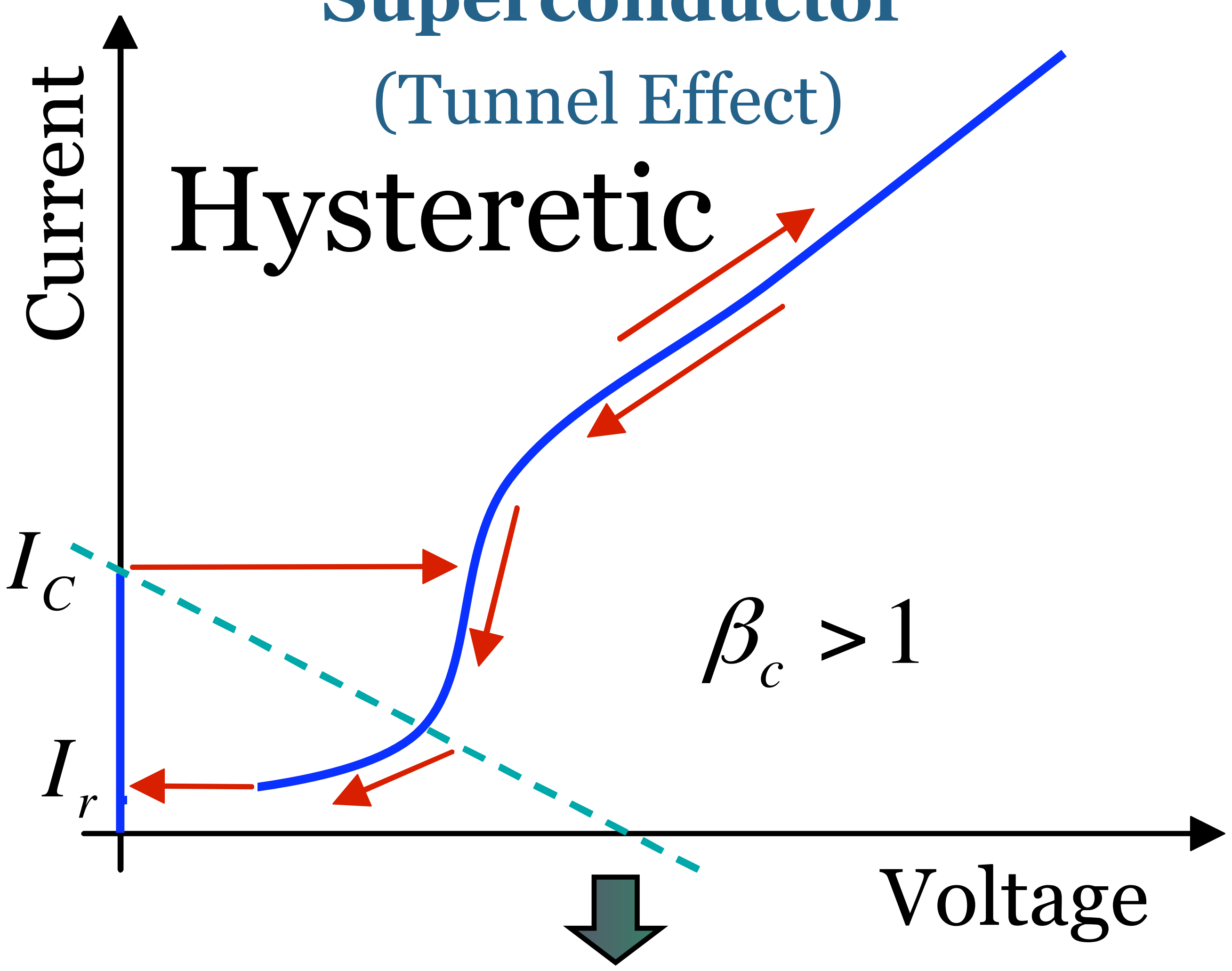
Stewart-McCumber Factor

Superconductor-
Normal Metal-
Superconductor
(Proximity Effect)



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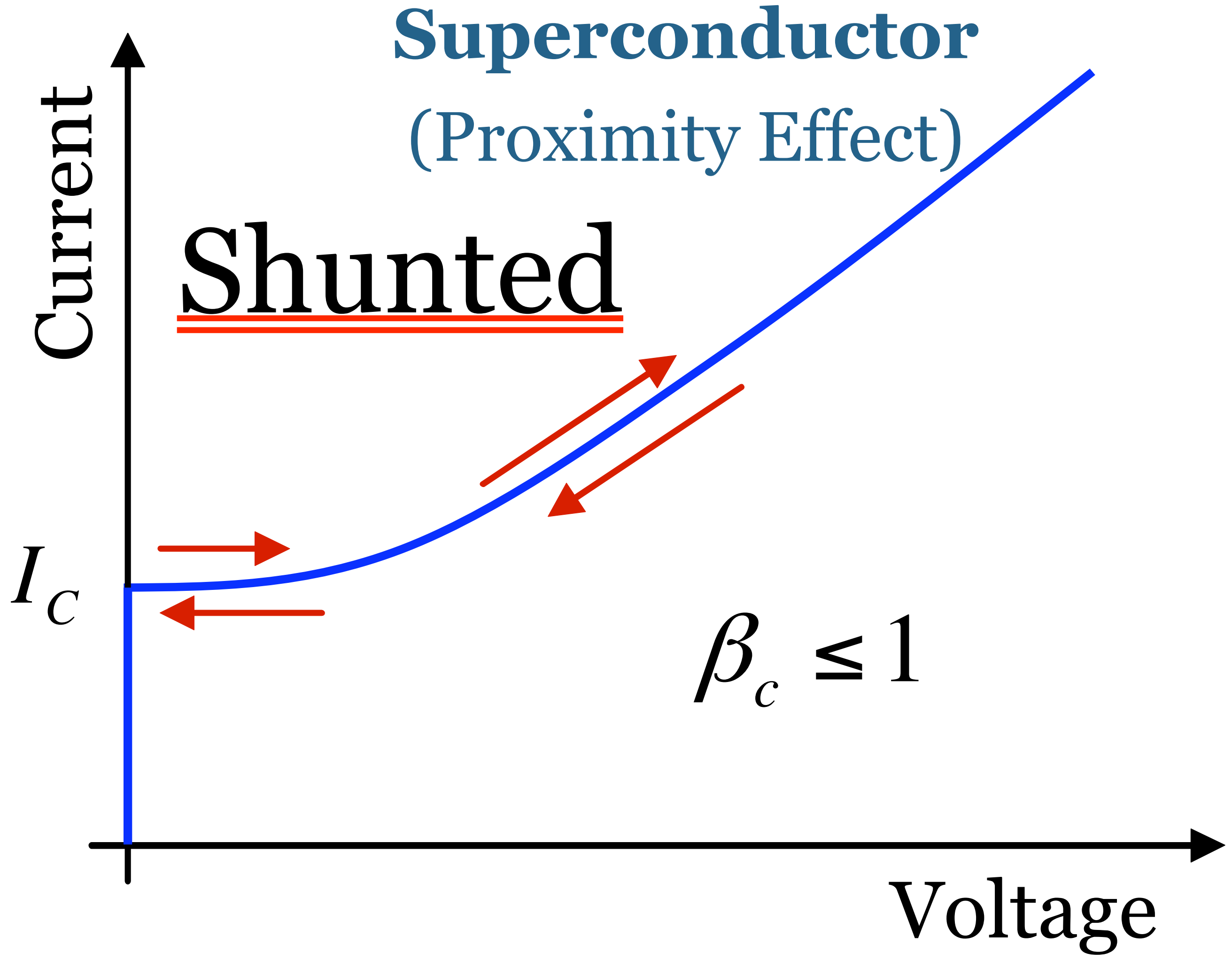

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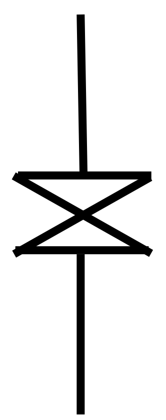

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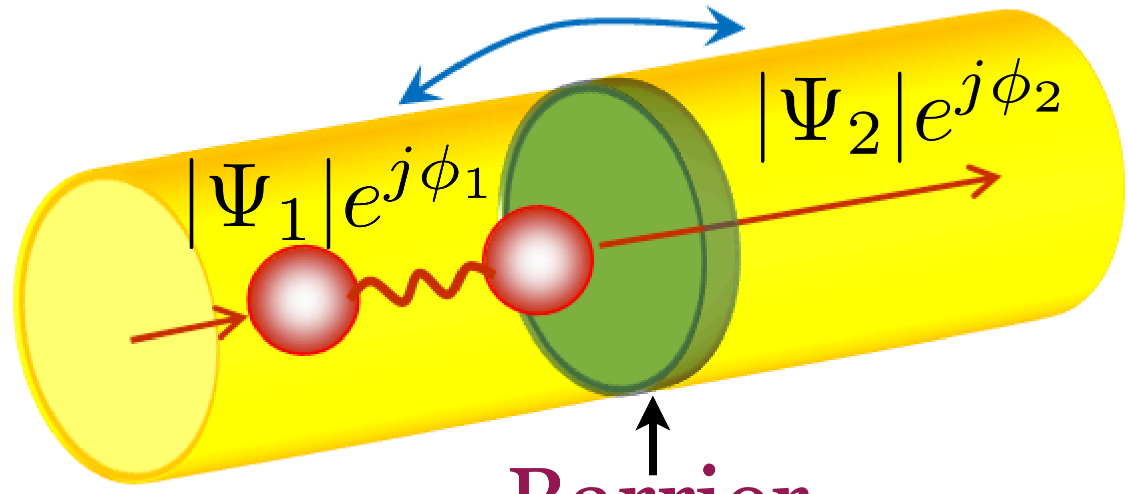

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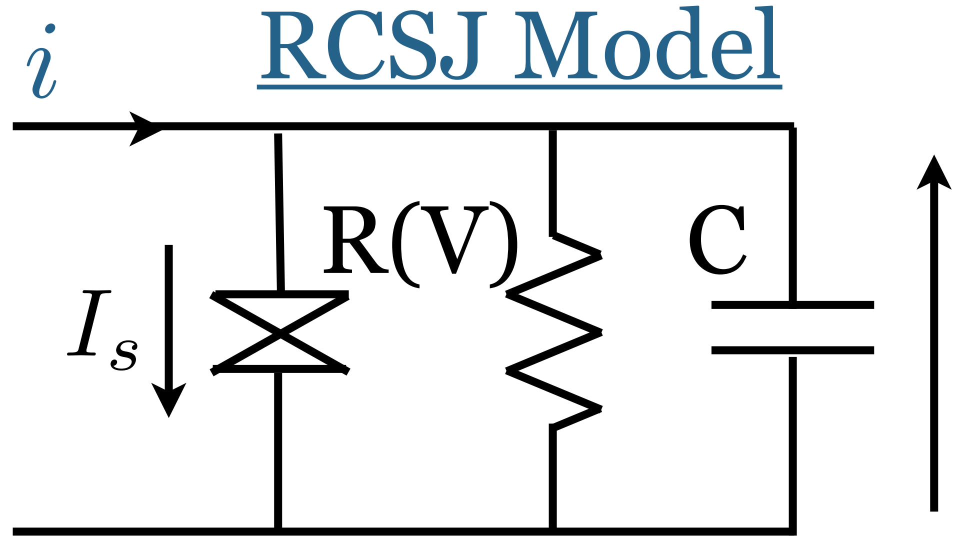

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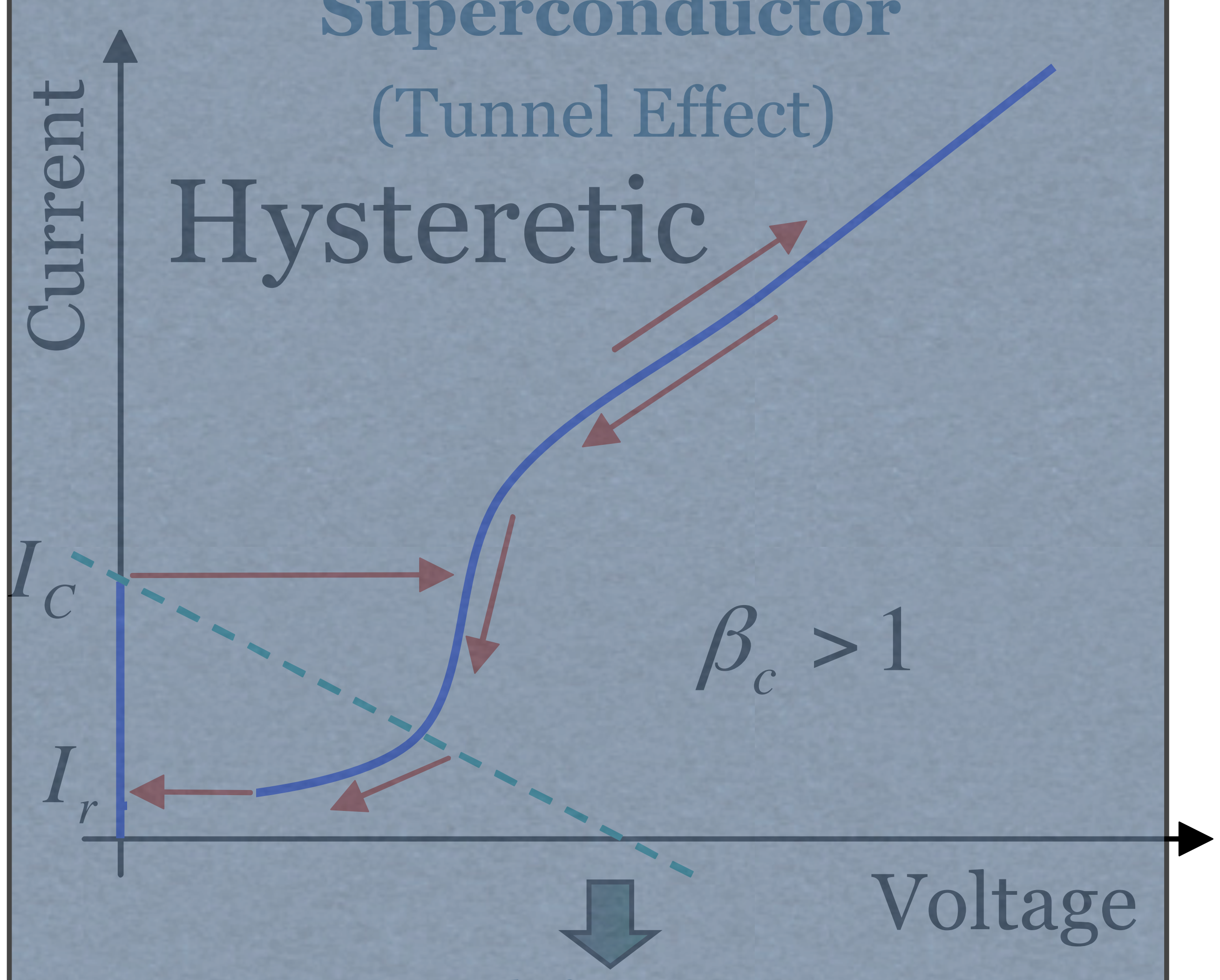
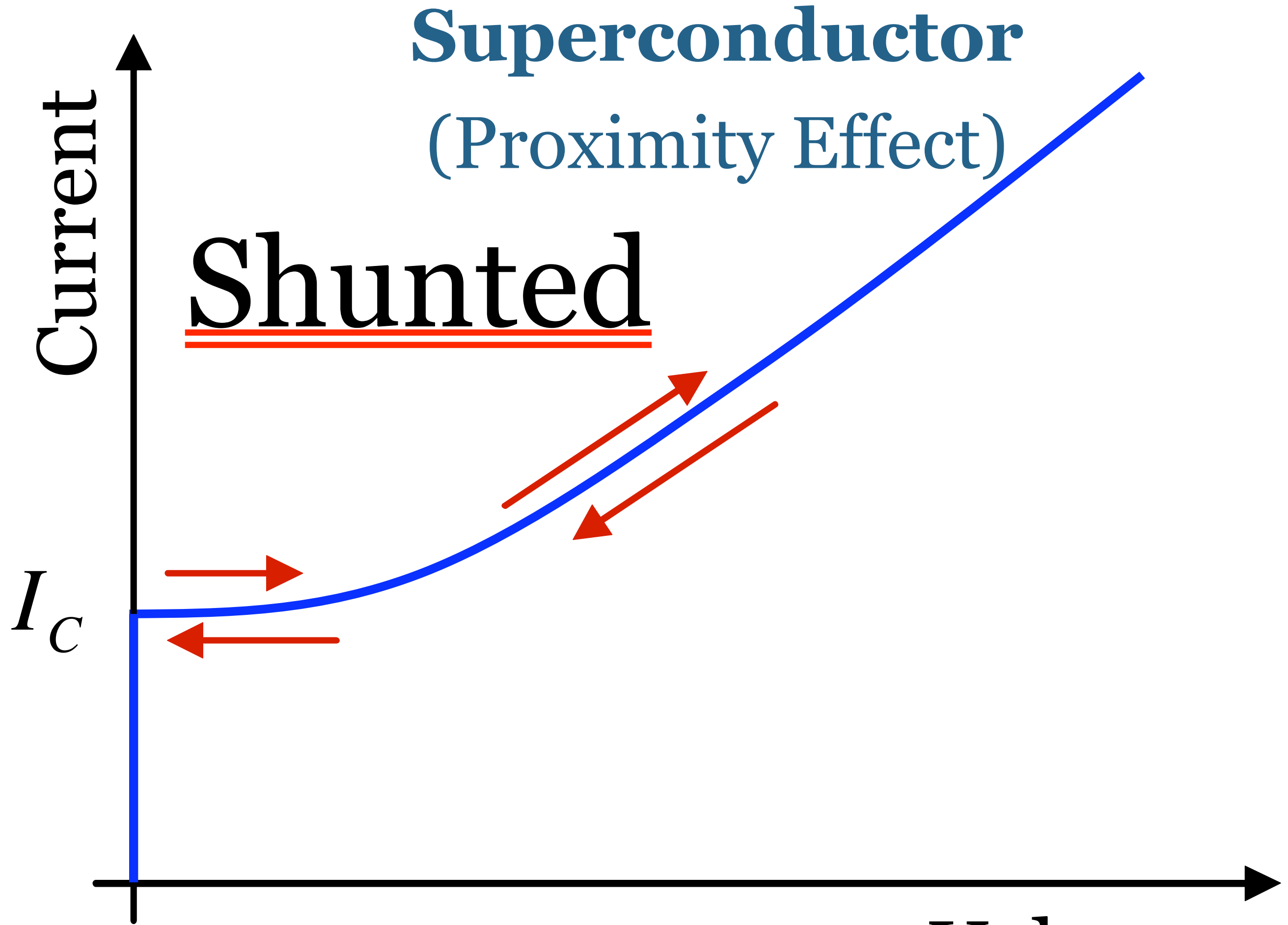
(Tunnel Effect)



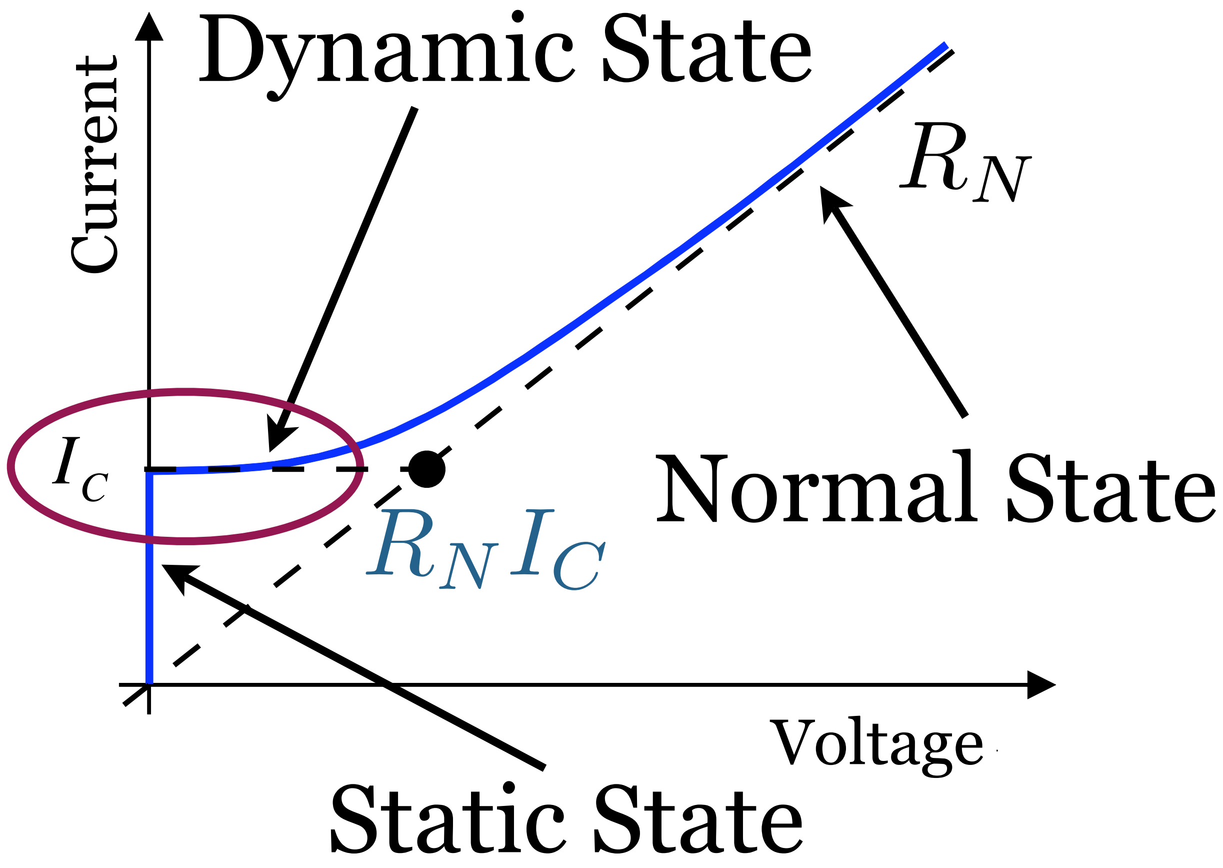
Latching Logic

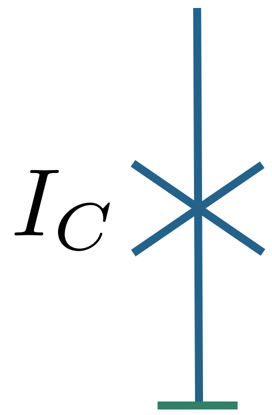
Superconductor-Normal Metal-Superconductor

(Proximity Effect)

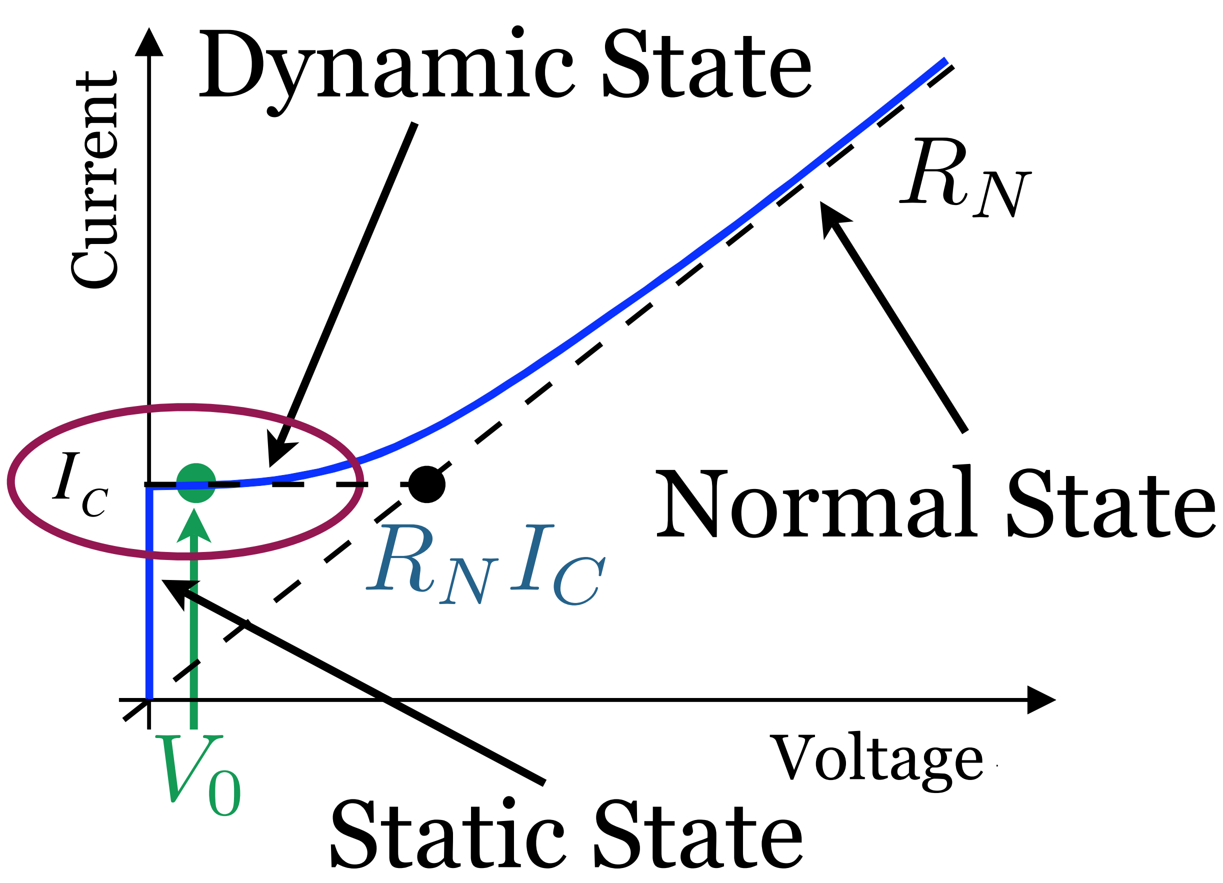


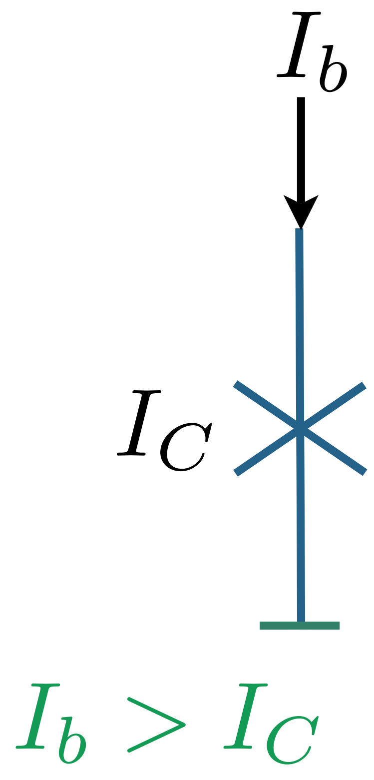
RSFQ Logic

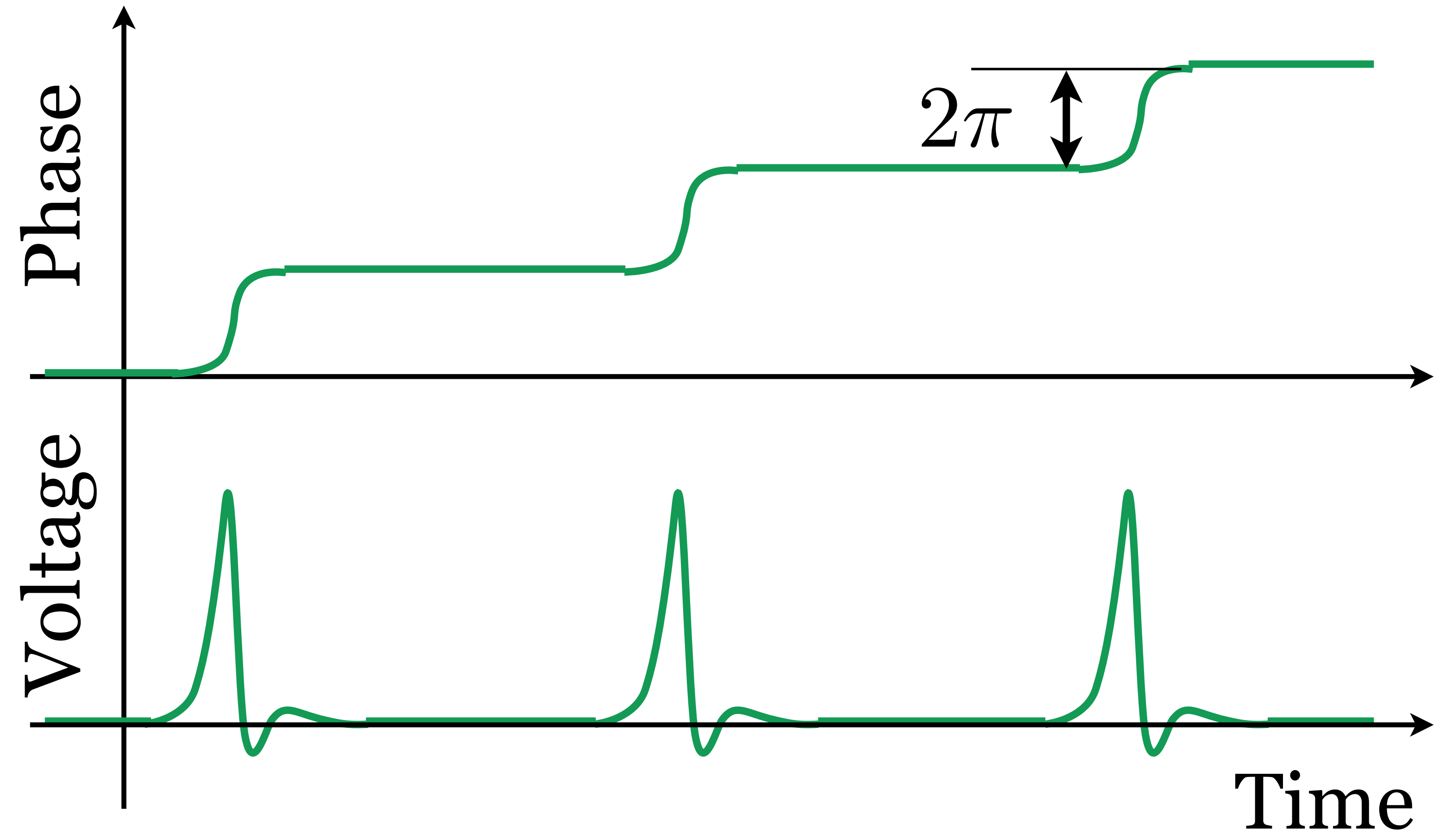

Dynamic State
Current
R_N
I_c
Normal State
$R_N I_C$
Voltage
Static State


I_C

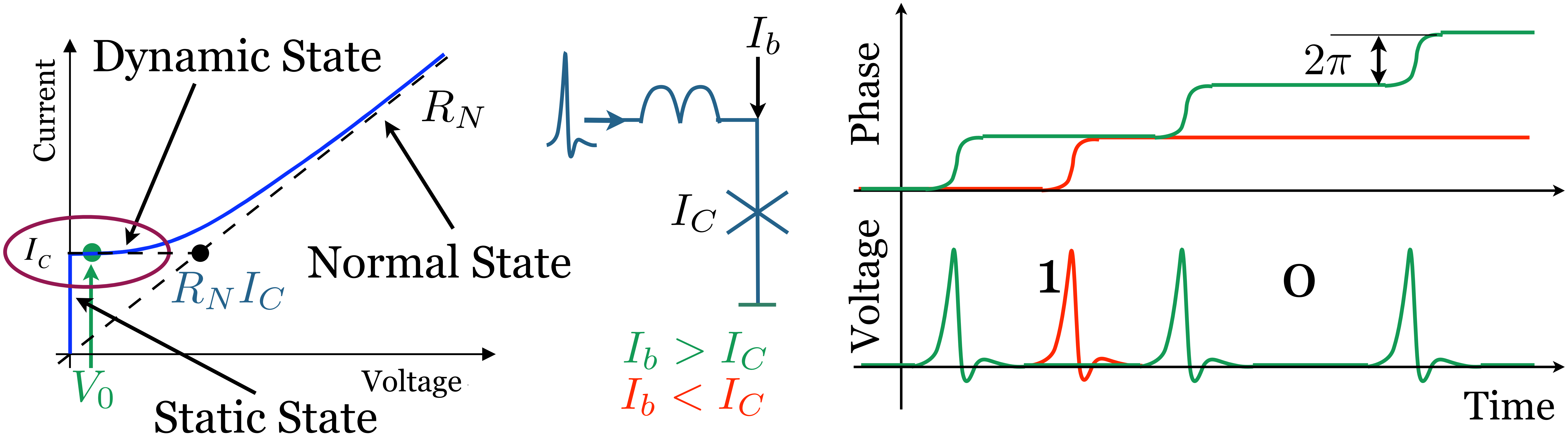
Le principe de la logique RSFQ



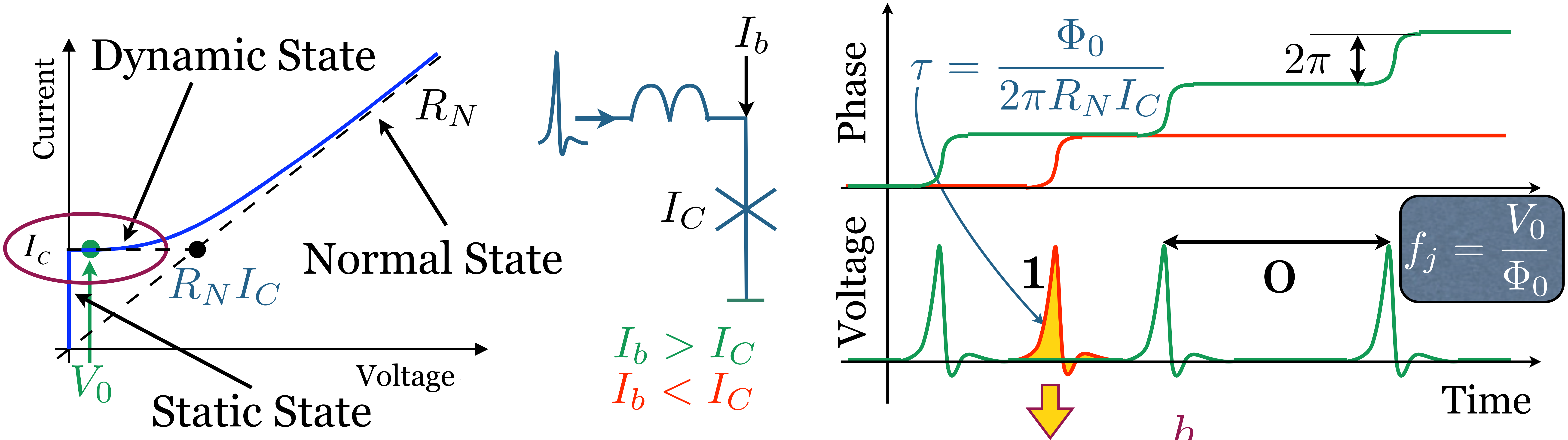




Le principe de la logique RSFQ

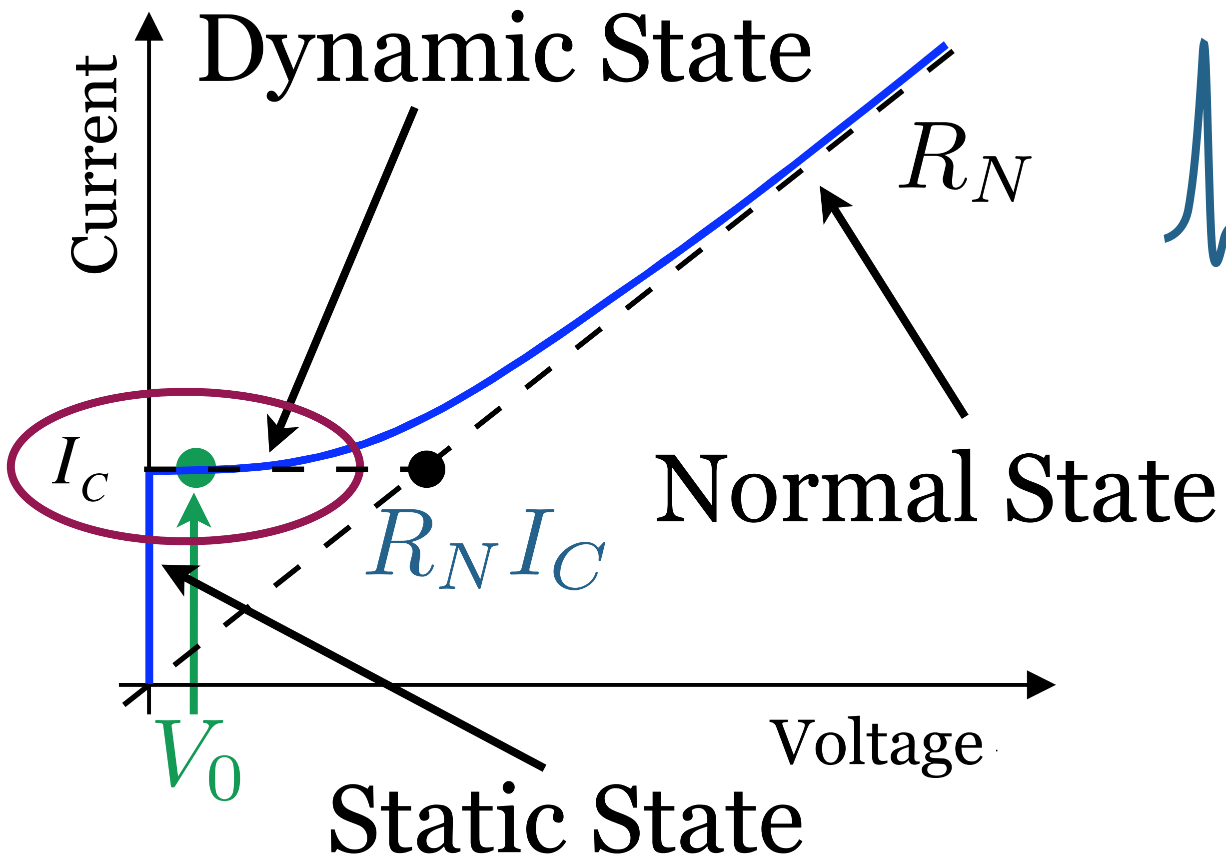


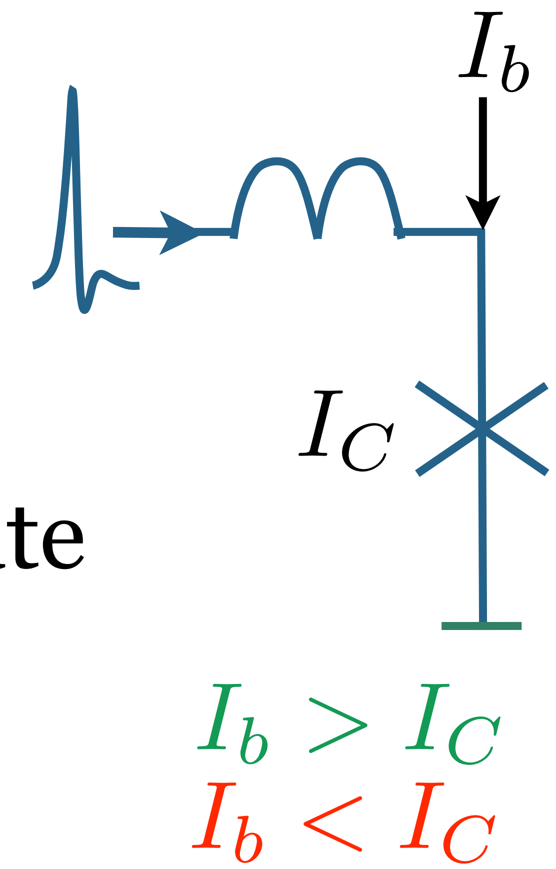
Le principe de la logique RSFQ

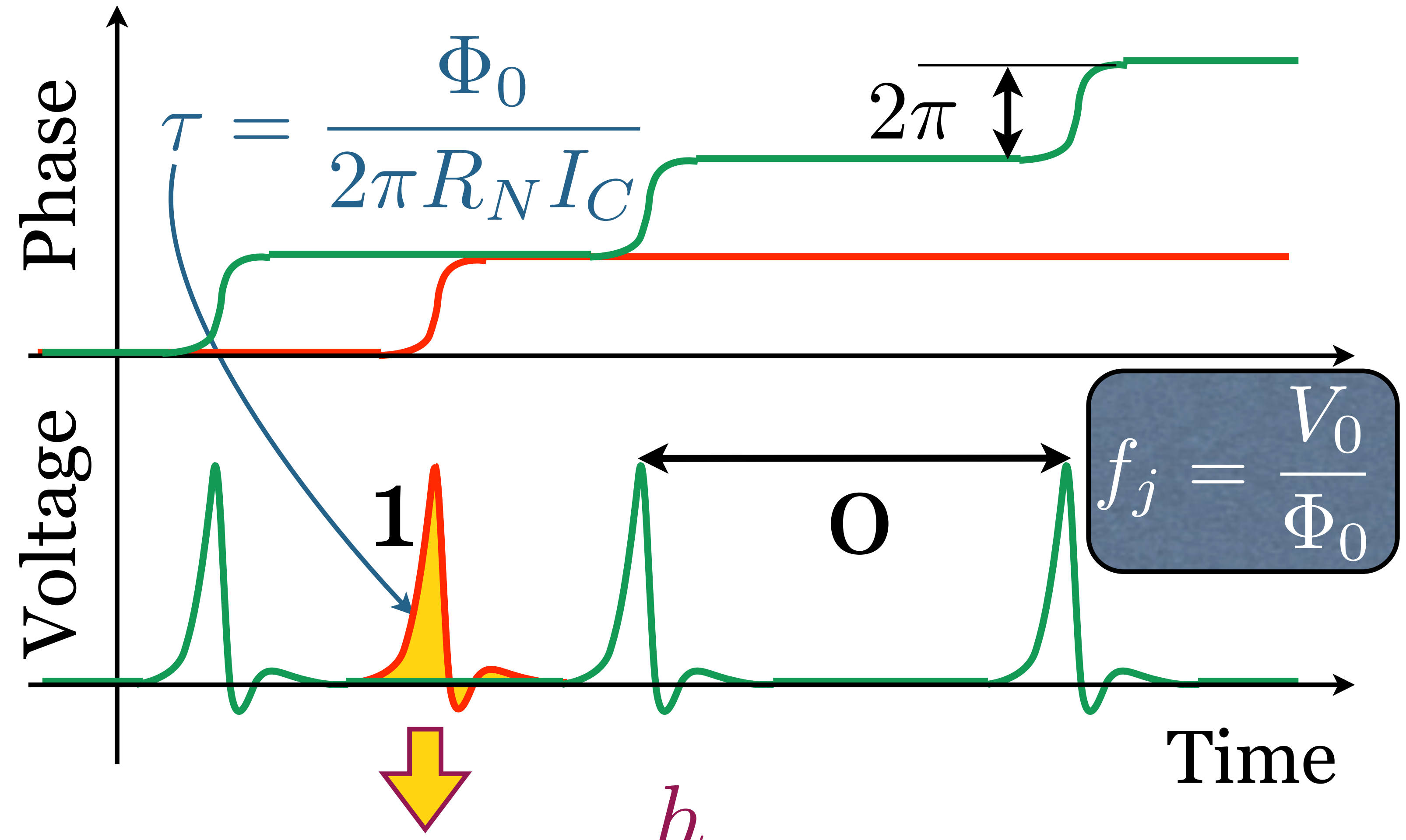


Quantum Flux: $\Phi_0 = \frac{h}{2e} = 2.07\mu\mathrm{V/GHz}$

Le principe de la logique RSFQ

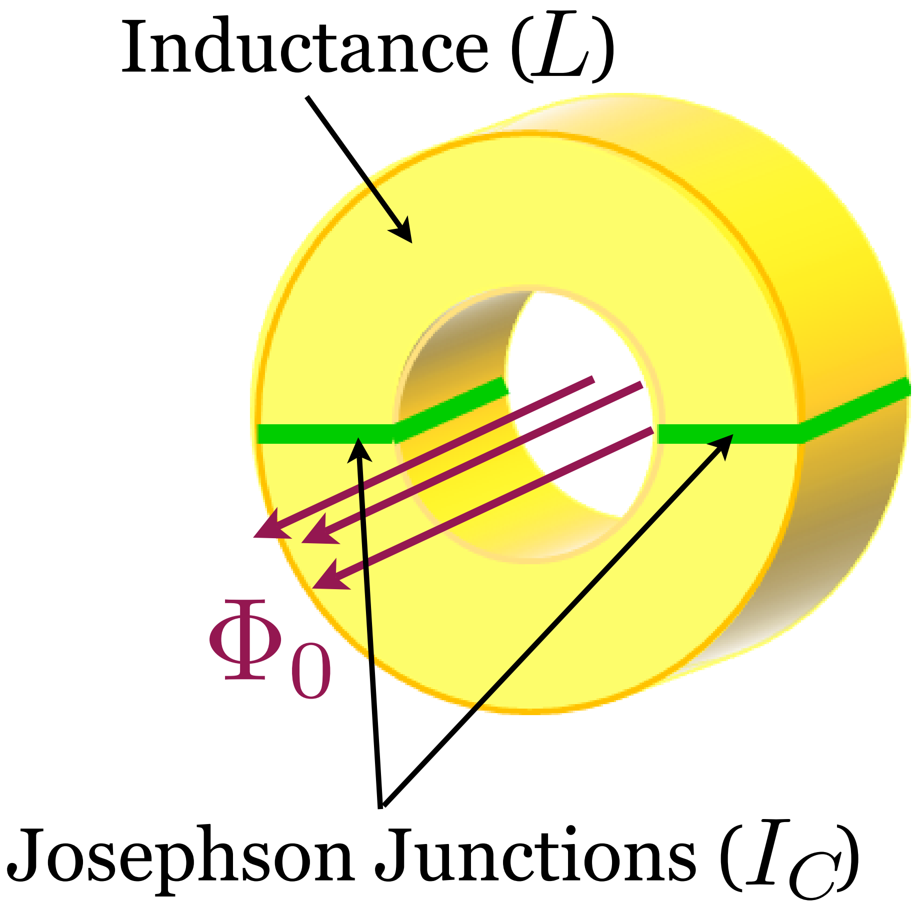




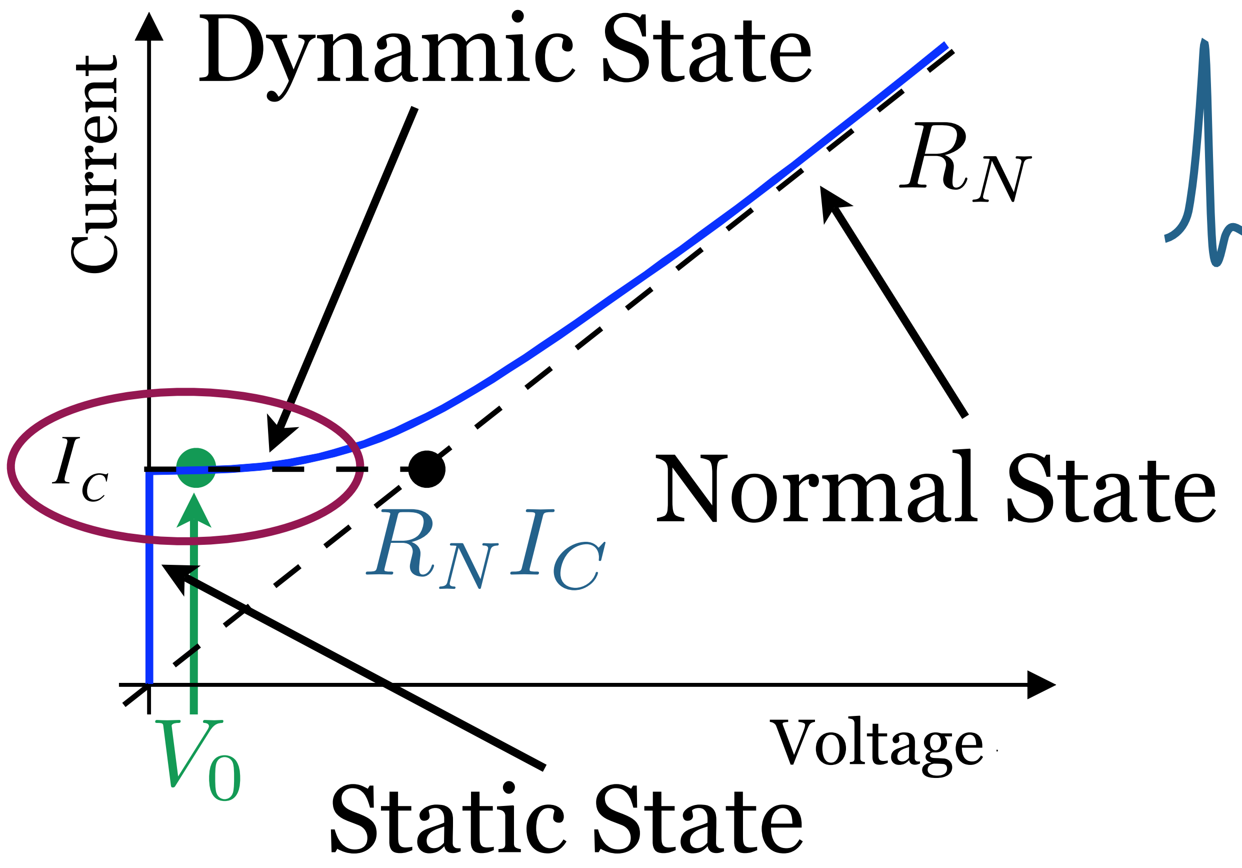


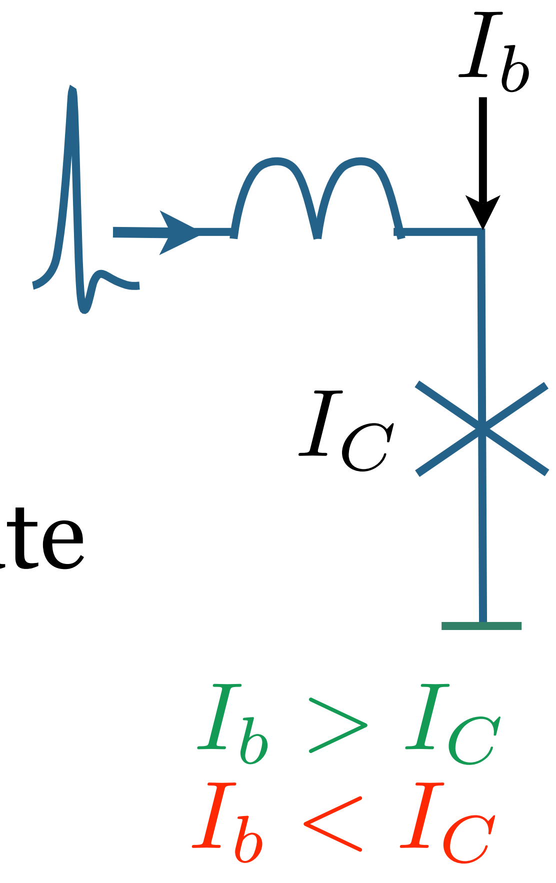
Quantum Flux: $\Phi_0 = \frac{h}{2e} = 2.07\mu V/GHz$

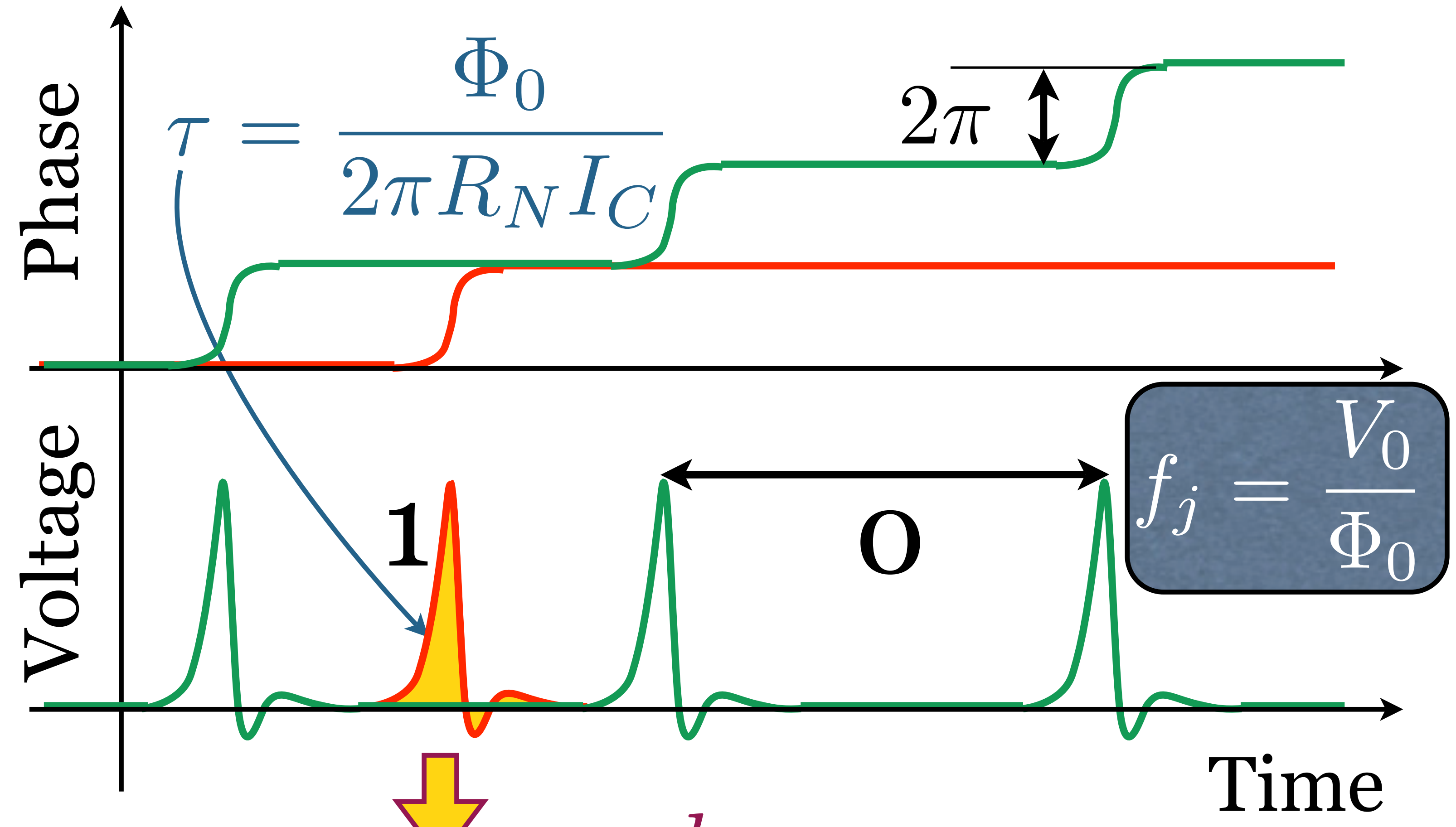
Superconducting **QU**antum **I**nterference **D**evice



Le principe de la logique RSFQ

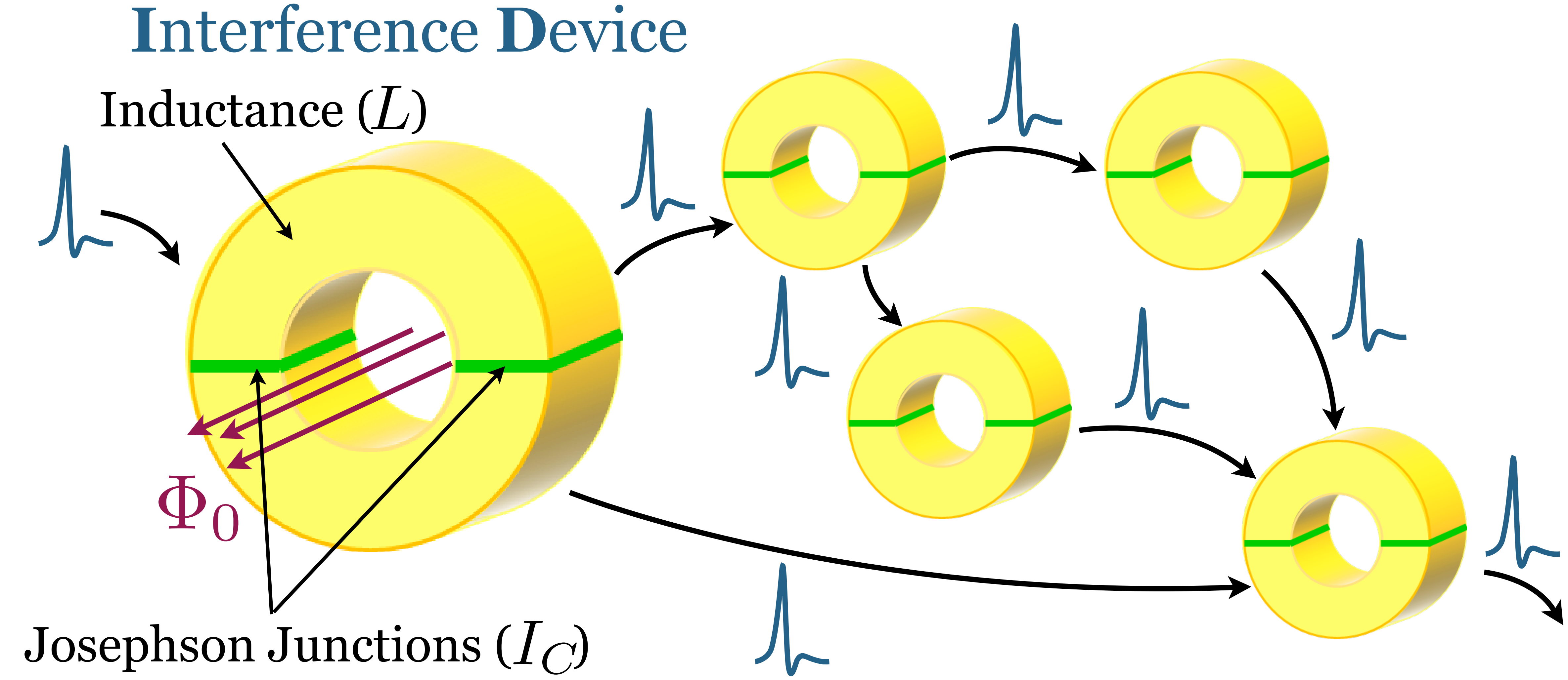






Quantum Flux: $\Phi_0 = \frac{h}{2e} = 2.07\mu V/GHz$

Superconducting **QU**antum **I**nterference **D**evice



Flux Transmission

$LI_C < 0.5\Phi_0$

Flux Storing

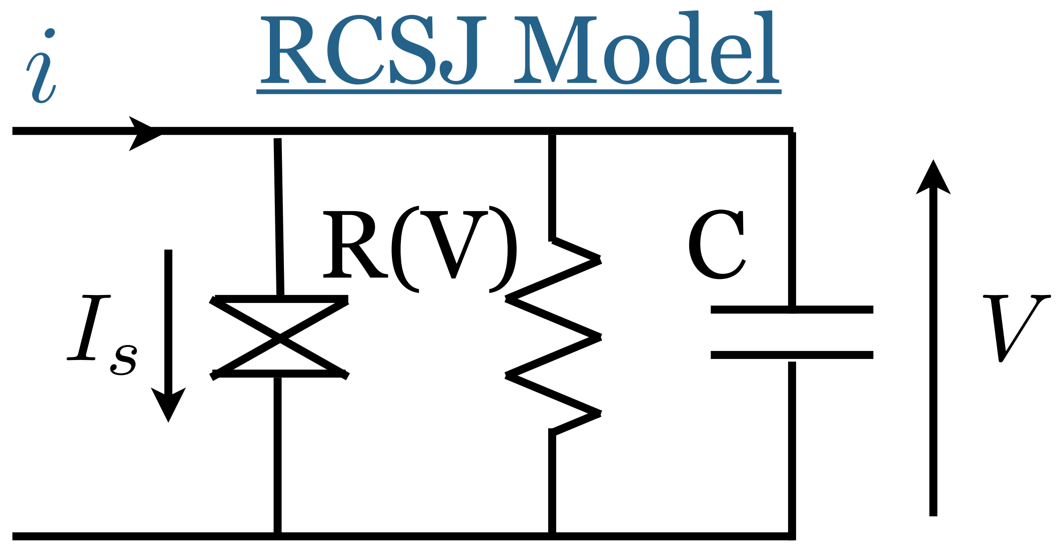
$LI_C > 1.5\Phi_0$

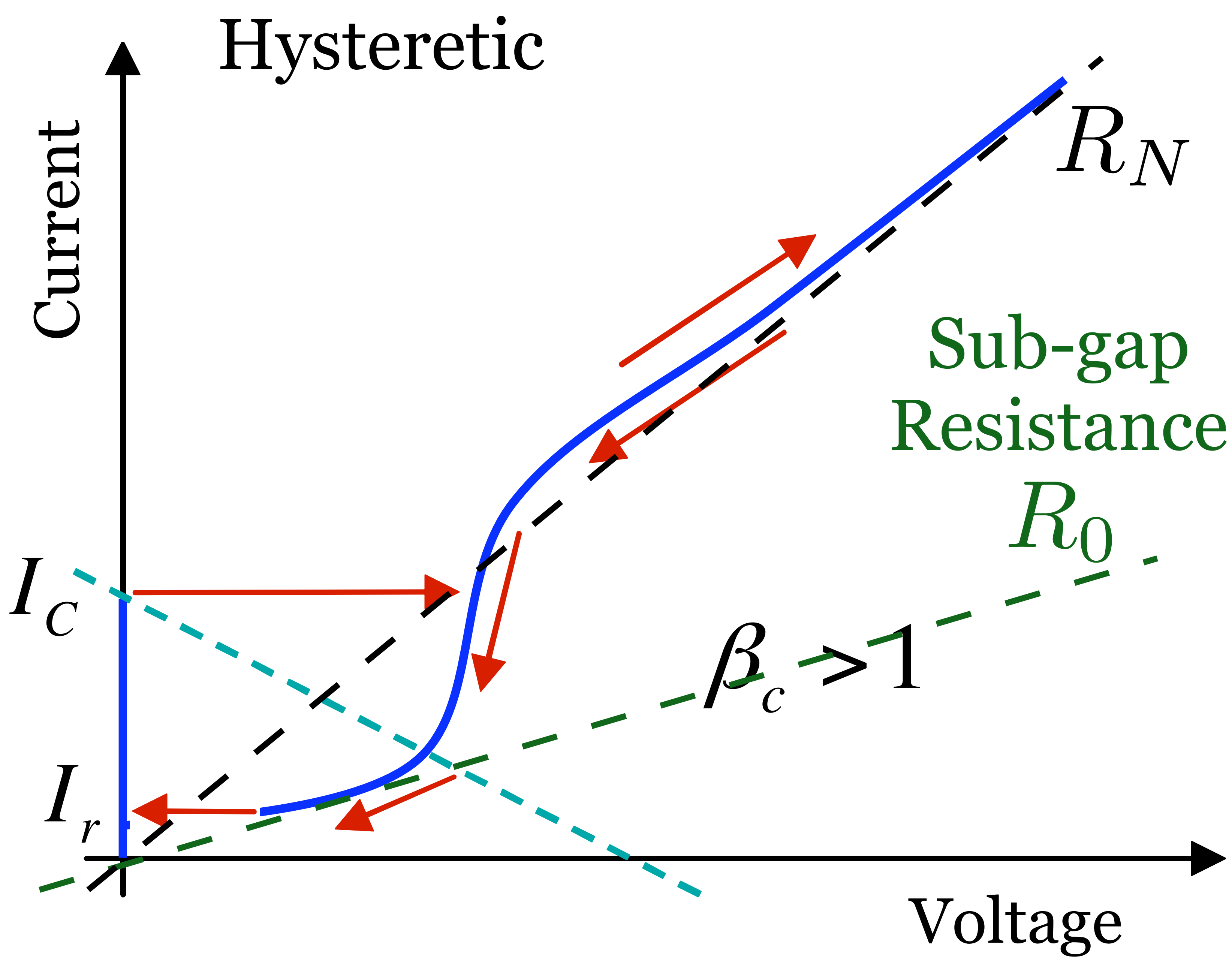
Les jonctions RSFQ existantes

- **SIS (Tunnel junctions) Externally Shunted Josephson junctions:**

✓ Nb/AlOx/Nb (4.2 K, 60k JJs)

✓ NbN/MgO/NbN (10 K, 10k JJs)





Les jonctions RSFQ existantes

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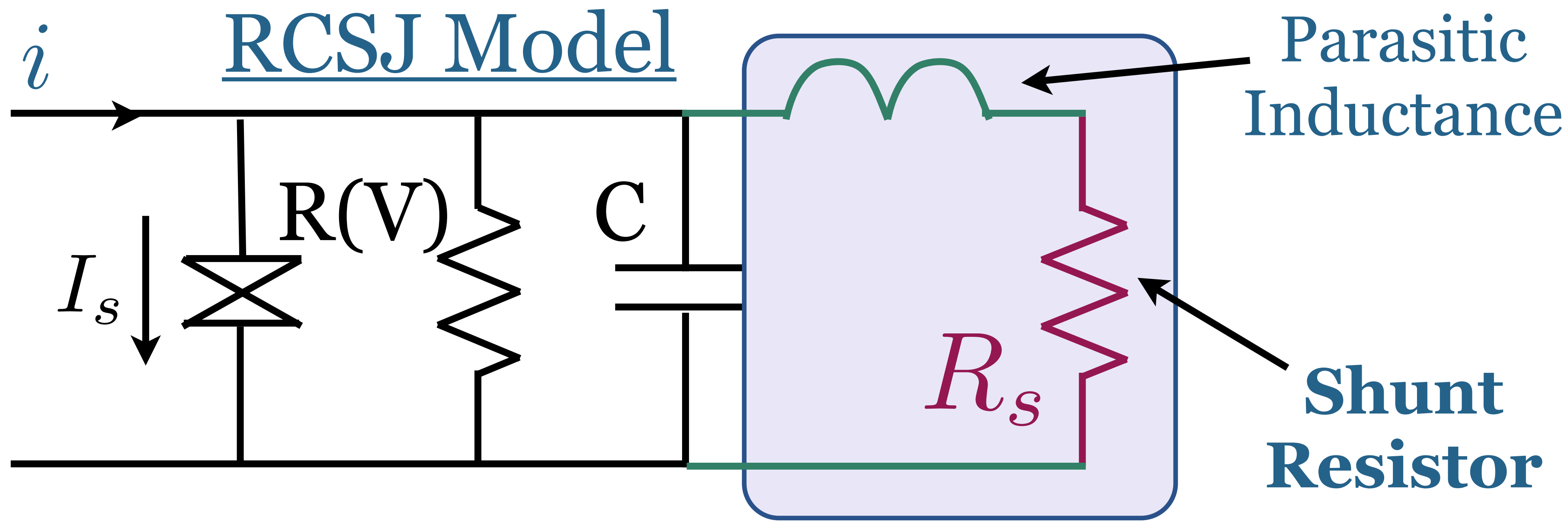
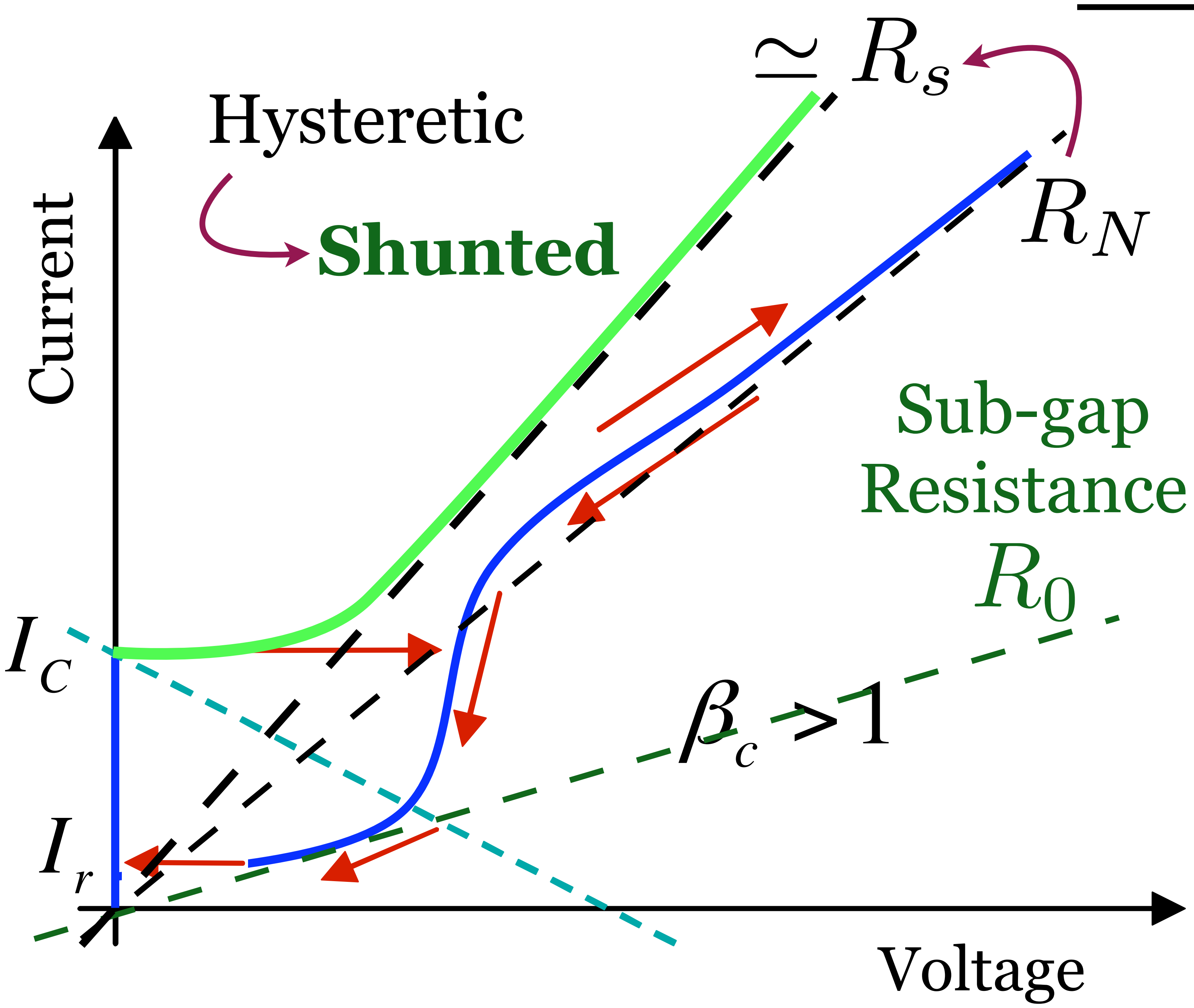


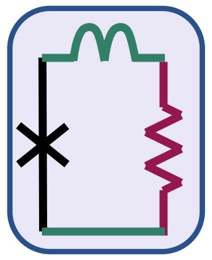


Externally reduced Stewart-McCumber factor

$$\beta_c = \frac{2\pi I_C \overbrace{(R_0//Rs)}^{\simeq R_s}{}^2 C}{\Phi_0} \simeq 1$$

Les Jonctions RSFQ existantes

- **SIS Externally Shunted JJs:**



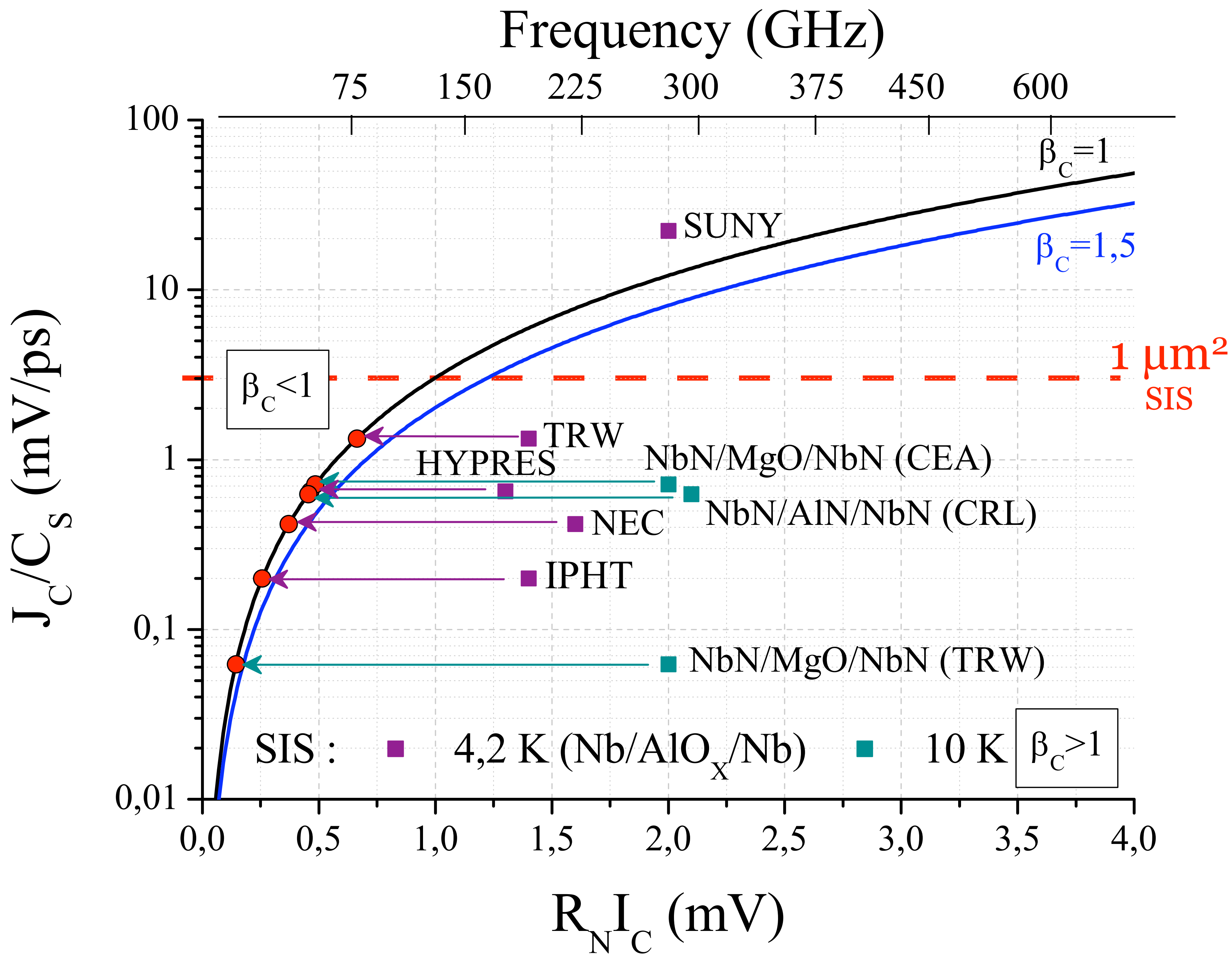
✓ Nb/AlOx/Nn

✓ NbN/MgO/NbN

$$R_N I_C[\text{SIS Ex. Sh.}] < R_N^* I_C[\text{SIS}]$$

$R_N I_C$ → Characteristic Voltage

$$f_{clock}[\text{GHz}] \propto R_N I_C[\text{mV}]$$



Les Jonctions RSFQ existantes

- **SIS Externally Shunted JJs:**
  - ✓ Nb/AlOx/Nn
  - ✓ NbN/MgO/NbN

$R_N I_C[\text{SIS Ex. Sh.}] < R_N^* I_C[\text{SIS}]$

$R_N I_C$ → Characteristic Voltage

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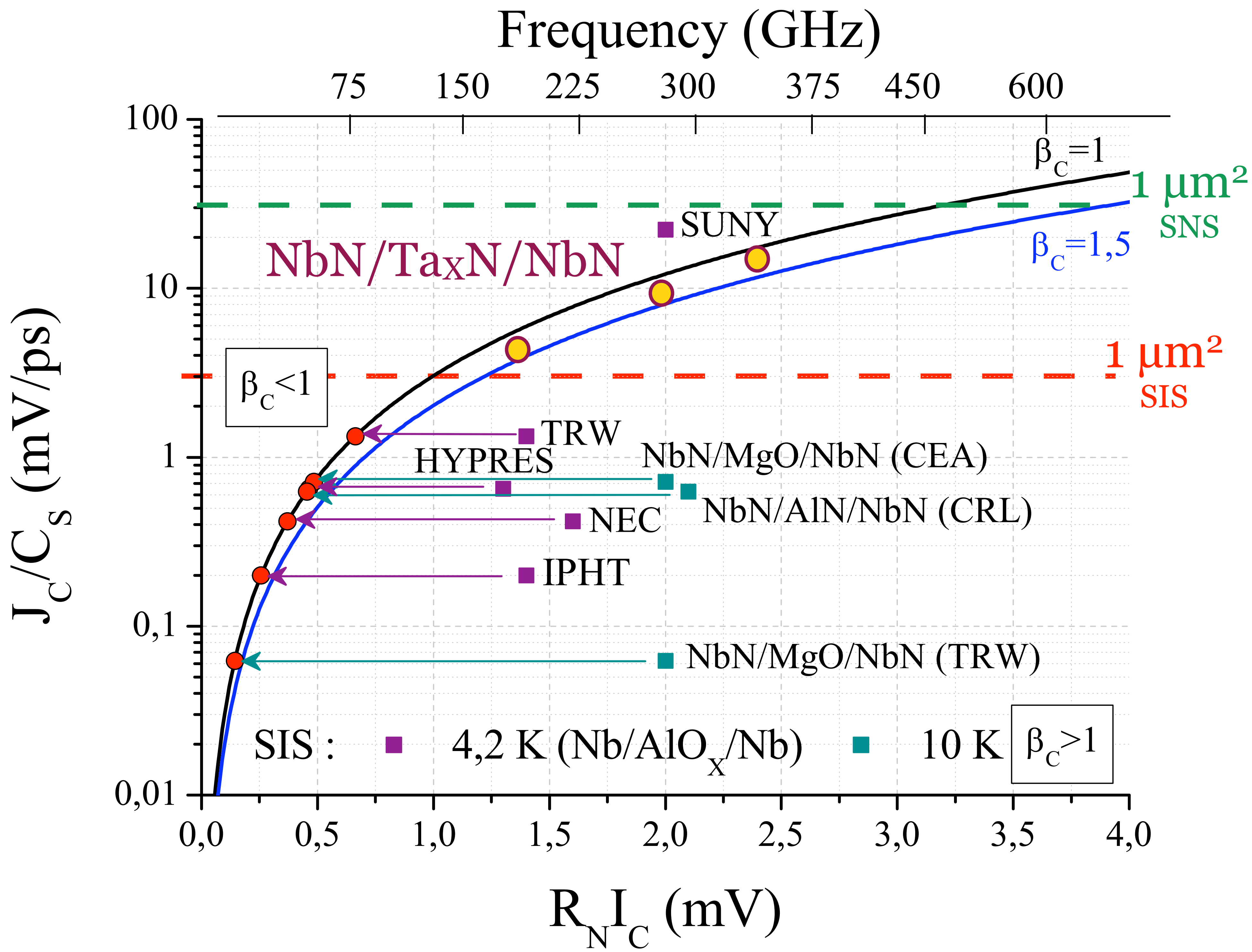


- **SNS Self-Shunted JJs:** →
  - ✳ No parasitic inductances
  - ✳ High circuit density
  - ✳ 1 order higher thickness

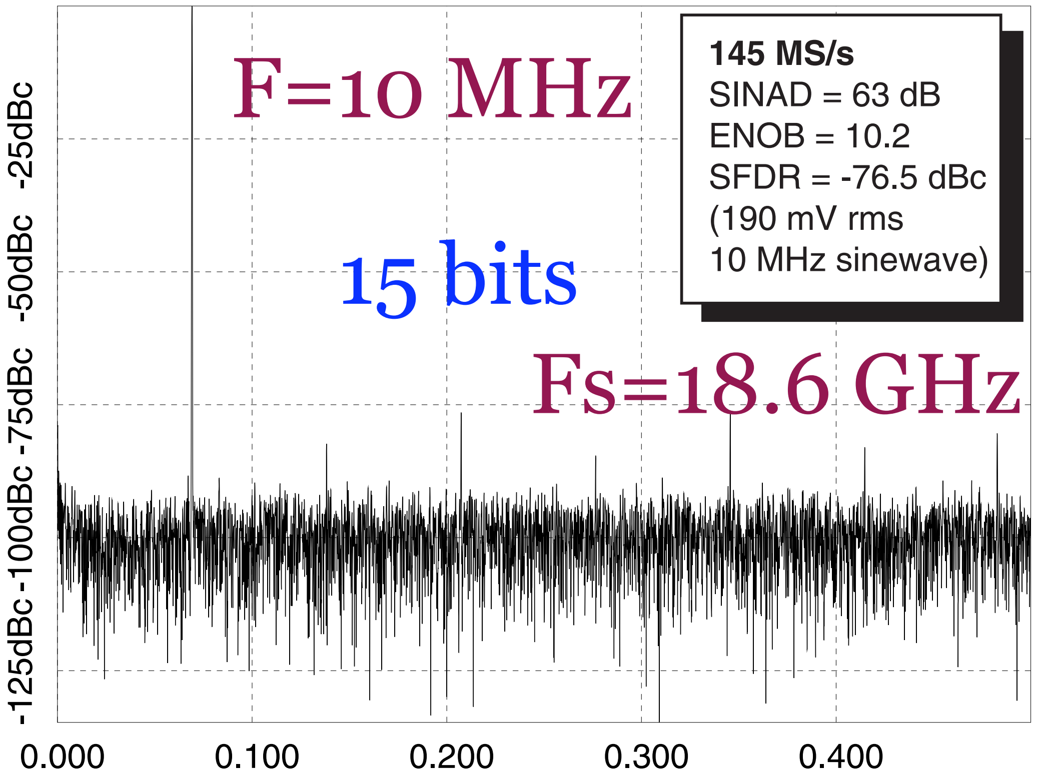
Internally reduced β_c

✓ **NbN/TaxN/NbN (10k JJs)** ➡ **Higher $R_N I_C$ even at low**

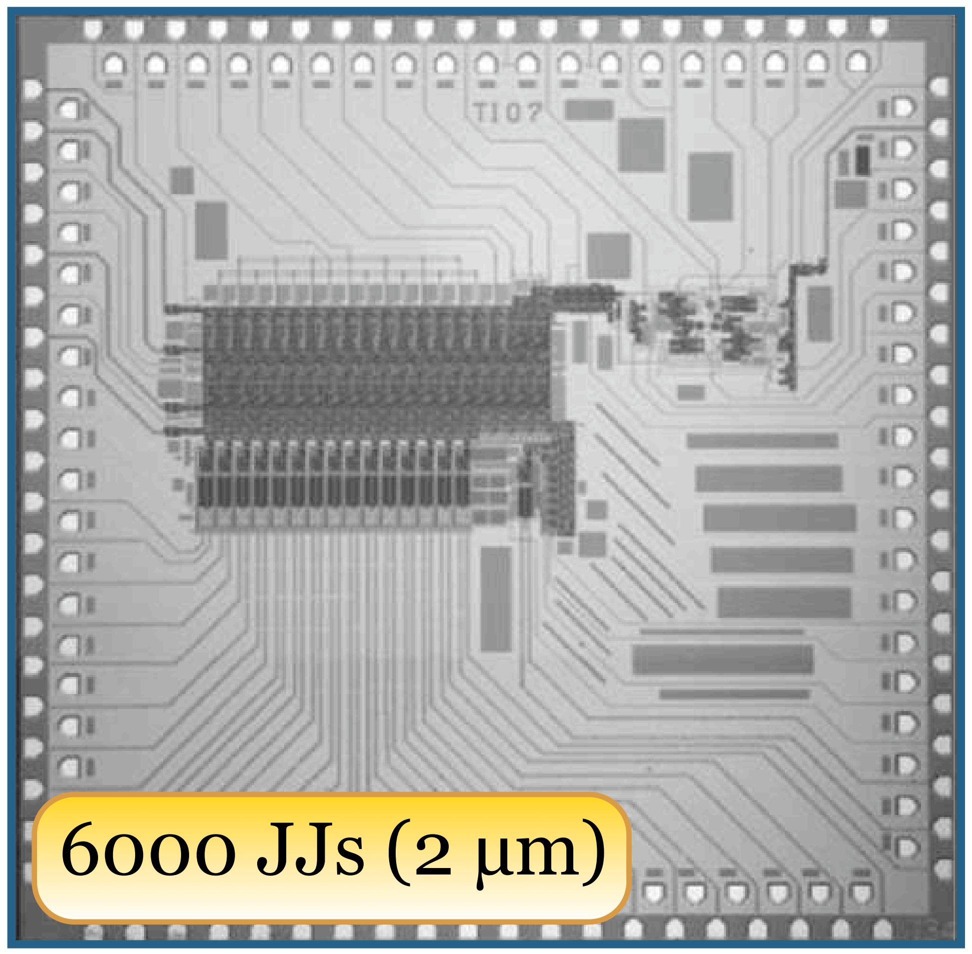
↑ Barrier tuned near the metal-insulator transition → **High Resistivity**

Etat de l'art des CAN

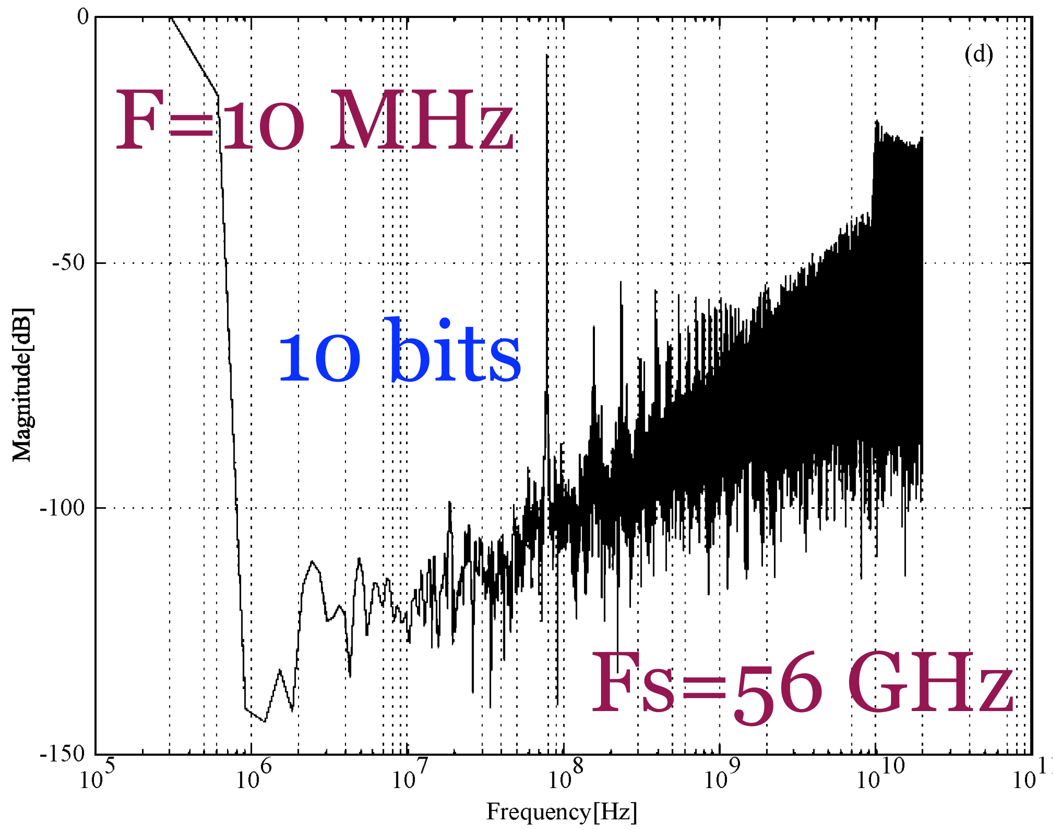
Phase Modulation–Demodulation ADC Architecture
[USA (HYPRES)]



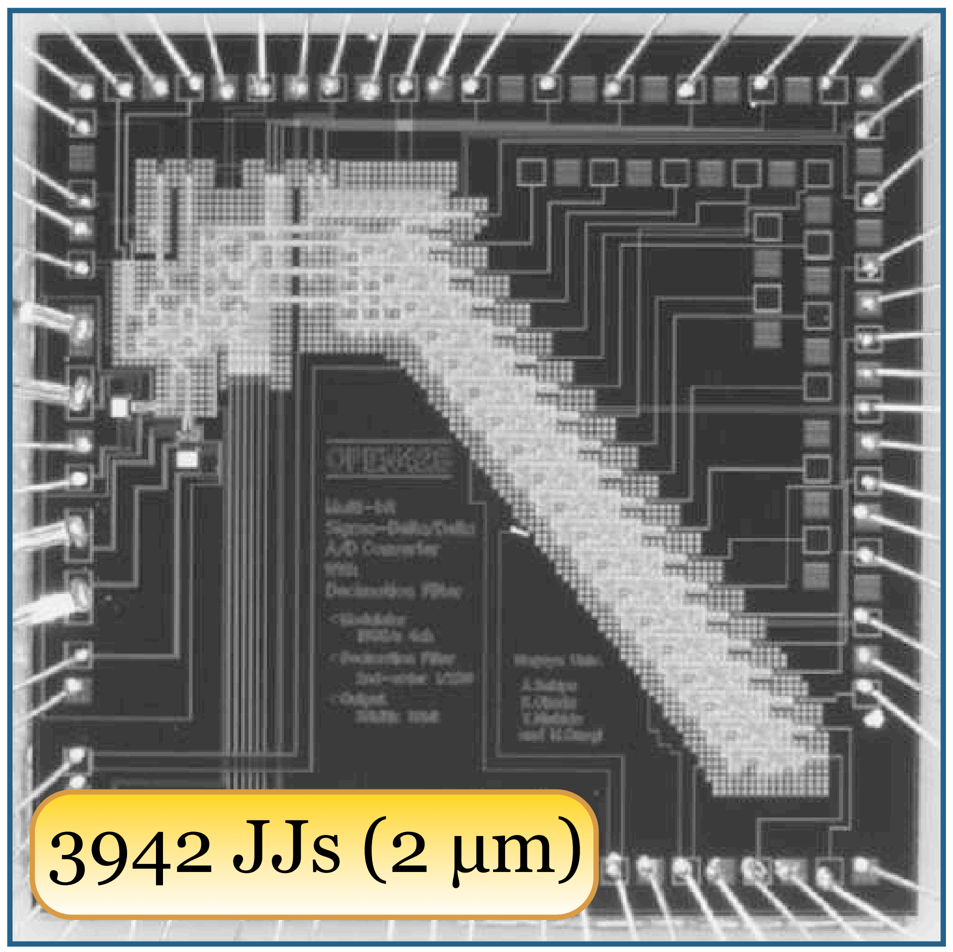
Tested at 145 Ms/s



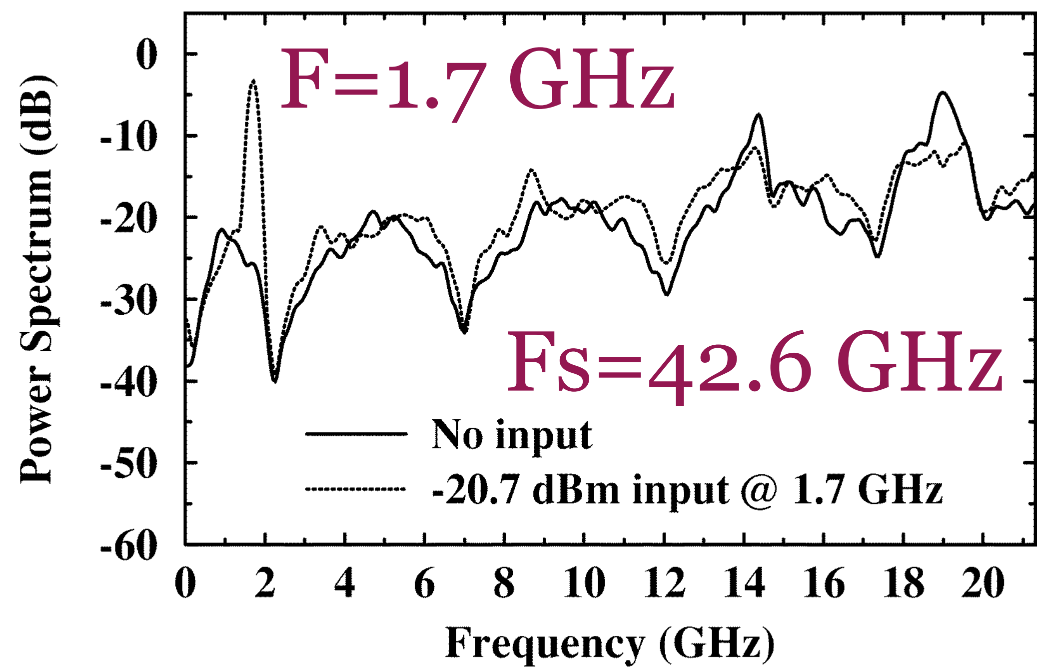
Low-Pass Sigma-Delta ADC Architecture
[Japan (NEC)]



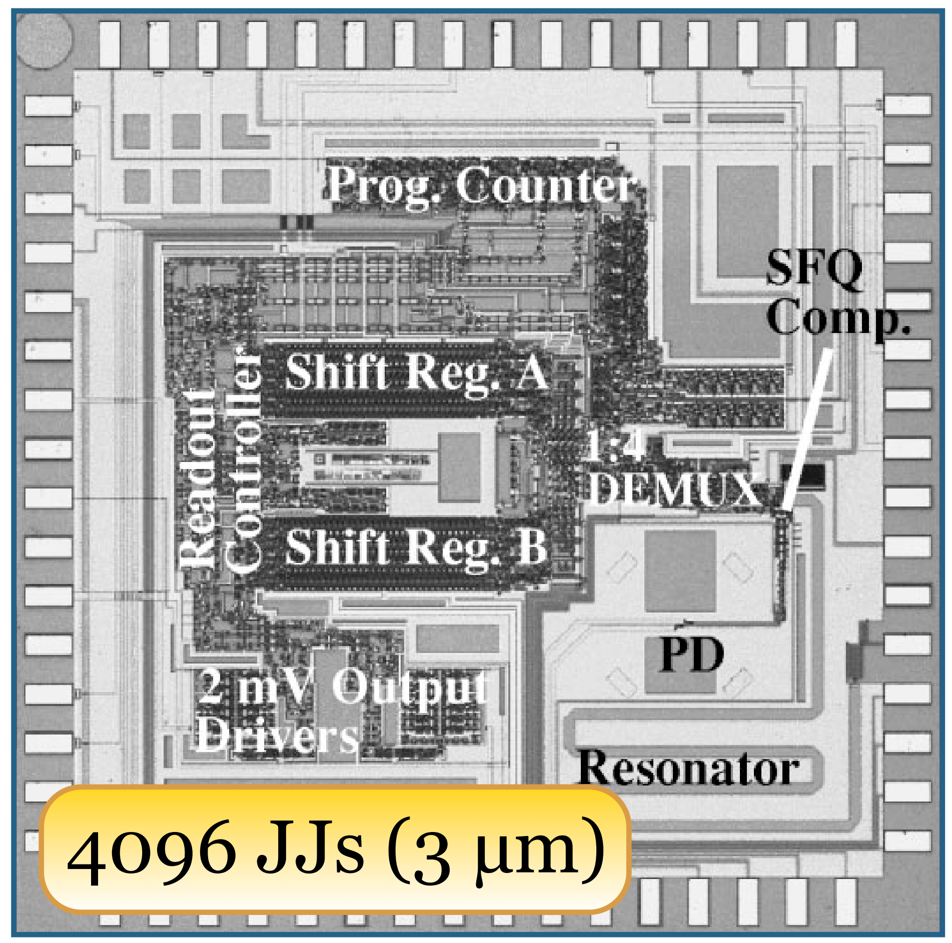
Tested at 218 Ms/s



Band-Pass Sigma-Delta Modulator
[USA (HYPRES)]



Tested at 320 Ms/s



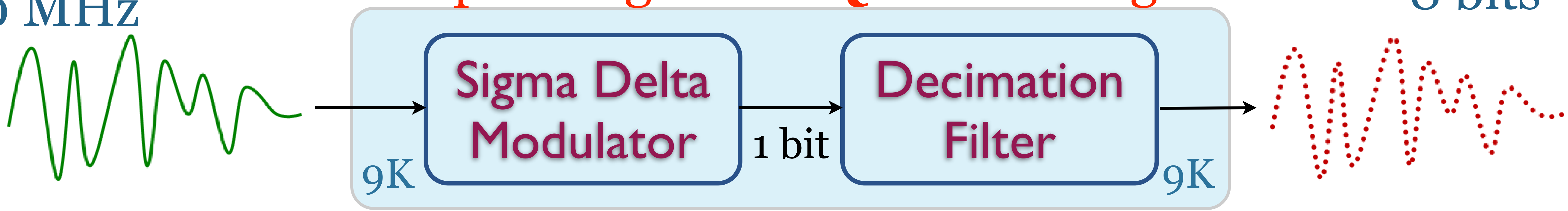
Objectif

Analog-to-Digital Converter based on ∑Δ Architecture

Fc=30 GHz
B=500 MHz

Superconducting
Rapid **S**ingle **F**lux **Q**uantum Logic

8 bits



Fs=200 GHz

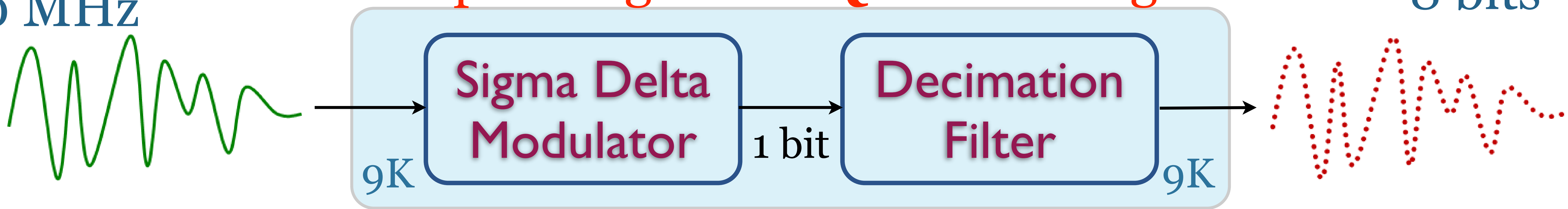
Objectif

Analog-to-Digital Converter based on ∑Δ Architecture

Fc=30 GHz
B=500 MHz

Superconducting
Rapid **S**ingle **F**lux **Q**uantum Logic

8 bits



Fs=200 GHz

New technology:

✓ **Self-shunted Josephson junctions NbN/Ta_XN/NbN**

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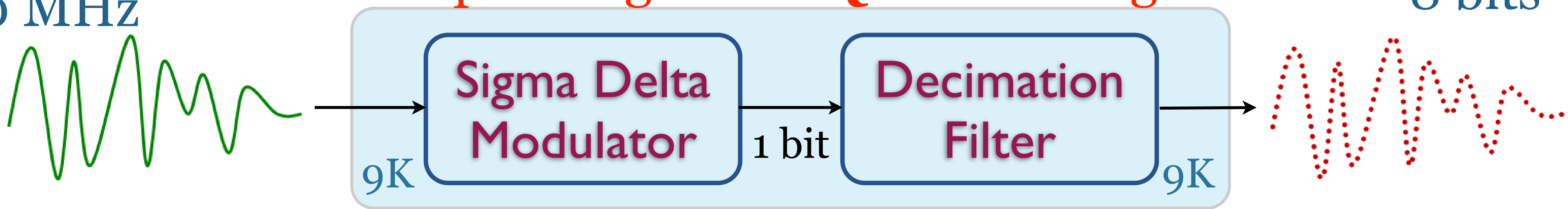

Fs=200 GHz

New technology:

✓ **Self-shunted Josephson junctions $NbN/Ta_xN/NbN$**

[LTS] **Superconductors Technologies** [HTS]

Nb (9.2 K) → **4.2 K**
NbN (16 K) → **9 K**
High Complexity (60-10 K JJ)

YBaCuO (90 K) → **40 K**
Low Complexity (100 JJ)

Objectif

Analog-to-Digital Converter based on ∑Δ Architecture

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B=500 MHz

Superconducting
Rapid **S**ingle **F**lux **Q**uantum Logic

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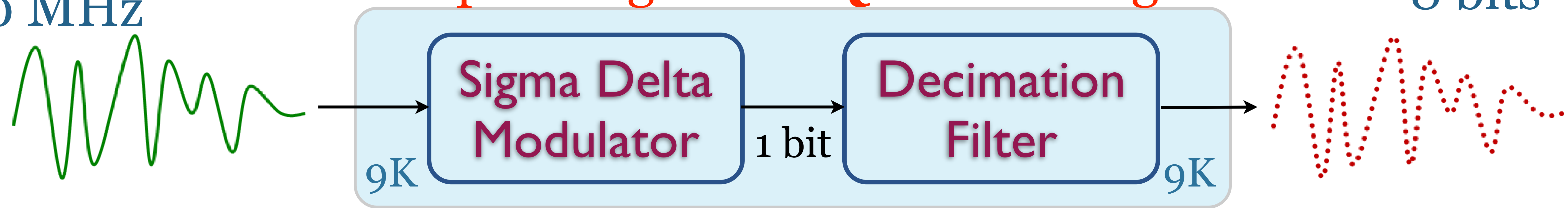


Fs=200 GHz

New technology:

✓ **Self-shunted Josephson junctions NbN/Ta_XN/NbN**

✓ Niobium Nitride (NbN) superconductor (16 K)

[LTS] **Superconductors Technologies** [HTS]

Nb (9.2 K) → 4.2 K

NbN (16 K) → **9 K**

High Complexity (60-10 K JJ)

YBaCuO (90 K) → 40 K

Low Complexity (100 JJ)

⇒ Relaxed cryogenic environment

[thèse N. Hadacek 2002 UJF]

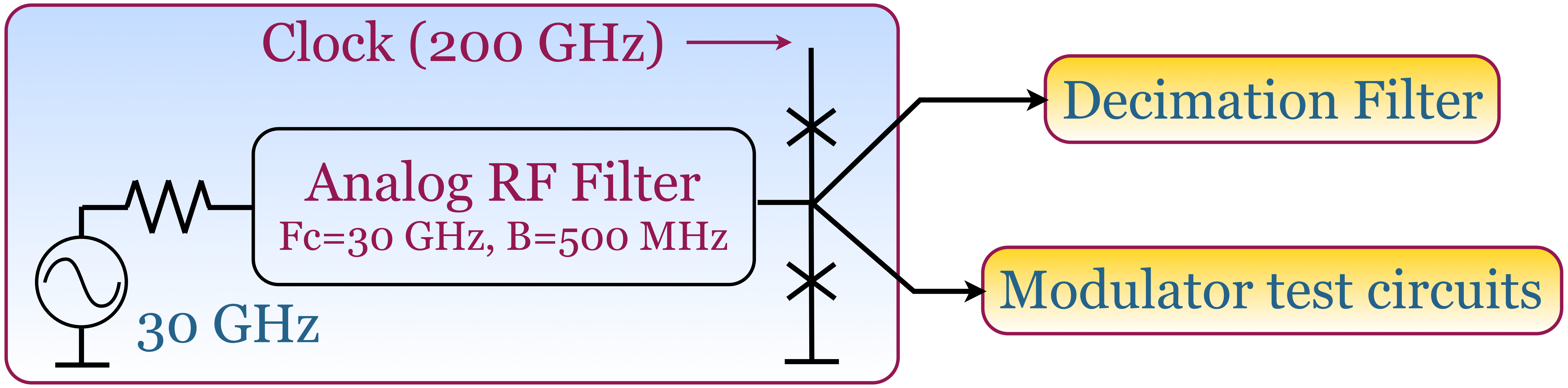
Plan de l'exposé

- Introduction
- Rappels sur le CAN et l'Electronique supraconductrice
- **Etude de la structure du CAN en NbN**
- Implementation et comparaison de la technologie NbN et Nb
- Conclusions et perspectives

[thèse J. Bulzachelli 2002 MIT]

Modulator based on the Bulzachelli schema (Fs=20 GHz, Fc=2 GHz, B=40 MHz)

We studied the ADC with the frequencies 1 order higher



Band-Pass Sigma-Delta Modulator

Conception du CAN

[thèse J. Bulzachelli 2002 MIT]

Modulator based on the Bulzachelli schema (Fs=20 GHz, Fc=2 GHz, B=40 MHz)

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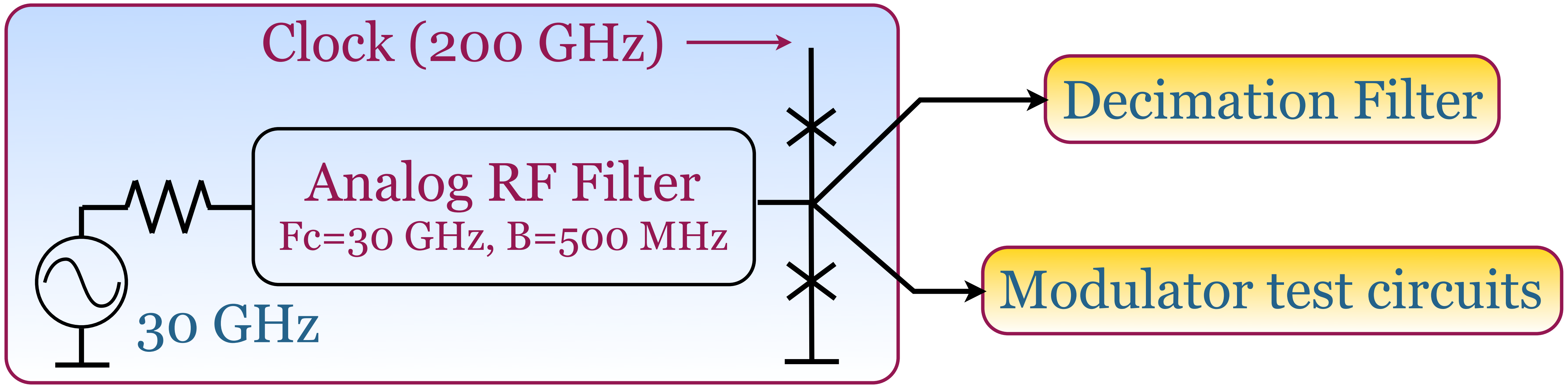
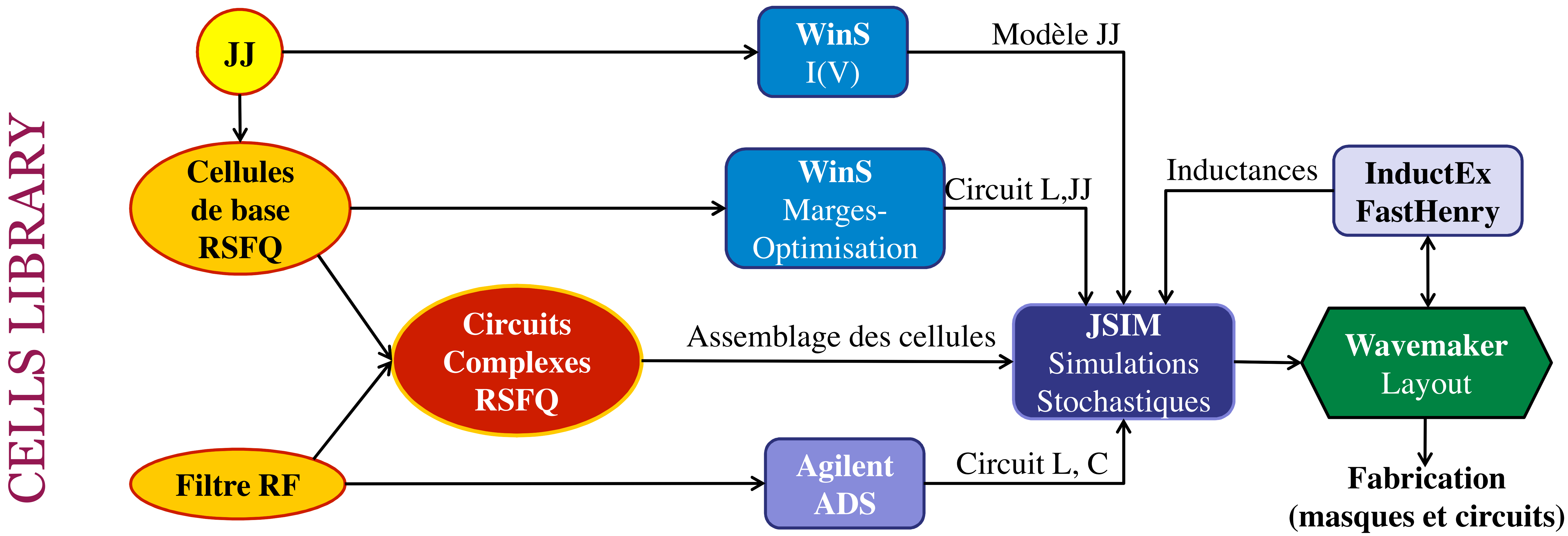


Band-Pass Sigma-Delta Modulator

✓ Simulation environnement



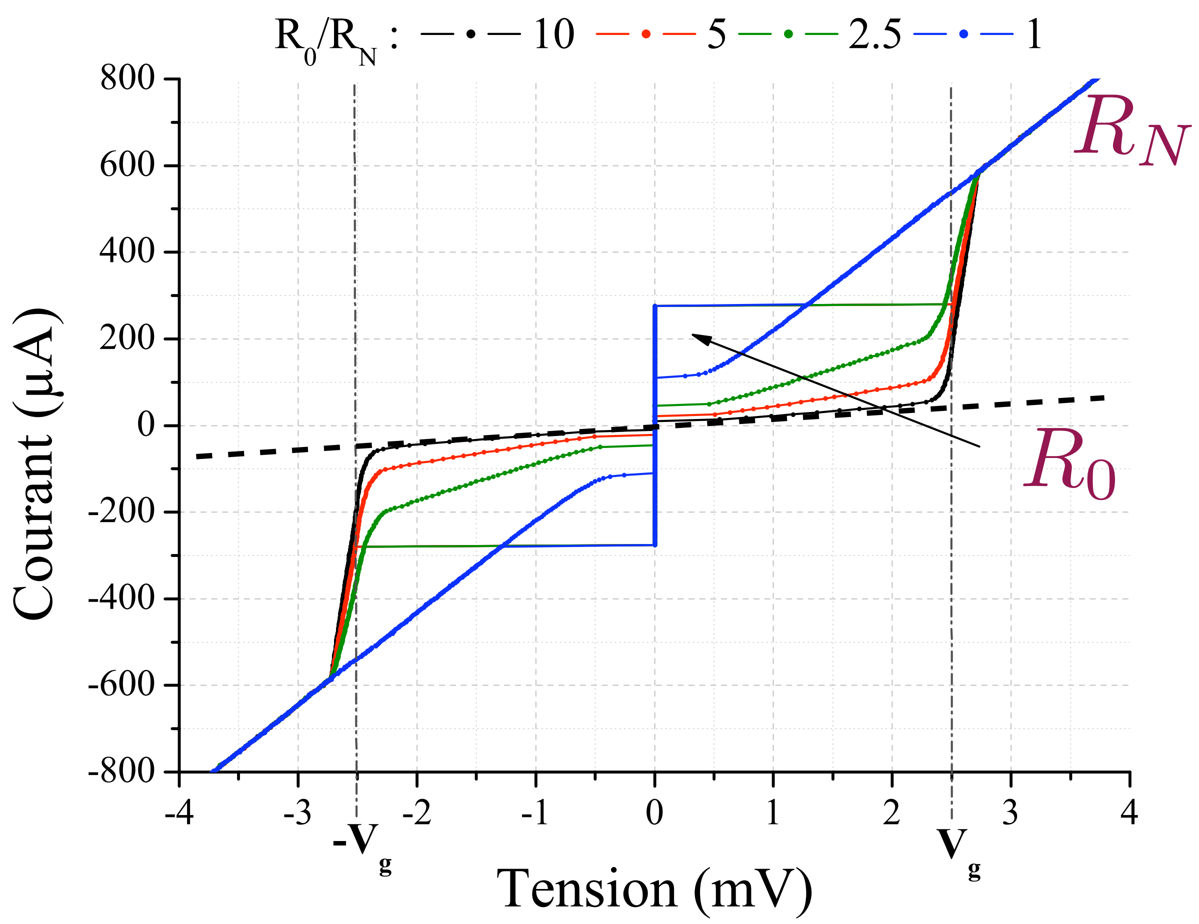
RSFQ cells schema and layout design are taken from the literature and Fluxonics respectively

Le modèle NbN/Ta_XN/NbN

Simulation

- ✓ JSIM (complexes circuits, thermal noise)
- ✓ WinS (I-V curves, gate margins)

RCSJ Model: R_0 → R_N



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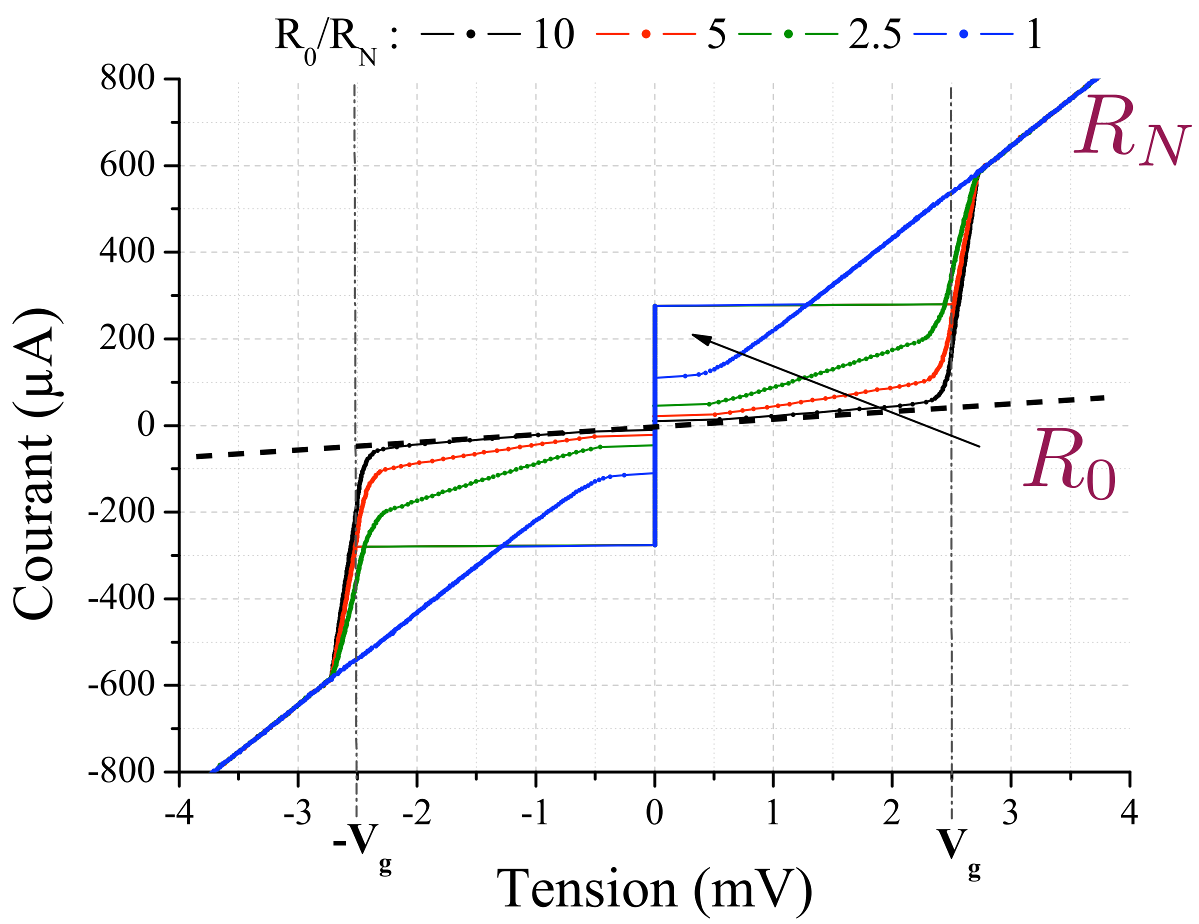
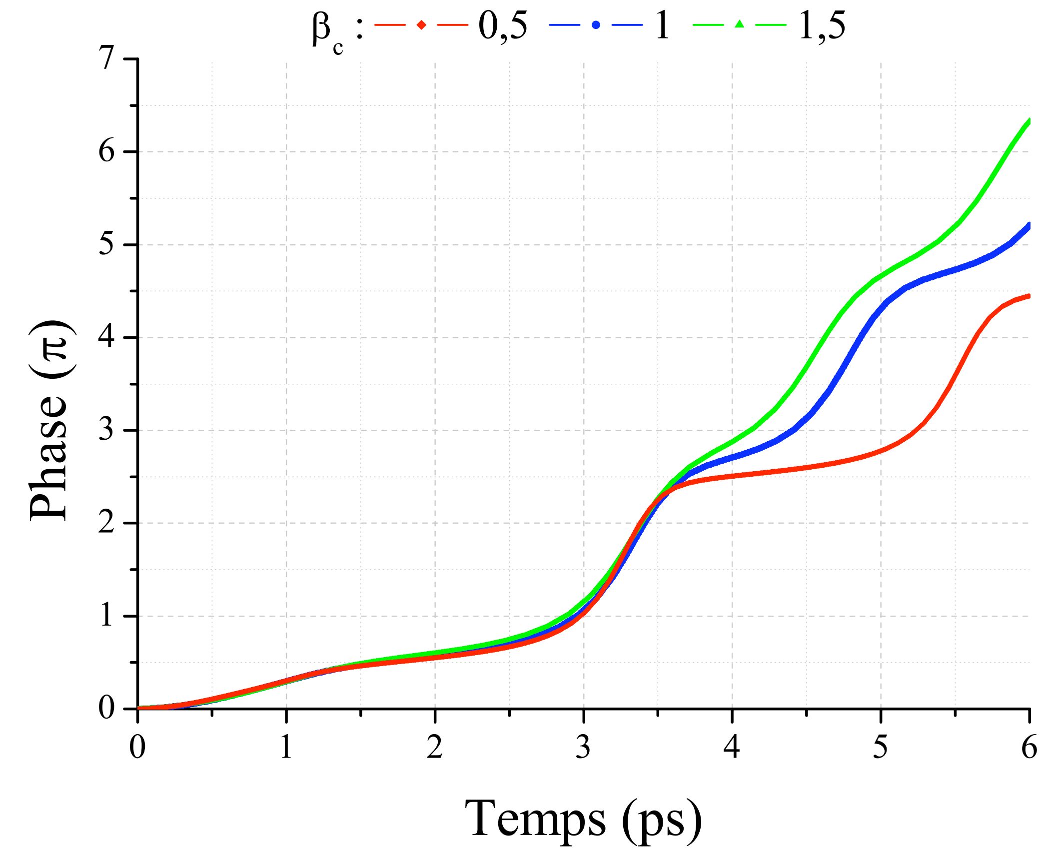
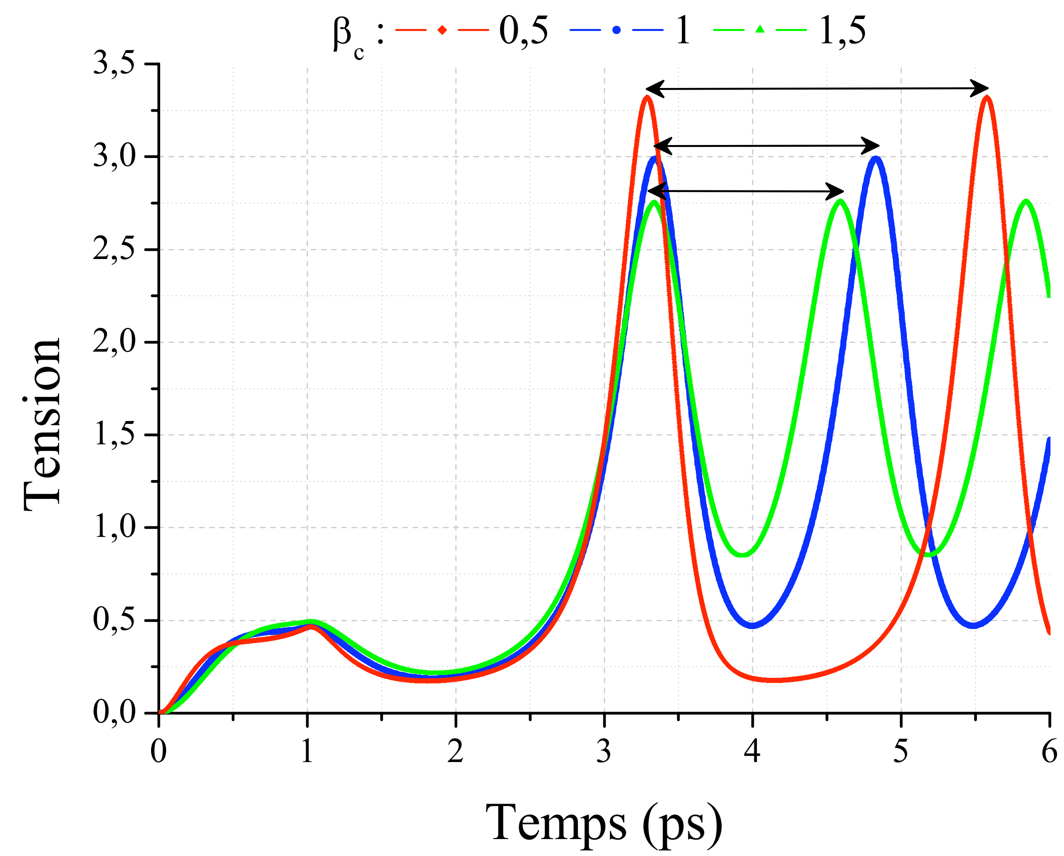
→ RCSJ Model: R_0 → R_N







A JJ is a shunt for the adjacent JJs

Le modèle NbN/Ta$_X$N/NbN

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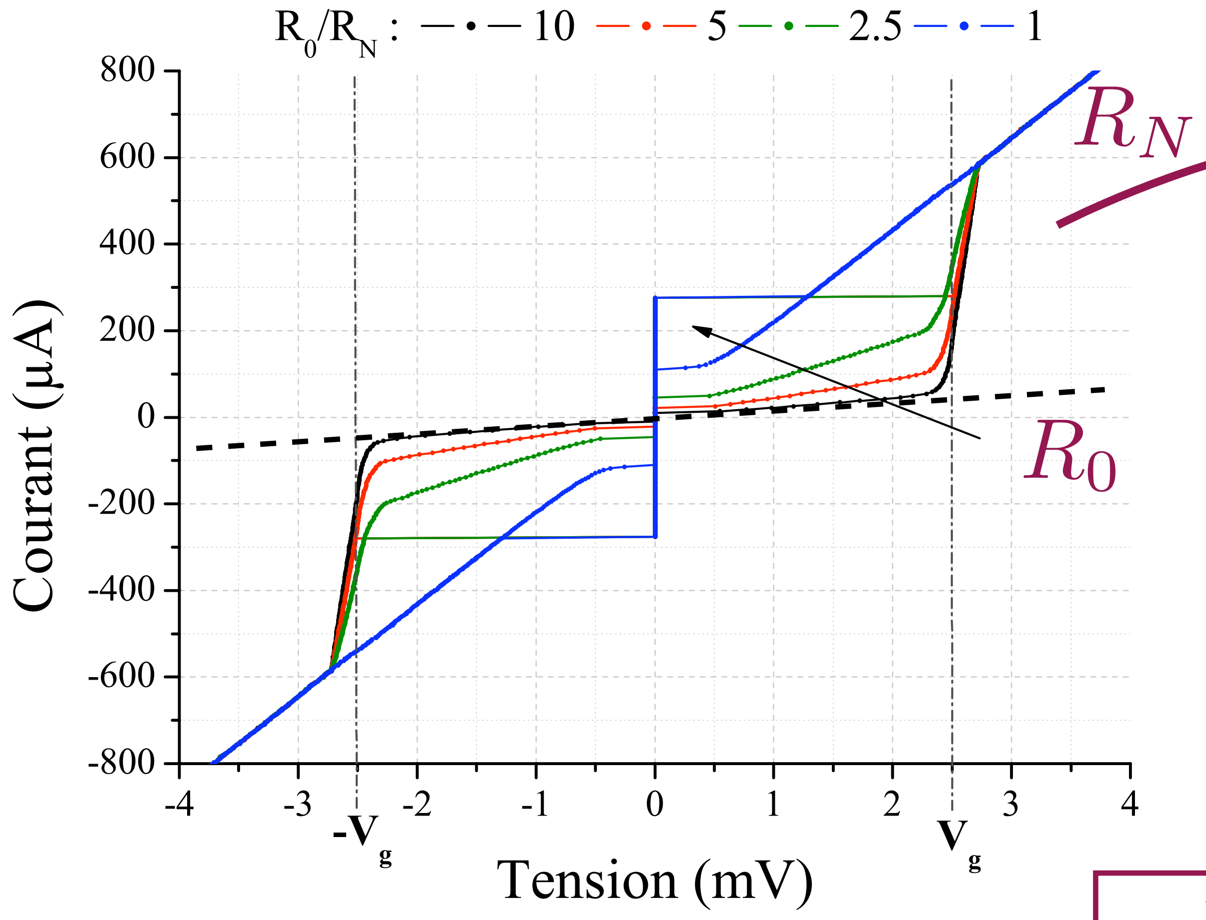
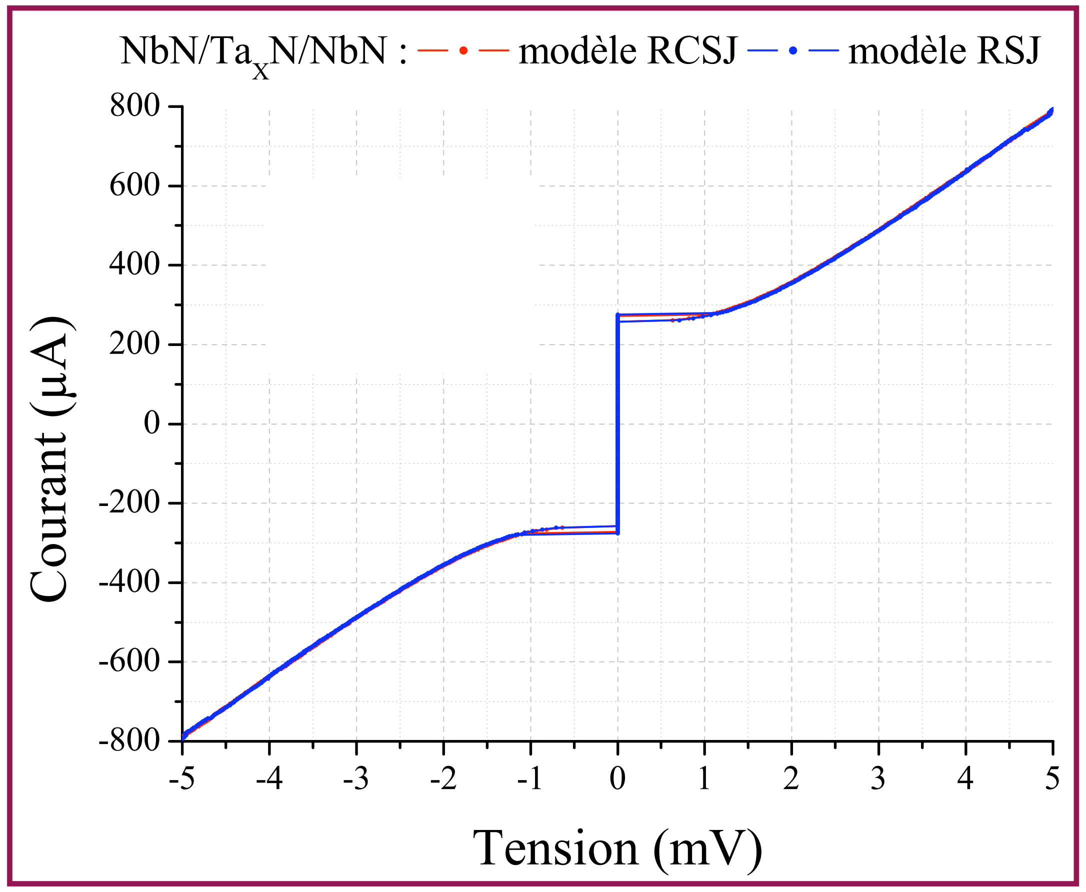
- ✓ JSIM (complexes circuits, thermal noise)
- ✓ WinS (I-V curves, gate margins)

→ RCSJ Model: $R_0 \rightarrow R_N$



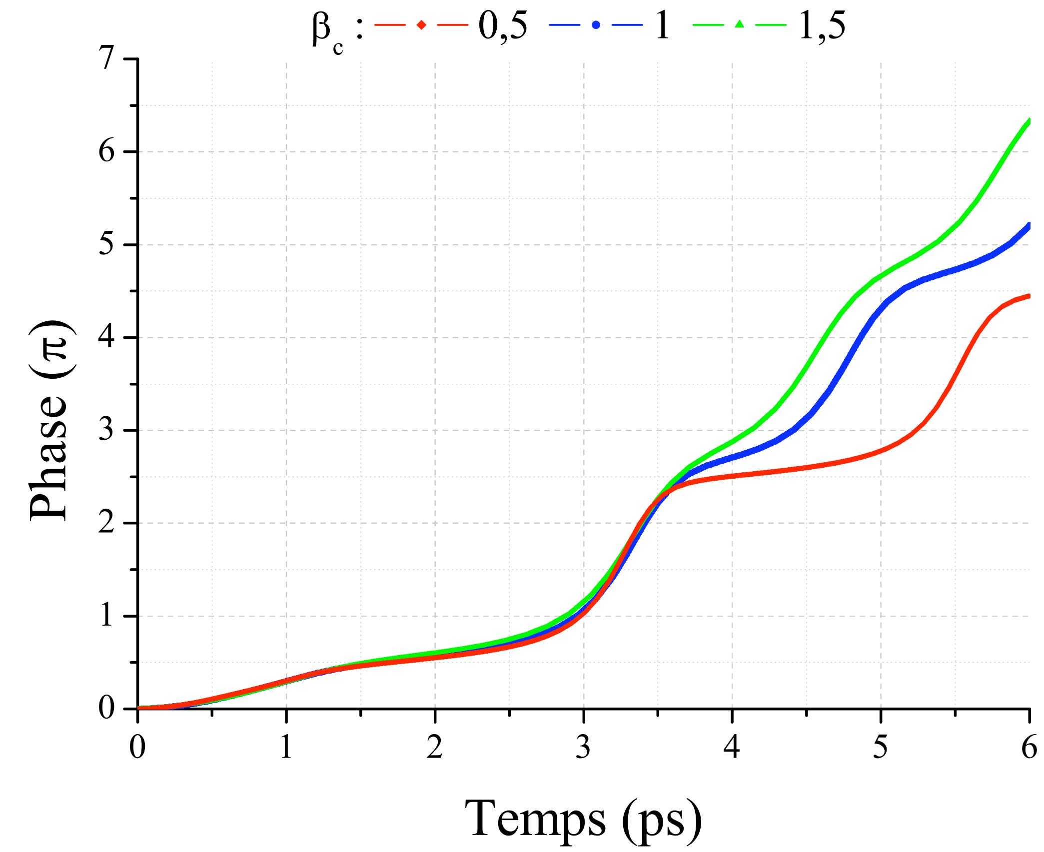
$$R_0 = R_N$$

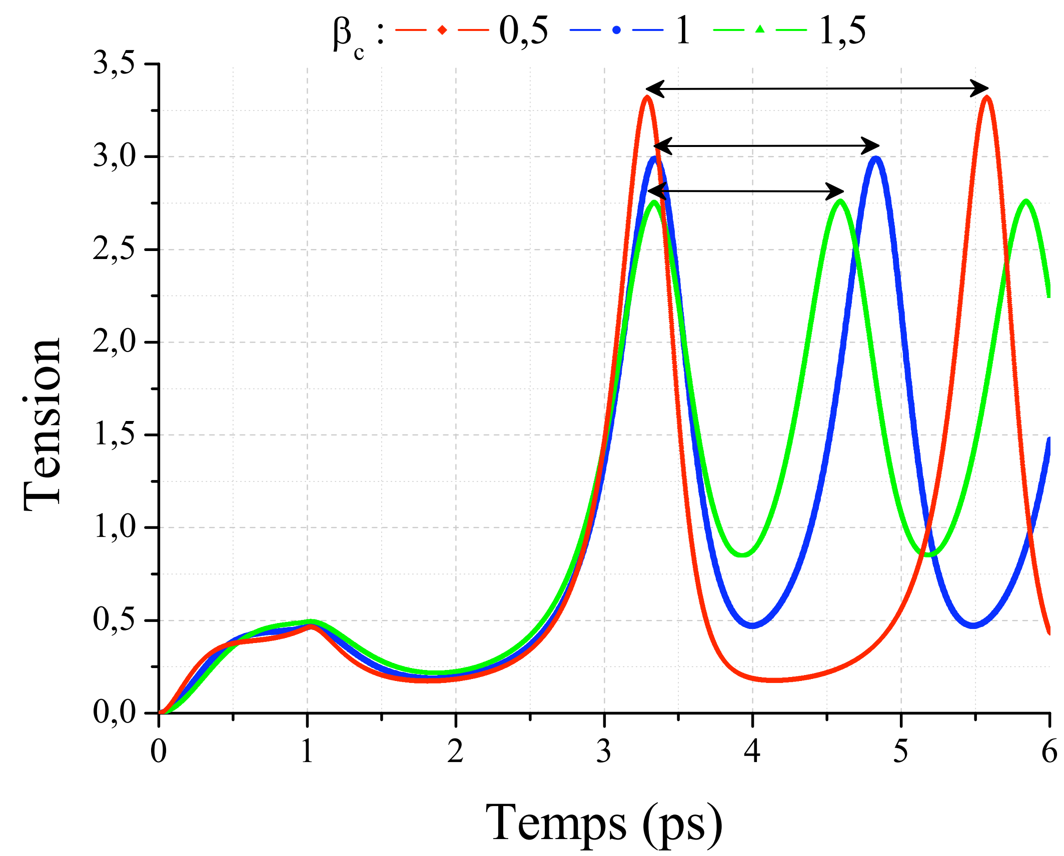
$$\beta_c = 1.1$$



$$\ast\ C = \frac{\beta_c \Phi_0}{2\pi I_C R_N^2}$$

✶ NbN quasi-particles model





A JJ is a shunt for the adjacent JJs

Définition des jonctions

$$J_C(9K) = 5\text{kA/cm}^2$$
$$R_N I_C(9K) = 1.75\text{mV}$$

Jonction	2r (μm)	Surface (μm^2)	I_c (μA)	R_N (Ω)	C_s (fF)
JJ1	7,2	40,7	2035	0,86	247
JJ2	4,7	17,3	867	2,02	105

6 Josephson junctions library

$$I_n(9K) = \frac{2\pi k_B T}{\Phi_0} \simeq 380\text{nA}$$

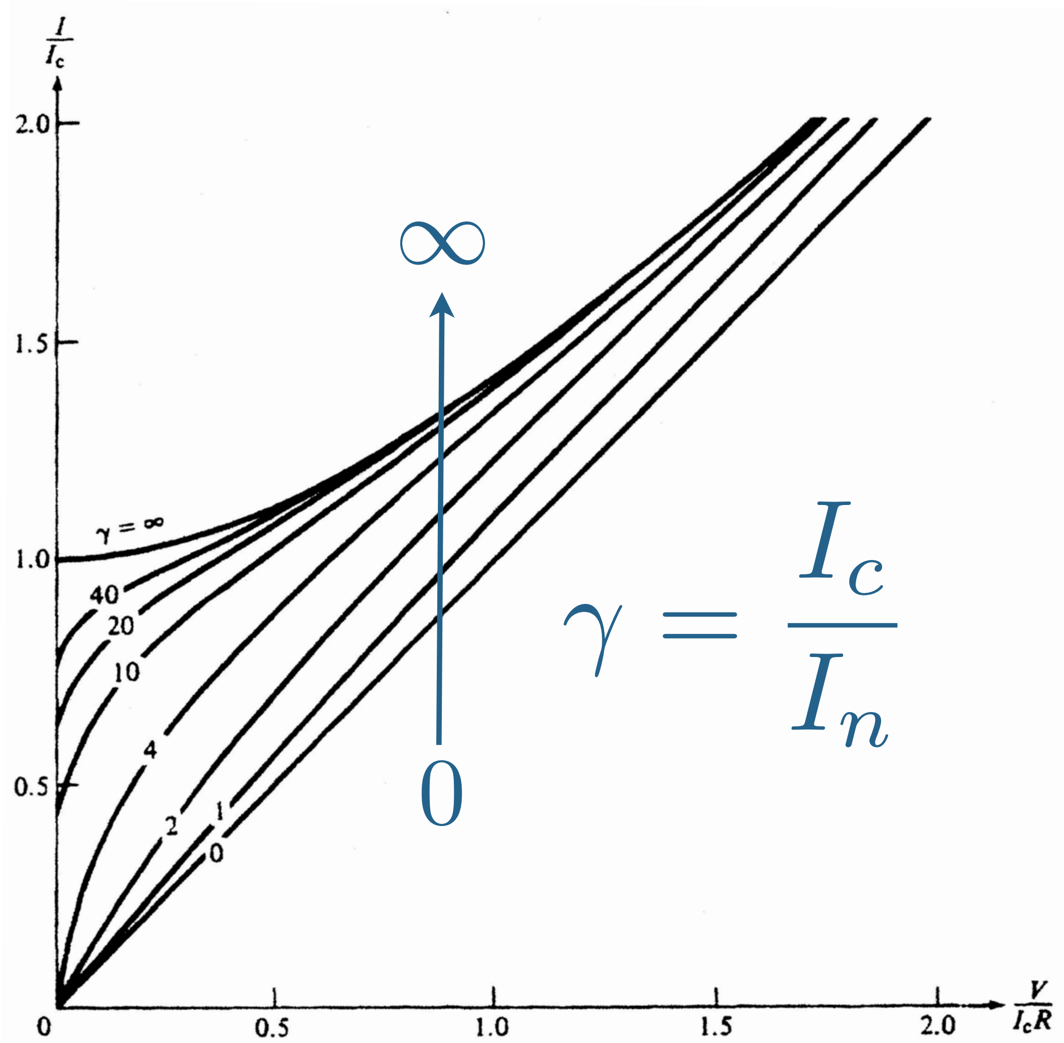
Thermal Fluctuations

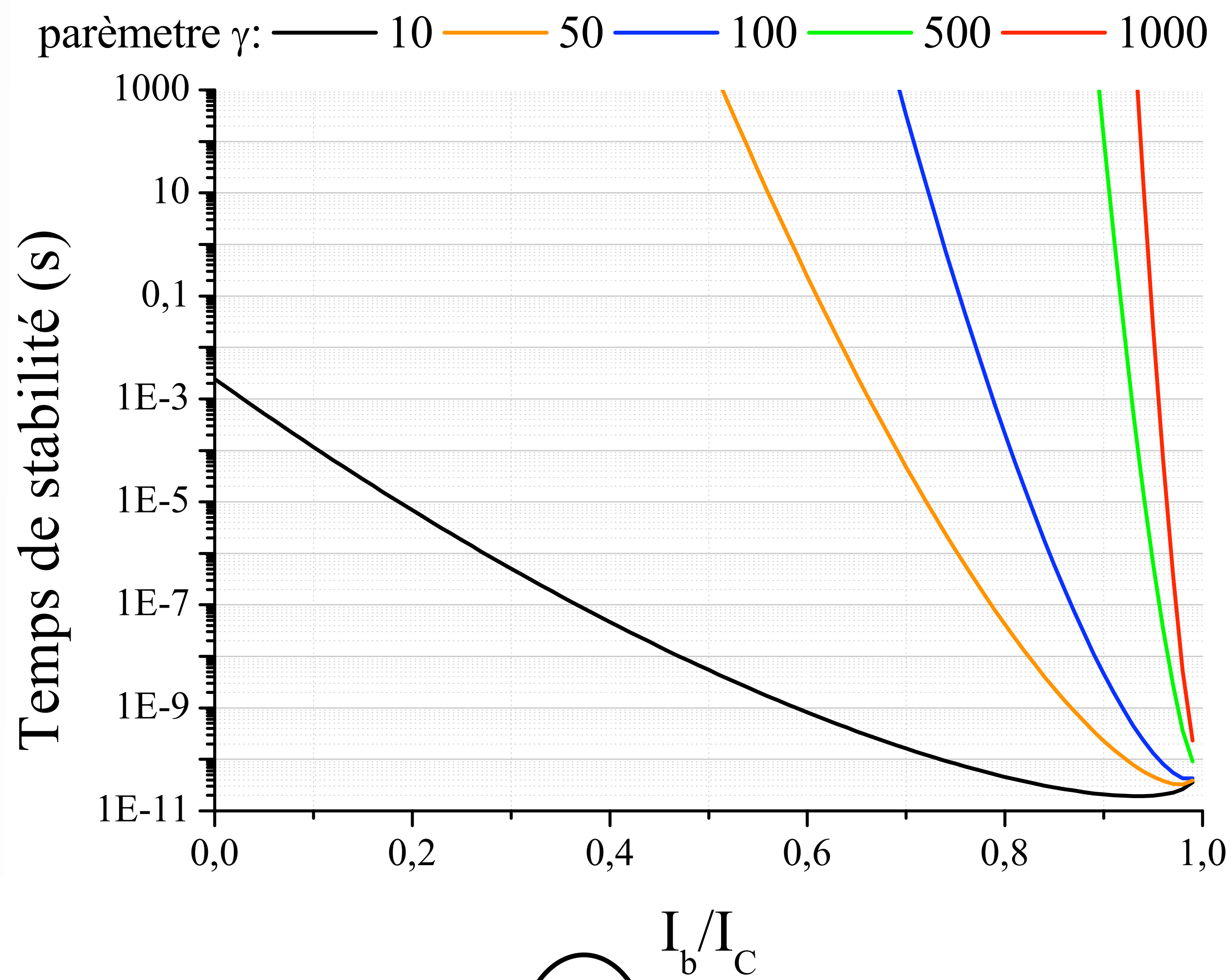
↓

Switching Errors

↓

$\gamma \geq 500 \Rightarrow I_C \geq 190\mu A$





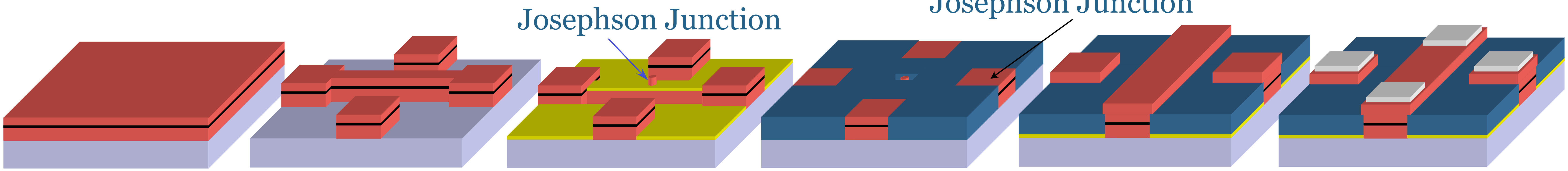
Jonction	JJ1	JJ2	JJ3	JJ4	JJ5	JJ6
γ	5384	2294	1661	1064	598	302

→ Only in output RSFQ circuits

Only thermal noise from bias resistors was considered during JSIM simulations

Réalisation des circuits NbN

Selective Niobium Etching Process (5 mask levels) [thèse R. Setzu 2007 UJF]



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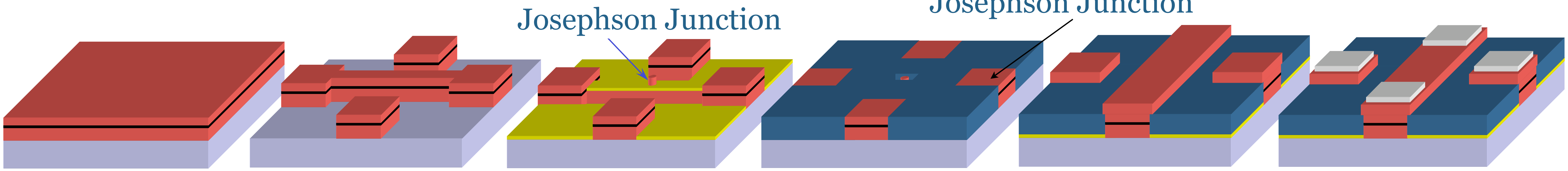
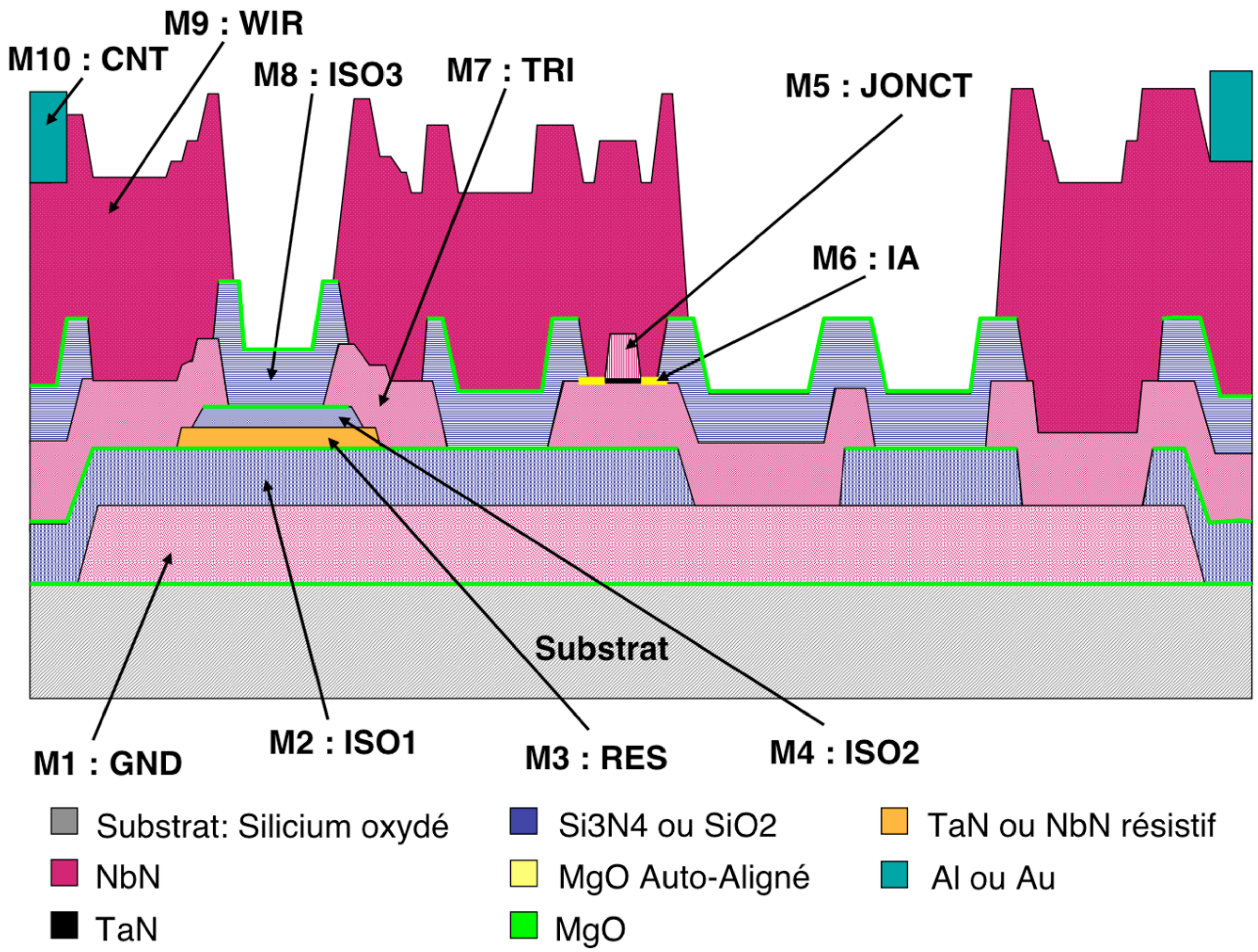
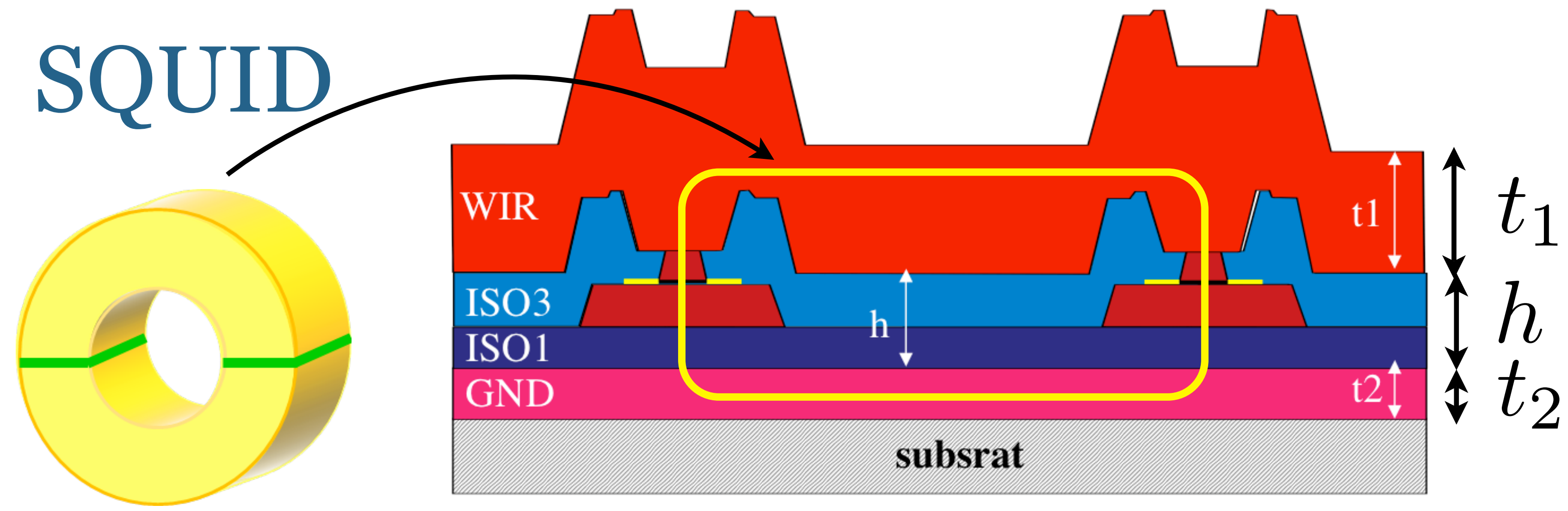


From the SNEP to the 10 mask levels process for RSFQ logic applications

- ✓ 1 NbN Common Ground Plane
- ✓ 2 NbN Interconnections Layers
- ✓ 1 Resistor Layer
- ✓ 3 SiO2 or Si3N4 Layers
- ✓ 1 Contacts Layer



Evaluation de l'inductance



$$L_\square = \frac{\mu_0}{K}[h + \lambda_L \coth(\frac{t_1}{\lambda_L}) + \lambda_L \coth(\frac{t_2}{\lambda_L})]$$

Problem:

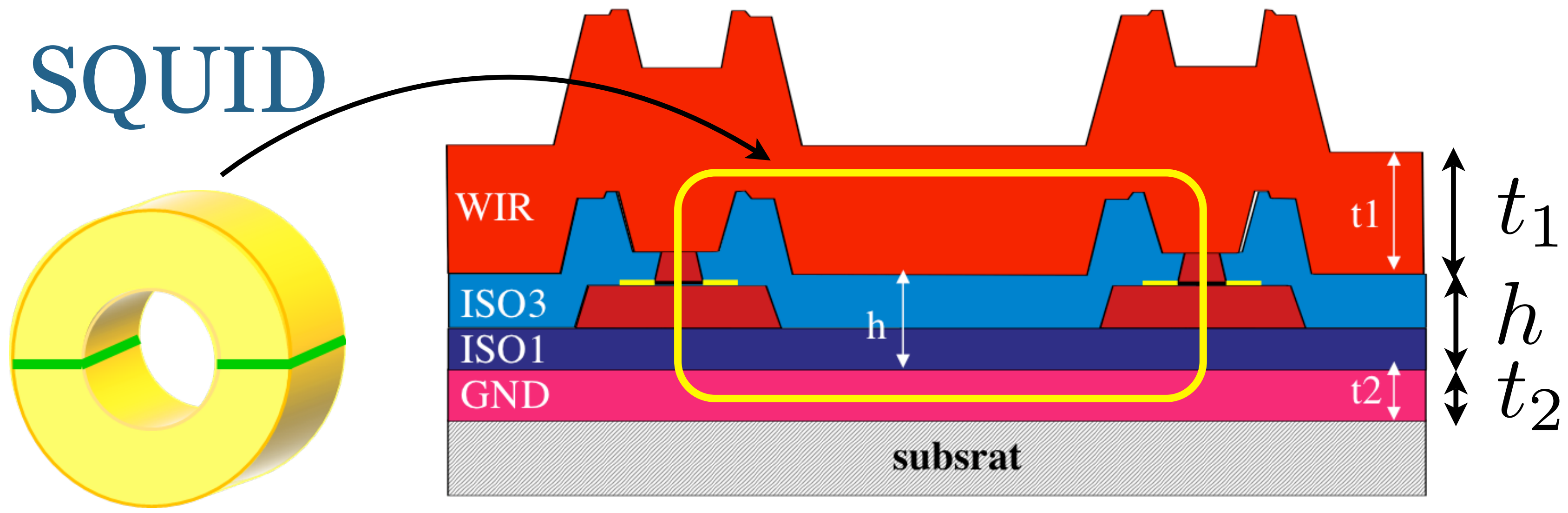
$$I_{C[min]}(\text{NbN}) \sim 2 \times I_{C[min]}(\text{Nb})$$

$$LI_C \leq 0.5\Phi_0$$

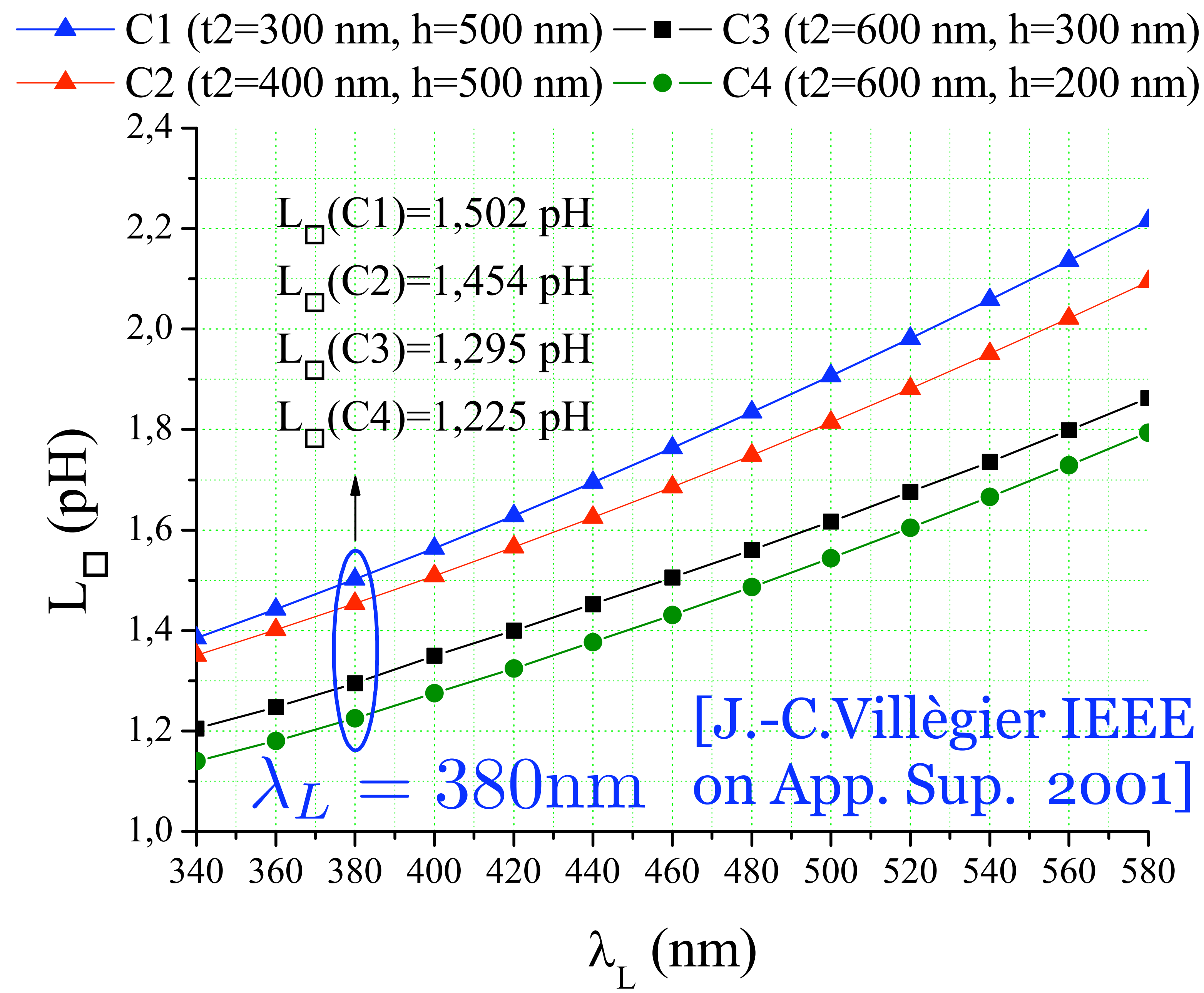
(Ex. $I_C = 400\mu\text{A} \longrightarrow L \leq 2.5\text{pH}$)

$$L_\square \leq 1.2\text{pH}$$

Evaluation de l'inductance



$$L_\square = \frac{\mu_0}{K}[h + \lambda_L \coth(\frac{t_1}{\lambda_L}) + \lambda_L \coth(\frac{t_2}{\lambda_L})]$$



Problem:

$$I_{C[min]}(\text{NbN}) \sim 2 \times I_{C[min]}(\text{Nb})$$

$$LI_C \leq 0.5\Phi_0$$

(Ex. $I_C = 400\mu\text{A} \longrightarrow L \leq 2.5\text{pH}$)

$$L_\square \leq 1.2\text{pH}$$

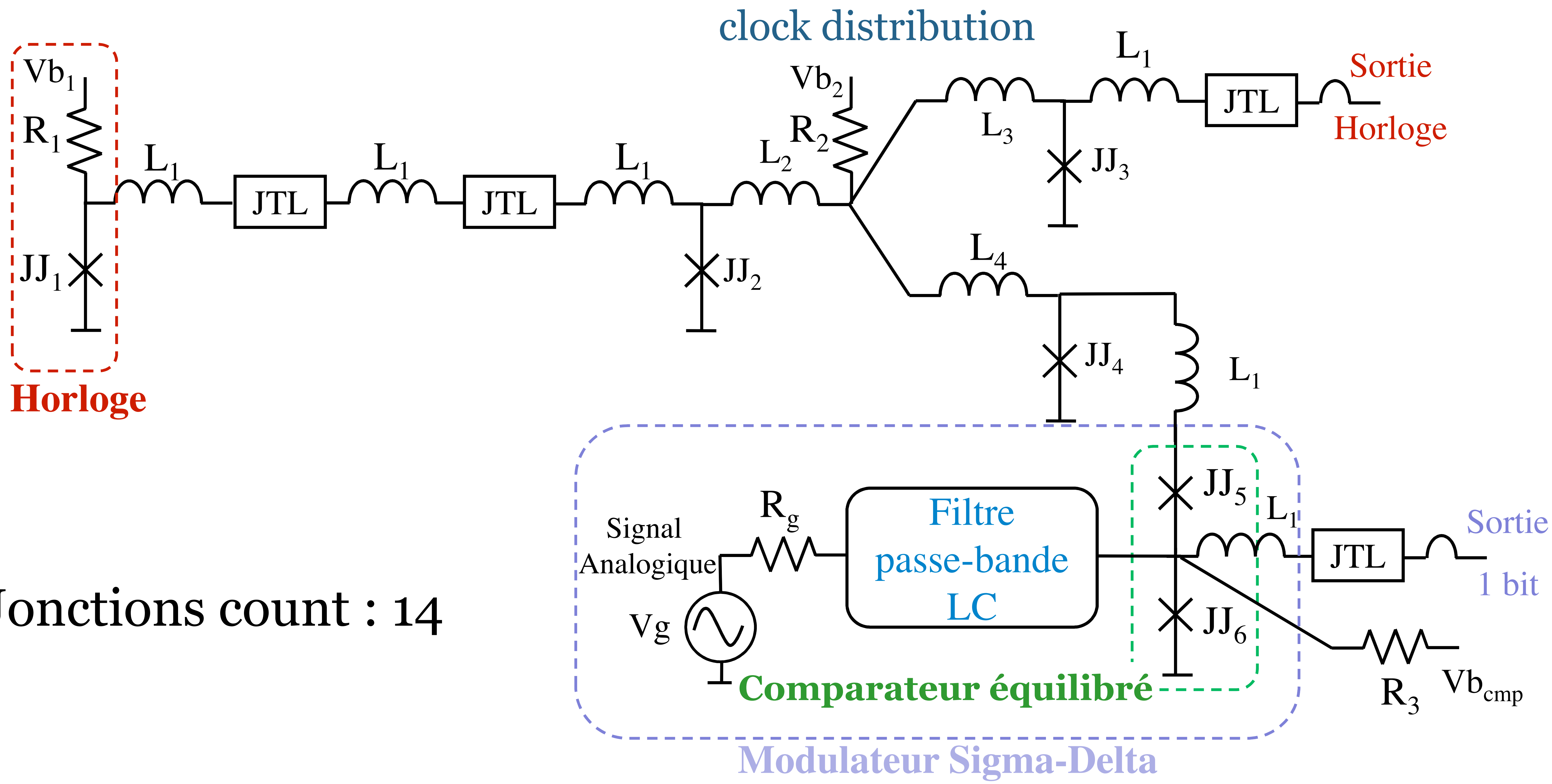
- For small $L_\square$, t_1 et t_2 must be higher than λ_L
- For high t_2 the GND roughness increases

$t_1 = 900\text{nm}\,;t_2 = 400\text{nm}$

$h = 300 + 200 = 500\text{nm}$

$L_\square = 1.45\text{pH}$

Etude du modulateur ΣΔ



Jonctions count : 14

50 Ω (analog input signal) ⟷ 2 Ω (comparator + JTL)

Band-pass filter with Fc=30 GHz and B=500 MHz

⇩

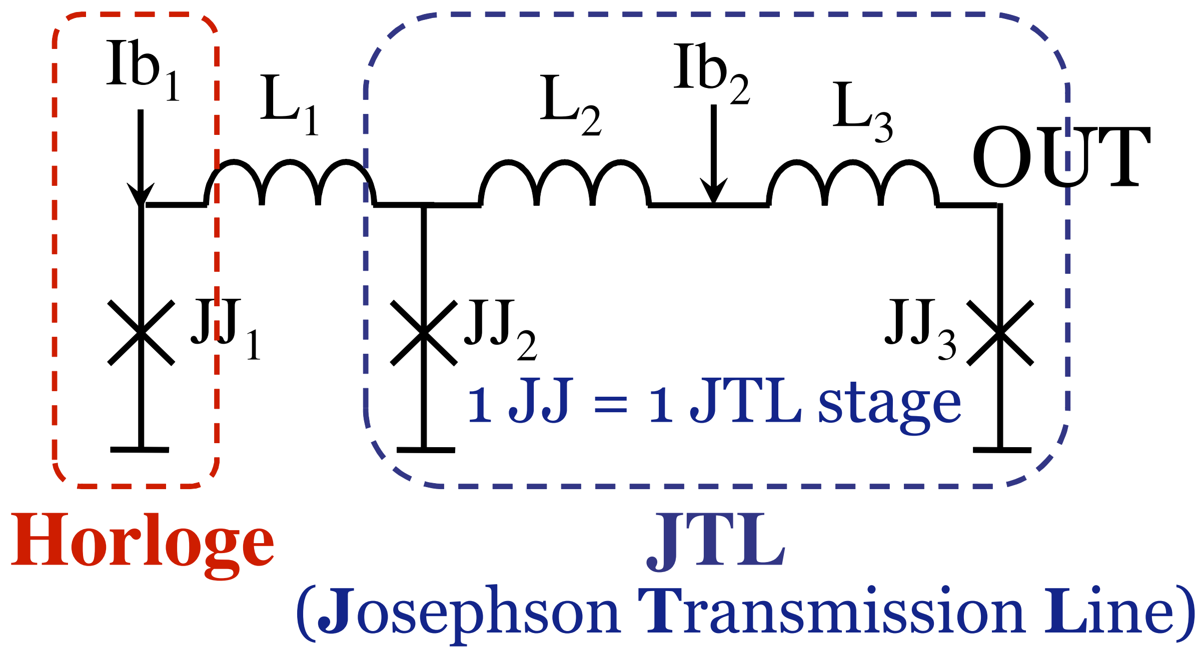
Order 3

Etude de l'horloge

Possible clock solutions:

- JTL ring
- Long JJ
- Optical clock
- **Overbiased single JJ**

The sampling frequency is tuned to 205 GHz by adjusting Ib_1

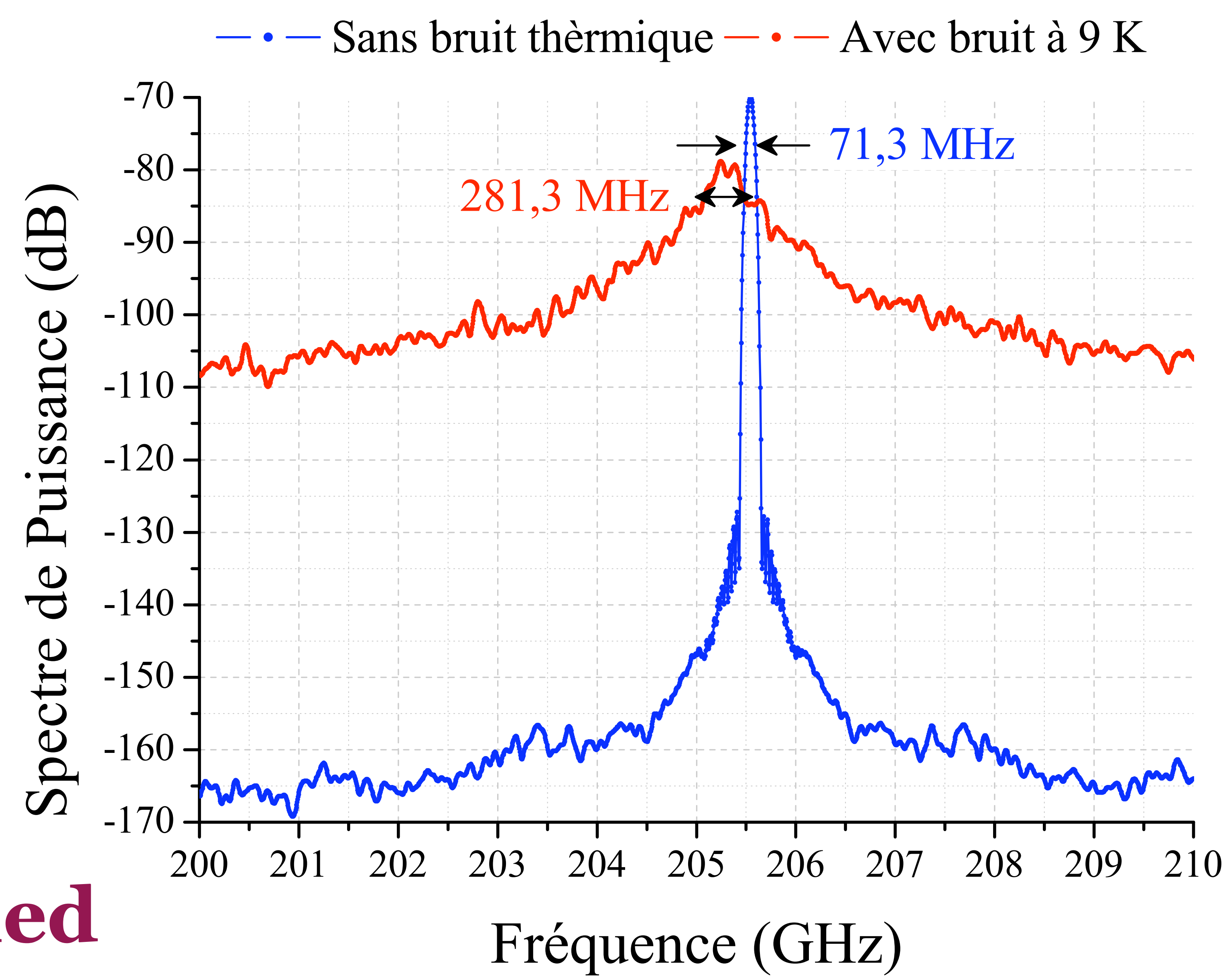


The spectral bandwidth increases with the temperature

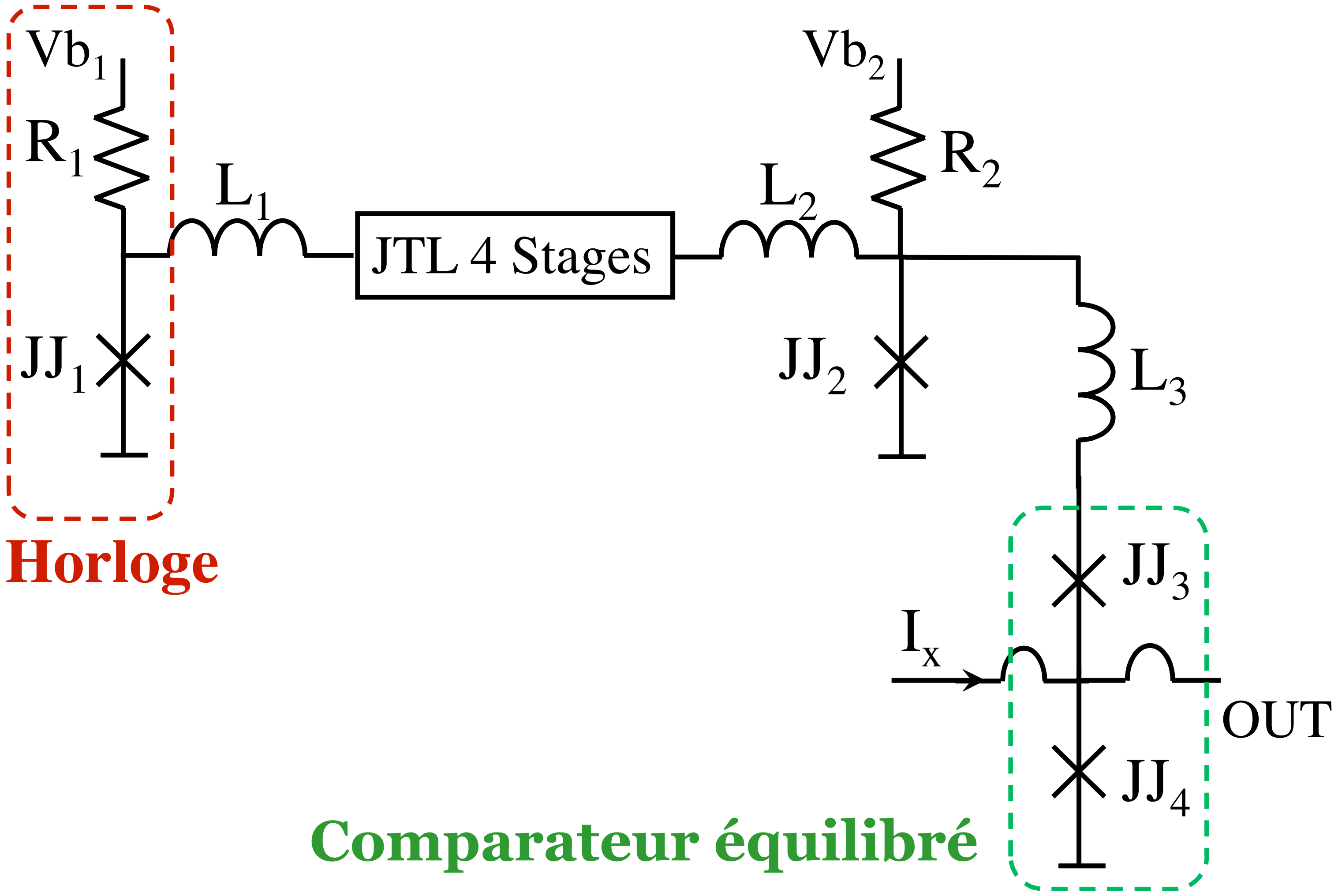
The quality factor decreases

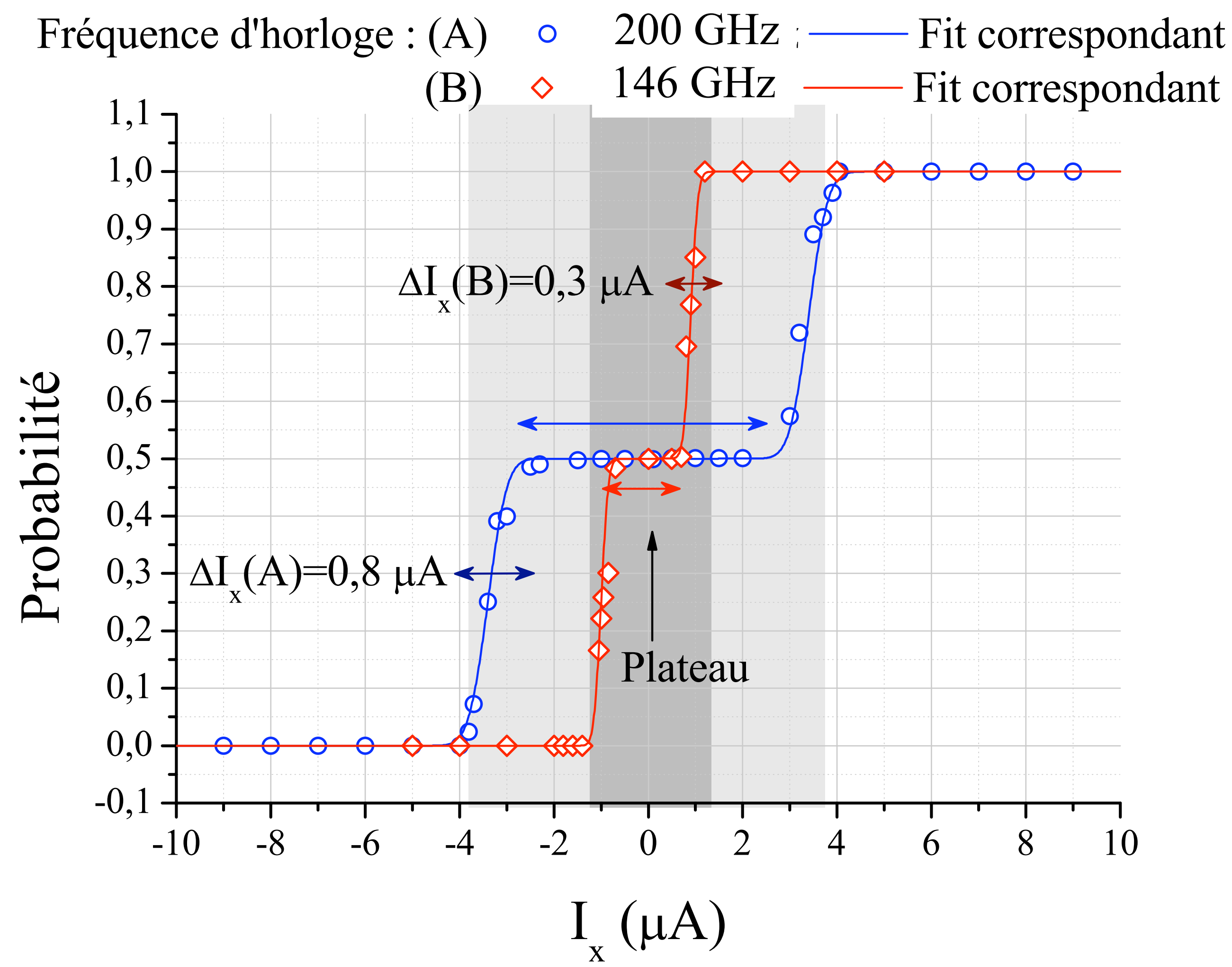
$$Q_{0K} = 2875 \Rightarrow Q_{9K} = 730$$

Jitter limitation to be studied

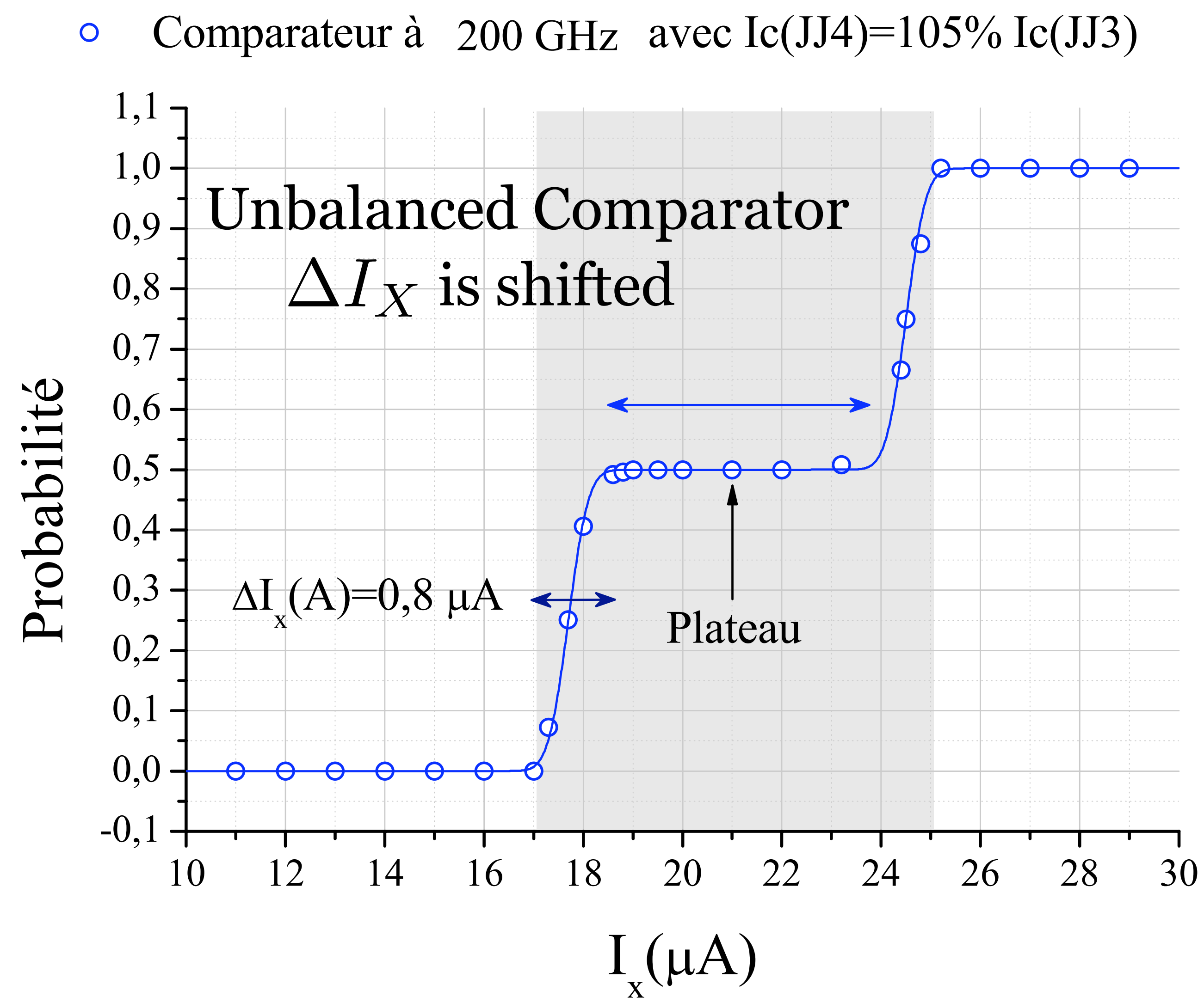


Etude du comparateur





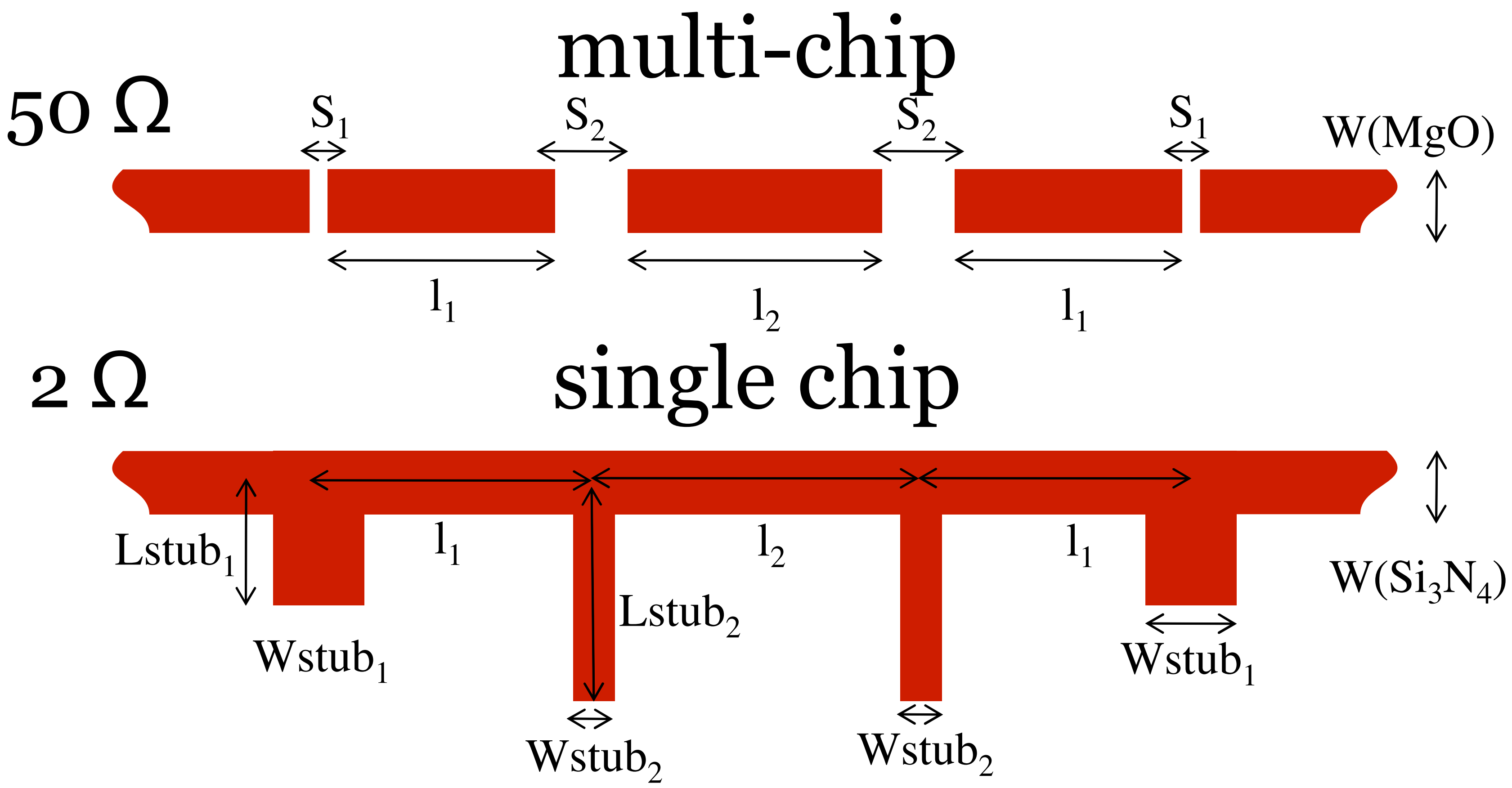
Switching probability $P = \dfrac{< V(JJ4) >}{< V(JJ1) >}$

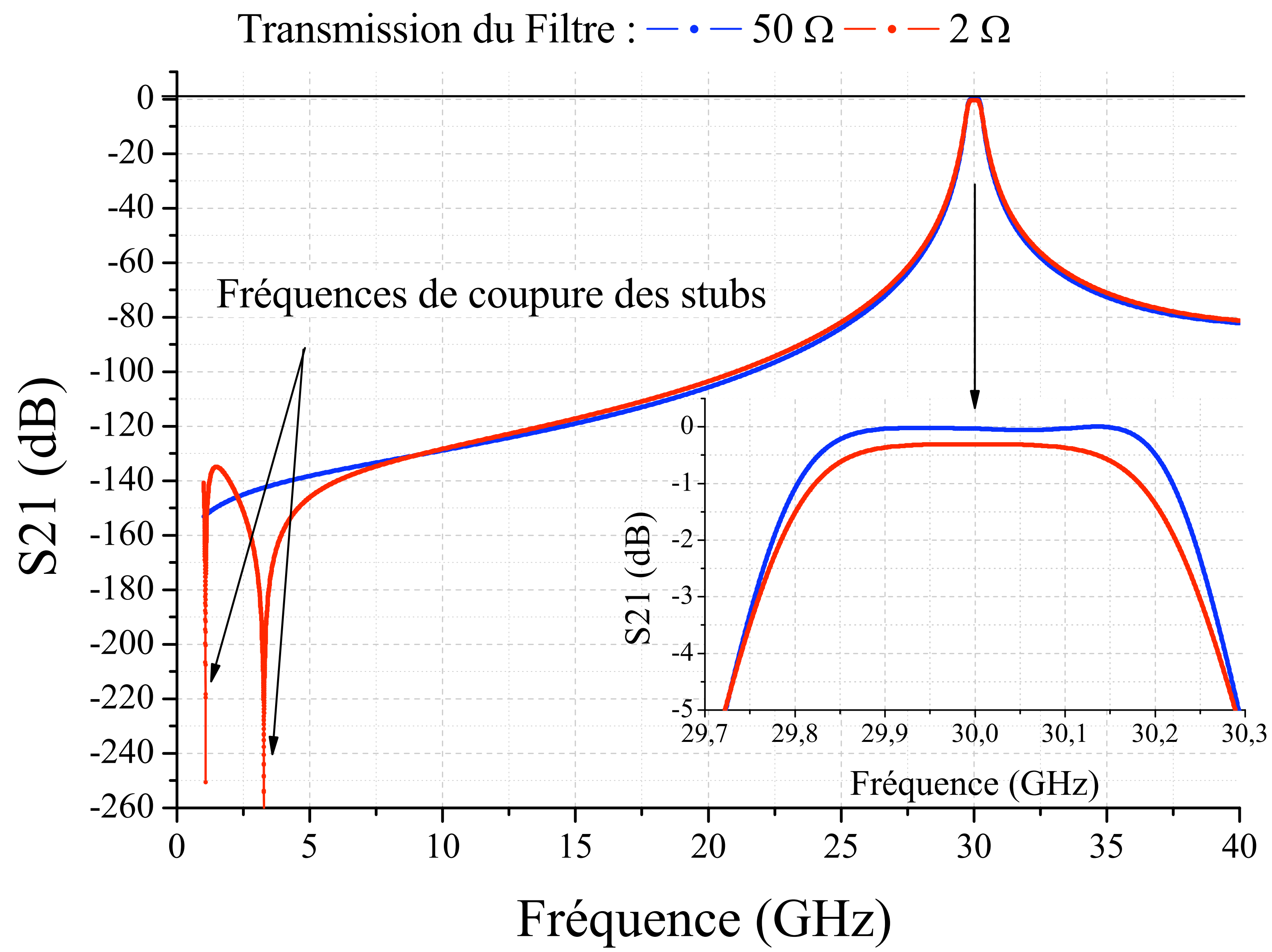


✓The ***gray zone*** and the ***plateau*** could be decreased of 25% from 200 GHz to 146 GHz of sampling frequency

✓The ***gray zone*** is about 5 times smaller than that obtained with the Nb technology

Etude du filtre analogique

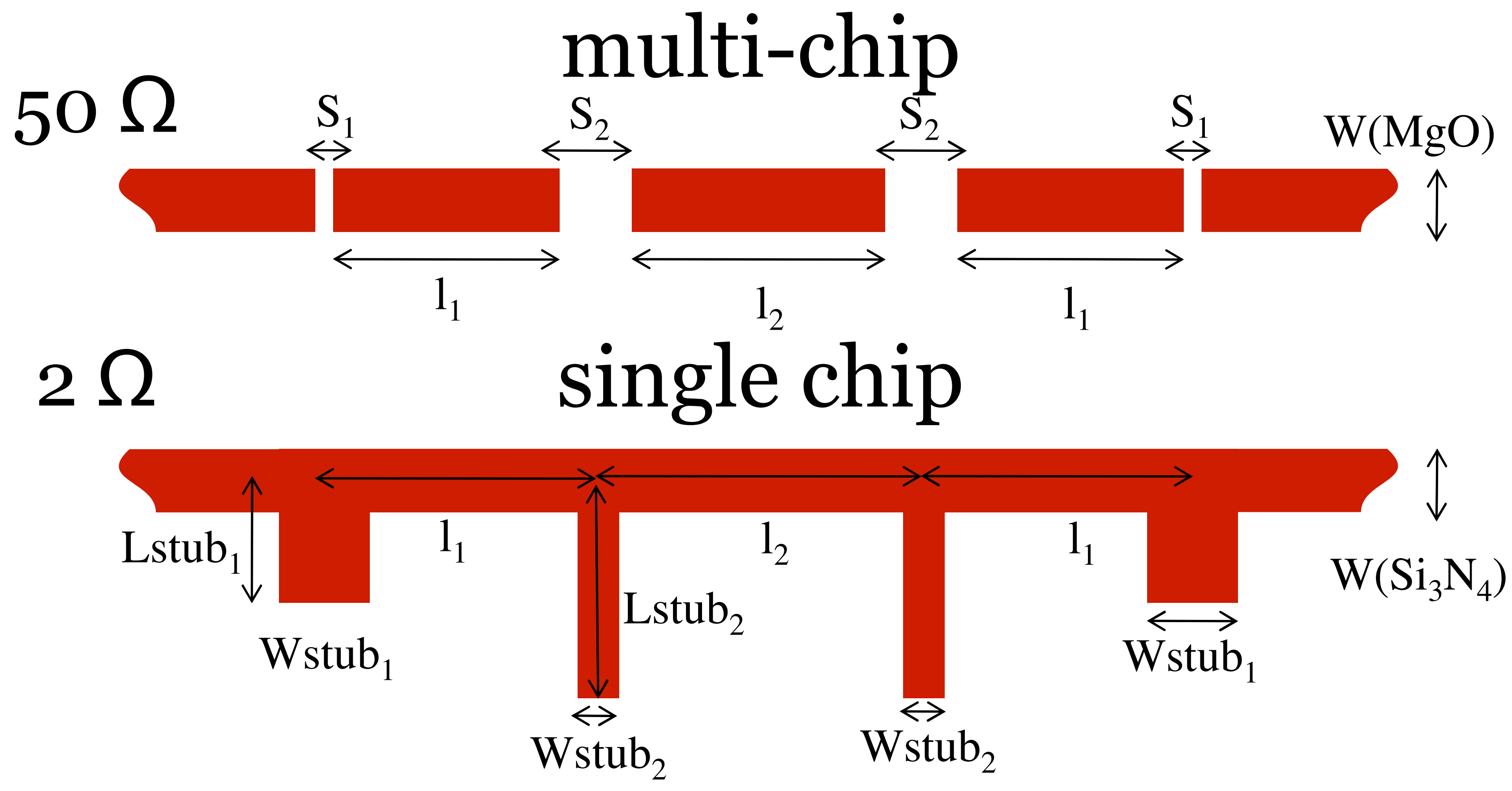


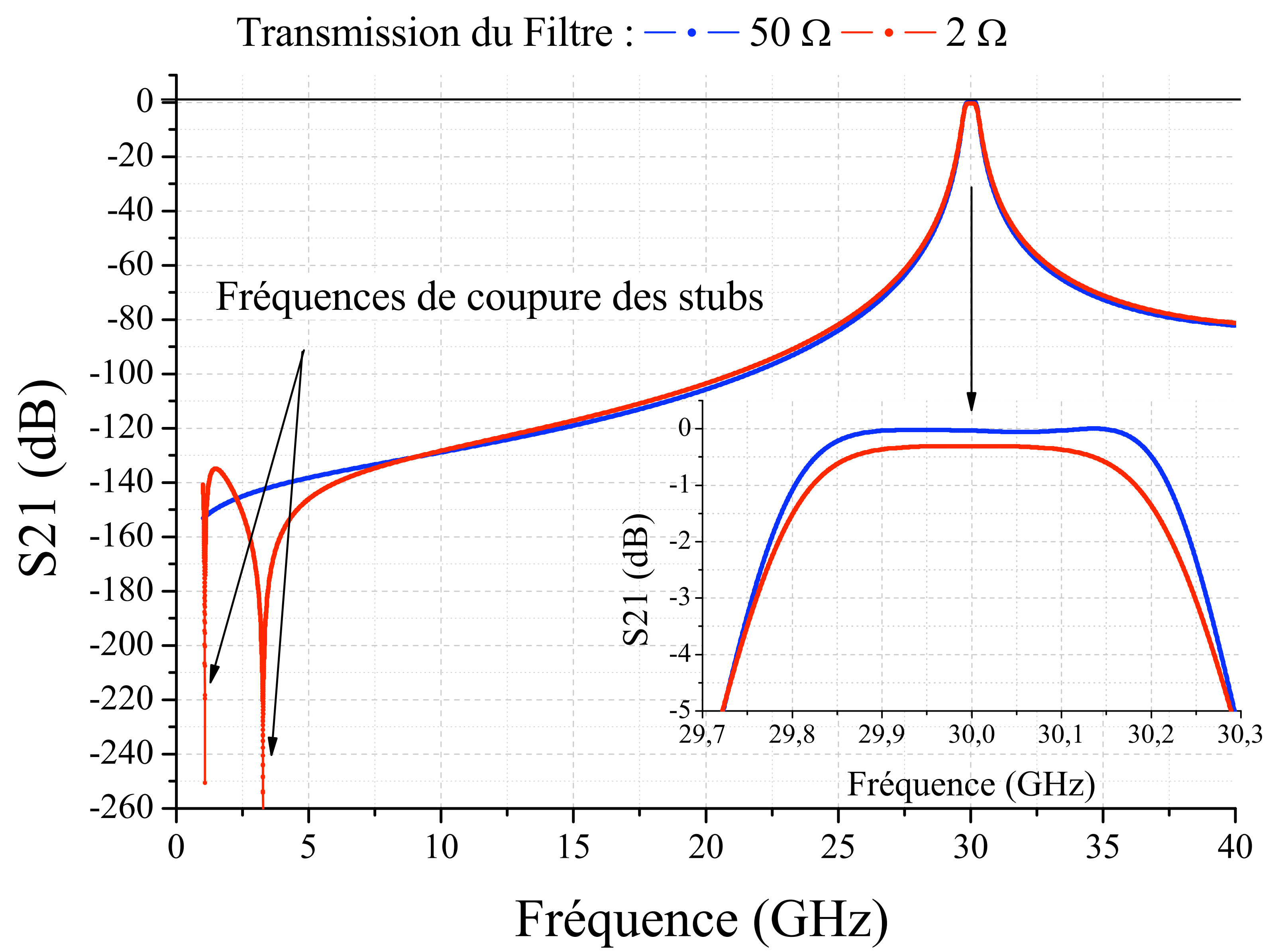


50 Ω: Fc=30.008 GHz, B=507 MHz and A=0.05 dB

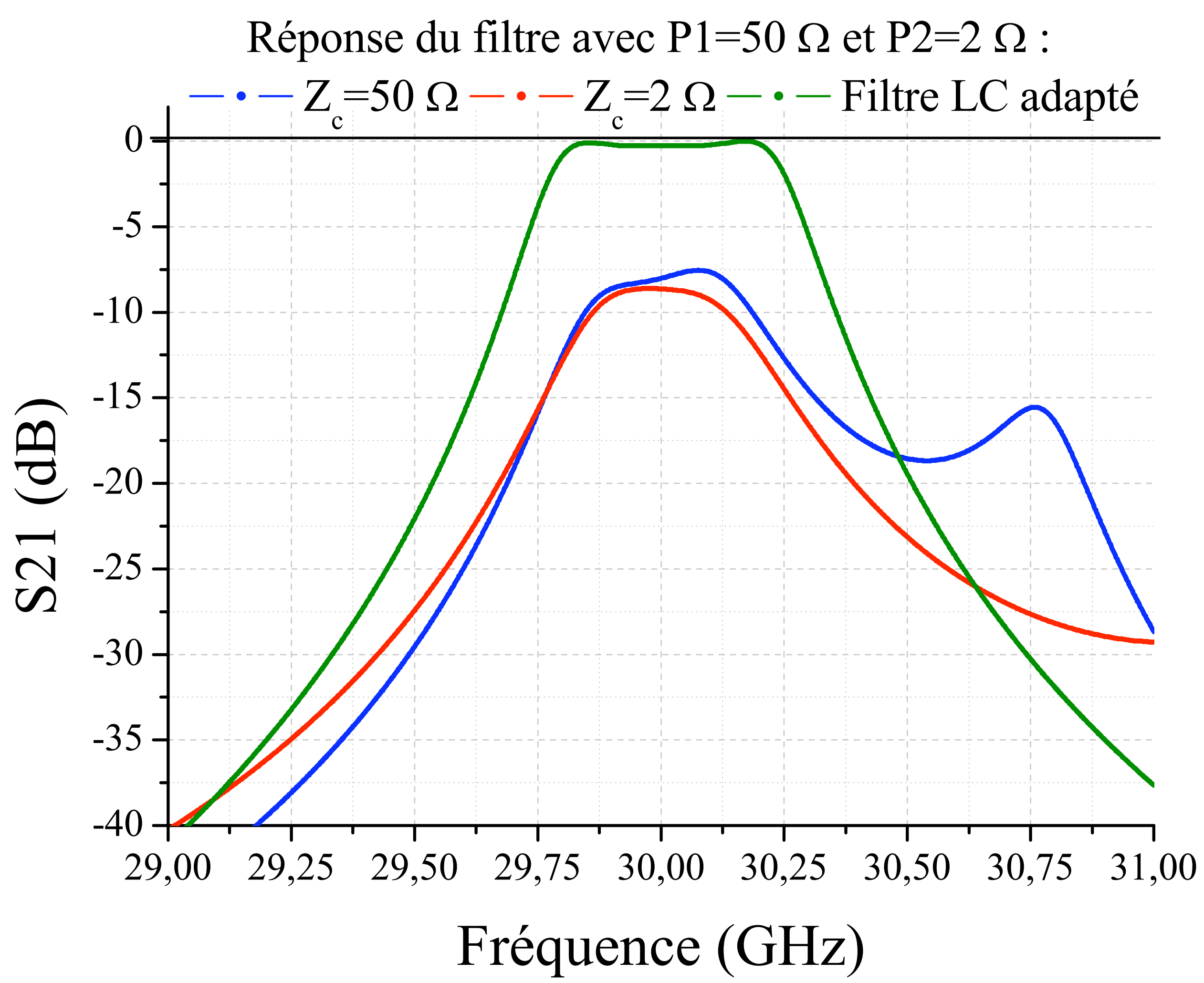
2 Ω: Fc=30.004 GHz, B=489 MHz and A=0.3 dB

Etude du filtre analogique





Matching problems



50 Ω: Fc=30.008 GHz, B=507 MHz and A=0.05 dB

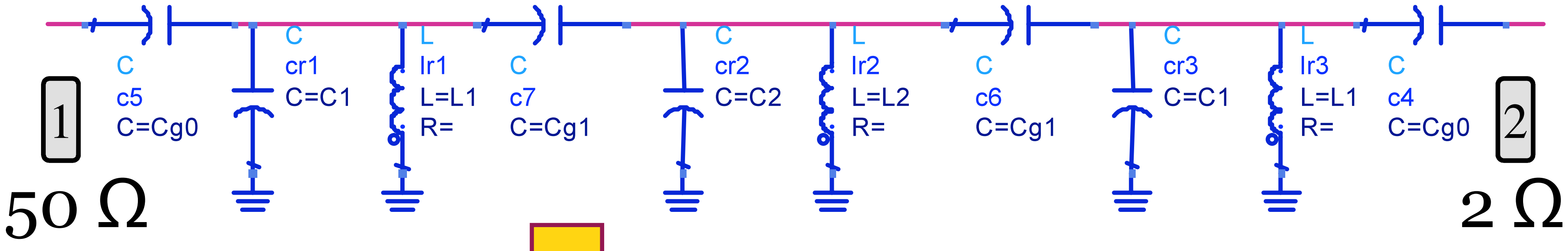
2 Ω: Fc=30.004 GHz, B=489 MHz and A=0.3 dB

Filter specifications results

Zc=2 Ω, Fc=30 GHz,
B=357 MHz and Att=8.64 dB

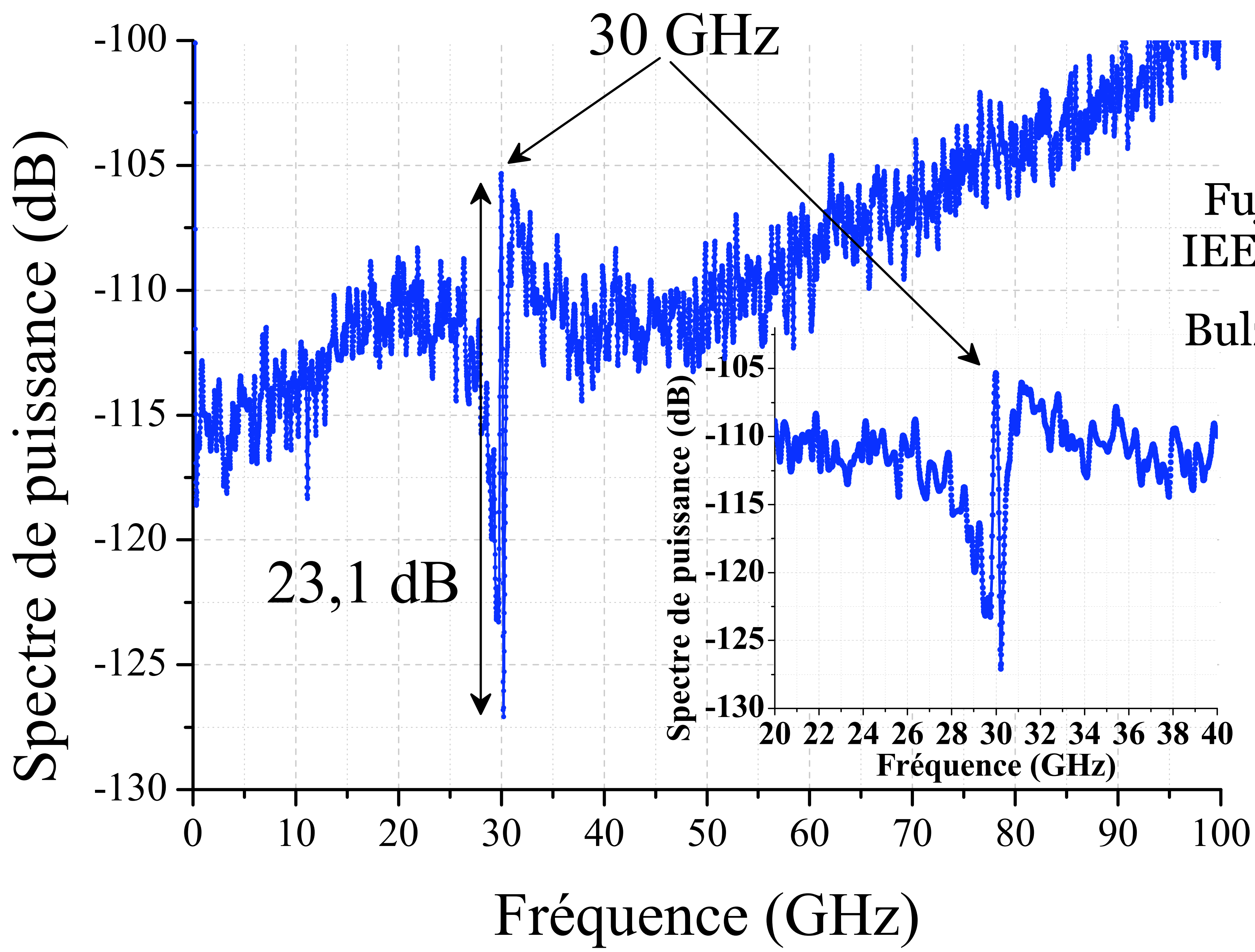
Performance du modulateur ΣΔ

LC Filter equivalent circuit



used for the JSIM simulations

Sigma-Delta Modulator Spectrum



- Comparator bias adjusted for 37% of 1
- Sine input signal: Vpp=200 μV, F=30 GHz

	Fs (GHz)	OSR	*l*	Vpp (mV)	SNR (dB)
Fujimaki IEEE 2003	20	100	1	/	44.5
Bulzachelli	20	256	1	340	24
	200	200	3	0.2	23.1

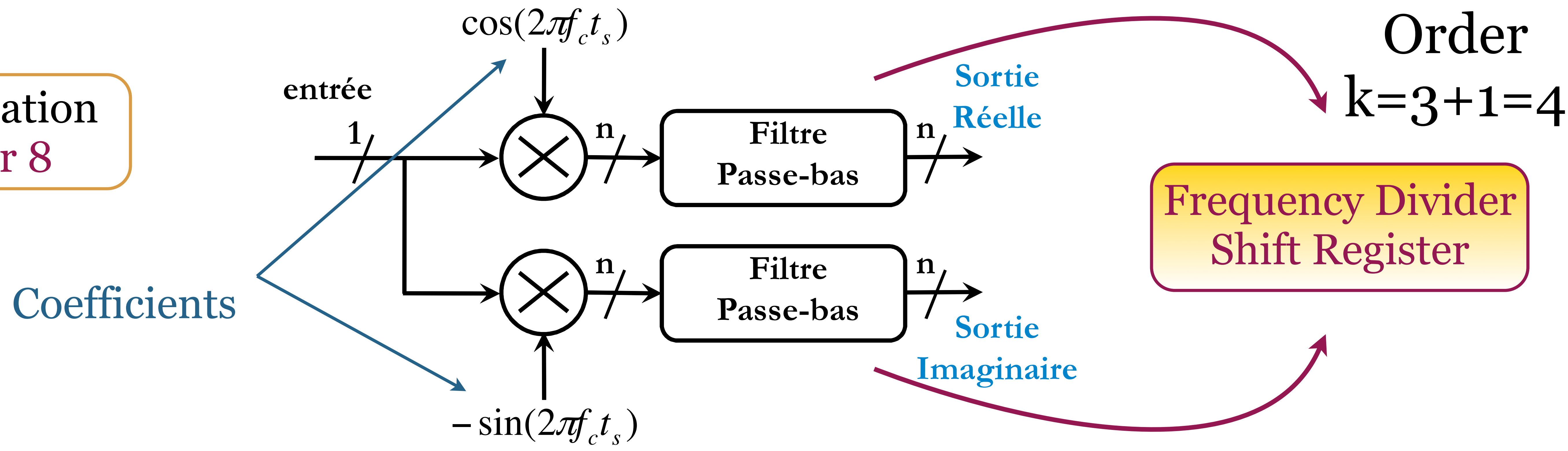
High sensibility

- Matching and comparator coupling to be improved
- Comparator *Plateau* to be suppressed

Expected SNR of 141 dB

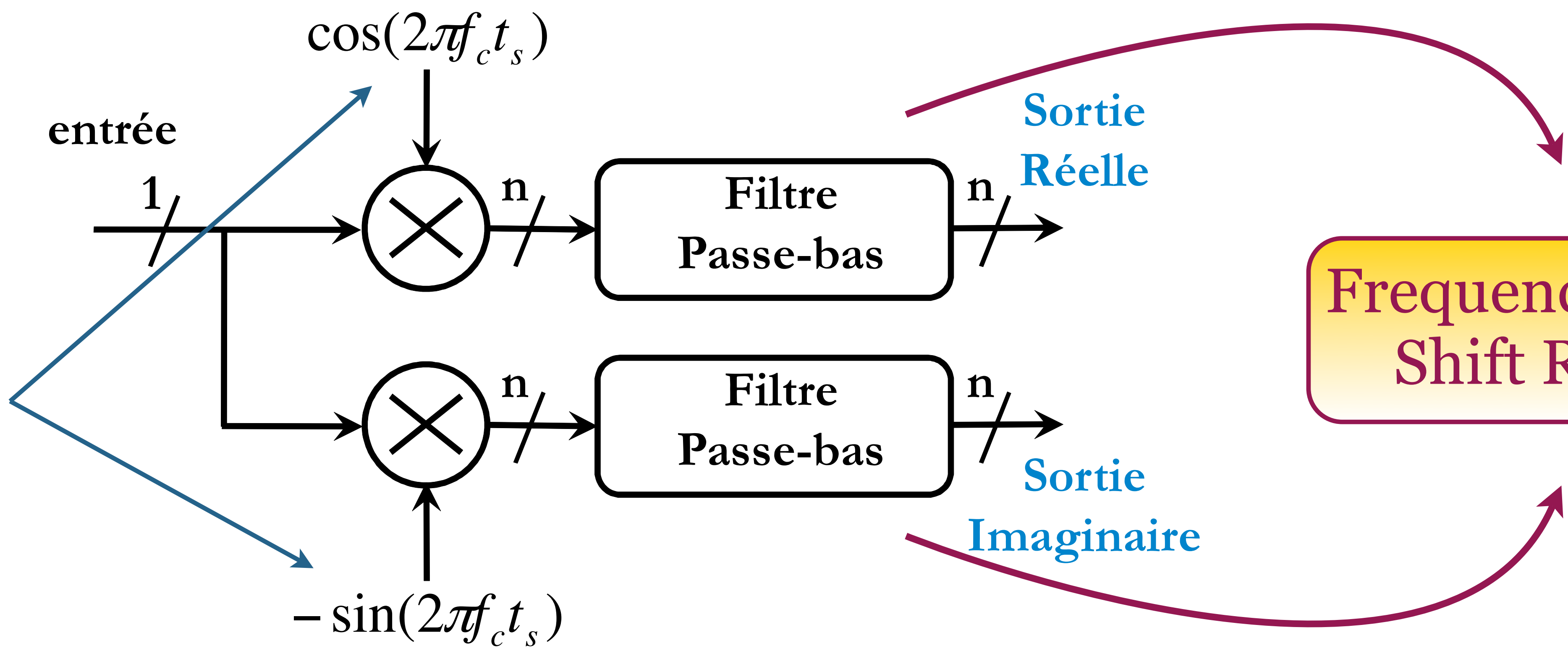
Etude du filtre de décimation (1/2)

Easy implementation for Fs/Fc=4 or 8



Etude du filtre de décimation (1/2)

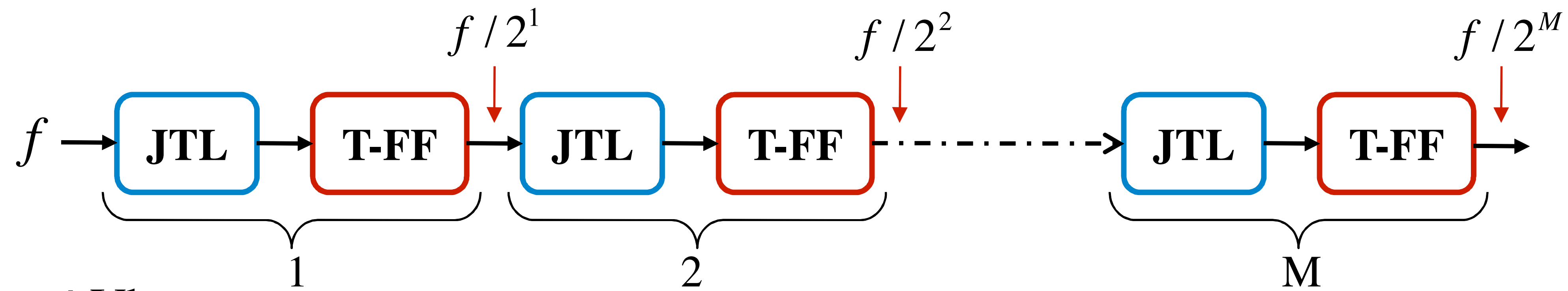
Easy implementation for Fs/Fc=4 or 8



Order k=3+1=4

Frequency Divider Shift Register

✓ Frequency divider

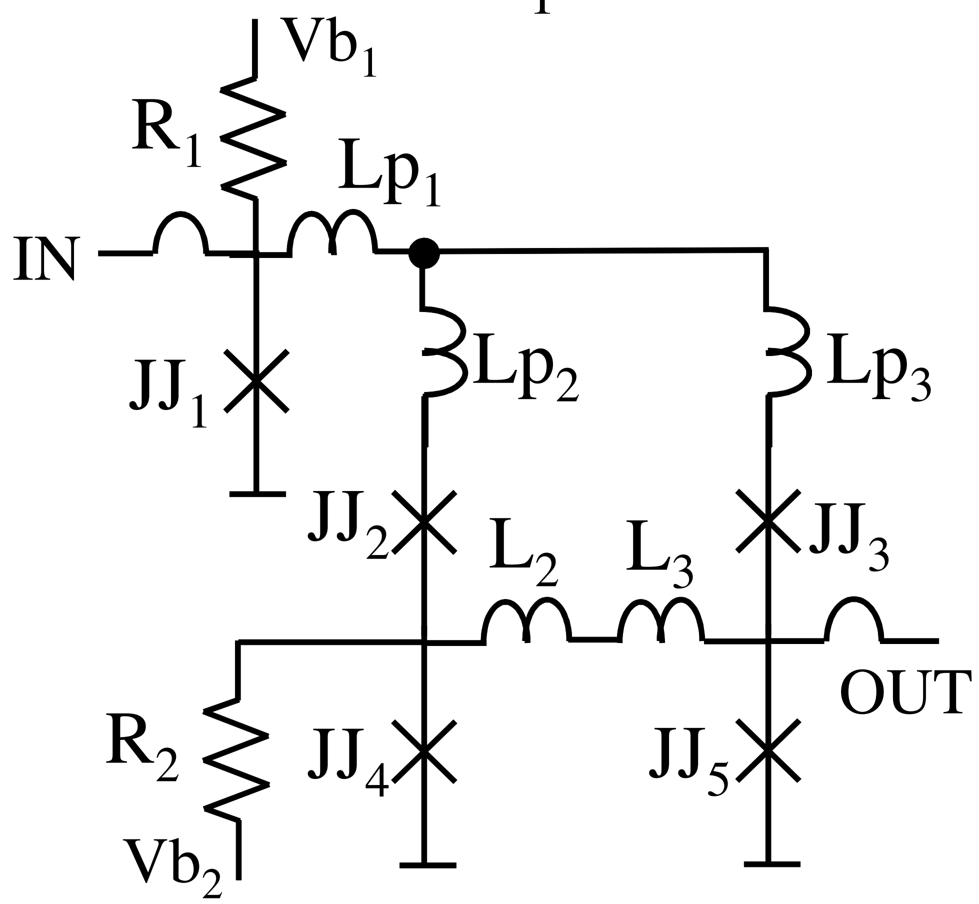


Fs/Fc=4

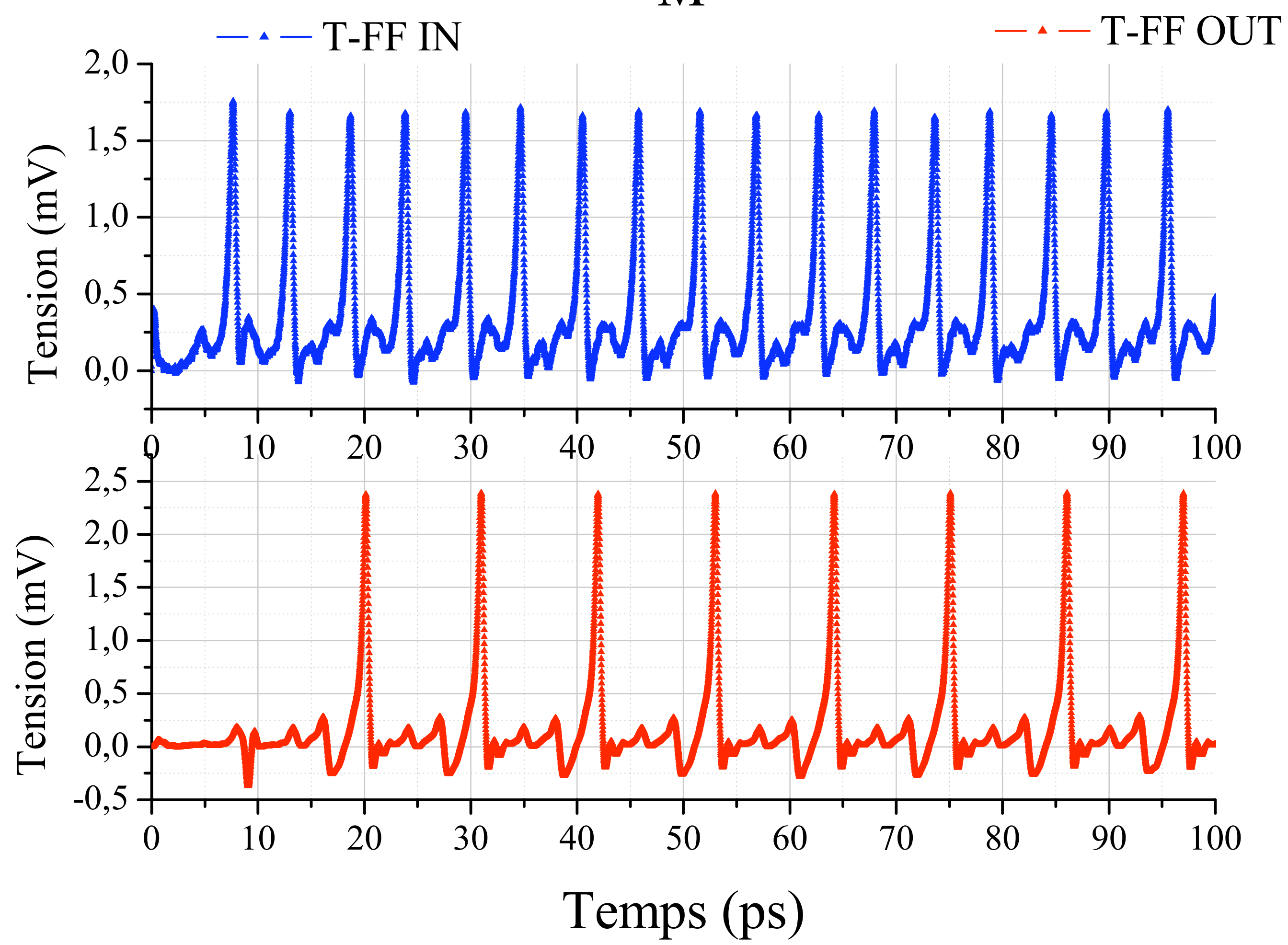
Fs=120 GHz
Decimation 1:128
[49 JJs]

Fs/Fc=8

Fs=240 GHz
Decimation 1:256
[56 JJs]



Toggle-Flip Flop (5 JJs)

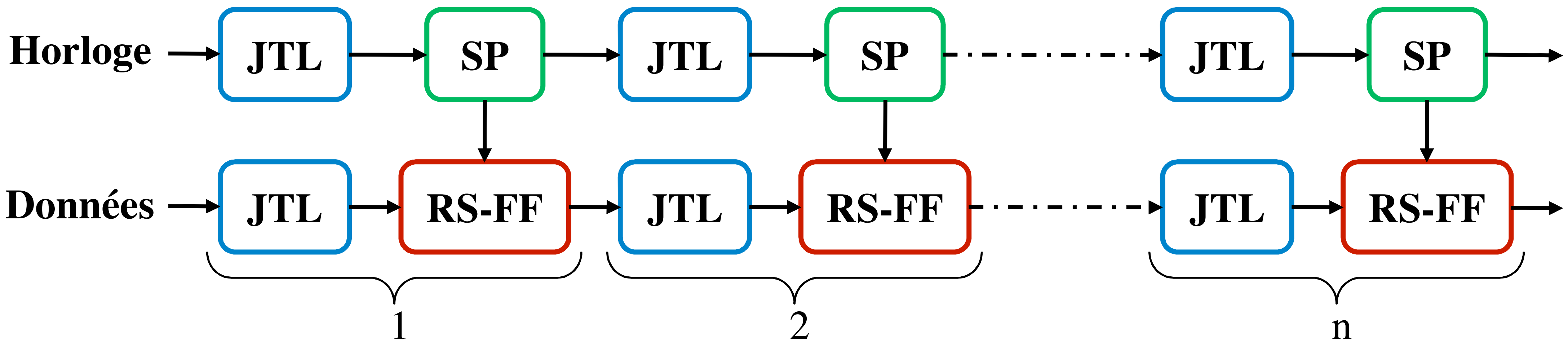


Etude du filtre de décimation (2/2)

For 1 Low-pass Decimation Filter (DF):

4 Accumulators and 4 Differentiators → 8 SR of 33 bits eachone

✓ Shift Register (SR)



1 SR of 33 bits
[396 JJs]

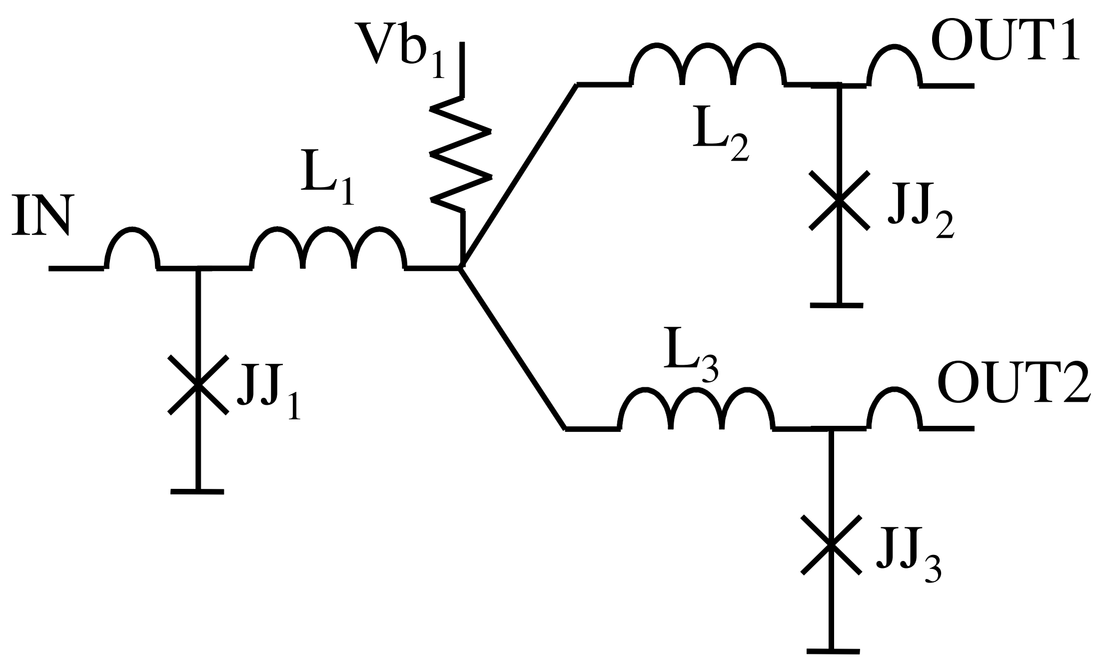
↓

8 SR
[3168 JJs]

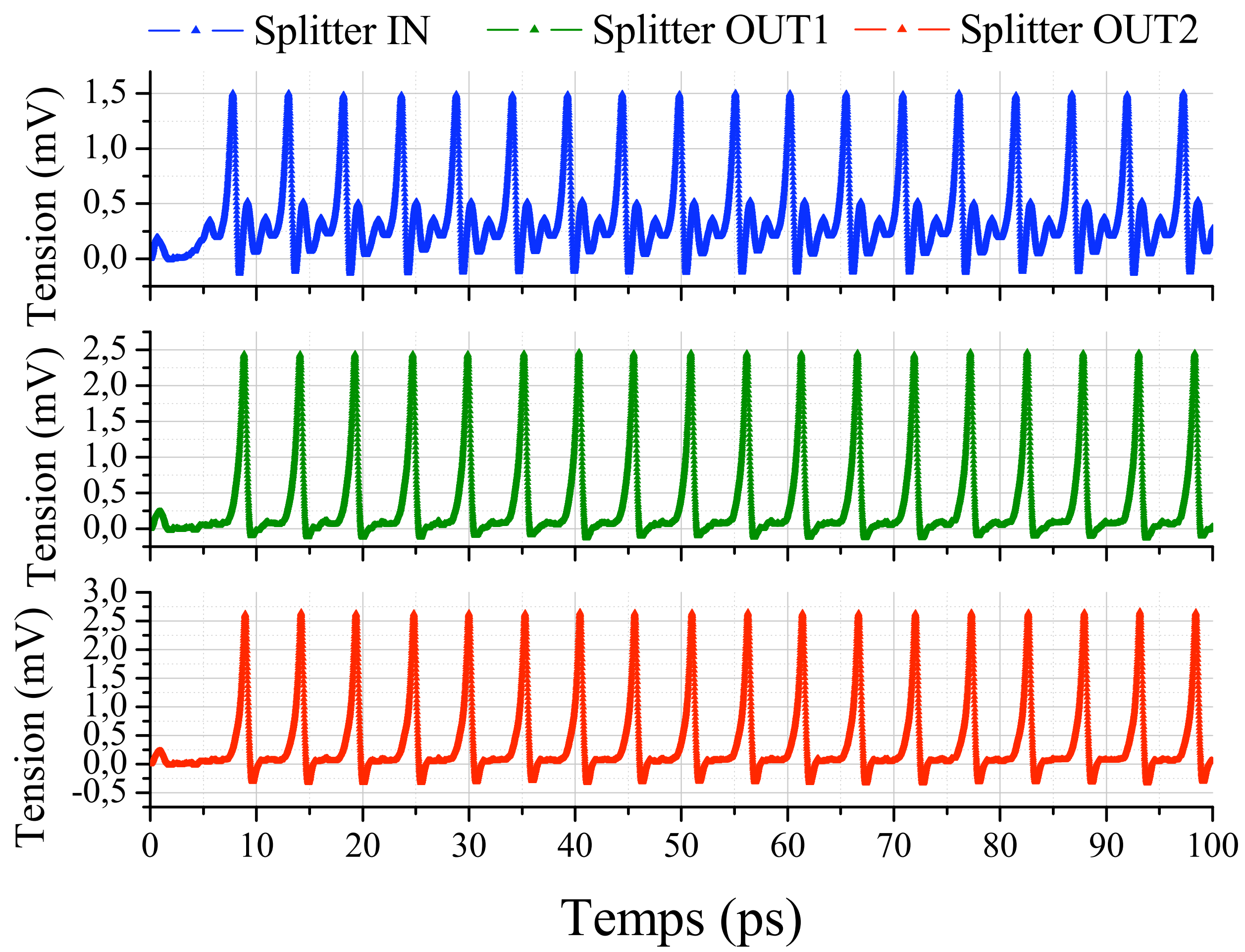
↓

1 Low-pass DF
[~3500 JJs]

1 bit SR → 12 JJs



Splitter (3 JJs)

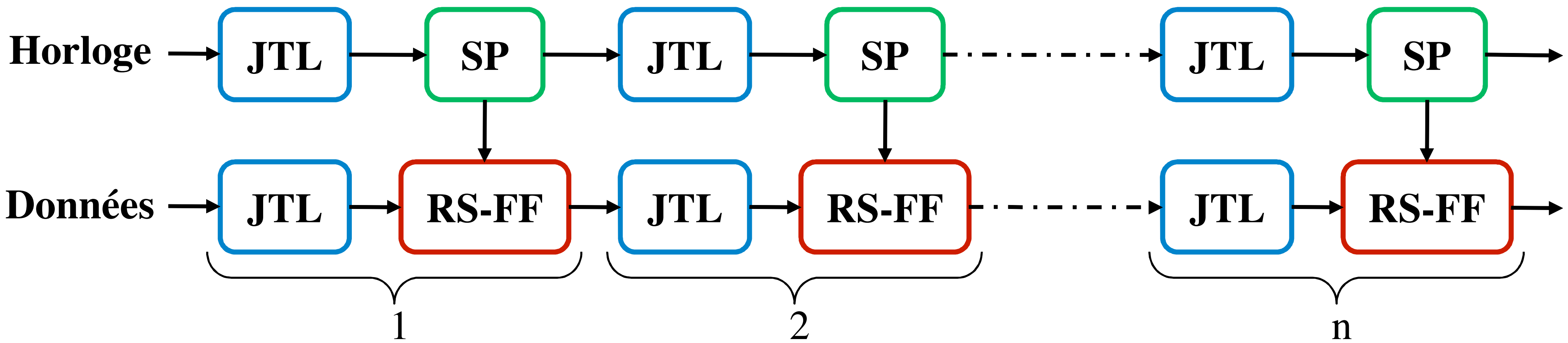


Etude du filtre de décimation (2/2)

For 1 Low-pass Decimation Filter (DF):

4 Accumulators and 4 Differentiators ➡ 8 SR of 33 bits eachone

✓ Shift Register (SR)

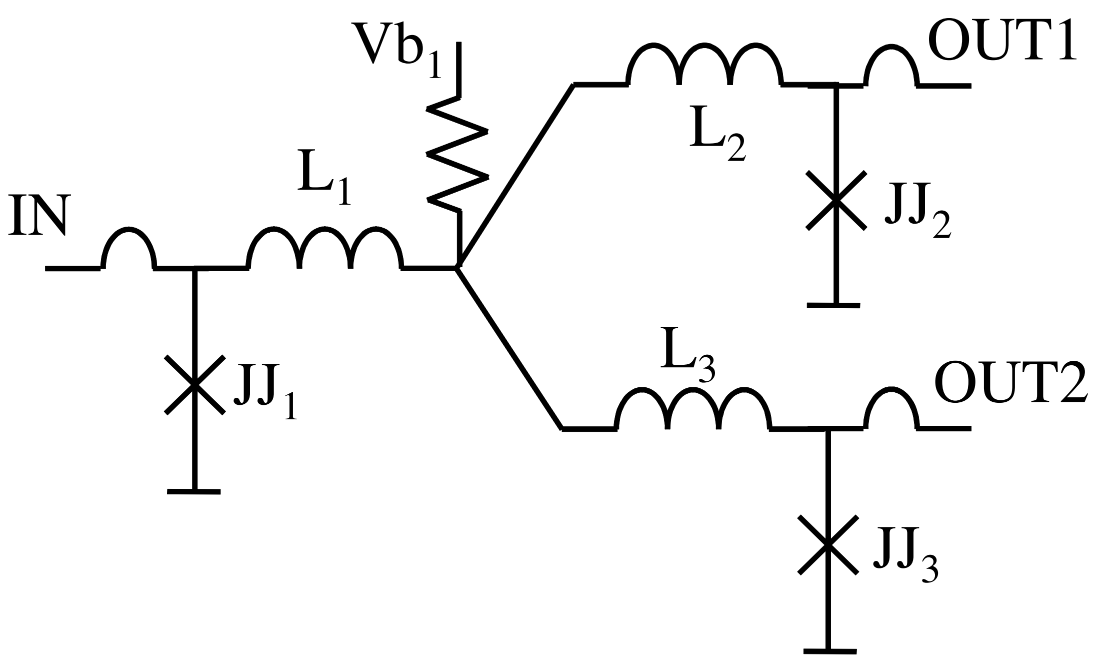


1 bit SR → 12 JJs

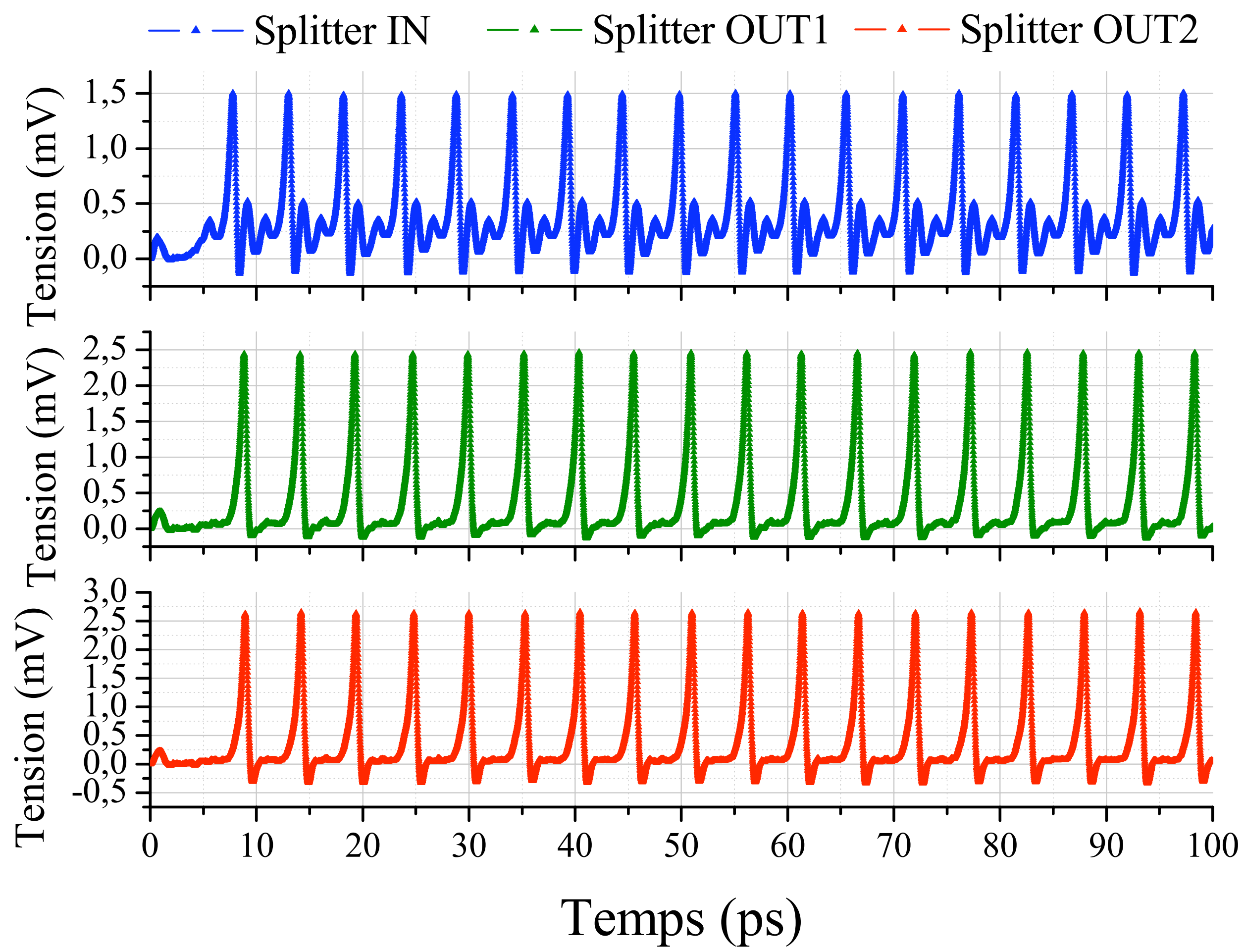
1 SR of 33 bits
[396 JJs]

8 SR
[3168 JJs]

1 Low-pass DF
[~3500 JJs]



Splitter (3 JJs)



Band-Pass Decimation filter:

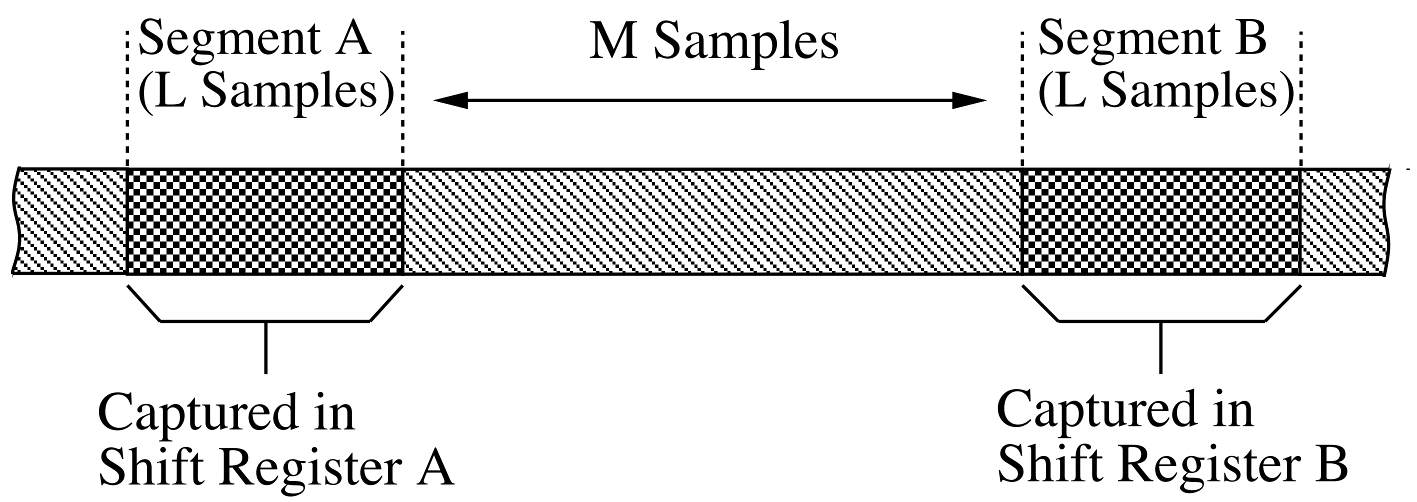
✳Fs/Fc=4 [~7500 JJs]
- coefficients: 0,±1
- 2 Low-Pass DFs

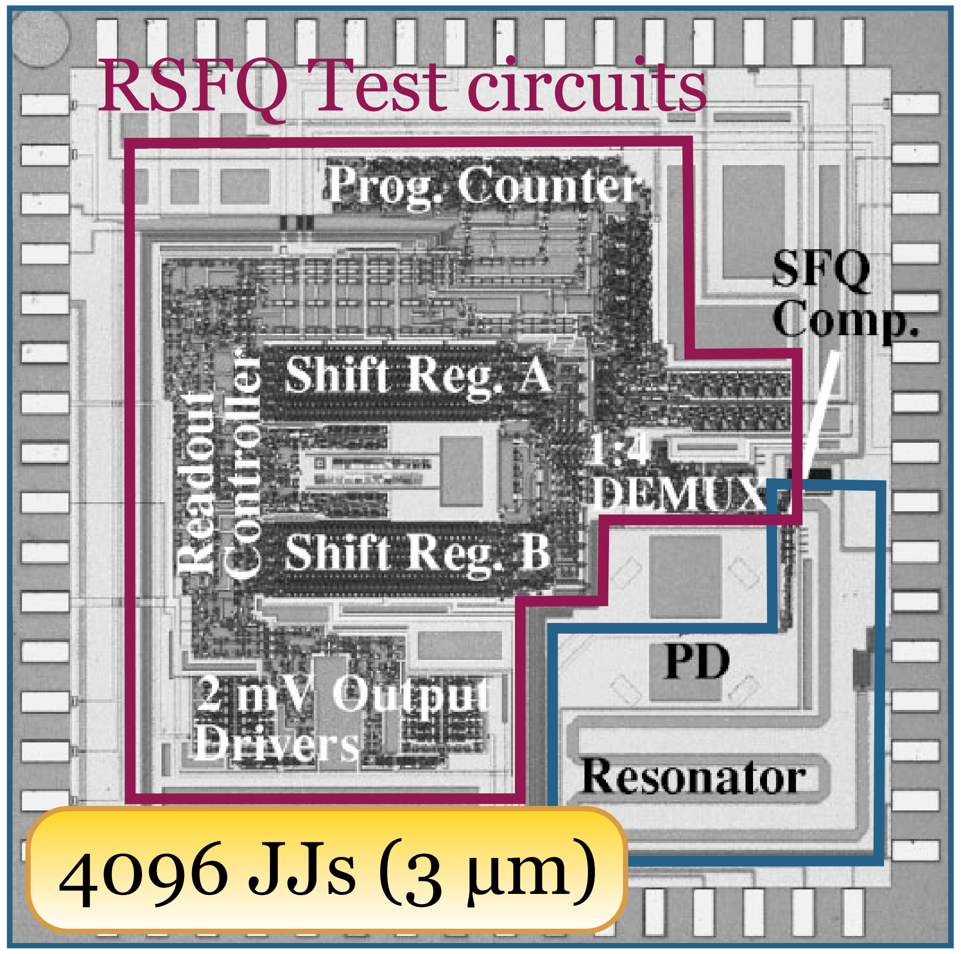
✳Fs/Fc=8 [~15000 JJs]
- coefficients: 0,±1,±1/$\sqrt{2}$
- 4 Low-Pass DFs

Méthodes de test possibles

✓ Segmented correlation [thèse J. Bulzachelli 2002 MIT]

Data (256 bits) read at 1.56 GHz





Méthodes de test possibles

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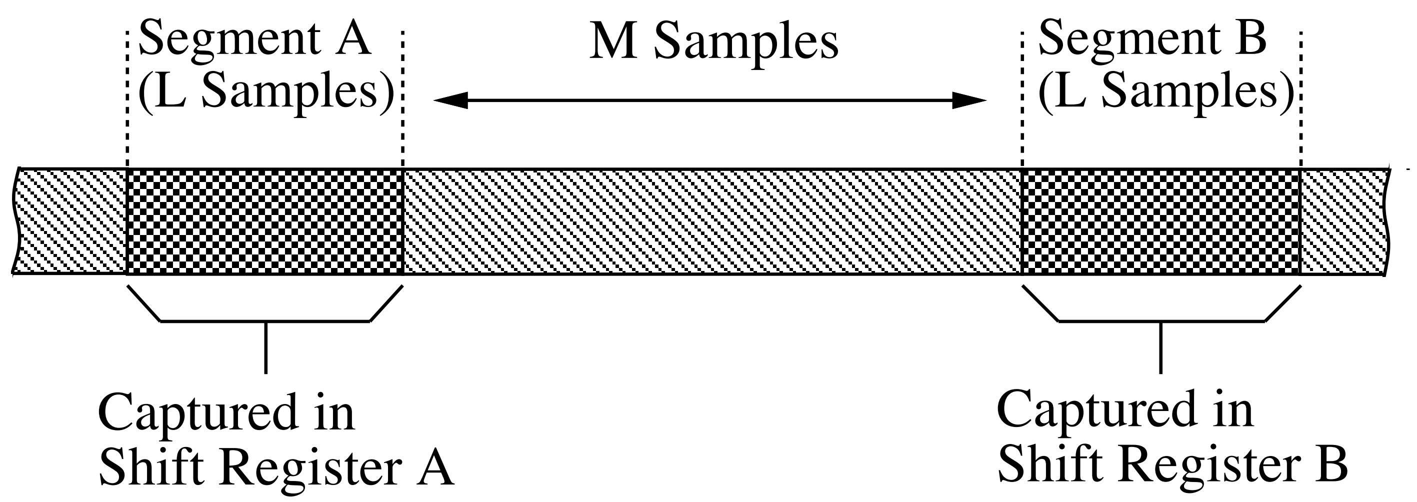
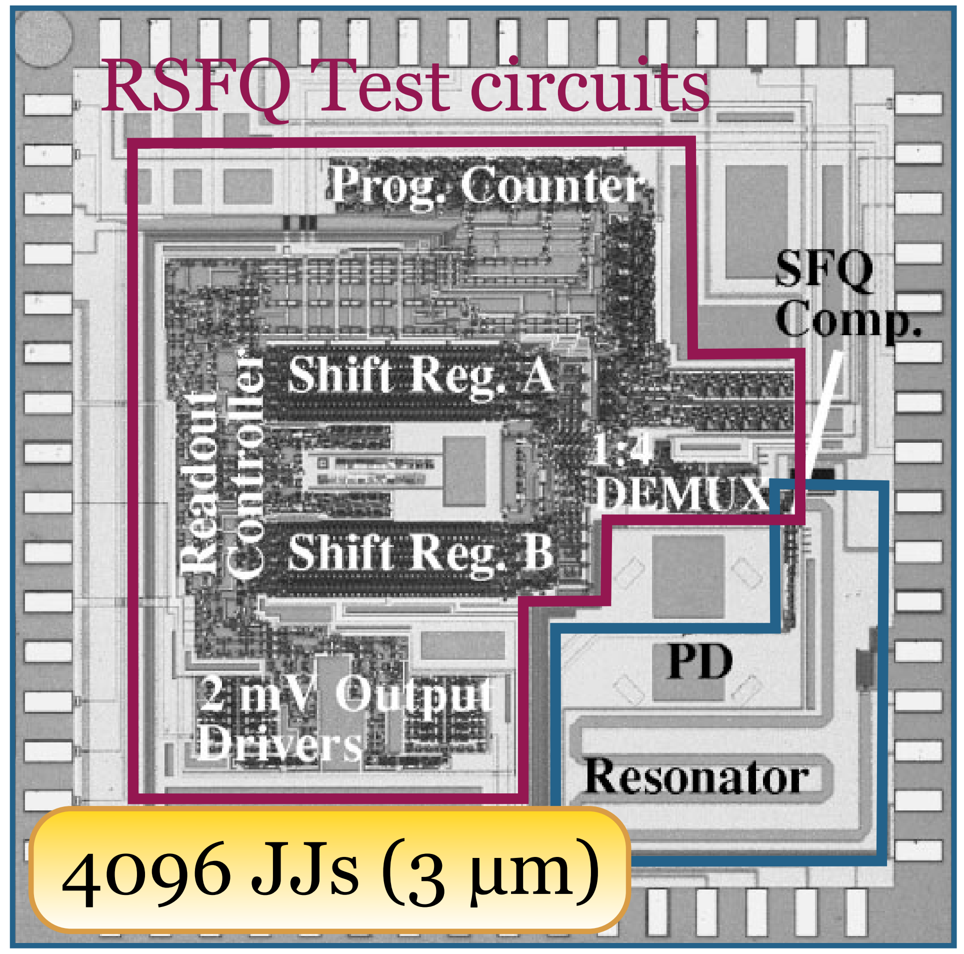
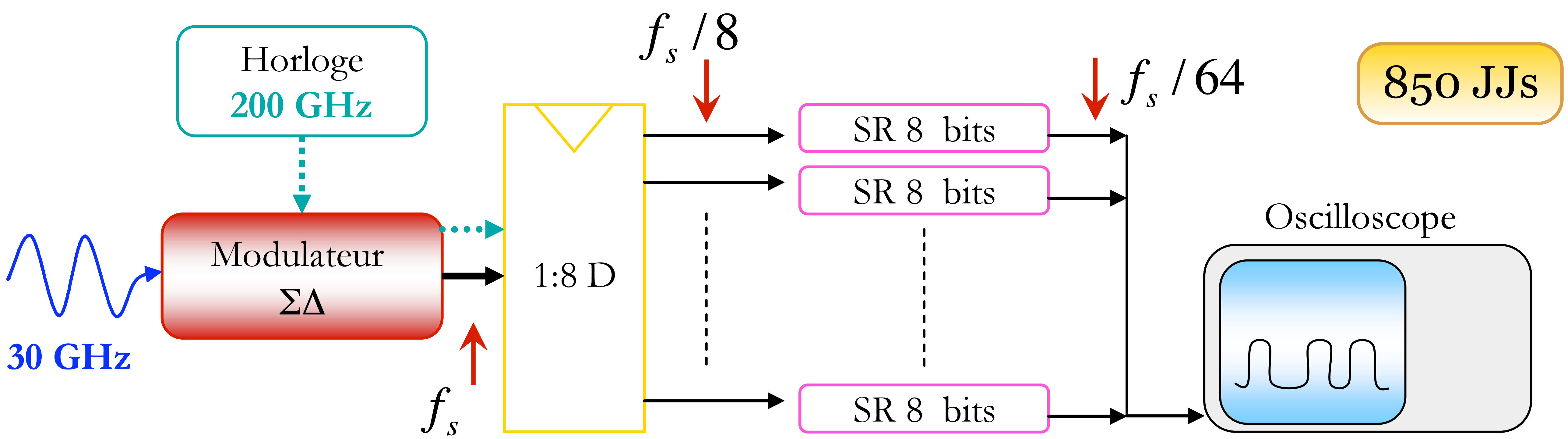




✓ Proposed Solution: Shift Registers and Demultiplexers

Data (64 bits) read at 3.12 GHz **RSFQ Memory on Chip**



Synthèse sur la conception

Compromis sur la fréquence d'échantillonnage → Eliminer le *plateau*, réduire la *zone grise* du comparateur et OSR en puissance de 2

Améliorer le couplage du filtre au comparateur et l'adaptation entre le signal en entrée et le comparateur → Augmenter le SNR

Fs/Fc=4 or Fs/Fc=8 → Une implémentation du filtre de décimation plus facile

ADC

Fs=120 GHz → Décimation 1:128 → 936 MHz Nyquist output

Fs=120 GHz → Fc=Fs/4=30 GHz → OSR= 128 → SNR= 125 dB

$R_N I_C = 1\text{mV}$

B=468 MHz

[Jonctions count: 8000]

Modulator test circuits

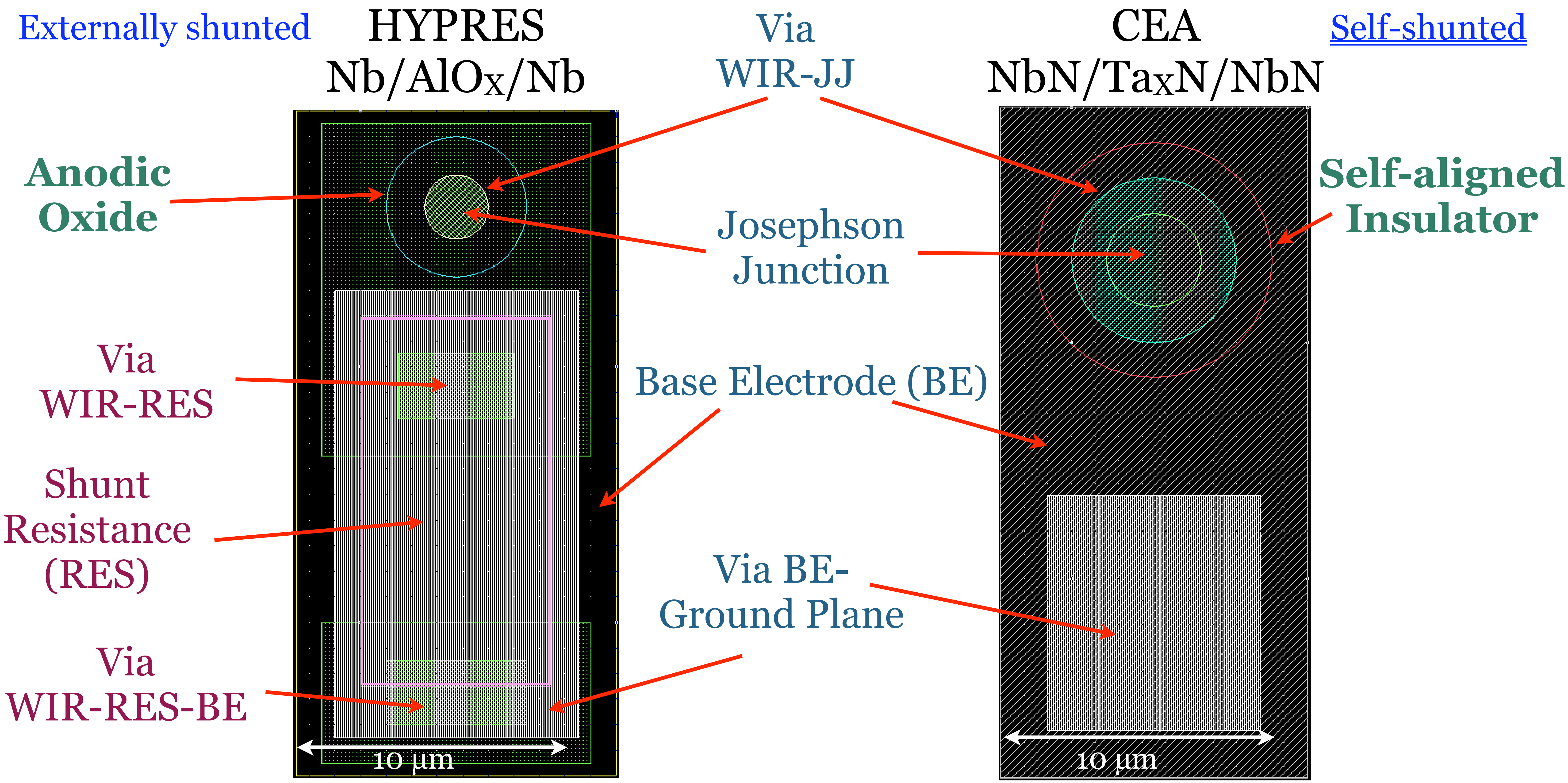
Segmented correlation → FFT (256 bits) → 1 GHz Readout **[4000 JJs]**

Simple Acquisition → FFT (64 bits) → 2 GHz Readout **[1000 JJs]**

Plan de l'exposé

- Introduction
- Rappels sur le CAN et l'Electronique supraconductrice
- Etude de la structure du CAN en NbN
- **Implémentation et comparaison de la technologie NbN et Nb**
- Conclusions et perspectives

Dessin des circuits RSFQ



Jc=4.5 kA/cm²

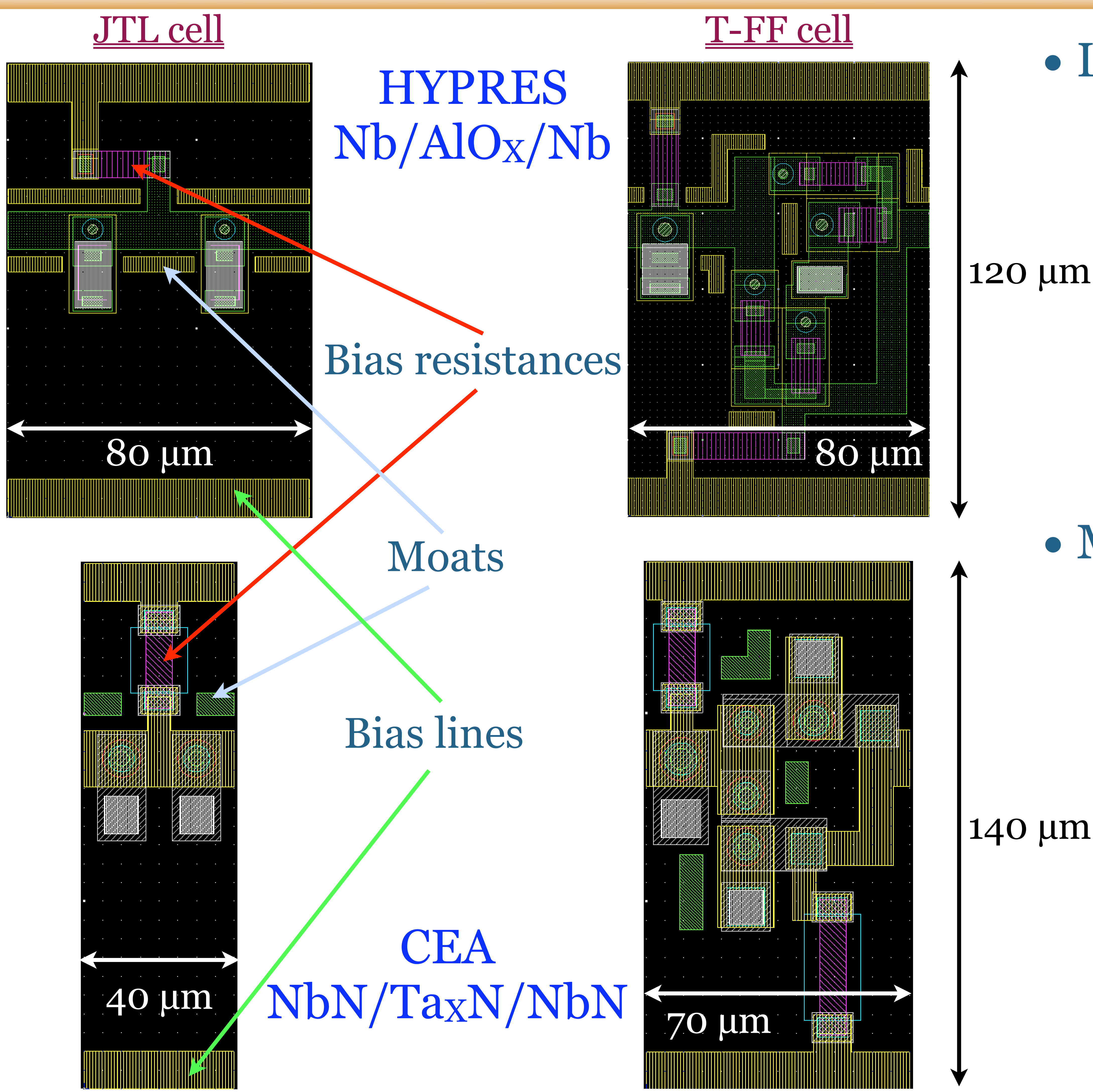
Jc=5 kA/cm²

d=1.5 µm
A=0.5 µm

$$\frac{I_C[JJ_X(\mathrm{NbN})]}{I_C[JJ_X(\mathrm{Nb})]} \sim \frac{9\mathrm{K}}{4.2\mathrm{K}}$$

d=2.5 µm
A=1.5 µm

Dessin des circuits RSFQ



- Lines considerations:

$$L_{\square}(\mathrm{Nb}) = 0.7\mathrm{pH}$$

$$L_{\square}(\mathrm{NbN}) = 1.45\mathrm{pH}$$

NbN lines are 2 times shorter

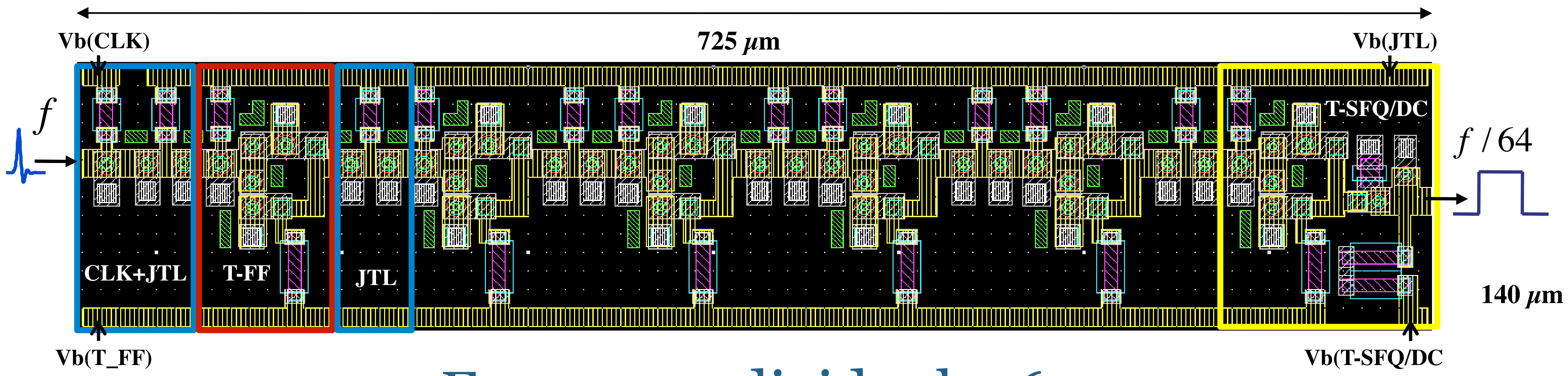
- Margins calculations:

	Nb(4.2 K) ~80 GHz	NbN (9 K) ~200 GHz
JTL	72.1%	48.5%
T-FF	25.7%	21.8%

Optimization requires a better lithography

Le diviseur de fréquence

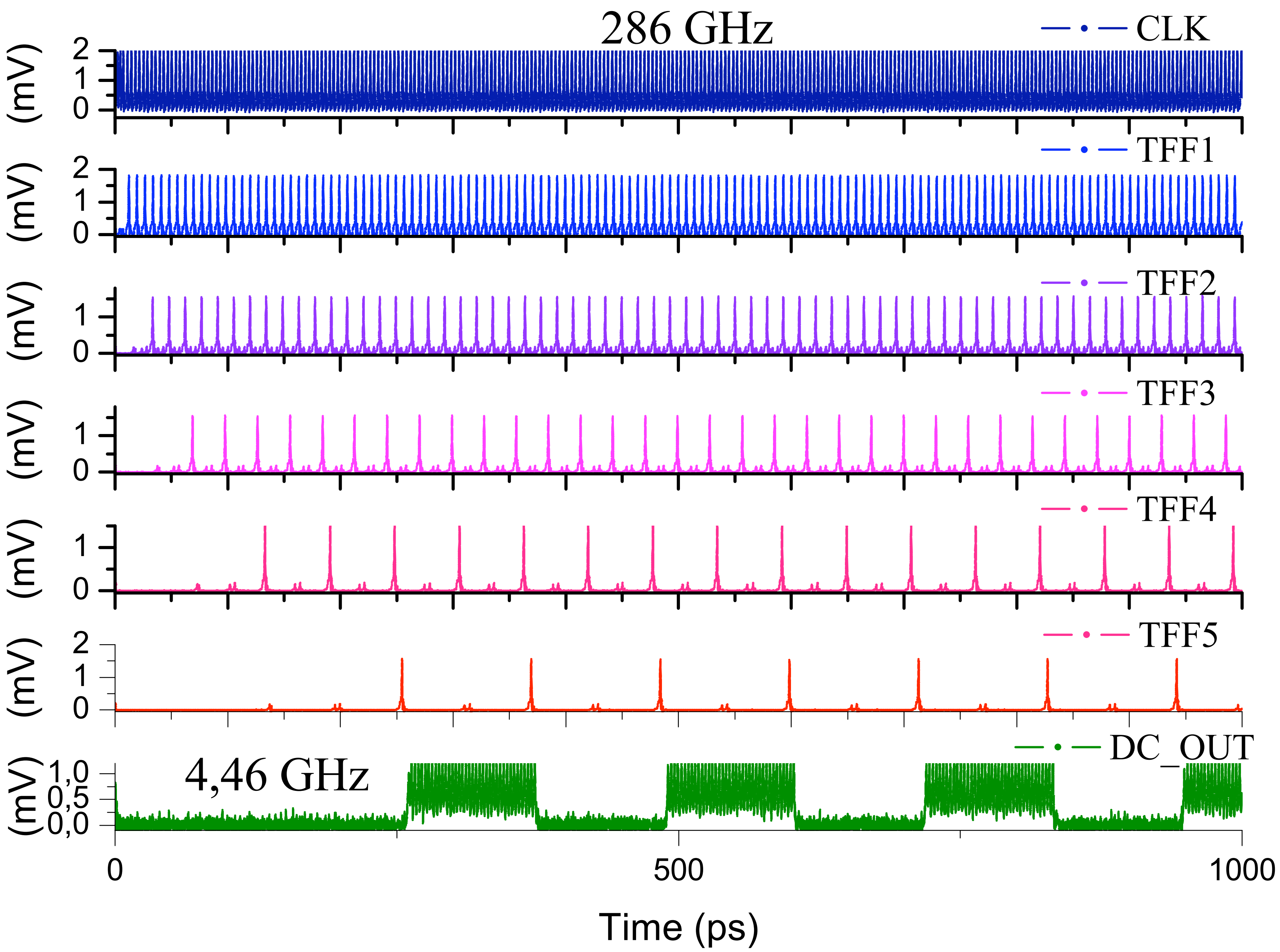
Technology performance benchmark



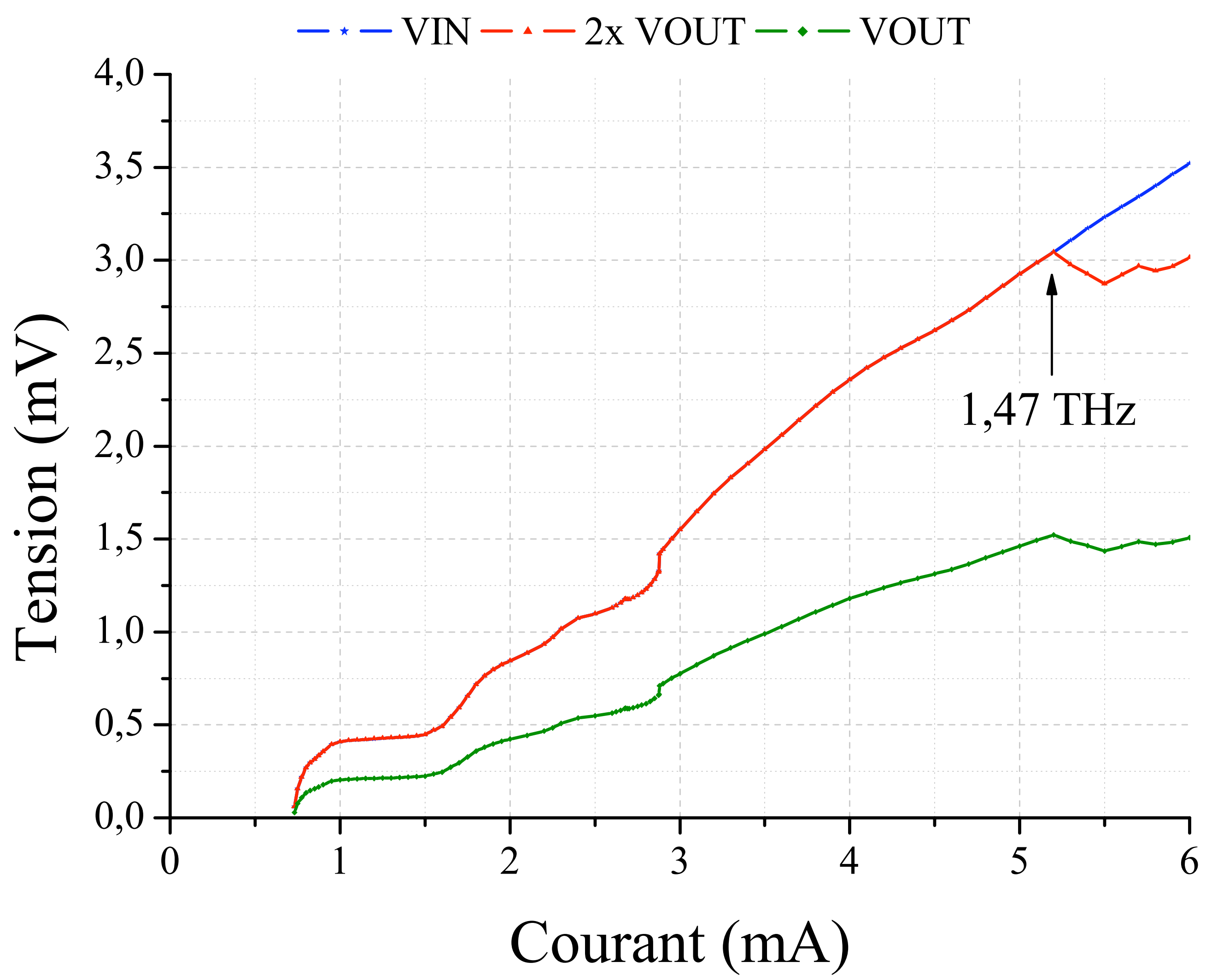
Frequency divider by 64

Clock frequency

NbN/Ta$_x$N/NbN	Nb/AlO$_x$/Nb
286 GHz	98 GHz

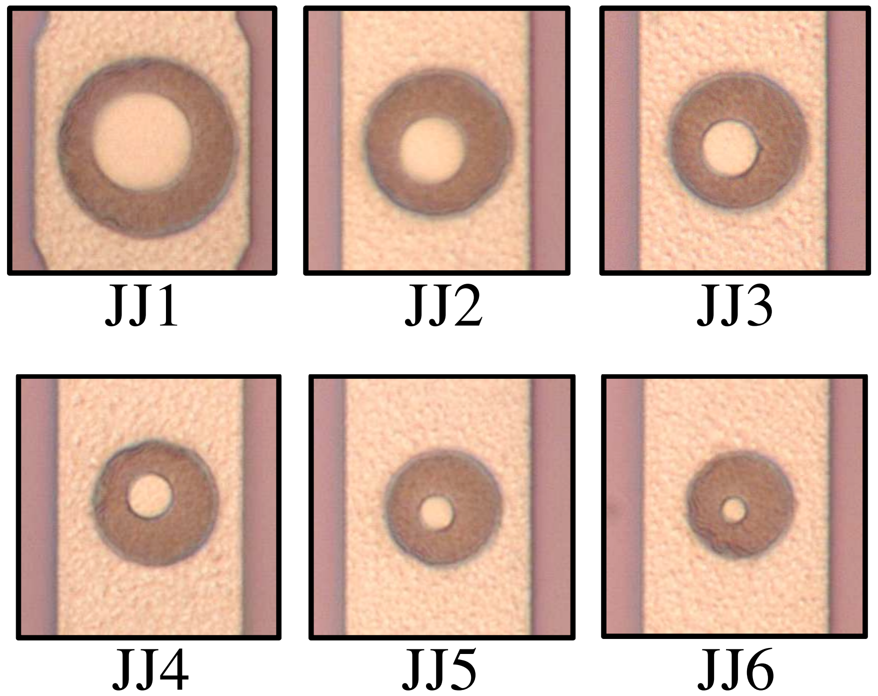


Simulated I(V) characteristic
for a single T-FF



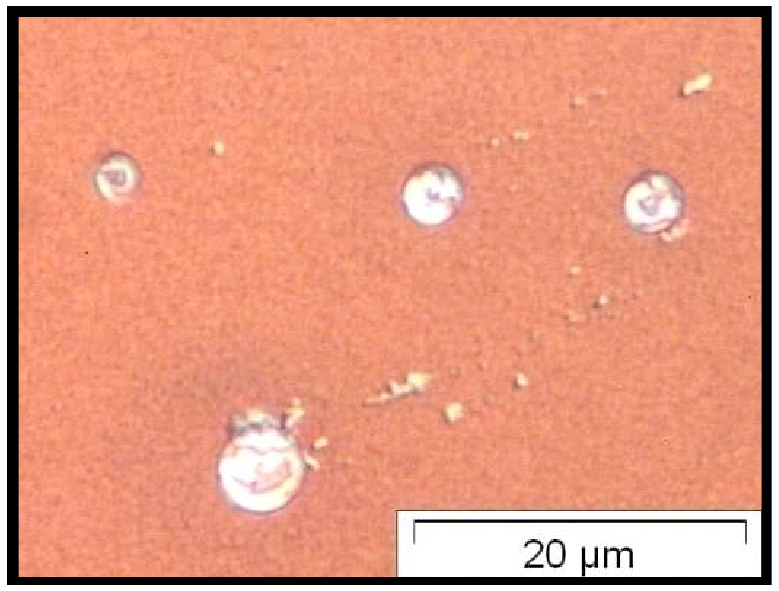
Fabrication des circuits

Ungrounded junctions library

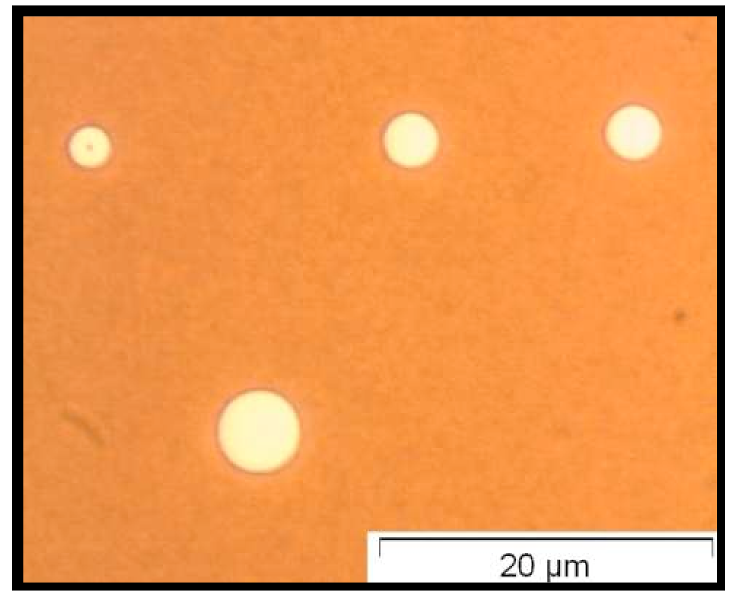


✓Critical problem after the self-insulator deposition

Difficulty to put out the photo-resist covering the JJ

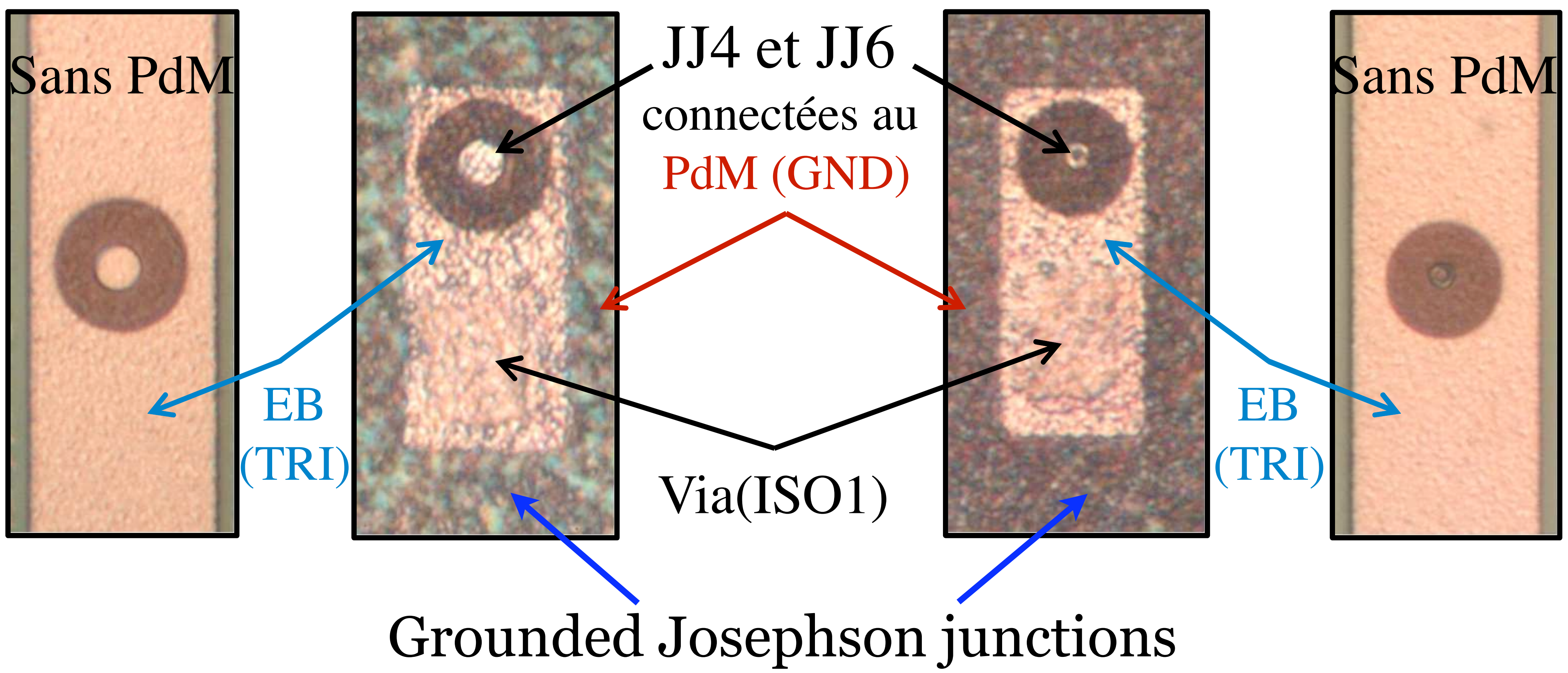


After Lift-off



After Lift-off
+wiping+RIE O_2

✓Ground plane effect



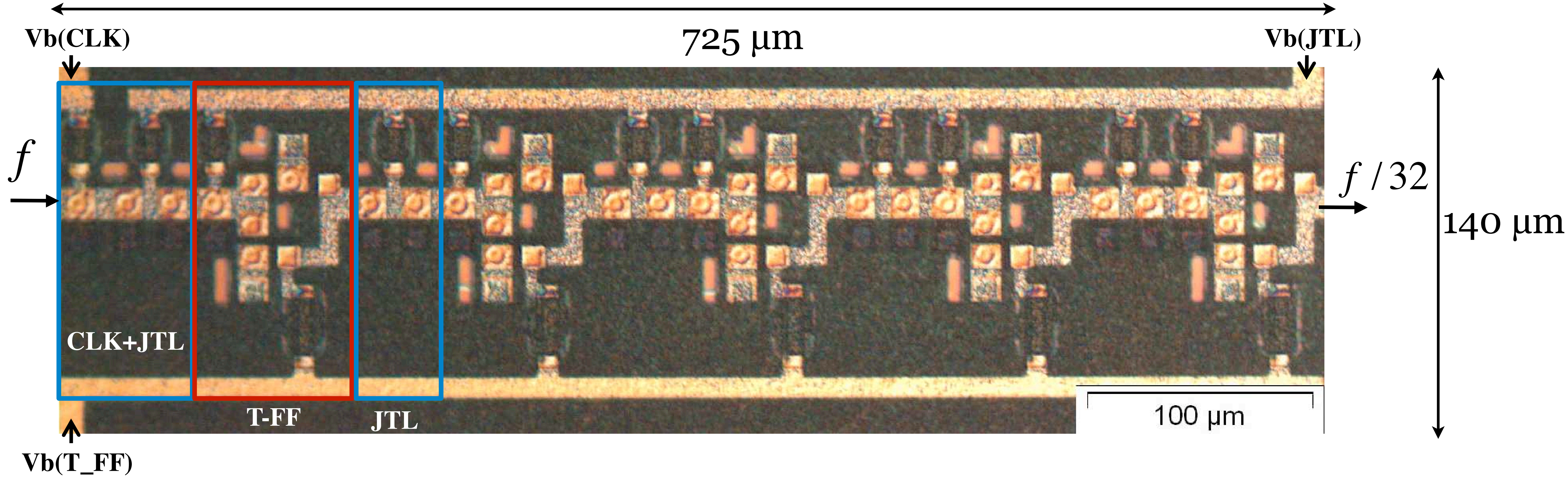
Some JJs of 2.5 µm of diameter are covered

The NbN (400 nm) ground plane increases the rugosity of the junctions

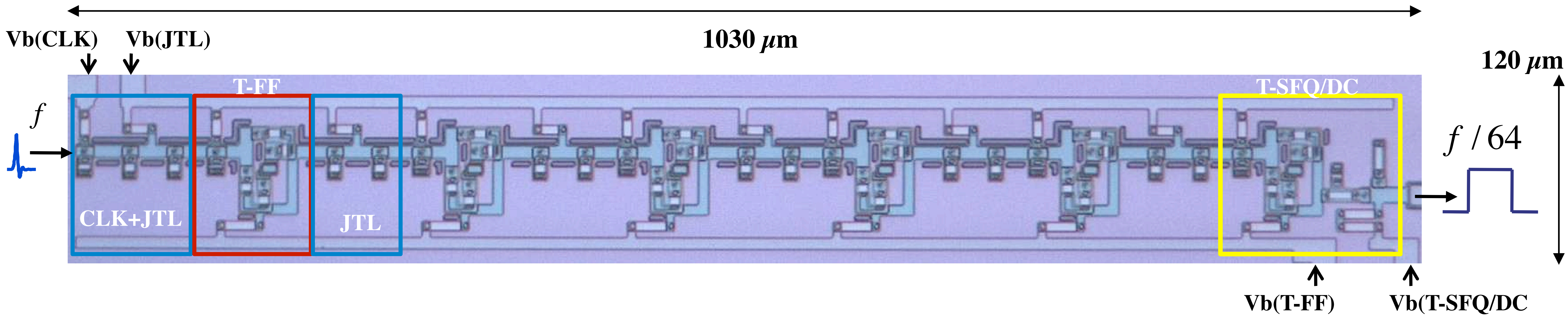
Diviseur de fréquence sur puce

CEA (NbN/Ta_XN/NbN)

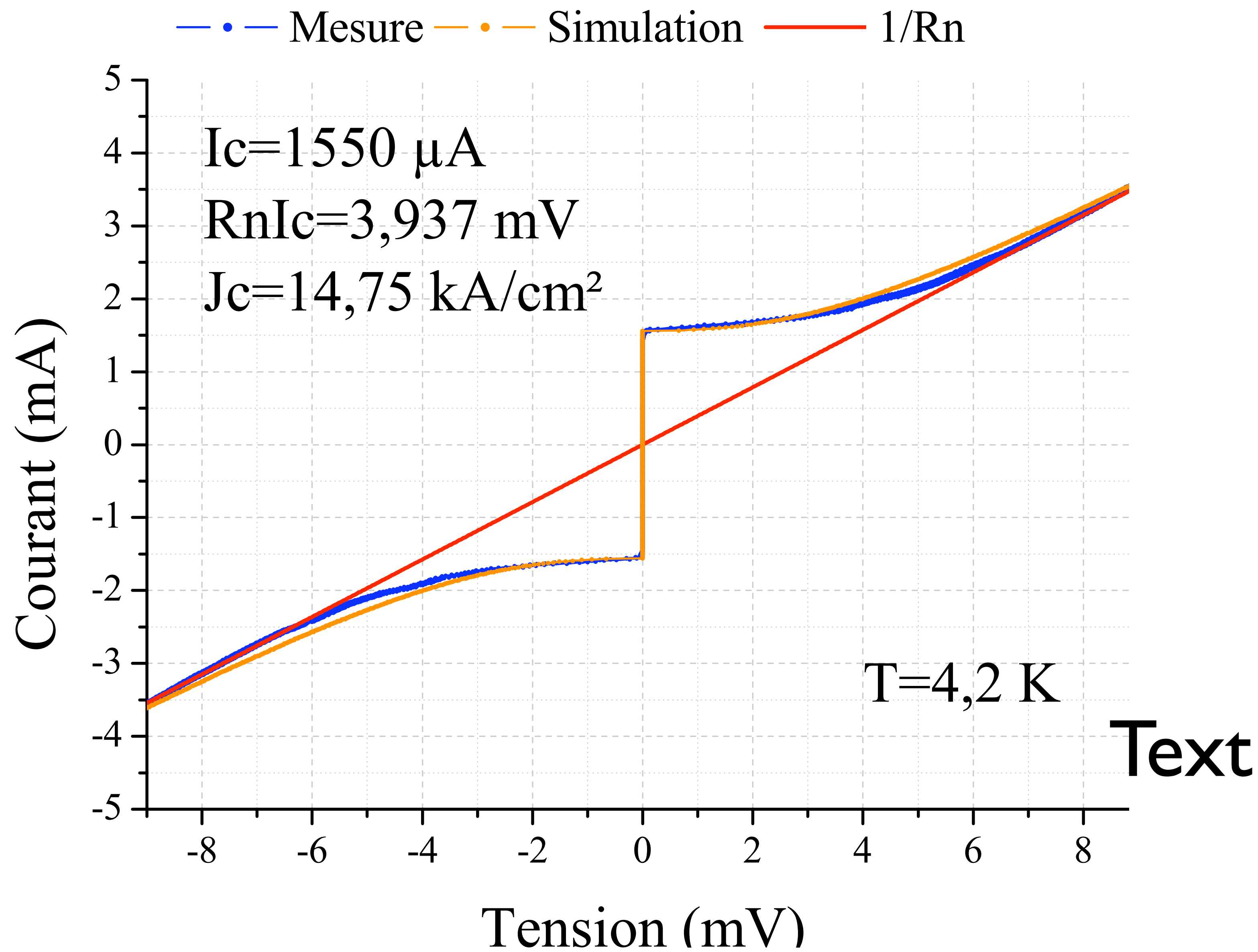
Area 18 % smaller

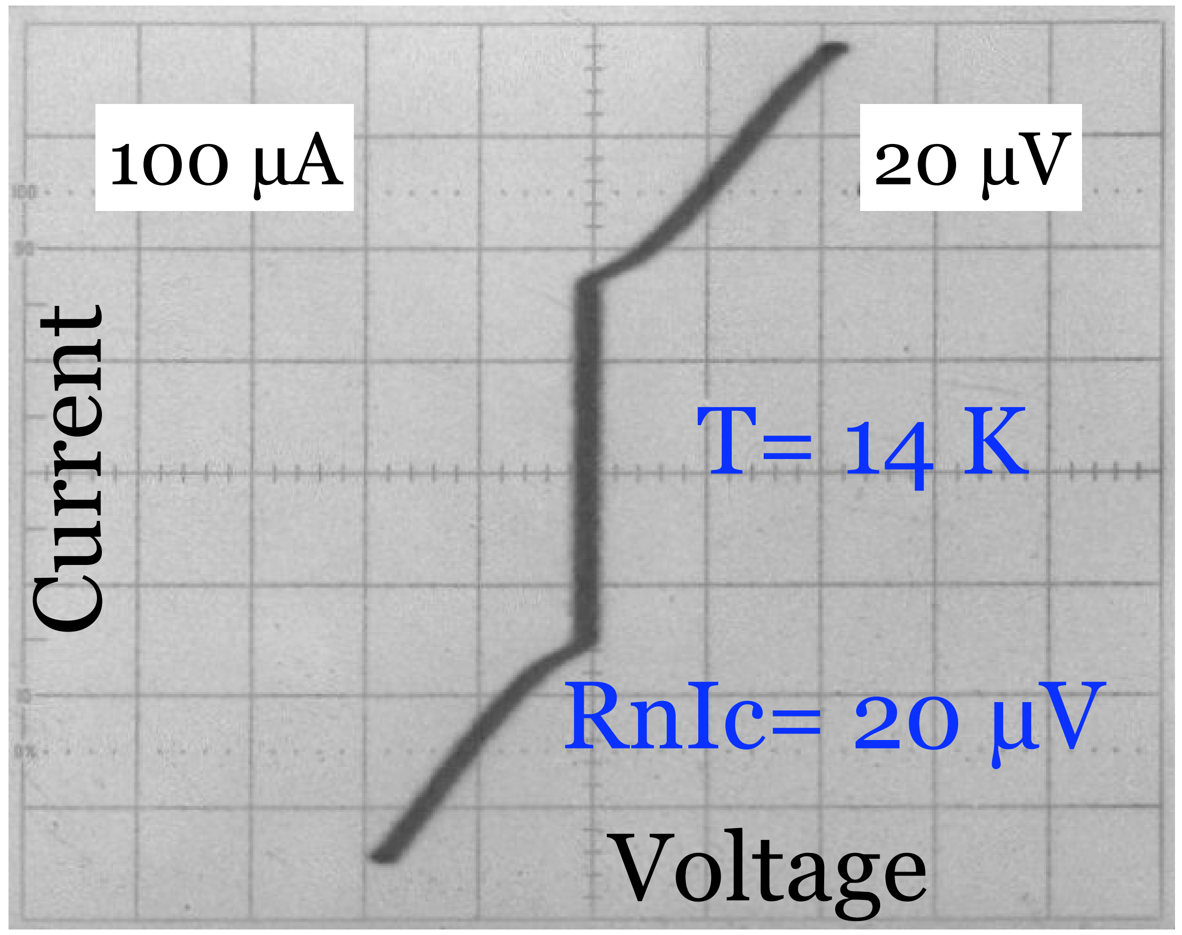


HYPRES(Nb/AlO_X/Nb)

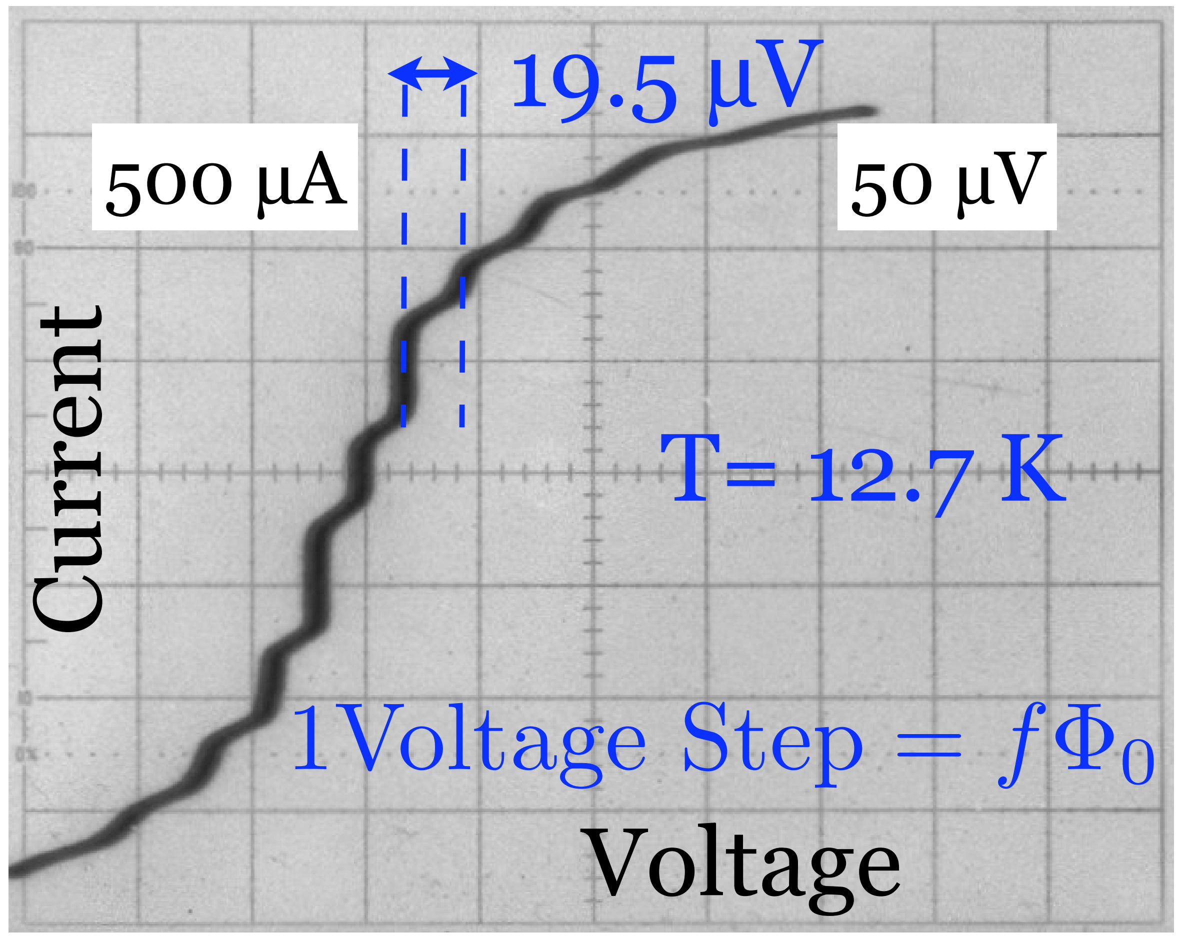


Test des JJs NbN/TaxN/NbN





- ✓High RnIc from 4.2 K up to 9 K
- ✓High Jc up to 14.7 kA/cm2 at 4.2 K



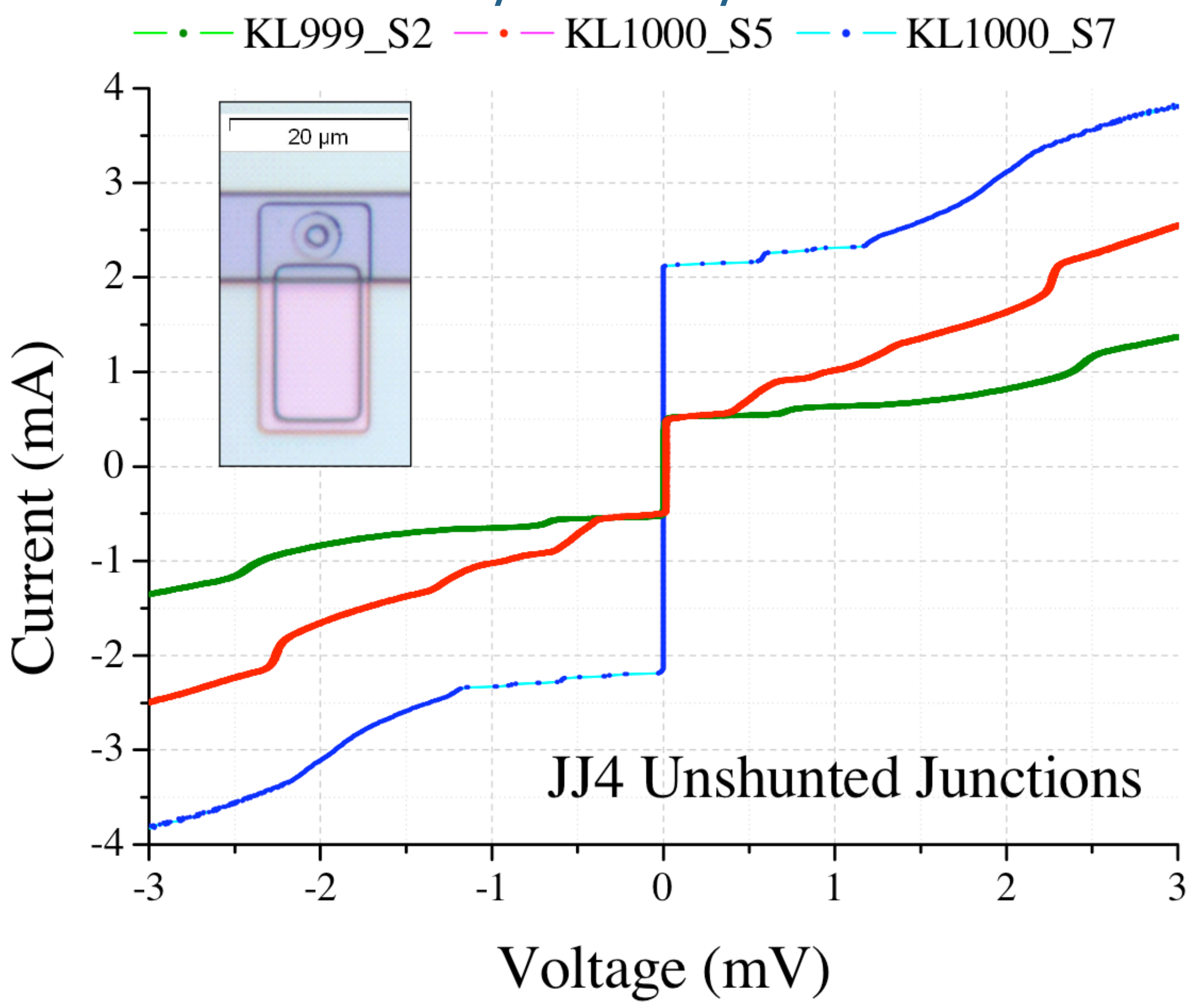
Shapiro steps at 9.4 GHz

The junctions are over-damped

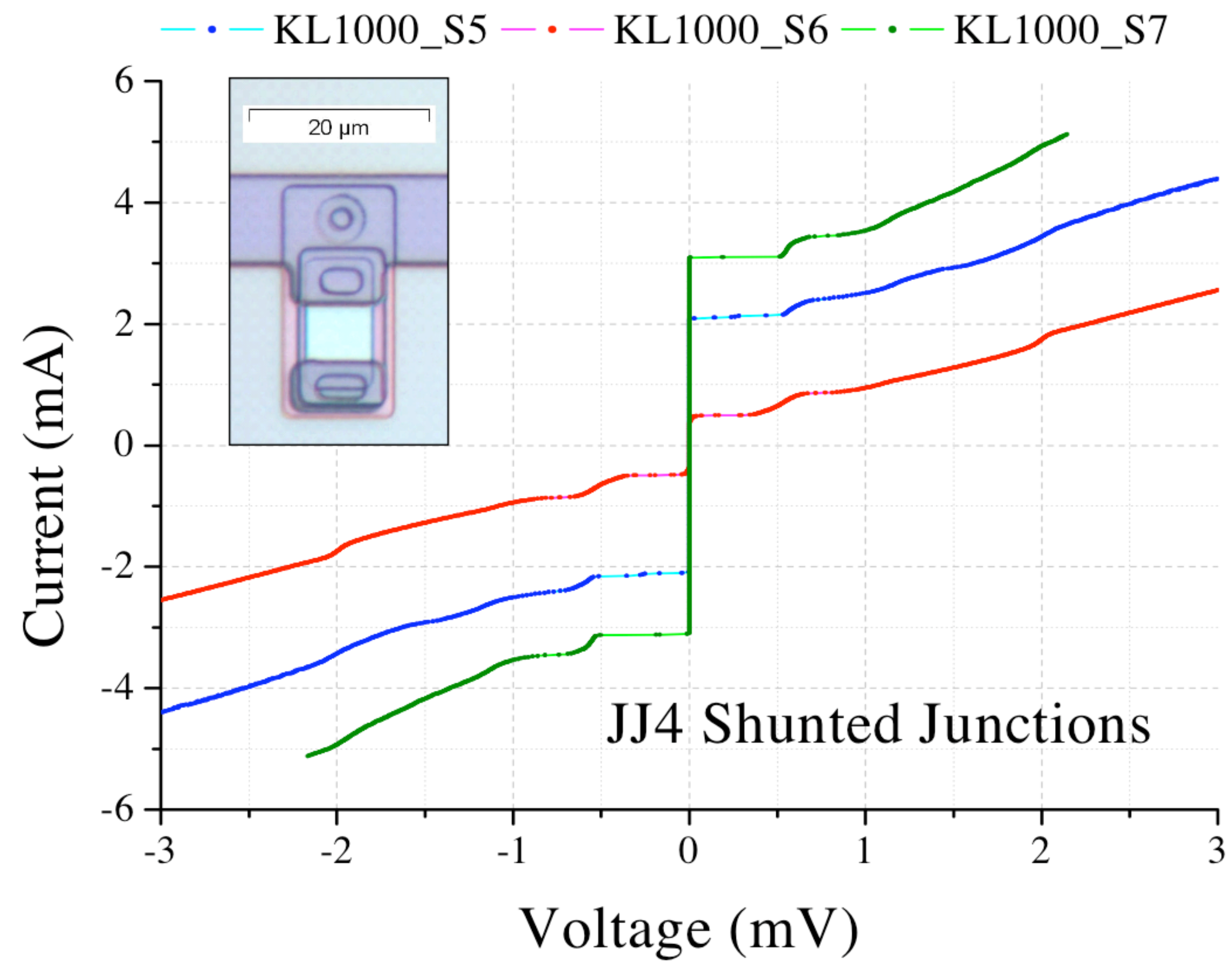
$\beta_c(4.2K) \sim 0.7 \rightarrow \underline{\beta_c(9K) \sim 0.4} \rightarrow \beta_c(14K) \sim 0.05$

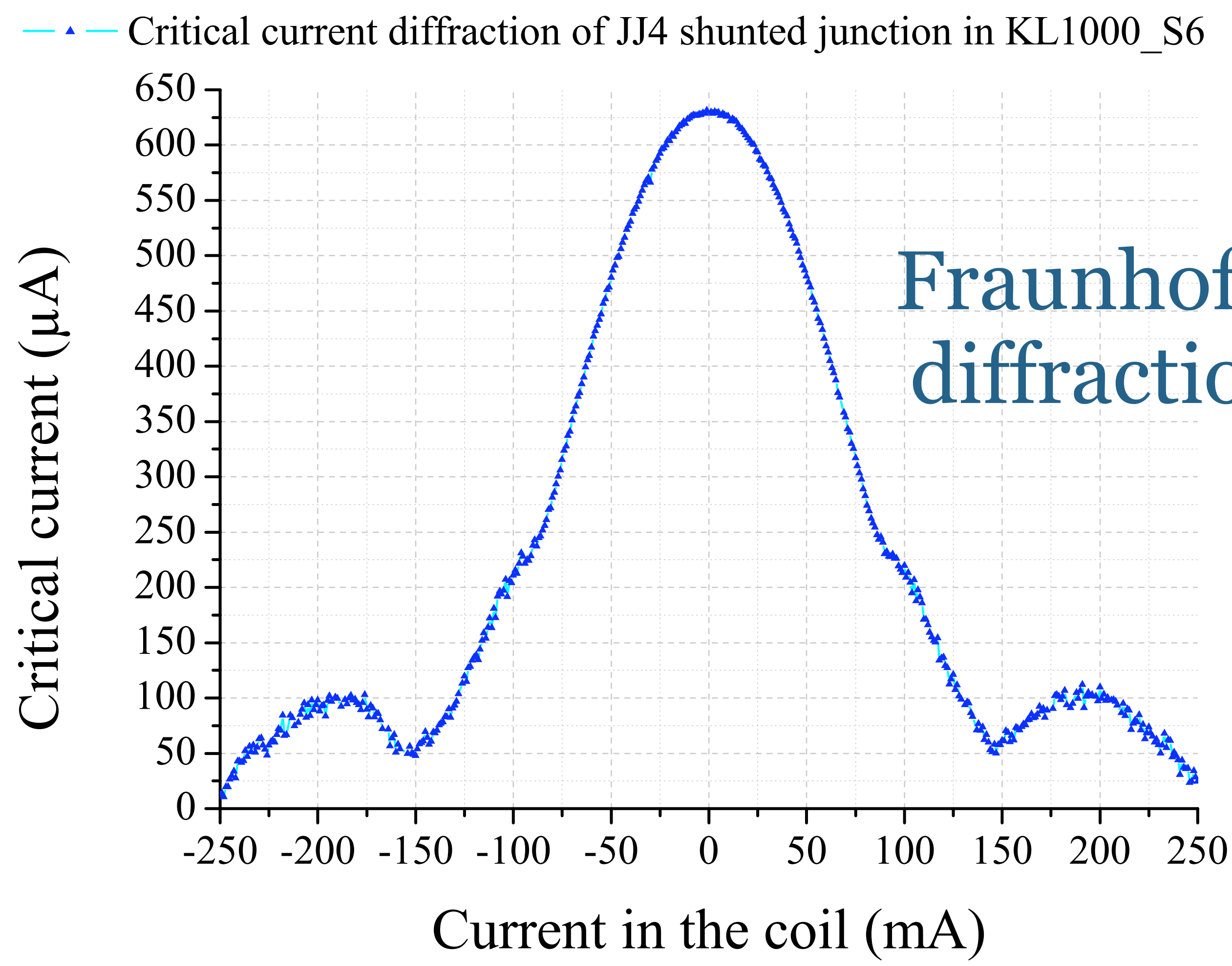
Test des JJs Nb/AlOx/Nb

Nb/AlOx/Nb



Nb/AlOx/Nb externally shunted





Fraunhofer diffraction

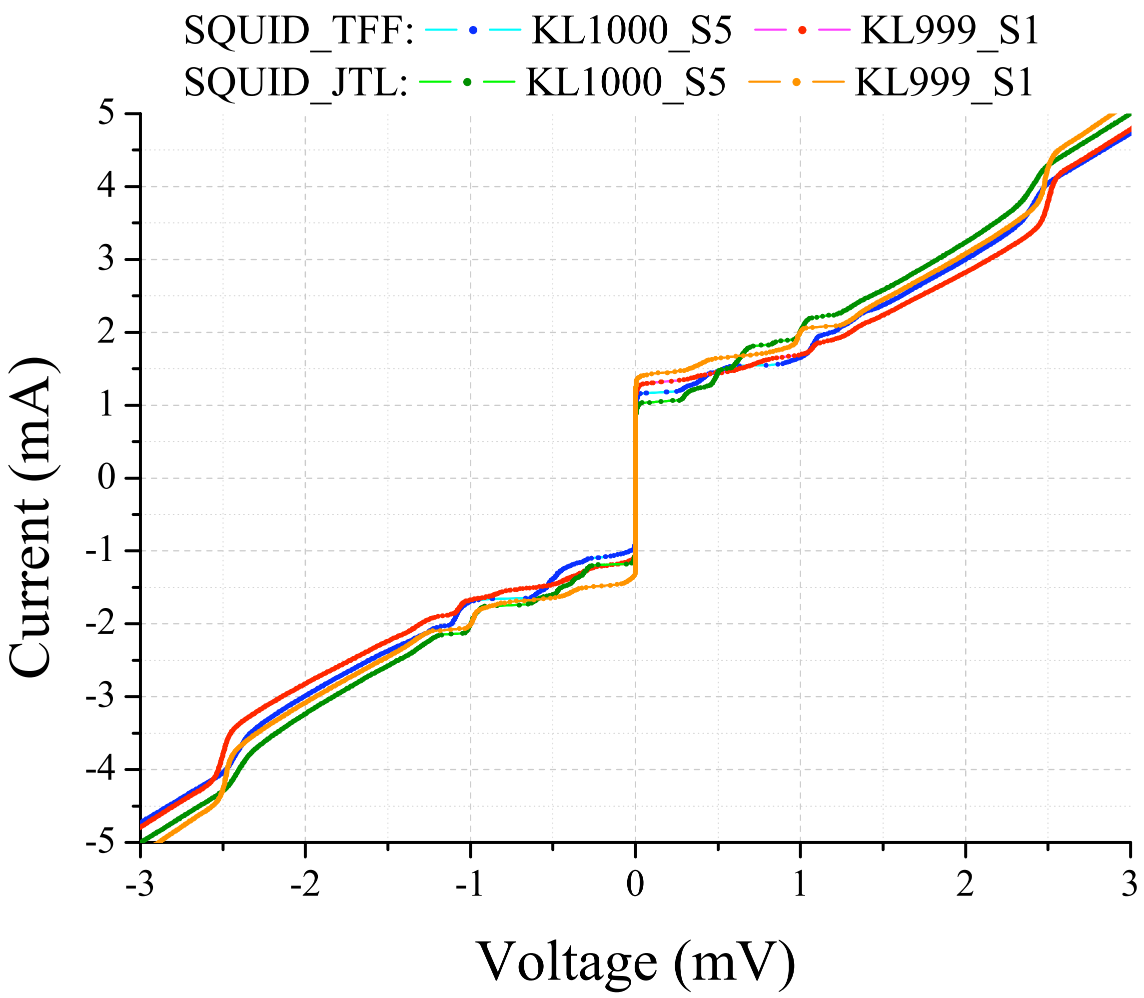
✓Any hysterisis present on the I(V) characteristics

✓Josephson effect is still present

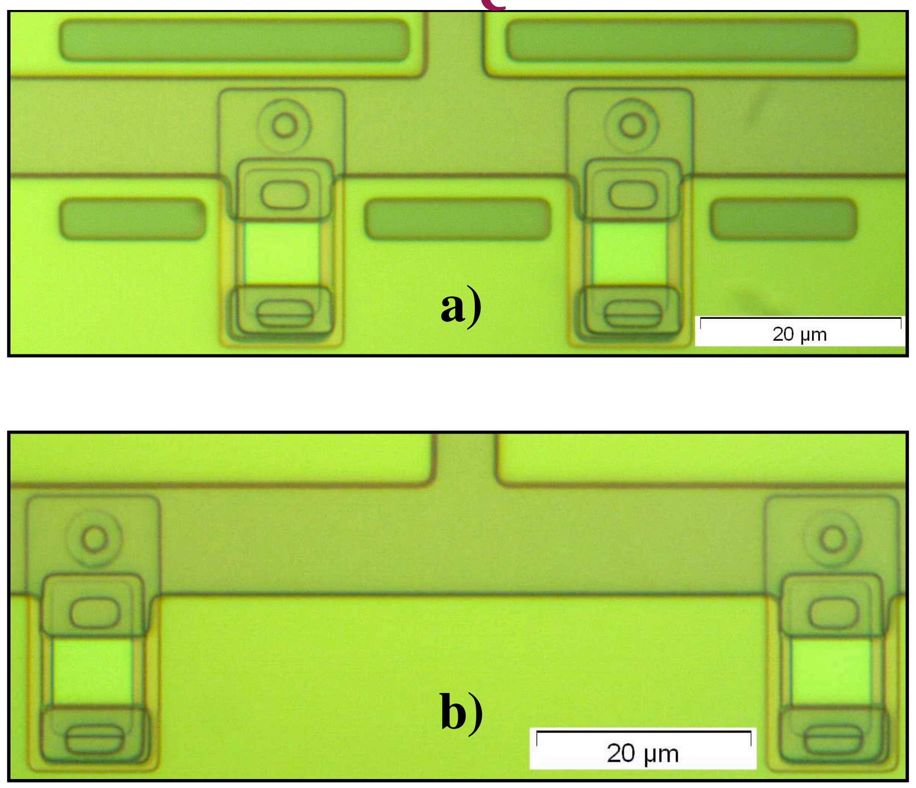
⬇

Superconducting short-circuit

Test des SQUIDs Nb/AlOx/Nb

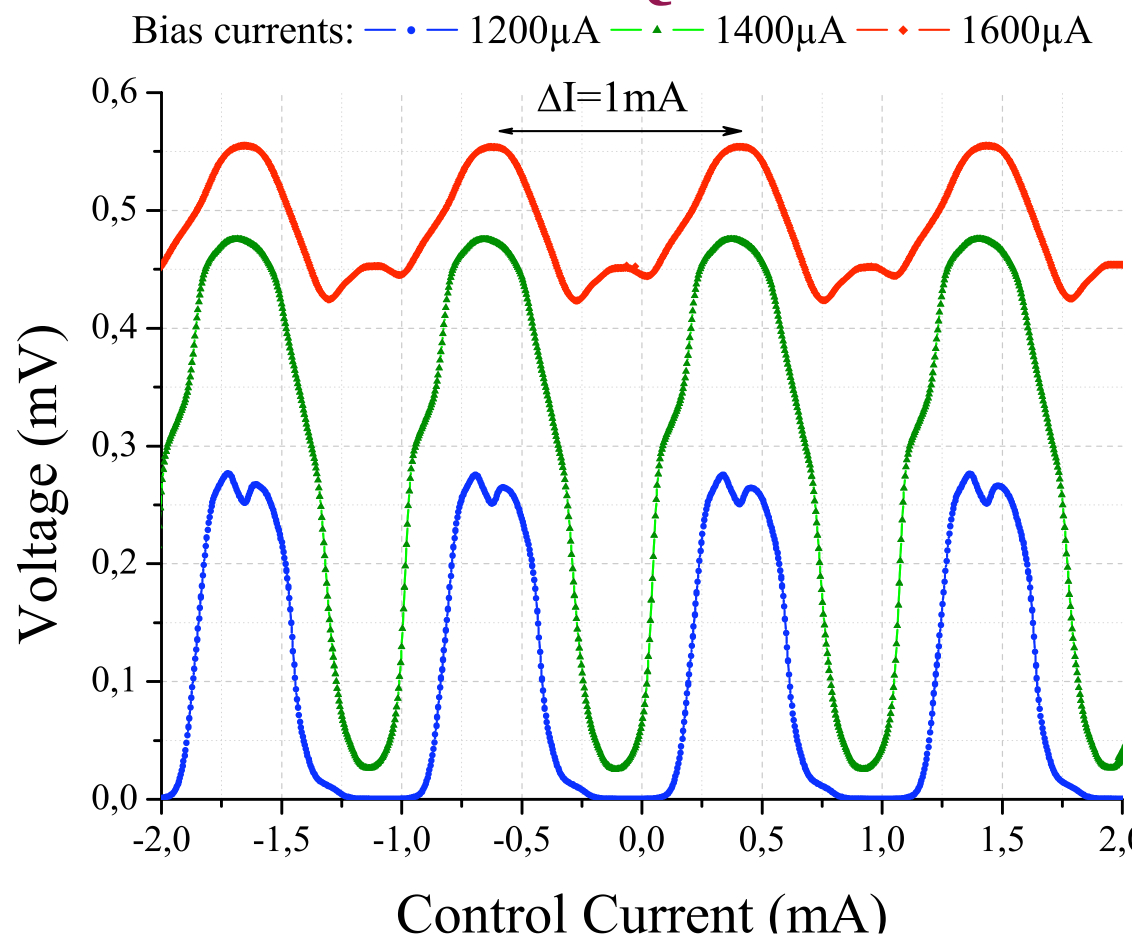


JTL SQUID



T-FF SQUID

JTL SQUID

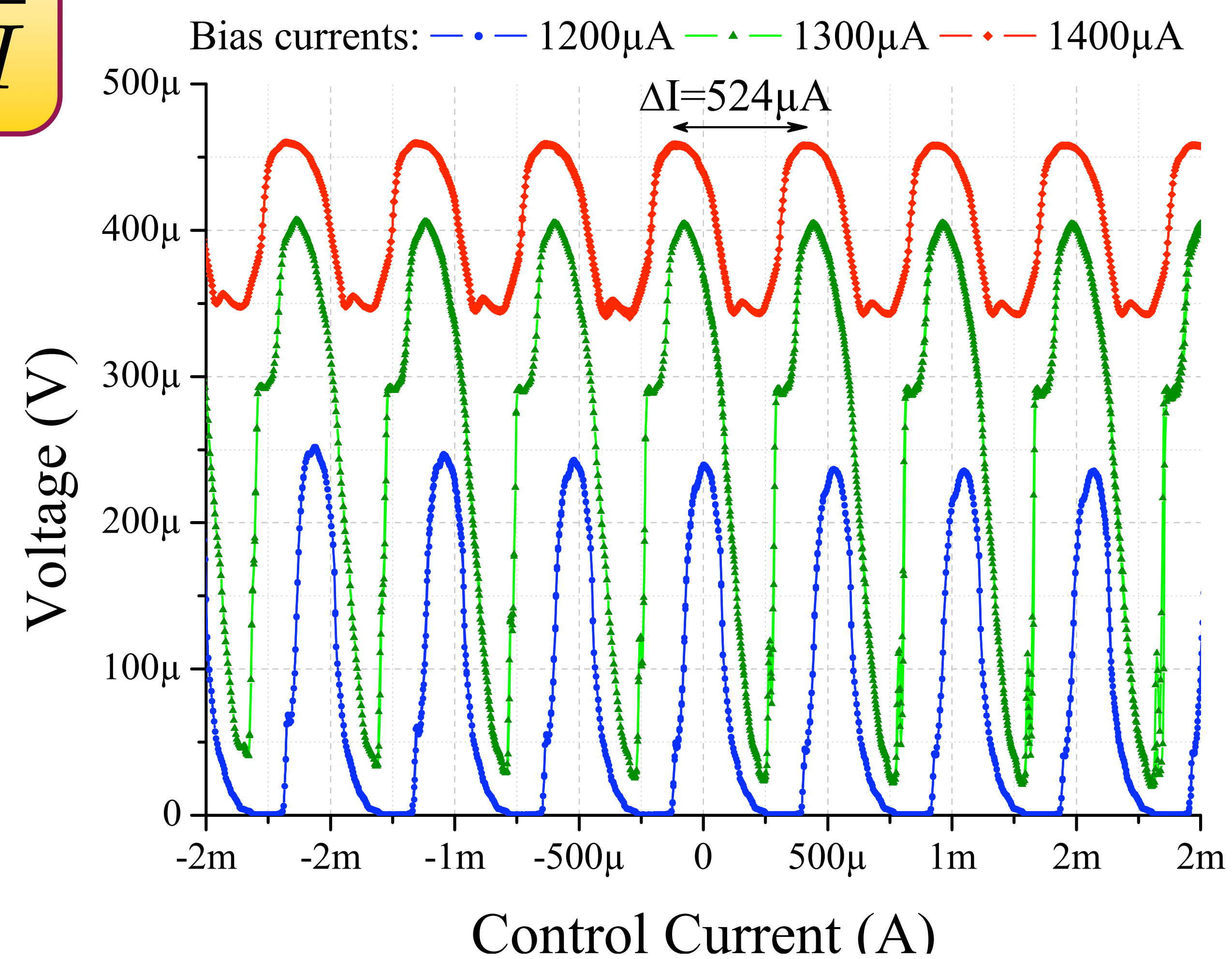


- ✓Inductance measurement from SQUID voltage interference period ΔI

$$L = \frac{\Phi_0}{\Delta I}$$

- ✓ Good agreement with the simulation from the design

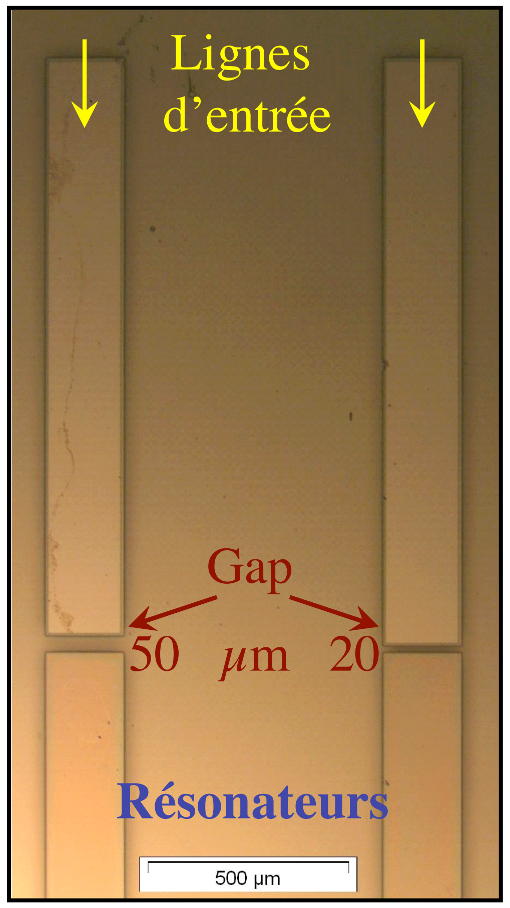
T-FF SQUID

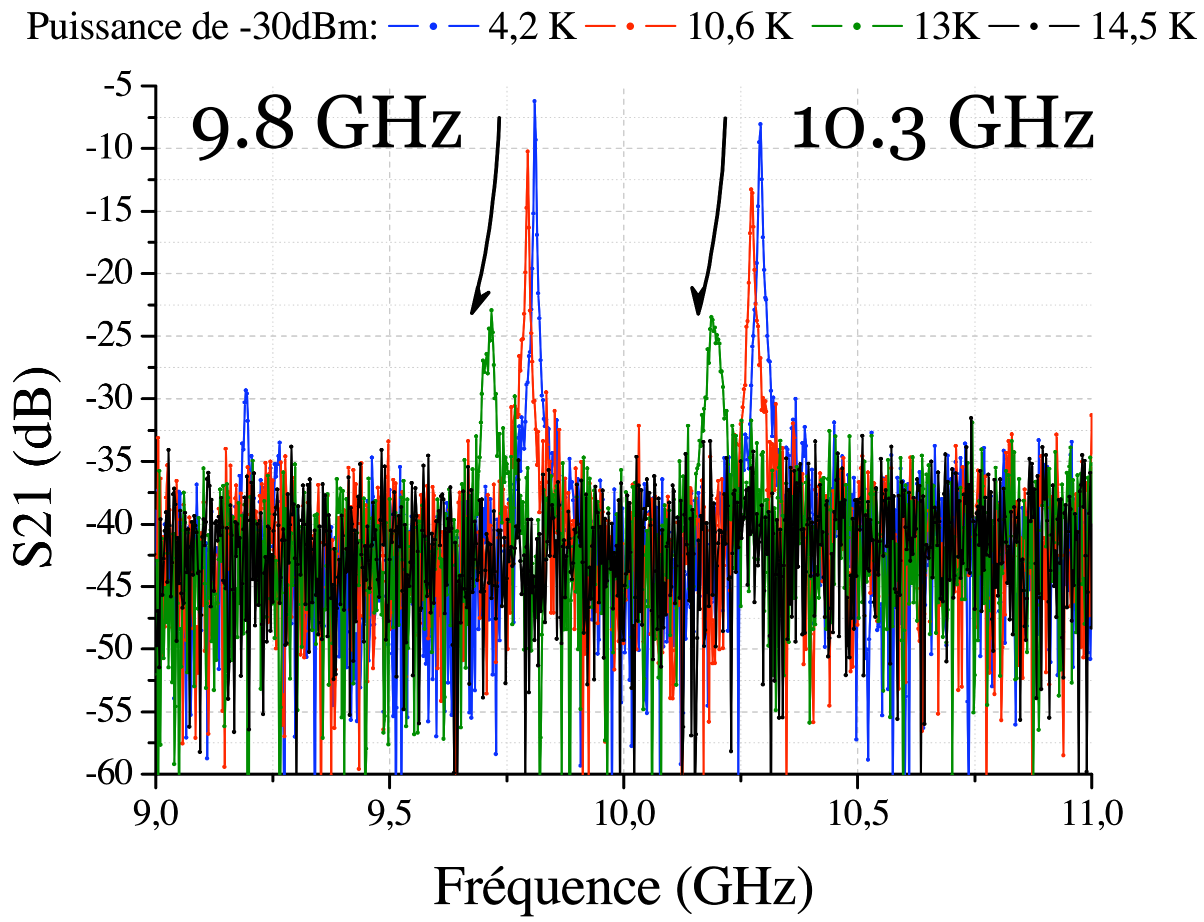


Element	$Valuer_{Cal}$	$Valeur_{Exp}$	**Ecart**
L(SQUID_JTL)	2,32 pH	2,07 pH	10,7%
L(SQUID_TFF)	4,35 pH	3,95 pH	9,1%

Variation de $\lambda_L(T)$ pour le NbN

NbN Microstrip Resonators designed for Zc=50 Ω (W=246 µm)





Resonators length = $\lambda_g/2 = 5700\mu m$ ⟶ 10.2 GHz

High Quality factor

($Q_{50\mu m} \simeq 5000$; $Q_{20\mu m} \simeq 3000$)

Coupling even over a distance of 3W

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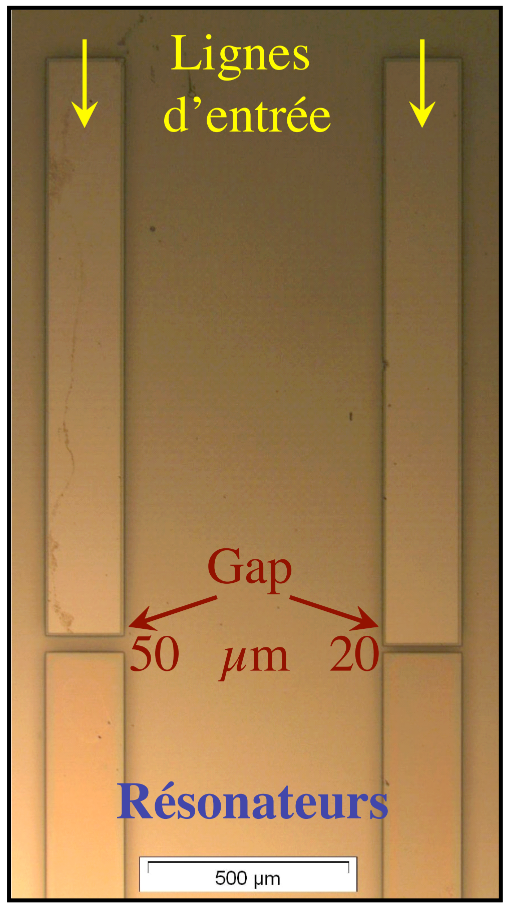
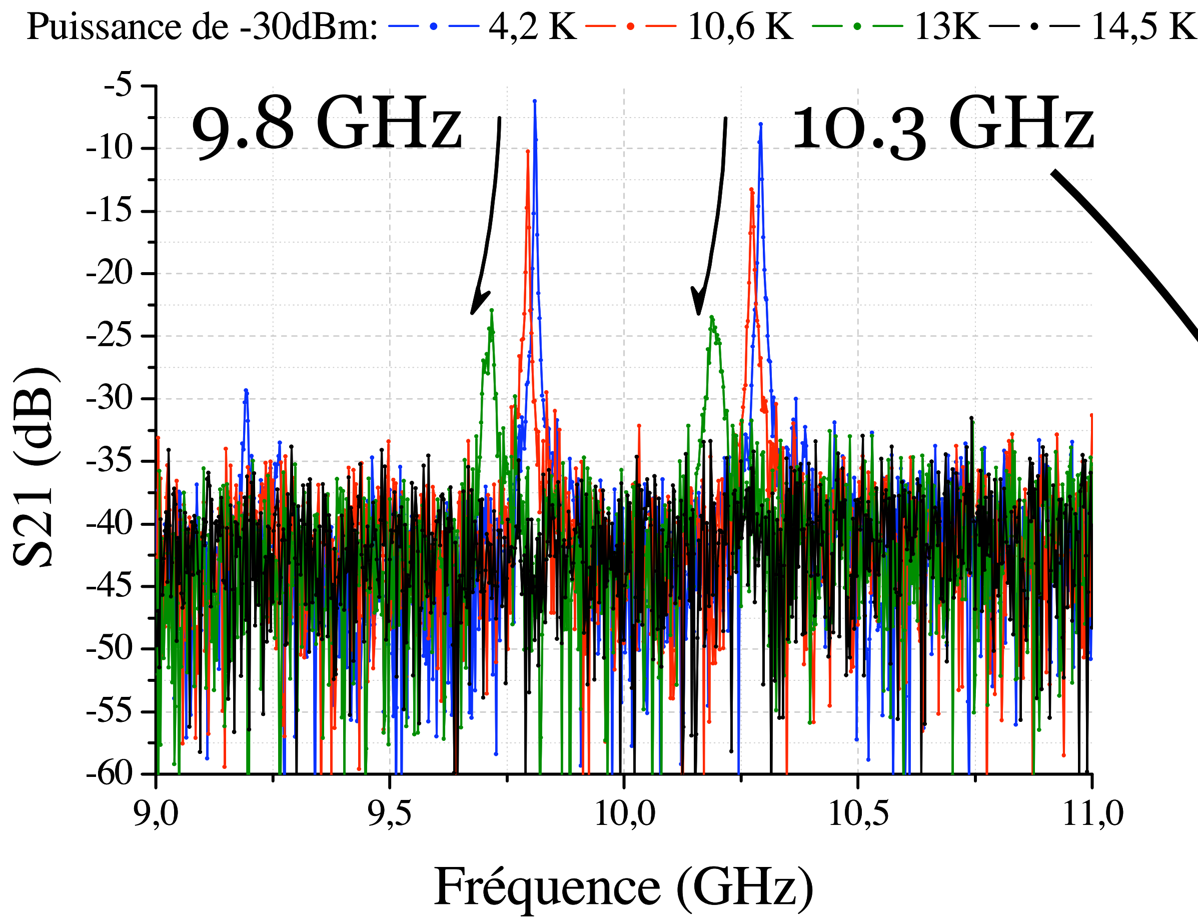
NbN Microstrip Resonators designed for Zc=50 Ω (W=246 μm)





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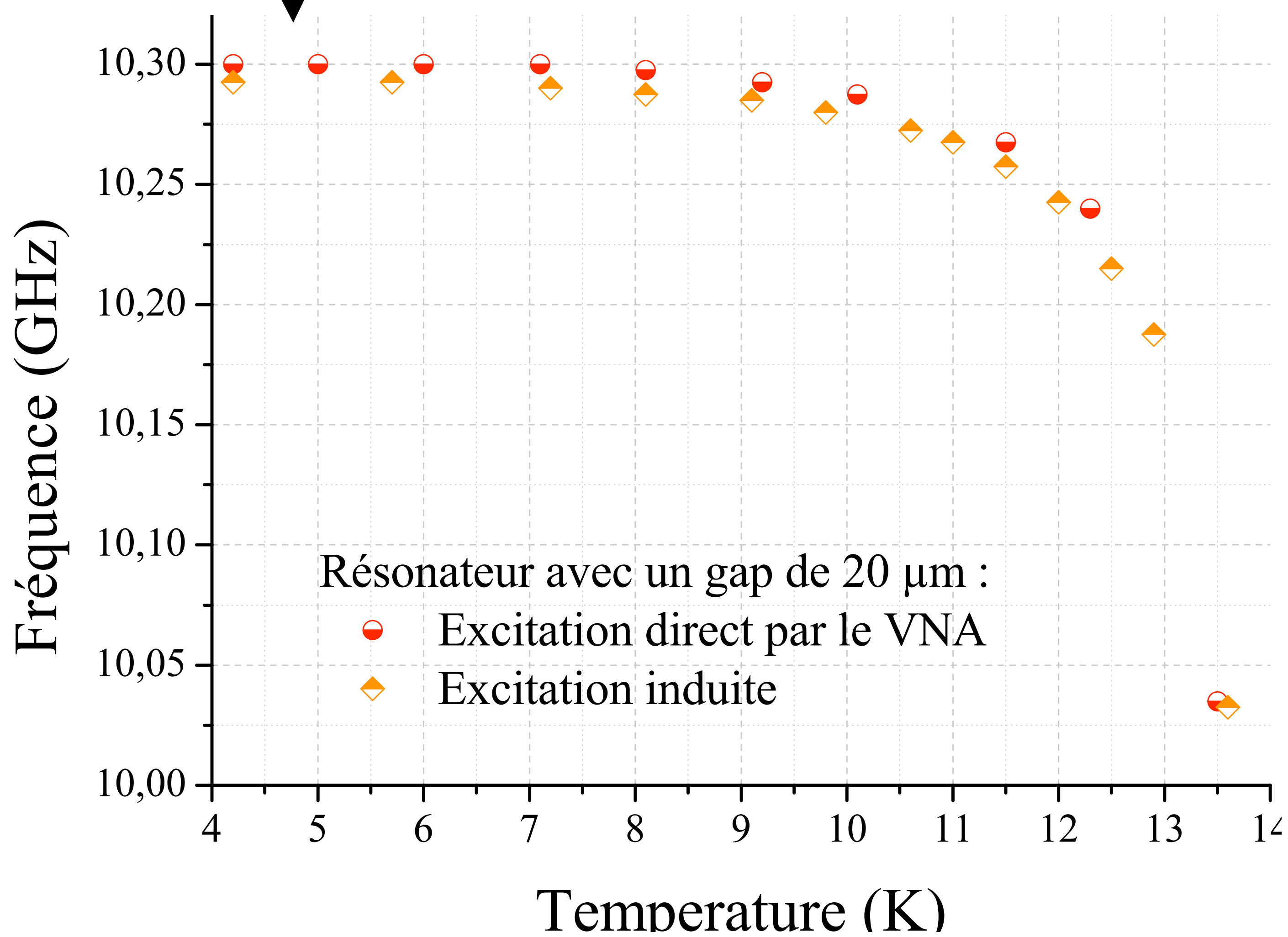
Coupling even over a distance of 3W

Temperature dependence of the resonance frequency

London penetration depht

λ_L(T≤ 10K) ≃ constant

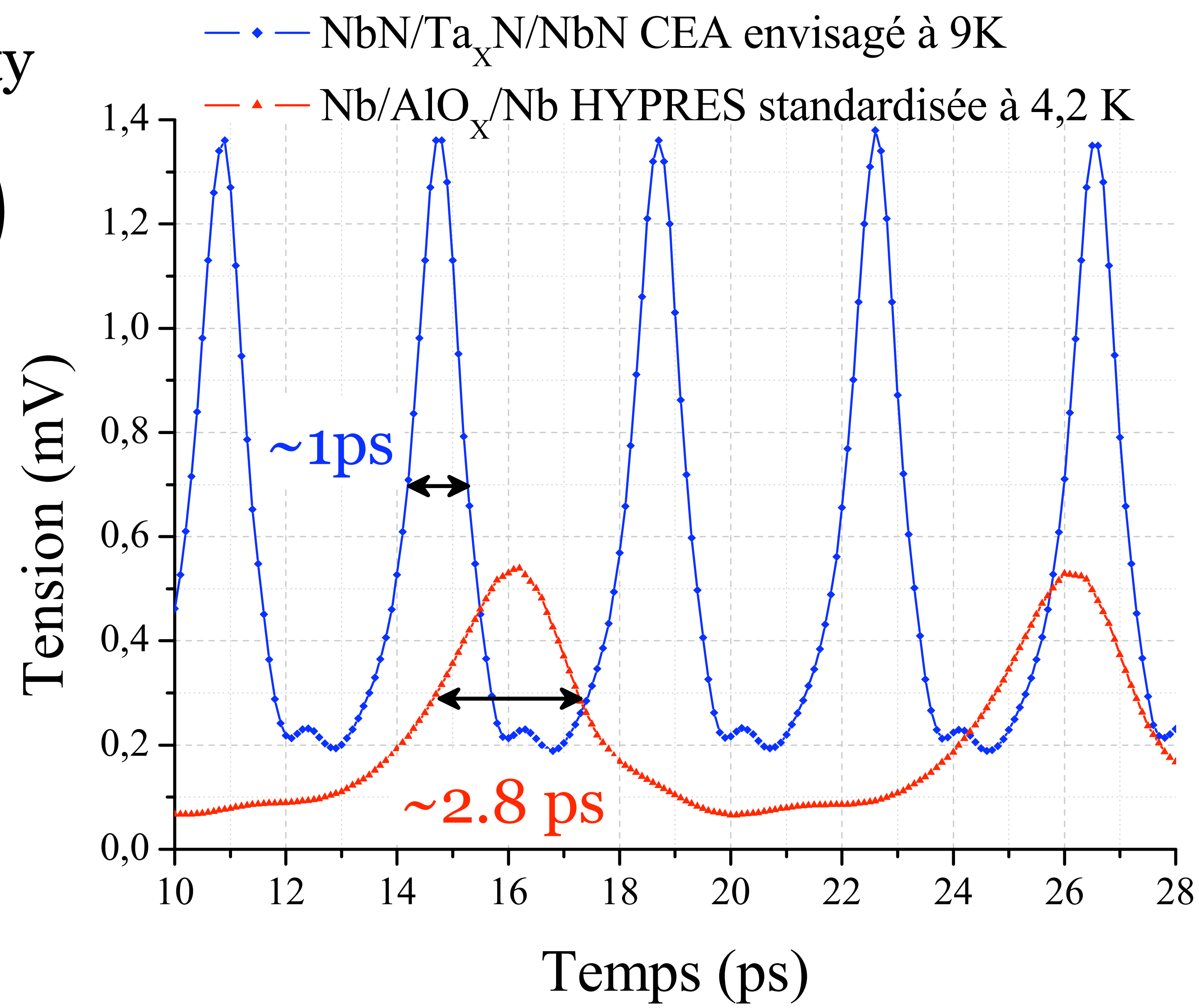
$L_\square$(T≤ 10K) ≃ constant



Synthèse sur la comparaison Nb et NbN

Arizona State University

	$Nb/AlO_x/Nb$	$NbN/Ta_xN/NbN$			
Foundry	Hypres	CEA		ASU	
T (K)	4.2	4.2	**9**	4.2	**10**
RnIc (mV)	0.49	3.9	**1.76**	0.6	**0.1**
Jc (kA/cm²)	4.5	14.7	**2.2**	50	**10**
ßc	1	0.7	**0.4**	1.9	**0.4**



Advantages

$NbN/Ta_xN/NbN$ self-shunted jonctions avoid parasitic inductances and increase the circuit density

RnIc higher than $Nb/AlO_x/Nb$ even at the same temperature of 4.2 K

Disadvantages

High $L_\square$

Temperature current noise is twice higher in NbN than Nb

Conclusions

✓ Démonstration des avantages des portes RSFQ NbN à jonctions auto-shuntées sur les portes Nb:

- T=9 K double du Nb, réfrigération allégée
- Fréquence de fonctionnement triple à 9 K : F_{RnIc}=900 GHz, $F_{circuit}$ =300 GHz, Jc=5 kA/cm²

Conclusions

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✓ Etude d'une structure de CAN sigma-delta en NbN:

- maîtrise de la zone grise du comparateur (compromis sur la fréquence d'échantillonnage)
- Proposition de solutions de filtres de décimation et de circuits de test du modulateur à complexité maîtrisée (quelques milliers de JJ)
- proposition de deux filtres RF d'entrée du modulateur (multi-puce et puce simple)
- **Grande sensibilité du CAN**: SNR=23.1 dB pour signal de 200 µV (Vpp) à 30 GHz

Conclusions

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- Proposition de solutions de filtres de décimation et de circuits de test du modulateur à complexité maîtrisée (quelques milliers de JJ)
- proposition de deux filtres RF d'entrée du modulateur (multi-puce et puce simple)
- **Grande sensibilité du CAN**: SNR=23.1 dB pour signal de 200 µV (Vpp) à 30 GHz

✓ Test des jonctions et des SQUIDs:

- Validation de la conception des inductances
- Les valeurs des jonctions et inductances NbN varient peu autour de T_f=9K

Perspectives

✓ Proposition d'un CAN adapté à l'ANR "HyperSCAN" :

- Fs=120 GHz, Fc=30 GHz, B=468 MHz, OSR=N=128 ⟶ SNR=125 dB
- complexité du CAN complet de 8000 JJ (RnIc=1.2 mV)
- évaluation de la gigue (jitter)

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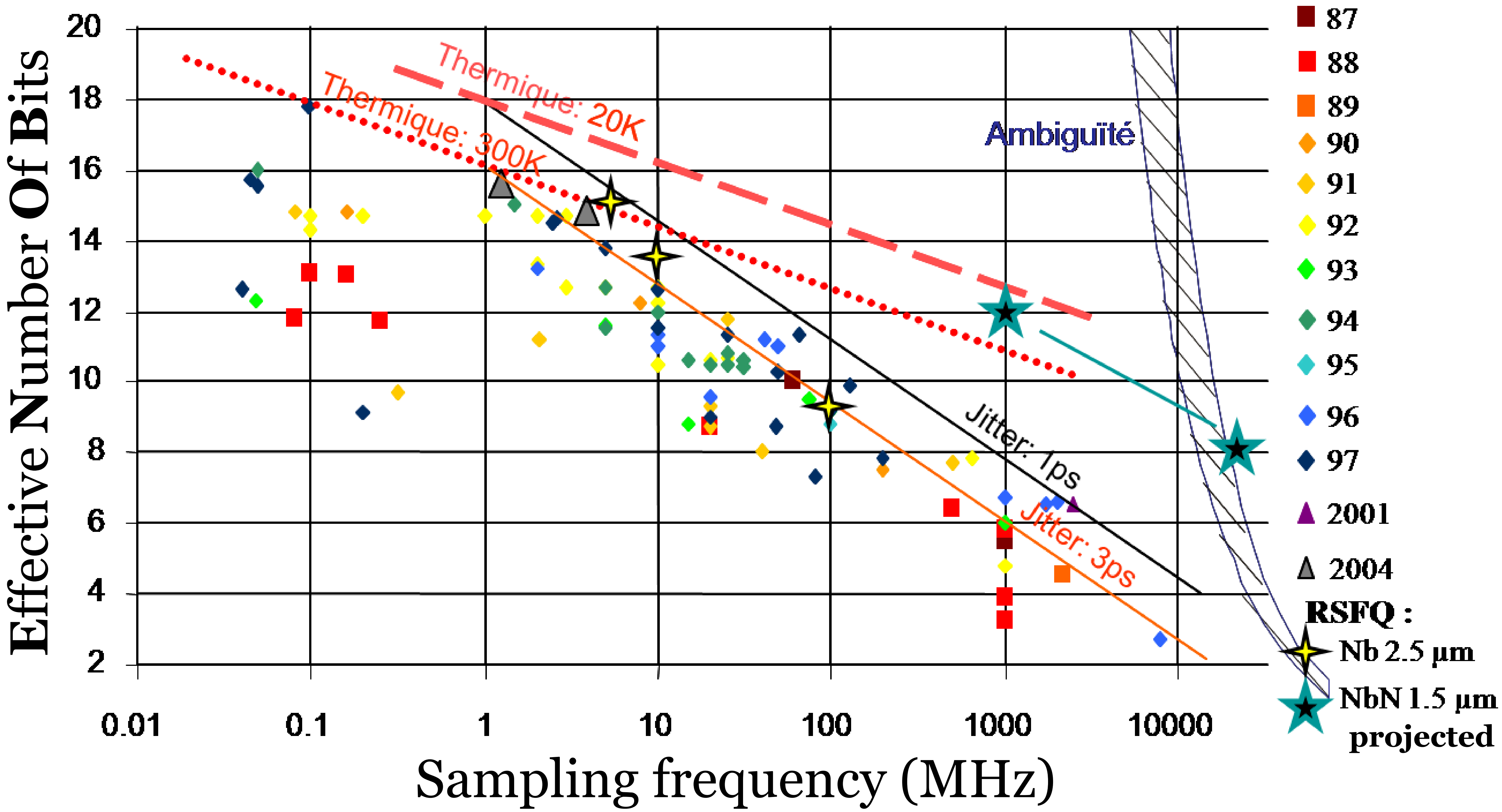
✓ Environnement de simulation enrichi (type CADENCE) :

- évaluation plus pertinente des marges des portes (Jc, RnIc, ßc en fonction de T)
- regrouper JSIM et InductEx évaluant les parasites du layout
- routing automatique et description VHDL des portes logiques

Merci pour votre attention

CAN en semiconducteurs et supraconducteurs



The ENOB increases of 1 bits every 7-8 years for the ADC Semiconductors

$$\mathrm{ENOB} = \frac{SNDR(dB) - 1.76}{6.02}$$

Signal-to-**N**oise plus **D**istortion **R**atio

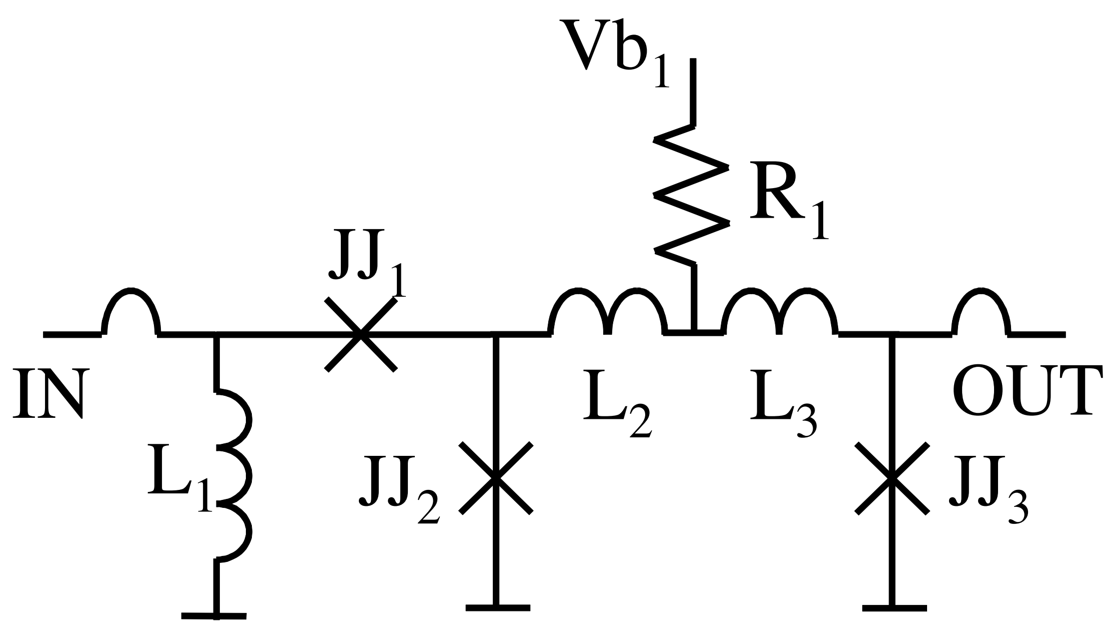
Higher in ADC superconductors thanks to the

- High Sampling rate
- Low Temperature

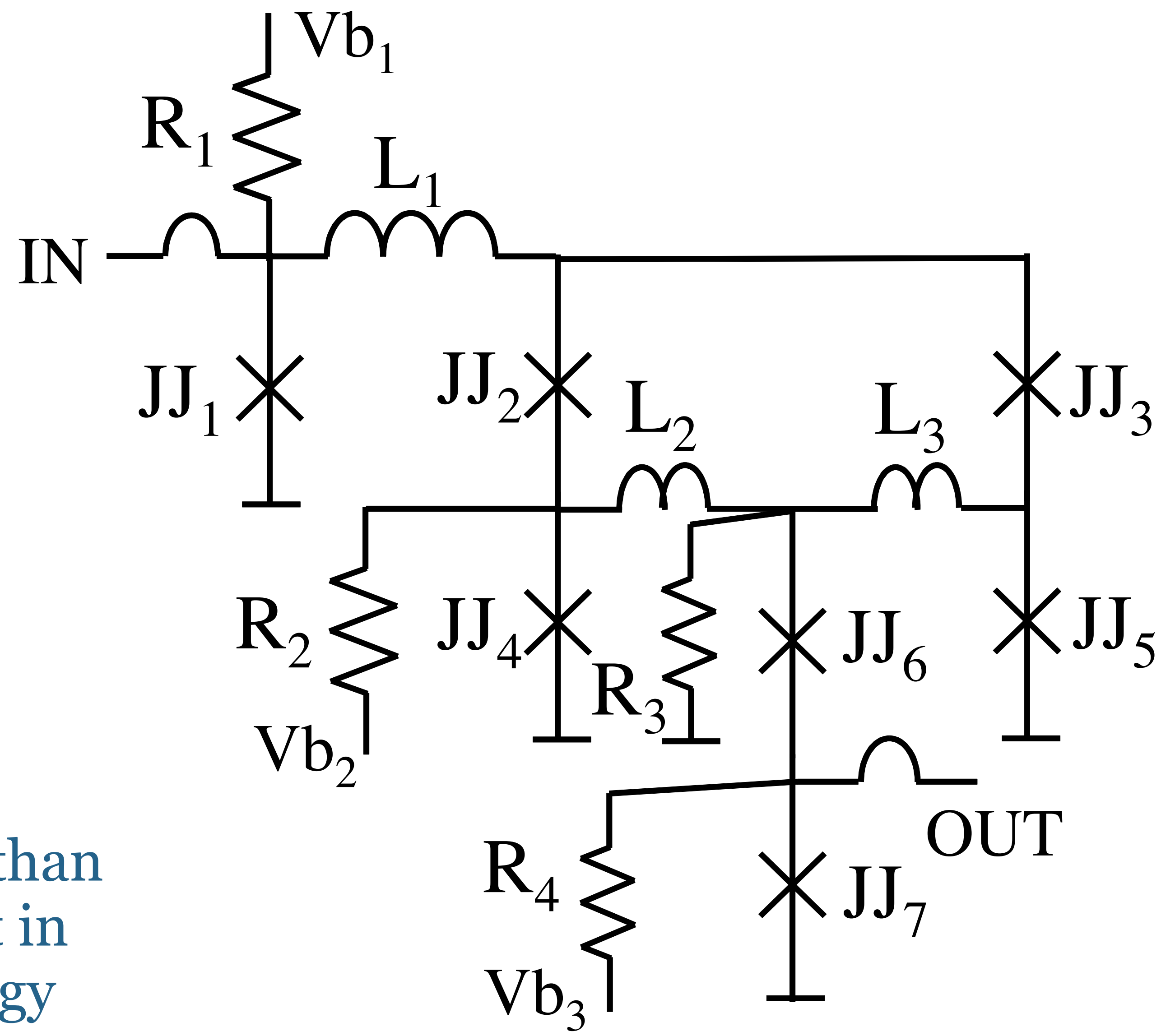
Interface Supra-Semiconducteurs

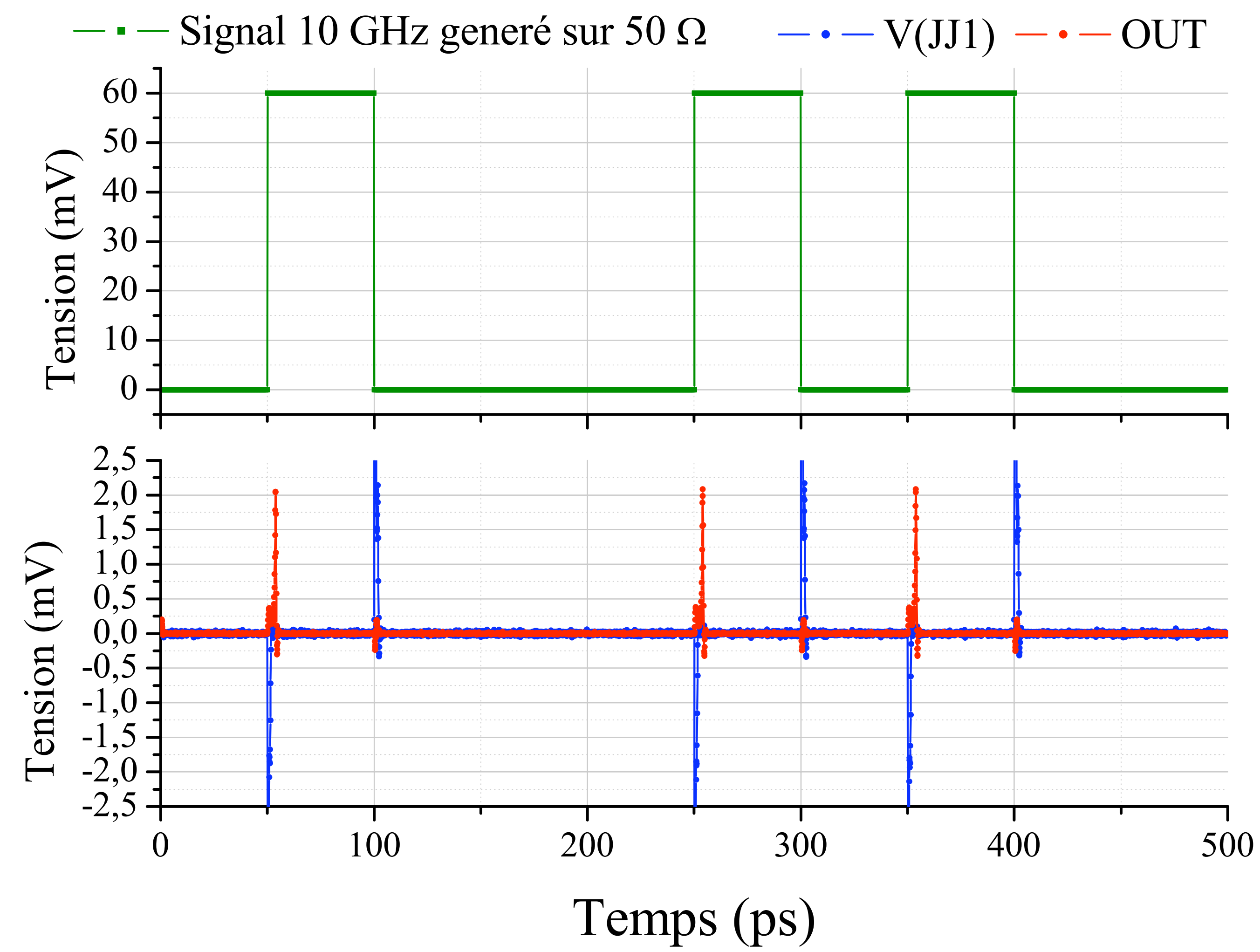
NbN/TaxN/NbN SFQ pulses width ~1ps

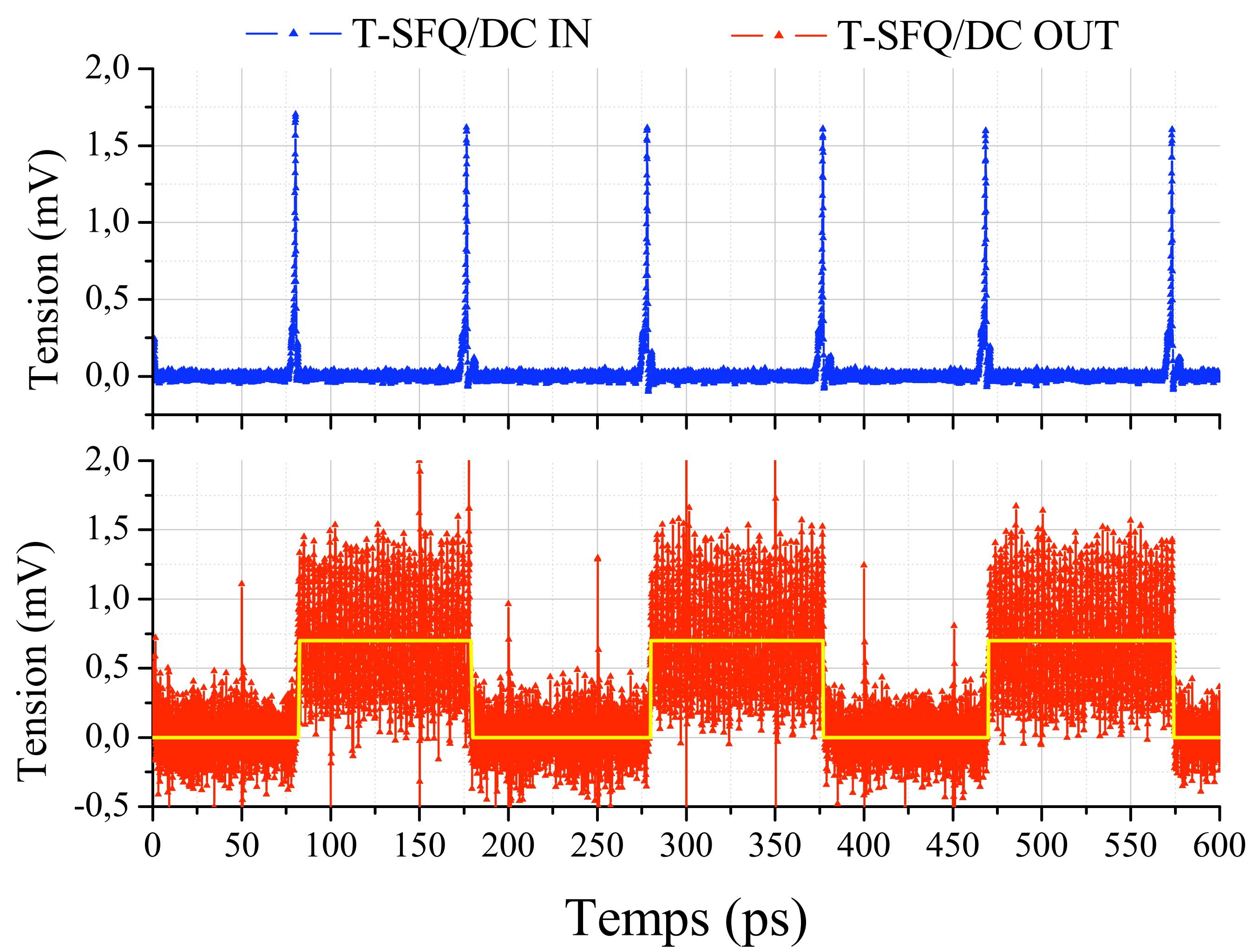
✓ DC/SFQ (3 JJs)



✓ SFQ/DC (7 JJs)







Readout

700 µV

3 times higher than the equivalent in Nb techonology