Soutenance de thèse
Université Joseph Fourier

Coulomb blockade in silicon nanowire MOSFETs

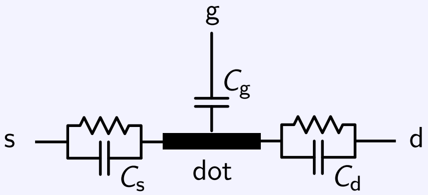
Blocage de Coulomb dans les transistors silicium à base de nanofils

Max Hofheinz

CEA-Grenoble/DRFMC/SPSMS

Grenoble, December 11, 2006

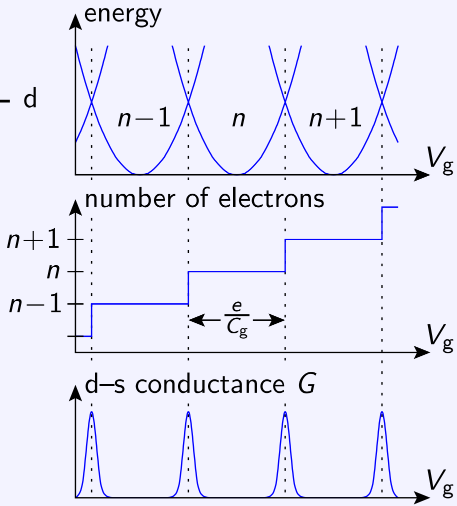
Single-electron transistor (SET)



Very small capacitor: each electron increases energy significantly

Conditions:

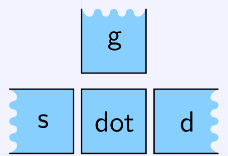
- island isolated: conductance $< \frac{e^2}{h}$
- low temperature: $k_B T < \frac{e^2}{C_g + C_s + C_d}$



Typical single-electron transistors

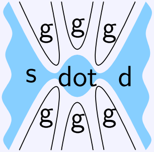
- metallic SETs
  - very high electron density
  - very high density of states
  - oxide barriers

Fulton & Dolan (1987)



- quantum dots in 2-dimensional electron gases
  - low electron density
  - ballistic, high mobility, long phase coherence length

Kastner (1989), ...



- many others: vertical dots, nanotubes, single molecules, ...

Silicon single-electron transistors

Several advantages:

- wide range of electron densities
- CMOS compatible
- benefit from advances in silicon technology:
  - very small sizes $\rightsquigarrow$ high charging energy, Coulomb blockade at high temperature
  - good control of doping
  - high-quality interfaces
- long spin coherence time (interesting for qubits).

But:

- short phase coherence lengths
- strong disorder
- so far most silicon quantum dots are based on disorder $\rightsquigarrow$ properties not controlled

Chou & Tsui, Kim & Park, Hiramoto, NTT, Cambridge, ...

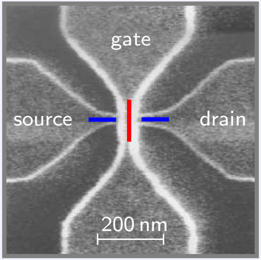
Outline

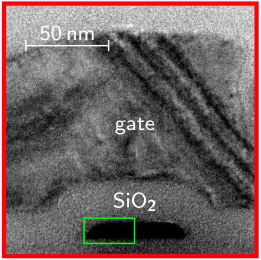
1. Silicon nanowire MOSFETs as SETs
2. Individual donor states in the barriers
3. Source and drain capacitances

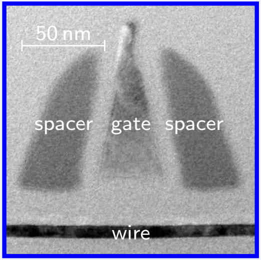
Outline

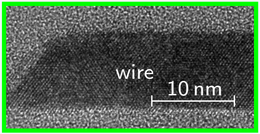
1. Silicon nanowire MOSFETs as SETs
   - Samples
   - Coulomb blockade
   - Conclusions
2. Individual donor states in the barriers
3. Source and drain capacitances

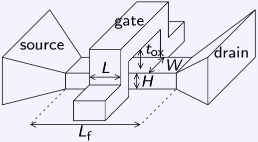
Sample geometry





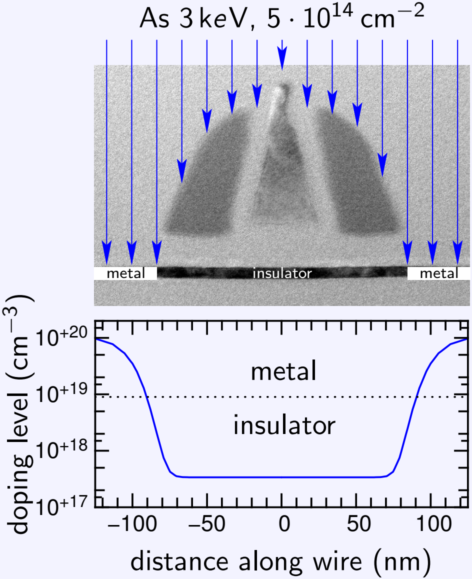






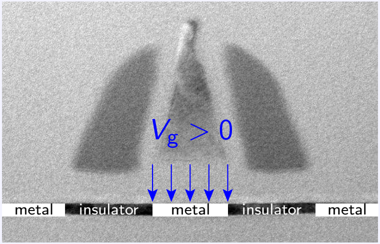
Samples made at CEA/Leti

Samples: doping



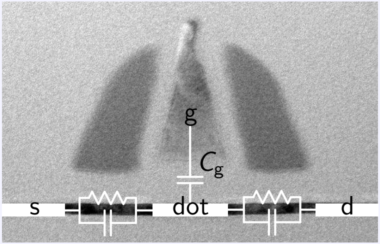
- Gate and spacers are a mask for doping.
  - Below: low doping level ⇝ insulator
  - Beyond: high doping level ⇝ metal

Samples: formation of a dot

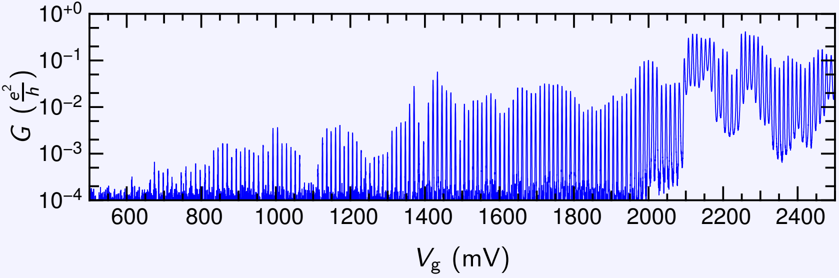


- Gate and spacers are a mask for doping.
  - Below: low doping level ⇝ insulator
  - Beyond: high doping level ⇝ metal
- A positive gate voltage attracts electrons below the gate.
  - central part of the wire becomes metallic, too
  - separated from rest by insulating parts

Samples: Coulomb blockade



We get a single-electron transistor.
$\sim$ 200 regular oscillations
(Measurement taken at 60 mK)



Size of the quantum dot

Peak spacing $V_+ = \frac{e}{C_g}$

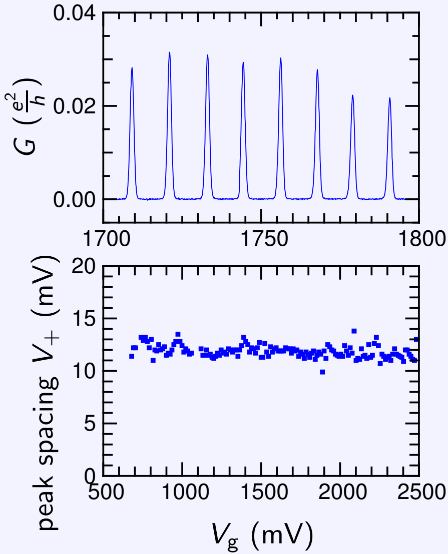
- small fluctuations of same order as single-particle level spacing: $e\alpha\sigma(V_+) \sim \Delta_1$

  Boehm, Hofheinz *et al.* PRB **71** 033305 (2005)

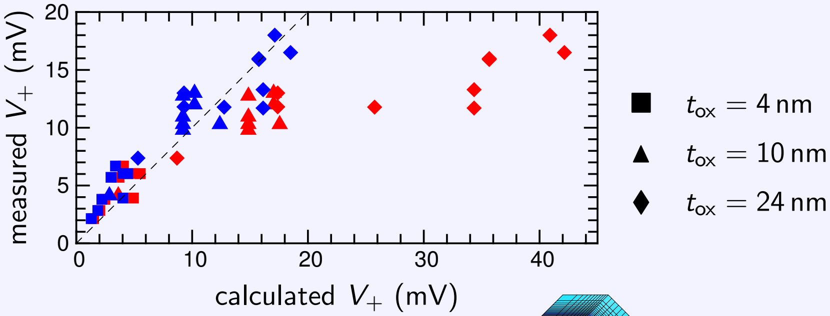
  Jehl, Hofheinz *et al.* Physica E **34** 620 (2006)

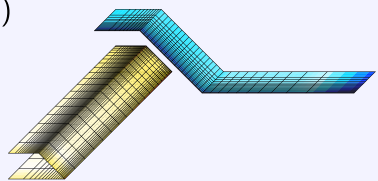
- virtually no gate voltage dependence

$\leadsto$ Gate capacitance and the size of the quantum dot are independent of gate voltage.



Size of the quantum dot





Gate capacitance C_g calculated by

- planar capacitor approximation: fails because $t_{ox} \sim L \sim W$
- numerical calculation of geometric capacitance: very good agreement

translated to peak spacing: $V_+ = \frac{e}{C_g}$

The silicon nanowire MOSFETs are good SETs

They are

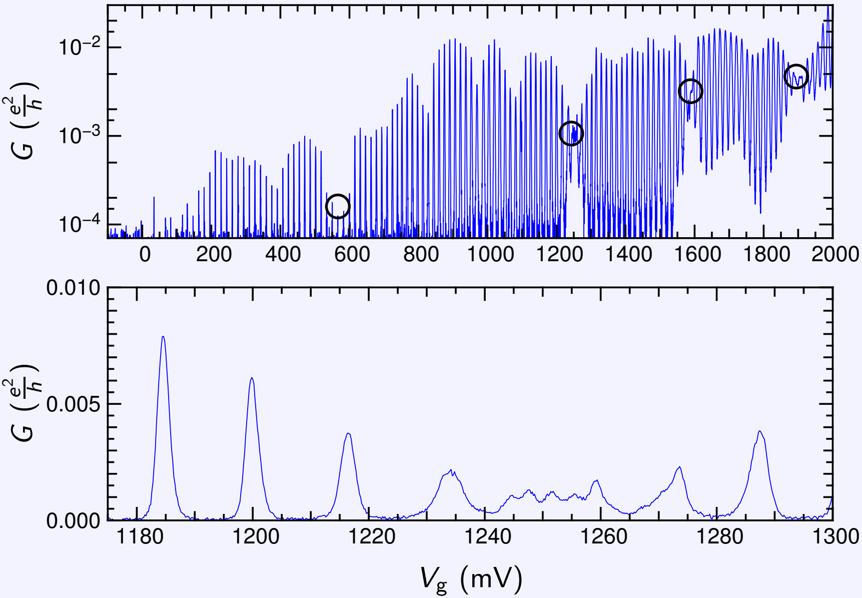
- simple
  - only one gate electrode
  - no constrictions or oxide barriers
- controlled
  - dot size / peak spacing controlled by gate/wire overlap
  - peak conductance controlled by doping level and spacer width
- stable
  - $Si\text{-}SiO_2$ interface well mastered
  - virtually no relaxation effects or sudden shifts

Hofheinz *et al.*, Appl. Phys. Lett. **89** 143504 (2006)

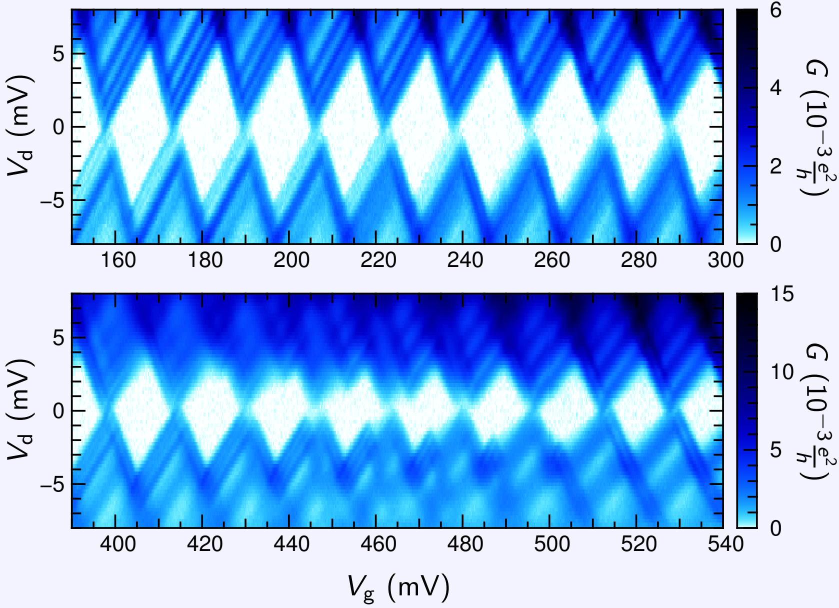
Outline

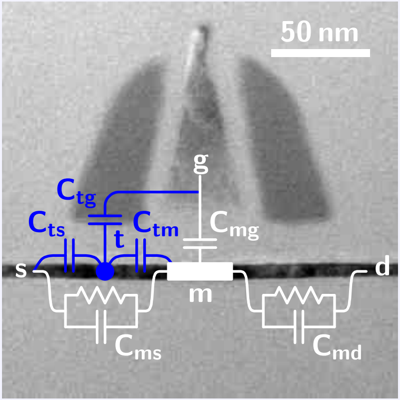
1. Silicon nanowire MOSFETs as SETs
2. Individual donor states in the barriers
   - Model
   - Capacitance matrix and position
   - Spin
   - Dynamics
3. Source and drain capacitances

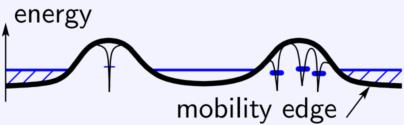
Anomalies in the Coulomb blockade spectrum



Anomalies in the Coulomb blockade diamonds







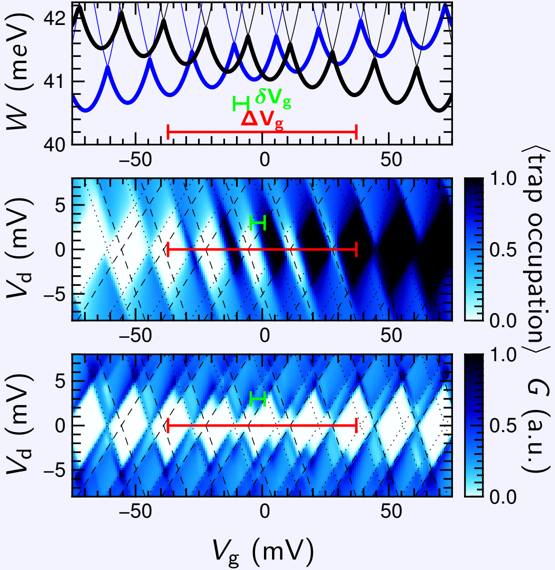
small impurity dot

- coupled capacitively to source, gate and main dot
- coupled with a very small conductance to source and main dot: acts only electrostatically

$$W = \frac{e^2\,(n_\mathrm{m} + \beta_\mathrm{t} n_\mathrm{t} - x_\mathrm{m} - \beta_\mathrm{t} x_\mathrm{t})^2}{2(C_\mathrm{m} + \beta_\mathrm{t} C_\mathrm{t})} + \frac{e^2\,(n_\mathrm{t} - x_\mathrm{t})^2}{2\,(C_\mathrm{t} + C_\mathrm{tm})}$$

with $\beta_\mathrm{t} = \frac{C_\mathrm{tm}}{C_\mathrm{t} + C_\mathrm{tm}}$

Simulation



Two effective parameters:

$$\alpha_t = \frac{C_{tg}}{C_t + C_{tm}}$$

$$\beta_t = \frac{C_{tm}}{C_t + C_{tm}}$$

Trap shifts oscillations by:

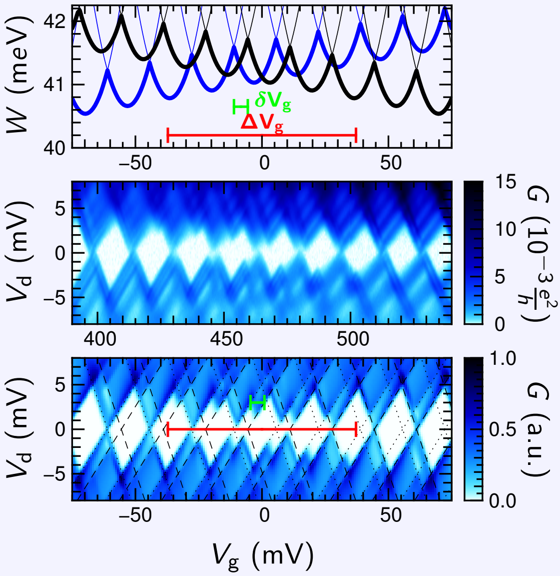
$$\delta V_g = \beta_t V_+$$

Resonances suppressed over:

$$\Delta V_g = \frac{\beta_t(1-\beta_t)}{\alpha_t}\alpha_m V_+$$

Numerical calculations:
sequential tunneling model

Simulation vs. experiment



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Numerical calculations: sequential tunneling model

Capacitance matrix and position

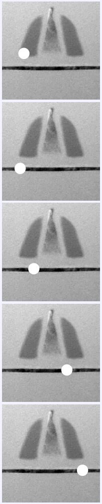
$\left(\frac{1}{10}, 2, 0, 1\right) \frac{e}{\mathrm{V}}$

$\left(\frac{1}{50}, 2, 0, 1\right) \frac{e}{\mathrm{V}}$

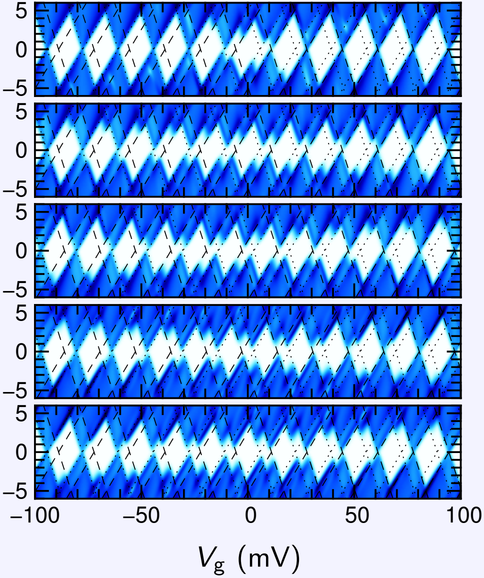
$\left(\frac{1}{50}, 1, 0, 2\right) \frac{e}{\mathrm{V}}$

$\left(\frac{1}{50}, 0, 1, 2\right) \frac{e}{\mathrm{V}}$

$\left(\frac{1}{50}, 0, 2, 1\right) \frac{e}{\mathrm{V}}$



$(C_{\mathrm{tg}}, C_{\mathrm{ts}}, C_{\mathrm{td}}, C_{\mathrm{tm}})$



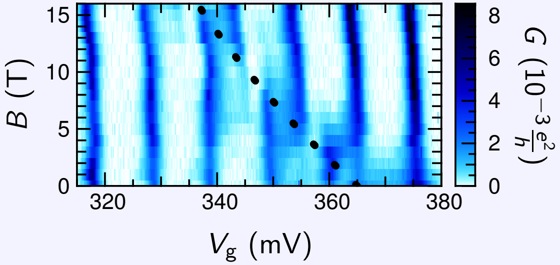
Capacitance matrix and position

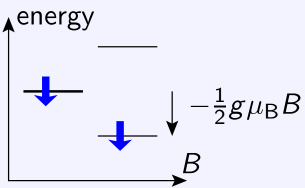
Capacitance matrix for observed traps:

- very different peak shifts observed: $\beta_\mathrm{t} = 0 \ldots 1$
- several Coulomb blockade resonances suppressed ($\Delta V_\mathrm{g} \gg V_+$):
  weak gate control for traps $\alpha_\mathrm{t} \sim 0.01$

Conclusions

- traps near nanowire
- β_t gives position along the wire





- shape of the trap signature gives

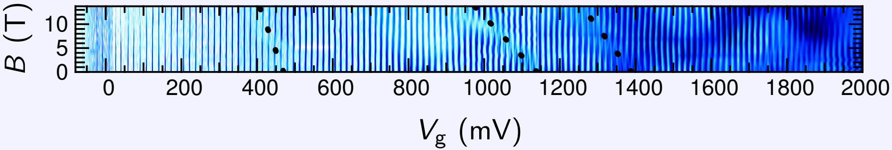
$$\beta_t \approx 0.5 \qquad \alpha_t \approx 0.026 \ldots 0.043$$

- Zeeman shift predicted with α_t and $S_z = -\frac{1}{2}$ (dotted lines):

$$e\alpha_t \frac{\partial V_g}{\partial B} = g \mu_B S_z$$

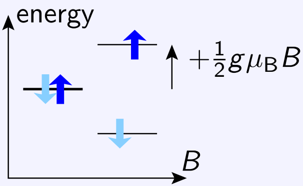
agrees very well with observed shift of the signature

Zeeman shifts indicate singly occupied traps



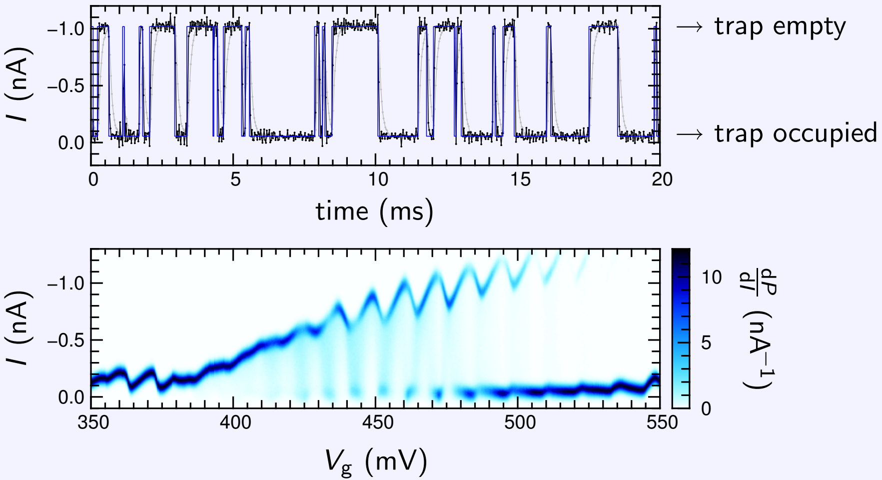
- Most Zeeman shifts go towards lower gate voltage.

- Traps occupied with several electrons would imply shifts to higher energy/gate voltage.



Traps can only be occupied with one electron:
Most likely dopant states.

Monitoring a trap: Random telegraph signal



All data at $V_d = -6\,\text{mV}$, upper panel at $V_g = 500\,\text{mV}$.

Fujisawa *et al.* APL **84** 2343 (2004) Bylander *et al.* Nature **434** 361 (2005) Gustavsson *et al.* PRL **96** 076605 (2006)

Random telegraph signal only visible for slow traps

Observation of random telegraph noise confirms model:

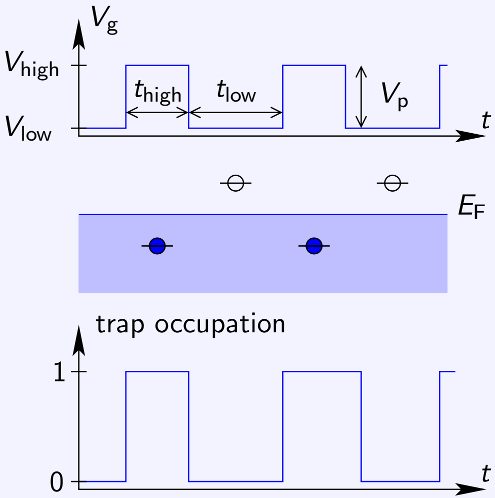
- anomalies caused by charge traps
- periodic oscillations of trap occupation with gate voltage

But random telegraph noise only observed with very few traps

- only traps slower than measurement (30 µs) show RTS
- interpretation: most traps are much faster
- if so: confirms that traps are in the wire and not in the oxide (traps in the oxide are slow)

Need to probe dynamics of faster traps!

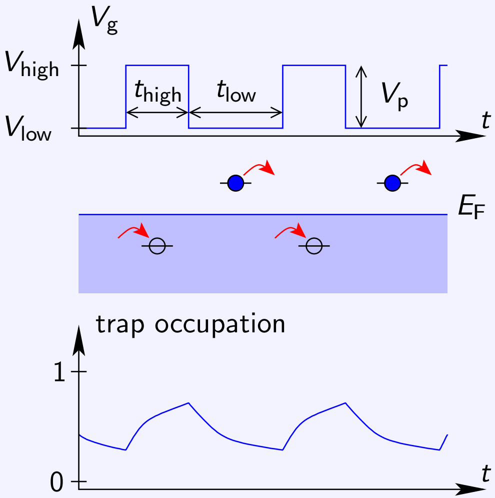
Pulse excitation



If the trap can follow the pulse signal:

- trap is always in its equilibrium state
- peak positions as in DC

Pulse excitation



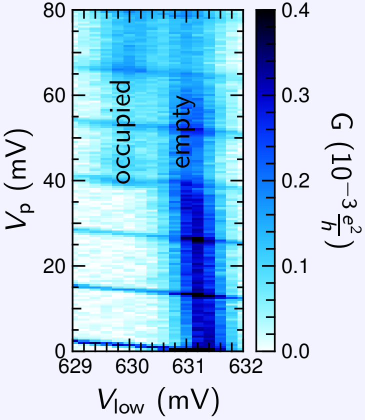
If the trap cannot follow the pulse signal:

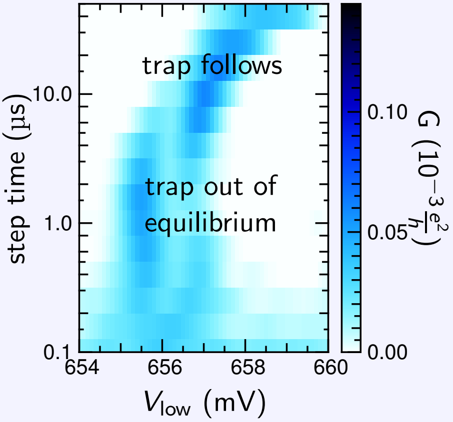
- statistical mixing of trap states
- resonances observed twice
  - once when trap is empty
  - once when trap is filled

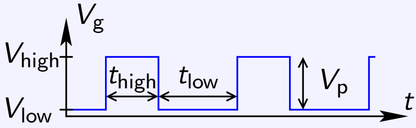
separation:

$$\delta V_g = \beta_t V_+$$

Pulse excitation: Results







- time constant of this trap $\sim 1\,\mu s$
- can only go to several MHz (otherwise ringing)
- most traps still faster

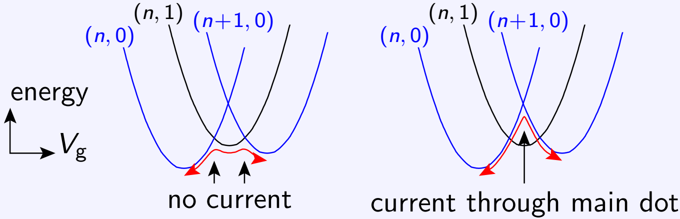
From pulse to sine-wave excitation

In DC we saw two effects of a trap:

- shifts Coulomb peaks:
  We applied pulse signals to see the dynamics.
- suppresses Coulomb peaks:
  Dynamics can be seen with a sine signal ⇝ no ringing.

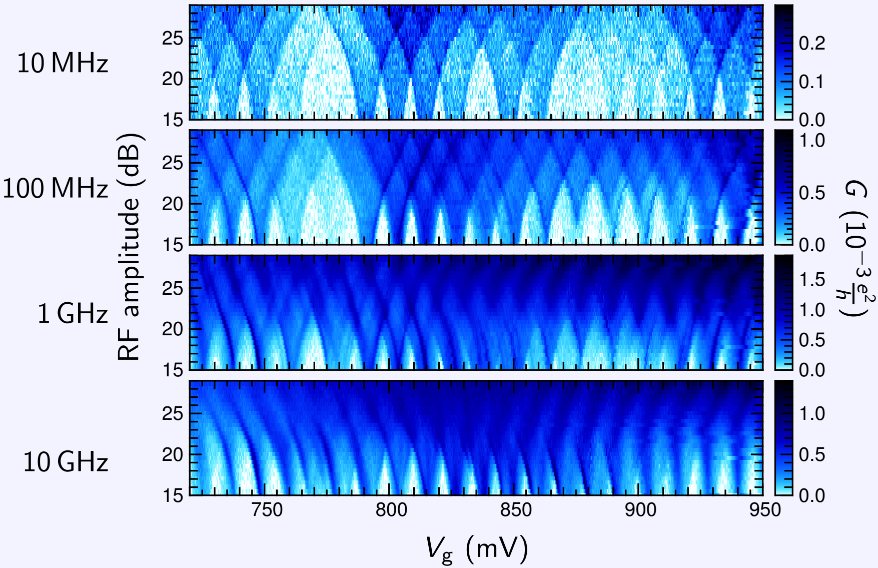
low frequency: trap charge relaxes

high frequency: trap cannot follow



Coulomb peaks restored when signal faster than trap.

Sine-wave excitation



Sine-wave-excitation: Results

Most traps very fast

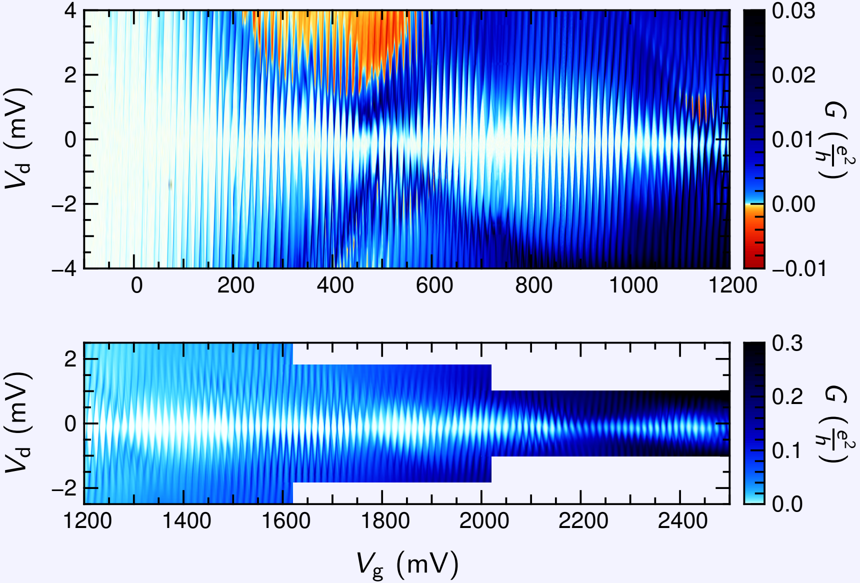
- $\sim 1\,\mathrm{ns}$
- as fast as main dot
- trap states in the wire, otherwise too slow

Most likely: dopant states.

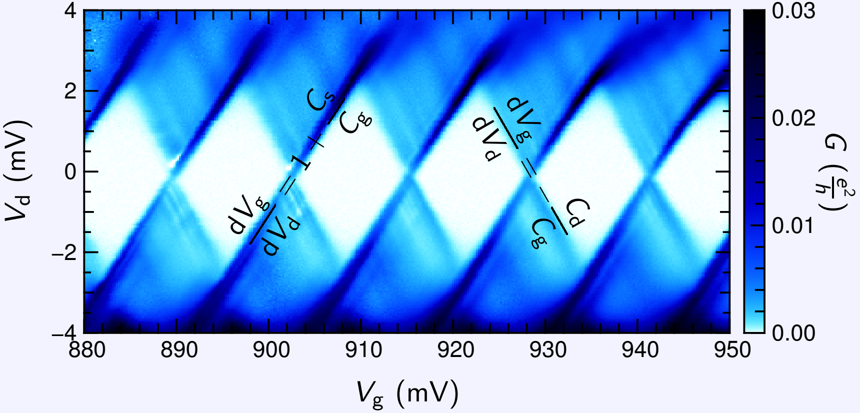
Outline

1. Silicon nanowire MOSFETs as SETs
2. Individual donor states in the barriers
3. Source and drain capacitances

Coulomb diamonds shrink with gate voltage

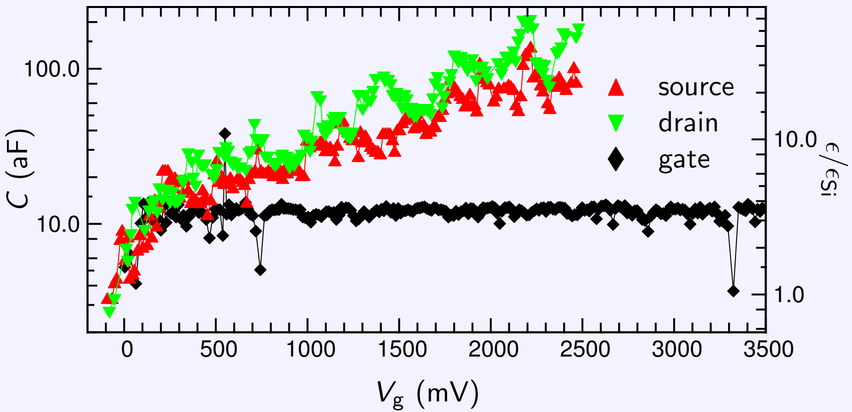


Source and drain capacitances



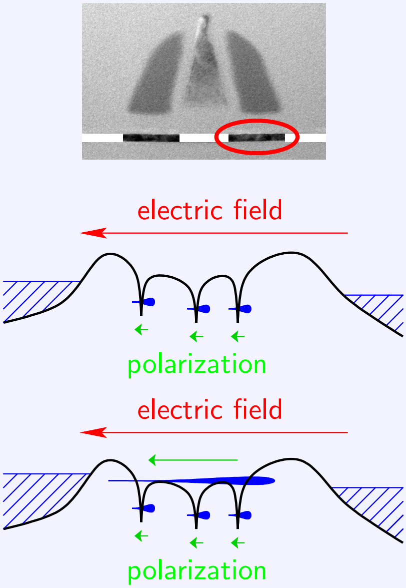
- Gate capacitance constant
- Diamond slopes determined by source and drain capacitances

Source and drain capacitances



- Gate capacitance constant (already seen)
- Source and drain capacitance increase by factor ~ 30
- Volume of source and drain capacitors constant.
- Increase due to dielectric constant!

Increase of the dielectric constant



When Fermi level is raised with respect to band edge:

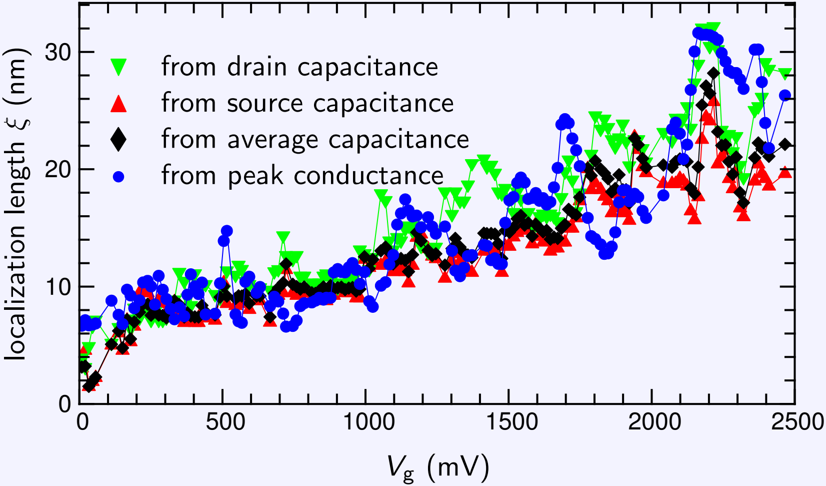
- Less localized states become occupied.
- These states have higher polarizability.
- Dielectric constant increases:

$$\epsilon \propto \xi^2$$

Imry *et al.*, Phys. Rev. B **26**, 3436 (1982)

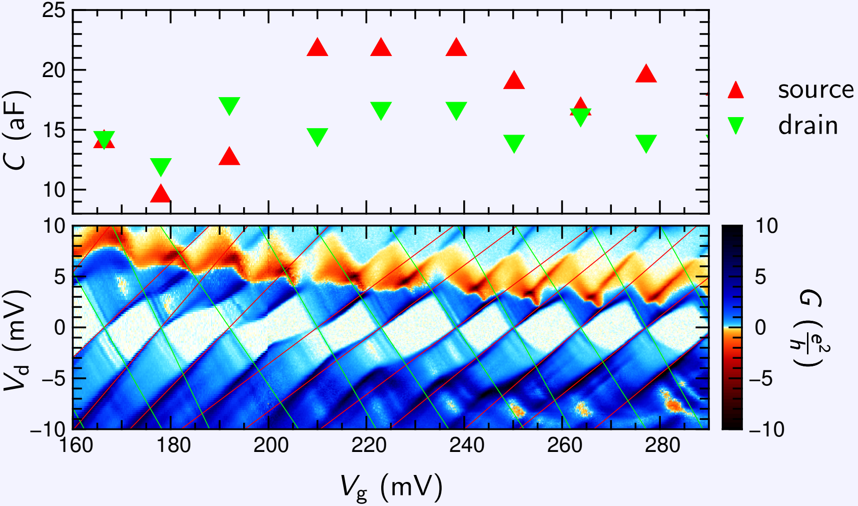
Castner *et al.*, Phys. Rev. Lett. **34** 1627 (1975)

Evolution of the localization length



Based on scaling laws $\langle \epsilon \rangle \propto \xi^2$ and $\langle G \rangle \propto e^{-2L/\xi}$

Increase of dielectric constant at trap signatures



Conclusions

- The silicon nanowires MOSFETs form good SETs.
  - simple
  - controlled
  - stable
- Trap states are probed with the SET. Measurements of
  - capacitance matrix
  - spin
  - dynamics

  support that traps are dopant states.

  Hofheinz *et al.*, to be published in Europhys. J. B, cond-mat/0504325
- First systematic study of source and drain capacitances
  - Strong increase in accordance with scaling laws for metal-insulator transition

Outlook

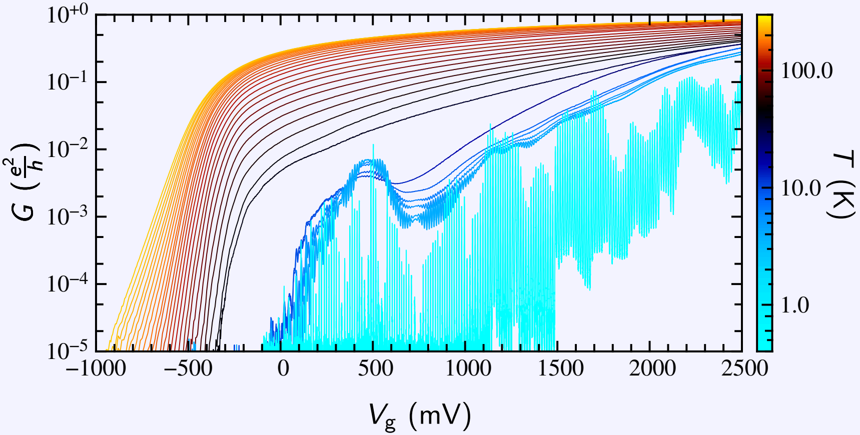
SET:

- use for applications (electron pump)
- test other doping profiles

Traps:

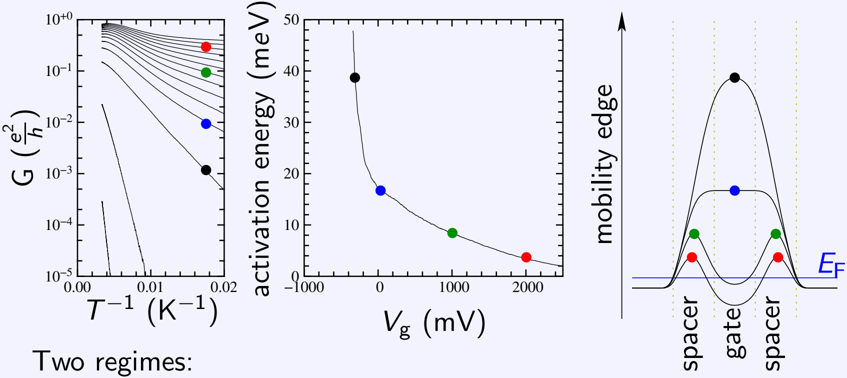
- verify attribution to dopant states with undoped wires
- measure spin relaxation

Cooling: FET → SET



Above 50 K: good FET

Below 10 K: regular Coulomb-blockade oscillations



Two regimes:

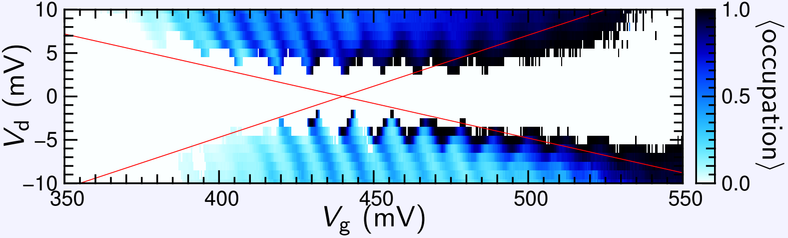
below threshold: Transport dominated by channel barrier height. Barrier height depends strongly on gate voltage

above threshold: Transport dominated by spacer regions. Barrier height depends weakly on gate voltage

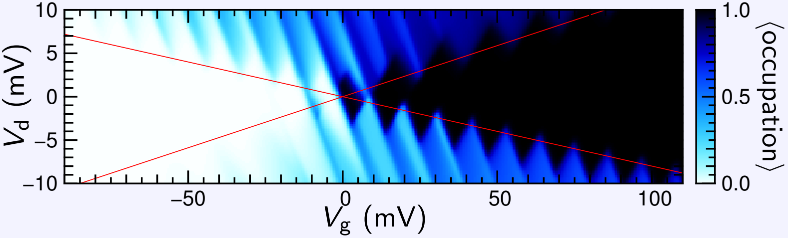
No thermal activation between 4.2 K and base temperature.

RTS of a slow trap

measured mean trap occupation

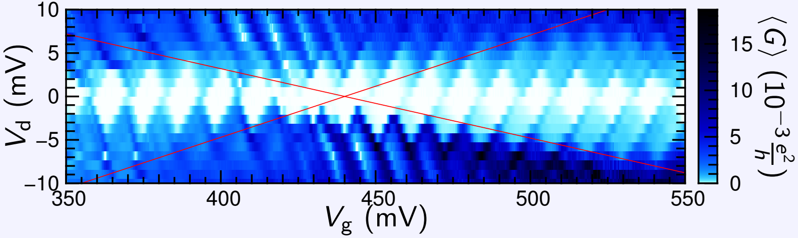


simulated mean trap occupation

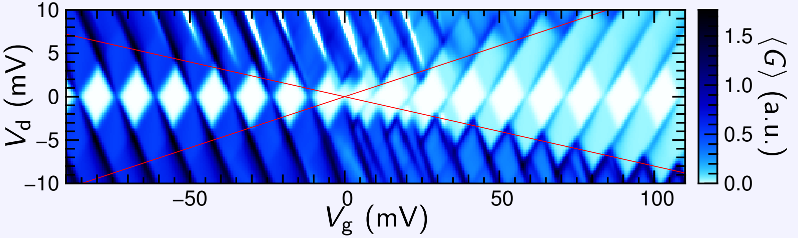


RTS of a slow trap

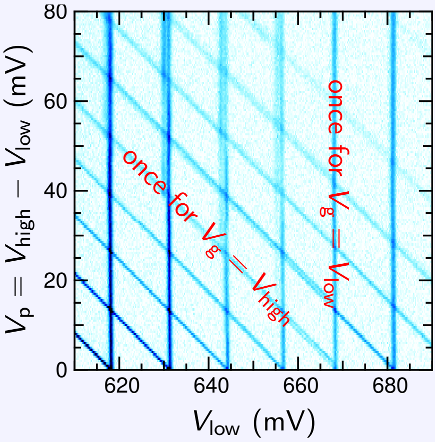
measured mean conductance

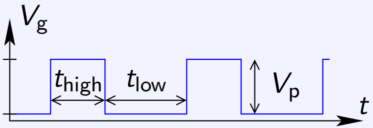


simulated mean conductance



Pulse excitation

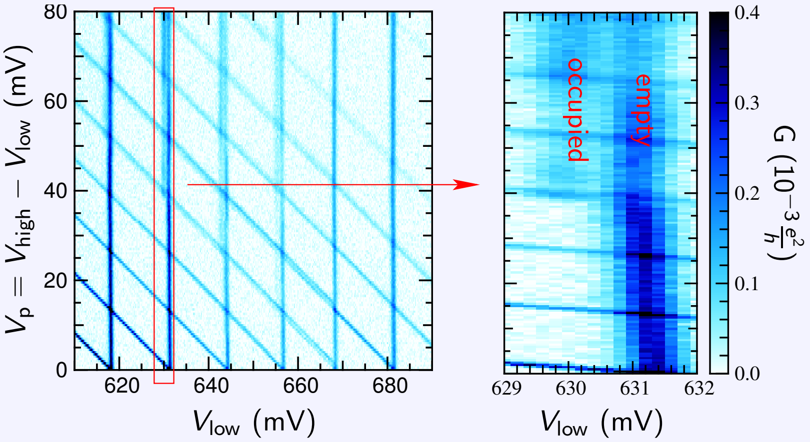




Each feature appears twice...

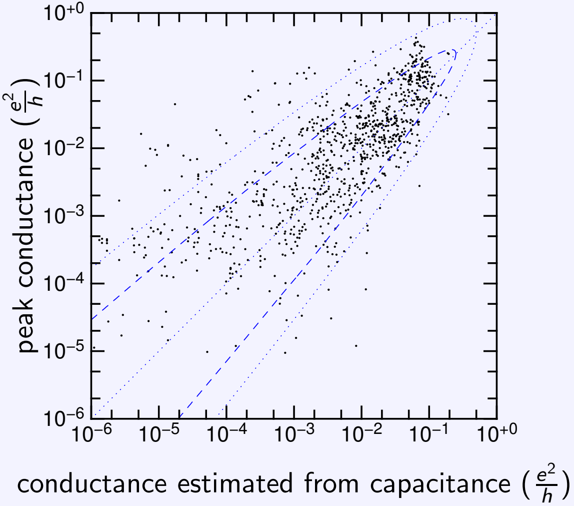
$t_{high} = t_{low} = 1\,\mu s$

Pulse excitation



At $t_{high} = t_{low} = 1\,\mu s$ the trap cannot follow:
Split for occupied and empty trap.

Scaling



- peak conductance estimated from capacitance via scaling laws:

$$\epsilon \propto \xi^2$$
$$G \propto e^{-2L/\xi}$$

- data from 10 samples
- lines: conductance fluctuations as predicted by RMT.