TOOLS FOR IMPEDANCE EXTRACTION IN INTEGRATED CIRCUITS (IC)

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Outils pour l'Extraction d'Impedance dans les Circuits Intégrés

(Tools for impedance extraction in integrated circuits (IC))

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Resumé

La fréquence d'opération des circuits intégrés continue de monter donc l'inductance des interconnexions devient non négligeable. Il est donc nécessaire de pouvoir la calculer de façon précise pour une analyse à posteriori correcte. Dans cette thèse, nous développons une nouvelle approche pour le calcul de l'impédance propre et mutuelle dans les interconnexions. Notre méthode alternative est moins chère, du point vu du calcul, que celle du PEEC. Elle est aussi plus stable mais tout de même aussi précise. Nous résoudrons le problème de capturer la dépendance en fréquence de l'impédance, conséquence des effets de proximité et de peau.

Nous étendons notre analyse a l'étude de l'impédance propre et mutuelle des dispositifs passifs, plus spécifiquement les inducteurs intentionnels. Nous incluons un modèle RLC utile pour capturer des informations importantes comme la fréquence de résonance ou le facteur de qualité.

Nous dérivons une expression originale pour le délai d'une ligne de transmission RLC excitée par une rampe avec un temps de montée non nul et avec une capacité de charge placée à la fin de la ligne.

Nous présentons une application utile des effets inductifs dans les circuits intégrés. Ce que nous montrons est la faisabilité pour transmettre des signaux à la vitesse maximale, celle de la lumière dans le milieu de transmission.

Abstract

With the onset of Gigahertz frequencies on integrated circuits (IC), inductance effects need to be accurately computed for posterior timing and noise simulations. In this thesis, we develop a consistent, accurate and computationally inexpensive approach to self and mutual impedance extraction of interconnects. Our alternative method is computationally much less expensive than the PEEC alternative, significantly more stable, while

equally accurate. We solve the problem of capturing the correct frequency dependence of the inductance and resistance extraction, one that fully accounts for proximity effects as function of frequency. Furthermore, we correctly generalize our treatment to incorporate nonuniform current distributions as needed to model the skin effect, that starts manifesting in digital IC's at frequencies near 15 GHz.

We extend our analysis to the study of passive inductor devices, both for self and mutual impedance computations. An RLC extraction method is presented in order to capture important information such as self-resonance frequency and quality number.

We derive an original equation for the delay of an RLC transmission line under a ramp excitation, with a finite load capacitance.

We present a useful application of inductance in digital IC's. What we demonstrate in this work is the feasibility to propagate signals at the maximum speed, that of light in the medium.

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Introduction (français)

Conception de circuits intégrés

Les avancés en microélectronique représentent un des plus merveilleux accomplissements dans l'histoire de la science et de la technologie. Gordon Moore [1] en 1965 étudiait les projections de coût d'introduction de nouvelles technologies. Il a trouvé un optimum quand les nouveaux procédés (noeuds de technologie) avec une plus petite taille (toutes les dimensions ajustées par le paramètre d'échelle $\lambda \approx 0.7$) sont introduits de façon constante une fois par an. Etant donné que le nombre de transistors est proportionnel à l'inverse du carré du paramètre d'échelle, i.e. $1/\lambda^2 \approx 1/0.49 \approx 2$, le nombre de transistors d'une technologie double tous les ans. En 1975, le PDG d'Intel, corrigea son observation par rapport à l'introduction de nouvelles technologies, d'une tous les ans à une tous les deux ans. Le nombre de transistors double donc tous les deux ans. Cette observation empirique devint une véritable prophétie, voir la Figure 1. Les entreprises de conception et de production ciblent leurs investissements sur de nouvelles technologies de façon à satisfaire cette "Loi de Moore". Ce qui a été projeté pour durer 10 ans a survécu 36 ans de croissance exponentielle comme la Figure 1 le montre. La croissance de l'industrie microélectronique est caractérisée par ce simple graphique. La courbe permet de comprendre deux résultats importants : le coût associé à la mise en place d'une fonction en microélectronique décroît de façon exponentielle avec le temps. La seconde conclusion : la performance (vitesse) associée à la fonction mise en place croit exponentiellement. La vitesse d'horloge des processeurs Intel, présents dans le graphique, a doublé à chaque nouvelle génération. La raison de cette amélioration en performance est en fait simple : la vitesse d'opération d'un circuit digital dépend de la vitesse de l'horloge qui contrôle l'exécution du système. La vitesse maximale de l'horloge est limitée par la vitesse de propagation d'un signal à travers une concaténation d'un nombre fixe (typiquement moins de dix) de fonctions logiques.

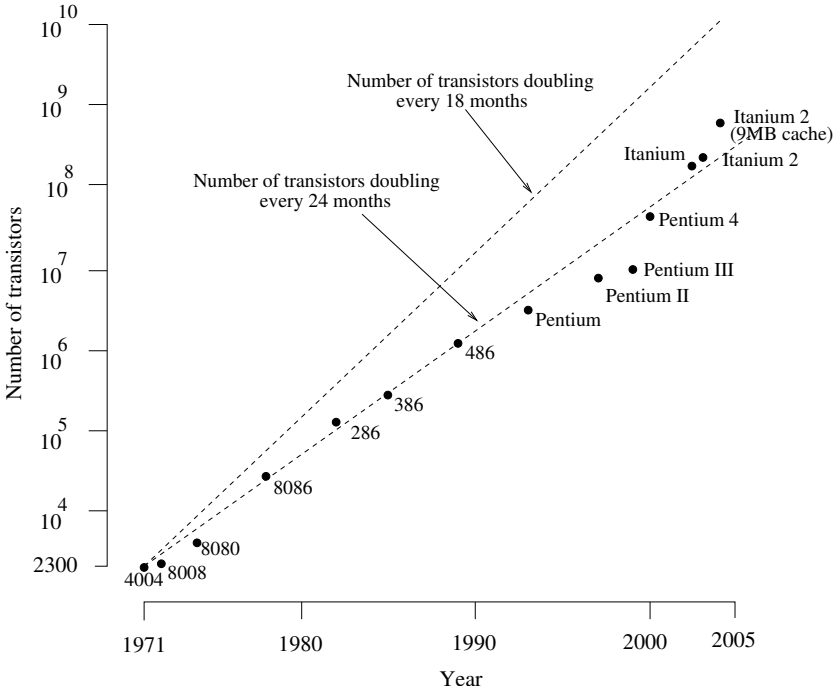


Figure 1: Nombre de transistors dans un processeur pour une année donnée

Le temps de propagation du signal dans une fonction logique, sans prendre en compte les effets dus aux fils, est égal à la somme des temps de transit des transistors qui composent la fonction logique. Les deux ingrédients de base qui contrôlent la performance d'une fonction logique sont le temps de transit d'un transistor et le délai dans un fil.

Examinons, premièrement, le délai dans les transistors. Le temps de transit τ_{tr} peut-être estimé comme :

$$\tau_{tr} = \frac{L^2}{\mu(V_{gs} - V_{thr})} \tag{1}$$

avec L la longueur du canal, μ la mobilité des électrons, V_{gs} le voltage dans la grille et V_{thr} la quantité de voltage nécessaire pour produire la transition dans le transistor.

Sous un changement de technologie (toutes les dimensions réduites par $\lambda \approx 0.7$) et avec des voltages réduits par la même échelle, le temps de transit τ_{tr}, est aussi réduit par λ. Le temps de transit est le temps minimal nécessaire pour qu'une charge dans la grille du transistor produise une charge équivalente à travers le canal, jusqu'à la grille du prochain transistor. Le temps de transit a évolué de 0.5 ns pour une technologie 6 μm en 1978, jusqu'à 0.01 ns pour une technologie 90 nm en 2005 [2]. Le temps

de transit a toujours été un élément clé dans la quête d'une meilleure performance des circuits intégrés. Pour décrire la performance du système à partir de la performance des transistors nous devons d'abord imposer une contrainte, celle de la performance des fils qui connectent les transistors (l'interconnexion). Durant les 25 premières années du développement technologique, la performance de l'interconnexion était majoré par le délai d'un nombre fixe d'étapes logiques multiplié par τ_{tr} [3]. Cet argument explique pourquoi le délai du système δ_{system} décroît avec λ:

$$\delta_{system_i} = \lambda \delta_{system_{i-1}} \tag{2}$$

La décroissance exponentielle du délai du système produit une croissance exponentielle de la performance. Un nombre croissant de transistors et une croissance dans le nombre de fils sont inévitablement liés. Aux premiers jours de la technologie de silicium (Si), il était possible de placer tous les signaux et fils de masse dans deux couches de métal, au plus. Avec l'augmentation de la densité de transistors dans une puce, il a été nécessaire d'augmenter le nombre de couches de métal pour pouvoir placer l'interconnexion (il est possible de mettre 10 couches de métal pour une technologie 65 nm en 2006). Il existe deux groupes de fils dans une puce de nos jours: les fils locaux, placés dans les deux premières couches de métal et qui représentent 90% de l'interconnexion et les fils globaux, placés dans les couches supérieures qui servent à connecter différents blocs de transistors. Le fils locaux ont des longueurs à l'échelle de λ, donc la supposition que leur délai est majoré par celui des transistors est toujours valide. Les fils globaux, quant à eux, ont une échelle qui n'est pas contrôlée par celle de la technologie. Leurs longueurs sont de l'ordre du millimètre, donc l'estimation du délai du système est sérieusement affectée par le délai des fils globaux. Pour cette raison, le comportement électrique de ce type de fils doit être connu avec une assez bonne précision.

Le délai dans les transistors continue de décroître avec la technologie, le délai des fils globaux devient donc le principal contributeur au délai du système. Cette crise a encouragé les concepteurs à placer des répéteurs dans les longues lignes de signaux critiques. Cette solution n'est pas très désirable, étant donné que ces répéteurs consomment une grande fraction de l'énergie totale du système, proche de 60% actuellement. La théorie de circuits rudimentaire nous indique qu'une impulsion appliquée dans une extrémité d'un conducteur se propage jusqu'à l'autre extrémité avec une constante de

Année	2005	2010	2015
Fréquence Maximal (GHz)	5.2	15.08	33.4

Table 1: Fréquence maximale dans une puce pour chaque technologie. Projections faites par le ITRS 2005 [2]

temps donnée par:

$$\tau_{sig} = RC \tag{3}$$

avec R et C la résistance et la capacité du fil, respectivement. Il est donc vital de pouvoir connaître les paramètres RC des fils globaux dans un circuit intégré pour pouvoir donner une bonne estimation de sa performance. Cette prémisse a stimulé Mentor Graphics pour réaliser des développements technologiques très importants dans ce domaine [4].

L'intérêt de cette thèse est sur le problème subséquent : Considérez la propagation d'un signal dans un fil, contrôlé par un transistors dans un système digital. Le signal de sortie d'un transistor, qui est en même temps le signal d'entrée du fil, est celui d'un interrupteur imparfait: une transition linéale d'un état de bas voltage (0 logique) vers un état de haut voltage (1 logique). Cette transition peut être bien approximée par une rampe avec un temps de montée de τ_{tr}. La transformée de Fourier de cette rampe contient une amplitude appréciable jusqu'à une fréquence de $f_{max} \approx \frac{1}{\pi\tau_{tr}}$.

Dans la Table 1 nous présentons f_{max} pour des technologies présentes et futures. Notez que f_{max} est proportionelle à $1/\lambda$.

Pour des fréquences allant jusqu'à 1 GHz, la propagation d'un signal peut être bien approximée en considérant seulement les contributions de la capacité et la résistance des segments qui forment un fil. La superposition de différents segments, chacun représenté par un élément RC, devient la solution de l'équation unidimensionnelle de diffusion. Des expressions pour le délai des systèmes RC pour une rampe en entrée sont connues dans la littérature [5].

La technologie a réussi à réduire le délai des fils dominés par RC. Le remplacement de l'aluminium (Al) par le cuivre (Cu)* et le remplacement de l'oxyde de silicium (SiO_2) par des matériaux organiques (une réduction de 30% de la constante diélectrique) sont les principaux responsables de cette réduction. Nous sommes près des limites de ce que la technologie peut faire pour améliorer R et C. D'abord, le cuivre n'a pas de

*Le cuivre est 1.6 fois moins résistif que l'aluminium

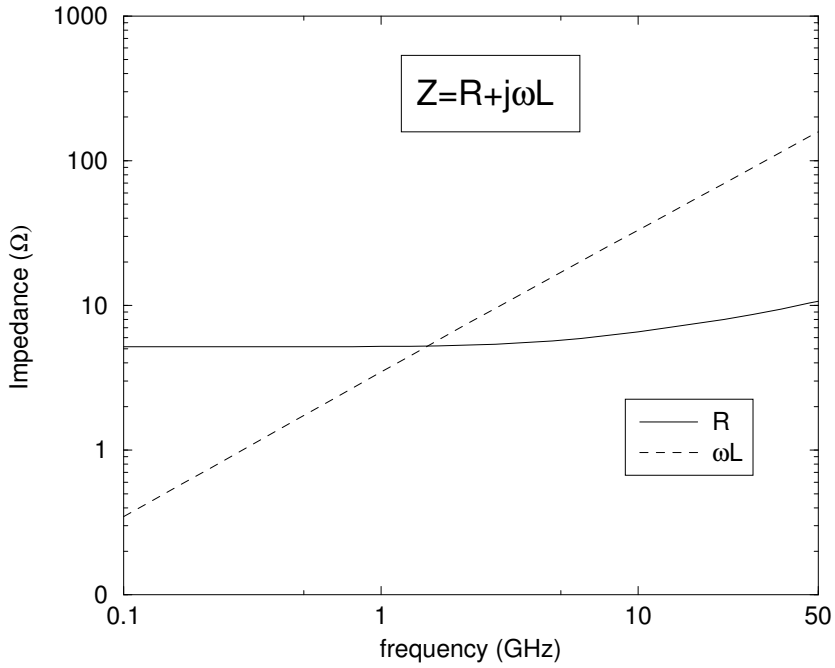


Figure 2: Résistance et réactance comme fonction de la fréquence pour un fil de Cu, avec une longueur d'un mm, avec une section transversale rectangulaire de dimensions 5 μm $\times$ 1 μm avec deux fils de masse comme retour, de la même longueur et de section transversale de 7 μm $\times$ 1 μm, les fils sont séparés de 5 μm.

concurrent et ensuite, il est très difficile de trouver des diélectriques qui puissent accommoder la croissance du cuivre avec une constante diélectrique plus petite et avec des propriétés thermiques meilleures que ce que nous avons aujourd'hui.

Si τ_{tr} décroît a chaque changement de technologie, le contenu maximal des fréquences dans la propagation des signaux augmente. Pour des fréquences supérieures à 1 GHz, la partie imaginaire de l'impédance, i.e. la réactance (la fréquence angulaire multipliée par l'inductance) d'un fil d'une longueur de l'ordre du millimètre, devient importante et il est alors nécessaire de la prendre en considération (voir Figure 2 pour clarification). La variation de la résistance avec la fréquence est aussi appréciable, il est donc nécessaire de prendre les deux phénomènes en considération pour une extraction et une simulation RL.

La fréquence n'est pas la seule variable qui déclenche la dominance des effets inductifs sur les effets de résistance et de capacité. La longueur des fils est aussi importante. Dans le chapitre 3, nous donnons les intervalles de longueur pour lesquels le

calcul d'inductance est important. L'intervalle de longueur des fils correspond à celui des interconnexions globales. C'est dans ce groupe d'interconnexions qu'une analyse soigneuse des effets inductifs doit être faite.

L'inductance dans les interconnexions est un phénomène incontournable. La bonne utilisation de l'inductance peut résulter en une performance optimale dans un circuit intégré. Nous abordons ce sujet dans le chapitre 6. La bonne caractérisation de l'inductance des fils est essentielle pour la conception et la validation des interconnexions globales dans un circuit intégré de haute performance.

Le sujet principal de cette dissertation est la caractérisation précise de l'inductance des fils en général. Cette caractérisation permettra la subséquente simulation, dans le domaine temporel et/ou fréquentiel, de circuits contenant des fils susceptibles à l'inductance et pour l'analyse du bruit entre les signaux.

A cet effet nous développons un code qui permet le calcul précis de l'inductance de segments arbitraires, placés en n'importe quelle disposition. Ce code de calcul est présenté dans le chapitre 2. Le contenu de ce chapitre n'ajoute rien de nouveau à ce qui est déjà connu, mis a part une nouvelle façon récursive de calculer la distance géométrique moyenne entre deux rectangles quelconques. Il est juste un compendium de formules connues dans la littérature, choisies par leur précision. Nous avons validé la précision et l'efficacité de ce simulateur avec la référence de la communauté FastHenry [6]. Ce simulateur est le noyau de calcul de tous nos outils pour l'extraction d'inductance parasite, ainsi que l'inductance intentionnelle, dans les circuits intégrés.

Dans le chapitre 3, nous développons une nouvelle approche pour l'extraction de l'inductance propre et mutuelle dans les interconnexions d'un circuit intégré. Notre nouvelle approche est significativement moins gourmande en temps de calcul que celle du PEEC (circuit équivalent avec des éléments partiels) [7] tout en gardant la même précision. Avec notre méthode, nous sommes capables de bien capturer le comportement monotone de la résistance et de l'inductance comme fonction de la fréquence. Nous avons même inclus le traitement nécessaire pour prendre en compte la non-uniformité du courant qui commence à se manifester dans les circuits intégrés digitaux à des fréquences de plus de 15 GHz. Une demande de brevet [8], déposée aux Etats Unis, couvre la technologie présentée dans ce chapitre.

Dans le chapitre 4, nous ajoutons à notre analyse l'étude des inducteurs passifs, tant pour l'impédance propre que pour l'impédance mutuelle. Une méthode d'extraction RLC est présentée dans ce chapitre. L'originalité de notre approche réside dans la

simplicité trouvée dans l'extraction de l'impédance mutuelle entre deux inducteurs (équation (4.29) qui permet son calcul efficace). Dans le chapitre nous présentons un exemple de validation. Un article dans une conférence de l'IEEE [9], une demande de brevet aux Etats-Unis [8] et un produit commercial en phase de test sont associés à ce travail. Le domaine d'application de cet outil est les circuits analogues de radio fréquences (RF): bluetooth, WiFi, téléphonie mobile, etc.

Dans le chapitre 5, nous dérivons une nouvelle expression (équation (5.41)) pour le délai d'une ligne de transmission RLC excitée par une rampe et avec une capacité de charge non nulle. Ce résultat est lié au travail d'extraction dans le sens qu'une ligne de signal avec ses fils de retour, dans un milieu homogène, peut être représentée comme une ligne de transmission. Finalement, dans le chapitre 6, nous présentons une application utile de l'inductance dans les circuits intégrés digitaux. Ce travail a été présenté en ICCAD, en IEEE's transactions on CAD et un brevet américain a été récemment octroyé [10–12]. Avant ce travail, la présence d'inductance dans un dessin était un motif de préoccupation. Nous démontrons que l'inductance peut être utilisée positivement pour assurer que la propagation des signaux dans les fils soit linéaire avec la longueur et non pas quadratique comme en RC. Un délai linéaire avec la longueur se traduit par une réduction dans le nombre de répéteurs et donc une réduction considérable de la consommation de puissance, qui est de nos jours, un véritable casse-tête.

Contributions de cette thèse

Les principales contributions de ce travail sont résumées ci-dessous:

- Un simulateur performant et précis pour le calcul de l'impédance partielle de configurations qui contiennent des fils avec une section transversale rectangulaire. Ce simulateur est le noyau de calcul des applications présentées dans cette thèse.

- Une nouvelle méthodologie pour l'extraction d'impédance, basée sur un traitement qui reconnaît correctement les boucles de circuits. Elle capture de façon précise les effets de proximité et de peau. Nous donnons un traitement valide pour des fréquences de l'ordre de 50 GHz. L'algorithme a été implémenté dans un outil commercial [13] qui a été prouvé précis et performant par de nombreux clients. Il a été utilisé dans une grande variété de problèmes: dessins en RF,

dessins digitaux complexes (e.g. processeur ARM) et “Systems on Chip (SoC)” (système sur une seule puce).

- Un outil pour calculer l’impédance propre d’un inducteur intentionnel et l’impédance mutuelle entre deux inducteurs intentionnels. L’outil inclut les effets RLC de l’inducteur de façon à pouvoir capturer sa fréquence de résonance et son facteur de qualité. Cet outil permet aux concepteurs d’expérimenter et d’optimiser le placement de plusieurs inducteurs dans une puce, de façon à minimiser le bruit parmi eux. L’implémentation commerciale de cet outil pour la vérification de bruit entre inducteurs est en train d’être lancée sur le marché.

- Une nouvelle expression pour le délai d’une ligne de transmission RLC excitée par une rampe et avec une capacité de charge non nulle (voir [10, 11]).

- Une méthode pour optimiser la vitesse de propagation d’un signal dans un fil d’horloge. La bonne utilisation de l’inductance est la clé de cette méthodologie. Elle propose une configuration composée par un fil de signal pris en sandwich par deux fils de masse. La méthode trouve des intervalles denses pour les paramètres de la configuration en sandwich qui assurent une vitesse de propagation optimale.

Chapter 1

Introduction

1.1 IC design

The advance in microelectronics constitutes one of the most marvelous technological feasts in the history of science and technology. Gordon Moore [1], while analyzing in 1965 cost projections for introducing new technologies, found an optimum when new processes (technology nodes) with smaller feature size (all dimensions scaled by the scale factor $\lambda \approx 0.7$) are introduced at a constant rate of once a year. The total number of transistors being proportional to the square of the inverse of the scale parameter, i.e. $1/\lambda^2 \approx 1/0.49 \approx 2$, would double every year. In 1975, the then chairman of the board of Intel, corrected a bit downward his observation regarding the introduction of new technology nodes, from one every year to one every two years, meaning transistor doubling every 24 months. Looking over a significantly longer time period, on microprocessors, doubling happens every two years. This empirical observation became a self fulfilling prophecy, see Fig. 1.1. Manufacturing companies and design houses target their investments in new technology so as to satisfy "Moore's law". What was initially projected to last nearly 10 years has survived 36 years of unfettered growth of an exponential nature as the figure demonstrates. The growth in the microelectronics industry is unequivocally characterized by this simple graph. The figure permits to understand two important results: The cost associated with implementing a function in microelectronics, decreases exponentially with time, sustaining the explosive growth of the technology. The second conclusion: The performance (speed) associated with the implemented function growths exponentially. The speed of operation of the Intel microprocessor chips represented in Fig. 1.1, identifiable by the chip clock's frequency;

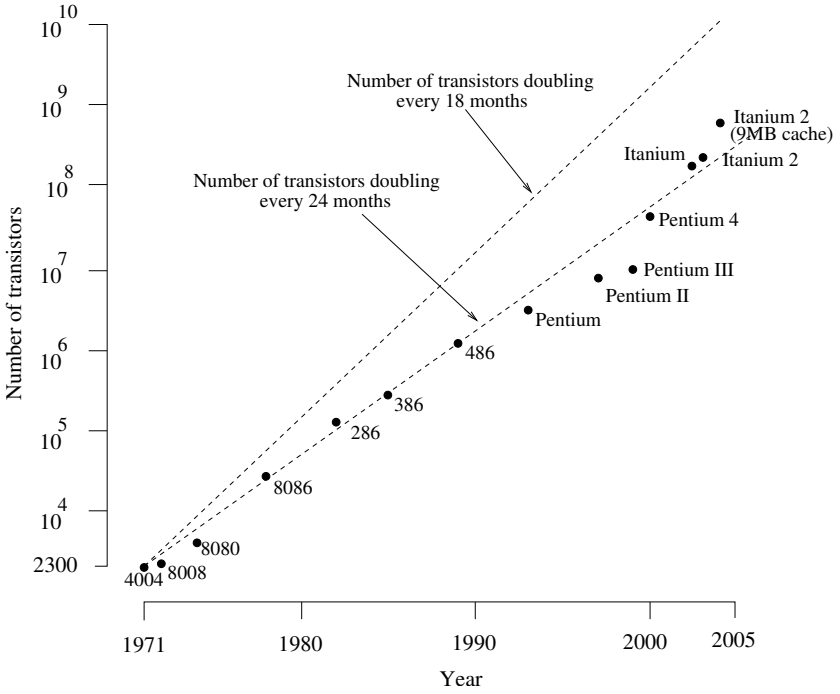


Figure 1.1: Number of transistors in a processor in a given year.

has been growing at a factor of two per generation. The reason for this performance increase is in fact simple: the speed of operation of a digital circuit, implemented as a synchronous system is accounted by the speed of the clock which controls the execution of the engine. The maximum speed of a clock is limited by the speed of propagation of a signal through a concatenation of a bounded number of logic functions, typically less than ten, between storage registers. The speed of propagation of a signal on a logic function, not counting for wires effects, is the sum of the transit times of the transistors on the logic function. The two basic ingredients that control function performance are transit time on a transistor and time delay on a wire.

Let us first examine the transistor time delay. The transit time τ_{tr} can be estimated as [3]:

$$\tau_{tr} = \frac{L^2}{\mu(V_{gs} - V_{thr})} \tag{1.1}$$

With L the channel length, μ the electron mobility, V_{gs} the gate voltage and V_{thr} the voltage threshold.

Under technology scaling (all dimensions reduced by $\lambda \approx 0.7$,) and applied voltages

reduced by the same scale, the transit time, using the previous equation, is reduced by λ. The transit time is the minimum time in which a charge placed on the gate of one transistor results in the transfer of a similar charge through the transistor's channel onto the gate of a subsequent transistor. The transit time evolved from 0.5 ns at 6 μm technologies around 1978 to 0.01 ns at 90 nm technologies in 2005 [2]. Transit time has been historically one key figure of merit in the unabated search for higher performance. To jump from transistor performance to system performance, we first impose a constraint, that will need to be revisited, that amounts to assuming a constant delay penalty introduced by wire delay, fully justifiable when the wires that connect the transistors are short. In that case, and this has been the rule rather than the exception, during the first 25 years of technology development, the minimum clock period for the implementation of a given function will be well approximated by the delay of a fixed number of logic stages (100 is a reasonable estimate) times τ_{tr} [3]. This simple argument explains the experimental fact that system delay δ_{System} scales with λ:

$$\delta_{System_i} = \lambda \delta_{System_{i-1}} \tag{1.2}$$

The exponential decrease of the system delay (λ is smaller than one), is source of the exponential increase in performance. To connect an exponentially increasing number of transistors with an exponentially growing number of wires is unavoidable. In the early days of silicon (Si) technology it was feasible to layout all signal wires as well as power and ground wires in at most two layers. As the transistor density increased it became necessary to slowly augment the number of metal layers needed for signal propagations (10 metal layers is doable at 65 nm in 2006). The chip layout, resembles the brain, with wires playing the role of synapses, a quasi two dimensional structure containing one very dense layer of transistor in one plane and a few planes of wires. The dimensionality of the system is that of a 2D plus epsilon. In the x-y plane, features (transistors) have dimensions of the order of the technology node (65 nm today) extended over length scale of the order of 1 cm (5 orders of magnitude larger), while in the vertical direction the active scale (not considering the substrate) is of the order of 10 μm. Manufacturing considerations, due to yield, put bounds on the chip linear dimensions, to be roughly upper limited to less than 15 mm on the side. It is not difficult to understand the two following features associated with Rent's rule on wirelength distribution on a chip [14]. Wires can be classified into two groups, one group providing the bulk of the interconnect

is local, with average length decreasing as λ and a second group providing for the interconnections among macro groups of transistors, whose average length does not scale [15]. At 90 nm technology node (2005), the average length of the first group of wires is in the neighborhood of 150 μm and accounts for over 90% of the wires. These local wires do not modify the basic assumption that the delay of the circuit is mostly determined by transistor delay. On the other hand, the global wires, in particular those whose lengths are larger than 1 mm (less than 1% of the total fraction) seriously affect the performance estimates. The wire delay associated with those wires impacts performance in a significant way and as such their electrical behavior needs to be known with sufficient accuracy. As it turns out, (we give quantitative bounds on chapter 3, equations (3.5) and (3.9)) global wires are the ones sensitive to inductance effects at frequencies starting at 1 GHz (this threshold is soft, and given as a qualitative estimate.) It is not surprising to understand why in the Integrated Circuit (IC) world, the concern about electromagnetic effects associated with inductance were not manifest until very recently, since they demand long wires and high frequency propagation, both factors that are beginning to show up at current nodes.

To further estimate the importance of wire propagation on system delay, it is useful to consider the following picture of a wire: For short wires, and anything shorter than 100 μm qualifies as such, an isolated wire segment can be treated as a resistor coupled to a capacitor to ground. Rudimentary circuit theory tells us that a pulse applied at one end of the wire, propagates to the other end with a time constant given by

$$\tau_{sig} = RC \tag{1.3}$$

with R and C the resistance and capacitance of the wire respectively. These values are computed using the following expressions:

$$R = \rho \frac{L}{w.t} \tag{1.4}$$

and

$$C = \varepsilon \frac{A}{d} \tag{1.5}$$

where L, w and t are the wire's length, width and thickness, respectively. The constant ρ is the resistivity of the wire, ε the relative dielectric permittivity of the media, d is a representative distance to a neighbor conductor and A is the area facing the neighbor

Isolated	Dense	Local	Global
$\tau_{sig} = \rho\varepsilon\frac{L^2}{t.d}$	$\rho\varepsilon\frac{L^2}{p.w}$	τ_{sig} constant	$\tau_{sig} \propto \frac{1}{\lambda^2}$

Table 1.1: Wire delay

conductor.

To get an order of magnitude of the parameters, we distinguish two types of wires, isolated wires whose capacitance is dominated by coupling to a large fixed plane such as substrate, and tightly coupled wires, whose capacitance is dominated by coupling to its neighbor.

The capacitance for these two kinds of wire is given by:

$$C_{isolated} = \varepsilon\frac{L.w}{h} \tag{1.6}$$

with h the distance to the fixed plane.

$$C_{coupled} = \varepsilon\frac{L.t}{p} \tag{1.7}$$

with p the wire separation.

Notice that τ_{sig} in this rudimentary calculation is scale invariant for an isolated wire. In table 1.1 the wire delay for the different kinds of wire is presented.

Under scaling, therefore, for a local (shrinking) wire RC remains constant, while for a global wire of fixed length the delay growths quadratically with scaling, leading to a fast exponential growth. The best one can do technologically for these global wires is either find a three dimensional mapping to ensure close proximity or do not scale the vertical dimensions of the upper metal layers. Today's technologist apply the last recipe in production while doing R&D in fully three dimensional chips. For a local wire of 100 μm of minimum width $\tau_{tr} > \tau_{sig}$ while for a 1 mm wire at 250 nm technology (1997) the inverse is true. A more complete relative picture of this phenomena is shown in Fig. 1.2. There are other factors that make this simple picture rather approximate, but do not change the qualitative behavior that emerges from its simplest incarnation.

Signal contribution to system delay grows in importance with scaling, becoming the dominant factor in limiting the performance of digital systems for technology nodes since 250 nm (1997) causing a major interconnect crisis.

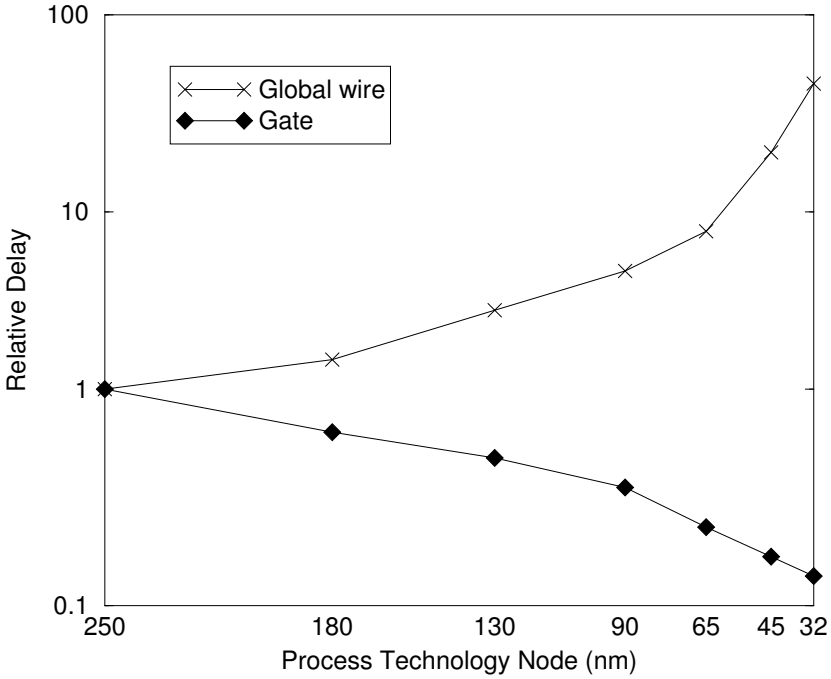


Figure 1.2: Delay relative to 250 nm node of global wiring and gate versus feature size [2].

Year	2005	2010	2015
On-chip maximum frequency (GHz)	5.2	15.1	33.4

Table 1.2: On-chip frequency limit per technology node based on fanout of four inverter delay. Projections made by the ITRS 2005 [2]

This crisis instigated designers to include buffers as signal boosters in the path of long critical wires, a not altogether desirable proposition, since these buffers consume a large fraction of the power budget, nearly 60% at last count. On the verification side the crisis lead to the the need to compute accurately the total and coupling capacitance of the interconnect. As such, the crisis led to important technology developments at Mentor Graphics on RC extraction [4].

Our interest in this thesis is in a follow up concern, that we proceed to explain: Consider signal propagation in wires, driven by transistors, on digital systems. The signal output of a transistor, input to a wire, is that of an imperfect switch from a low voltage (a logic zero) to a high voltage (a logic one). This transition is well approximated by a ramp whose rise time is τ_{tr}. The Fourier transform of a ramp signal contains appreciable amplitude up to a frequency $f_{max} \approx \frac{1}{\pi\tau_{tr}}$.

In table 1.2 we show f_{max} for current and future technology nodes. Notice that f_{max} scales as $1/\lambda$.

For frequencies up to roughly 1 GHz, signal propagation on a wire is well approximated as arising from the contributions due to capacitance and resistance of the multiple segments that make a wire. The superposition of different segments, each one represented by a RC lumped element, becomes in the continuum limit the one dimensional diffusion equation. Approximate solutions for the delay of such systems under a step function input are known [5].

Technology has contributed to diminish the delay due to wires dominated by RC. The replacement of aluminium (Al) by copper (Cu)* and the replacement of SiO_2 by organic compounds of smaller dielectric constants (a 30% decrease of ε) are the main components. We are close to the limits of what technology can do to improve R and C. First, Cu has no competitor, and, second, it is very difficult to find insulators that can accommodate Cu growth with smaller dielectric constant and compatible thermal properties than what we have today.

*Copper is 1.6 times less resistive than Aluminum.

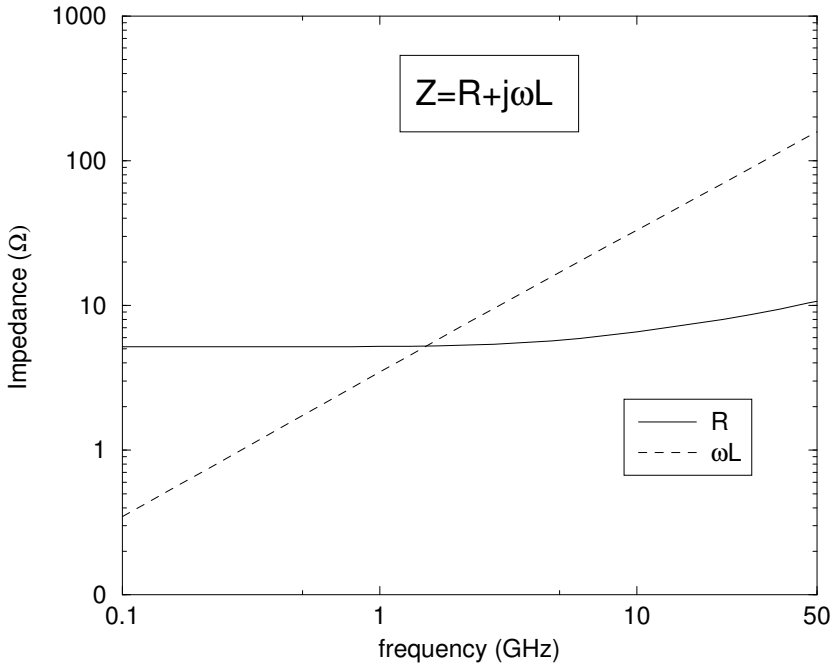


Figure 1.3: Resistance and reactance as a function of frequency for a copper wire, 1 mm long, with rectangular cross-section of 5 μm $\times$ 1 μm and two return ground wires of same length and rectangular cross-section of 7 μm $\times$ 1 μm, with a 5 μm wire separation.

As τ_{tr} decreases with scaling, the maximum frequency content on wire propagation increases. For frequencies above 1 GHz, the reactance part of the serial impedance (reactance is equal to angular frequency times inductance-ωL) of a millimeter scale wire segment becomes appreciable and needs to be included. See Fig. 1.3 for clarification. The resistance variation with frequency is appreciable, both phenomena need to be accounted for in RL extraction and simulation.

Frequency is not the only variable that impacts the onset of inductance effects on and above resistance and capacitance effects. The length of the wire also matters. In chapter 3, we show the bounds on lengths appropriate for inductance calculations (equations (3.5) and (3.9)). It is the regime of wire lengths corresponding to global interconnect, where a careful analysis of inductance effects needs to be undertaken.

Technology plays a secondary role in localizing or mitigating inductance effects. We can quote one isolated instance of using manufacturing technology to this end. During the design of a DEC Alpha superscalar RISC microprocessor [16], ground planes were

added in between signal planes so as to reduce the area of the circuit loops and hence the inductance of the signals. Including ground planes in a design is very expensive and interferes with routing, so this methodology was rapidly abandoned.

Inductance in interconnect is an unavoidable phenomena and if well used, can benefit the power dissipation for a given performance of an IC. We shall address this application domain in chapter 6. Good characterization of wire inductance is essential during the design and validation of global wiring for high performance IC's.

The topic of this dissertation is the accurate characterization of wire inductance for downstream simulations of circuits containing wires sensitive to inductance.

This we do by first developing a code that permits the accurate computation of inductance for arbitrary segments immersed in a layout, in whatever relative placement and orientation under uniform current distribution. This is the topic of chapter 2. The content in this chapter, is not original, with the exception of a new method for computing the geometric mean distance in between arbitrarily oriented segments in a plane. It is mostly a compendium of published formulae selected for their accuracy, that we validated against the 3D field solver FastHenry [6]. The simplicity and efficiency of the resulting code is demonstrated initially with a calibration against toy examples, and later validated with large designs from Industry. The resulting simulator, is the workhorse that permitted us to address the impedance extraction of wires in an IC.

In chapter 3, we develop a consistent, accurate and computationally inexpensive approach to self and mutual impedance extraction of interconnects. System complexity, in addition to accuracy is a figure of merit that needs to be considered. The key difference between the problem treated in chapter 2 and the one in chapter 3 is one of size. In the core engine, described in chapter 2, we consider configurations consisting of at most a few tens of well identified wire segments. In chapter 3, we attack the problem with three to four orders of magnitude more segments, and unidentified current loops. Prior to our work there were two contributing groups to inductance extraction, one in industry, Sequence, whose results are patented [17] and the other group from Columbia University [18] implemented by one of our competitors Cadence. Both groups use the loop inductance formalism. The resulting approaches and code are oversimplifications of the problem that lead to large errors in the computation of inductance. For this reason, most of the academic community, embarked in a different approach based on the Partial Element Equivalent Circuit (PEEC) method due to Ruehli [7]. The PEEC formalism is discussed in Chapter 3 and its pitfalls are shown. The alternative formalism that we

develop in chapter 3 is computationally much less expensive than the PEEC alternative, significantly more stable, while equally accurate. We solve the problem of capturing the correct frequency dependence of the inductance and resistance extraction, one that fully accounts for proximity effects as function of frequency, whose presence materializes in the regime of 4-15 GHz. Furthermore, we correctly generalize our treatment to incorporate nonuniform current distributions as needed to model the skin effect, that starts manifesting in digital IC's at frequencies near 15 GHz. Validation to field solver simulations and experimental data is included. A US patent application [8] covers the description of the method presented in this chapter.

In chapter 4, we extend our analysis to the study of passive inductor devices, both for self and mutual impedance computations. An RLC extraction method is presented. The originality of the approach lies in the simplicity encountered in the extraction of the mutual impedance among two inductors (equation (4.29)) permitting efficiency into the implementation. A validation example is shown in this chapter. An IEEE conference paper [9], a patent application [8] and a product in beta release are associated with this work. The domain of application is Radio Frequency (RF) analog circuits as used in telecommunications, up and including cellular phones.

In chapter 5, we derive an original equation (equation (5.41)) for the delay of an RLC transmission line under a ramp excitation, with a finite load capacitance. This work was published on IEEE [10, 11]. This result is connected to the extraction work by the simple fact, that in a homogeneous media, a configuration consisting by a signal wire and its parallel return paths can be represented by a transmission line. Signal propagation on these lines is at the core of our interest, ergo the importance of the derived delay expressions. In chapter 6, we present a useful application of inductance in digital IC's. This work has been published in ICCAD, IEEE's transactions on CAD, and a US patent has been awarded [10–12]. Prior to this work, the presence of inductance in digital systems was taken as a concern. What we demonstrate in this work is the feasibility to propagate electromagnetic waves in the dielectric at the speed of light in the medium, with delay linear with the length, instead of quadratic as in RC diffusion, and as such, needing significantly less power injection, a very important concern at 65 nm and beyond. Short distance propagation with transmission lines was known and understood before this work, and considered useful for short distance propagation. Our work permits a large jump into multiple millimiter length scale with complicated route configurations. This line of work is in progress.

1.2 Inductance extraction in IC

Maxwell solvers have been developed for a variety of applications. Some of them have been validated in Printed Circuit Boards (PCB), e.g. HFSS [19], Momentum [20], Sonnet [21], etc. Extensions to IC's are nearly beyond the realm of the possible. The number of variables rapidly exceeds many millions for even the simplest problems. A localized circuit representation with parameters, which are frequency dependent in the regime of interest, determined with field solver accuracy is a realizable characterization to the study of electromagnetic effects in an IC. At low frequencies and for simple geometrical features resistance computations are straightforward. Calculation at a system level is simply a task of breaking each wires into rectangular shapes and applying well known formulae and the most computationally expensive part is that associated with keeping track of the connectivity [4]. At higher frequencies resistance calculations cannot be separated from inductance calculations. Capacitance, being a localized phenomena, is computable using surface methods by considering a small window around each conductor. The shielding to electric field penetration in the quasistatic case, provided by the presence of other conductors justifies this approach. There is a number of well developed capacitance engines, at the field solver level (FASTCAP [22]) and at the system level (Mentor xRC [4]). Inductance, in the intermediate frequency region does not benefit from shielding. Inductance is a property of current loops. It is not at all easy to recognize which are the constitutive loops within an IC. For instance, looking at the SEM photograph of a typical interconnect in Fig. 1.4 one can easily realise how difficult this task is. This ambiguity led to the development of an alternative treatment in which the computation of the electromagnetic parameters -resistance, capacitance and inductance- is done in terms of the contributions of each and every segment in a layout, without distinguishing which segment is associated with which loop. This is the Partial Element Equivalent Circuit (PEEC) model [7]. Calculating the contribution of each wire segment in an IC layout and furthermore, computing the inductance and capacitive coupling among all of them, results in a netlist that is unmanageable by the most powerful circuit simulators. Neglecting magnetic couplings, even the smallest ones, in order to reduce the size of the netlist, may result in a loss of stability of the circuit. Plenty of effort has been invested so as to find methods in which inductive coupling between far wires in a PEEC formalism can be safely neglected without affecting stability. The results today are meager.

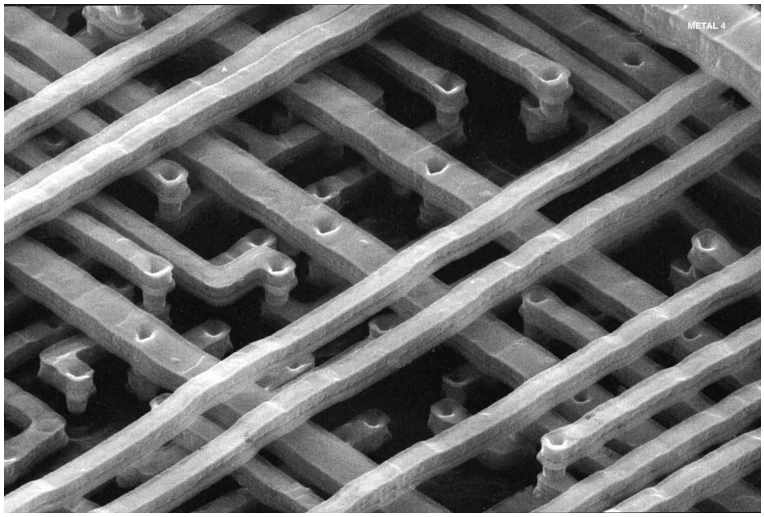


Figure 1.4: SEM photograph of a typical interconnect.

A different approach to inductance and resistance extraction is within the loop formalism. One needs to recognize the return path of each signal wire in a layout. Previous work considered as return candidates the two closest ground wires to any signal [23]. The results are highly inaccurate and miss completely the significant variations in resistance and inductance in the frequency range of two to fifteen GHz, today explorable by the technology. We present a realistic interpretation for the loop identification, one that realizes that the current distribution for the return path as well as the choice of participants is frequency dependent. We can evaluate it from first principles. Both the correct frequency behavior for R and L are reproduced. Moreover, we can handle the skin effect at higher frequencies, in signal wires and large conduction planes, with limited increase in computational demand. Our approach is valid up to 50 GHz, sufficient for design exploration over the next decade.

1.3 Contributions

The main contributions presented in this thesis are summarized as follows:

- A fast and accurate partial impedance simulator for configurations containing wires with rectangular cross-section. This tool is the calculation kernel for the applications presented in this work.

- A new methodology (algorithm and code) for impedance extraction, based on a loop treatment that correctly identifies loop configurations. It captures accurately proximity and skin effect. We provide a treatment valid up to frequencies and distances where radiation effects need to be considered, roughly 50 GHz. The resulting algorithms have been incorporated into a commercial tool [13] and validated by multiple customers for accuracy and performance. The commercial tool has been used for validation of Radio Frequency (RF) designs, complex digital designs, (e.g., ARM microprocessors.) and Systems on Chip (SoC).

- A 3D electromagnetic tool to compute self impedance of intentional inductors and mutual impedance between two intentional inductors. The tools includes RLC effects so as to capture inductor's self resonance frequency and quality factor. This tool permits the designer to experiment and optimize the placement of inductors so as to minimize the magnetic noise among them. This tool is being released as a commercial tool for noise checking [24].

- An accurate formula for time delay of a transmission line fed by a signal with nonzero rise time including corrections due to finite load capacitance, See [10, 11].

- A method for optimizing the signal propagation speed of a clock wire. The use of inductance is paramount. It proposes a tree configuration consisting of the clock signal wire sandwiched between two parallel ground wires. Ranges of values for the physical parameters of the ground-signal-ground layout are found such as to ensure transmission line behavior for signals propagating on the configuration for short τ_{tr}. These results have been published in [10, 11] and a US patent has been awarded [12].

1.4 Thesis outline

This thesis is organized as follows:

In chapter 2, we present a quasimagnetostatic electromagnetic volume formulation and its application to impedance simulation. Resistance and inductance expressions collected from different sources are identified, and used in the implementation of an impedance simulator.

In chapter 3, we present an impedance extraction methodology based in a novel extension of the loop treatment. The method permits extraction in a broad regime of frequencies and has been amply validated.

In chapter 4, we present a natural simplification to compute the mutual impedance between two intentional inductors that we insert in a quasi electromagnetic treatment used for self impedance characterization and noise analysis.

In chapter 5, a new expression for the time delay of a transmission line fed by a signal with nonzero rise time and finite load capacitance is derived.

In chapter 6, a method of optimizing the signal propagation speed on a SBHT is proposed as a method for clock distribution in high performance IC applications.

In Chapter 7, we include some concluding remarks.

1.5 Mentor Graphics

This work has been carried out in its totality at Mentor Graphics. Mentor Graphics is a US company that provides engineering solutions to the design and manufacturing of IC's and PCB. The solution space includes software, and hardware software combinations, and the overall domain is usually referred to as Computer Aided Design of Electronic Circuits (CAD) or Electronic Design Automation (EDA). Mentor Graphics, in business since 1982, is the third largest provider of CAD products in the Electronic Industry, capturing twenty percent of the total market of four billion US dollars ($\$4\times10^9$). The total number of players in this industry exceeds 60. Mentor Graphics headquarters are located in Oregon, USA. It has nearly 4000 employees distributed over more than 20 countries with 28 engineering sites worldwide. Mentor Graphics spends well over 20% of its raw income in R&D and engineering activities. The company is structured into 5 divisions according to technology segments. Scalable Verification, Design to Silicon, and Integrated PCB-FPGA (Field Programmable Gate Arrays) Systems Design are the three major Areas of focus. In the analog mixed signal domain as well as in the high frequency parasitic extraction, the Mentor center of excellence is located in Montbonnot, France. Our team develops technology for implementation in verification tools, known in the market place as Calibre suite of tools, globally the number one contender in the verification market, casting nearly 50% of a total verification market of: USD 450M. I have been a student member of the R&D team working in inductance extraction since 2001. I have been recently invited and accepted a staff position within the group.

Chapter 2

A 3D impedance simulator

Simulateur d'impédance 3D

Résumé

Dans ce chapitre nous présentons, dans un premier temps, une brève discussion sur les équations électromagnétiques qui sont la base de notre traitement. Dans la deuxième partie, les équations de la première partie sont assemblées dans un simulateur d'impédance. Ce simulateur sert de noyau de calcul pour les applications présentées dans les autres chapitres de cette thèse. La précision du simulateur ainsi que sa performance, sont comparées à un simulateur d'impédance utilisé dans la communauté comme le standard de référence.

2.1 Introduction

This chapter is divided into two parts: the first one where the fundamental equations in electromagnetism and their derivation to impedance simulation applications, are presented; the second part, where the equations of the first part are put together into an implementation of an impedance simulator. The computational core of this simulator is the main building block of the applications presented in the other chapters of the thesis.

In detail, the chapter is divided as follows:

In section 2.2 a brief description of the electromagnetic physics in conductor closed circuits is presented. Maxwell's equations in the magneto-quasistatic approximation

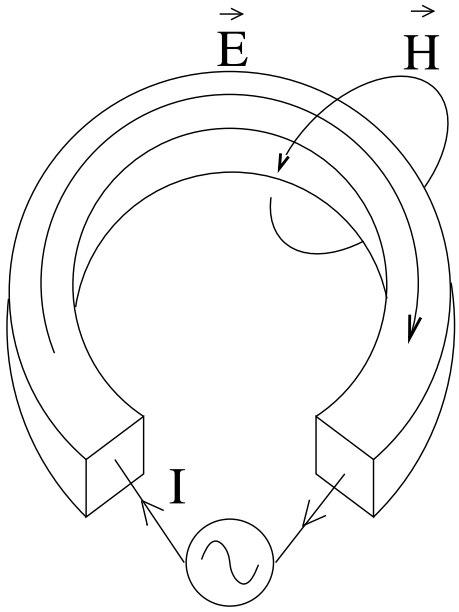


Figure 2.1: A conductor loop

(MQS) are discussed. In the same section, we apply the MQS equations to the unphysical case of a closed circuit composed of one rectilinear conductor. The equations are further generalized to n-segment circuits. This is the basis of the partial inductance treatment. We caution the reader that what looks as an unphysical application of Maxwell's equations is in fact a mathematical trick useful to break down the entire problem into subproblems that are easier to understand and, hence, easier to solve. In section 2.3 we compile well known expressions, some of them analytical, other approximations, for the solution of the MQS equations in the low frequency domain for the particular cases that interest us in this thesis. In particular, we present expressions for the partial self and mutual inductance of rectilinear conductors.

In section 2.4 we present our implementation of a core for impedance calculation. This core uses the expressions presented in section 2.3. At the end of this section we compare accuracy and performance of our implementation against the community's golden standard FastHenry [6].

2.2 Basic concepts

Consider a time varying current I circulating through a closed circuit made up of a conductor (Fig. 2.1). The conductor is surrounded by a dielectric. The flowing of this current generates an electric field $\vec{E}$ and a magnetic field $\vec{H}$. Fields $\vec{E}$ and $\vec{H}$ are related through the Maxwell's Equations which in sinusoidal steady state, for an angular frequency ω, are given by [25]:

$$\vec{\nabla} \times \vec{E} = -j\omega\mu\vec{H} \tag{2.1}$$

$$\vec{\nabla} \times \vec{H} = j\omega\varepsilon\vec{E} + \vec{J} \tag{2.2}$$

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon} \tag{2.3}$$

$$\vec{\nabla} \cdot \mu\vec{H} = 0 \tag{2.4}$$

Where $\vec{J}(\vec{x})$ is the current density at the source $\vec{x}$ and $\rho(\vec{x})$ is the charge density; μ and ε are the magnetic permeability and dielectric permittivity of the material at the source, respectively.

The current distribution is null outside the conductor. The charge density is null inside the conductor but not on its surface. For non-ferromagnetic material, the magnetic permeability is equal to that of free space, i.e. $\mu_0 = 4\pi \times 10^{-7}$ H/m. The dielectric permittivity of the medium is proportional to the permittivity of free space, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m, i.e. $\varepsilon = \varepsilon_r\, \varepsilon_0$ with the coefficient ε_r generally referred to as the relative dielectric permittivity or dielectric constant (e.g. $\varepsilon_r \approx 11.9$ for Si, $\varepsilon_r \approx 3.9$ for SiO_2). It is generally accepted to consider $\varepsilon_r = 1$ inside the conductor.

In addition, within the conductor's homogeneous media, the use of Ohm's law is applicable, that written in three dimensional form reads:

$$\vec{J}(\vec{x}) = \sigma\vec{E}(\vec{x}) \tag{2.5}$$

where σ is the conductivity of the material the conductor is made off.

For an observation point $\vec{x}$ inside the conductor, we substitute (2.5) in (2.2). For high conductivities, e.g. copper ($\sigma = 5.8 \times 10^7\, \mho/m$), the term $\sigma\vec{E}$ is several orders of magnitude larger than the counterpart $\omega\varepsilon\vec{E}$, even for frequencies of the order of 100 GHz which are beyond the frequency limit of this study. For this reason it is safe to neglect this term. This rends (2.2) into

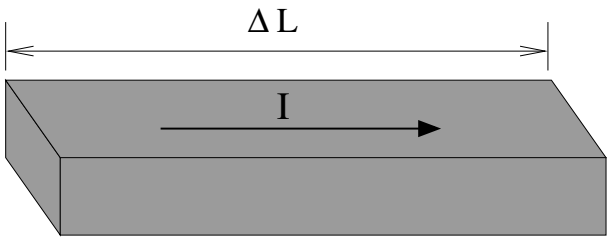


Figure 2.2: A conductor segment with rectangular cross-section.

$$\vec{\nabla} \times \vec{H} = \vec{J} \tag{2.6}$$

The term $\omega\varepsilon\vec{E}$ that is neglected corresponds to the displacement current inside the conductor. By neglecting this term we fall into the magneto-quasistatic domain [25].

A solution to (2.1) together with (2.6) is given by

$$\vec{E}(\vec{x}) = -\frac{j\omega\mu}{4\pi} \int_{\bar{\Omega}} \frac{\vec{J}(\vec{x'})}{\|\vec{x} - \vec{x'}\|} d\Omega' - \vec{\nabla} V(\vec{x}) \tag{2.7}$$

with $V(\vec{x})$ referred to as the scalar potential and $\bar{\Omega}$ is the volume of all conductors.

Equating (2.7) and (2.5) results in the relationship

$$\frac{\vec{J}(\vec{x})}{\sigma} + \frac{j\omega\mu}{4\pi} \int_{\bar{\Omega}} \frac{\vec{J}(\vec{x'})}{\|\vec{x} - \vec{x'}\|} d\Omega' = -\vec{\nabla} V(\vec{x}). \tag{2.8}$$

Expression (2.8) in the quasistatic domain is supplemented by the current conservation equation

$$\vec{\nabla} \cdot \vec{J} = 0. \tag{2.9}$$

For a given V we can compute $\vec{J}$ by solving equation (2.8) together with (2.9). We search a discretization of the unknown current distribution $\vec{J}(\vec{x})$. Once $\vec{J}$ is known, the electro-magnetic fields $\vec{H}$ and $\vec{E}$ can be computed. In the next section we explain in detail a widely used discretization technique.

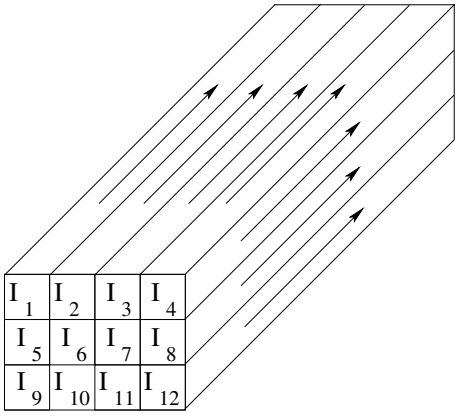


Figure 2.3: A conductor of rectangular cross-section partitioned into filaments ($m = 12$).

2.2.1 2D Volume discretization for an isolated conductor

Divide the conductor in Fig. 2.1 into short segments. Each segment can be thought of as a straight conductor with rectangular cross-section as in Fig. 2.2. We consider a perfect ground below the conductor. We take the conductor shorted to a perfect ground at one end. If we apply a sinusoidal input voltage between one end of the conductor and the perfect ground, current flows inside this closed circuit. Neglecting displacements currents, we make the approximation that the current inside the conductor flows parallel to its walls along the direction of the applied potential difference, i.e. along the conductor's longitudinal direction (Fig. 2.2). The electromagnetic fields generated by this current can be computed by solving (2.8) together with (2.9).

We break the conductor into m rectilinear filaments of finite volume and constant cross-section as in Fig. 2.3. We denote the longitudinal direction of filament k as $\hat{\ell}_k$. With this discretization, current distribution inside each filament can be considered uniform and hence, the unknown current distribution inside filament k is given by

$$\vec{J}(\vec{x}) = \frac{I_k}{A_k}\,\hat{\ell}_k \tag{2.10}$$

with I_k the unknown current inside filament k and A_k its transverse area. Defining the delta functions:

$$\delta_k(\vec{x}) = \begin{cases} 1 & \text{if} \quad \vec{x} \in \text{Fil}_k \\ 0 & \quad\;\; \text{else} \end{cases} \tag{2.11}$$

the current distribution at any point of the conductor can be expressed as the finite sum:

$$\vec{J}(\vec{x}) \approx \sum_{k=1}^{m} \frac{I_k}{A_k} \delta_k(\vec{x})\, \hat{\ell}_k \tag{2.12}$$

We substitute (2.12) in (2.8). By linearity (2.8) becomes

$$\sum_{k=1}^{m} \left[\frac{I_k \delta_k(\vec{x})\, \hat{\ell}_k}{\sigma A_k} + \frac{j\omega\mu\, I_k}{4\pi A_k} \int_{\bar{\Omega}_k} \frac{\hat{\ell}_k}{\|\vec{x} - \vec{x'}\|}\, d\Omega' \right] = -\vec{\nabla} V(\vec{x}). \tag{2.13}$$

where $\bar{\Omega}_k$ represents the volume of filament k.

Consider the inner product of two functions f and g whose domain is in the space $\mathcal{X}$:

$$< f, g >= \int_{\mathcal{X}} f\ g\ dx \tag{2.14}$$

Take as weight functions the set of functions $w_i(\vec{x})$ such that

$$w_i(\vec{x}) = \frac{\delta_i(\vec{x})\hat{\ell}_i}{A_i}. \tag{2.15}$$

We use the method of moments [26]: For $i = 1, \ldots, m$, we apply the inner product between the weight function w_i and both sides of the inhomogeneous equation (2.13). For the left hand side, the real part of the resulting expression is:

$$\int_{\Omega} \left[\sum_{k=1}^{m} \frac{I_k \delta_k(\vec{x})\, \hat{\ell}_k}{\sigma A_k} \right] \cdot \frac{\delta_i(\vec{x})\hat{\ell}_i}{A_i}\, d\Omega \tag{2.16}$$

with Ω the union of all filament volumes. This integral is equal to zero outside the volume of filament i because of the function δ_i, we can reduce the integration domain to $\bar{\Omega}_i$. In this domain of integration the sum in (2.16) is nonzero only when $k = i$, this reduces to

$$\begin{aligned}\int_{\bar{\Omega}_i} \frac{I_i\,\hat{\ell}_i}{\sigma A_i}\cdot\frac{\hat{\ell}_i}{A_i}\,d\Omega &= \frac{I_i}{\sigma A_i^2}\int_{\bar{\Omega}_i} 1\,d\Omega \\ &= \frac{I_i}{\sigma A_i^2}(A_i l_i) \\ &= \frac{l_i I_i}{\sigma A_i}\end{aligned} \tag{2.17}$$

where l_i is the length of filament i.

With the same reasoning regarding the delta functions, the imaginary part of the inner product between the weight function w_i and the left hand side of the inhomogeneous equation (2.13) results in

$$\omega\sum_{k=1}^{m}\left(\frac{\mu}{4\pi A_i A_k}\int_{\bar{\Omega}_i}\int_{\bar{\Omega}_k}\frac{\hat{\ell}_i\cdot\hat{\ell}_k}{\|\vec{x}-\vec{x'}\|}\,d\Omega'\,d\Omega\right)I_k \tag{2.18}$$

The resulting inhomogeneous equation is:

$$\left(\frac{l_i}{\sigma A_i}\right)I_i + j\omega\sum_{k=1}^{m}\left(\frac{\mu}{4\pi A_i A_k}\int_{\bar{\Omega}_i}\int_{\bar{\Omega}_k}\frac{\hat{\ell}_i\cdot\hat{\ell}_k}{\|\vec{x}-\vec{x'}\|}\,d\Omega'\,d\Omega\right)I_k = -\int_{\bar{\Omega}_i}\vec{\nabla}V(\vec{x})\cdot\frac{\hat{\ell}_i}{A_i}\,d\Omega \tag{2.19}$$

The right hand side of (2.21) can be rewritten as

$$\begin{aligned}\int_{\bar{\Omega}_i}\vec{\nabla}V(\vec{x})\cdot\frac{\hat{\ell}_i}{A_i}\,d\Omega &= \int_{A_i}\frac{1}{A_i}\left(\int_{l_i}\vec{\nabla}V(\vec{x})\cdot\hat{\ell}_i\,dL\right)dA \\ &= \frac{1}{A_i}\int_{A_i}(V_b - V_a)\,dA = \bar{V}_b - \bar{V}_a\end{aligned} \tag{2.20}$$

with functions V_a and V_b defined as the potential on the points in the filament's end faces and $\bar{V}_a$ and $\bar{V}_b$ are the voltage at the end faces.

Replacing (2.20) in (2.19) results in:

$$\left(\frac{l_i}{\sigma A_i}\right) I_i + j\omega \sum_{k=1}^{m} \left(\frac{\mu}{4\pi A_i A_k} \int_{\bar{\Omega}_i} \int_{\bar{\Omega}_k} \frac{\hat{\ell}_i \cdot \hat{\ell}_k}{\|\vec{x} - \vec{x}'\|} \, d\Omega' \, d\Omega \right) I_k = \bar{V}_b - \bar{V}_a \tag{2.21}$$

We can write (2.21), for $i = 1, \ldots, m$, as a $m \times m$ linear system of the form:

$$\mathbf{ZI} = \mathbf{V}, \tag{2.22}$$

With $(\mathbf{Z})_{i,k}$ given by:

When $i = k$ (called the partial self impedance of filament i):

$$(\mathbf{Z})_{i,i} = \frac{l_i}{\sigma A_i} + \frac{j\omega\mu}{4\pi {A_i}^2} \int_{\bar{\Omega}_i} \int_{\bar{\Omega}_i} \frac{\hat{\ell}_i \cdot \hat{\ell}_k}{\|\vec{x} - \vec{x}'\|} \, d\Omega' \, d\Omega \tag{2.23}$$

and when $i \neq k$ (called the partial mutual impedance between filament i and filament k):

$$(\mathbf{Z})_{i,k} = \frac{j\omega\mu}{4\pi A_i A_k} \int_{\bar{\Omega}_i} \int_{\bar{\Omega}_k} \frac{\hat{\ell}_i \cdot \hat{\ell}_k}{\|\vec{x} - \vec{x}'\|} \, d\Omega' \, d\Omega \tag{2.24}$$

The real part in (2.23) is the resistance of the filament and the imaginary part is the reactance. The reactance divided by ω is known as the partial self inductance of the filament. In (2.24), the reactance divided by ω is known as the partial mutual inductance between two different filaments.

The vector $\mathbf{I}$ corresponds to the currents flowing through the m filaments and $\mathbf{V}$ is the difference between the average potential of the two ends of each of the m filaments.

We apply a sinusoidal potential of v_{io} volts at one end of the conductor and ground the other end. From (2.20) we are free to consider the same potential difference v_{io} for all filaments. In other words, the corresponding system (2.22) is written as:

$$\mathbf{ZI} = v_{io}\mathbf{u_m}, \tag{2.25}$$

with $\mathbf{u_m}$ being the vector of dimension m with all entries equal to one. For non-singular Z, the vector of filamentary currents is equal to

$$\mathbf{I} = v_{io} \begin{pmatrix} \sum_{k=1}^{m} (\mathbf{Z}^{-1})_{1,k} \\ \vdots \\ \sum_{k=1}^{m} (\mathbf{Z}^{-1})_{m,k} \end{pmatrix}, \tag{2.26}$$

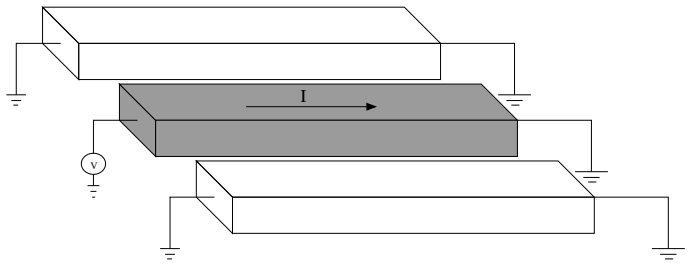


Figure 2.4: A n-conductor configuration ($n = 3$). A sinusoidal is applied to one conductor while the others are set to ground.

with $(\mathbf{Z}^{-1})_{i,k}$ being the element ik of the matrix Z^{-1}.

The total current going through the conductor is equal to the sum of the currents going through each filament:

$$I = \sum_{i=1}^{m} I_i = v_{io} \sum_{i=1}^{m} \sum_{k=1}^{m} (\mathbf{Z}^{-1})_{i,k}. \tag{2.27}$$

This equation can be written as

$$\left(\sum_{i=1}^{m} \sum_{k=1}^{m} (\mathbf{Z}^{-1})_{i,k} \right)^{-1} I = v_{io}. \tag{2.28}$$

By Ohm's law, the coefficient multiplying the current in the left hand side of (2.28) is the total input/output self impedance of the conductor.

We resume: to compute the self impedance of a conductor, we first break it into m filaments, we compute the $m \times m$ partial impedance matrix Z, we invert it and sum its entries. The self impedance is then the inverse of this sum.

2.2.2 The n-conductor impedance matrix

Consider a system of n rectilinear conductors with constant cross-section (for example Fig. 2.4 with 3 conductors). Each conductor is partitioned into m_i filaments, with $i = 1, \ldots, n$. In order to avoid confusions we use the index k_c when referring to conductors and the index k_f when referring to filaments, i.e. $k_c = 1_c, \ldots, n_c$ and $k_f = 1_f, \ldots, m_f$.

Equation (2.21) being local to the volumes of the filaments can be generalized to the n-conductor case by considering all conductors' filaments together in a single $\mathbf{Z}$

matrix. We apply a potential difference to one of the conductors and leave the other $n-1$ conductors quiet. With this voltage right hand side, the corresponding $\mathbf{ZI} = \mathbf{V}$ system is solved for the unknown current vector $\mathbf{I}$. As for the 1-conductor case, the current in one conductor will be equal to the sum of currents in the filaments into which the conductor was partitioned, i.e. from the filamentary current vector we obtain a current vector $\mathbf{I}^{(k_c)}$ with n elements corresponding to the total current inside each of the n conductors:

$$\mathbf{I}^{(k_c)} = \begin{pmatrix} \sum_{i_f \in \text{conductor } 1_c} (\mathbf{I})_{i_f} \\ \sum_{i_f \in \text{conductor } 2_c} (\mathbf{I})_{i_f} \\ \vdots \\ \sum_{i_f \in \text{conductor } n_c} (\mathbf{I})_{i_f} \end{pmatrix} \tag{2.29}$$

From (2.21), there exists a $n \times n$ matrix Z that multiplied by $\mathbf{I}^{(k_c)}$ results in the potential vector where the only nonzero element corresponds to the active conductor. In other words

$$\mathbf{ZI}^{(k_c)} = v_{io}\mathbf{e}^{(k_c)} \tag{2.30}$$

with $\mathbf{e}^{(k_c)}$ the vector with element k_c equal to one and other elements equal to zero and with v_{io} the difference of potential applied to the active conductor.

Setting v_{io} equal to 1 and repeating the process for the other $n-1$ conductors results in a collection of n vectors of currents $\mathbf{I}^{(k_c)}$, for $k_c = 1_c, \ldots, n_c$. From (2.30) for $k_c = 1_c, \ldots, n_c$, the matrix $\mathbf{Z}$ is the inverse of the matrix $\mathbf{Y}$ whose columns are the vectors $\mathbf{I}^{(k_c)}$, i.e.

$$\mathbf{Z} = \mathbf{Y}^{-1} := \left[\mathbf{I}^{(1_c)}| \ldots |\mathbf{I}^{(n_c)}\right]^{-1} \tag{2.31}$$

The matrix $\mathbf{Z}$ corresponds to the partial impedance matrix of the n-conductor configuration. This is the $n \times n$ matrix with elements equal to the self partial impedance of each conductor in the diagonal, and the partial mutual impedance among the conductors in the off-diagonal.

To resume, the method is as follows: for $k_c = 1_c, \ldots, n_c$ we apply a sinusoidal

potential of one volt at one end of conductor k_c and ground the other end. All other conductors are grounded at both ends (see Fig. 2.4). The corresponding linear system (2.22) is

$$\mathbf{ZI} = \mathbf{e}^{(k_c)} \tag{2.32}$$

the i_f-th entry in $\mathbf{e}^{(k_c)}$ is equal to one if filament i_f belongs to conductor k_c, and equal to zero if not.

After solving for $\mathbf{I}$ in (2.32), the k-th column of $\mathbf{Y}$ is formed by summing currents of filaments inside each of the n conductors:

$$(\mathbf{Y})_k = \begin{pmatrix} \sum\limits_{i_f \in \text{conductor } 1_c} (\mathbf{I})_{i_f} \\ \sum\limits_{i_f \in \text{conductor } 2_c} (\mathbf{I})_{i_f} \\ \vdots \\ \sum\limits_{i_f \in \text{conductor } n_c} (\mathbf{I})_{i_f} \end{pmatrix}. \tag{2.33}$$

Once the process has been repeated for the n conductors, we invert $\mathbf{Y}$ to obtain the n-conductor partial impedance matrix $\mathbf{Z}$.

2.3 Low frequency impedance simulation

We will consider the low frequency domain. In this domain the current distribution $\vec{J}$ is uniform in all the conductor's cross-section*. We do not need to discretize the conductors' cross-sections ($m = 1$ for all conductors). From the methodology presented in the previous section, this amounts to compute the partial impedance matrix $\mathbf{Z}$ using (2.23) for each conductor and (2.24) among conductors.

From (2.23), the static (DC) resistance of a conductor of length L and with constant cross-section of area A is given by

$$R_{DC} = \frac{L}{\sigma A}. \tag{2.34}$$

*See section 3.9

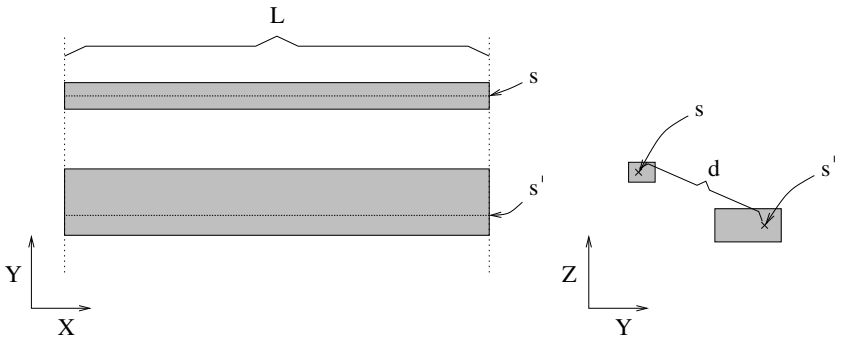


Figure 2.5: Two parallel wires of length L and constant cross-section, sharing the same perpendiculars

and its partial self inductance is

$$\mathcal{L} = \frac{\mu}{4\pi A^2} \int_{\bar{\Omega}} \int_{\bar{\Omega}} \frac{1}{\|x - x'\|} \, d\Omega \, d\Omega'. \tag{2.35}$$

with $\bar{\Omega}$ the conductor's volume.

From (2.24), the partial mutual inductance between two conductors with volumes $\bar{\Omega}_i$ and $\bar{\Omega}_k$, respectively, is given by

$$\mathcal{L}_{ik} = \frac{\mu}{4\pi A_i A_k} \int_{\bar{\Omega}_i} \int_{\bar{\Omega}_k} \frac{\hat{\ell}_i \cdot \hat{\ell}_k}{\|x - x'\|} \, d\Omega \, d\Omega'. \tag{2.36}$$

with A_i and A_k the area of the constant cross-section of conductor i and k, respectively.

2.3.1 Partial inductance of 2D configurations

We consider two parallel conductors of equal length L and ends sharing the same perpendicular with rectangular and constant cross-sections of area A_i and A_k, as shown in Fig. 2.5. For simplicity we call this kind of configuration a 2D configuration. We use the 2D terminology in the sense that the two wires share the same limits in the length coordinate, leaving just the limits in the two-dimensional cross-sections as free variables. Notice that despite the chosen name the computation of the inductance of a 2D configuration is in fact a 3D problem.

Exact Solutions

Exact solutions to both (2.35) and (2.36) for 2D configurations, are known in the literature. The one for the partial self inductance is due to Ruehli [7] and is given by:

$$
\begin{aligned}
\mathcal{L} = \frac{2\mu L}{\pi}\Bigg\{ & \frac{1}{4}\left[\frac{1}{W}\sinh^{-1}\frac{W}{\alpha_t}+\frac{1}{T}\sinh^{-1}\frac{T}{\alpha_w}+\sinh^{-1}\frac{1}{r}\right] \\
& +\frac{1}{24}\Bigg[\frac{T^2}{W}\sinh^{-1}\frac{W}{T\,\alpha_t(r+\alpha_r)}+\frac{W^2}{T}\sinh^{-1}\frac{T}{W\,\alpha_w(r+\alpha_r)} \\
& \quad +\frac{T^2}{W^2}\sinh^{-1}\frac{W^2}{T\,r(\alpha_t+\alpha_r)}+\frac{W^2}{T^2}\sinh^{-1}\frac{T^2}{W\,r(\alpha_w+\alpha_r)} \\
& \quad +\frac{1}{W\,T^2}\sinh^{-1}\frac{W\,T^2}{\alpha_t(\alpha_w+\alpha_r)}+\frac{1}{T\,W^2}\sinh^{-1}\frac{T\,W^2}{\alpha_w(\alpha_t+\alpha_r)}\Bigg] \\
& -\frac{1}{60}\Bigg[\frac{T^2(\alpha_r+r+T+\alpha_t)}{(r+\alpha_r)(r+T)(T+\alpha_t)(\alpha_t+\alpha_r)} \\
& \quad +\frac{W^2(\alpha_r+r+W+\alpha_w)}{(r+\alpha_r)(r+W)(W+\alpha_w)(\alpha_w+\alpha_r)} \\
& \quad +\frac{\alpha_r+\alpha_w+\alpha_t+1}{(\alpha_w+\alpha_r)(\alpha_t+\alpha_r)(\alpha_w+1)(\alpha_t+1)}\Bigg] \\
& -\frac{1}{6}\left[\frac{1}{W\,T}\tan^{-1}\frac{W\,T}{\alpha_r}+\frac{T}{W}\tan^{-1}\frac{W}{T\,\alpha_r}+\frac{W}{T}\tan^{-1}\frac{T}{W\,\alpha_r}\right] \\
& -\frac{1}{20}\left[\frac{1}{r+\alpha_r}+\frac{1}{\alpha_w+\alpha_r}+\frac{1}{\alpha_t+\alpha_r}\right]\Bigg\}
\end{aligned}
\tag{2.37}
$$

where L, w, t are the length, width and thickness of the conductor, respectively, $W = w/L$, $T = t/L$, $r = \sqrt{W^2+T^2}$, $\alpha_w = \sqrt{W^2+1}$, $\alpha_t = \sqrt{T^2+1}$ and $\alpha_r = \sqrt{W^2+T^2+1}$.

For 2D configurations, the partial mutual inductance between two rectangular wires (2.36) can be expressed exactly as a weighted sum of 16 partial self inductance values. This result is due to Zhong and Koh [27]. The expression for the partial mutual inductance between parallel wires of length L and respective cross-section areas $w_a \times t_a$ and $w_b \times t_b$ is given by:

$$
\mathcal{L}_{a,b} = \frac{1}{8\,w_a\,w_b\,t_a\,t_b}\sum_{i=1}^{4}\sum_{k=1}^{4}(-1)^{i+k}A^2_{a_i,b_k}\mathcal{L}_{a_i,b_k} \tag{2.38}
$$

with $\mathcal{L}_{a_i,b_k}$ the partial self inductance of the segment of length L and cross-section equal to the rectangle formed with vertices a_i and b_k (see Fig. 2.6). The value A_{a_i,b_k} being the area of this rectangle. For the general case in which the parallel segments are located in any placement, the corresponding expression becomes a weighted sum of 64 partial

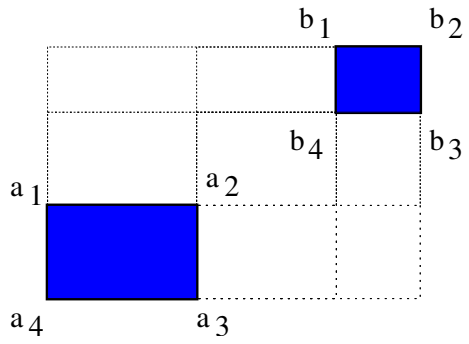


Figure 2.6: The cross-sections of two parallel wires

self inductance values.

The reader may notice the high complexity of using these exact solutions to compute partial self and mutual inductance of wire segments. For a realizable simulator capable of computing inductance of millions of wire segments, the use of simpler approximations is a priority, leaving these complex solutions just for particular cases in which great accuracy is needed.

Approximations

Equation (2.36) can be rewritten as

$$\mathcal{L}_{ik} = \frac{1}{A_i A_k} \int_{S_i} \int_{S_k} \underbrace{\left[\frac{\mu}{4\pi} \int_0^L \int_0^L \frac{1}{\|x - x'\|} \, dl \, dl' \right]}_{\mathcal{L}_{fil}} dS \; dS', \tag{2.39}$$

where S_i and S_k are the cross-section of conductor i and k, respectively. For two different cross-section points s and s', the integral inside the brackets in (2.39) corresponds to the partial mutual inductance between two infinitesimally thin parallel filaments of equal length L passing through s and s' (see Fig. 2.5). The exact solution to this integral is known and given by [28]

$$\mathcal{L}_{fil} = \frac{\mu L}{2\pi} \left[\ln\left(\frac{L}{d} + \sqrt{1 + \frac{L^2}{d^2}} \right) - \sqrt{1 + \frac{d^2}{L^2}} + \frac{d}{L} \right], \tag{2.40}$$

with d the distance between the cross-section points s and s' and $\ln(x)$ the natural logarithm function.

When $L \gg d$, expression (2.40) can be approximated by

$$\mathcal{L}_{fil} \approx \frac{\mu L}{2\pi}\left[\ln\left(\frac{2L}{d}\right) + \frac{d}{L} - 1\right]. \tag{2.41}$$

Substituting (2.41) in (2.39) results in the following approximation to the mutual inductance between two long and parallel conductors:

$$\mathcal{L} = \frac{\mu L}{2\pi}\left[\ln\left(\frac{2L}{d_g}\right) + \frac{d_a}{L} - 1\right] \tag{2.42}$$

with d_g and d_a the geometric mean distance (GMD) and the arithmetic mean distances (AMD) of the conductors' cross-section, respectively. The GMD and AMD are given by:

$$\ln(d_g) = \frac{1}{A_i A_k}\int_{S_i}\int_{S_k} \ln\|x - x'\|\, ds\, ds', \tag{2.43}$$

$$d_a = \frac{1}{A_i A_k}\int_{S_i}\int_{S_k} \|x - x'\|\, ds\, ds'. \tag{2.44}$$

When the center-center distance between two identical parallel conductors tends to zero, i.e. the conductors occupy the exact same volume in space, the expression (2.39), becomes the partial self inductance of the conductor:

$$\mathcal{L} = \int_{S_i}\int_{S_i} \frac{1}{A_i^2}\left[\frac{\mu}{4\pi}\int_0^L\int_0^L \frac{1}{\|x - x'\|}\, dl\, dl'\right] dS\; dS'. \tag{2.45}$$

This expression contains infinite poles, which are integrable nevertheless. Once again, if the length of the conductor is larger than the cross-section dimensions, expression (2.42) approximates well to the partial self inductance of the conductor, when replacing both d_g and d_a in the expression by the GMD and the AMD of the conductor's cross-section to itself, respectively [28].

2.3.2 GMD of a rectangle to itself

The GMD of a single rectangle of area $w \times h$ to itself, it is to a very good approximation given by [28]:

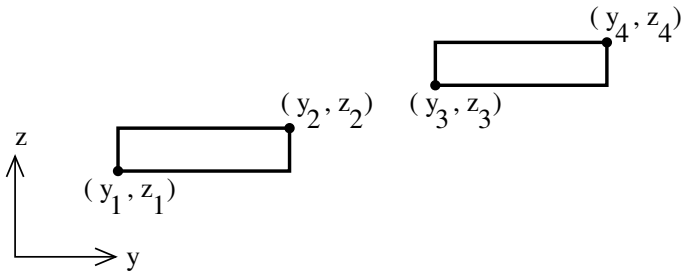


Figure 2.7: General configuration of two rectangles.

$$\ln(GMD) \approx \ln(w + h) - 3/2. \tag{2.46}$$

2.3.3 GMD between two different rectangles

The GMD of two rectangles, as shown in Fig. 2.7, is given by:

$$\ln\left(GMD_{A,B}\right) = \frac{1}{A \times B} \int_{y_1}^{y_2} \int_{z_1}^{z_2} \int_{y_3}^{y_4} \int_{z_3}^{z_4} \ln \sqrt{(y - y')^2 + (z - z')^2}\, dz'dy'dz\, dy, \tag{2.47}$$

with $A = (y_2 - y_1) \times (z_2 - z_1)$ and $B = (y_4 - y_3) \times (z_4 - z_3)$, the areas of the rectangles.

For the case when two identical rectangles are located on the same plane, i.e. $y_1 = y_3$ or $z_1 = z_3$, we can use the following approximation to their GMD [28]:

$$\ln\left(GMD\right) = \ln\left(a\right) + \ln\left(k\right), \tag{2.48}$$

with a the center to center distance between the rectangles and $\ln\left(k\right)$ a tabulated correction value that depends on the ratios between separation and cross-section dimensions.

To compute the GMD between two coplanar rectangles with same thickness but different width (Fig. 2.8.a,) we use the methodology presented in [10] that we proceed to explain in detail. This consist on partitioning the rectangle with maximum width, rectangle B in the figure, in $n = \lfloor B/A \rfloor$ pieces of cross-sectional area $B_i = A$, for $i = 1, \ldots, n$ and a remaining piece of cross-sectional area B_{n+1}. The following proposition, permits us to approximate the original GMD using the expression (2.48) for identical rectangles.

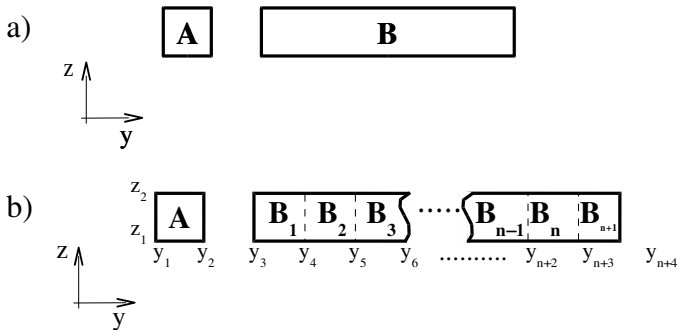


Figure 2.8: a) Front view of two wires with rectangular cross-section, b) Partitioning of the wire with larger width.

Proposition 1 *Given two rectangles of area A and B, as shown in Fig. 2.8.b, it holds that:*

$$\ln(GMD_{A,B}) = \frac{A\sum_{i=1}^{n}(\ln(GMD_{A,B_i})) + B_{n+1}\ln(GMD_{A,B_{n+1}})}{B}. \tag{2.49}$$

Proof: Call $G(y,y',z,z') := \sqrt{(y-y')^2+(z-z')^2}$ and $d\Omega := dy'dy\,dz'dz$.

From (2.47) it follows that

$$\ln(GMD_{A,B}) = \frac{1}{A\times B}\int_{z_1}^{z_2}\int_{z_1}^{z_2}\int_{y_1}^{y_2}\int_{y_3}^{y_{n+4}}\ln(G)\,d\Omega.$$

Partitioning the last integral

$$\begin{aligned}\ln(GMD_{A,B}) =& \frac{1}{A\times B}\int_{z_1}^{z_2}\int_{z_1}^{z_2}\int_{y_1}^{y_2}\sum_{i=3}^{n+3}\int_{y_i}^{y_{i+1}}\ln(G)\,d\Omega\\ =& \sum_{i=3}^{n+2}\left(\frac{1}{A\times B}\int_{z_1}^{z_2}\int_{z_1}^{z_2}\int_{y_1}^{y_2}\int_{y_i}^{y_{i+1}}\ln(G)\,d\Omega\right)+\frac{1}{A\times B}\int_{z_1}^{z_2}\int_{z_1}^{z_2}\int_{y_1}^{y_2}\int_{y_{n+3}}^{y_{n+4}}\ln(G)\,d\Omega,\end{aligned}$$

therefore

$$\ln(GMD_{A,B}) = \sum_{i=3}^{n+2}\left(\frac{B_{i-2}}{B}\frac{1}{A\times B_{i-2}}\int_{z_1}^{z_2}\int_{z_1}^{z_2}\int_{y_1}^{y_2}\int_{y_i}^{y_{i+1}}\ln(G)\,d\Omega\right) + \frac{B_{n+1}}{B}\frac{1}{A\times B_{n+1}}\int_{z_1}^{z_2}\int_{z_1}^{z_2}\int_{y_1}^{y_2}\int_{y_{n+3}}^{y_{n+4}}\ln(G)\,d\Omega.$$

Using (2.47) and since $B_i = A$ for $i < n+1$:

$$\ln(GMD_{A,B}) = \frac{A}{B}\sum_{i=1}^{n}(\ln(GMD_{A,B_i})) + \frac{B_{n+1}}{B}\ln(GMD_{A,B_{n+1}}).$$

■

In (2.49), all but the last term correspond to calculations of GMD's of identical rectangles. To compute the last term $GMD_{A,B_{n+1}}$ we use recursion with (2.49) but with A changed to B_{n+1} and B changed to A. We continue until the last remaining term is either negligible or strictly of zero size. We find that a recursion depth of 4 suffices to achieve an upper bound of 1% of error in the computation of the partial mutual inductance for realistic configurations.

We have verified empirically that the recursion method remains accurate for rectangles that are non coplanar. Each of the GMD's between non coplanar rectangles in the recursion can be approximated by the corresponding GMD between the same rectangles rotated around their centers so as to become coplanar. This approximation is explained in Fig. 2.9.

As a consequence of this approximation, together with Proposition 1, a similar recursion method can be applied when the rectangles do not have the same thickness. We partition the thickest rectangles into segments of thick equal to that of the finest rectangle. Only GMD's of rectangles with equal thickness but possibly different width need to be computed. We use for these the original recursion.

When the thickness or width of one rectangle is much larger than that of the other rectangle, the recursion method can become quite expensive. This kind of situation arises when computing the mutual inductance between, for example, a thin signal wire and a ground plane. Ground planes can have width of chip size, i.e., orders of magnitude wider than typical signal wires.

The exact solution to (2.47) can be calculated exactly observing that

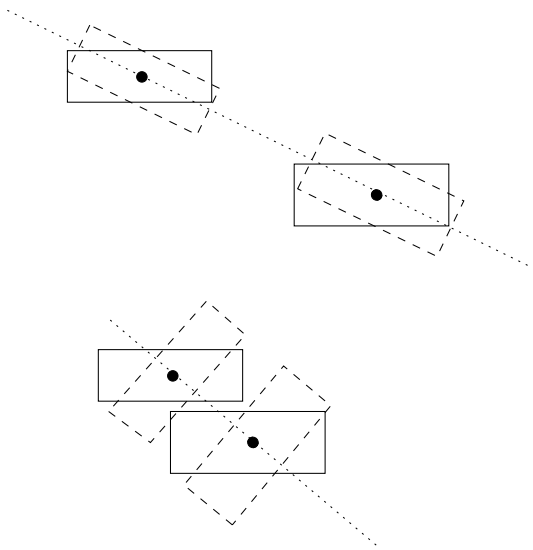


Figure 2.9: Approximation of the non-coplanar configuration. Dotted lines represent the approximated configuration for which the GMD is computed.

$$\frac{\partial^4 F(y-y',z-z')}{\partial y \partial z \partial y' \partial z'} = -\ln\left[(y-y')^2+(z-z')^2\right] - \frac{25}{6} \tag{2.50}$$

where

$$F(y,z) = \frac{y^4 - 6y^2z^2 + z^4}{24}\ln(y^2+z^2) - \frac{yz}{3}\left(y^2\tan^{-1}\frac{z}{y} + z^2\tan^{-1}\frac{y}{z}\right) \tag{2.51}$$

Using the above observation, equation (2.47) evaluates to

$$\ln(GMD_{A,B}) = \frac{1}{A\times B}\left[-\frac{1}{2}\ F(y-y',z-z')\Big|_{y_1}^{y_2}\Big|_{y_3}^{y_4}\Big|_{z_1}^{z_2}\Big|_{z_3}^{z_4} - \frac{25}{12}w_1w_2t_1t_2\right] \tag{2.52}$$

with $w_1 = y_2 - y_1$, $w_2 = y_4 - y_3$, $t_1 = z_2 - z_1$ and $t_2 = z_4 - z_3$.

This is an expression with 33 terms, most of them a combination of hyperbolic functions.

Therefore, we use this expression only when the recursion method is more expensive. Several heuristics are implemented in order to decide when to use the recursion methodology or the exact formula.

2.3.4 What if $d \geq L$?

The previous expressions are valid for configurations where transverse dimensions are much smaller than longitudinal dimensions, i.e., $L \gg d$. In other words, using (2.42) to compute self inductance of a short and wide (or thick) wire or using (2.42) to compute mutual inductance between two short and wide wires separated by a large distance, may result in large inaccuracies. To this effect, new expressions need to be used to assure the robustness of the method.

Self inductance of short and wide wires

We concentrate our attention in wires that have their transverse dimensions of the order of (or larger than) their length. For a wire with this characteristic, approximation (2.42) is not longer valid.

The trivial workaround that one could propose is to simply break the wire into m filaments, with m large enough so as to assure that the transverse dimension of each of the filaments are smaller than their length.

Take for instance a wire with length L and width $w = 2L$. Suppose the thickness to be much smaller than the length. This wire would need to be partitioned in its width into at least $m = 20$ filaments in order to comply $w_s < 0.1L$, with w_s the width of the filaments in which the wire was partitioned.

The self inductance of the wire is then computed using (2.28), i.e., one needs to compute the $m \times m$ self and mutual inductance interactions among filaments, as well as the static resistance of the m filaments. Some of the mutual inductance interactions will certainly violate the condition $l > d$ but their weight in the final sum will be negligible compared to the self interactions of the n wires and the mutual interaction of the filaments satisfying the condition $l > d$.

As an example, let us take a wire of length $L = 10\mu$m with rectangular cross-section $w = 100\mu$m and $t = 1\mu$m. In table 2.1 we show how the self inductance accuracy improved by using the partitioning scheme. Results are compared against (2.37).

Although precision has been recovered with this method, the overhead created by computing the $O(m^2)$ values and inverting the matrix makes it unattractive for IC simulation in which inductance of million of wires need to be calculated.

For the example given above, we use of the Ruehli's expression which is exact and it is about one order of magnitude slower than using (2.42). This increase in complexity

Nb. of filaments	1	10	100	Ruehli
Self induct.(in pH)	.437	.684	.686	.686

Table 2.1: Self inductance of a wire of length $L = 10\mu$m and rectangular cross-section $w = 100\mu$m and $t = 1\mu$m. Comparisons between Ruehli's expression and the partitioning scheme.

is the price we pay in order to achieve good accuracy.

Mutual inductance of short wires separated by large distance

There are two possible cases when computing the mutual inductance between short wires that have center-center distance much larger than their lengths. The trivial case is when the width of both wires is much smaller than the center-center distance. In this case both wires see each other as filaments, so it is reasonable to think that the original formula for filaments (eq. (2.40)) with d replaced by their center-center distance would suffice.

Take for instance one configuration consisting of two wires with $L = 10\mu$m, $w = 1\mu$m and $t = 1\mu$m, with a center-center distance of $d = 100\mu$m. The mutual inductance of this configuration using the exact (2.38) is 0.1 pH, which is exactly the same result when using (2.40). Furthermore, varying the width of both wires to $w = 30\mu$m results in no noticeable difference in the mutual inductance. This seems to verify that for long distance, the use of the filamentary expression is valid as long as $w < d/3$.

The other case is when two short and wide wires have an edge-edge distance close to zero, i.e. $w \approx d$. In this case using the filamentary approximation is not accurate. We could also partition the wires into filaments such that the condition $d > w$ is recovered. Taken n and m as the respective number of filaments in which the wires were broken, the mutual inductance of the original configuration would be equal to the sum of the $m.n$ mutual inductance terms between filaments at each wire. This is a $O(n^2)$ approach in the worst case (when $n \approx m$). This result in a method that could be several orders of magnitude slower than the original method, where no wires were partitioned, when high accuracy is required. Again, using such approach, albeit very accurate, becomes unattractive for real IC designs for which the number of wires can exceed a million.

For this case we prefer to use the exact expression due to Zhong and Koh which is one order of magnitude slower than using (2.42).

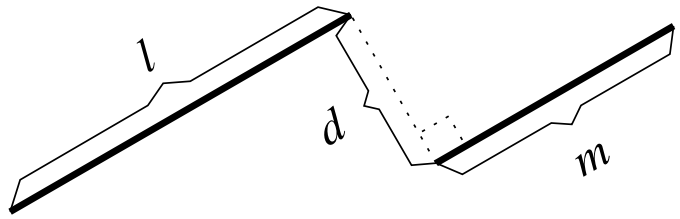


Figure 2.10: Two parallel filaments.

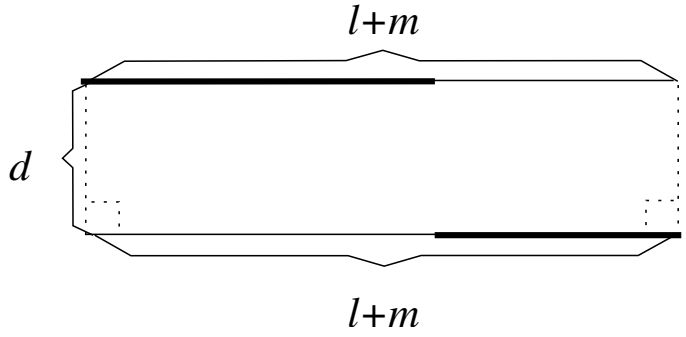


Figure 2.11: The amplified configuration of the two parallel filaments.

2.3.5 General partial mutual inductance (3D configurations)

Previous equations for 2D configurations are useful for computing partial inductance of configurations placed in any relative position, what we call 3D configurations. Take for instance the configuration of the two parallel filaments, with the end of one filament at the same orthogonal line as the start of the other filament. These filaments are shown in Fig. 2.10.

We denote as $\mathcal{L}_{l;d}$ the partial inductance of the 2D configuration given by two parallel filaments i and k with length l and separation d. In other words

$$\mathcal{L}_{l;d} = \frac{\mu}{4\pi} \int_0^l \int_0^l \frac{\hat{\ell}_i \cdot \hat{\ell}_k}{||x - x'||} \, dx \, dx' \tag{2.53}$$

with $\hat{\ell}_i$ and $\hat{\ell}_k$ the unit vector in the longitudinal direction of filament i and k, respectively.

Consider the extension of the previous configuration to one in which both filaments have the same length $l + m$. Without loss of generality, we take this configuration to

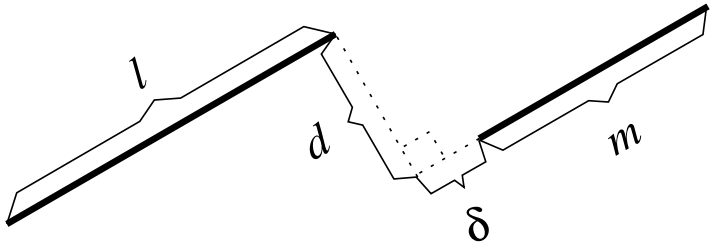


Figure 2.12: Two parallel filaments.

be parallel to the x-axis. See Fig. 2.11. From (2.53), the partial mutual inductance between this two filaments is given by the double integral:

$$\mathcal{L}_{l+m;d} = \int_0^{l+m}\int_0^{l+m} F(x,x')\,dx\,dx'. \tag{2.54}$$

with $F(x,x') = \mu\hat{\ell}_i \cdot \hat{\ell}_k/(4\pi\sqrt{(x-x')^2+d^2})$. Partitioning the integral limits we can rewrite (2.54) as:

$$\begin{aligned}\mathcal{L}_{l+m;d} &= \int_0^{l}\int_0^{l} F(x,x')\,dx\,dx' + \int_0^{l}\int_l^{l+m} F(x,x')\,dx\,dx' + \int_l^{l+m}\int_0^{l} F(x,x')\,dx\,dx' \\ &\quad + \int_l^{l+m}\int_l^{l+m} F(x,x')\,dx\,dx' \\ &= \int_0^{l}\int_0^{l} F(x,x')\,dx\,dx' + 2\int_0^{l}\int_l^{l+m} F(x,x')\,dx\,dx' + \int_l^{l+m}\int_l^{l+m} F(x,x')\,dx\,dx'\end{aligned} \tag{2.55}$$

From (2.55) and (2.53) the partial mutual inductance between the two original filaments in Fig. 2.10 is:

$$\mathcal{L} = \frac{\mathcal{L}_{l+m;d} - (\mathcal{L}_{l;d} + \mathcal{L}_{m;d})}{2}. \tag{2.56}$$

Consider the same configuration as before but with one filament shifted by a distance δ as shown in Fig. 2.12 and with both filaments having length equal to $l + m + \delta$. The corresponding double integral is given by:

$$\begin{aligned}\mathcal{L}_{l+m+\delta;d} &= \int_0^{l+\delta}\int_0^{l+\delta} F(x,x')\,dx\,dx' + \int_0^{l+\delta}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx' + \int_{l+\delta}^{l+m+\delta}\int_0^{l+\delta} F(x,x')\,dx\,dx' \\ &\quad + \int_{l+\delta}^{l+m+\delta}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx' \\ &= \int_0^{l+\delta}\int_0^{l+\delta} F(x,x')\,dx\,dx' + 2\int_0^{l+\delta}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx' + \int_{l+\delta}^{l+m+\delta}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx' \\ &= \int_0^{l+\delta}\int_0^{l+\delta} F(x,x')\,dx\,dx' + 2\int_0^{l}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx' + 2\int_{l}^{l+\delta}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx' \\ &\quad + \int_{l+\delta}^{l+m+\delta}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx'\end{aligned} \tag{2.57}$$

The third term at the last equality in (2.57) correspond to a configuration as the one in Fig. 2.10, but with l changed to δ. From (2.56):

$$\int_{l}^{l+\delta}\int_{l+\delta}^{l+m+\delta} F(x,x')\,dx\,dx' = \mathcal{L}_{l+m;d} - (\mathcal{L}_{l;d} + \mathcal{L}_{m;d}). \tag{2.58}$$

Replacing (2.58) in (2.57) and reordering, results in the partial mutual inductance between the two filaments of Fig. 2.12:

$$\mathcal{L} = \frac{\mathcal{L}_{l+m+\delta;d} + \mathcal{L}_{\delta;d} - (\mathcal{L}_{l+\delta;d} + \mathcal{L}_{m+\delta;d})}{2}. \tag{2.59}$$

Notice the convergence of (2.59) to (2.56) when $\delta = 0$. In the case of overlapping filaments, that is $\delta < 0$, the same expression applies but taking absolute value of the expressions where δ appears, that may be negative, i.e.:

$$\mathcal{L} = \frac{\mathcal{L}_{|l+m+\delta|;d} + \mathcal{L}_{|\delta|;d} - (\mathcal{L}_{|l+\delta|;d} + \mathcal{L}_{|m+\delta|;d})}{2}. \tag{2.60}$$

Expression (2.59) also holds for wires with finite cross-section. Each terms in this

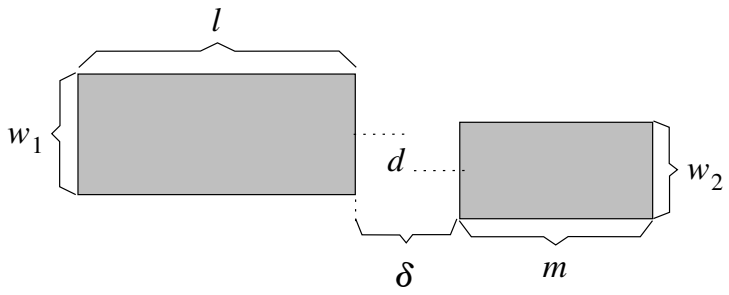


Figure 2.13: Two parallel wires with different widths w_1 and w_2.

expression is to be calculated using the expressions for partial mutual inductance of 2D configurations presented in the previous sections.

In the case of wires with finite cross-section, it may be possible to face a configuration as the one in Fig. 2.13. The first term of (2.59) for this configuration will correspond to the mutual inductance between two wires with center-center distance d greater than zero, but with their cross-sections sharing space. Although this kind of configuration is totally unphysical, its corresponding double volumetric integral (2.36) is solvable and furthermore (2.38), is the exact solution to this integral.

For two collinear wires ($d = 0$) with identical cross-section, expression (2.59) will result in the calculation of the mutual inductance of two identical wires with zero center-center distance which corresponds to the self inductance of one of the wires. For this case, (2.59) becomes:

$$\mathcal{L} = \frac{L_{l+m+\delta} + L_{\delta} - (L_{l+\delta} + L_{m+\delta})}{2}, \tag{2.61}$$

with L_l defined as the partial self inductance of the wire of length l and cross-section identical to that of the two original wires.

When the wires do not have identical cross-section, (2.59) will result in calculations of partial mutual inductance between two concentric wires with different cross-section. Once again, the expression due to Zhong and Koh is the exact solution to the double volumetric integral (2.36) for this particular case.

2.3.6 Partial mutual inductance of nonparallel wires

Consider the two filaments shown in Fig. 2.14. The mutual inductance between these two filaments is given by [28]:

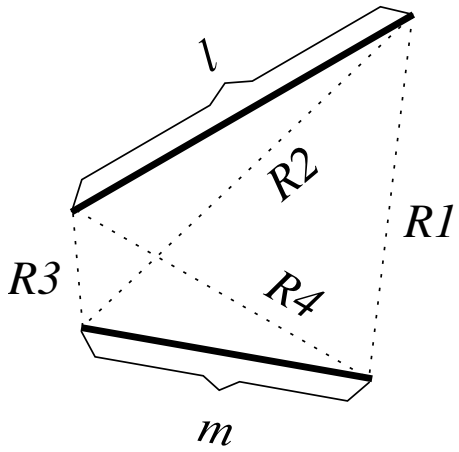


Figure 2.14: Two general filaments. R1, R2, R3 and R4 are the distances between their ends. Notice that these filaments are not necessarily located on the same plane.

$$\begin{aligned}\mathcal{L} = \frac{\mu k}{2\pi}\Bigg[&(u+l)\tanh^{-1}\frac{m}{R_1+R_2} + (v+m)\tanh^{-1}\frac{l}{R_1+R_4} \\ &- u\tanh^{-1}\frac{m}{R_3+R_4} - v\tanh^{-1}\frac{l}{R_2+R_3} - \frac{\Omega d}{2\sqrt{1-k^2}}\Bigg]\end{aligned} \tag{2.62}$$

where

$$\begin{aligned}\Omega =& \tanh^{-1}\frac{d^2k + (u+l)(v+m)(1-k^2)}{dR_1\sqrt{1-k^2}} - \tanh^{-1}\frac{d^2k + (u+l)v(1-k^2)}{dR_2\sqrt{1-k^2}} \\ &+ \tanh^{-1}\frac{d^2k + uv(1-k^2)}{dR_3\sqrt{1-k^2}} - \tanh^{-1}\frac{d^2k + u(v+m)(1-k^2)}{dR_4\sqrt{1-k^2}}, \\ k =& \frac{\alpha^2}{2lm}, \\ \alpha^2 =& {R_4}^2 - {R_3}^2 + {R_2}^2 - {R_1}^2, \\ d^2 =& {R_3}^2 - u^2 - v^2 + 2uvk, \\ u =& \frac{2m^2l({R_2}^2 - {R_3}^2 - l^2) + \alpha^2 l({R_4}^2 - {R_3}^2 - m^2)}{4l^2m^2 - \alpha^4}, \\ v =& \frac{2l^2m({R_4}^2 - {R_3}^2 - m^2) + \alpha^2 m({R_2}^2 - {R_3}^2 - l^2)}{4l^2m^2 - \alpha^4}.\end{aligned} \tag{2.63}$$

We approximate the partial mutual inductance of two nonparallel wires with finite cross-section, considering the two filaments passing through each of their centers and

using (2.62).

2.3.7 Summary

We present in tables 2.2 and 2.3 a quick reference to the equations for partial self and mutual inductance used in each case.

Type of configuration	Expression used
Thin wire ($w, t \ll L$)	(2.42)
Otherwise	(2.37)

Table 2.2: Partial self inductance expressions

Type of configuration	Expression used
2D: thin and near wires ($w, t, d \ll L$)	(2.42)
2D: short wires with $w, t \ll d$	(2.40) with d the center-center distance
2D: short wires with $w, t \approx d$	(2.38)
3D: wires: parallel	(2.56), (2.59) and (2.60)
3D: wires: collinear	(2.61)
3D: wires, nonparallel	(2.62)

Table 2.3: Partial mutual inductance expressions

2.4 3D magneto-quasistatic field solver

All the previous expressions for resistance and inductance of both 2D and 3D configurations are implemented in a low frequency impedance simulation tool. The simulator receives an input file where n wires are defined. The output of this tool are the resistance and partial inductance matrices:

$$\mathbf{R} = \begin{pmatrix} R_1 & 0 & \dots & 0 \\ 0 & R_2 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & R_n \end{pmatrix} \tag{2.64}$$

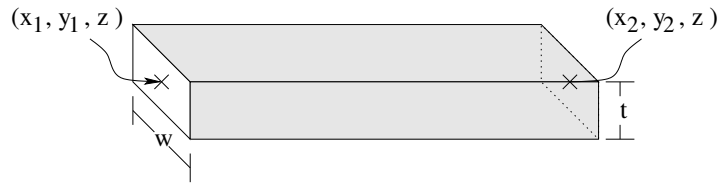


Figure 2.15: A wire defined for the simulator

$$\mathbf{L} = \begin{pmatrix} \mathcal{L}_1 & \mathcal{L}_{1,2} & \dots & \mathcal{L}_{1,n} \\ \mathcal{L}_{2,1} & \mathcal{L}_2 & \dots & \mathcal{L}_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ \mathcal{L}_{n,1} & \mathcal{L}_{n,2} & \dots & \mathcal{L}_n \end{pmatrix} \tag{2.65}$$

where R_i and $\mathcal{L}_i$ are the resistance and partial self inductance of the i-th wire, respectively. The value $\mathcal{L}_{i,k}$ corresponds to the partial mutual inductance between wire i and wire k.

2.4.1 Syntax of the input file

The syntax of the input file needed for the 3D impedance simulator is as follows:

```
*Comment Line
n=<number of wires>
<length units>
N1 w=<val> t=<val> x1=<val> x2=<val> y1=<val> y2=<val> z=<val> s=<val>
:
:
Nn w=<val> t=<val> x1=<val> x2=<val> y1=<val> y2=<val> z=<val> s=<val>
END
```

The values w and t are the width and thickness of the corresponding wire, respectively. The coordinates of the center points at each end of the wire are given by $(x1, y1, z)$ and $(x2, y2, z)$ (see Fig. 2.15). The value `s` is the conductivity of the material in which the wire is made off. All values are in agreement with the units defined in the `<length units>` line. For instance a value equal to 1e-6 corresponds to all distance values given in μm and the conductivity as $\mho/\mu$m.

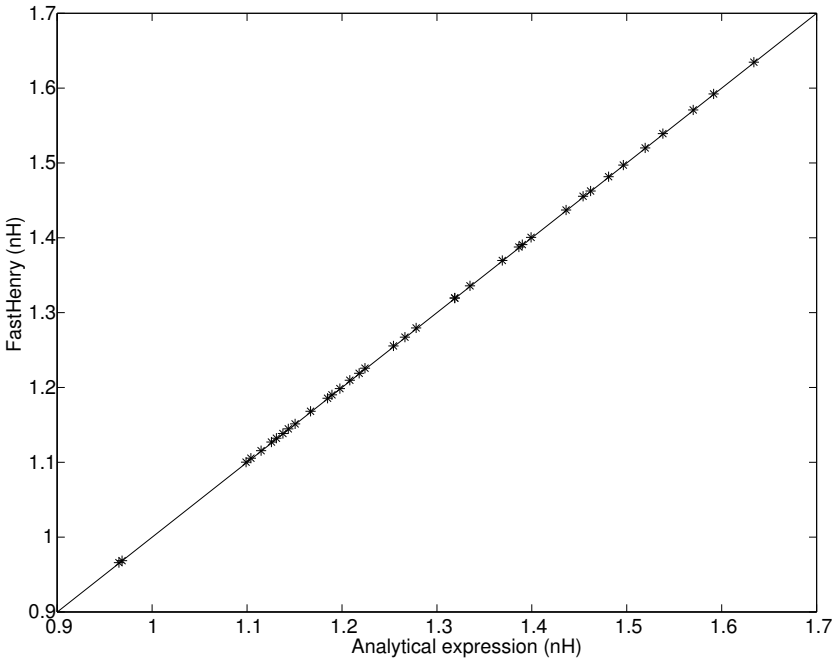


Figure 2.16: Partial self inductance: Comparison between FastHenry and the analytical expression.

2.4.2 Accuracy of the simulator

We proceed to compare the accuracy of this simulator against the golden standard used in the academical community. This is the 3D impedance simulator FastHenry [6] from MIT.

We compare accuracy of our inductance expressions, both for 2D and 3D configurations. We start by comparing the partial self inductance expression for several configurations with the corresponding values from FastHenry.

In the $L \gg d$ approximation the term d_a/L in (2.42) is small compared to the other terms. Furthermore, there are not known analytical expressions neither for the AMD of a rectangle to itself, nor for the AMD between two rectangles. We prefer to replace AMD in the inductance expressions by the corresponding GMD for which, as we have shown in previous sections, analytical expressions as well as accurate approximations exist. We do this to improve performance of the computations.

Results agree to within 1% in accuracy, as shown in Fig. 2.16. The method is computationally efficient as we will see in the next section.

Regarding partial mutual inductance, we have chosen several configurations with

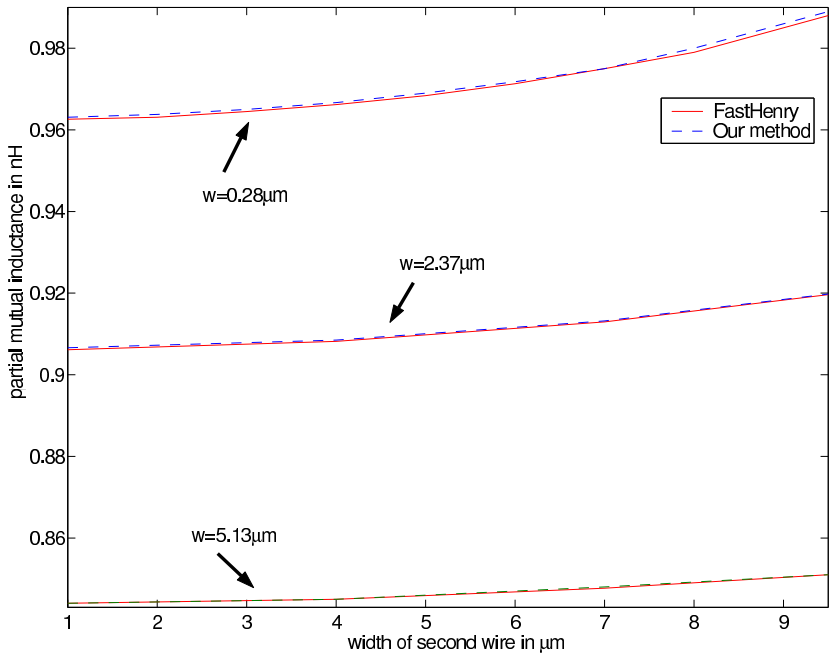


Figure 2.17: Partial mutual inductance: Comparison between FastHenry and our simplified expression.

different width values and center to center separation in order to validate our recursive approach to the calculation of the GMD between the two cross-sections (see section 2.3.3). In Fig. 2.17 the comparison between results from FastHenry and our simulator are shown.

As a second test case we use a configuration consisting of a dodecagon spiral inductor as shown in Fig. 2.18. We partitioned the inductor at each vertex in order to have straight segments. We choose this configuration as a test case since partial inductance of both 2D and 3D configurations are computed, so to validate accuracy of all the previous expressions.

The resistance matrix for this configuration was exactly the same in FastHenry and in our simulator. This is due to the fact that both FastHenry and our simulator use the resistance formula (2.34).

For purposes of illustration, the partial inductance matrix for the segments in the first turn of the inductor given by FastHenry is:

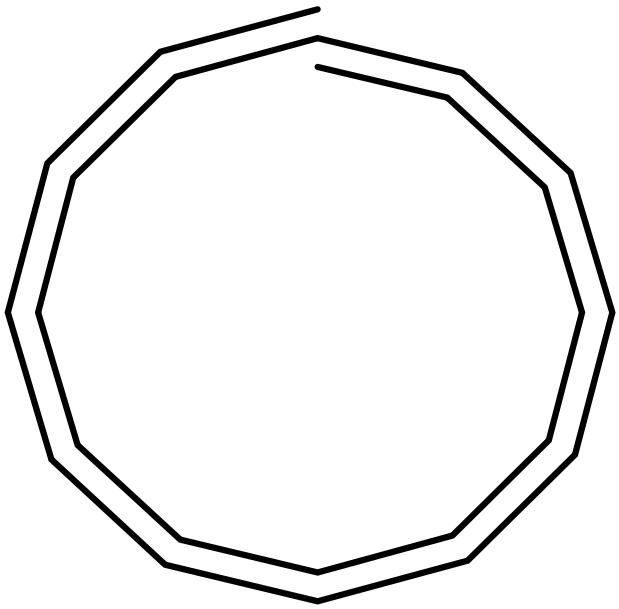


Figure 2.18: A dodecagon spiral inductor with 2 turns. With width=4μm, thickness=0.65μm, interwire separation=5μm and outer radius=100μm.

$$\mathcal{L} = \begin{pmatrix} 8.25 & 0.734 & -0.317 & -0.532 & -0.307 & 0.66 & 3.89 & 0.639 & -0.299 & -0.499 & -0.287 & 0.571 \\ 0.735 & 8.06 & 0.723 & -0.309 & -0.521 & -0.303 & 0.647 & 3.78 & 0.624 & -0.292 & -0.489 & -0.282 \\ -0.317 & 0.721 & 7.89 & 0.706 & -0.303 & -0.512 & -0.296 & 0.634 & 3.68 & 0.611 & -0.286 & -0.48 \\ -0.532 & -0.311 & 0.708 & 7.71 & 0.696 & -0.298 & -0.502 & -0.293 & 0.619 & 3.57 & 0.599 & -0.28 \\ -0.308 & -0.521 & -0.304 & 0.695 & 7.52 & 0.682 & -0.293 & -0.491 & -0.285 & 0.608 & 3.47 & 0.585 \\ 0.66 & -0.304 & -0.512 & -0.3 & 0.681 & 7.35 & 0.666 & -0.288 & -0.484 & -0.281 & 0.594 & 3.37 \\ 3.89 & 0.647 & -0.298 & -0.503 & -0.291 & 0.668 & 7.17 & 0.656 & -0.283 & -0.474 & -0.273 & 0.582 \\ 0.638 & 3.78 & 0.635 & -0.291 & -0.491 & -0.287 & 0.656 & 6.99 & 0.642 & -0.276 & -0.463 & -0.269 \\ -0.299 & 0.624 & 3.68 & 0.619 & -0.284 & -0.484 & -0.281 & 0.642 & 6.82 & 0.628 & -0.27 & -0.455 \\ -0.499 & -0.293 & 0.612 & 3.57 & 0.609 & -0.28 & -0.473 & -0.277 & 0.626 & 6.64 & 0.616 & -0.264 \\ -0.287 & -0.489 & -0.286 & 0.599 & 3.47 & 0.595 & -0.274 & -0.463 & -0.27 & 0.616 & 6.47 & 0.602 \\ 0.571 & -0.283 & -0.48 & -0.282 & 0.584 & 3.37 & 0.58 & -0.27 & -0.456 & -0.265 & 0.602 & 6.29 \end{pmatrix} * 10^{-11} H \quad (2.66)$$

And the corresponding partial inductance matrix given by our simulator is:

$$\mathcal{L} = \begin{pmatrix} 8.24 & 0.739 & -0.316 & -0.532 & -0.309 & 0.661 & 3.86 & 0.639 & -0.298 & -0.499 & -0.288 & 0.571 \\ 0.739 & 8.06 & 0.725 & -0.31 & -0.522 & -0.303 & 0.648 & 3.76 & 0.625 & -0.292 & -0.489 & -0.282 \\ -0.316 & 0.725 & 7.88 & 0.712 & -0.305 & -0.512 & -0.297 & 0.634 & 3.65 & 0.612 & -0.286 & -0.479 \\ -0.532 & -0.31 & 0.712 & 7.7 & 0.699 & -0.299 & -0.503 & -0.292 & 0.621 & 3.58 & 0.599 & -0.281 \\ -0.309 & -0.522 & -0.305 & 0.699 & 7.52 & 0.686 & -0.293 & -0.493 & -0.286 & 0.608 & 3.48 & 0.585 \\ 0.661 & -0.303 & -0.512 & -0.299 & 0.686 & 7.35 & 0.672 & -0.287 & -0.483 & -0.28 & 0.595 & 3.38 \\ 3.86 & 0.648 & -0.297 & -0.503 & -0.293 & 0.672 & 7.17 & 0.659 & -0.282 & -0.473 & -0.274 & 0.582 \\ 0.639 & 3.76 & 0.634 & -0.292 & -0.493 & -0.287 & 0.659 & 6.99 & 0.646 & -0.276 & -0.463 & -0.269 \\ -0.298 & 0.625 & 3.65 & 0.621 & -0.286 & -0.483 & -0.282 & 0.646 & 6.81 & 0.632 & -0.27 & -0.454 \\ -0.499 & -0.292 & 0.612 & 3.58 & 0.608 & -0.28 & -0.473 & -0.276 & 0.632 & 6.64 & 0.619 & -0.264 \\ -0.288 & -0.489 & -0.286 & 0.599 & 3.48 & 0.595 & -0.274 & -0.463 & -0.27 & 0.619 & 6.46 & 0.606 \\ 0.571 & -0.282 & -0.479 & -0.281 & 0.585 & 3.38 & 0.582 & -0.269 & -0.454 & -0.264 & 0.606 & 6.29 \end{pmatrix} * 10^{-11} H \quad (2.67)$$

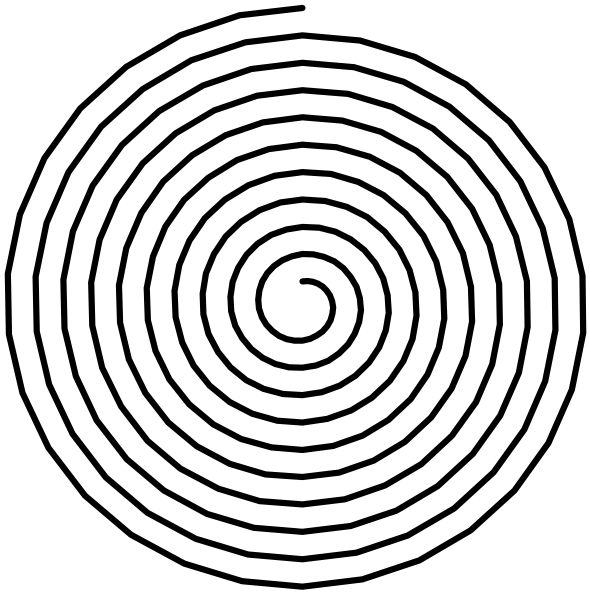


Figure 2.19: A polygonal inductor of 30 sides and 10 turns. With width=4μm, thickness=0.65μm, interwire separation=5μm and outer radius=100μm.

	Avg. Run time.(in *s*)
FH	4.2
Our Sim.	0.27

Table 2.4: Average run time to compute the impedance matrix of the spiral presented in Fig. 2.19

The average relative error in the values of the entire 24×24 partial inductance matrix was less than 0.5% with a maximum relative error of 2%.

2.4.3 Performance

We proceed to compare the performance of our simulator against FastHenry. We chose as a test case a polygonal inductor of 30 sides and 10 turns, as shown in Fig. 2.19.

We forced both FastHenry and our simulator to compute the impedance matrix of this configuration 100 times[†]. The resulting time of computation was then divided by

[†]this is done in order to have a comparison that is the most independent possible of the execution environment (cpu usage by other processes, memory, etc)

100. The average run time to compute the impedance matrix for this configuration are presented in table 2.4. As can be seen in the table our simulator was one order of magnitude faster than FastHenry, with a relative error of less than 2%.

The simplicity and accuracy of this simulator have made of this tool the computational core of the three applications presented in the following chapters.

Chapter 3

Integrated circuits impedance extraction

Extraction d'impédance dans les circuits intégrés

Résumé

Les fréquences employées dans les circuits intégrés continuent d'augmenter. Les effets d'inductance parasite sur la performance des circuits deviennent très significatifs. Par conséquent, une modélisation efficace et une analyse des phénomènes d'inductance deviennent une problématique d'un grand intérêt pour les concepteurs de circuits. Dans ce chapitre, nous présentons une méthodologie utile pour l'extraction des impédances dans les circuits intégrés. Cette méthodologie permet aux concepteurs d'avoir des valeurs mesurables des effets inductifs présents dans leur dessins. Cette méthodologie a été lancée sur le marché de la conception aidée par ordinateur (CAO), comme un produit de la société Mentor Graphics. Des brevets mondiaux pour protéger cette nouvelle technologie ont été également déposés.

3.1 Introduction

With integrated circuits reaching tenths of GHz new phenomena need to be captured in the wire behavior. As we incrementally move up in frequency the characterization of wires evolve from simple resistance in series with a capacitance to ground, to a

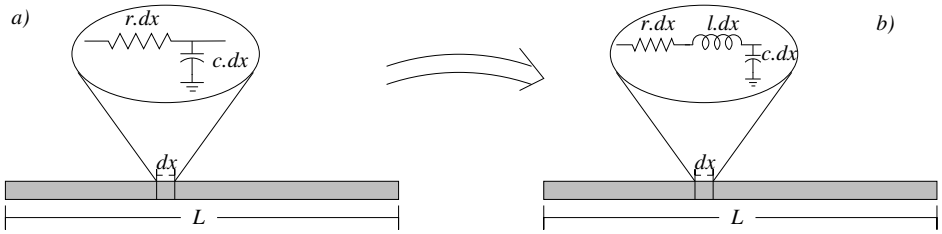


Figure 3.1: The RC and RLC representations of a wire of length L.

distributed version of the same [5] (Fig. 3.1.a). When inductance is important, we move up from the concatenation of RC segments, to an RLC distributed circuit (Fig. 3.1.b). To accurately capture in the wires the finite nature of the speed of light, the wires need to be represented as a distributed concatenation of RC or RLC lumped elements as shown in Fig. 3.1. When the number of elements tend to infinity and dx tends to zero this representation becomes an exact solution to the diffusion equation:

$$\frac{\partial^2 V(x,t)}{\partial x^2} = rc\frac{\partial V(x,t)}{\partial t} \tag{3.1}$$

for the RC case and to the telegraphist equation:

$$\frac{\partial^2 V(x,t)}{\partial x^2} = lc\frac{\partial^2 V(x,t)}{\partial t^2} + rc\frac{\partial V(x,t)}{\partial t} \tag{3.2}$$

for the RLC case, with $V(x,t)$ the voltage at the position x and at the time t. Both equations are direct consequences of the Maxwell equations (2.1-2.4) treated in the temporal domain [29]. A discretization using distributed lump representation, as in Fig. 3.1, reproduces exact solution to (3.2). For wire lengths of the order of the wavelength λ it suffices to set a sufficiently large number of lumped elements, say $n > 10$, or equivalently setting $dx \leq \lambda/10$ in the distributed representation.

With this lower bound to the number of lumped elements for each wire, we can get an idea of the complexity associated with the problem: It suffices to notice that a leading edge digital circuit at 65 nm contains $O(3 * 10^9)$ transistors, and $O(10^{10})$ wires. Each wire is distributed in average $O(10)$ segments, the data to be computed and hence to be stored for this example would amount to:

- $O(10^{11})$ values for resistance, capacitance and inductance
- $O(10^{22})$ values for mutual capacitance and mutual impedance among segments

A monumental computation indeed, as well as a large memory usage. In what follows, we present a divide-and-conquer methodology to extract the high frequency behavior in a way that is both computationally economical and with varying degrees of accuracy: from field solver accuracy, when such is demanded, to moderate accuracy for studies that only demand the knowledge of bounds, as in noise applications.

The application domains of the technology presented in this thesis are:

- Parasitic extraction of self impedance
- Parasitic extraction of mutual impedance
- Frequency dependence of the self and mutual impedance
- Timing representation
- Synthesis of clock structures accounting for inductance phenomena
- Impedance extraction of intentional devices , e.g. Inductors.
- Mutual impedance extraction among intentional inductors

This chapter is divided as follows:

In section 3.2 we describe the layout preprocessing steps, necessary for the impedance extraction. In section 3.3, we describe the approach widely used in the academic community for representation of parasitics in IC, the partial electric equivalent circuit (PEEC) [7]. We give detail of some of the recent techniques incorporated to the PEEC treatment in order to reduce its inherent limitations in IC.

In section 3.4 we present the loop impedance approach for representing circuits. We describe its advantages over the PEEC method as well as its applicability in IC. In section 3.5 we present our implementation of the impedance extraction tool for IC using the loop impedance approach. We start in this section with the self impedance extraction part of the flow for low frequency. We include in the same section, the extension of our self impedance extraction tool to the high frequency domain. We continue in section 3.6 with the second part of our flow, that of the low frequency mutual impedance extraction. We also include details of the heuristics implemented in our tool so as to greatly improve its performance. In section 3.8 an IC testcase to validate our methodology is presented.

We end the chapter in section 3.9 with an informal discussion about the frequency dependence of the current distribution in a conductor. We include an informal proof to

demonstrate why and how the distribution of currents ceases to be homogeneous with the increase of frequency.

3.2 Layout preprocessing

We start with a layout file representing the IC configuration. As a preprocessing step, a standard layout versus schematics (LVS) checking is performed [4]. The LVS process consists in comparing a schematics* of the IC configuration to its corresponding geometrical layout representation. By matching nodes and net names in the schematics with those in the geometrical layout, interconnect wires and their connectivity are recognized. This information is stored in a special database referred to as the Persistent Hierarchical DataBase (PHDB).

In a second preprocessing step, using the information in the PHDB, shapes in the layout file belonging to wire nets are broken in such a way as to only have straight segments of wire with constant width. This is done by searching for changes in direction and/or changes in width. Every time such a discontinuity is found, the wire is broken at this point. Each segment is considered to be a rectangle. Further partitioning refinements as those for fulfilling the maximal length bound of segments, for a particular wavelength, are also performed.

The broken layout will be represented in a database where geometrical information for each segment constituting the wire is stored. Each wire segment is represented by the center line coordinates of the extremes, width of the rectangle, layer and resistivity. Additional placeholders for each segment are created. These will be used downstream to store the resistance and inductance parameters for each segment. At the end of each wire segment, a linking table pointing to other wire segments' nodes, will be used to store both the coupling capacitance, and coupling impedance with other wire segments. This defines our "Parasitic Database", that we refer from here on as the PDB.

The next preprocessing step in our extraction flow, not explained in this thesis, is the extraction of total capacitance for each wire segment as well as the computation of the coupling capacitance among wire segments. The values computed in this step are stored in the corresponding placeholders found in the PDB. This process is done preserving the hierarchy in the initial design. For further information about capacitance extraction we refer the reader to [4].

*A topological representation consisting of devices and wires

3.3 Partial elements approach (PEEC)

Inductance is a property of *current loops*. The specification of what constitutes a loop within an IC is not always self evident when analyzing the layout. This possible ambiguity led to the development of an alternative treatment for the computation of the electromagnetic parameters resistance, capacitance and inductance, in terms of the contributions of each and every segment in a layout, without distinguishing which segment is associated with which loop [7]. The entire signal and power/ground network is represented in a large matrix. Each segment contributes to partial resistance, partial self inductance and partial mutual inductance, following the formulation of chapter 2. During circuit simulation the system is solved and the frequency dependent currents branches are computed. Our system consists of a set of metal interconnects which is a passive system[†]. For a passive system, the partial inductance matrix is positive definite, but not necessarily diagonally dominant. The ratio of non diagonal elements to diagonal ones decreases with distance as the inverse of the logarithm of the relative distance ((2.40)). The main consequence of the slow falloff is the inability to neglect small off diagonal terms in the dense partial inductance matrix. One cannot neglect them without putting into peril the positiveness of the eigenvalues. In [30] examples are shown were the sparsification of a partial inductance matrix results in the matrix having nonpositive eigenvalues, violating passivity of the system. It is only for systems that are positive definite and diagonally dominant where we can ensure that the elimination of small non diagonal terms in the matrix does not alter the sign of the lowest eigenvalues. A passive system with this characteristic remains passive after reduction. The price to pay keeping a PEEC formalism is that of dealing with unstable systems. The matrix dimensionality, for frequencies below the emergence of the skin effect, is determined by the total number of segments on the layout. Furthermore, at higher frequencies, the dimensionality of the matrix is multiplied by the number of filaments in a segment, needed for describing non uniform current distribution, rendering the PEEC formalism unattractive for high frequency extraction.

3.3.1 Implementation of the PEEC formalism

Partial self inductance, as well as static resistance of each wire segment in the PDB are computed. In a second step the partial mutual inductance between any two wire seg-

[†]A system where no energy is produced

ments is computed. To compute partial inductance we use the expressions as presented in tables 2.2 and 2.3. The value of partial self inductance will be stored in the corresponding placeholder of the PDB. All the partial mutual inductance values are stored in the linking table built to this effect.

The PDB is thought as a graph were nodes are connected by RLC elements. This will make possible the building of the equivalent netlist for posterior analysis. For passive systems, timing and noise simulation complexity ranges from $O(n^3)$ when the system is dense (i.e. $O(n^2)$ coupling elements), to $O(n^{3/2})$ when the system is sparse, with n the number of individual wire segments. Given the dense nature of the PEEC approach, the $O(n^3)$ bound is reached. This makes simulation unfeasible for modern circuits for which $n = O(10^{10})$. Great amount of effort has been invested to find techniques to sparsify the partial inductance matrix so to alleviate the dominant $O(n^3)$ cost.

3.3.2 Shift-truncate potential method

Truncating the partial inductance matrix by just setting to zero small elements in the off-diagonal may lead to losing the positive definiteness of the inductance matrix $\mathcal{L}$. In [30, 31] a sparsification scheme for $\mathcal{L}$ that guarantees conservation of the passivity is proposed. This methodology consists in assuming the return of currents of all segments to be at a finite distance r_0, instead of the conventional but not physical approach $r_0 = \infty$. The term $1/\|\vec{x} - \vec{x'}\|$ in (2.36) is replaced by the function

$$f(\vec{x}, \vec{x'}, r_O) = \begin{cases} \left(\frac{1}{\|\vec{x}-\vec{x'}\|} - \frac{1}{r_0}\right) & \text{if} \quad \|\vec{x} - \vec{x'}\| \leq r_0 \\ 0 & \text{else} \end{cases} \tag{3.3}$$

The choice of a small value of r_0 greatly increases the sparsity of the system. A small r_0 models very well the behavior in the high frequency regime since currents return through the nearest ground wires. It is the low frequency behavior the one which is very difficult to capture with this methodology. With a small r_0 the approximated circuit model will result in an important loss in accuracy compared to the original PEEC model.

In [30, 31], an iterative algorithm to search for the optimal r_0 is presented. The fact that the low frequency behavior of linear circuits is dominated by the smallest poles in the circuit is used. As r_0 increases, the dominant poles of the circuit stop changing since more return conductors are added to the representation. Using a moment expansion of the impulse response at $\omega = 0$ the ratio of two successive moments, (m_j/m_{j+1}) quickly

converges to the dominant pole, with increasing j [32]. The stop condition for the iterative method is fulfilled when the relative difference between the ratio of moments in one step and the ratio of moments in the previous step is smaller than a certain tolerance.

At each iteration, for a new value r_0, one has to compute the corresponding shell partial inductance matrix and then compute the ratio between the two consecutive moments to check for the stop condition, making of this methodology a very expensive one. Furthermore, no guarantee is given that for general configurations, the resulting shell radius r_0 will not be large enough so as to lose any sparsification and hence deprive this method of any advantage against the full partial inductance one.

3.3.3 The reluctance matrix ($K = \mathcal{L}^{-1}$) method

In [33] a different methodology for sparsification of the partial inductance matrix is proposed. This methodology consists in using the reluctance matrix $K = \mathcal{L}^{-1}$. The methodology in that paper is based in the belief, not yet formally proven, that the reluctance matrix is diagonal dominant. Such a matrix has the property that its rows fulfill the relationship:

$$|K_{ii}| > \sum_{j \neq i} |K_{ij}|. \tag{3.4}$$

This property together with the fact that elements in the diagonal are always positive [33] assure that any sparsification in the off-diagonal elements of K will result in a positive definite matrix. This, we remind, is to differ with the matrix $\mathcal{L}$ for which any sparsification might render the equivalent circuit system unstable.

Being able to sparsify K has the trivial advantage of making the circuit representation smaller and therefore improving the performance of the circuit simulation.

The obvious problem of this method is the cost involved in computing the inverse of $\mathcal{L}$. Furthermore, circuit simulators need to be modified to account for this new K matrix. Simulators able to directly work with the K matrix have been implemented [34, 35]. Also, EDA companies like Mentor Graphics and Synopsys have recently included the direct treatment of the K matrix in their timing simulators: Eldo [36] and HSpice [37], respectively. Exemplary uses of this methodology have shown instabilities.

For other Spice-based simulators with no support of the K matrix an equivalent model using known Spice elements is possible. This circuit representation was intro-

duced in [38]. Although the use of this clever description improves the performance vis-a-vis the original full $\mathcal{L}$ matrix simulation, its performance is even worse than that of the simulators that treat K directly. This is mainly due to the fact that non passive devices (current and voltage sources) need to be included in the description.

3.3.4 Double inverse method

In the same line of reluctance models, in [39] the use of the inverse of a windowed version of the $\mathcal{L}$ matrix denoted as the susceptance matrix S[‡] is proposed. The first step is to construct, for each conductor segment j, a partial inductance matrix $\mathcal{L}^{(j)}$ with segment j and all conductor segments within a window around it. The submatrices $S^{(j)}$ are computed by inverting the $\mathcal{L}_{(j)}$ matrices.

Once the susceptance matrices $S^{(j)}$ are computed for all j, they are merged into one complete and sparse susceptance matrix S. The matrix is not symmetric since $S_{ij}^{(j)} \neq S_{ij}^{(i)}$. The matrix S is rendered symmetric by setting its ij and ji elements to the value that results when choosing from $S_{ij}^{(j)}$ and $S_{ij}^{(i)}$ the one with the smallest magnitude.

This susceptance matrix is proven in [39] to be diagonal dominant and with diagonal elements positive, i.e. the matrix is positive definite and any truncation of off-diagonal terms does not affect its positiveness. Once the matrix has been truncated, it is inverted and the resulting partial inductance matrix $\tilde{\mathcal{L}} = S^{-1}$ is used for simulation.

The main disadvantage of this methodology is in the fact that inverting a sparse matrix does not necessarily results into a sparse matrix. In other words, no formal guarantee is given in that paper that the new "windowed" partial inductance matrix $\tilde{\mathcal{L}}$ will be sparse so as to show any advantage in the use of this matrix vis-a-vis the original full partial matrix in simulations.

3.4 Loop impedance approaches

In the loop impedance approach, circuit loops formed by signal wires and their corresponding return path, as well as power wires with their ground returns are considered. In the PC board world the loops are easily identifiable, the grounded backplane provides the natural return path. In the IC world, this is not that simple, there are multiple routes

[‡]Notice that both the reluctance and susceptance refer to the inverse of $\mathcal{L}$. Reluctance being the historical name. The difference in name, and hence notation, is the result of the two groups working independently and in parallel.

that can make up the current loop. The ground and power nets close to the signal wires are the main candidates to form the return path. The substrate, being low conductivity media is one among many possible return paths for the signal currents, giving often negligible contribution to the return path current. An important matter is then that of identifying which ones among the multiple choices provides the correct answer.

Once the return path of a signal/power wire is known, the loop impedance of the circuit formed by the signal/power and its return path is computed and the corresponding netlist is generated. Only the loop impedance of the signal lines and the mutual inductance among loops is included in the netlist, i.e. the size of the netlist is reduced by implicitly including the contribution of the ground in the loop treatment.

For the rest of this discussion we consider only loops formed by a signal and its return path. Similar reasoning may be applied for the loops formed by a power line and its return.

3.4.1 Previous work in the loop approach

A commercial tool from Sequence, named Columbus [23], includes a loop approach for impedance extraction. This tool breaks the signal lines into rectilinear pieces and then form circuits considering the signal line segment plus the two closest grounds. Instead of using known expressions for partial inductance, they perform extrapolation of values for inductance located in an "interconnect library". This library is filled by considering several different signal-two-ground configurations with different physical parameters (width, thickness, spacing).

The main disadvantage of this tool is the fact that choosing only the two closest grounds can ensure accuracy only in the very high frequency limit (section 3.5.7), so for designs with lower frequencies the accuracy is uncertain. Another evident disadvantage is the time incurred in filling the interconnect library and the possible inaccuracy that extrapolation from this library may produce.

In [18], a different divide-and-conquer methodology for the impedance extraction in IC using the loop approach is presented. The methodology in that paper amounts to divide the entire layout into disconnected regions where only grounds belonging to a region are considered as return path of the signals in the same region, and only signals within the same region are consider to interact. The layout is partitioned using "halos". A halo is one of the six semi-infinite imaginary boundaries emanated from the

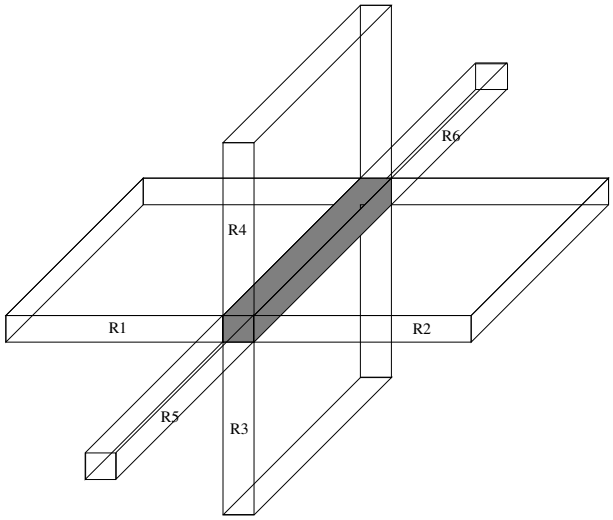


Figure 3.2: The halo of a ground segment consists of six semi-infinite boundaries R1, R2, R3, R4, R5 and R6.

power/ground faces as shown in Fig. 3.2. As the main rule, any halo emanating from a power/ground that is blocked by a signal wire parallel to the power/ground wire is neglected. The non blocked halos divide the chip into a collection of disjoint interaction regions. Loop circuits will be formed with signals and power/grounds belonging to the same region and loop impedance for each loop circuit is computed as well as loop inductance among all loops in a region. This partitioning of the layout can easily result into two signal lines belonging to different regions but sharing the ground wire in the boundary, as shown in Fig 3.3. The mutual inductance between two loops sharing a return path may be large. In other words, with their partitioning methodology truncation of important values in the inductance matrix may occur, significantly affecting accuracy.

This methodology is included in the commercial tool from Cadence: Assura RCX-PL [40].

3.4.2 Our contribution

For this thesis, we have developed a methodology for impedance extraction in IC using the loop approach. Instead of arbitrary breaking the layout into disconnected regions, we explore the layout, breaking the wires into 2D configurations (see chapter 2) formed by a single signal segment and the power/grounds segments that, we demonstrate, form its return path.

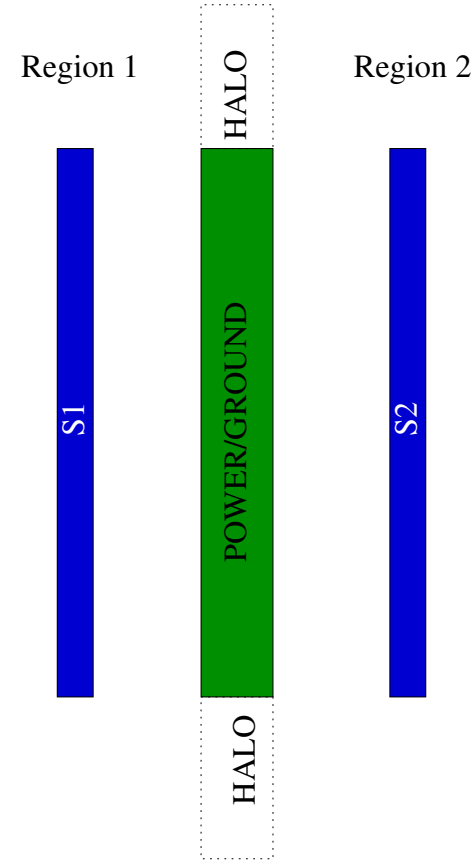


Figure 3.3: Two signal lines sharing the same power/ground line but lying in two different regions

Our new methodology becomes self-explanatory in the following sections.

3.5 A new loop impedance extraction scheme

We develop a new impedance extraction scheme using as a basis the loop impedance formalism. We consider the industry standard practice of layout in two orthogonal directions (x,y) as recommended for lithography considerations. This style is called "Manhattan layout" [41].

A detailed description of our divide-and-conquer scheme for impedance extraction is presented in the following sections.

3.5.1 Qualified list generation, filtering

There is a limited set of wire parameters (length, thickness and sheet resistance) for which inductance effects in timing analysis are important [42].

We provide the expressions for the lower and upper limits for the lengths of signal paths (L_{min} and L_{max}, respectively) for a given frequency f, such that inductance is significant.

We are not interested in short wires where the delay due to transistors dominates the total delay. The lower bound can be determined from the condition that the signal rise time T_{rise} be smaller than the time it takes to a signal to travel through the wire from source to destination and back to the source (first reflexion), at the speed of light in the medium (υ), this results in the lower bound L_{min}:

$$L_{min} = \frac{T_{rise}\upsilon}{2} \tag{3.5}$$

The time delay for line of length L is lower bounded by the time of flight, given by the linear expression [29]:

$$t_f = \sqrt{lc}L \tag{3.6}$$

with l and c the inductance and capacitance per-unit length, respectively. When the diffusion part of the delay dominates, the time delay of the distributed RLC line follows the quadratical expression [43]

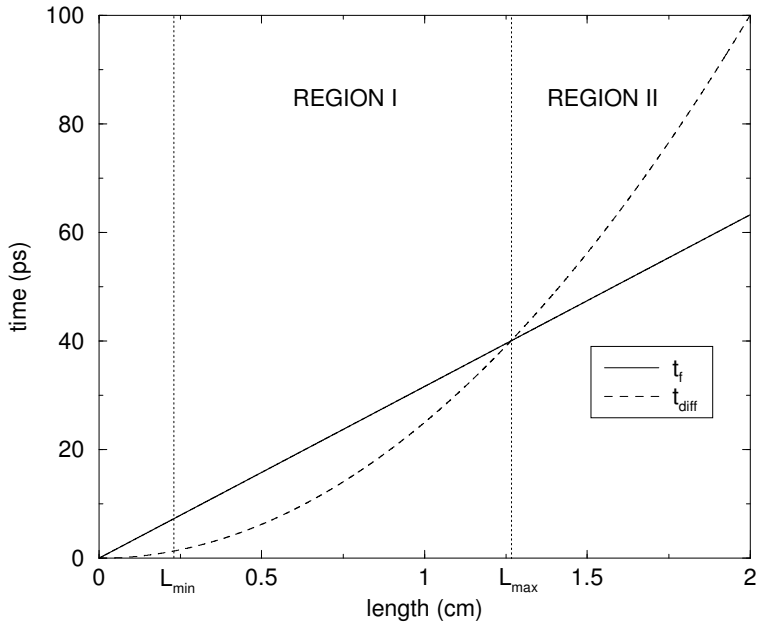


Figure 3.4: Time delay for a RLC line as a function of length and represented as the maximum value between time of flight and diffusion delay. Values used: $r = 5000\Omega$/m, $l = 10^{-7}$H/m and $c = 10^{-10}$F/m.

$$t_{diff} = \frac{rc}{2}L^2 \tag{3.7}$$

with r the resistance per unit length. This is known as the Elmore delay. Which one of the time delay expressions is valid depends on the length of the particular wire. This can be easily understood by observing Fig. 3.4, where both (3.6) and (3.7) are plotted as a function of length. We will compute inductance only for those wires that fall in region I. This is to say, wires with maximum length L_{max} such that

$$\delta_{rc} = \delta_{lc} \quad \Rightarrow \quad \frac{rcL_{max}^2}{2} = \sqrt{lc}L_{max} \tag{3.8}$$

and therefore

$$L_{max} = \frac{2}{r}\sqrt{\frac{l}{c}} \tag{3.9}$$

The process of filtering consists in identifying and storing in the prequalified list the signal paths whose total length from source to destination L satisfies $L_{min} \leq L \leq L_{max}$. Signals not belonging to this interval are insensitive to dynamic impedance and can be

treated as distributed RC networks, or alternatively as single lumped π sections, depending on their length: For small lengths, propagation can be considered as instantaneous, and lumped description applies. For very long wires, there is too much attenuation, due to multiple reflections that make the inductance effects disappear. Only a small percentage of the total number of signals, survives the filtering scheme, roughly $O(10^{-2}n)$ with n the total number of wires.

Notice that for the range of wire lengths where inductance is important, the signals cannot be treated as lumped objects for which standard circuit theory applies. It is accepted practice [10,42,44] to use lumped circuit elements for lengths that are smaller than $\frac{\lambda}{10}$ with λ the wave length which is given by

$$\lambda = \frac{\upsilon}{f} \tag{3.10}$$

The maximum frequency content of a pulse with time rise T_{rise} is approximately given by:

$$f_{max} = \frac{1}{\pi T_{rise}}. \tag{3.11}$$

From (3.10) and (3.11), the lower bound (3.5) can be rewritten as:

$$L_{min} \approx \frac{\lambda}{6}. \tag{3.12}$$

Any wire where inductance effects are important violates the $L < \lambda/10$ bound, therefore we must treat the circuit containing the wire as a distributed RLC circuit (Fig. 3.1.b).

Filtering is the first active computational step in our impedance extraction scheme.

3.5.2 Frequency selection

Impedance extraction is better physically represented in the frequency domain than in the time domain. Both the real and imaginary part of the impedance matrix are frequency dependent. There are two choices for impedance extraction: Narrow band extraction for which one fixes one frequency, and broadband extraction for which one fixes a maximum frequency. Broadband is useful for simulation of digital systems. In the broadband mode one performs the extraction such that is valid for the open interval Ω

$$\Omega = \{f : 0 < f < f_{max} = \frac{1}{\pi * T_{rise}}\} \tag{3.13}$$

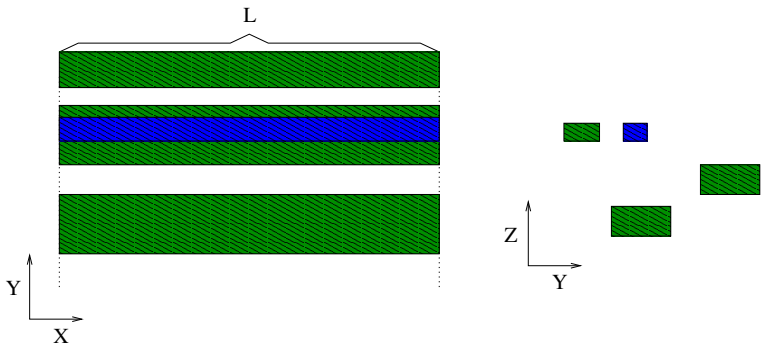


Figure 3.5: A typical bundle. The signal wire is in blue, the power/ground wires in green.

with T_{rise} the minimum rise time of signals on the circuit.

The maximum frequency, f_{max}, is the result of computing a realistic upper limit to the signal content of a finite pulse. In the low frequency part of the spectrum, when $2\pi f\mathcal{L} \ll R$, one can omit $\mathcal{L}$ extraction.

3.5.3 The power grid

The power and ground grid in its totality, or power and ground separately, needs to be considered for impedance calculation. In the presence of multiple power/grounds only the one attached to the analyzed wire is loaded. In what follows, we use the term ground indistinctly to label ground or power wires.

3.5.4 Fracturing

Only the signal lines that survive filtering are to be processed. In the preprocessing step these signal lines are broken into segments and each of the segment's information is stored in the PDB. We partition each segment into individual configurations that contain one signal and a set of parallel ground wires of the same length and sharing same perpendiculars, structures that we call *bundles*. An example of a bundle is shown in Fig. 3.5. *We do this to maximize the use of expressions for inductance of 2D configurations* (tables 2.2 and 2.3). In first order, there is no inductance coupling between horizontal and vertical wires ($\hat{\ell}_i \cdot \hat{\ell}_k = 0$ in (2.21)), we fracture vertical (in Y) and horizontal (in X) wires segments separately.

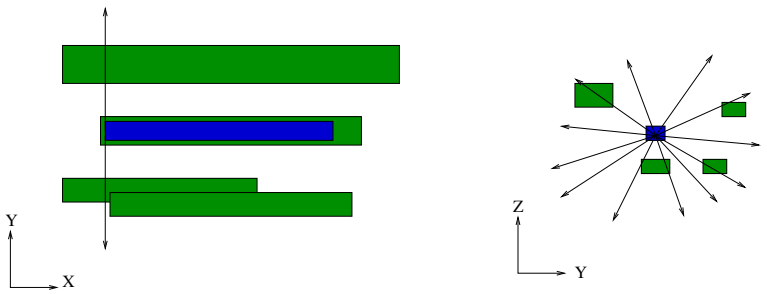


Figure 3.6: Looking for ground wires using scan lines emanating from the signal segment's end

To explain the method, we resort to present the flow as if each signal segment were to be analyzed separately. The reader will be reminded that the process of bundle generation for multiple signal segments is done in a single pass. This is computationally simpler, while less obvious to follow.

At the starting coordinate of the signal segment we throw orthogonal scan lines in all directions looking for ground wires in the vicinity, as shown in Fig. 3.6. Those ground wires intersected by these scan lines are placed into a queue. From this queue we chose the n grounds closest to the signal segment, using as metric, the euclidean distance between the wires' centers. We cut the signal segment and the ground segments in the queue so as to have a bundle with length equal to that of the shortest wire segment in the collection. This is shown in Fig. 3.7. If the signal segment was broken to form the bundle, we repeat the scan process from the coordinate where the cut was performed, otherwise we continue with the next signal segment in the list.

In pseudocode:

```
for horizontal and vertical wires
    for each signal segment in the PDB
        store in a list the ground wire segments intersected by the scan lines
        chose from the list the n closest return wire segments
        break all wire segments and form the bundle
        if the signal segment was broken
            repeat bundling from the coordinate where the signal was cut
        else continue.
    end
end
```

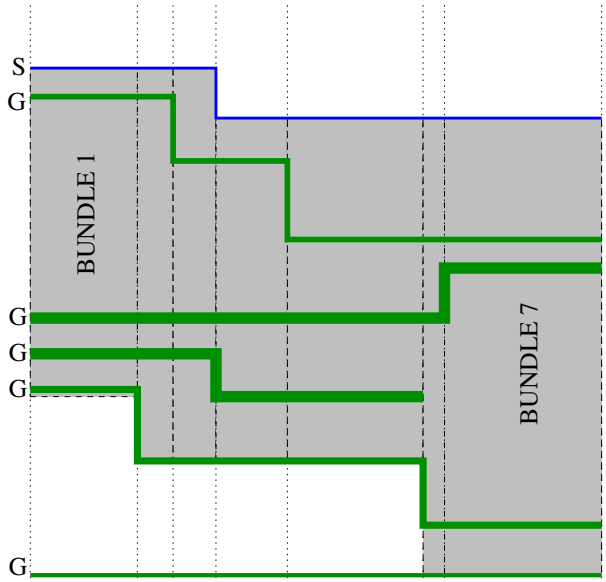


Figure 3.7: Partitioning of the design into bands such that wires inside it have equal length. The dotted lines represent where the partitioning has been performed. In this example, the signal path has been broken into 7 bundles (represented with the gray boxes). Only the $n = 3$ closest ground wires are chosen.

3.5.5 Loop impedance of a bundle

Consider a closed circuit representing a signal wire in parallel with n ground wires, the type of configuration we are interested in when computing loop impedance of a bundle (see Fig. 3.8.)

Applying Kirchoff voltage laws to the circuit shown in Fig. 3.8, at angular frequency ω, gives:

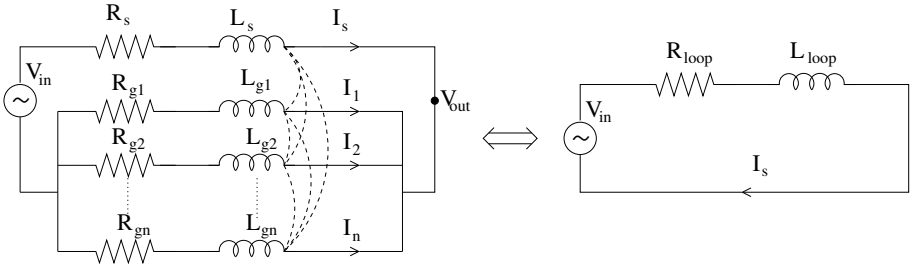


Figure 3.8: Equivalent circuit

$$\begin{bmatrix} R_s + j\omega\mathcal{L}_s & j\omega\mathcal{L}_{s,g_1} & \dots & j\omega\mathcal{L}_{s,g_n} \\ j\omega\mathcal{L}_{g_1,s} & R_{g_1} + j\omega\mathcal{L}_{g_1} & \dots & j\omega\mathcal{L}_{g_1,g_n} \\ \vdots & \vdots & & \vdots \\ j\omega\mathcal{L}_{g_n,s} & j\omega\mathcal{L}_{g_n,g_1} & \dots & R_{g_n} + j\omega\mathcal{L}_{g_n} \end{bmatrix} \begin{bmatrix} I_s \\ I_1 \\ \vdots \\ I_n \end{bmatrix} = \begin{bmatrix} V_{in} - V_{out} \\ -V_{out} \\ \vdots \\ -V_{out} \end{bmatrix} \tag{3.14}$$

in matrix form

$$\mathbf{Z}(\omega)\mathbf{I}(\omega) = \mathbf{V}(\omega).$$

where R_s and $\mathcal{L}_s$ are the static resistance and partial self inductance of the signal wire, respectively; R_{g_i} and $\mathcal{L}_{g_i}$ are the static resistance and partial self inductance of the i-th ground wire, respectively. The value $\mathcal{L}_{i,j}$ represents the partial mutual inductance between wires i and j.

The loop impedance of this circuit is the scalar complex value $Z_{loop} = R_{loop} + j\omega\mathcal{L}_{loop}$ that satisfies the relationship

$$Z_{loop} I_s = V_{in}. \tag{3.15}$$

The loop treatment, as here defined, reduces the full circuit, into an equivalent and much simpler representation as shown in Fig. 3.8.

In the simplest case of a single return path ($n = 1$), (3.14) reduces to a 2x2 linear system with trivial solution given by

$$I_s = \frac{V_{in}}{Z_s + Z_{g_1} - 2 * Z_{s,g_1}} \tag{3.16}$$

The loop impedance in this case is then:

$$Z_{loop} = R_s + R_{g_1} + j\omega\left(\mathcal{L}_s + \mathcal{L}_{g_1} - 2 * \mathcal{L}_{s,g_1}\right) \tag{3.17}$$

The general solution to (3.15) is not an analytical expression except at very low frequencies. An earlier analysis due to Krauter and Mehrotra (K&M) in [45] provides a simple approximation to the loop impedance of the circuit in Fig. 3.8. The basic assumption being that the current on the return wires should be computed entirely in terms of their resistance, totally neglecting the reactance contribution. For low enough frequencies, all reactance elements $\omega\mathcal{L}$ are clearly smaller than the resistance parts, ensuring the validity of this approximation. The resulting expressions for $\mathcal{L}_{loop}$ and

R_{loop} are:

$$\begin{aligned} R_{loop} &= R_s + R_{GND} \\ R_{GND} &= (R_{g_1}^{-1} + \ldots + R_{g_n}^{-1})^{-1} \\ \mathcal{L}_{loop} &= \mathcal{L}_s + \sum_{i=1}^{n} \alpha_i \mathcal{L}_{s,g_i} + \sum_{i=1}^{n} \alpha_i \sum_{j=1}^{n} \alpha_j \mathcal{L}_{g_i,g_j} \\ \alpha_i &= \frac{-R_{GND}}{R_{g_i}} \quad \text{for} \quad i > 0 \end{aligned}$$

Equation (3.14) represents a system of $n + 1$ equations with $n + 2$ unknowns (the $n + 1$ currents and the potential V_{out}). The system is completed with Kirchoff's current law.

$$I_s + \sum_{i=1}^{n} I_i = 0. \tag{3.18}$$

Once the $n + 2$ unknowns, for a particular frequency and for a particular V_{in} has been found, the loop impedance Z_{loop} for that frequency is given by $Z_{loop} = V_{in}/I_s$.

To solve this problem we rewrite (3.14) as

$$\mathbf{ZI} = \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix} - V_{out} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}, \tag{3.19}$$

We solve the two associated systems

$$\mathbf{Zx} = \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad \text{and} \quad \mathbf{Zy} = \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}.$$

and rewrite (3.19) as

$$\mathbf{I} = \mathbf{x} - V_{out}\mathbf{y} \tag{3.20}$$

summing the rows on both side of (3.20) and using (3.18) results in

$$V_{out} = \frac{\sum x_i}{\sum y_i},$$

therefore

$$I_s = x_1 - \frac{\sum x_i}{\sum y_i} y_1.$$

We set $V_{out} = 1$v. By virtue of (3.15)

$$Z_{loop} = \left(x_1 - \frac{\sum x_i}{\sum y_i} y_1 \right)^{-1}.$$

Two linear systems need to be solved, one for $\mathbf{x}$ the other for $\mathbf{y}$. Both systems involve the same matrix $\mathbf{Z}$. For this, we use a matrix factorization that takes advantage of the symmetry of the matrix, the LDL^T factorization.

The current coefficients α_i for each wire in the bundle are stored for future reference. These coefficients are given by

$$\alpha_i = -\frac{I_i}{I_s} \tag{3.21}$$

and for the signal wire

$$\alpha_s = 1$$

These complex coefficients are frequency dependent.

3.5.6 LDL^T factorization

We first review the LDL^T factorization [46] for real matrices followed by our extension to factorizing complex matrices as we need for the solution of nodal equations $\mathbf{ZI} = \mathbf{V}$.

Real matrices

Consider $\mathbf{A}$ a $n \times n$ real symmetric, positive definite matrix (SPD) i.e. it satisfies: $\mathbf{A}^T = \mathbf{A}$; and $\mathbf{x}^T\mathbf{Ax} > 0$ for any $\mathbf{x} \neq \mathbf{0}$.

Given such matrix, there exists a lower triangular unit matrix $\mathbf{L}$ and a diagonal matrix $\mathbf{D}$ such that

$$\mathbf{L}\mathbf{D}\mathbf{L}^T = \mathbf{A}. \tag{3.22}$$

The proof is available in [46]. Consequently, for a linear system of the form $\mathbf{A}\mathbf{x} = \mathbf{b}$ with $\mathbf{A}$ SPD, it can be rewritten as $\mathbf{L}\mathbf{D}\mathbf{L}^T\mathbf{x} = \mathbf{b}$ and its solution can be found by performing one forward elimination to solve $\mathbf{L}\mathbf{y} = \mathbf{b}$, followed by n divisions to solve $\mathbf{D}\mathbf{y} = \mathbf{z}$, and finally one backward substitution to solve $\mathbf{L}^T\mathbf{x} = \mathbf{y}$.

The standard algorithm for LDL^T factorization is:

Algorithm 1 (LDL^T) Given $\mathbf{A}$, $n \times n$ real SPD matrix. This algorithm returns a triangular unit matrix $\mathbf{L}$ and a vector $\mathbf{d}$ whose elements represent the nonzero elements of a diagonal matrix $\mathbf{D}$ such that $\mathbf{A} = \mathbf{L}\mathbf{D}\mathbf{L}^T$.

for $j = 1 : n$
  sum=$A(j, j)$
  for $i = 1 : j - 1$
    $v(i) = L(j, i)d(i)$
    sum=sum$-L(j, i)v(i)$
  end
  $d(j)$=sum
  $v(j)$=sum
  for $i = j + 1 : n$
    sum=$A(j, i)$
    for $k = 1 : j - 1$
      sum=sum$-L(i, k)v(k)$
    end
    $L(i, j)$=sum$/v(j)$
  end
end

It is known from [46] that the positive definiteness of $\mathbf{A}$ guarantees the completion of the algorithm and ensure that all the diagonal elements of $\mathbf{D}$ are strictly positive. One can construct the diagonal matrix $\mathbf{D}^{1/2}$ with entries equal to the square root of the elements of $\mathbf{D}$. It follows that (3.22) can be rewritten as

$$(\mathbf{L}\mathbf{D}^{1/2})(\mathbf{L}\mathbf{D}^{1/2})^T = \hat{\mathbf{L}}\hat{\mathbf{L}}^T = \mathbf{A}. \tag{3.23}$$

This form of rewriting of the LDL^T factorization is known as the Cholesky factorization [46].

To build the matrix $\hat{\mathbf{L}}$ we use the following recursion procedure [47]:

$$\hat{L}_{ii} = \sqrt{a_{ii} - \sum_{k=1}^{i-1} \hat{L}_{ik}^2} \tag{3.24}$$

and

$$\hat{L}_{ji} = \frac{1}{\hat{L}_{ii}} \left(a_{ij} - \sum_{k=1}^{i-1} \hat{L}_{ik} \hat{L}_{jk} \right) \quad \text{for } j > i. \tag{3.25}$$

LDL^T and Cholesky factorization algorithms require access to only the upper triangular part and the diagonal of $\mathbf{A}$. We can use the lower triangular part of $\mathbf{A}$ to store the lower part of $\mathbf{L}$ and use an additional vector to store the diagonal elements of $\mathbf{L}$. This simple recipe renders both algorithms memory efficient.

Complex matrices

We propose a natural and straightforward extension of Algorithm 1 to the complex case.

The LDL^T algorithm for general complex matrices is:

Algorithm 2 (LDL^T) Given $\mathbf{Z} = \mathbf{A} + j\mathbf{B}$ a $n \times n$ complex symmetric matrix. Upon completion, this algorithm returns a complex triangular unit matrix $\mathbf{L}$ and a diagonal matrix $\mathbf{D}$, such that $\mathbf{Z} = \mathbf{L}\mathbf{D}\mathbf{L}^T$. The matrix $\mathbf{L}$ is represented by a real $n \times n$ matrix $\mathbf{G}$ where $G(i, j) = \mathrm{Re}(L(i, j))$ and $G(j, i) = \mathrm{Im}(L(i, j))$ for $i > j$. Two real vectors d_r and d_i correspond to the real and imaginary parts of the diagonal elements of $\mathbf{D}$, respectively.

for $j = 1 : n$
  sumr = $A(j, j)$
  sumi = $B(j, j)$
  for $i = 1 : j - 1$
    $v_r(i) = G(j, i)d_r(i) - G(i, j)d_i(i)$
    $v_i(i) = G(i, j)d_r(i) + G(j, i)d_i(i)$
    sumr = sumr $- (G(j, i)v_r(i) - G(i, j)v_i(i))$
    sumi = sumi $- (G(i, j)v_r(i) + G(j, i)v_i(i))$
  end
  $d_r(j)$ = sumr
  $d_j(j)$ = sumi
  $v_r(j)$ = sumr
  $v_i(j)$ = sumi
  for $i = j + 1 : n$
    sumr = $A(j, i)$

```
    sumi = B(j, i)
    for k = 1 : j − 1
        sumr = sumr − (G(i, k)v_r(k) − G(k, i)v_i(k))
        sumi = sumi − (G(k, i)v_r(k) + G(i, k)v_i(k))
    end
    G(i, j) = (sumr∗v_r(j)+sumi∗v_i(j))/(v_r(j)^2 + v_i(j)^2)
    G(j, i) = (sumi∗v_r(j)+sumr∗v_i(j))/(v_r(j)^2 + v_i(j)^2)
  end
end
```

Memory consumption can be reduced by overwriting the lower parts of **A** and **B** with the lower and upper parts of **G** (i.e., the real and imaginary parts of **L**), respectively.

The extension of the Cholesky factorization to the complex case consists in simply changing the real operations in (3.24) and (3.25) to complex operations. For our application we prefer to use the LDL^T factorization since the expensive square roots calculations are avoided.

Existence of the LDL^T factorization for complex matrices

In general, algorithm 2 breaks when a value $d(i) = d_r(i) + jd_i(i)$ is found to be zero. In some cases, this can be avoided by performing what is known as pivoting. This is, interchange rows and columns in the original matrix **Z** until a d different from zero is found. This results in a factorization, of a permuted matrix $\mathbf{PZP}^T$, of the form $\mathbf{LDL}^T$ where **L** is lower triangular and **D** is block diagonal with blocks of size 1 or 2.

The LDL^T and Cholesky factorizations are known to exist without pivoting for complex hermitian positive definite matrices [46]. The impedance matrix **Z**, is complex and symmetric but not hermitian.

For a complex symmetric (not hermitian) matrix $\mathbf{Z} = \mathbf{A} + j\mathbf{B}$, with **A**, and **B**, real SPD matrices, Higham in [48] shows that an LDL^T factorization for $\mathbf{PZP}^T$ exists. He denotes this kind of matrices as CSPD.

It is easy to show that the pivots $d(i) = d_r(i) + jd_i(i)$ in Algorithm 2 result from the following recursion:

$$d(i) = \frac{\det(Z_i)}{\det(Z_{i-1})} \tag{3.26}$$

where $\det(Z_i)$ is the determinant of the submatrix $Z_i = Z(1 : i, 1 : i)$. By construction $d(1) = Z(1, 1)$. Higham proved that a CSPD matrix is nonsingular, i.e., its determinant its nonzero. He also proved that each submatrix Z_i of a CSPD matrix is also CSPD.

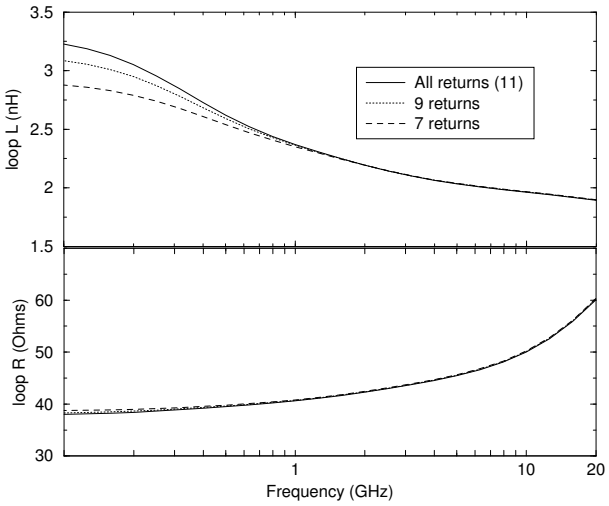


Figure 3.9: Loop impedance of a bundle

For this reason $d(i) \neq 0$ for $i = 1, \ldots, n$. This means that no pivoting is necessary to compute the LDL^T factorization of a CSPD matrix and hence for this kind of matrices Algorithm 2 runs to completion.

The real part of the impedance matrix $\mathbf{Z}$ is the resistance matrix which is trivially positive definite. The imaginary part corresponds to the inductance matrix times a positive value, the angular frequency. For passives circuits the inductance matrix is positive definite. Algorithm 2 is guaranteed to arrive to completion when applied to matrix $\mathbf{Z}$.

Since Cholesky factorization is a special case of the LDL^T factorization, we can ensure that the former exists under the same constraints as the later.

3.5.7 Localized return path

How many return wires to include in a bundle depends on the frequency. For low frequencies, the real part of the impedance dominates. This is to say, currents in a signal line will tend to return through as many power/ground so as to minimize the resistance. At higher frequencies, when the imaginary part of the impedance starts to be significant, the currents will prefer those return wires in the vicinity so as to reduce the size of the loop and therefore reduce the inductance. For consistency and in order to capture the frequency behavior of the impedance we choose a fixed number n of return wires in a bundle for any frequency. The value of n is selected such as to give a close fit

to the impedance at intermediate frequencies. Choosing a fixed value of n guarantees the correct monotonicity of both the resistance and the inductance with frequency.

We show in Fig. 3.9 the loop resistance and inductance as a function of frequency of a bundle with 11 return wires. In that figure we also show what would be the loop resistance and inductance of the same bundle if we took only the closest 9 or 7 return wires. We observe that taking the closest 7 returns approximates very well the loop impedance for frequencies above 500 MHz.

The reader may notice that at higher frequencies the contribution of some of the wires, specially those at large distance from the signal, is negligible. Instead of changing the number of return paths according to the frequency we prefer to keep a fixed number of return paths. *The choice of a fixed number of return wires is ensures a smooth representation of the frequency dependence of both the resistance and inductance.*

3.5.8 Loop self impedance associated with a signal segment

The loop self impedance associated with a signal segment is computed using our divide-and-conquer scheme. Each signal segment is partitioned into a series connection of bundles for which loop impedance is computable as presented in the previous sections. The loop impedance of a circuit composed of two elements in series is equal to the sum of the loop impedance of each element plus twice the mutual impedance between the segments. This extends to the general case in which a circuit is formed by the series connection of m elements, i.e. the self impedance of a signal wire segment in the database is the sum of the loop self impedance of the bundles into which it was partitioned plus twice the mutual impedance among all bundles. We call the mutual impedance between bundles belonging to the same wire segment: forward coupling.

The forward coupling between bundles decays quadratically with distance [49]. In fact, the forward coupling between two bundles is negligible compared to the self impedance values, when the length of the bundles is an order of magnitude larger than their transverse dimensions [11].

Forward coupling corrections

This subsection provides a method for computing the mutual interaction among bundles belonging to the same signal wire.

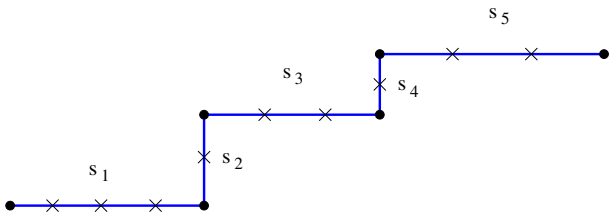


Figure 3.10: A signal line broken into 5 PDB segments. The boundaries of the bundles into which each segment is broken are shown with crosses.

To this effect we proceed as follows: Given a signal wire path from source to destination, broken into segments, each segment further partitioned into multiple subsegments to form a non overlapping set of bundles, as shown in Fig 3.10. We use the fact that in the loop formalism, the mutual inductance between bundles falls off as a power of the separation of the bundles [49]. We group all bundles in a wire segment and compute the forward coupling values only between adjacent bundles, i.e. for n bundles we compute $n-1$ forward couplings. The correction to the self impedance of the wire segment is equal to twice the sum of the $n-1$ forward coupling values.

The mutual loop inductance between two bundles is given by [49]:

$$\mathcal{L}_{a,b} = \sum_{i \in \text{bundle}_a} \sum_{j \in \text{bundle}_b} \alpha_i \alpha_j \mathcal{L}_{i,j} \tag{3.27}$$

with $\mathcal{L}_{i,j}$ the partial mutual inductance between wire segment i in bundle a and wire segment j in bundle b. The coefficients α are calculated and stored in the self impedance step. We remind

$$\alpha_i = -\frac{I_i}{I_s} \quad \text{and} \quad \alpha_s = 1$$

3.5.9 High frequency impedance

The frequency spectrum on IC applications can be classified in the following fashion

- Low frequencies ($f \leq 500MHz$, i.e. $R >> \omega\mathcal{L}$) negligible inductance effects, static resistance and Capacitance suffices to describe wires.

- Mid frequencies ($500MHz < f < 10GHz$, i.e. $R > \omega\mathcal{L}$), while $\omega\mathcal{L}$ non negligible. Uniform current distribution, inductance changes with frequency due to

proximity effects. $R\mathcal{L}C$ distributed description applies. Dynamic Resistance replaces static resistance. R changes with frequency.

- High frequencies ($10GHz < f < 40GHz$, i.e $\omega\mathcal{L}$ comparable to or larger than R), current ceases to be uniform inside the conductors and as frequency increases it crowds towards the surfaces. Proximity effects continues to play a role.

Consider the last regime, where current inside the conductors ceases to be uniform. In order to account for the physics of current crowding[§], the conductors are broken into filaments, to discretize the non constant current distribution. The current distribution in each filament of small transverse area is considered uniform across its area (chapter 2). For a bundle with wires partitioned into filaments, this results in a linear system of the form:

$$\mathbf{ZI} = \mathbf{V},$$

where $\mathbf{Z}$ is the partial impedance matrix including all filaments contained in a wire segment, $\mathbf{I}$ is the vector of unknown currents at each filament and $\mathbf{V}$ the vector of voltages. Given a bundle (one signal plus return wires in parallel), the voltage vector $\mathbf{V}$ is given by

$$\begin{aligned} V_i &= V_{in} - V_{out} \quad \text{if } i \in \text{signal wire} \\ V_i &= -V_{out} \quad \text{otherwise.} \end{aligned} \tag{3.28}$$

The value V_{out} is the unknown voltage at the end of the signal line (Fig. 3.8). Without loss of generality we assume $V_{in} = 1$v. We solve this system in the following fashion, call

$$\mathbf{x} = \mathbf{Z}^{-1}\mathbf{e} \tag{3.29}$$

$$\mathbf{y} = \mathbf{Z}^{-1}\mathbf{1} \tag{3.30}$$

with vector $\mathbf{e}$ the vector with ones for filaments in the signal wire, and zero for the rest of the filaments. The vector $\mathbf{1}$ is a vector with all entries equal to 1.

With $\mathbf{x}$ and $\mathbf{y}$ the $\mathbf{ZI} = \mathbf{V}$ system can be rewritten as

[§]The reader is invited at the end of this chapter where a discussion about frequency phenomena, together with an informal demonstration of skin and proximity effects are presented

$$\mathbf{I} = \mathbf{x} - V_{out}\mathbf{y}$$

Since the sum of all currents in I has to be zero (Kirchoff's law) the unknown voltage V_{out} is given by

$$V_{out} = \frac{\sum \mathbf{x}}{\sum \mathbf{y}}$$

with $\sum \mathbf{x}$ and $\sum \mathbf{y}$ the sum of the elements in $\mathbf{x}$ and $\mathbf{y}$, respectively. Therefore the unknown vector I is given by

$$\mathbf{I} = \mathbf{x} - \frac{\sum \mathbf{x}}{\sum \mathbf{y}}\mathbf{y}$$

The loop impedance of the bundle is then given by the inverse of the current going through the signal wire. This current is equal to the sum of currents passing through the filaments into which the signal was partitioned, i.e.

$$Z_{loop} = \left(\sum_{i \in \text{signal}} I_i \right)^{-1}$$

Volumetric discretization

Currents in a conductor's cross-section crowds near its surface as the frequency increases. In unidimensional treatment, the current inside the conductor decays exponentially going inside from the surface [25]. An important parameter to measure the current crowding is the skin depth. This is the distance from the conductor's surface where 63% $(1 - 1/e)$ of the total current is concentrated (Fig 3.11. The formula for the skin depth is given by [25]:

$$\delta = \left(\sqrt{\pi \mu \sigma f} \right)^{-1} \tag{3.31}$$

with σ the conductivity of the metal (e.g. $\sigma = 5.8 \times 10^7$ $\mho$/m for copper), μ the magnetic permeability, i.e. for non ferromagnetic material $\mu = \mu_0 = 4\pi \times 10^{-7}$ H/m and f the frequency.

To take advantage of this exponential decay, we partition the conductor into filaments with transverse dimensions that increase exponentially as we move towards the center. In Figure 3.12 the partitioning is shown:

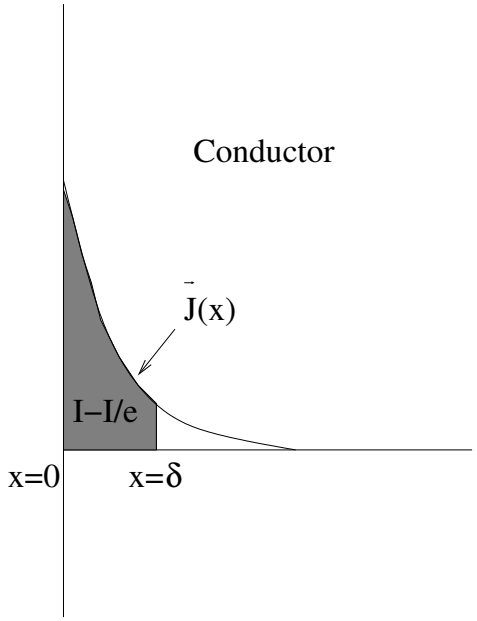


Figure 3.11: Unidimensional Current distribution of a conductor.

Filaments width and thickness follows the following parametrization

$$w_i = \lambda^i w_0 \quad \text{and} \quad t_i = \lambda^i t_0$$

where w_0 and t_0 are the width and thickness of the filaments at the corners. For a given frequency and λ we find the optimal number of filaments into which the wire is going to be partitioned. We force the extra condition to be fulfilled

$$w_0(1+\lambda) < \delta \quad \text{and} \quad t_0(1+\lambda) < \delta$$

to ensure an accurate discretization of the conductor's volume.

3.6 Mutual impedance

We are interested in the impedance coupling between signal nets in an IC. Given the size and the number of nets a design can have, it is expensive to compute the mutual impedance among all nets. We only consider the interaction among signal wires that have survived filtering (section 3.5.1). We take advantage of the fracturing already per-

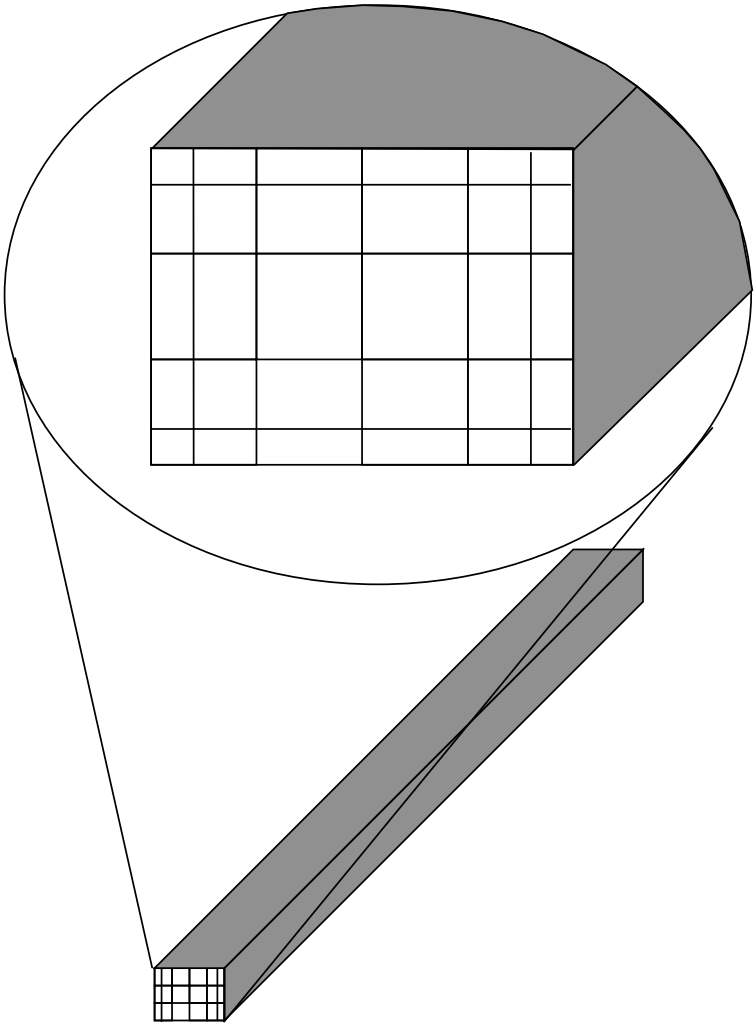


Figure 3.12: A Conductor partitioned into filaments

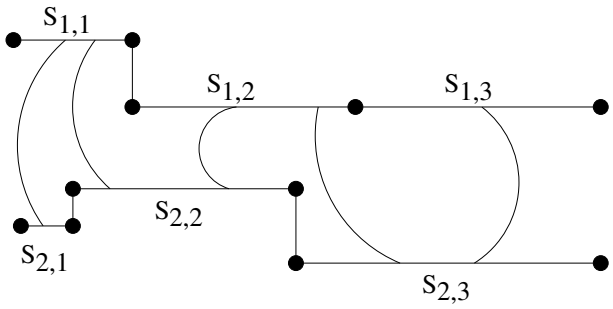


Figure 3.13: Two signal nets as partitioned in the PDB. For clearness not all couplings are shown.

formed when the wires are included into the PDB. The resulting mutual loop impedance between two signal paths will be distributed according to this fracturing of wires. In Fig. 3.13 this idea is illustrated. In the figure, the black dots represent the boundaries of each signal segment in the PDB. The curved lines represent the inductive coupling among the segments. Each segment will be represented as a resistance in series with an inductance, as seen in previous sections. Each segment in a signal path is coupled with all the segments in another signal path.

To compute the mutual loop impedance associated with two signal segments we need to compute the mutual impedance between two loops, each one of them consisting of the signal segments and its corresponding return paths. In the self impedance step, each signal and its return path is represented as the series connection of bundles. Therefore, the total mutual loop impedance between the two signal segments is equal to the sum of the mutual impedance values among the bundles in one signal segment and the bundles in the other signal segment.

In the following section we explain in detail how the loop mutual impedance between two bundles is computed.

3.6.1 Mutual impedance between two bundles

Each bundle of size $n + 1$ can be thought as a parallel connection of n simple loops (Fig. 3.14). Each loop being formed by the signal and one wire in the return path. The mutual coupling between two bundles is then the weighted sum of the magnetic coupling between all loops in one bundle and all loops in the other bundle. The weights coefficients given by the percentage of the total current going through each loop, i.e. the values of alpha computed with (3.21).

We approximate the mutual impedance between two bundles with the following expression [49]:

$$Z_{a,b} = j\omega \sum_{i \in a} \sum_{j \in b} \alpha_i \alpha_j \mathcal{L}_{i,j} \tag{3.32}$$

where $\mathcal{L}_{i,j}$ is the partial inductance between segment i in bundle a and segment j in bundle b. The current coefficients α_i and α_j correspond to the current coefficients computed in the self impedance step. The coefficients alpha are complex numbers. The resulting real part of $Z_{a,b}$ is known as the mutual resistance between the two bundles.

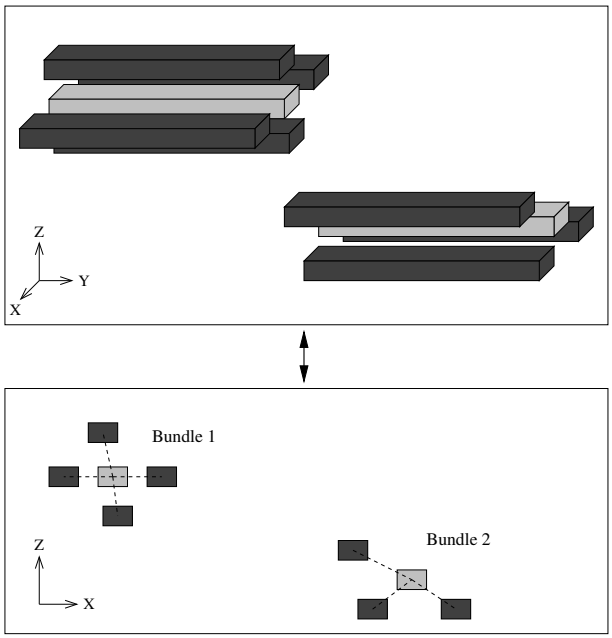


Figure 3.14: A system of 2 bundles. The signal line in light gray, the ground wires in dark gray

3.6.2 Accuracy

We refer the reader to section 3.8 where the accuracy of this methodology is demonstrated with a testcase.

3.6.3 Detailed implementation

As a function of separation, the mutual loop inductance between two closed circuits falls off, at long distances, with the square (in $2D$) or cube (in $3D$) of the distance between the centers of the loops [49]. We are therefore interested in those signal loops that are "close" to the victim signal loop.

In order to implement these notions we proceed as follows:

1. Given the victim signal path, we define its "interaction cylinder" of diameter W, as in Fig. 3.15, with W such that there are ground/power wires along the entire cylinder.

2. We consider "aggressors" those signals that stay close to the victim during most of its journey. In other words, those signal wires that have most of their length

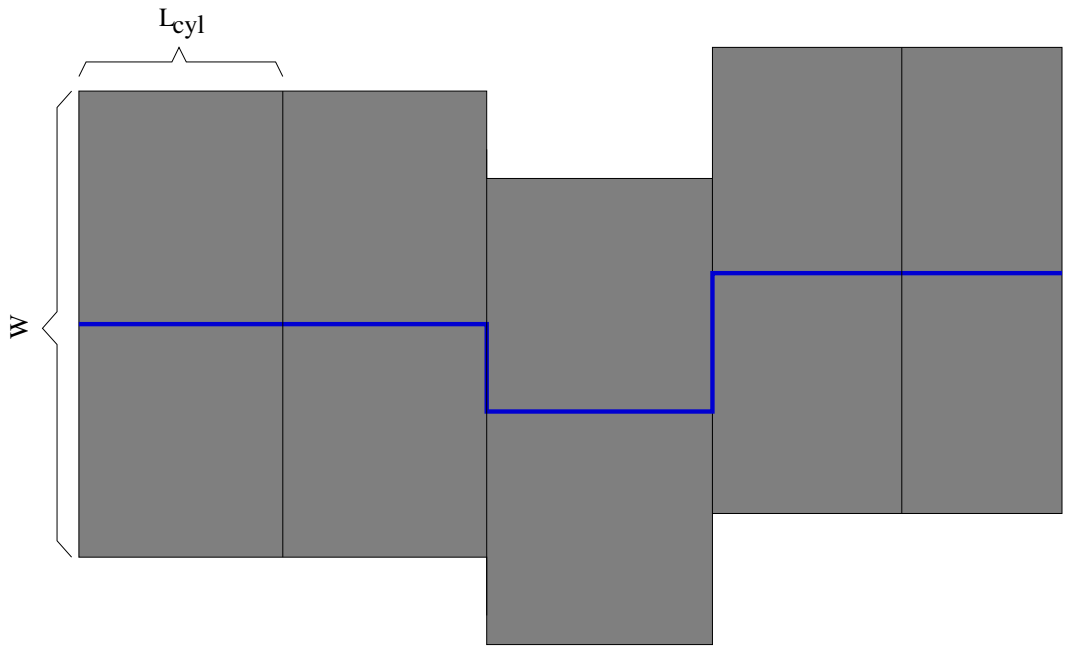


Figure 3.15: Interaction cylinder.

inside the victim's interaction cylinder. From experiments we have found that using a coverage of 70% results in a good compromise between accuracy and performance. This value is adjustable.

3. This cylinder is cut in pieces of length L_{cyl}. This cut results in regions that we call "interaction regions". We do this so as to assure that mutual inductance among signal segments in different interaction regions be small enough so as to discard them. In Fig. 3.16 an exemplary interaction region is shown. Signal S2 is considered as the aggressor of signal S1.

4. To compute the mutual impedance between a wire segment in the victim signal and another wire segment in any of the aggressors we perform bundling, as for the self impedance but considering only two ground returns. In Fig. 3.17 the bundling of both the victim and the aggressor is Fig. 3.16 is displayed. The mutual impedance values between bundles in the victim and bundles in the aggressors are computed.

5. Mutual impedance between any pair of bundles within an interaction region are computed. Mutual impedance between bundles belonging to different interaction

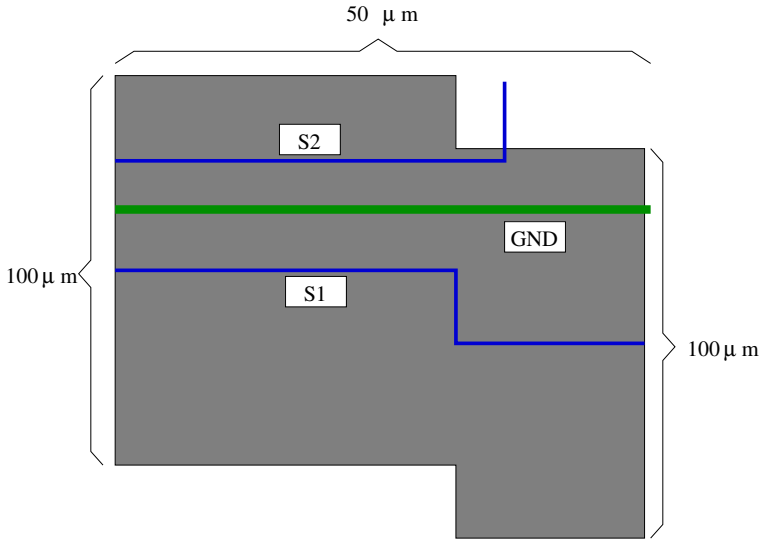


Figure 3.16: Interaction region. Other signal lines omitted for simplicity.

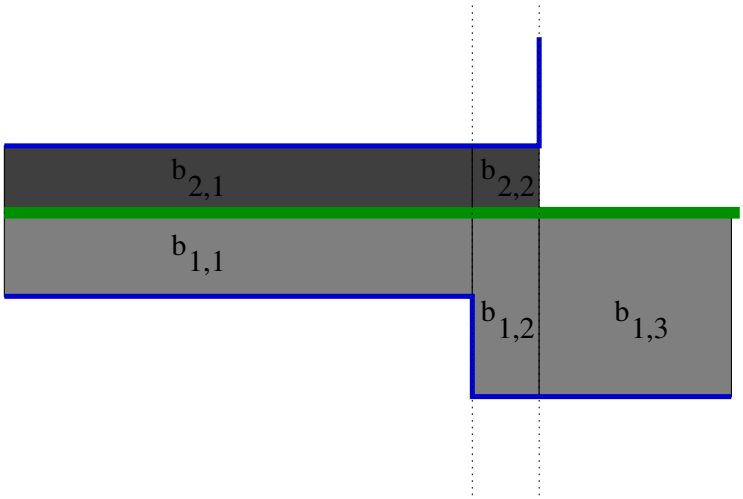


Figure 3.17: Bundling in the interaction region.

regions is neglected.

Given that bundles are connected in series, the mutual impedance between a wire segment in the victim and another wire segment in the aggressor is given by the algebraic sum of all mutual impedances between the bundles in which the victim segment was fractured and the bundles in which the aggressor segment was fractured:

$$Z_{S_1,S_2} = \sum_{a \in S_1} \sum_{b \in S_2} Z_{a,b} \tag{3.33}$$

where $Z_{a,b}$ is given in (3.32).

3.7 Mutual and self impedance in the presence of a ground plane

When a ground plane participates as return path for currents, in general its width is much larger than the skin depth δ for any except very low frequencies. Therefore, skin effect like computations, are mandatory for ground planes, starting at the lowest frequencies in which inductance is important (nearly 1 GHz).

We discuss here the inclusion of ground planes for the general treatment of self and mutual impedance. We present the method with an example, with as many subtleties as reasonable to envision. Simultaneously, we wish the reader to understand that the implementation is obviously more general.

We consider all signal wires and ground planes starting and beginning in the same perpendicular. For signals with different length the layout can be fractured as to fulfill this premise. We show this in Fig. 3.18.

Consider as example a configuration consisting of 3 ground planes with 7 signal lines as displayed in figure 3.19. The problem consists in finding the impedance matrix of the configuration in which each signal line chooses the three ground planes as return path.

Current density in a ground plane, at any but very low frequencies is larger nearest the signal and decreases as we separate from the signal (see section 3.9). For this reason, we finely partition the ground plane in the "shadow" of the signal wires. The farther we are from the shadow of a signal line, the more homogeneous the current in the ground plane will be. We partition the cross-section of the ground plane with filaments whose

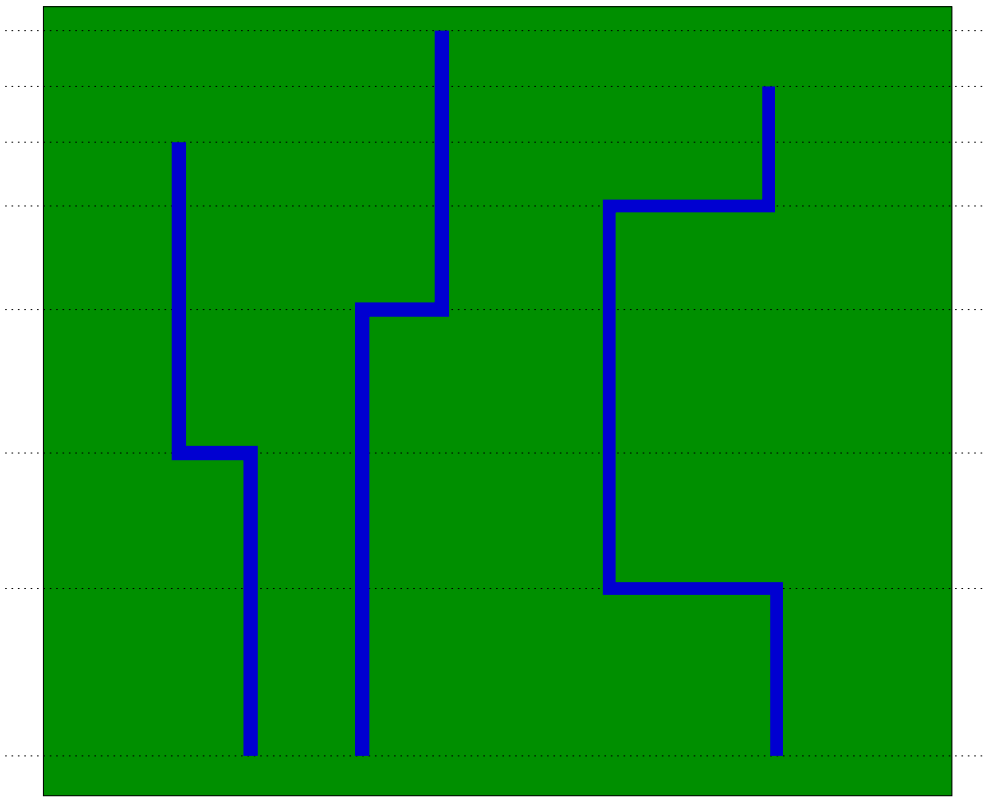


Figure 3.18: Partitioning the layout so as to have wires with same length.

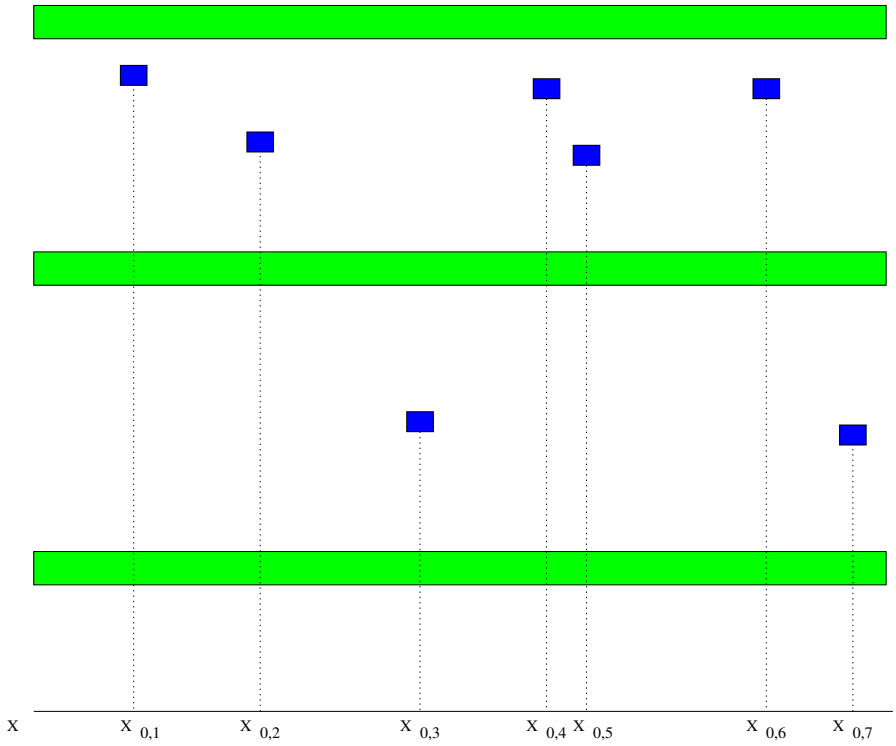


Figure 3.19: Cross section view of an exemplary configuration with $n = 10$ conductors (7 signals, 3 ground planes).

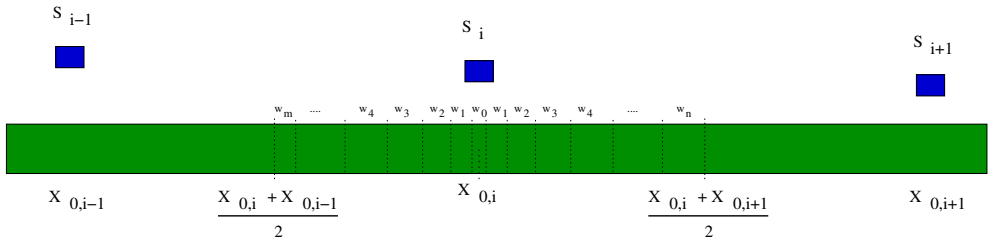


Figure 3.20: Partitioning of the ground plane in the shadow of signal i.

width increases exponentially with the distance to the center of the signal's shadow. The partition of the ground plane is therefore signal dependent.

For signal i, we break the ground plane with an exponential partitioning starting from the center of each signal's shadow. The method is trivial for a single signal line. For multiple signals, we increase exponentially the width of the cross-sections and we stop at the center of the shadows of two neighbor signals, as seen in figure 3.20.

In detail: we start with a filament of width w_0 centered at $x_{0,i}$. The x coordinates of the center of each filament and their respective widths are stored in four vectors using the following recursion:

To the right:

$$\begin{aligned} w^+(i) &= w^+(i-1)\delta_w \\ x^+(i) &= x^+(i-1) + 0.5(w^+(i-1) + w^+(i)) \end{aligned} \tag{3.34}$$

To the left:

$$\begin{aligned} w^-(i) &= w^-(i-1)\delta_w \\ x^-(i) &= x^-(i-1) - 0.5(w^-(i-1) + w^-(i)) \end{aligned} \tag{3.35}$$

with $w^+(1) = w^-(1) = w_0$, $x^-(1) = x^+(1) = x_{0,i}$ and $\delta_w > 1$ the growth coefficient.

Notice that the last width on the right or on the left may not correspond exactly to the one obtained with the recursion given in (3.34) or (3.35). Its value is adjusted so as to exactly cover the interval.

Once the ground planes are partitioned, we proceed to compute the partial impedance matrix for a given frequency f consisting of the self impedance of all the signals and all the ground plane filaments, and the mutual impedance values among themselves, i.e:

$$Z(i,i) = R_i + j(2\pi f \mathcal{L}_i) \quad \text{and} \quad Z(i,k) = j(2\pi f \mathcal{L}_{i,k}). \tag{3.36}$$

with R_i and $\mathcal{L}_i$ the static resistance and the partial inductance of filament i, respectively. $\mathcal{L}_{i,k}$ the partial mutual inductance between filaments i and k.

Reduced impedance matrix

Given n_s signal segments and n_g ground planes of same length. Call m the total number of filaments into which the signal segments and the ground planes are partitioned. The $n_s \times n_s$ loop impedance matrix Z can be computed from the $m \times m$ partial impedance matrix $\tilde{Z}$ in the following fashion:

1. For $i = 1, \ldots, n_s$,

   1.1 solve the linear system $\tilde{Z} I_i = V_i$, with V_i formed as: for $k = 1, \ldots, m$, $V_i(k) = 1$ if filament k belongs to conductor i and $V_i(k) = 0$, otherwise.

   1.2 create a vector I of size n_s: for $k = 1, \ldots, n_s$, $I(k) = \sum_{r \in \text{cond } k} I_i(r)$

   1.3 assign to the i-th column of the $n_s \times n_s$ matrix Y the vector I

   end for

2. Invert the $n_s \times n_s$ matrix Y to obtain Z.

Since n_s linear systems will be solved using the same matrix $\tilde{Z}$ we can decompose the matrix using our modified version of the LDL^T factorization for complex and symmetric matrices (see section 3.5.6) to reduce the $O(n_s m^3)$ operations into $O(m^3 + n_s * m^2)$ operations.

Validation

The above method was implemented and tested. We exemplify with a configuration as the one shown in Fig. 3.19, with the following parameters:

- Length of the wires: 1000 μm
- Thickness of the signal wires: 1.5 μm

- Thickness of the ground planes: 1 μm
- Width of signal wires: 1.5 μm
- Width of ground planes: 1000 μm
- Position of the signal wires: $x_{0,1} = -400$ μm, $x_{0,2} = -300$ μm, $x_{0,3} = -200$ μm, $x_{0,4} = 200$ μm, $x_{0,5} = 250$ μm, $x_{0,6} = 350$ μm and $x_{0,7} = 450$ μm. The ground planes are centered at $x = 0$ μm
- Height of the ground planes: first one at $z = 0$ μm, second one at $z = 3$ μm and third one at $z = 9$ μm
- Height of the signal wires: signal 1, 4 and 6 at $z = 4$ μm; signal 2 and 5 at $z = 5$ μm; signal 3 and 7 at $z = 2$ μm

The error in computing the 7×7 impedance matrices with our algorithm vis-a-vis the matrix produced using FastHenry [6] is less than 1% up to the maximum frequency tested (20 GHz). The resistance vector and the inductance matrix from our methodology are:

```
    | 9.13 |
    | 9.19 |
    | 11.1 |
R = | 9.13 |
    | 9.19 |
    | 9.13 |
    | 11.1 |

    | 3.05e-10 1.13e-16 5.67e-18 9.18e-18 4e-18    8.46e-18 5.86e-18 |
    | 1.13e-16 3.05e-10 1.05e-17 4.79e-18 1.96e-18 3.78e-18 2.1e-18  |
    | 5.67e-18 1.05e-17 1.54e-10 2.93e-18 1.27e-18 3.2e-18  3.52e-18 |
L = | 9.18e-18 4.79e-18 2.93e-18 3.05e-10 5.35e-16 9.41e-17 6.67e-18 | H
    | 4e-18    1.96e-18 1.27e-18 5.35e-16 3.05e-10 1.12e-16 3.71e-18 |
    | 8.46e-18 3.78e-18  3.2e-18 9.41e-17 1.12e-16 3.05e-10 1.77e-17 |
    | 5.86e-18  2.1e-18 3.52e-18 6.67e-18 3.71e-18 1.77e-17 1.54e-10 |
```

From FastHenry:

$$
R = \begin{vmatrix} 9.12614 \\ 9.18347 \\ 11.05080 \\ 9.12615 \\ 9.18347 \\ 9.12614 \\ 11.05080 \end{vmatrix}
$$

$$
L = \begin{vmatrix} 3.04e\text{-}10 & 1.21e\text{-}16 & 6.81e\text{-}18 & 1.07e\text{-}17 & 4.77e\text{-}18 & 1e\text{-}17 & 7.3e\text{-}18 \\ 1.21e\text{-}16 & 3.04e\text{-}10 & 5.41e\text{-}18 & 5.58e\text{-}18 & 2.31e\text{-}18 & 4.51e\text{-}18 & 2.69e\text{-}18 \\ 6.81e\text{-}18 & 5.41e\text{-}18 & 1.54e\text{-}10 & 3.63e\text{-}18 & 1.62e\text{-}18 & 3.98e\text{-}18 & 4.42e\text{-}18 \\ 1.07e\text{-}17 & 5.58e\text{-}18 & 3.63e\text{-}18 & 3.04e\text{-}10 & 3.47e\text{-}16 & 1.05e\text{-}16 & 8.43e\text{-}18 \\ 4.77e\text{-}18 & 2.31e\text{-}18 & 1.62e\text{-}18 & 3.47e\text{-}16 & 3.04e\text{-}10 & 1.19e\text{-}16 & 4.54e\text{-}18 \\ 1e\text{-}17 & 4.51e\text{-}18 & 3.98e\text{-}18 & 1.05e\text{-}16 & 1.19e\text{-}16 & 3.04e\text{-}10 & 1.74e\text{-}17 \\ 7.3e\text{-}18 & 2.69e\text{-}18 & 4.42e\text{-}18 & 8.43e\text{-}18 & 4.54e\text{-}18 & 1.74e\text{-}17 & 1.54e\text{-}10 \end{vmatrix} H
$$

Notice that the differences in the offdiagonal terms of the inductance matrix are important, but these terms are, in most of the cases, eight orders of magnitude smaller than those in the diagonal. This difference are simply due to numerical errors.

External and independent validation

Independent validation of the ground plane method has been performed by a well known taiwanese foundry. Their battery of testcases consisted in 528 different configurations. The 528 configurations are divided in four groups:

1. One signal wire on top of one ground plane (Fig. 3.21.a)

2. One signal wire with a ground plane above and a second ground plane below (Fig. 3.21.b)

3. Two signal lines with a ground plane above and a second ground plane below (Fig. 3.21.c)

4. Two signal lines with a ground plane above and a second ground plane below and with two ground wires in the same plane (Fig. 3.21.d)

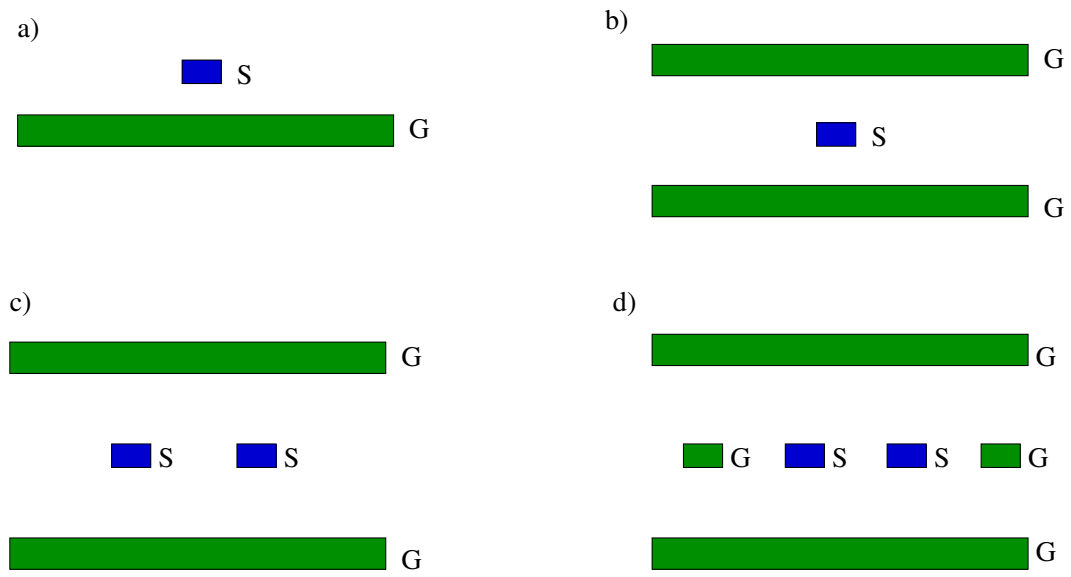


Figure 3.21: The four types of ground plane configuration

Varying the thickness, width and position of the wires and ground planes, as well as their length, their edge-to-edge separation, and the frequency of operation produced the 528 configurations.

Comparisons were made by the foundry against their "gold results". In Figures 3.22, 3.23 and 3.24 we present the histogram of the distribution of the relative errors between our tool and the gold results for self inductance of the signals, self resistance, and mutual inductance between the two signals for the configurations belonging to groups 3 and 4 (188 of the total), respectively. A further study of the "gold data" used by the validator, shown that the presence of outliers was due to misuse of the tool to generate the gold results.

3.8 Testcase validation for IC

We designed a testcase to validate our impedance extraction methodology. The layout consists of two signal lines surrounded by 4 ground lines. We generate two netlists, the first one, with partial elements computed as in the PEEC approach, the second one, using our loop impedance extraction flow. The interconnect layout with its geometrical characteristics is shown in Fig. 3.25. In both approaches, the lines were broken into wire segments with length smaller than 100 μm. We do this to ensure a good distributed

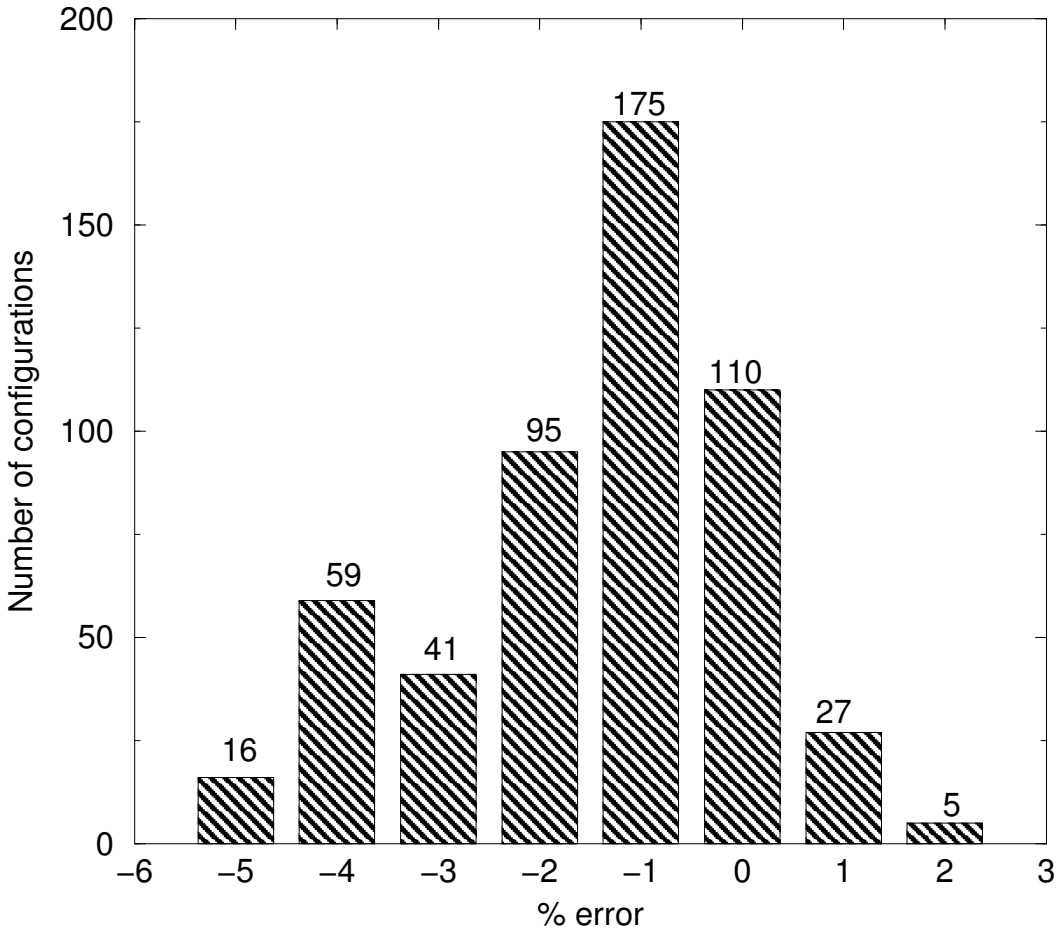


Figure 3.22: Distribution of relative error for loop resistance of signal wires

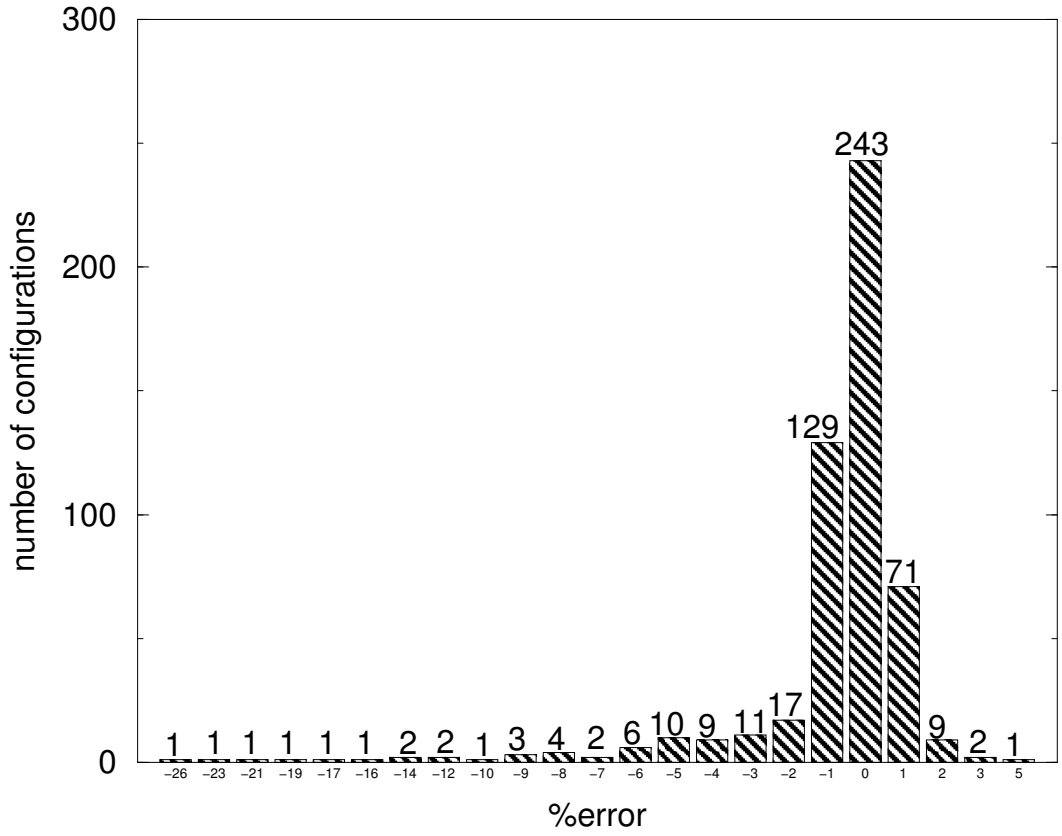


Figure 3.23: Distribution of relative error for loop inductance of signal wires

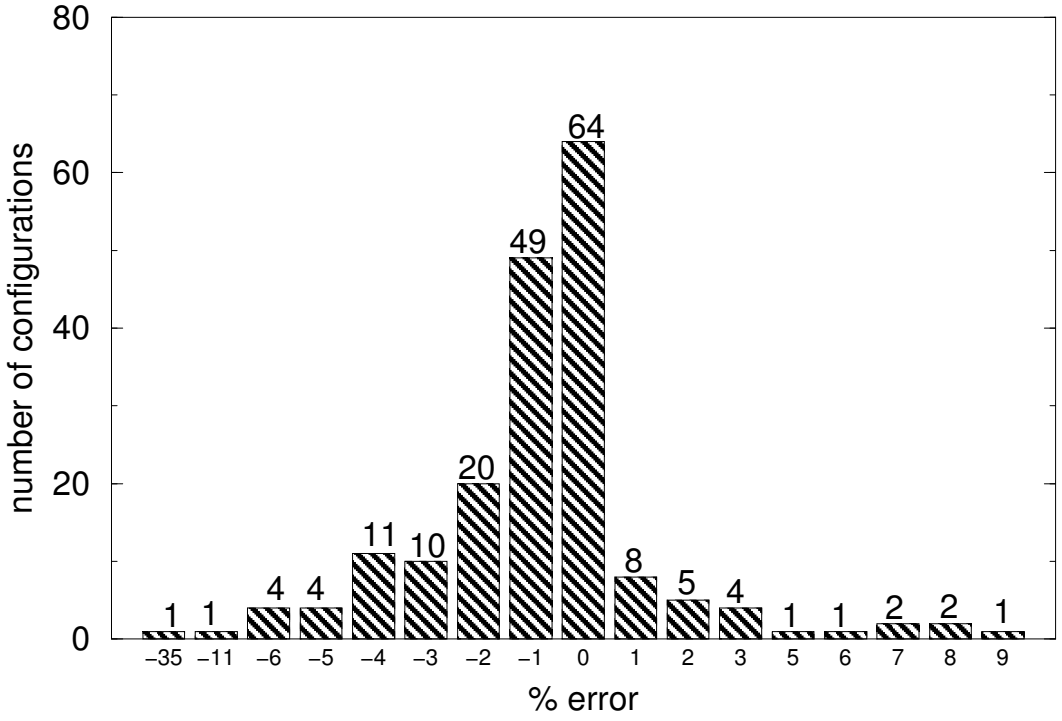


Figure 3.24: Distribution of relative error for mutual inductance between signal wires

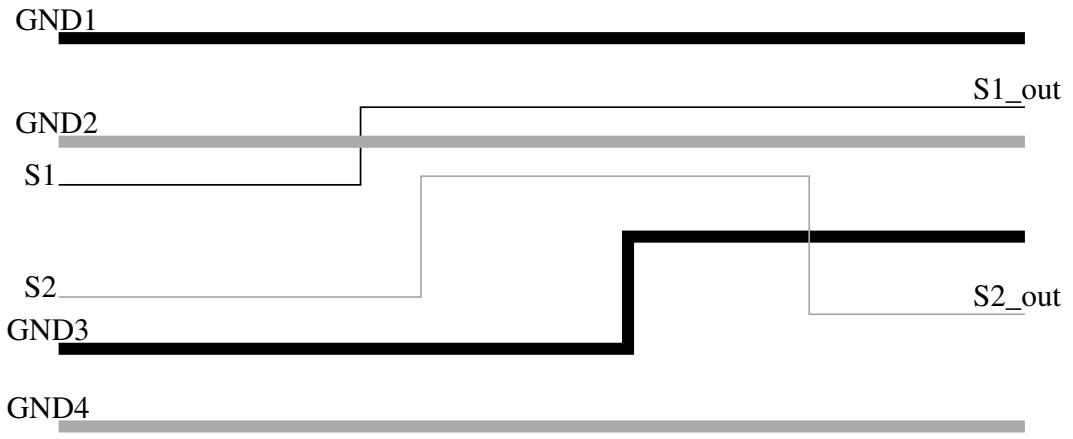


Figure 3.25: IC configuration. The length of the wires is 1mm, the width of signal S1 and S2 is 1μm, the width of grounds G1, G2, G3 and G4 is 5μm. Wires in black are in a metal layer 1μm thick those in gray are in a metal layer 0.75μm thick.

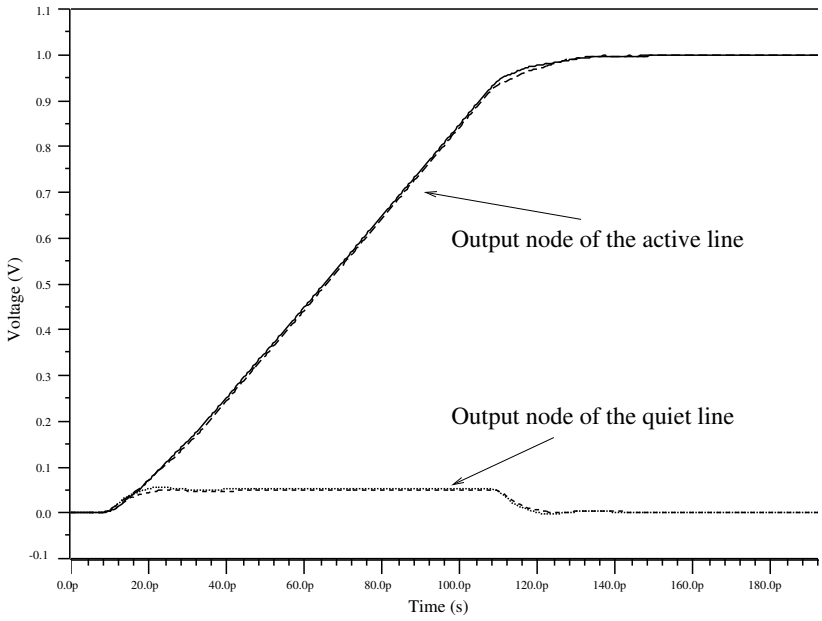


Figure 3.26: Voltage at the output nodes of both the quiet and the active line.

representation of the wires. For the timing analysis we fed the signal line S1 with a Heaviside voltage pulse of 1 volt and left the signal S2 quiet. The idea is to compare the responses of the active and the quiet line (noise), analyzing both the PEEC and the loop netlists, such as to validate our loop self and mutual impedance methodology. We simulate the presence of devices (drivers and receivers) at the ends of each line with a resistor of value $R_{tr} = 50\Omega$ at nodes S1 and S2 and a capacitor to ground of value $C_{load} = 1$fF at the node S1_out and S2_out. The capacitance among signal segments and between signal segments and ground are included. These are computed in the preprocessing part of the extraction, as we mentioned in section 3.2.

In Fig. 3.26 the waveforms at the nodes S1_out and S2_out as a function of time for both netlists are presented. The waveforms coming from the loop approach sit well on top of those coming from the PEEC approach. Our loop approach overestimates the maximum peak of noise in the quiet line by 10%, a very good precision for noise analysis.

Performance of standard timing simulators such as Eldo [36] or HSpice [37] depends on the size of the input netlist. The size of a netlists is determined by two parameters: the number of elements and the number of nodes. To understand what is an

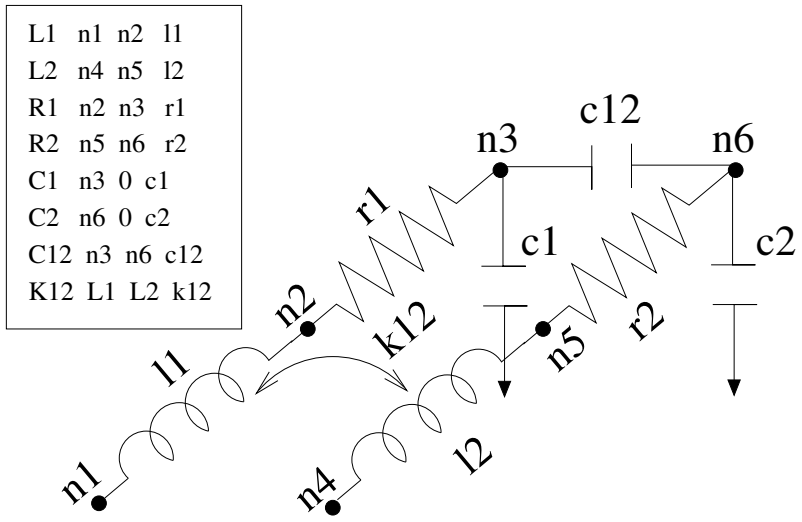


Figure 3.27: The circuit representation of a typical netlist in Spice syntax. The number of nodes is 6, the number of elements is 8.

element and what is a node see Fig. 3.27 where a netlist and its corresponding circuit representation are displayed.

In table 3.1 the number of RLC elements in both netlists is shown. With the loop impedance method the number of impedance coupling elements is reduced to 5% of the original PEEC number. The number of nodes has been reduced to a third of the original PEEC number, due to the fact that ground wire segments are now implicitly considered in our treatment. For this reason the number of capacitors also reduces to a third of those in the original PEEC netlist. The number of circuit elements reduces to 10% of the elements in the original PEEC netlist. This results in an obvious improvement of performance: it takes five times more CPU time to analyze the PEEC netlist than the netlist produced with our methodology.

3.8.1 Performance in real-life designs

We present performance results of our impedance extraction tool when used in three real-life designs:

1. testcase 1: a digital design with 12000 transistors

2. testcase 2: a digital design with 235000 transistors

	resistors	inductors	capacitors	impedance couplings	Total	Average run time (s)
PEEC	70	70	118	2415	2673	10.2
Loop	26	26	34	128	214	1.9

Table 3.1: Number of RLC elements in both the PEEC netlist and the netlist produced by our loop impedance extraction flow. Impedance couplings correspond to both mutual inductance and mutual resistance.

Testcase	CPU time (s)	memory (MB)	PDB wire segments	No. of nets
1	241	80	363040	21923
2	3027	158	287183	109165
3	5883	513	213105	1596940

Table 3.2: Runtime of impedance extraction for three digital IC's.

3. testcase 3: a 32-bit RISC microcomputer

In table 3.2 we present results in CPU time and memory usage for impedance extraction. The third column corresponds to the number of wire segments in the PDB after the preprocessing and the filtering parts were done. The last column corresponds to the number of nets[¶] in the design. Runs were performed in a Sun Fire V-210 server with dual 1GHz-processor and 4GB of RAM.

We observe how the run for testcase 3, that has fewer PDB wire segments to consider than both testcase 2 and testcase 1, consumes the most in CPU time. This is due to the filtering, since testcase 3 has 10 times more nets to prequalify (section 3.5.1) than testcase 2. Without the filtering step, the testcase 3 run would take 100 times more CPU time to finish and also 100 times more memory. This shows how important the filtering step is for complex designs.

Our tool has proven to be able to handle complex designs like this RISC microprocessor in less than 2 hours and using a very modest amount of memory. There are no known alternative methods with this level of performance and compactness that provide the field solver accuracy achieved by our tool.

[¶]A collection of wire segments electrically connected

3.9 Frequency dependence of the current distribution

The current distribution $\vec{J}$ within each conductor depends on the frequency of operation.

For frequencies in which skin depth δ is smaller than transverse dimensions, the resistance of a conductor grows as the inverse of δ, i.e. the resistance grows as the square root of the frequency [29]. Furthermore, the inductance of a wire tends to an asymptotic finite value. This means that the ratio $r/j\omega\mathcal{L}$ tends to zero when omega tends to infinity, i.e. the reactance part of the impedance dominates the resistance. The currents in the interior of the cross-section crowd into the portions nearer the surface of the wire so to minimize the dominant term of the impedance, i.e. the inductance.

This can be seen from the solution to (2.25) for a conductor which has been broken into m equal filaments. This complex system can be solved using the associated real system [46]

$$\left(\begin{array}{c|c} \mathbf{R} & -\omega\mathcal{L} \\ \hline \omega\mathcal{L} & \mathbf{R} \end{array}\right)\left(\begin{array}{c} \mathbf{I}^{re} \\ \hline \mathbf{I}^{im} \end{array}\right) = v_{io}\left(\begin{array}{c} \mathbf{u_m} \\ \hline \mathbf{0} \end{array}\right) \tag{3.37}$$

where $\mathbf{R}$ and $\mathcal{L}$ are the partial resistance and partial inductance matrices of the m filaments, respectively. The vectors $\mathbf{I}^{re}$ and $\mathbf{I}^{im}$ are the real and imaginary parts of the vector $\mathbf{I}$, respectively.

In the low frequency regime, where the impedance is completely dominated by its real part, we can neglect the imaginary part of $\mathbf{Z}$. The system (3.37) becomes a diagonal system. The trivial solution to this system is the $\mathbf{I}^{re}$ with entries equal to the inverse of the resistance of the corresponding filament times the term v_{io} and $\mathbf{I}^{im} = 0$. Since all filaments have the same resistance, then all entries in the solution vector will be identical, i.e. homogeneous current distribution.

In the high frequency limit, it is the imaginary part $\omega\mathcal{L}$ that dominates. We can neglect the real part of $\mathbf{Z}$. Therefore system (3.37) can be written as the two real systems

$$\begin{aligned} -\omega\mathcal{L}\mathbf{I}^{im} &= v_{io}\mathbf{u_m} \quad \text{and} \\ \omega\mathcal{L}\mathbf{I}^{re} &= \mathbf{0}. \end{aligned} \tag{3.38}$$

Since the inductance matrix $\mathcal{L}$ is non singular, the second system directly implies $\mathbf{I}^{re} = \mathbf{0}$.

In our magneto-quasistatic approximation all currents inside filaments flow in the

same direction, therefore signs of the entries in $\mathbf{I}^{im}$ are the same. From the first system in (3.37) we conclude that all entries in $\mathbf{I}^{im}$ are negative.

From the above results, the vector $\tilde{\mathbf{I}}$ defined as $\tilde{\mathbf{I}} = -\mathbf{I}^{im}$ is solution to the real system

$$\omega\mathcal{L}\tilde{\mathbf{I}} = v_{io}\mathbf{u_m}. \tag{3.39}$$

Since $\mathcal{L}$ is symmetric and positive definite, so it is $\omega\mathcal{L}$. Therefore, the solution vector $\tilde{\mathbf{I}}$ for the above system is the unique vector that minimizes the associated quadratic functional [50]

$$\omega\tilde{\mathbf{I}}^T\mathcal{L}\tilde{\mathbf{I}} - v_{io}\tilde{\mathbf{I}}^T\mathbf{u_m}. \tag{3.40}$$

The above functional can be rewritten as

$$\omega\sum_{i=1}^{m}\sum_{j=1}^{m}\mathcal{L}_{ij}\,\tilde{I}_i\,\tilde{I}_j - v_{io}\sum_{i=1}^{m}\tilde{I}_i. \tag{3.41}$$

The second term in (3.41) goes unbounded to $-\infty$ due to the fact that entries in the vector $\tilde{\mathbf{I}}$ are positive. The first term, on the contrary grows unbounded as the square of the currents. The minimum is attained by giving maximum magnitude to pairs of entries i and j in the solution such that their companion coefficients $\mathcal{L}_{ij}$ are the smallest ones. From (2.21) the element $\mathcal{L}_{ij}$ is given by

$$\mathcal{L}_{ij} = \left(\frac{\mu_0}{4\pi a_i a_j}\int_{\bar{\Omega}_i}\int_{\bar{\Omega}'_j}\frac{\mathbf{l}_i\cdot\mathbf{l}_j}{\|\vec{x}-\vec{x}'\|}d\Omega' d\Omega\right). \tag{3.42}$$

The coefficients $\mathcal{L}_{ij}$ decrease with the distance between the filaments. Therefore, in a equi-partitioned wire with square cross-section, the filaments in the four corners will have the smallest $\mathcal{L}_{ij}$ terms among them and hence their corresponding current magnitude I_i and I_j will be the largest so as to minimize the first term in (3.42). This can be seen in Fig. 3.28 where currents in an isolated wire with rectangular cross-section tend to crowd to the corners of the conductor when frequency increases. In this figure the real part of the impedance matrix is not neglected and the complete system is solved numerically for a large value of m. What is printed in the figure is the magnitude of the entries in the solution current vector. The figure shows that our result is indeed the asymptotic behavior of the current distribution when ω grows. This effect is known as

the "skin effect".

Furthermore, the presence of other conductors in the vicinity changes the distribution of the currents traveling inside the conductor. This is known as the "proximity effect". Consider for instance two parallel conductors. We feed one end of each conductor with a sinusoidal voltage v_{io} and each of the other ends connected to ground. Fracturing both conductors into n filaments each, the corresponding linear system for this configuration is

$$\left(\begin{array}{c|c} \mathbf{Z_{a,a}} & \mathbf{Z_{a,b}} \\ \hline \mathbf{Z_{b,a}} & \mathbf{Z_{b,b}} \end{array}\right)\left(\begin{array}{c} \mathbf{I_a} \\ \hline \mathbf{I_b} \end{array}\right) = v_{io}\left(\begin{array}{c} \mathbf{u_m} \\ \hline \mathbf{u_m} \end{array}\right) \qquad \mathbf{ZI} = v_{io}\mathbf{u_{2m}} \tag{3.43}$$

with $\mathbf{Z_{a,a}}$ and $\mathbf{Z_{b,b}}$ the partial impedance matrix of filaments in conductor a and conductor b, respectively. The off-diagonal term being the partial mutual inductance between filaments in conductor a and filaments in conductor b. The associated real system for (3.43) is given by

$$\left(\begin{array}{cc|cc} \mathbf{R_{a,a}} & \mathbf{0} & -\omega\mathcal{L}_{\mathbf{a,a}} & -\omega\mathcal{L}_{\mathbf{a,b}} \\ \mathbf{0} & \mathbf{R_{b,b}} & -\omega\mathcal{L}_{\mathbf{b,a}} & -\omega\mathcal{L}_{\mathbf{b,b}} \\ \hline \omega\mathcal{L}_{\mathbf{a,a}} & \omega\mathcal{L}_{\mathbf{a,b}} & \mathbf{R_{a,a}} & \mathbf{0} \\ \omega\mathcal{L}_{\mathbf{b,a}} & \omega\mathcal{L}_{\mathbf{b,b}} & \mathbf{0} & \mathbf{R_{b,b}} \end{array}\right)\left(\begin{array}{c} \mathbf{I_a}^{re} \\ \mathbf{I_b}^{re} \\ \hline \mathbf{I_a}^{im} \\ \mathbf{I_a}^{im} \end{array}\right) = v_{io}\left(\begin{array}{c} \mathbf{u_m} \\ \mathbf{u_m} \\ \hline \mathbf{0} \\ \mathbf{0} \end{array}\right) \tag{3.44}$$

Once again, for the low frequency limit the linear system (3.44) can be approximated to a diagonal system with trivial solution $I_i^{re} = v_{io}/R_{ii}$ and $I_i^{im} = 0$. In other words, uniform current distribution among filaments.

For the high frequency limit we neglect the real part of $\mathbf{Z}$. This lead us to two real systems

$$\begin{aligned} -\omega\left(\begin{array}{c|c} \mathcal{L}_{\mathbf{a,a}} & \mathcal{L}_{\mathbf{a,b}} \\ \hline \mathcal{L}_{\mathbf{b,a}} & \mathcal{L}_{\mathbf{b,b}} \end{array}\right)\left(\begin{array}{c} \mathbf{I_a}^{im} \\ \hline \mathbf{I_b}^{im} \end{array}\right) &= v_{io}\left(\begin{array}{c} \mathbf{u_m} \\ \hline \mathbf{u_m} \end{array}\right) \\ \text{and} \quad \omega\left(\begin{array}{c|c} \mathcal{L}_{\mathbf{a,a}} & \mathcal{L}_{\mathbf{a,b}} \\ \hline \mathcal{L}_{\mathbf{b,a}} & \mathcal{L}_{\mathbf{b,b}} \end{array}\right)\left(\begin{array}{c} \mathbf{I_a^{re}} \\ \hline \mathbf{I_b^{re}} \end{array}\right) &= v_{io}\left(\begin{array}{c} \mathbf{0} \\ \hline \mathbf{0} \end{array}\right) \end{aligned} \tag{3.45}$$

the second system implies $\mathbf{I_a^{re}} = \mathbf{0}$ and $\mathbf{I_b^{re}} = \mathbf{0}$

We consider the case in which currents in one conductor flow opposite to the currents in the other conductor. This condition can be forced by changing the right hand side of the first system in (3.45) to

$$v_{io}\begin{pmatrix}\mathbf{u_m}\\ \hline -\mathbf{u_m}\end{pmatrix} \tag{3.46}$$

The resulting real system is

$$\begin{gathered}\omega\left(\begin{array}{c|c}\mathcal{L}_{\mathbf{a,a}} & \mathcal{L}_{\mathbf{a,b}}\\ \hline \mathcal{L}_{\mathbf{b,a}} & \mathcal{L}_{\mathbf{b,b}}\end{array}\right)\begin{pmatrix}\mathbf{I_a}^{im}\\ \hline \mathbf{I_a}^{im}\end{pmatrix} = v_{io}\begin{pmatrix}-\mathbf{u_m}\\ \hline \mathbf{u_m}\end{pmatrix}\\ \omega\mathcal{L}\mathbf{I}^{im} = v_{io}\mathbf{u'_{2m}}.\end{gathered} \tag{3.47}$$

The block inductance matrix is positive definite, therefore the solution vector $\mathbf{I}^{im} = [\mathbf{I_a^{im}}\mathbf{I_b^{im}}]^T$ to (3.47) is the unique minimum of the functional

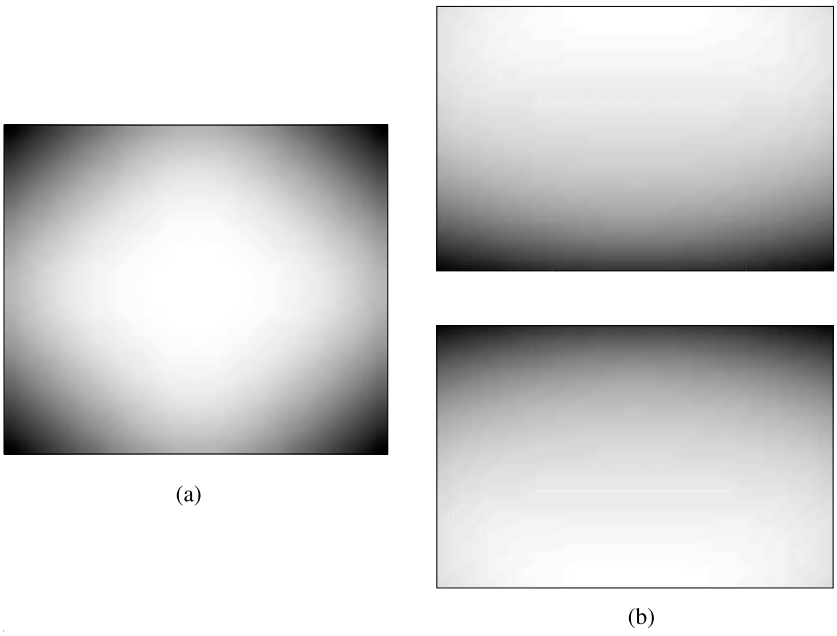
$$\mathbf{I}^{im^T}\mathcal{L}\mathbf{I}^{im} - v_{io}\mathbf{I}^{im^T}\mathbf{u'_{2m}}. \tag{3.48}$$

The above functional can be rewritten as

$$\sum_{i=1}^{m}\sum_{j=1}^{m}\left[(\mathcal{L}_{\mathbf{a,a}})_{ij}\,(\mathbf{I_a}^{im})_i\,(\mathbf{I_a}^{im})_j + (\mathcal{L}_{\mathbf{b,b}})_{ij}\,(\mathbf{I_b}^{im})_i\,(\mathbf{I_b}^{im})_j + 2(\mathcal{L}_{\mathbf{a,b}})_{ij}\,(\mathbf{I_a}^{im})_i\,(\mathbf{I_b}^{im})_j\right] - v_{io}\sum_{i=1}^{2m}\tilde{I}_i. \tag{3.49}$$

The first two terms in the double summation are always positive, since they correspond to multiplication of currents in the same conductor. The third term are negative since currents in filaments of conductor a are opposite to currents in in filaments of conductor b. For this reason, the largest entries in $\mathbf{I}^{im}$ will be those that maximize these negative terms. In other words, they are those $(\mathbf{I_a}^{im})_i$ and $(\mathbf{I_b}^{im})_j$ such that the coefficients $(\mathcal{L}_{\mathbf{a,b}})_{ij}$ are the largest ones. The largest inductance values between filaments in conductor a and filaments in conductor b are of those filaments at minimum distance. This can be seen in Fig. 3.28.(b) where the currents of two conductors crowd to their facing sides when both currents travel in opposite direction.

If currents in both conductors go in the same direction the minimum of (3.49) is attained when the third term in the summation, which is now positive, is minimized, i.e. currents will crowd in the farthest points of the conductors.



(a)

(b)

Figure 3.28: Current distribution at 10GHz, darker color means more current. (a) cross-section of an isolated conductor (Skin effect). (b) two facing conductors with opposite currents (Skin and proximity effects).

Chapter 4

Intentional inductors

Inducteurs intentionnels

Résumé

Les dispositifs communiquants ont bénéficie de beaucoup d'attention ces dernières années. Un grand effort a été investi pour que ces dispositifs puissent communiquer entre eux sans utiliser de fils électriques. Les dispositifs précédents étaient encombrants, or l'espace a toujours été un souci. Les nouvelles avancées dans la conception d'IC ont rendu possible l'intégration des émetteurs-récepteurs à l'intérieur d'une micro-plaquette. Non seulement la taille des dispositifs a été réduite mais également la robustesse de leur intercommunication s'est bien améliorée.

Les composants clefs dans un émetteur-récepteur sont ses dispositifs passifs. Dans ce chapitre nous focalisons notre attention dans un des dispositifs passifs : l'inducteur. Une brève discussion au sujet des inducteurs intentionnels et de leur représentation électrique est présentée. Nous développons une méthode et les expressions pour calculer l'impédance d'entrée d'un inducteur intentionnel, valable tant pour les basses que pour les hautes fréquences. Nous completons avec une méthode pour calculer l'impédance mutuelle entre deux inducteurs intentionnels.

4.1 Introduction

Communicating devices are getting a lot of attention during the last years. Plenty of effort has been invested in making these devices communicate among themselves wirelessly. Previous devices were bulky and space was a concern. New advances in IC design have made possible to integrate transceivers inside a single chip.

Important components in a transceiver are the passive devices. In this chapter we will focus our attention in one of these passive devices: the inductor.

When designing an inductor an important factor to consider is its self-resonance frequency. This is the frequency at which the current traveling the inductor is maximum. Another important factor in designing an inductor is the "quality factor" Q. The higher the value of Q the more energy can be stored for a given loss. The quality factor of an inductor is mainly determined by its physical layout, the material used in its construction and the dielectric in which the inductor has been placed. Designers face a big challenge, they need transceivers fitting in a single chip, operating at a given frequency with minimum loss. The availability of tools to accurately predict the electromagnetic parameters of an inductor during the design stage is paramount to the success of its correct operation.

This chapter is divided as follows:

In section 4.2 a brief discussion about intentional inductors and their electrical representation is presented. In section 4.3 we present the methodology and expressions to compute the self impedance of an intentional inductor, at low and high frequency. In section 4.4 we formulate the computational scheme for mutual impedance between intentional inductors. The coupled approach in which all inductors are treated together is presented. In section 4.5 we present a method to compute impedance of a system of n-inductors by considering each inductor separately. In this section the coupled approach and ours are contrasted in terms of complexity. In section 4.6 we extend the self impedance model with the inclusion of capacitance couplings in the intentional inductors. This we do so as to be able to capture the self-resonance frequency, otherwise not feasible. A validation testcase to our method is presented in section 4.8. We conclude this chapter in section 4.7 with some details regarding our implementation.

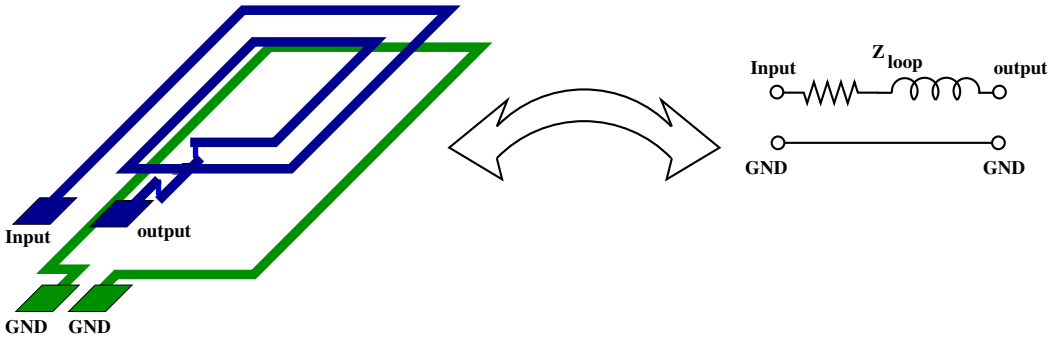


Figure 4.1: The equivalent loop RL circuit of a two-port inductor configuration

4.2 Intentional inductors

Consider the inductor configuration as a two-port system: The input, output and ground nodes, as shown in Fig. 4.1. In real circuits these ground nodes would be metal pads connected to a resistive substrate or ground plane. In our approximate treatment we consider the two ground nodes as connected by a perfect conductor, therefore electrically equivalent. This approximation is accurate as long as the input and output nodes are located sufficiently close to each other so as to minimize the impedance of the path between the ground nodes permitting us to represent the inductor as a closed loop.

4.2.1 Self resonance frequency and quality factor

The self-resonance frequency is the frequency f_{res} for which the current traveling the inductor is maximum. The impedance of a serial RLC tank, as shown in Fig. 4.2, is given by

$$Z = R + j\left(\omega\mathcal{L} - \frac{1}{\omega C}\right) \tag{4.1}$$

The maximum current passing through the tank is attained when the imaginary part of Z is zero, i.e. for f_{res} such that

$$f_{res} = \frac{1}{2\pi\sqrt{\mathcal{L}C}} \tag{4.2}$$

Intentional inductors are devices that store energy dissipating a small amount of it. The dissipation of energy is minimized when the quality factor Q is maximum. The

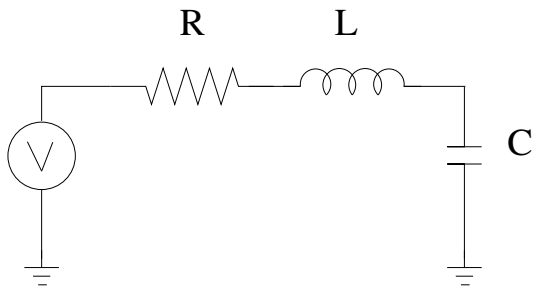


Figure 4.2: A serial RLC tank

quality factor Q is given by the expression [51]

$$Q = \frac{\omega\,(W_m + W_e)}{P_l} \tag{4.3}$$

with $\omega = 2\pi f$, the angular frequency; W_m and W_e the time average of the stored magnetic and electric energy, respectively; and P_l the average power dissipated.

A minimum value of P_l and maximum values of W_m and W_e results in the maximum quality factor. Below the self resonance frequency, the quality factor is well approximated by [51]

$$Q_{ind} = \frac{\omega\mathcal{L}}{R} \tag{4.4}$$

For a general inductor at any frequency, the quality factor is given by [51]

$$Q_{ind} = \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})} \tag{4.5}$$

with Z_{in} the input impedance. In our work, we use (4.5) as the quality factor of an intentional inductor.

4.3 Self impedance

Short circuiting the output node of the inductor to ground and injecting a potential difference V_1 between the input node of the inductor and ground, generates a loop current I_{loop} on the inductor. This current is determined using Ohm's law in the frequency domain:

$$Z_{\mathrm{loop}}(f) I_{\mathrm{loop}}(f) = V_1 \tag{4.6}$$

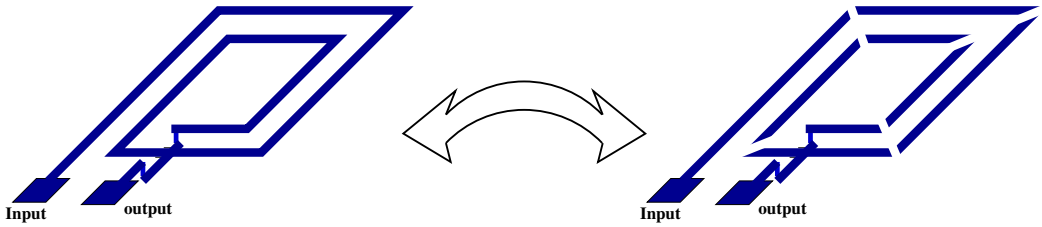


Figure 4.3: Breaking the inductor into segments

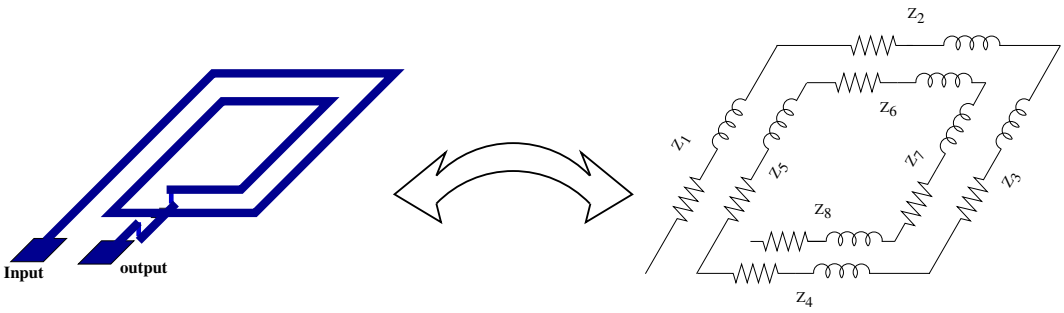


Figure 4.4: The equivalent lumped RL circuit of a two-port inductor configuration. For simplicity mutual inductance between segments is not presented, but taken into account in our study.

where Z_{loop} is the loop impedance of the inductor and f the frequency. In the absence of capacitive effects, the real part of Z_{loop} corresponds to the loop resistance of the inductor and its imaginary part corresponds to the loop self inductance of the inductor times $\omega = 2\pi f$, the angular frequency.

An intentional inductor is built as a concatenation of n rectilinear segments, as seen in Fig. 4.3. Each segment i is described as a RL lumped element with resistance and partial self inductance R_i and $\mathcal{L}_i$, respectively, as shown in Fig. 4.4. Although not shown in the figure, we consider the mutual inductance between segments i and j that we denote as $\mathcal{L}_{ij}$. Inductors in IC design are made of metal wires with rectangular cross-section, the partial values of inductance, as well as the resistance of each segment, can be computed using the equations compiled in table 2.2 and 2.3.

Currents and voltage drops in each segment of the inductor are related by the following linear system:

$$\begin{pmatrix} Z_{1,1} & Z_{1,2} & \dots & Z_{1,n} \\ Z_{2,1} & Z_{2,2} & \dots & Z_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{n,1} & Z_{n,2} & \dots & Z_{n,n} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \end{pmatrix} = \begin{pmatrix} V_1 - V_2 \\ V_2 - V_3 \\ \vdots \\ V_n - V_{n+1} \end{pmatrix} \tag{4.7}$$
$$\mathbf{ZI} = \mathbf{V}$$

With $Z_{i,j}$ the partial mutual impedance between segment i and segment j and I_j the current in segment j. The value V_j is the voltage at node j, where V_1 is the input voltage and V_{n+1} is the output voltage. For $i = j$, $Z_{i,i}$ is the partial self impedance of segment i. This linear system has n current unknowns, I_i, as well as $n-1$ nodal voltages unknowns, V_i. Applying Kirchoff's currents law (KCL) at each node results in $I_1 = I_2 = \ldots = I_n$. This reduces the current unknowns to only one common current. Therefore the linear system is complete. We can sum all rows of system (4.7) and end with a single equation $Z_{\text{loop}} I = V_1 - V_{n+1}$ with Z_{loop} given as

$$Z_{\text{loop}} = \sum_{i=1}^{n} R_i + j\omega \left(\sum_{i=1}^{n} \mathcal{L}_i + \sum_{i=1}^{n} \sum_{j=1}^{n} \mathcal{L}_{ij} \right), \tag{4.8}$$

with ω the angular frequency, i.e. $\omega = 2\pi f$, where f is the frequency. This result was first introduced by Greenhouse [52].

4.3.1 Self impedance at high frequency

In chapter 3, we showed that at high frequencies current inside a conductor ceases to be uniform. Volumetric methods as FastHenry [6] discretize the volume of the straight conductor with rectangular cross-section into several "filaments". Each filament being a segment with transversal dimensions small enough as to assure constant current through its cross-section. For a high frequency model we use volumetric discretization.

We start by breaking each segment in the inductor into m filaments, as shown in Fig. 4.5.

Given that currents along the cross-section crowd around the borders of the inductor, a reasonable partitioning scheme would be one in which filaments at the boundaries of the segment have smaller cross-section than those in the middle of the conductor. This is what tools as FastHenry do. Notice in Fig. 4.5 the increase of the filaments' width

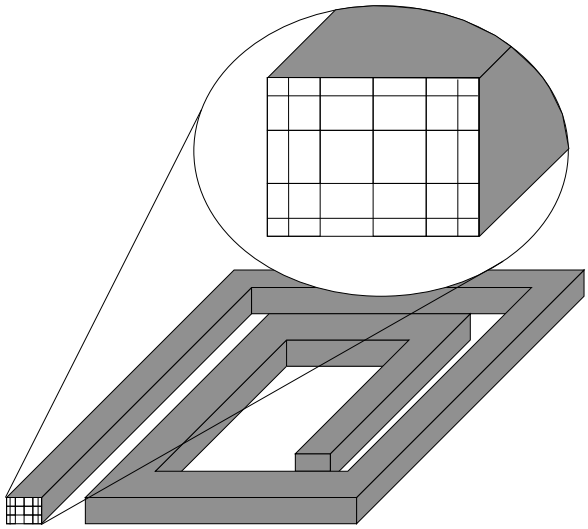


Figure 4.5: Non-uniform partitioning of the inductor's cross-section

and thickness when we approach the cross-section's center.

The associated KVL linear system for this new circuit written in block form is identical to the linear system in (4.7). The extension is that each scalar $Z_{i,j}$ in the $\mathbf{Z}$ matrix is replaced by a submatrix defined as the mutual impedance matrix between filaments in segment i and filaments in segment j:

$$\mathbf{Z_{i,j}} = \begin{pmatrix} j\omega\mathcal{L}_{i1,j1} & j\omega\mathcal{L}_{i1,j2} & \dots & j\omega\mathcal{L}_{i1,jm} \\ j\omega\mathcal{L}_{i2,j1} & j\omega\mathcal{L}_{i2,j2} & \dots & j\omega\mathcal{L}_{i2,jm} \\ \vdots & \vdots & \ddots & \vdots \\ j\omega\mathcal{L}_{im,j1} & j\omega\mathcal{L}_{im,j2} & \dots & j\omega\mathcal{L}_{im,jm} \end{pmatrix} \tag{4.9}$$

with $\mathcal{L}_{ik,jr}$ the partial mutual inductance between the k-th filament in segment i and the r-th filament in conductor j.

When $i = j$ the scalar $Z_{i,i}$ is replaced by the impedance matrix among the filaments of segment i, i.e:

$$\mathbf{Z_{i,i}} = \begin{pmatrix} R_{i1} + j\omega\mathcal{L}_{i1} & j\omega\mathcal{L}_{i1,i2} & \dots & j\omega\mathcal{L}_{i1,im} \\ j\omega\mathcal{L}_{i2,i1} & R_{i2} + j\omega\mathcal{L}_{i2} & \dots & j\omega\mathcal{L}_{i2,im} \\ \vdots & \vdots & \ddots & \vdots \\ j\omega\mathcal{L}_{im,i1} & j\omega\mathcal{L}_{im,i2} & \dots & R_{im} + j\omega\mathcal{L}_{im} \end{pmatrix} \tag{4.10}$$

With R_{ik} and $\mathcal{L}_{ik}$ the resistance and partial self inductance of the k-th filament in segment i, respectively.

Each current I_1 in (4.7) is replaced by a subvector of the form:

$$\mathbf{I_j} = \begin{pmatrix} I_{j1} \\ I_{j2} \\ \vdots \\ I_{jm} \end{pmatrix} \tag{4.11}$$

where I_{jk} is the value of current in the k-th filament of segment j.

Similarly, the vector $\mathbf{V}$ at the right hand side of (4.7) is replaced by a block vector $\mathbf{V}$:

$$\mathbf{V} = \begin{pmatrix} \mathbf{V_1} \\ \mathbf{V_2} \\ \vdots \\ \mathbf{V_n} \end{pmatrix} \tag{4.12}$$

To reduce the size of the problem, the unknown voltage drop in all filaments within a segment is taken to be equal to the unknown average voltage drop between the two end faces of the conductor. The block elements in (4.12) are therefore:

$$\mathbf{V_j} = \left.\begin{pmatrix} V_j - V_{j+1} \\ V_j - V_{j+1} \\ \vdots \\ V_j - V_{j+1} \end{pmatrix}\right\} m \text{ times} \tag{4.13}$$

The block version of system (4.7) consists of $m \times n$ unknown currents and $n - 1$ unknown node voltages. Furthermore, due to current conservation, the total current in one segment must be equal to the total current going through the next segment. Therefore, the sum of filament currents in one segment will be equal to the sum of filament currents in the next segment. The remaining $n - 1$ equations are given by

$$\sum_{k=1}^{m} I_{ik} = \sum_{k=1}^{m} I_{(i+1)k}, \text{ for } \; i = 1, \ldots, n-1 \tag{4.14}$$

The block version of system (4.7) together with (4.14) can be rewritten as a single

$(m * n + n - 1)^2$ system of the form

$$\left(\begin{array}{c|c} \mathbf{Z} & \mathbf{A} \\ \hline \mathbf{A}^T & \mathbf{N} \end{array}\right)\left(\begin{array}{c} \mathbf{I} \\ \hline \tilde{\mathbf{V}} \end{array}\right) = \left(\begin{array}{c} \mathbf{V}_{\text{io}} \\ \hline \mathbf{0} \end{array}\right) \tag{4.15}$$

With block $\mathbf{A}$ defined as

$$\mathbf{A} = \left(\begin{array}{cccccc} -1 & 0 & 0 & 0 & & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots \\ -1 & 0 & 0 & 0 & & 0 \\ \hline 1 & -1 & 0 & 0 & & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots \\ 1 & -1 & 0 & 0 & & 0 \\ \hline 0 & 1 & -1 & 0 & & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots \\ 0 & 1 & -1 & 0 & & 0 \\ \hline \vdots & \vdots & \vdots & \vdots & & \vdots \\ \hline 0 & 0 & 0 & 0 & & 1 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots \\ 0 & 0 & 0 & 0 & & 1 \end{array}\right) \tag{4.16}$$

The n blocks in (4.16) have m rows and $n-1$ columns each. Block $\mathbf{N}$ is the $(n-1)\times(n-1)$ null matrix. In the unknowns, $\tilde{\mathbf{V}}$ corresponds to the $n-1$ unknown nodal voltages $\tilde{\mathbf{V}} = (V_2 \;\; V_3 \;\; \ldots \;\; V_n)^T$.

In the independent vector, $\mathbf{V}_{\text{io}}$ is given by

$$\mathbf{V}_{\text{io}} = \left(\begin{array}{c} V_1 \\ \vdots \\ V_1 \\ 0 \\ \vdots \\ 0 \\ -V_{n+1} \\ \vdots \\ -V_{n+1} \end{array}\right) \begin{array}{l} \left.\begin{array}{c} \\ \\ \\ \end{array}\right\} m \text{ times} \\ \left.\begin{array}{c} \\ \\ \\ \end{array}\right\} m(n-2) \text{ times} \\ \left.\begin{array}{c} \\ \\ \\ \end{array}\right\} m \text{ times} \end{array} \tag{4.17}$$

and vector $\mathbf{0}$ is the null vector of size $n-1$.

The current in each segment is given by the sum of currents flowing through each filament in which the segment has been broken into. According to (4.14) the total current in one segment is equal to that in the other segments. This means that the total current I flowing through the inductor must fulfill the relationship:

$$ZI = V_1 - V_{n+1} \tag{4.18}$$

with Z the input-output impedance of the inductor, the value we are interested to compute. We close the circuit, i.e. make $v_{n+1} = 0v$ and set input potential of $v_1 = 1v$. We solve for $\mathbf{I}$ in (4.15) with these boundary conditions. From (4.14), the total current going through the inductor is equal to the current going through the first segment, i.e., the sum of the first m entries in $\mathbf{I}$. From the total current we can compute

$$Z_{\text{loop}} = \left(\sum_{k=1}^{m} I_{1k} \right)^{-1} \tag{4.19}$$

This frequency dependent loop impedance is in fact the loop impedance of the inductor taken as a two-port RL circuit with one of the ports short circuited.

4.4 Mutual impedance between inductors

Designers frequently use multiple intentional inductors in an IC. Each one of these devices occupies an amount of real estate on the chip in the order of 100 μm^2. Design and manufacturing considerations favor placing the different inductors closely spaced so as to minimize the occupied area and as such improve on the manufacturing yield. To be able to do it safely, a quantitative measure of the electromagnetic noise that one inductor induces on another is essential. We attempt to compute the noise.

4.4.1 Frequencies much smaller than f_{res}

Given two inductors a and b partitioned into $n^{(a)}$ and $n^{(b)}$ rectilinear segments, respectively. The associated KVL system, written in block form, is given by:

$$\left(\begin{array}{c|c} \mathbf{Z_{a,a}} & \mathbf{Z_{a,b}} \\ \hline \mathbf{Z_{b,a}} & \mathbf{Z_{b,b}} \end{array} \right) \left(\begin{array}{c} \mathbf{I_a} \\ \hline \mathbf{I_b} \end{array} \right) = \left(\begin{array}{c} \mathbf{V_a} \\ \hline \mathbf{V_b} \end{array} \right) \tag{4.20}$$

where $\mathbf{Z_{a,a}}$ and $\mathbf{Z_{b,b}}$ are the segment-segment partial self impedance matrices of inductor a and b, respectively (see (4.7)). These diagonal blocks are size $n^{(a)} \times n^{(a)}$ and $n^{(b)} \times n^{(b)}$, respectively. The offdiagonal block elements correspond to the partial mutual inductance between segments in inductor a and segments in inductor b times the angular frequency ω. The size of these blocks is $n^{(a)} \times n^{(b)}$ and $n^{(b)} \times n^{(a)}$. Block elements $\mathbf{I_a}$ and $\mathbf{I_b}$ correspond to the currents in the respective inductor. Block elements $\mathbf{V_a}$ and $\mathbf{V_b}$ are the nodal voltages at the respective inductor. The size of the total system is $(n^{(a)} + n^{(b)})^2$

This system is reducible to a 2×2 system. The diagonal elements in this reduced matrix are the loop self impedance of each inductor; its offdiagonal elements correspond to the mutual impedance between the two inductors. This reduction can be done in two steps, one in which inductor a is active and inductor b quiet and the second step just the other way around.

In the 2×2 total system what we are looking for is the two current vectors such that:

$$\mathbf{ZI_1} = \begin{pmatrix} 1 \\ 0 \end{pmatrix} \tag{4.21}$$

and

$$\mathbf{ZI_2} = \begin{pmatrix} 0 \\ 1 \end{pmatrix} \tag{4.22}$$

Trivially, the current matrix $\mathbf{Y}$ with columns equal to vectors $\mathbf{I_1}$ and $\mathbf{I_2}$ is the inverse of the impedance matrix Z.

To solve the system (4.20) we proceed as follows: in a first step we make the inductor a active by injecting an input/output voltage difference of $V_1 - V_0 = 1v$, this creates voltages at each node in the inductor. The voltage vector $\mathbf{V_a}$ is therefore equal to:

$$\mathbf{V_a} = \begin{pmatrix} 1 - V_2 \\ V_2 - V_3 \\ \vdots \\ V_n \end{pmatrix} \tag{4.23}$$

and $\mathbf{V_b}$ is set to zero to make inductor b quiet. In the second step we interchange a and b.

For each one of these two steps we solve (4.20) for currents in each inductor. Since currents in all segments are identical, the total current in one inductor will be equal to the current of the first segment. We then construct the matrix $\mathbf{Y}$ as:

$$\mathbf{Y} = \begin{pmatrix} \mathbf{I}_{\mathbf{a}1}^{I} & \mathbf{I}_{\mathbf{a}1}^{II} \\ \mathbf{I}_{\mathbf{b}1}^{I} & \mathbf{I}_{\mathbf{b}1}^{II} \end{pmatrix} \tag{4.24}$$

where superindices I and II represent at what step the current column was computed.

Inverting this 2×2 matrix results in the matrix $\mathbf{Z}$ of loop impedance we are interested in:

$$\mathbf{Z} = \begin{pmatrix} Z_a & Z_{a,b} \\ Z_{b,a} & Z_b \end{pmatrix} \tag{4.25}$$

From the off-diagonal element $Z_{a,b}$ we can obtain the coupling coefficient between the two inductors. This is a figure of merit for noise analysis. It is defined as:

$$\kappa = \frac{\mathcal{L}_{a,b}}{\sqrt{\mathcal{L}_a \mathcal{L}_b}} = \frac{\mathrm{Im}(Z_{a,b})}{\sqrt{\mathrm{Im}(Z_a)\mathrm{Im}(Z_b)}} \tag{4.26}$$

For a passive system, the eigenvalues of the matrix $\mathrm{Im}(\mathbf{Z})/\omega$ are positive. This means that the determinant of the matrix has to be positive, i.e.

$$\det(\mathcal{L}) = \mathcal{L}_a \mathcal{L}_b - \mathcal{L}_{a,b}^2 \geq 0 \tag{4.27}$$

condition (4.27) trivially leads to $|\kappa| \leq 1$.

4.4.2 Frequencies around or above f_{res}

At higher frequencies, the two inductors are broken into filaments as the one-inductor case. Block elements Z_a and Z_b in (4.20) become themselves block matrices with block elements in the diagonal given as in(4.10) and in the offdiagonal as in (4.9). The offdiagonal block elements $\mathbf{Z_{a,b}}$ and $\mathbf{Z_{b,a}}$ in (4.20) correspond to block matrices with elements given by the mutual impedance among filaments of inductor a and inductor b.

Segments in inductors a and b are broken into $m^{(a)}$ and $m^{(b)}$ filaments, respectively. We recall that inductors a and b were broken into $n^{(a)}$ and $n^{(b)}$ rectilinear segments, respectively. This makes of (4.20) a dense linear system of size $(n^{(a)}m^{(a)} + n^{(b)}m^{(b)})^2$.

We do as for the low frequency case: to activate one inductor at a time in order to look for the 2×2 impedance matrix. Due to the current redistribution at each node of the inductors, the total current of each inductor will be equal to the sum of currents inside the filaments of their first segments. The matrix $\mathbf{Y}$ is in this case given by

$$\mathbf{Y} = \begin{pmatrix} \sum_{k=1}^{m} I_{1k}^{I} & \sum_{k=1}^{m} I_{1k}^{II} \\ \sum_{k=1}^{m} I_{1k}^{I} & \sum_{k=1}^{m} I_{1k}^{II} \end{pmatrix} \tag{4.28}$$

and the loop impedance matrix for the configuration is as before given as $\mathbf{Z}_{\text{loop}} = \mathbf{Y}^{-1}$.

4.5 Approximations to full impedance extraction

Finding the impedance matrix of a 2-inductor system can become expensive. Furthermore, the 2-inductor linear system generalizes easily to a n-inductor linear system. The complexity of the linear system grows rapidly with the number of inductors and becomes rapidly unmanageable.

We propose an alternative method to compute the loop impedance matrix $\mathbf{Z}$ in (4.25) without requiring to explicitly solve the huge associated linear system. Our methodology is based in the approximation that current distribution in the segments of an inductor is not affected by the presence of another inductor.

We have verified by means of simulations that the modification of current distribution in a "victim" inductor due to the "aggressor" decays rapidly with their separation. For edge-edge distances of about 30 μm between the victim and the aggressor, the variation in current and hence the variation in the self impedance of the victim inductor accounts to less than 1% for tested configurations. Furthermore, we found that for frequencies as high as 30 GHz the presence of an aggressor inductor, at this distance, does not affect the current distribution inside the volume of the victim inductor.

We compute Z_a and Z_b separately. During a second step, compute $Z_{a,b}$ with the low frequency approximation given as the sum of all mutual inductance between segments in one inductor and all segments in the other, i.e:

$$Z_{a,b} = j\omega \sum_{i=1}^{n^{(a)}} \sum_{k=1}^{n^{(b)}} \mathcal{L}_{ik} \tag{4.29}$$

4.5.1 Complexity of the coupled approach

Consider the general case of two inductors a and b with respectively $n^{(a)}$ and $n^{(b)}$ number of segments and with $m^{(a)}$ and $m^{(b)}$ filaments per segment, we define the size of the configuration as the total number of filaments in the configuration:

$$N = n^{(a)}m^{(a)} + n^{(b)}m^{(b)}$$

The general problem of computing the impedance matrix of this 2-inductor configuration is divided into two main steps:

1. Fill the partial impedance matrix $\mathbf{Z}$
2. Solve the $\mathbf{ZI} = \mathbf{V}$ system for two different vectors V

Step 1, consists in computing the partial self impedance of each filament in each inductor and the partial mutual impedance among all filaments in both inductors. We denote the cost for computing the resistance and partial self inductance of a filament as T_r and T_l, respectively. The cost for computing the mutual inductance between two filaments, we denote as T_m. Notice from tables (2.2) and (2.3) that both T_l and T_m are case dependent. Without loss of generality, for this analysis, we consider both figures as constants for any case.

The total cost for step 1 is then:

$$T_{\text{step 1}} = N(T_r + T_l) + \frac{N^2 - N}{2}T_m \tag{4.30}$$

Once the impedance matrix $\mathbf{Z}$ is filled, we proceed to step 2 where the linear system (4.20) is solved twice. This linear system can be rewritten as a block system of the form

$$\left(\begin{array}{cc|cc} \mathbf{Z_{a,a}} & \mathbf{Z_{a,b}} & \mathbf{A_a} & \mathbf{0} \\ \mathbf{Z_{b,a}} & \mathbf{Z_{b,b}} & \mathbf{0} & \mathbf{A_b} \\ \hline \mathbf{A_a}^T & \mathbf{0} & \multicolumn{2}{c}{\multirow{2}{*}{$\mathbf{0}$}} \\ \mathbf{0} & \mathbf{A_b}^T & & \end{array}\right)\left(\begin{array}{c} \mathbf{I_a} \\ \mathbf{I_b} \\ \hline \tilde{\mathbf{V}}_\mathbf{a} \\ \tilde{\mathbf{V}}_\mathbf{b} \end{array}\right) = \left(\begin{array}{c} \mathbf{V}_{\text{io}}^{(a)} \\ \mathbf{V}_{\text{io}}^{(b)} \\ \hline \mathbf{0} \end{array}\right) \tag{4.31}$$

where matrices $\mathbf{A_a}$ and $\mathbf{A_b}$ are the block matrices of size $m^{(a)} \times n^{(a)}$ and $m^{(b)} \times n^{(b)}$, as defined in (4.16). Vectors $\tilde{\mathbf{V}}_\mathbf{a}$ and $\tilde{\mathbf{V}}_\mathbf{b}$ are the unknown node voltages of inductor a and inductor b, respectively. Vectors $\mathbf{V}_{\text{io}}^{(a)}$ and $\mathbf{V}_{\text{io}}^{(b)}$ are the input/output vector of size $m^{(a)}n^{(a)}$ and $m^{(a)}n^{(a)}$, respectively, defined as in (4.17).

System (4.31) has rank $N + n^{(a)} + n^{(b)} - 2$. The cost of solving the linear system (4.31) twice, using a direct method (cubic complexity), would be:

$$T_{\text{step 2}} = 2(N + n^{(a)} + n^{(b)} - 2)^3 \tag{4.32}$$

The total complexity of this method is then given by

$$T_{coupled} = N(T_r + T_l) + \frac{N^2 - N}{2} T_m + 2(N + n^{(a)} + n^{(b)} - 2)^3 \tag{4.33}$$

4.5.2 Complexity of the decoupled method

The big advantage in our decoupled method is in the size of the linear systems to be solved, instead of solving systems of rank N we will be solving separate systems of size $n^{(a)}m^{(a)}$ and size $n^{(b)}m^{(b)}$. These systems correspond to finding the loop self impedance of each inductor as with the 1-inductor configuration case. The last step is that of computing the mutual loop impedance between the two inductors using (4.29).

The complexity of the decoupled method is:

Step 1: we compute the partial self inductance and resistance for all filaments. We compute the partial mutual inductance among all filaments in each of the inductors and then the partial mutual inductance between segments of one inductor and segments of the other. The cost is

$$T_{\text{step 1}} = N(T_r + T_l) + T_m \left(\frac{(n^{(a)}m^{(a)})^2 - (n^{(a)}m^{(a)})}{2} + \frac{(n^{(b)}m^{(b)})^2 - (n^{(b)}m^{(b)})}{2} \right) + T_m(n^{(a)}n^{(b)}) \tag{4.34}$$

Step 2: we compute the loop self impedance of each inductor. Using a direct method as with the method in 3.5.6. This means that the cost of step 2 is given by:

$$T_{\text{step 2}} = (n^{(a)}m^{(a)} + n^{(a)})^3 + (n^{(b)}m^{(b)} + n^{(b)})^3 \tag{4.35}$$

Step 3: we compute the mutual loop inductance between the two inductors using (4.29). The cost of this sum is

$$T_{\text{step 3}} = n^{(a)}n^{(b)} \tag{4.36}$$

The total complexity of our method is then given by

$$T_{ours} = N(T_r + T_l) + T_m \left(\frac{(N_a)^2 - N_a}{2} + \frac{(N_b)^2 - N_b}{2} + n^{(a)}n^{(b)} \right) + n^{(a)}n^{(b)} \tag{4.37}$$

with $N_a = n^{(a)}m^{(a)}$ and $N_b = n^{(b)}m^{(b)}$ the total number of filaments in a and b, respec-

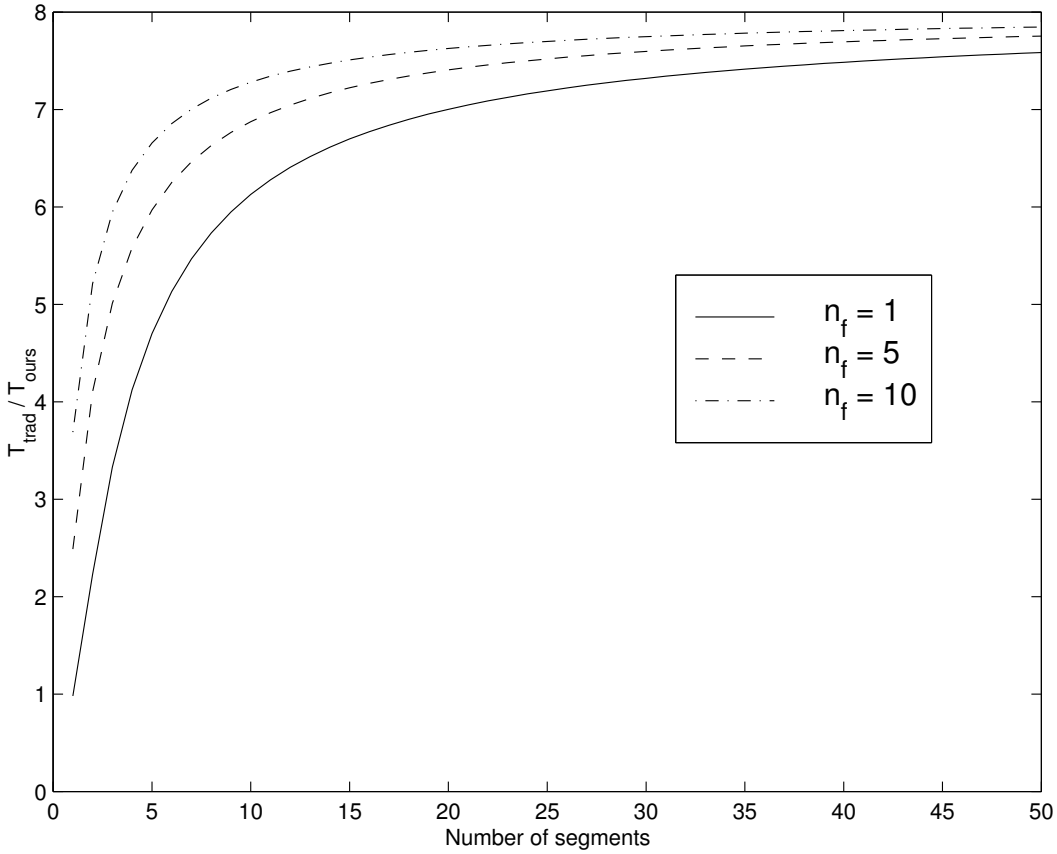


Figure 4.6: The performance ratio $T_{\text{coupled}}/T_{\text{ours}}$ for 2 inductors, as a function of n and for different values of m

tively.

Complexity ratio between the coupled and the decoupled approaches

We recall (4.33) and (4.37). In Fig. 4.6 values of the performance ratio $T_{\text{coupled}}/T_{\text{ours}}$ as a function of n and for different values of m are presented. We observe how the performance ratio rapidly attains its asymptotic value when both the number of filaments and the number of segments increased. For two inductors with 20 segments each and only one filament per segment the complexity of our decoupled methodology is already seven times smaller than that of the coupled case. Notice that the cubic term in T_{ours} grows linearly with the number of inductors, while the cubic term in $T_{coupled}$ grows cubicly with the number of inductors. Therefore, for a 4-inductor configuration, the performance ratio would be around 28. This generalizes to the following formula for

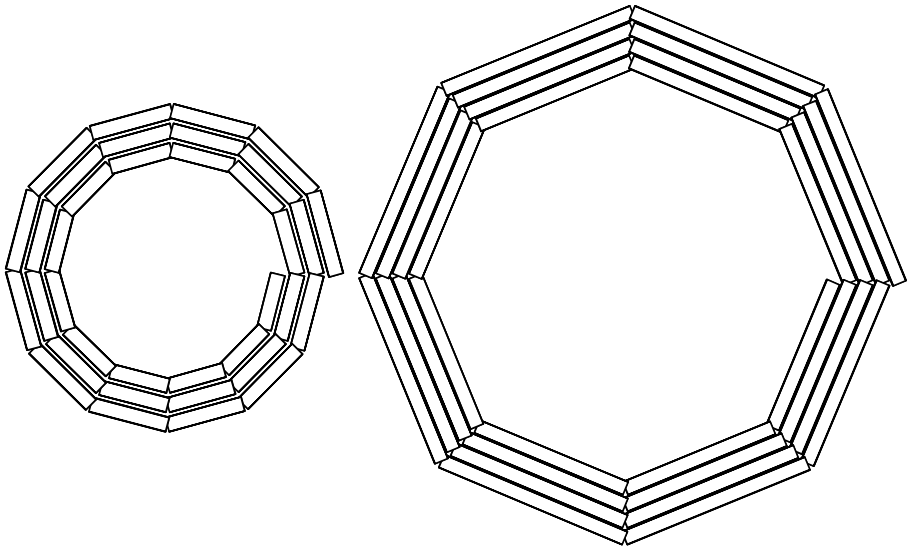


Figure 4.7: The 2-inductor configuration

the n-inductor case:

$$\frac{T_{\text{coupled}}}{T_{\text{ours}}}(n) = \frac{14}{8}n^2 \tag{4.38}$$

For inductors with a small number of segments, the term dependent of T_r, T_l and T_m dominates the computation easily hiding the performance gains of our method. Nonetheless, the process of computing the impedance matrix is easily parallelizable, therefore, given enough processors, the dominance of the impedance calculation can be overcame. Furthermore, our methodology is very useful in layout exploration. Designers face the problem of placing the inductors in a minimum space and in a way such as the noise among them is minimum. For this problem, our decoupled methodology shows its benefits: we compute once the self impedance of each inductor and then we only need to update the mutual impedance among inductors using expression (4.29) for each change in position.

4.5.3 Accuracy

We proceed to analyze the accuracy of our decoupled methodology vis-a-vis computing the entire N system. We have layout and simulated two polygonal inductors as shown in Fig. 4.7. Both metal width and separation were chosen such as skin and proximity

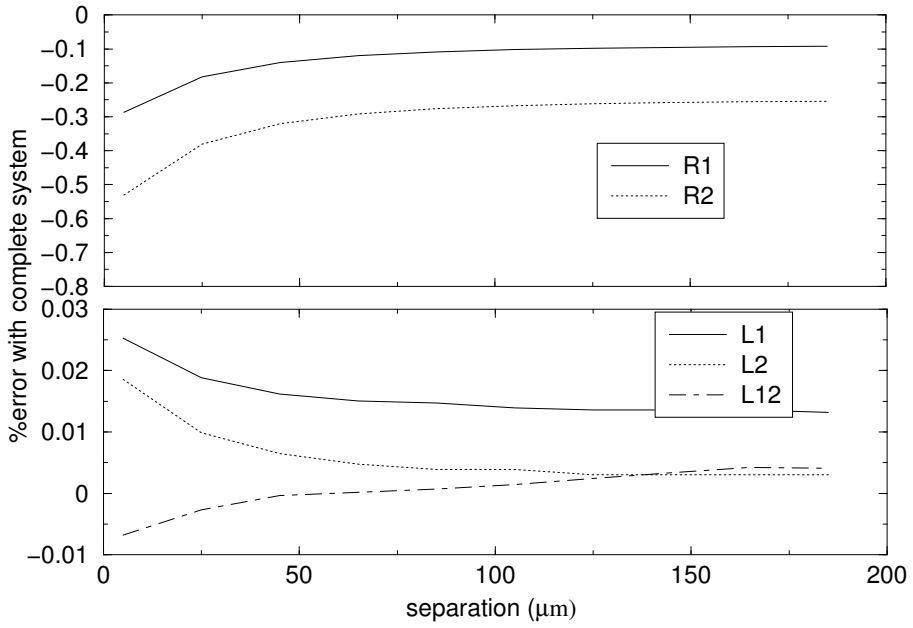


Figure 4.8: The relative error between the coupled approach and our decoupled methodology

effects be fully developed. We have selected as operating frequency $f = 20$ GHz to validate our approach into frequencies well beyond a regime where we have reasons to expect accurate results.

We break the inductors into filaments so as to capture the frequency effects (section 4.4.2). We solve the coupled linear system for the 2-inductor configuration for a given separation. We start with the two inductors as near as possible (without touching) and then increase their separation until 190 μm. With our method we compute only once the self impedance of each inductor, and for each separation we use the approximation given in (4.29) to compute the mutual impedance.

In Fig. 4.8 we present the relative errors in impedance between the coupled approach and ours. As expected, the errors in our approach are larger when the inductors are located very near one another, but are smaller than 0.5% which is an excellent agreement. Notice that errors tend to asymptotically converge to a value around 0.01% instead of 0%, i.e. a difference in the fifth significant digit, due to numerical rounding errors.

4.6 RLC representation

In the previous sections we have considered the magneto-quasistatic (MQS) description of the inductor, ignoring the capacitance in our treatment. The presence of capacitance needs to be considered for accuracy. Furthermore, the inclusion of capacitance in the model is compulsory if we want to compute the self resonance frequency of an inductor. In the MQS (RL-only) representation, the resonances cannot be captured. We proceed to include first the capacitance to ground and in a second improved approximation the capacitance among the segments of the inductor.

To compute the capacitance matrix **C** of the configuration we use the public domain electro-static solver FastCap, from MIT [22]. We provide as input the discretization into panels for each of the inductor's segments for accurate capacitance extraction. For an inductor with n segments, the capacitance matrix resulting from FastCap will be of rank n. The capacitance matrix is given in the standard Maxwell representation: the capacitance between segment i and segment j is equal to the negative of the offdiagonal element C_{ij}; to obtain the capacitance to ground of segment i, we subtract from the total capacitance C_{ii} the absolute values of the sum of entries in the i-th row of the capacitance matrix, i.e.

$$C_i = C_{ii} - |\sum_{j \neq i} C_{ij}| \tag{4.39}$$

4.6.1 First model: include only capacitance to ground

Consider a configuration consisting of one inductor with n segments and each segment broken into m filaments. Our first RLC model for this inductor consists on a concatenation of n T-elements as shown in Fig. 4.9. The KVL equations for this system are similar to the case were capacitances were not included. The impedance matrix **Z** is identical to that of the RL model, i.e, with elements being the partial impedance among the filaments inside all segments. As in the RL configuration, our linear system has $n * m$ current unknowns as well as $n - 1$ node voltage unknowns. The remaining $n - 1$ equations are those relating currents in one segment and the next. This equations are similar to those in (4.14). The only difference will be the capacitance to ground at each node. In Fig. 4.10 a node of the inductor is presented in detail. Kirchoff's law in this node states that the current exiting segment i, must be the equal to the current entering

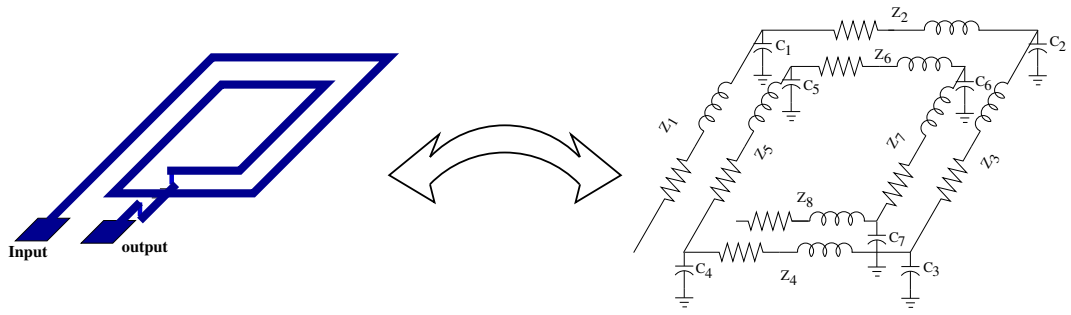


Figure 4.9: Representation of an inductor as a cascade of T-elements. For simplicity reasons, only the total impedance of each segment is presented. The impedance of each filament are indeed considered independently in the calculation. Also for simplicity, mutual couplings among segments are not displayed but are included in the calculation

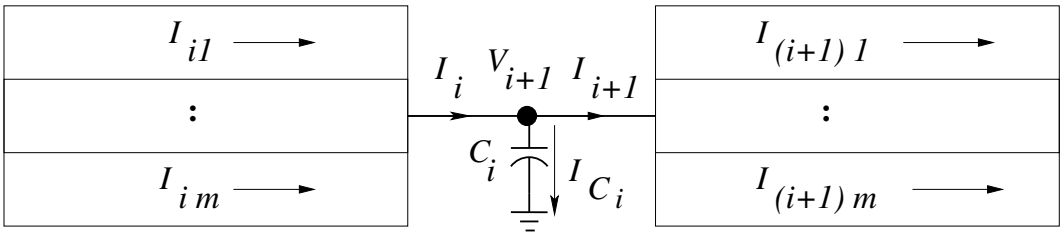


Figure 4.10: The inter-segment node where capacitance to ground are included

into segment $i+1$, plus the current going to ground due to the capacitance C_i. This is to say

$$I_i = I_{i+1} + I_{C_i} \tag{4.40}$$

where I_{C_i} is the current going to the ground through C_i, i.e.

$$I_{C_i} = j\omega V_{i+1} C_i \tag{4.41}$$

Expression (4.40) together with (4.41) results in the new current redistribution equations, when each of the segments are broken into m filaments:

$$\sum_{k=1}^{m} I_{ik} = \sum_{k=1}^{m} I_{(i+1)k} + j\omega V_{i+1} C_i, \quad \text{for} \quad i = 1, \ldots, n-1 \tag{4.42}$$

As with the RL case, the linear system $\mathbf{ZI} = \mathbf{V}$ and equations (4.42) can be joined

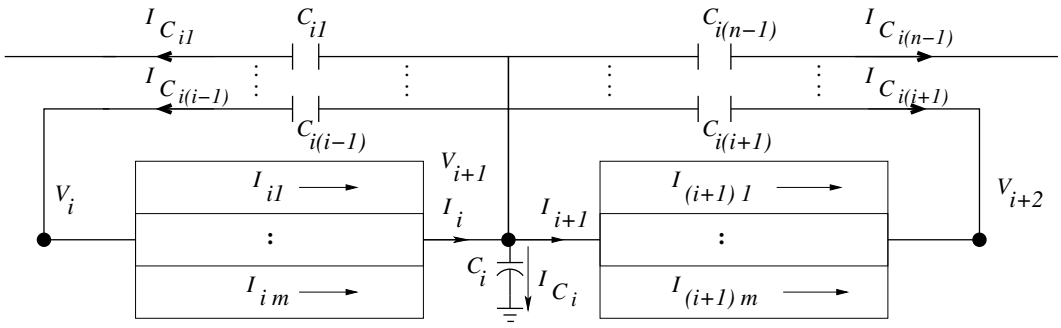


Figure 4.11: The inter-segment node where capacitance to ground and coupling capacitance are included. Arrows represent the direction of currents relative to the reference node

into a single linear system where the unknowns are to be found. The resulting system has the same shape as the one in (4.15) with block N replaced by a diagonal matrix with nonzero elements equal to $-j\omega C_i$, for $i = 1, \ldots, n$.

The input impedance of the inductor is given by the inverse of the current going through the first segment, i.e.

$$Z_{in} = \left(\sum_{k=1}^{m} I_{1k} \right)^{-1} \tag{4.43}$$

4.6.2 Second, enhanced model: adding coupling capacitance among segments

We enhance our capacitance model with the inclusion of coupling capacitance among the segments. The nodal equations include the presence of the capacitive coupling among the segments as well as the capacitance to ground. In Fig. 4.11 we observe one node of the configuration. Kirchoff's law in this node result in the equation:

$$I_i = I_j + I_{C_i} + \sum_{j \neq i} I_{C_{ij}} \tag{4.44}$$

where I_{C_i} is the current going to the ground through C_i and $I_{C_{ij}}$ is the current going through the coupling capacitance between segment i and segment j. This coupling current is related to C_{ij} and the node voltages V_{i+1} and V_{j+1} via KVL as

$$I_{C_{ij}} = j\omega(V_{i+1} - V_{j+1})C_{ij} \tag{4.45}$$

Expression (4.44) together with (4.41) and (4.45) results in the new current redistribution equations, when each of the segments are broken into m filaments:

$$\sum_{k=1}^{m} I_{ik} = \sum_{k=1}^{m} I_{(i+1)k} + j\omega \left(V_{i+1} C_i + \sum_{j \neq i} (V_{i+1} - V_{j+1}) C_{ij} \right) \tag{4.46}$$

which can be rewritten into

$$\sum_{k=1}^{m} I_{ik} = \sum_{k=1}^{m} I_{(i+1)k} + j\omega \left[V_{i+1} \left(C_i + \sum_{j} C_{ij} \right) - \sum_{j \neq i} V_{j+1} C_{ij} \right] \tag{4.47}$$

The linear system $\mathbf{ZI} = \mathbf{V}$ together with (4.47) can be rewritten in block form as in

$$\left(\begin{array}{c|c} \mathbf{Z} & \mathbf{A} \\ \hline \mathbf{A}^T & -\mathbf{j}\omega\mathbf{C} \end{array} \right) \left(\frac{\mathbf{I}}{\tilde{\mathbf{V}}} \right) = \left(\frac{\mathbf{V}_{\text{io}}}{\mathbf{0}} \right) \tag{4.48}$$

with C the capacitance matrix.

4.7 Implementation

We implemented an impedance simulator for intentional inductors. For this purpose, our methodology, presented in this chapter, has been implemented in a stand alone program. The program has four parts:

1. Input: the parameters for the n-inductor configuration are read
2. Layout: the n-inductor configuration is generated from the input parameters
3. Calculation engine: the impedance matrix of the n-inductor configuration is computed
4. Output: graphical and written information is output

We proceed to explain in detail each of the previous steps including the data structures.

4.7.1 Data structure

We created a structure called `inductor`. This structure contains all the properties necessary to represent an inductor. The properties of this structure are:

- `type`: the type of inductor. See: Layout section.
- `w`: the metal width
- `s`: the metal separation
- `t`: the metal thickness
- `R`: the inductor's radius. This is the distance from the geometric center to the outer edge
- `ns`: number of sides
- `nt`: number of turns
- `dx`, `dy`, `dz`: the coordinates of the inductor's geometric center
- `nboffil`: the number of filaments into which each segment of the inductor is partitioned.
- `rot`: rotation clockwise in number of segments
- For non planar inductor we include `R_via`, the resistance per via and `N_via`, the number of vias to place when changing metal layers
- `wires`: this is a list with the geometrical representation of all filaments inside the inductor

A exemplary inductor explaining each of the properties is shown in Fig. 4.12.

4.7.2 Input

The input consists on the physical and geometrical parameters for the n-inductor configuration. An example of an input file defining a 4-inductor system would be:

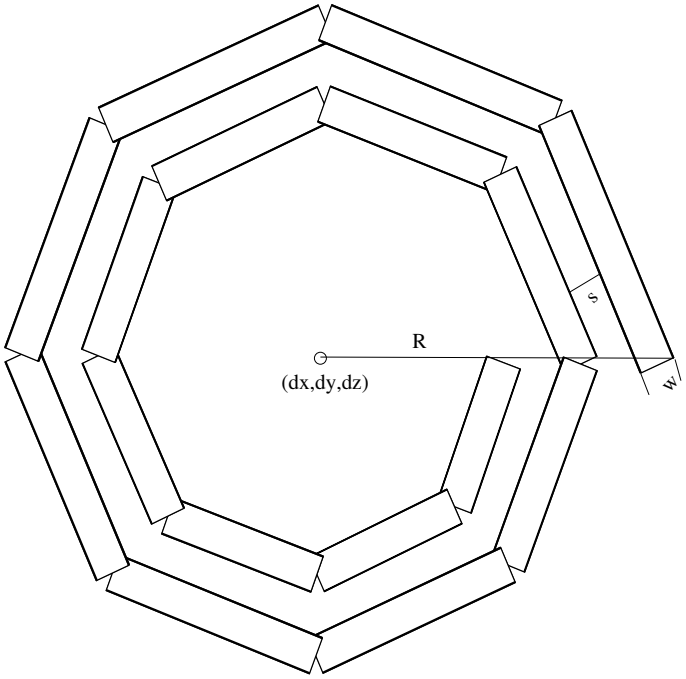


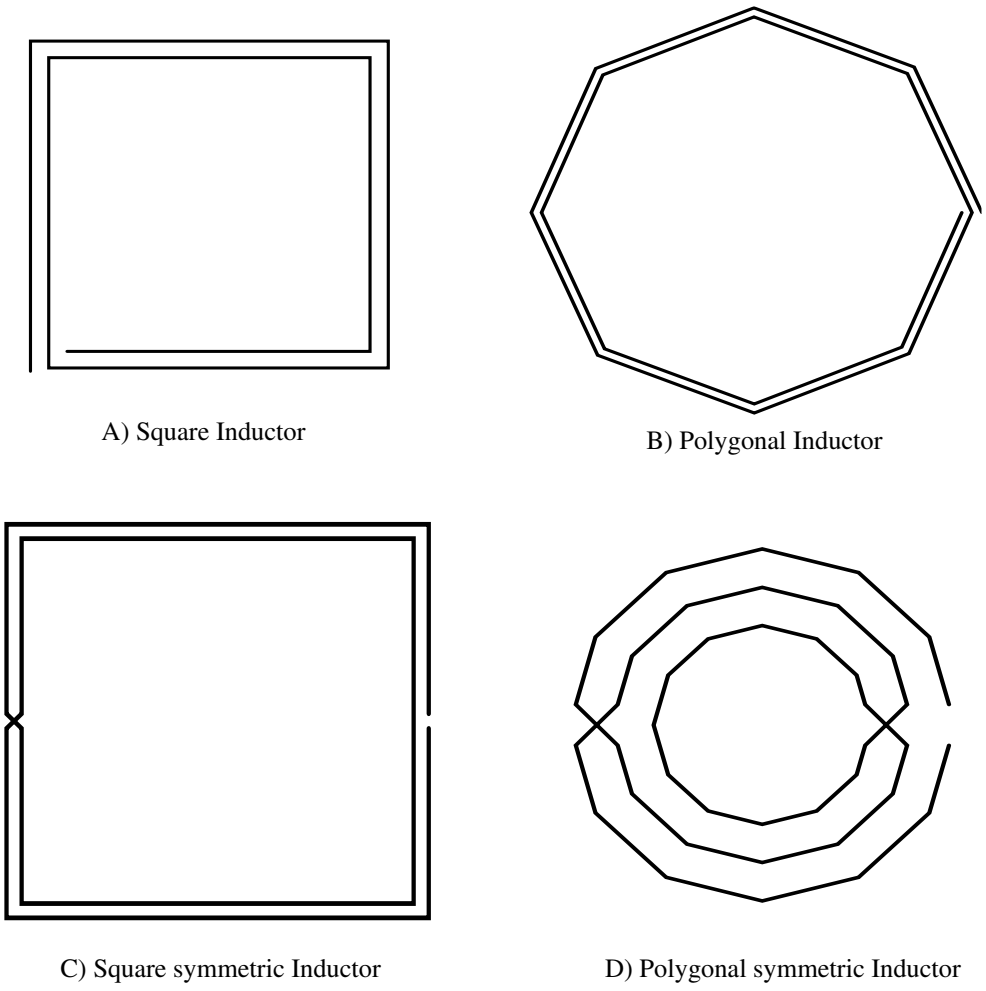
Figure 4.12: A polygonal inductor with nt=2, ns=8 and rot=0.

```
n=4
units=1e-6
type=1 w=2 s=3 t=1.96 R=50 ns=4 nt=2 dx=0 dy=0 dz=0 rot=0
type=2 w=3 s=1 t=0.65 R=100 ns=8 nt=2 dx=0 dy=200 dz=3 rot=0
type=3 w=6 s=1 t=0.65 R=100 ns=4 nt=2 dx=200 dy=0 dz=3 rot=0
       + R_via=50 N_via=25
type=4 w=5 s=5 t=1.96 R=50 ns=12 nt=3 dx=100 dy=0 dz=0 rot=0
       + R_via=50 N_via=25
```

The first line indicates the number of inductors in the configuration. The second line indicates the length units. In this case `units=1e-6` represents microns. The remaining lines contain the geometrical information for each inductor. For instance, the line

```
type=2 w=3 s=1 t=0.65 R=100 ns=8 nt=2 dx=0 dy=200 dz=3 rot=0
```

corresponds to an inductor of type 2 (see next section) with metal width equal to 3 length units, microns in this case; the edge-edge metal spacing is 1μm; the metal thickness is 0.65μm; the radius of the inductor is 100μm; the number of sides and turns is 8 and 2, respectively; and the coordinates of the inductor's geometrical center are $(0, 200, 3)\mu$m.



A) Square Inductor

B) Polygonal Inductor

C) Square symmetric Inductor

D) Polygonal symmetric Inductor

Figure 4.13: The four common types of implemented inductors

4.7.3 Layout

After reading the input file, we layout the inductors according to their `type` parameter. We have implemented the layout of 4 different types of inductor:

- Type 1: square inductor (Fig. 4.13.A)
- Type 2: polygonal inductor (Fig. 4.13.B)
- Type 3: symmetric square inductor (Fig. 4.13.C)
- Type 4: symmetric polygonal inductor (Fig. 4.13.D)

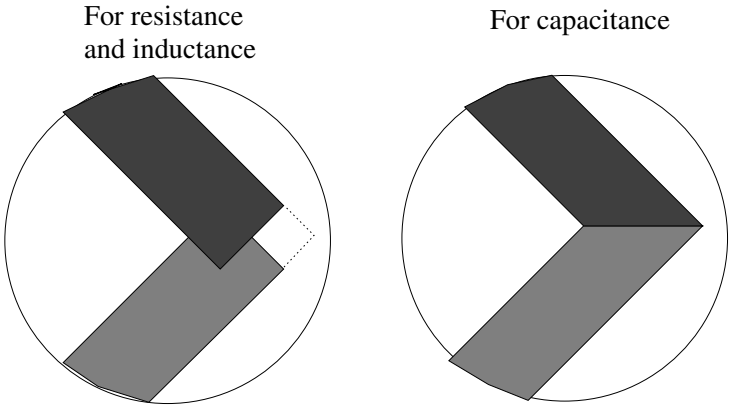


Figure 4.14: Partition of the inductor at the corners

Type 1 and Type 2 are coplanar inductors, this means that all the wires in the inductor are located at the same layer. Symmetric inductors, on the other hand, have segments that cross. This is done by putting one of the segments in a different layer. The connections between the rest of the inductor and this segment are done through vias*.

Since our 2D expressions for resistance and inductance work only for wires with parallelepiped shape, we partition the inductors at each corner into segments with rectangular shape. As can be seen in Fig. 4.14 this partitioning creates an unphysical overlap region. We break the inductor into disjoint polygons in order to avoid the unphysical overlap, as shown in figure 4.14.

We briefly describe how we construct each type of inductor:

Square inductor

The length of the first 3 segments in the square inductor at the i-th turn follows the sequence:

$$L^i_{1,2,3} = 2 * r - (i-1)2(w+s) \tag{4.49}$$

The fourth segment at each turn follows this sequence:

*For wires that change planes, we will conserve the resistance of the vertical segment (vias). Given that the interlayer space in a typical IC is many orders of magnitude smaller than the length of the wires, we can ignore the reactance of the via, which is proportional to its length, for all frequencies of interest.

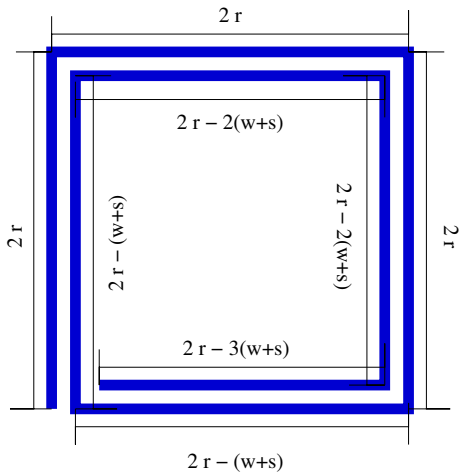


Figure 4.15: Construction of a square inductor of outer length $2r$

$$L_4^i = 2 * r - (2i - 1)(w + s) \tag{4.50}$$

In Fig. 4.15 we show an example of a square inductor.

Polygonal inductor

For this particular case we use the parametrization of a circular spiral and find the intersection points according to the number of sides of the inductor. The inner distance d of the circular spiral is related to the metal spacing s as shown in Fig. 4.16, where we display the intersection of a 8-side polygonal inductor with 2 turns with the corresponding circular spiral.

Symmetric square inductor

We generate this inductor in three sweeps: first, we generate the segments in the upper half; next, those in the lower half. As a last sweep we join the two halves with diagonal segments belonging to different layers. We show the construction of one 2-turns symmetric square inductor in Fig. 4.17.

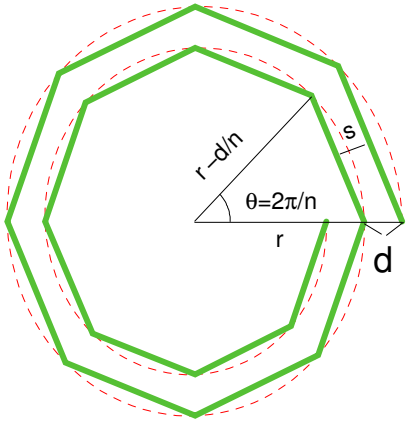


Figure 4.16: Construction of a 8-side polygonal inductor by intersection with a circular spiral

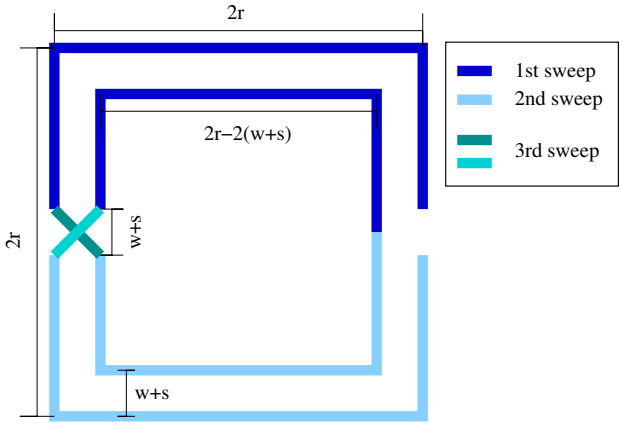


Figure 4.17: Construction of a 2-turn symmetric square inductor

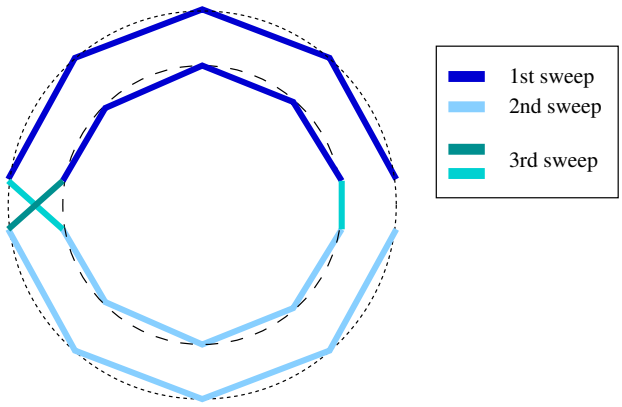


Figure 4.18: Construction of a 8-side 2-turn symmetric polygonal inductor by intersection with concentric circles

Symmetric polygonal inductor

As for the symmetric square inductor we generate this inductor in three sweeps. Each half of the inductor will be intersected to the N_t concentric circles with decreasing radius so as to ensure that the segments in the inductor have the required separation s. We show an exemplary 8-side 2-turn symmetric polygonal inductor in Fig. 4.18.

The wires in structure `inductor` are constructed using the layout methodology for the particular type of inductor. If the property `nboffil` is different to 1, each of the inductor's segment will be partitioned into that many filaments. The filaments with different cross-section area as shown in Fig. 4.5. The filaments will be stored in the `wire` structure ordered according to the segment they belong. For instance, the first `nboffil` elements of `inductor->wire` correspond to the filaments in which the first segment of the inductor is partitioned.

4.7.4 The engine

Following the method presented in section 4.5, we consider each inductor separately. With the geometrical information about the filaments in the property `wire` of the structure `inductor`, we compute the resistance and partial self inductance of each filament and the partial mutual inductance among them. The resistance of the filaments is stored in a vector **R** and the inductance matrix is stored in a symmetric matrix **L**. If a capacitance model is desired, a FastCap input file representing the inductor is built. We

compute the capacitance matrix for each of the segments in the inductor without breaking it into filaments[†]. An external system call to FastCap is performed using the FastCap input file. The capacitance matrix is stored in a matrix **C**.

With **R**, **L** and the optional **C** we implicitly build the extended impedance matrix **Z** as in (4.48). This matrix is decomposed using a modified version of the LDL^T factorization for complex and symmetric matrices (see section 3.5.6). With this decomposition we proceed to solve the extended system for currents in each filament. We sum the currents in the filaments in the first segment and the inverse of this sum is what we consider the input impedance of the inductor.

If the configuration consists of more than one inductor we proceed to compute the mutual impedance among inductors. We do this iteratively taking two inductors in the configuration at a time, computing the mutual inductance between segments in one inductor and segments in the other. Using (4.29) we compute the mutual impedance between these two inductors.

4.7.5 Output

We output the impedance matrix of the system for the frequency f. This matrix correspond to the $n \times n$ complex matrix with elements in the diagonal equal to the self impedance of the n inductors and elements in the off-diagonal equal to the mutual impedance among the n inductors.

4.8 Validation testcase

We proceed to compare results from our implementation against the tool for intentional inductors simulation ASITIC, from UC Berkeley [53]. We consider a square inductor (Fig. 4.19) with following characteristics:

- Inner radius: $R = 125\ \mu$m
- Metal thickness: $t = 1\ \mu$m
- Metal width: $w = 10\ \mu$m
- Metal spacing: $s = 5\ \mu$m

[†]We neglect displacement currents inside the conductors

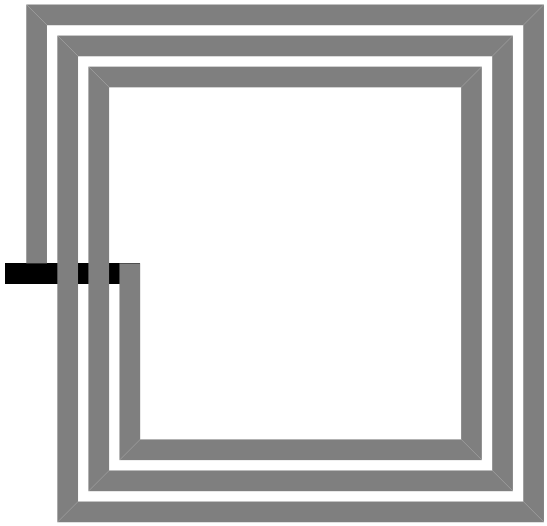


Figure 4.19: A square inductor with an exit segment in lower metal layer

- Number of turns: $nt = 3.25$
- Resistivity: $\rho = 0.017\ \Omega.\mu\text{m}$ (Cu)
- We assume null resistance for vias
- The inductor is placed at $z = 3\ \mu\text{m}$ over a high resistivity substrate and surrounded by a dielectric layer of thickness $t = 20\ \mu\text{m}$ with relative permittivity $\varepsilon_r = 3.9$ (SiO)
- The exit bridge is located 1 μm below the inductor's metal layer

Using the `2port` command in ASITIC we obtain the Z-parameters for the inductor when considered as a two-port. This is a 2x2 matrix of the form:

$$\mathbf{Z_{2port}} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \tag{4.51}$$

The relationship between currents and voltage drops in the two-port structure (Fig. 4.20) are related by the Z-parameters in the following way:

$$\begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{4.52}$$

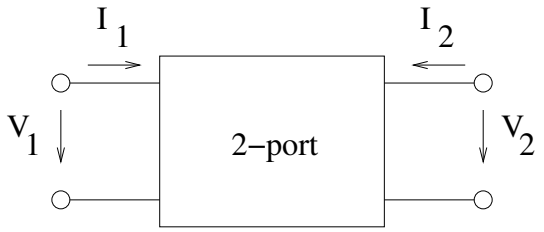


Figure 4.20: A two-port structure

Short circuiting the end ports, i.e., setting $V_2 = 0$ and forcing an input potential of $V_1 = 1$ v, results in the following expression for the inductor's input impedance Z_{in}:

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}} \tag{4.53}$$

We layout the inductor with the given parameters. We create an input file for the capacitance simulator. Using the capacitance matrix and the impedance matrix we compute the input impedance of the inductor as explained in section 4.6.2.

In Fig. 4.21 we show the values of the real and imaginary parts of the input impedance coming from ASITIC (using (4.53)) and our model, both as a function of frequency. Both models agree very well. The most noticeable difference is in the self-resonance frequency: for our model is $f = 6.8$ GHz and for ASITIC is $f = 6.4$ GHz. This difference is due to the over simplified parallel plate approximation used for capacitance simulation in ASITIC. We use instead an accurate capacitance simulator. We verify this by including results from FastHenryand FastCap in Fig. 4.21. This later results agree with the self-resonance frequency predicted by our method.

In Fig. 4.22 we show the quality factor $Q_{ind} = \mathrm{Im}(Z_{in})/\mathrm{Re}(Z_{in})$ for the inductor, for both models, as a function of frequency. We consider only a small window around the maximum quality factor, which is usually the frequency at which the inductor will operate in an RF design.

4.9 A DRC implementation

A Design Rule Checking (DRC) has been implemented using our intentional inductor methodology. Designers using more than one intentional inductor in their designs can easily verify if the inductive coupling between any two inductors is more than an

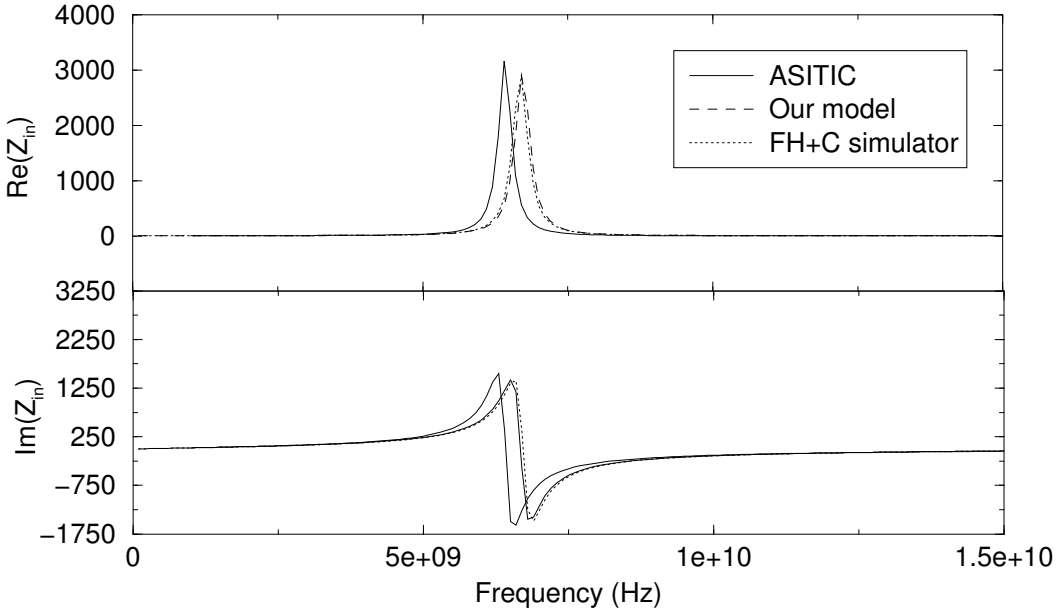


Figure 4.21: Real and imaginary parts of Z as a function of frequency

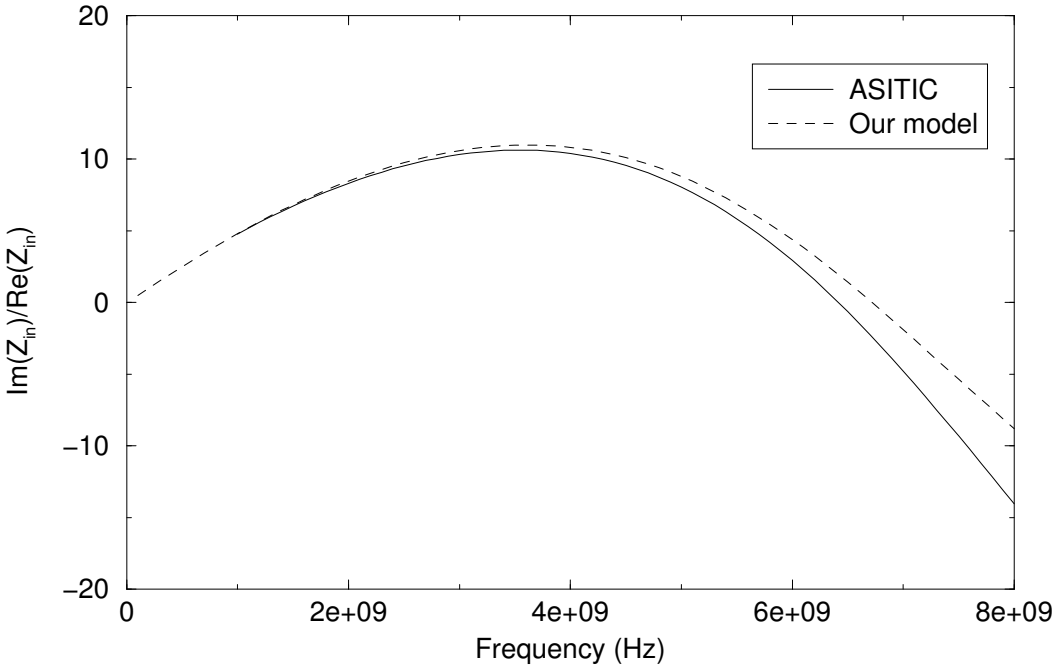


Figure 4.22: Quality factor as a function of frequency

accepted value.

To use this tool, the designer feeds it with a layout file (GDSII, Oasis, etc) where the inductors are located. In a separated file the electric rules are included.

The tool recognizes the inductors and proceed to compute the input impedance of each one as presented in previous sections. In a second step, the mutual impedance between any pair of inductors is computed. The inductance coupling coefficient

$$K = \frac{\mathrm{Im}(Z_{a,b})}{\sqrt{\mathrm{Im}(Z_a)\mathrm{Im}(Z_b)}}$$

is computed for any two pair of inductors and compared with the rules given by the user. If any of the rules is violated, the user gets a warning.

Chapter 5

Time delay in the RLC domain

Temps de réponse dans le domaine RLC

Résumé

Des expressions pour le temps de réponse d'une signal dans le domaine RC sont bien connues. En 2000 Davis et Meindl (DM) donnent des solutions exactes à l'équation du Télégraphiste dans le domaine temporel, pour une ligne de transmission ouverte, stimulée par un signal d'entrée avec un temps de montée nul. Ils proposent aussi des expressions pour le temps de réponse de la dite ligne. Dans ce chapitre j'introduis une correction à l'expression de DM pour le temps de réponse d'une ligne de transmission ouverte quand le signal d'entrée présente un temps de montée diffèrent de zéro. Une fois cette expression dérivée, nous la complétons avec la correction nécessaire quand on ajoute au bout de la ligne, un dispositif avec une capacité finie.

Ce chapitre est une extension d'un des résultats présentés dans l'article [11].

5.1 Introduction

With clock frequencies rising, inductance effects become noticeable and start playing an important role in time delay. Delay expressions for RC interconnects are well known. Those expressions are accurate when inductance is negligible but become unphysical otherwise. For this reason new time expressions with inductance taken into account are needed in order to get an accurate description of the waveforms and hence the time

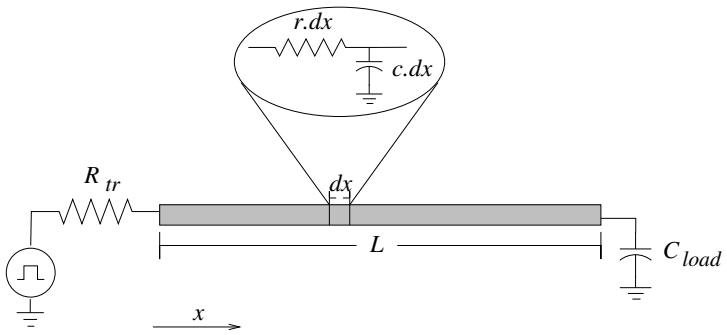


Figure 5.1: The RC representation of a wire.

delay in signal lines. In [54] exact solutions for the telegraphist equation in the time domain are presented. These expressions, although very useful are restrained to the case in which an open ended interconnect is fed by a Heaviside step pulse. What we propose in this work are corrections to these RLC expressions due to non-zero rise time of the input signal and the presence of a load capacitance at the end of the line.

This chapter is divided as follows: In section 5.2 a brief description of general RC expressions are presented. In section 5.3 we present a summary of the exact solutions to the telegraphist equations in the time domain as presented in [54]. In section 5.4, time delay expressions for an open-ended line with a Heaviside step pulse are presented. This expression being the direct consequence of the solutions presented in section 5.3. In section 5.5, we present our corrections to the time delay expressions in the presence of finite rise-time and load capacitance at the end of the line. In the last section our concluding remarks are presented.

5.2 Previous work - RC domain

At low frequencies, the real part of the impedance dominates its imaginary part, i.e. $r >> \omega l$. The inductance can be discarded. This is referred to as the RC domain. Wires in this domain are well represented by RC networks (Fig. 5.1), satisfying the diffusion equation:

$$\frac{\partial^2 V(x,t)}{\partial x^2} = rc\frac{\partial V(x,t)}{\partial t} \tag{5.1}$$

with r and c representing the capacitance and resistance per unit length of the wire. The function $V(x,t)$ is the potential at a position x of the wire and at a time t. We consider wires with transversal dimensions much smaller than longitudinal dimensions. Therefore, a one dimensional model for the potential suffices, with the spatial variable in the longitudinal direction of the line. Transversal dimensions are averaged over. This equation can be derived from (2.8) by standard methods [55].

Solutions to this equation are useful to derive expressions for the time delay. For instance, an important value to know is the time it takes for the output voltage to reach one half the amplitude of the input signal V_{dd}, i.e. $V(L, t_{50\%}) = 1/2V_{dd}$. This figure is known as the 50% time delay. Notice that 50% of the input voltage is above the threshold in which transition at a transistor attached to the output of the line occurs.

Taking the leading term of a series expansion for the solution of (5.1) at the far end of the line, Sakurai [5] derives a well known approximation to the 50% delay of an RC line feed by a Heaviside step pulse of arbitrary amplitude. The expression is given by

$$t_{50\%} = 0.377rcL^2 + 0.693\left(R_{tr}cL + C_{load}rL + R_{tr}C_{load}\right), \tag{5.2}$$

where L is the length of the line, R_{tr} is the load resistance at the beginning of the line and C_{load} is the total load capacitance at the end of the line (see Fig. 5.1). Values R_{tr} and C_{load} are used to represent respectively the resistance of the driver and the capacitance of the receiver attached to the line. It is the interest of the designer to minimize this delay.

This approximate expression, turns out to be a lower bound on the delay of an RC line. This is due to the fact that the distributed RC representation of the wire is approximated as a single RC lumped element with resistance equal to $r.L$ and capacitance equal to $c.L$. In Fig. 5.2 we show the comparison between the distributed model and the single lumped element for typical values of the parameters. In this figure we observe how the $t_{50\%}$ is underestimated when taking a single lumped element.

For illustration purposes, we display in Fig. 5.3 the devices' contribution to the delay (second term of (5.2)) against the total delay including the quadratic term. From the graph we can observe how the quadratic term starts to dominate the delay for wires in the centimeter range. The engineering answer is to put repeaters in this position in order to maintain the linear term dominating the delay [56]. The function of a repeater is to restore the signal voltage value $V(L,t)$ to V_{dd}.

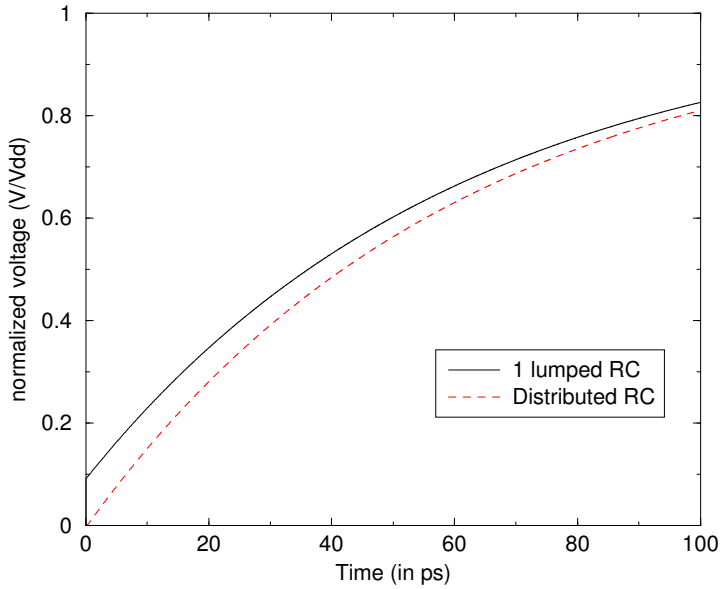


Figure 5.2: Normalized voltage in function of time for a RC line. Both the distributed and the single lumped element representations are displayed. For a wire of rectangular cross-section with width 5μm and thickness of 0.65μm. Load values: $R_{tr} = 50\Omega$ and $C_{load} = 1$pF.

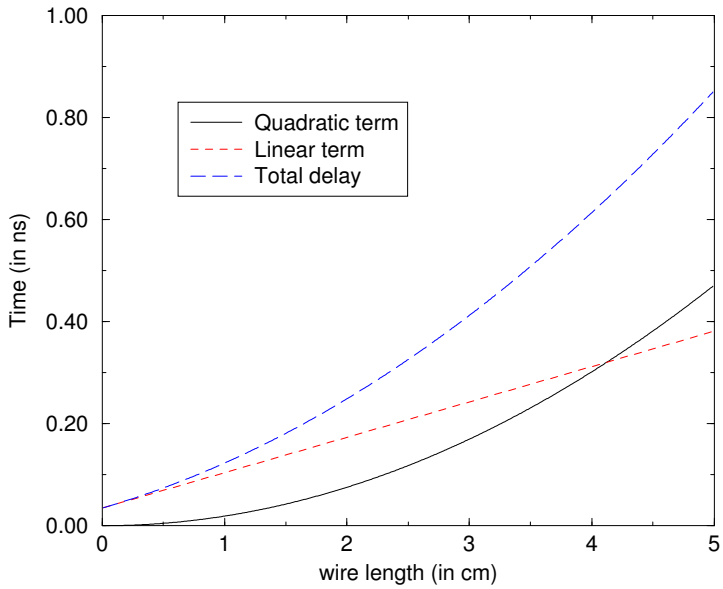


Figure 5.3: The linear and quadratic terms of Sakurai expression. Using same parameters as for Fig. 5.2

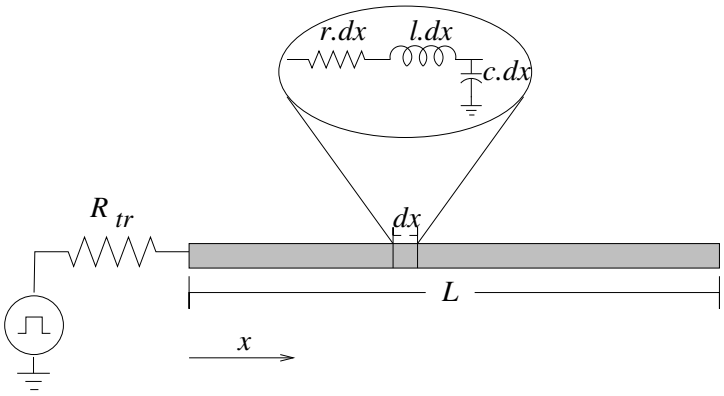


Figure 5.4: The RLC representation of a wire.

5.3 Distributed RLC lines

For a single line represented by RLC networks, as in Fig. 5.4, the PDE that generalizes (5.1) is the telegraphist equation:

$$\frac{\partial^2 V(x,t)}{\partial x^2} = lc\frac{\partial^2 V(x,t)}{\partial t^2} + rc\frac{\partial V(x,t)}{\partial t} \tag{5.3}$$

Equation (5.3) replaces (5.1), and the additional parameter l is the inductance per unit length of the line. It can be derived from the Maxwell's equations [55].

Solutions to (5.3) in the frequency domain have been studied in detail in the literature [29]. Applying inverse Laplace transform to these solutions in order to obtain solutions in the time domain is not possible for the general case. In most of the works approximations to the solutions in the Laplace space are used. For these simpler expressions it is possible to apply the inverse Laplace transform and thereby obtain expressions in the time domain. For special boundary conditions these time domain approximations are accurate.

In [54] an exact solution in the time domain for an open ended line fed by a Heaviside step pulse is given. This approximation is valid when the parameters r and c are constant for the domain of interest. This is the case in our application. The representation, while exact, is an infinite series involving modified Bessel functions.

We make extensive use of results presented in [54], and refer the reader to the original article for details. Note is given to the corresponding equations in the original paper.

5.3.1 Time domain solutions

Following [54], the solution for a semi-infinite line fed by a Heaviside step pulse V_{in}, at $x = 0$, in the transformed Laplace coordinates s, x is

$$V_{inf}(x, s) = V_{in}(s)\frac{Z(s)}{Z(s) + R_{tr}}e^{-\Phi(x,s)} \tag{5.4}$$

where

$$\Phi(x, s) = x\sqrt{lcs(s + \tfrac{r}{l})} \tag{5.5}$$

$$Z(s) = Z_0\sqrt{\tfrac{s+\frac{r}{l}}{s}} \tag{5.6}$$

$$Z_0 = \sqrt{\tfrac{l}{c}} \tag{5.7}$$

An interesting limit is r going to zero. In this limit one can calculate exactly the inverse Laplace transform given in the time domain. This gives rise to a close form expression:

$$V_{inf}(x, t) = V_{dd}\frac{Z_0}{Z_0 + R_{tr}}u_0(t - x\sqrt{lc}) \tag{5.8}$$

where V_{dd}, the power supply voltage, is the amplitude of the pulse and u_0 is a Heaviside unit step function. This is the solution for a traveling wave in a lossless line, i.e. the wave travels without attenuation.

For finite r, the front end voltage wave form can be expressed as

$$V_{inf}(x, t = x\sqrt{lc}) = V_{dd}\frac{Z_0}{Z_0 + R_{tr}}e^{-(rx/2Z_0)} \tag{5.9}$$

Equation (5.9) (equation (25) in [54]) is a known expression in the transmission line literature. It does not reflect important parts of the behavior we are interested in.

A better representation to describe the transient voltage near the wave front is given by (equation (32) in [54]):

$$\begin{aligned}\frac{V_{inf}(x, t')}{V_{dd}} =& \Big[\frac{Z_0}{R_{tr} + Z_0}e^{-(rx/2Z_0)t'}I_0\left(\frac{rx}{2Z_0}\sqrt{t'^2 - 1}\right) \\ &+ \frac{1}{2}e^{-(rx/2Z_0)t'}(f(t') - f(1))\Big]u_0(t' - 1)\end{aligned} \tag{5.10}$$

where (equation (27) in [54])

$$
\begin{aligned}
f(t') &= \sum_{k=0}^{\infty} \frac{1}{k!} \left(\frac{rx}{2Z_0} \right)^k (t'-1)^k (4 - (1+\Gamma)^2 \Gamma^{k-1}) \\
&= 4e^{(rx/4Z_0)(t'-1)} - \frac{(1+\Gamma)^2}{\Gamma} e^{(rx/4Z_0)\Gamma(t'-1)}
\end{aligned}
\tag{5.11}
$$

with the normalized time t' given by

$$
t' = \frac{t}{x\sqrt{lc}} \tag{5.12}
$$

and with Γ the reflection coefficient:

$$
\Gamma = \frac{\frac{R_{tr}}{Z_0} - 1}{\frac{R_{tr}}{Z_0} + 1}. \tag{5.13}
$$

The function $I_0(x)$ being the modified Bessel function I of zero-th order.

5.3.2 Finite lines

In [54] a more appropriate boundary condition is given by a finite line with an arbitrary source impedance and open circuit termination, as seen in Fig. 5.4.

The complete expression in the time domain is given by (equation 42 in [54])

$$
\begin{aligned}
V_{fin}(x,t) &= 2V_{inf}(x,t) + 2V_{dd} \frac{Z_0}{Z_0 + R_{tr}} e^{-\sigma t} \\
&\times \sum_{n=1}^{q} \sum_{i=0}^{n} \sum_{j=0}^{\infty} \Bigg\{ \frac{n(n-1+j)!}{i!\,j!\,(n-i)!} (-1)^i \Gamma^{n-i+j} \\
&\times \Bigg[\left(\frac{t-t_n}{t+t_n} \right)^{(i+j)/2} I_{i+j} \left(\sigma \sqrt{t^2 - (t_n)^2} \right) \\
&+ \frac{1}{1-\Gamma} \sum_{k=1}^{\infty} \left(\frac{t-t_n}{t+t_n} \right)^{(i+j+k)/2} \\
&\times I_{i+j+k} \left(\sigma \sqrt{t^2 - (t_n)^2} \right) (4 - (1+\Gamma)^2 \Gamma^{k-1}) \Bigg] \\
&\times u_0(t-t_n) \Bigg\},
\end{aligned}
\tag{5.14}
$$

with $q = \left\lfloor 0.5 \left(\frac{t}{x\sqrt{lc}} + 1.0 \right) \right\rfloor$, $t_n = (2n+1)x\sqrt{lc}$, $\sigma = r/(2l)$ and $I_k(-)$ the modified Bessel

function I of order k-th.

The first term before the first reflection gives $2V_{inf}(L,t)$, the other terms give the later reflections that occur at odd multiples of $t_f = L\sqrt{lc}$ each one attenuated by exponential decay.

Expression (5.14) differs from traditional lossless transmission line theory, in which a matched source of impedance $R_{tr} = Z_0$, i.e. $\Gamma = 0$, absorbs all power from the transmission line leaving only the first reflection. In interconnects, the impedance varies with the frequency and moreover is a complex number since the voltage and current ratio are out of phase. This makes the match of impedance unrealistic. Only in the lossless case, is the impedance at any point of the line constant and real.

There are two useful expressions in the first reflection approximation (good for $rx/2Z_0 < 1$ and arbitrary source impedance)

$$\begin{aligned}\frac{V_{fin}(x,t')}{V_{dd}} =& \frac{2Z_0}{R_{tr}+Z_0} e^{-(rx/2Z_0)t'} u_0(t'-1) \\ &+ e^{-(rx/2Z_0)t'}(f(t') - f(1))u_0(t'-1)\end{aligned} \tag{5.15}$$

The first term in this expression is the fast rising "LC" portion and the second term is the slow rising "RC" portion. Accounting for the next reflection leads to equation

$$\begin{aligned}&V_{fin}(x=L,t) \\ &=2V_{dd}\left\{\begin{array}{l}\dfrac{Z_0}{R_{tr}+Z_0} e^{-(rx/2Z_0)t'} I_0\left(\dfrac{rx}{2Z_0}\sqrt{t'^2-1}\right) \\ +\dfrac{1}{2} e^{-(rx/2Z_0)t'}\left(\dfrac{t'-1}{t'+1}\right)^{0.5}(4-(1+\Gamma^2))I_1\left(\dfrac{rx}{2Z_0}\sqrt{t'^2-1}\right) \\ +\dfrac{1}{2} e^{-(rx/2Z_0)t'}(-(t-1)f'(1)+f(t')-f(1))\end{array}\right\} \\ &\times(u_0(t'-1)-u_0(t'-3)) + V_{dd}u_0(t'-3)\end{aligned} \tag{5.16}$$

In Fig. 5.5 one can notice the overshoot, a phenomena that one wishes to minimize to prevent damage. Notice that the maximum overshoot occurs when $t' = 3$ this means that the expression for the peak overshoot is given by

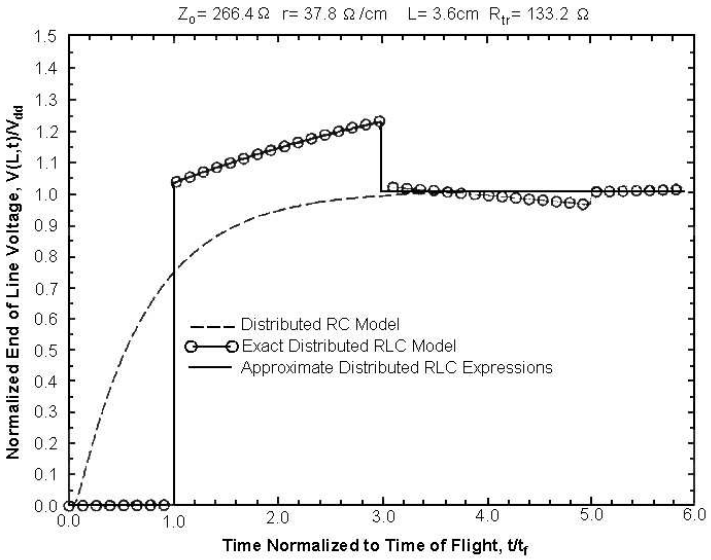


Figure 5.5: Finite line first reflection approximation compared to complete compact model. Figure taken from [54]

$$\frac{V(L,t=3t_f)}{V_{dd}} = \frac{2Z_0}{Z_0+R_{tr}} e^{-(3rL/2Z_0)} \times \left\{ \begin{array}{l} I_0\left(\frac{rL}{2Z_0}\sqrt{8}\right) + (\Gamma+3)\left(\frac{1}{2}\right)^{1/2} I_1\left(\frac{rL}{2Z_0}\sqrt{8}\right) \\ + \frac{(\Gamma(\Gamma+3)+4)}{2} I_2\left(\frac{rL}{2Z_0}\sqrt{8}\right) \end{array} \right\} \tag{5.17}$$

Equation (5.17) really express overshoot when its value is greater than one. If the result is less than one, one can assume that there is not overshoot, thus a better expression for the peak overshoot would be

$$\frac{V_{overshoot}}{V_{dd}} = \max\left(1, \frac{V(L,t=3t_f)}{V_{dd}}\right) \tag{5.18}$$

5.4 Time delay expressions in the RLC domain

In the RLC domain, Sakurai's approximation is no longer valid. In this domain the requirement for $t_{50\%} = t_f$, is the condition for which the front end voltage of a finite line

is greater than half V_{dd}, i.e.

$$V_{fin}(L, t_f) > 0.5\, V_{dd} \tag{5.19}$$

Using equation (5.14) together with (5.9), we rewrite the condition to

$$\frac{4Z_0}{R_{tr} + Z_0} e^{-(rL/2Z_0)} > 1, \tag{5.20}$$

therefore

$$e^{rL/2Z_0} < \frac{4Z_0}{R_{tr} + Z_0} \tag{5.21}$$

with leads to the resulting condition:

$$\frac{rL}{Z_0} < 2 \ln \frac{4Z_0}{R_{tr} + Z_0}. \tag{5.22a}$$

Moreover the relationship

$$R_{tr} < 3Z_0 \tag{5.22b}$$

must hold, otherwise the logarithmic term in the right-hand side of (5.22a) becomes negative, making the satisfaction of this condition impossible.

We impose, a safeguard to the sub-domain, for the purpose of protecting the remains of the circuit to overshoot that can among other things damage a transistor situated at the end of the line. In Fig. 5.6 it is shown the normalized peak overshoot for some values of Z_0 and R_{tr}. This figure is the result of applying equation (5.17). Notice that we can avoid overshoot if the condition $\frac{R_{tr}}{Z_0} \geq 1$ holds.

We shall then introduce as constraint:

$$R_{tr} \geq Z_0. \tag{5.22c}$$

If the previous conditions can be satisfied for reasonable values of the parameters such as to be useful in a feasible design, the wire would be operating as a transmission line. This is to say, the domain where the delay is linear with the distance and the speed of propagation is that of the speed of light in the medium, the fastest propagation physically possible.

This time of flight propagation requires satisfaction of (5.22a). For safe designs

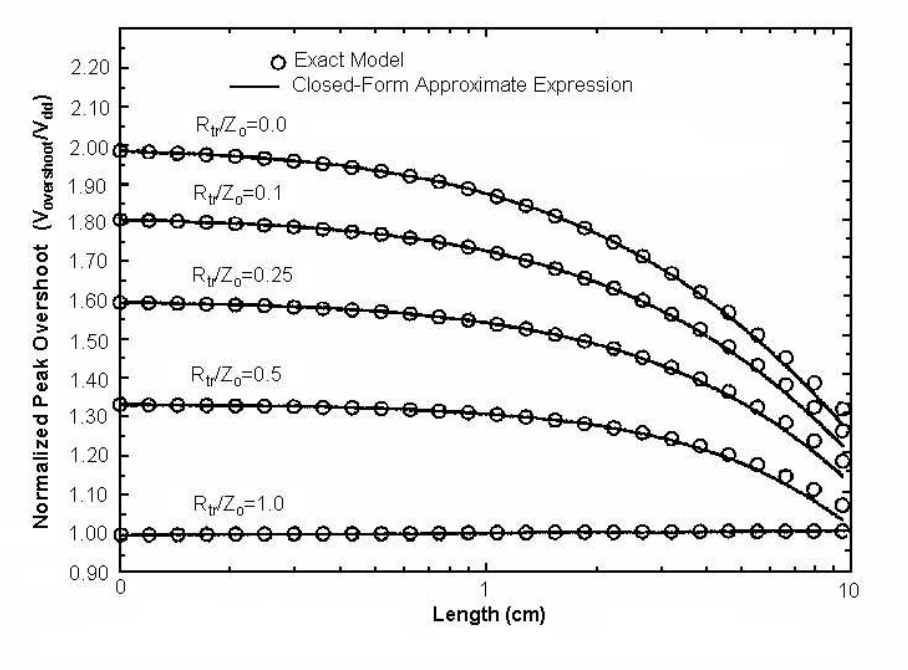


Figure 5.6: Verification of simplified overshoot expression ($Z_0 = 266.5\Omega, r = 37.87\Omega/cm$). Figure taken from [54].

with no overshoot the condition (5.22c) has to be fulfilled.

The propagation time delay is then given by the following model:

$$\begin{aligned} \tau &= \sqrt{lc}L \\ \text{when } \frac{rL}{Z_0} &< 2\ln\frac{4Z_0}{R_{tr}+Z_0} \text{ and } Z_0 \leq R_{tr} \end{aligned} \tag{5.23}$$

In [54] this region of transmission line behavior is called Region I. Wires which do not fulfill (5.22a) can be considered as belonging to the RC domain. For these wires Sakurai's expression is valid.

There are cases for realistic values of the parameters, where the direct application of Sakurai's expression leads to a lower value, than the corresponding RLC delay. These cases are unphysical. Sakurai's expression in neglecting the wave behavior, does not take into account causality effects, maximum speed of signal propagation. The expression becomes clearly invalid when the predicted time delay is shorter than that of a signal propagating at the speed of light in the medium. As can be seen in Fig. 5.7, the RC delay expression violates causality for wires shorter than a centimeter. In this graph

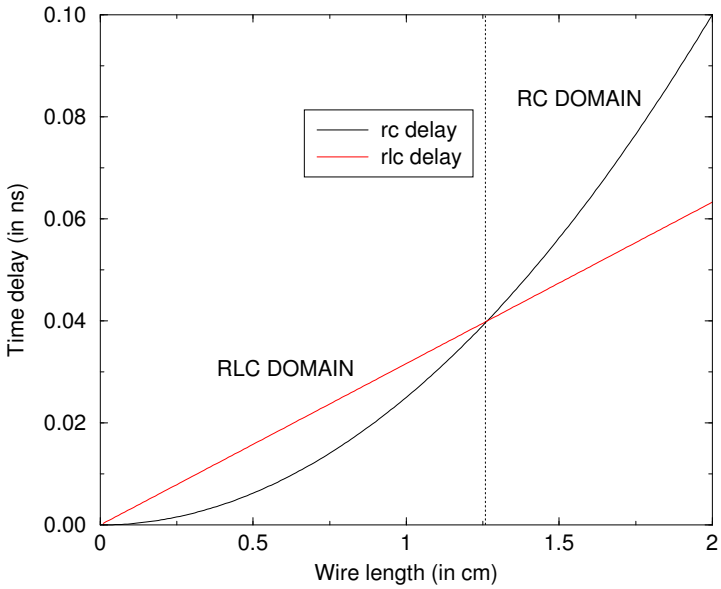


Figure 5.7: Time delay in function of wire length in the RC and RLC domains. For a wire of rectangular cross-section with width 5μm and thickness of 0.65μm.

we can observe the wire lengths for which each of the two domains is applicable.

5.5 New time delay expression for nonzero rise time and finite load capacitance

The function $V_{DM}(t) := V_{fin}(L, t)$ given in (5.14) corresponds to the response of a finite and open-ended wire to a Heaviside step pulse with amplitude V_{dd}. A correction to $t_{50\%}$ is necessary when the input signal has nonzero rise time T_{rise}. For wires in region I, the correction in zeroth order is given by:

$$t_{50\%} = t_f + \frac{T_{rise}}{2}. \tag{5.24}$$

We shall improve on this approximation.

We want to find the expression of $V_{out}(t) = V(x = L, t)$ for a general input signal. We know that the response to an input signal $I(t)$ is related to the transfer function $T(t)$ of the line as:

$$T(t) * I(t) = V_{out}(t), \tag{5.25}$$

where $f * g$ means the convolution of f and g:

$$f(t) * g(t) = \int_{-\infty}^{\infty} f(\tau)g(t-\tau)d\tau. \tag{5.26}$$

If $I(t)$ is a Heaviside unit step function $H(t)$, then $V_{out}(t) = V_{DM}(t)/V_{dd}$. Thus, we have:

$$T(t) * H(t) = \frac{V_{DM}(t)}{V_{dd}}. \tag{5.27}$$

Convoluting both sides of equation (5.25) with $H(t)$ and similarly convoluting both sides of equation (5.27) with $I(t)$ we have:

$$(T(t) * I(t)) * H(t) = V_{out}(t) * H(t) \tag{5.28}$$

and

$$(T(t) * H(t)) * I(t) = \frac{V_{DM}(t)}{V_{dd}} * I(t) \tag{5.29}$$

equating (5.28) and (5.29) we obtain

$$V_{out}(t) * H(t) = \frac{V_{DM}(t)}{V_{dd}} * I(t). \tag{5.30}$$

Differentiating both sides of equation (5.30) we arrive to:

$$V_{out}(t) = \frac{1}{V_{dd}} \frac{d}{dt}(V_{DM}(t) * I(t)). \tag{5.31}$$

This means that the response V_{out} to any general input signal $I(t)$ is a function of the response to a Heaviside step pulse, $V_{DM}(t)$.

Consider now a Heaviside function with non-zero rise time, with amplitude V_{dd}, i.e. $I(t)$ is of the form:

$$I(t) = \begin{cases} 0 & \text{if } t \leq 0 \\ \frac{V_{dd}t}{T_{rise}} & \text{if } 0 < t \leq T_{rise} \\ V_{dd} & \text{if } t > T_{rise} \end{cases}. \tag{5.32}$$

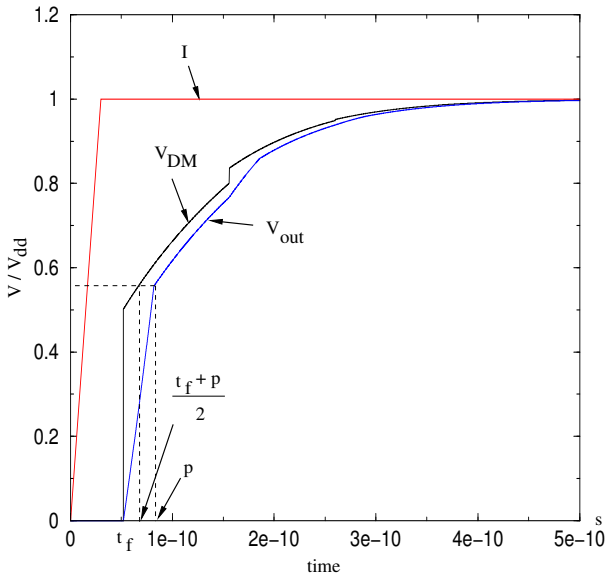


Figure 5.8: Voltage response for both a step and a finite rise time Heaviside functions.

By virtue of (5.31), the response, $V_{out}(t)$, to this input signal is given by:

$$V_{out}(t) = \frac{1}{V_{dd}} \int_{-\infty}^{\infty} V_{DM}(\tau) \frac{dI(t-\tau)}{dt} d\tau. \tag{5.33}$$

Using (5.32) to compute the time derivative of $I(t-\tau)$ leads to

$$V_{out}(t) = \frac{1}{T_{rise}} \int_{t-T_{rise}}^{t} V_{DM}(\tau) d\tau. \tag{5.34}$$

We assign values of the parameters (R_{tr}, L, r, l and c) in (5.16) such that the resulting configuration be in Region I. We evaluate numerically (5.34). Results are shown in Fig. 5.8. Notice that the derivative of $V_{out}(t)$ has its first two discontinuities at $t = t_f$ and at a point $t = p$, that we shall identify. To this effect, we derivate (5.34):

$$V'_{out}(t) = \frac{1}{T_{rise}} \left[V_{DM}(t) - V_{DM}(t - T_{rise}) \right]. \tag{5.35}$$

The first two discontinuities of (5.35) are at $t = t_f$ and $t = t_f + T_{rise}$, since V_{DM} has a discontinuity at $t = t_f$. We conclude that: $p = t_f + T_{rise}$.

Evaluating (5.34) at $t = t_f + T_{rise}$

$$V_{out}(t_f + T_{rise}) = \frac{1}{T_{rise}} \int_{t_f}^{t_f+T_{rise}} V_{DM}(\tau)d\tau. \tag{5.36}$$

From the mean value theorem, it follows that:

$$V_{out}(t_f + T_{rise}) \approx V_{DM}(t_f + \frac{T_{rise}}{2}). \tag{5.37}$$

Consider now the linear approximation to $V_{out}(t)$ in the interval $t_f \leq t \leq t_f + T_{rise}$:

$$V_{out}(t) \approx \frac{V_{DM}(t_f + T_{rise}/2)}{T_{rise}}(t - t_f). \tag{5.38}$$

Impose $V_{out}(t) = 0.5V_{dd}$, which is feasible since we take solutions in Region I, and obtain:

$$t_{50\%} = t_f + \frac{T_{rise}}{2}\left(\frac{V_{dd}}{V_{DM}(t_f + T_{rise}/2)}\right), \tag{5.39}$$

which is the corrected expression for the 50% time delay in the presence of a nonzero rise time. It improves significantly over the naive shift in the delay computation presented in (5.24). The expression (5.39) has been derived for $T_{rise} < 4t_f$, since at this point other discontinuities are encountered in $V_{DM}(t)$. It is worth noticing that if the condition $T_{rise} < 4t_f$ is fulfilled then the function $V_{DM}(t)$ is well approximated by the simpler expression (5.16).

We verify numerically that the relative error incurred in the delay calculation, resulting from the linear approximations presented above, is very small for $T_{rise} \leq 2t_f$. For this purpose we take an exemplary line with parameters such as to belong to region I. The line is fed with a Heaviside function of amplitude V_{dd} with time rise T_{rise}. In Fig. 5.9 we present the relative difference between results from time simulation and results obtained using (5.39) as a function of T_{rise}.

The error increases with T_{rise}, and for $T_{rise} = 2t_f$ is a reasonable 3%. The error becomes large by the time we reach the upper limit $T_{rise} = 4t_f$. We can summarize these bounds in the following fashion:

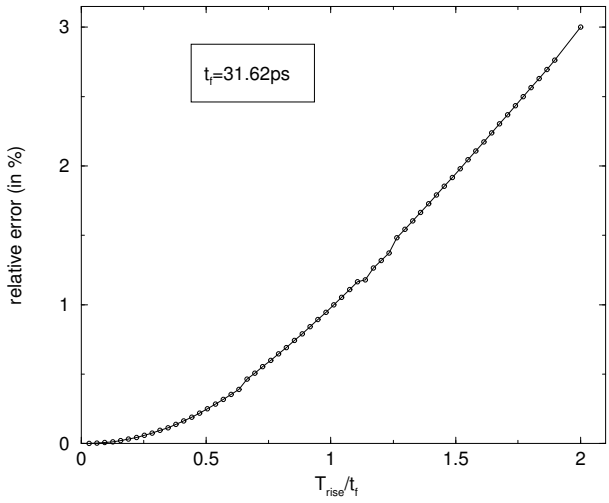


Figure 5.9: Relative error in $t_{50\%}$ when using (5.39) as a function of T_{rise}/t_f. Parameters used: $r = 5000\ \Omega$/m, $l = 2 \times 10^{-7}$ H/m, $c = 2 \times 10^{-10}$ H/m, $L = 5$ mm, $R_{tr} = 50\ \Omega$

Expression (5.39), is a solution to the delay estimate for a signal in Region I if

$$T_{rise} \leq 2\sqrt{lc}L = 2t_f. \tag{5.40}$$

As a matter of fact, for fixed T_{rise}, the L dependence in (5.39) displays both linear and quadratic behavior. The quadratic term in length is not present in the zero rise time solution. Its contributions is nonetheless negligible due to (5.23). Both (5.23) and (5.40) have been previously derived in the literature for RLC behavior using alternative methods, see [44] and [57].

5.5.1 Finite Period and Finite Load Capacitance Effects

Clocks have a finite period. It is provable that corrections to (5.39) due to a finite clock period are negligible for a clock period of reasonable bandwidth (clock period larger than $6\,T_{rise}$.)

To preserve the validity of TL description, load capacitance must be small compared to line capacitance. The presence of a finite lumped load capacitance in the delay calculation can be treated as a two-step procedure: the propagation delay of the line with zero load plus the delay associated with charging the load capacitance. To compute the last term we treat the line as a resistance of value Z_0. In the standard Sakurai [5] treatment

we estimate that the total delay becomes:

$$t_{50\%} = t_f + \frac{T_{rise}}{2}\left(\frac{V_{dd}}{V_{DM}(t_f + T_{rise}/2)}\right) + 0.693 Z_0 C_{load}, \tag{5.41}$$

if $T_{rise} < 2t_f$, $\frac{rL}{Z_0} < 2\ln\frac{4Z_0}{R_{tr}+Z_0}$ and $\frac{C_{load}}{cL} << 1$. Otherwise,

$$t_{50\%} = 0.377 rcL^2 + 0.693(R_{tr}cL + (Z_0 + R_{tr})C_{load}). \tag{5.42}$$

The previous expressions characterize the extended transmission line domains and distributed capacitance-resistance domains. A complementary analysis of the finite capacitance effects can be seen in [58].

5.5.2 Follow up work in this domain

In a recent paper from UCLA [59], a simplified and efficient model for the response of a single transmission line considering non-zero rise time and load capacitance is presented. Their approach consists in first considering the capacitive loaded line as an open line by adding the contribution of C_{load} into the inductive and capacitive parts of the line. Using an efficient and accurate piecewise linear approximation to (5.14) and using our result in (5.31) they achieve very high accuracy in both the waveform and the delay prediction for the general case.

5.6 Concluding remarks

In this chapter we have mostly displayed the relevant equations for RLC lines from a recent paper of Davis and Meindl. This equations permit to extend the delay calculation to the RLC domain. We have not dwelled on other approaches, namely those who replace a transmission line with a discrete single RLC section. The reason why we are doubtful of the results of a single RLC section is that it will show instantaneous propagation, moreover, the effects of inductance will be overemphasized - it is the smoothing effect due to several reflections that lead to the correct behavior. As a side remark we should add, that in the RC domain the replacement of the full RC network with a single section is significantly less dangerous, we would say even permissible in a restricted sub-domain. Monotonicity in the time behavior of RC signals supports the validity of the approximation. No such behavior is guaranteed in the RLC domain.

As corrections to DM expressions we derived new expression(s) for the time delay calculation in the RLC domain in the presence of finite T_{rise} (5.39). We propose a general expression accounting for transmission line, finite rise time as well as finite lumped C_{load} effects.

Chapter 6

Optimal design of clock trees

Conception optimale d'arbres d'horloge

Résumé

Dans ce chapitre nous proposons une méthodologie de conception pour des arbres d'horloge. Cette méthodologie consiste à trouver un intervalle de valeurs des paramètres géométriques de façon à assurer que les signaux se déplacent à la vitesse de la lumière dans le milieux, i.e., la plus grande vitesse possible. Cette méthodologie est très utile pour les concepteurs qui cherchent à créer des horloges avec un temps de réponse minimum. Pour assurer un temps de désynchronisation minimal, nous étudions les arbres H, dont le signal est entouré par deux arbres de masse. Cette configuration permet un contrôle réalisable des valeurs d'inductance de boucle. Ceci permet donc l'utilisation en notre faveur de ce que la plupart des spécialistes préfèrent réduire et négliger : l'inductance.

Ce chapitre est une extension d'un des résultats présentés dans les articles [10] et [11]. Un brevet américain, protégeant cette technologie, a été attribué en Avril 2006 [12].

6.1 Introduction

Circuit designers and technology engineers work vigorously towards developing techniques to minimize inductance influence so as not to perturb well developed and under-

stood design styles. We take a different twist - that of making good use of inductance effects on wire line delays so as to attempt to minimize these delays by a careful balancing of the electric and magnetic content on the energy content of a line such that as an end effect the propagation of a voltage perturbation on the line can be as fast as possible: the speed of light on the medium, the maximum possible speed of propagation of a signal. The way we attack this problem is by a combination of nonlinear optimization techniques, with the solution of known linear partial differential equations. The proposed methodology can be used as a pre-estimator and or as a verifier of layout techniques for wires that carry critical signals on a high speed logic design. We find that in fact an extensive set of technology parameters (wire widths, lengths, separations and thicknesses) can be set so as to satisfy this desideratum. Our resulting parameter values fall well within what is possible and doable with current technologies.

We shall illustrate our methodology on what is perhaps the most important wire configuration for today's top speed microprocessors: The Clock. The clock is unarguably one of the most important components of a synchronous digital design. Its signal must arrive with minimum tolerance (skew) to all synchronized elements within a synchronization region. The size of the maximum synchronization region is determined by the ability of the signal to reach all its destinations within a predetermined interval. What is the interval: A rule of thumb would say larger than the rise time of the signal, and significantly shorter than the period of the clock. For generations of digital designs the whole chip has been considered as the synchronization region. In todays world of Ultra Very Large Scale Integration (UVLSI) a new regime is being explored. Let us elaborate: thanks to miniaturization, rise times which are controlled by the transistor propagation delays are of the order of 15 pico-seconds at todays leading edge technologies. This number scales as $1/\Lambda$, where Λ is the scaling factor: The ratio of the critical dimension at the new technology over the precedent technology.

Thus the range for an aggressive 4 GHz design are

$$1.5 \times 10^{-11} s < t < 0.25 \times 10^{-9} s\,.$$

To be able to minimize the latency during a clock period one wishes for t to be comfortably close to the lower limit. A realizable expected goal for the propagation time across the synchronization region is $t \approx 10^{-10} s$. And its variance in arriving to different destinations to be smaller than a predetermined budget of $\Delta t \leq 5 \times 10^{-11} s$. This last

figure is what we call the skew. What is the maximum distance that a signal can travel within this time period: The absolute bound is given by signals propagating at the speed of light in the medium:

$$c = \frac{3 \times 10^8}{\sqrt{\varepsilon_r \mu_r}} \frac{m}{s};$$

where ε_r is the relative permittivity of the surrounding dielectric and μ_r is the magnetic permeability of the medium. For today's designs where $\varepsilon_r \approx 2$ the maximum possible synchronization distance for this aggressive processor choice is 3cm, comparable to the linear chip dimension. It is the advent of UVLSI that has made the global clock discipline a new hard concern in the design of digital systems. The faster the clock, the shorter the synchronization distance. Similarly the corresponding synchronization budget for the skew forces a maximum $\Delta l < 1.5cm$ between different paths of the clock between source and destination to arrive within the pre-specified budget. A path synchronization to an accuracy of $1.5cm$ is not so hard to achieve. But the truth is that this bound is very optimistic. Indeed it presumes the ideal situation in which the propagation signals on the different parts of the clock circuit can in fact be considered as the propagation over transmission lines, at the speed of light. Signal propagation over wires do not necessarily fall within this regime. Most wires in fact operate within the regime of RC "diffusion lines", whose speed of propagation- or rather diffusion- are significantly smaller than the speed of light with uncertainties which in the diffusion delay regime are difficult to control. This is due to their sensitivity to the signal activity in nearby lines. This complicated picture forces an iterative procedure of design followed by verification and redesign in order to control the time delay and skew bounds.

The purpose of this work is to contribute to the state of the art and design effort towards finding appropriate regimes for the wire distribution and its environment such that the theoretical limits regarding signal arrival times and length variations can be satisfied.

6.2 The model problem

Given a routing plane with clock input C_0, and with multiple destinations P_i, $i = 1, \ldots, n$, we want to find the layout of interconnection that minimizes both the delay

$$D = \max t(C_0, P_i)$$

and the skew

$$S = \max\{|t(C_0, P_i) - t(C_0, P_j)|\},$$

where $t(C_0, P_i)$ is the time that the signal needs to arrive from C_0 to P_i.

There are several approaches to layout clocks [60]:

1. Balanced H trees, as seen in figure 6.1.a)
2. Centrally driven grids, as seen in figure 6.1.b)
3. Length-matched serpentine 6.1.c)
4. A variation of 1 and 2: here the global wiring is done with balanced H trees, supported by grids near the transistor destination.

The configuration choices presented above are the result of years of experience in the RC domain.

In the new domain of RLC only a subset of these choices survive. The reason for the additional chopping is the controllability of the inductance effects. In particular Configurations 2 and 3 fall into the category of configurations where it is difficult to bound prior to knowing the full layout the magnitude of the inductance, and therefore its main impact on the delay.

We are driven to examine carefully Balanced H-trees with the possible inclusion of grids very near the terminal devices. These inclusions we anticipate will not affect our conclusions, and we omit their analysis in this study.

There are other authors who have previously considered inductance effects in wire delay. We discussed relevant results in the previous section. We need to add to this list a recent study done by [61] contribution which we use as a starting point in our work. In that paper, the H-tree clock signal layout is considered. This design consists of: The association for each segment of clock wire two parallel segments of ground, one at each side of the line. This is the so called “sandwich style”, as we can see in figure 6.2, a technique adopted earlier by IBM [60].

The Stanford group studies the upper and lower bounds on chip clock loop inductance. This information provides some insights into the timing problem of delay, without answering the fundamental question of minimizing the time delay or the skew. The reason being is that Inductance minimization by itself does not produce desirable configuration for time delay since the resulting configuration (ground wires very close to

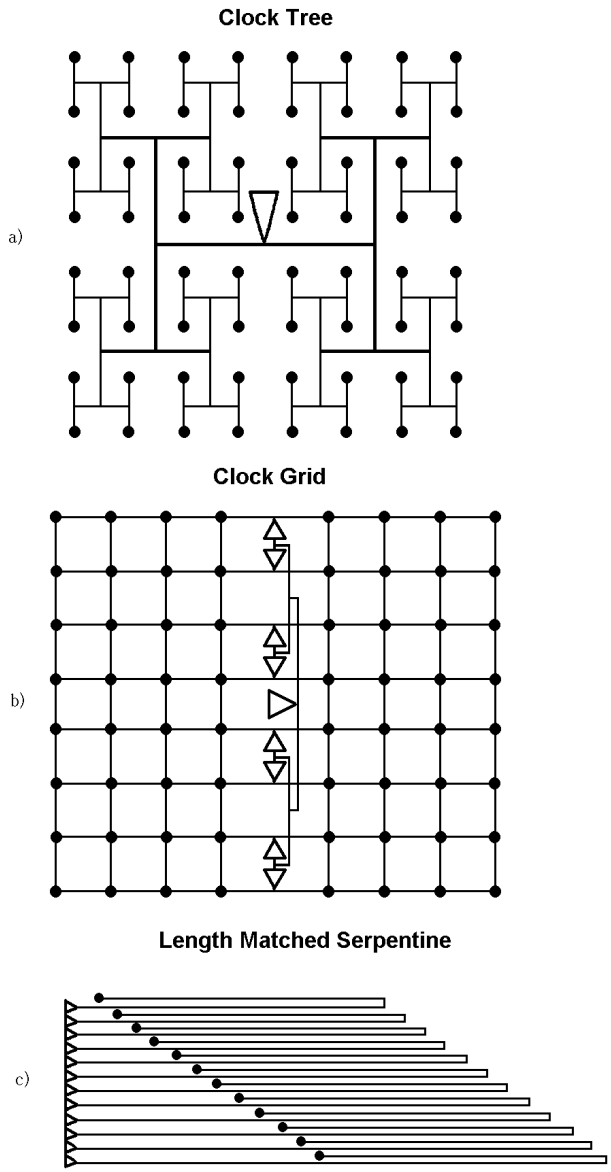


Figure 6.1: Different clock layouts [60]: a) A balanced clock H, b) centrally driven grid and c) length-matched serpentine.

the signal line), is one in which the mutual capacitances reaches their upper limit. Both components: Capacitance and inductance need to be simultaneously optimized to solve the fundamental problem posed at the introduction of the Stanford paper.

We shall address the fundamental timing optimization problem for sandwich Bal-

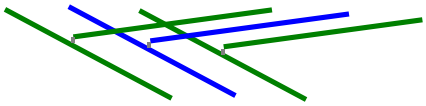


Figure 6.2: Example of a configuration using the "Sandwich style". The blue line represents the signal wire. The two other green lines represent the ground neighbors.

anced H-trees. We attack this problem using the fundamental equations of transmission line theory in the time domain as recently derived by Davis and Meindl and presented in chapter 5. The determination of the r, c and l parameters will be the result of accurate 3D evaluations. We finally address the resulting nonlinear r,l,c coupled optimization using well known techniques.

6.2.1 Balanced H trees

We will focus our analysis in the balanced H tree clock layout. See figure 6.3. This kind of networks have some very positive features. Topologically, an H tree has the property of connecting its nodes in a way such that the Manhattan L_1 distance between the root and any of the leaves is minimal, fulfilling the restriction that they have to be equal. This type of configuration guarantees minimum skew, and searches to minimize delay a-posteriori.

In a world of high frequencies, where inductance effects become relevant, a key advantage of the sandwiched style balanced H trees is the controllability of the loop inductance.

For a Sandwich Balanced H-Tree (SBHT) as in figure 6.3, the total loop inductance of any path can be calculated as the sum of the loop inductances of the straight wires that conform it, this means that, given a path $P(C_0, P_i) = \{C_0, N_1, N_2, ..., N_k = P_i\}$ we have

$$L_{loop}(P(C_0, P_i)) = \sum_{j=1}^{k} L_{loop}(\{N_{j-1}, N_j\}), \text{ where } N_0 = C_0 \tag{6.1}$$

This proposition, the cascade rule, was empirically proposed by [62]. Using a test problem we were able to verify the accuracy of this proposition, and as such its suitability. With the H tree as in figure 6.4 we have calculated the total loop inductance from the clock source C_0 to all the destinations P_i. Then we have compared it to the

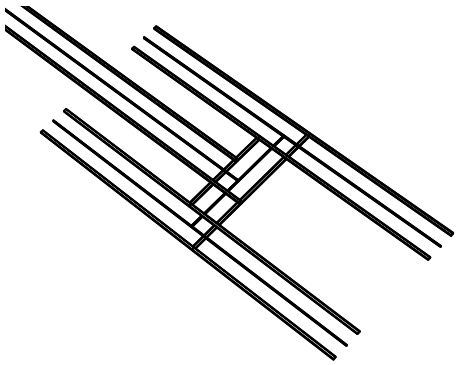


Figure 6.3: An example of an H-tree designed in a sandwich style.

sum of the loop inductances of the pieces (N_j, N_{j+1}) that form each path $P(C_0, P_i)$. In table 6.1 the values of the loop inductance of each of the complete paths and the approximate values using the cascade rule are shown. We used for this experiment the 3D inductance simulation tool, FastHenry [6] from MIT. We verify also that the inclusion of extra ground wires further away do not sensibly modify this important result.

P_i	Total l of $P(C_0, P_i)$	Cascade rule
P1	0.687	0.687
P2	0.688	0.687
P3	0.688	0.687
P4	0.688	0.687
P5	0.689	0.687
P6	0.689	0.687
P7	0.689	0.687
P8	0.689	0.687

Table 6.1: Values of the total loop inductance of path $(C_0 - P_i)$ compared to the value of using the cascade rule. Values in nH.

It is in fact a very important benefit to be able to locally bound the inductance values well before a detailed routing of signals is attempted. This automatically leads to the selection of SBHT for clock design.

The problem of calculating the loop inductance of complex paths of signal wires, in a SBHT configuration where the wires are allowed to change their widths and lengths with each change of direction, is now reduced to the problem of finding the loop induc-

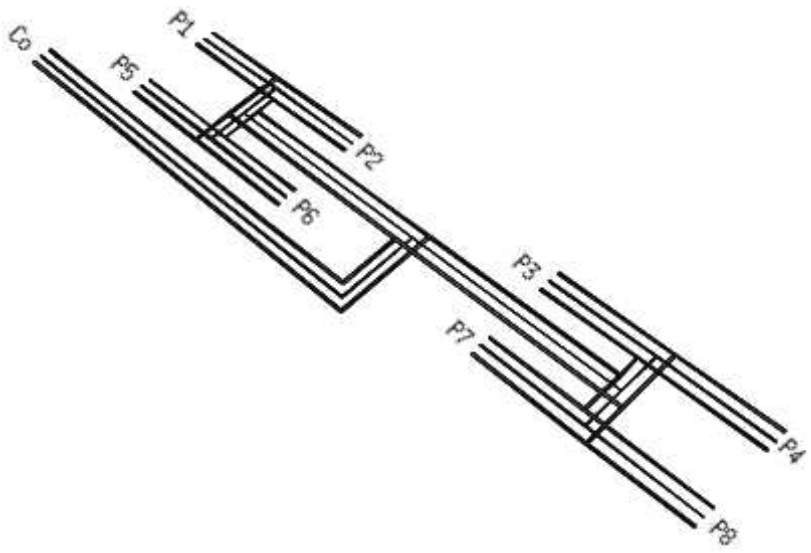


Figure 6.4: A test H-tree (sandwich style), with source C_0 and eight destinations N_i.

tance of a 3-wire sandwich of same length, a consequence of (6.1), which is substantially simpler to solve.

6.3 Time delay minimization

We can forego the skew minimization, since it is automatically included by design on SBHT.

In the presence of coupling with nearby ground wires, wire length L is just one of the variables that determines time delay. The other relevant variables, that impact on the delay of the signal are: wire separation; wire width and thickness; and driver resistance. We have the challenge of finding technically feasible configurations that minimize the propagation delay. A configuration is defined as the complete characterization of all the variables for a specific technology and a specific realization of the layout of the clock. We use the 50% metric as has become standard practice, i.e., we translate our problem into one of finding configurations in the RLC regime that minimize the 50% time delay. Thus, our problem is:

$$\begin{aligned} &\min t_{50\%} \\ &\{\text{Subject to some constraints relative to the technology}\} \end{aligned} \tag{6.2}$$

6.4 Transmission line propagation

6.4.1 Domains of Validity

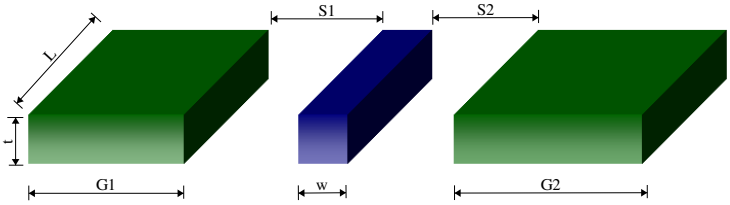


Figure 6.5: The model problem. A sandwich style bus.

We consider the model problem of the SBHT clock system (figure 6.5). The variables of this problem are those that define a given configuration:

1. L: length of the wires.
2. t: thickness of the corresponding metal layer.
3. w: width of the signal line.
4. G_1, G_2: widths of the ground wires.
5. S_1, S_2: edge-edge spacing between the signal wire and its neighbors.
6. R_{tr}: The effective resistance of the driving transistor.

A key goal is to find domains of the physical variables where the configurations belong to region I, i.e. fulfilling constraints in (5.23). Inserting r, l and c for a given configuration and testing if inequalities in (5.23) are satisfied is extremely inefficient. We use instead a method for solving nonlinear equations to identify the feasible domains. To this effect we take some variables as external parameters. The signal wire's

width w is the result of a specific routing configuration and as such is a natural parameter. The variable t takes only a few discrete values, another parameter. The driver's strength measured by R_{tr} is external to the wire configuration and determined by transistor dynamics, we take it as a parameter, and so is the length of the line L, determined by the chip dimensions and the particular starting point of the routing. We are left with s and g as independent variables which are natural ones in the sense that variables vary on a continuous fashion while parameters take discrete values.

We define the functional F:

$$F = \frac{rL}{Z_0} - 2\ln(\frac{4Z_0}{R_{tr} + Z_0}), \tag{6.3}$$

We search domains where $F \leq 0$ is satisfied, i.e. to fulfill (5.22a).

To ensure safe operation of the circuit we add the restriction $Z_0 \leq R_{tr}$ (from (5.22c)) that guarantees the absence of overshoots [54], and the corresponding functional:

$$P = Z_0 - R_{tr}, \tag{6.4}$$

i.e., the solution domains must satisfy $P \leq 0$.

This approach is complemented a-posteriori with the insight gained during the search of minima. In fact it is found that continuous regions in the space of the independent variables can be found such that they belong to the region bounded by equation (5.23). It is the richness of this spectrum what provides viability to the method as a design assistance tool for clock tree layout.

6.4.2 The functions

The functions F and P in (6.3) and (6.4), respectively, can be generated from the knowledge of the following three functions:

1. r: the resistance per unit of length of the configuration.
2. l: the inductance per unit of length of the configuration.
3. c: the total capacitance per unit of length of the wire.

Since we are interested in the computation of the time delay of a three-wire circuit we have to compute the values of r and l of the configuration in terms of the corresponding values for its constituents. In so doing we arrive to an equivalent description

in terms of a single wire of loop inductance l and loop resistance r in the presence of an ideal ground.

6.4.3 Resistance

We have seen, in chapter 2 that for configurations where there is no skin effect, the closed form for the resistance per unit length in a wire of cross-section area A is given by

$$r_w = \frac{\rho}{A} \tag{6.5}$$

with ρ the resistivity of the material the wires are made of (e.g. $\rho = 1.72 \times 10^{-6}\Omega$.cm for Cu).

Wires have rectangular cross-section: the signal one with $A = w \times t$ and the ground wires with $A = G \times t$.

Given the circuit as in figure 6.6, we are interested in finding an equivalent series resistor using the same overall voltage drop V, Ohm's law $V = RI$, and the same I the total current of the circuit.

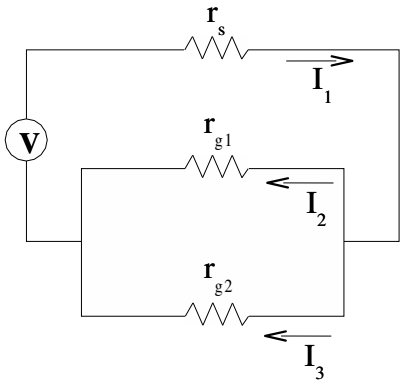


Figure 6.6: A sandwich-style design with resistance only.

From Ohm's law:

$$\begin{aligned} V &= r_s I_1 + r_{g1} I_2, \\ V &= r_s I_1 + r_{g2} I_3. \end{aligned} \tag{6.6}$$

Since we are considering the symmetric problem we have

$$r_{g1} = r_{g2} \text{ and}$$
$$I_2 = I_3,$$

since

$$I_1 = I_2 + I_3,$$

therefore

$$I_2 = \frac{1}{2} I_1.$$

Given this, it follows that

$$V = (r_s + \frac{r_g}{2}) I_1. \tag{6.7}$$

Therefore the equivalent resistance is

$$r = r_s + \frac{r_g}{2}, \tag{6.8}$$

where

$$r_s = \frac{\rho}{w \times t},$$
$$r_g = \frac{\rho}{G \times t}.$$

6.4.4 Inductance

For the calculation of the inductance for the configuration of interest, the sandwich configuration, under uniform current distribution we use the formulas presented in chapter 2.

Using a similar analysis as we have done with the equivalence resistance of the circuit, we can derive the expression for the equivalent loop inductance.

In figure 6.7 we represent the circuit considering the partial inductances as well. We have, from Ohm's law in the Fourier domain:

$$V = (r_s I_1 + r_{g1} I_2) + j\omega(l_s I_1 + l_{g1} I_2 - 2l_{s,g1} I_2 - 2l_{s,g2} I_3 - l_{g1,g2} I_2) \tag{6.9}$$

where ω is the frequency in radians per second, i.e. $\omega = 2\pi f$ with f the frequency in hertz.

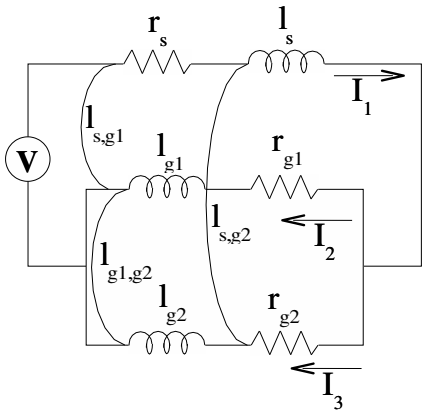


Figure 6.7: SBHT design including resistance and inductance.

Given the symmetry of our problem, it follows that

$$l_{s,g1} = l_{s,g2} \text{ and}$$
$$I_2 = I_3,$$

since

$$I_1 = I_2 + I_3,$$

we have

$$I_2 = \frac{1}{2} I_1,$$

therefore the imaginary part of V is

$$\text{Imag}(V) = \omega(l_s + 2l_{s,g} + \frac{1}{2} l_{g,g} + \frac{1}{2} l_g) I_1. \tag{6.10}$$

Finally the equivalent loop inductance of the circuit is given by

$$l = l_s - 2l_{s,g} + \frac{1}{2}l_{g,g} + \frac{1}{2}l_g. \tag{6.11}$$

In the above equations, the values l_s and l_g are the partial self inductances of the signal wire and of one ground wire, respectively; the values $l_{s,g}$ and $l_{g,g}$ are the signal-ground and ground-ground mutual inductances, respectively.

6.4.5 Capacitance

The equivalent capacitance per unit length of a sandwich element c_{tot} is given by:

$$c_{tot} = c_{s,g_1} + c_{s,g_2} + c_r, \tag{6.12}$$

with c_{s,g_1} and c_{s,g_2} the mutual capacitance between the signal wire and each of the ground wires. The value c_r is the sum of the capacitances of the signal wire to substrate and other wires not participating in the return path. All of the previous quantities are per unit length. Given the symmetry of the problem: $c_{s,g} := c_{s,g1} = c_{s,g2}$.

At variance with resistance and inductance, there are no closed form expressions for the capacitance. We need to perform multiple calculations of the capacitance. The iterative of simulators for this task is out of the question since the task is CPU intensive. We attack the problem in a more efficient way: We use function approximation techniques, that perform data fitting to 3D simulation results. The choice of functional form, that is arbitrary is guided by experience. The parameter fitting process is the result of a non linear least square fit.

In order to choose a sensible functional form for the representation, we perform 3D simulations with the capacitance simulator ICARE, from LETI [63] with representative values of the independent parameters.

We consider separately the capacitance of the signal wire respect to its neighbor ($c_{s,g}$), and its capacitance respect to the layer beneath plus the capacitance with the substrate (c_r).

Mutual capacitance

In figure 6.8 we display the mutual capacitance as a function of S, the dots represent observations, i.e., 3D simulation using ICARE. At simple sight, an exponential depen-

dency seems natural.

Similarly as a function of its width, the mutual capacitance is displayed in figure 6.9. It is suggestive of something approximating a square root behavior.

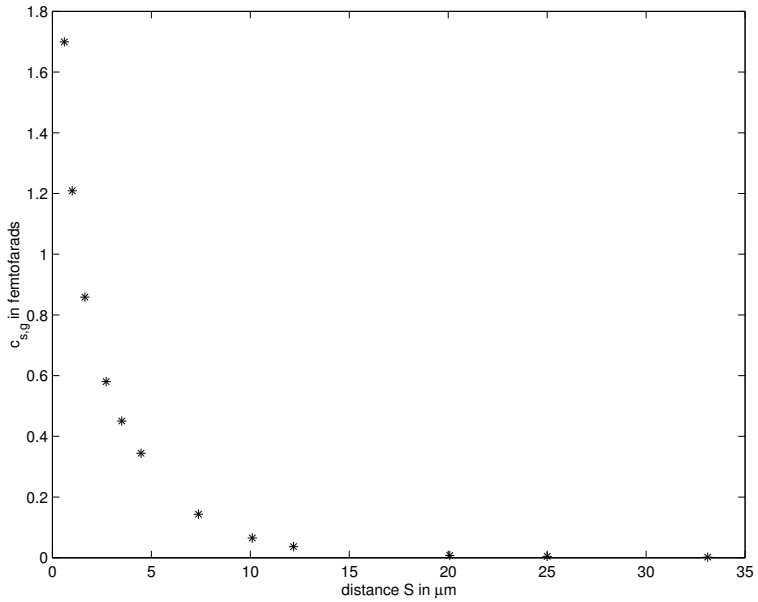


Figure 6.8: Observations: mutual capacitance as function of distance.

Based on these observations we propose the following functional form for the mutual capacitance between the signal wire and one of its ground neighbors*:

$$c_{s,g}(S, w) \approx \left(\beta_1 e^{-\alpha_1 S} + \beta_2 \left(\frac{S}{0.25}\right)^{-\alpha_2}\right) \beta_3 w^{\alpha_3}. \tag{6.13}$$

The problem of fitting function (6.13) to a given set of observations can be considered as a nonlinear least square problem with variables that separate [64], in the following fashion:

First, given a collection of values of variable S, $S = \{S_1, S_2, \ldots, S_n\}$, we can obtain their respective observation values $y_i = c_{s,g}(S_i, w)$ (we set $w = 1$) using ICARE. Now the original problem is represented as the problem of fitting the data (S_i, y_i) to the equation

$$c_1(S) = \beta_1 e^{-\alpha_1 S} + \beta_2 \left(\frac{S}{0.25}\right)^{-\alpha_2} \tag{6.14}$$

*This parameterization is used extensively by Mentor Graphics in Capacitance Extraction Tools

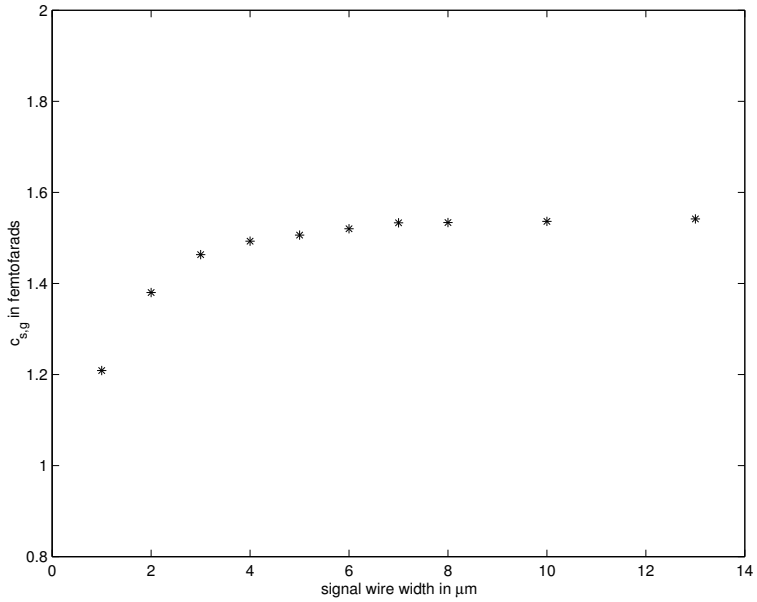


Figure 6.9: Observations: mutual capacitance as function of width.

Our task is to find the values $\boldsymbol{\beta} = (\beta_1, \beta_2)$ and $\boldsymbol{\alpha} = (\alpha_1, \alpha_2)$ that minimize the nonlinear functional

$$r(\boldsymbol{\beta}, \boldsymbol{\alpha}) = \sum_{i=1}^{n} \left[y_i - c_1(\boldsymbol{\beta}, \boldsymbol{\alpha}; S_i) \right]^2 \tag{6.15}$$

Defining $\phi_1(\boldsymbol{\alpha}; S_i) = e^{-\alpha_1 S_i}$ and $\phi_2(\boldsymbol{\alpha}; S_i) = \left(\frac{S_i}{0.25}\right)^{-\alpha_2}$, the functional $r(\boldsymbol{\beta}, \boldsymbol{\alpha})$ can be rewritten as

$$r(\boldsymbol{\beta}, \boldsymbol{\alpha}) = \|\mathbf{y} - \Phi(\boldsymbol{\alpha})\boldsymbol{\beta}\|^2 \tag{6.16}$$

where $\{\Phi\}_{i,j} = \phi_j(\boldsymbol{\alpha}; S_i)$ and $\mathbf{y} = (y_1, \ldots, y_n)^T$, $i = 1, \ldots, n$; $j = 1, 2$.

As explained in the classical paper [64], the aim is to minimize a modified functional which depends only on the nonlinear parameters $\boldsymbol{\alpha}$, and then proceed to obtain the linear parameters $\mathbf{a}$.

In order to obtain the separation of variables, we consider the modified functional

$$r_2(\boldsymbol{\alpha}) = \|\mathbf{y} - \Phi(\boldsymbol{\alpha})\Phi^+(\boldsymbol{\alpha})\mathbf{y}\|^2, \tag{6.17}$$

where $\Phi^+(\boldsymbol{\alpha})$ is the Moore-Penrose generalized inverse of $\Phi(\boldsymbol{\alpha})$. Once optimal parame-

ters $\hat{\boldsymbol{\alpha}}$ have been found by minimizing (6.17), then the linear parameters $\hat{\boldsymbol{\beta}}$ are obtained as the solution of the linear least square problem.

$$\min \|\mathbf{y} - \Phi(\hat{\boldsymbol{\alpha}})\boldsymbol{\beta}\|^2. \tag{6.18}$$

Once we obtain $\hat{\boldsymbol{\alpha}}$ and $\hat{\boldsymbol{\beta}}$ we can compute the value of α_3 and β_3 fixing some value of $S = S_k$ we generate a data set by performing simulations for $w = \{w_1, w_2, \ldots, w_m\}$, we call the resulting observations $y_i = c_{s,g}(S_k, w_i)$. The problem becomes fitting the data (w_i, y_i) to the equation

$$c_2(w) = c_1(S_k)\beta_3 w^{\alpha_3}. \tag{6.19}$$

This new least square problem is also nonlinear, and we again use the non linear least square method of Golub and Pereyra.

We use a modified version of the algorithm proposed by Golub and Pereyra [65] to find the values of the linear parameters $\boldsymbol{\beta} = (\beta_1, \beta_2, \beta_3)$ and the non-linear parameters $\boldsymbol{\alpha} = (\alpha_1, \alpha_2, \alpha_3)$ which best fit the mutual capacitance to (6.13). In figures 6.10 and 6.11 we display the fit.

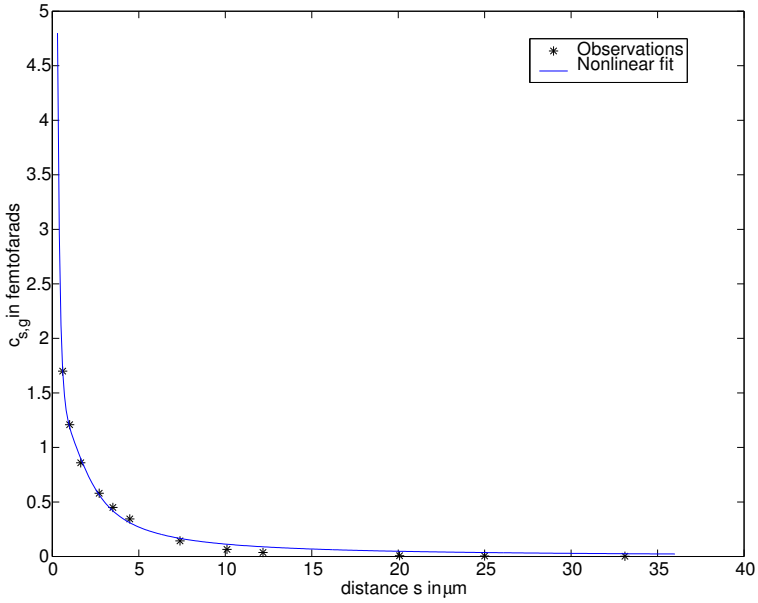


Figure 6.10: fit of c_1, and chosen observation values.

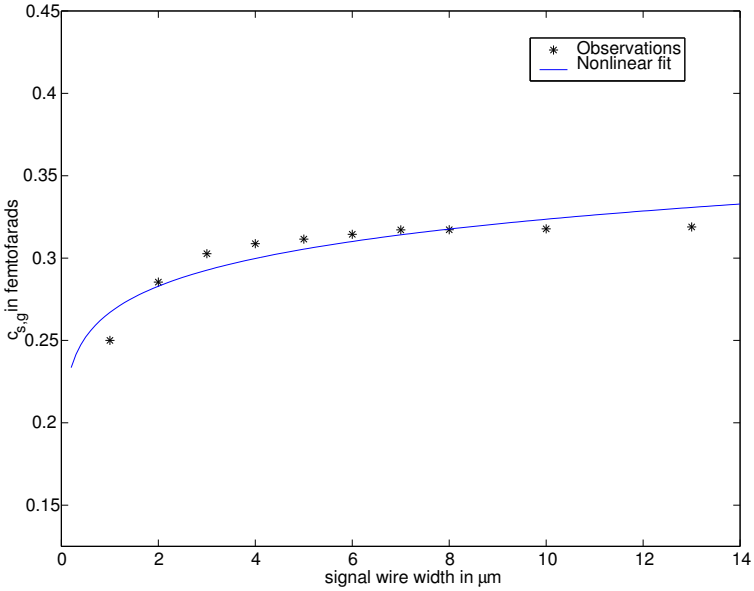


Figure 6.11: fit of c_2 and chosen observation values.

Capacitance to the substrate and to lower layers

Values of c_r in function of S, for different values of w are shown in figure 6.12. There is very weak dependence of c_r versus S. For this reason, we will calculate once, using the simulator, the value of c_r for the given parameter w and a value of S pre-specified by the user. During the optimization phase, the value of c_r will remain constant.

6.5 Minimization

6.5.1 The objective function

Let's examine first the monotonicity of F and P respect to variables s and g. The derivative of F respect to Z_0 is given by

$$\frac{dF}{dZ_0} = -\frac{rLR_{tr} + rLZ_0 + 2\,R_{tr}\,Z_0}{(R_{tr} + Z_0)\,{Z_0}^2}. \tag{6.20}$$

Clearly, functional F is monotonically decreasing with respect to Z_0.

The loop inductance of a sandwich element is evidently monotonically increasing with s. The coupling capacitance $c_{s,g}$ is monotonically decreasing with s. Therefore,

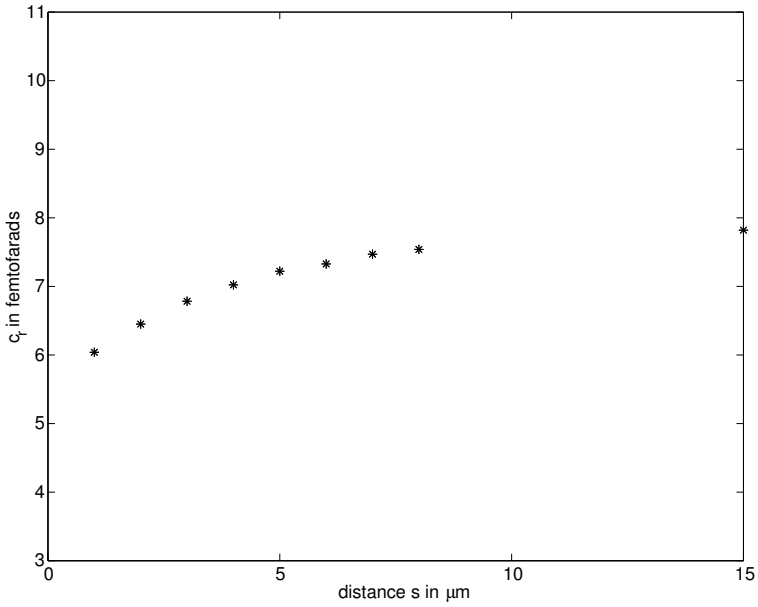


Figure 6.12: c_r observations as function of S.

functional Z_0 is monotonically increasing with respect to s. This implies F is monotonically decreasing with s and P monotonically increasing with s.

Simulations with FastHenry show that Z_0 as a function of g displays a single minimum (Fig. 6.13), consequently, P as function of g, have at most two vanishing points. Furthermore, it is verifiable that F, as function of g, has at most one point where it vanishes.

We take advantage of monotonicity of both functionals F and P in order to find the solution set for variables s and g. We consider two independent problems: The first one in which solution sets for s are found for a fixed value of g, and the second one in which solution sets for g are found for a fixed value of s.

In the first problem we search the two values of s: $s = s_F$ and $s = s_P$ where functionals F and P respectively vanish. Notice that by virtue of monotonicity of functionals F and P, the solution set in s is a continuous interval. This property is critical for successful clock synthesis using this method. This solution interval, if it exists, is the intersection of the following two intervals: $[s_F, s_P]$ and $[s_{min}, \lambda/10)$, with s_{min} the technology's minimum feasible metal spacing and λ the wavelength. The upper bound $\lambda/10$ being the limit of validity of the TL representation.

Regarding to variable g, the interval, if it exists, where $F(g) \leq 0$ is $[g_F, \lambda/10)$ with

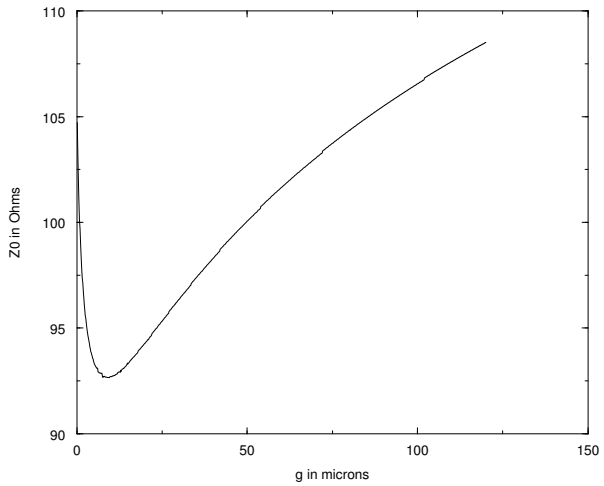


Figure 6.13: Z_0 as a function of g.

g_F the value of g where F vanishes. This interval has to be intersected with the intervals of g where $P(g) \leq 0$. We find this intersection by obtaining the values of g where P vanishes, if they exist, and then identify these intervals by inspection.

6.5.2 Tools

To solve the minimization problem we built an integrated tool-set. In the following list we enumerate and briefly describe the tools of the set. In figure 6.14 a diagram flow is presented.

1. The program LR3.c: This C program calculates the loop inductance and the loop resistance of a 3-wire bus. This program uses the low frequency formulae of chapter 2.

2. The subroutine varpro.f: This is a Fortran77 implementation of the algorithm of Golub and Pereyra, for the resolution of the non-linear least square problem whose variables separate. This implementation is due to J. Boldstad, given to us by Professor Pereyra.

3. The program Capa.c: The C implementation of the capacitance calculator. This program uses the results obtained with the subroutine varpro to compute the total capacitance of the signal wire with the parameterization given in (6.13).

4. The subroutine fun.c: The C implementation of functionals F and P. This subroutine calls the programs LR3.c and Capa.c, and returns the value of the functional F.

5. The driver program TL.c: This is the main program of the minimization problem. The program dialogs with the user to obtain the parameters and the functional is minimized. Results are output.

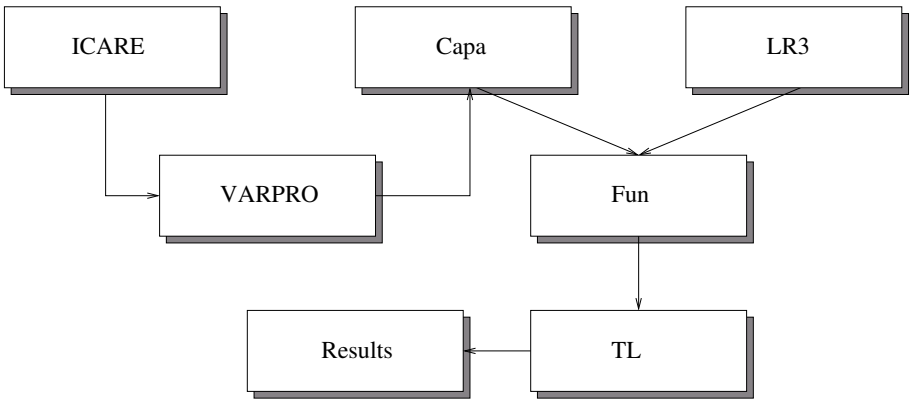


Figure 6.14: All the tools.

6.5.3 Results

We solve the two nonlinear equations $F = 0$ and $P = 0$ using Newton's method [50]. We approximate the derivatives using finite differences, approach that is tractable since the evaluation of the functionals is computationally inexpensive. To ensure the convergence from any initial point we include the method of bisection [50], at a small extra computational cost.

Some results are displayed in table 6.2. For all configurations we set $t = 0.65$ μm and we use *Cu* for conductors.

The table can be read as follows: Consider ID number one. We fixed L the common length of the three wires to be 2500 μm, the driver circuit has $R_{tr} = 100\Omega$ and the width of the signal wire is fixed at 6 μm. For a separation between the edge of the signal wire and the edge of either ground wire given by $s = 2\mu$m, there is a continuum of solutions for the width of the ground wires starting at 5.3μm and ending at 59.0μm. On

Table 6.2: Some Results

ID	L (μm)	$R_{tr}(\Omega)$	w (μm)	g (μm)		s (μm)	
				$s = 2\ \mu$m	$s = 5\ \mu$m	$g = 6\ \mu$m	$g = 8\ \mu$m
1	2500	100	6.0	[5.3, 59.0]	(*, *)	[0.28, 4.0]	[0.26, 4.0]
2			8.0	[5.3, 83.0]	(*, *)	[0.27, 4.5]	[0.26, 4.5]
3			10.0	[5.3, 756.0]	[5.3, 314.0]	[0.31, 20.0]	[0.29, 22.0]
4		150	6.0	[5.3, -)	[5.3, 1105.0]	[0.5, 34.0]	[0.45,37.0]
5			8.0	[5.3, -)	[5.3, -]	[0.49, 41.0]	[0.45, 44.0]
6			10.0	[5.3, -)	[5.3, -)	[0.91, 560.0]	[0.77, 621.0]
7	5000	100	6.0	[5.3, 58.0]	(*, *)	[0.37, 4.0]	[0.34, 4.0]
8			8.0	[5.3, 81.0]	(*, *)	[0.35, 4.5]	[0.33, 4.5]
9			10.0	[5.3, 653.0]	[5.3, 291.0]	[0.42, 20.0]	[0.38, 21.0]
10		150	6.0	[5.3, -)	[5.3, 892.0]	[0.78, 34.0]	[0.66, 36.0]
11			8.0	[5.3, -)	[5.3, -)	[0.71, 40.0]	[0.62, 43.0]
12			10.0	[5.5, -)	[5.3, -)	[1.9, 515.0]	[1.6, 566.0]
13	10000	100	6.0	[5.3, 57.0]	(*, *)	[0.71, 4.0]	[0.8, 4.0]
14			8.0	[5.3, 80.0]	(*, *)	[0.6, 4.5]	[0.5, 4.5]
15			10.0	[5.3, 643.0]	[5.3, 288.0]	[1.2, 20.0]	[0.81, 21.0]
16		150	6.0	[7.6, -)	[5.3, 874.0]	[2.3, 33.0]	[1.9, 36.0]
17			8.0	[5.7, -)	[5.3, -)	[2.0, 40.0]	[1.6, 43.0]
18			10.0	[23.0, -)	[5.6, -)	[4.8, 497.0]	[4.0, 544.0]

Note: We take $s_{min} = 0.2\ \mu$m and $w \geq 5.3\ \mu$m (to upper bound DC wire resistance by 50Ω/cm.) '-' means that the corresponding variable is bounded by $g < 0.1\lambda$ and (*, *) means not feasible. ID is a identification tag used as reference.

the same column, for the separation between the signal wire and the ground wires of 5μm there are no feasible solutions. On the next column, for ground wire width equal to 6μm the corresponding interval in the separation between the signal wire and either ground wire is from 0.28μm to 4.0μm. For the width of the ground wire equal to 8μm the corresponding interval in the s variable becomes: from $s = 0.26\mu$m to $s = 4.0\mu$m. The remaining of the table is straightforward to read.

These intervals represent valid configurations for signal propagation at the speed of light. They are continuous in terms of the independent variables and rich enough to permit a synthesis methodology.

6.6 Frequency-Dependent Effects

In general, RLC parameters are frequency dependent in accordance to well understood phenomena: proximity and skin effects and dielectric relaxation. The range of frequencies that we need to evaluate the frequency response is determined by the rise time of the signal. The frequency spectrum will contain appreciable content up to frequencies bounded by:

$$f_{max} = \frac{1}{\pi\, T_{rise}}. \tag{6.21}$$

The rise time T_{rise} is determined by technology and circuit considerations (e.g. $T_{rise} \approx 30$ ps at 130 nm.) The signal spectrum will be appreciable up to $O(10)$ GHz at 130 nm. We proceed to estimate the deviations from constant values for the electromagnetic parameters RLC due to skin and proximity effect.

We remind that the parameter that controls the skin effect, the skin depth δ, can be computed from [55]:

$$\delta = \sqrt{\frac{1}{\mu_0 \pi f \sigma}}. \tag{6.22}$$

To minimize its influence, meaning uniform current distribution throughout the transverse cross-section, we take the thickness of the metal layer $t < 2\delta$ with $\delta \approx 650$ nm for Cu at 10 GHz. There also exists the simultaneous need to minimize r which itself calls for thicker metal. A compromise of $t \approx \delta$ is what we use. In practice we set $t = 650$ nm. Simulations run using FastHenry permitted us to verify that skin effect

Table 6.3: Relative Decrease of Loop Inductance from Quasi-static to 10 GHz.

g (in μm)	% decrease in l
10	5.1%
15	5.2%
30	4.9%
50	4.5%

Note: $t = 0.65\mu$m, $w = 10\mu$m and $s = g$.

corrections are in fact negligible up to 10 GHz. With the help of process technology we can consistently prevent skin effect corrections at lower process dimension and higher frequencies by performing reverse scaling of the upper metal layers where the clock trees are layout.

With regards to capacitance, the dielectric response times are much shorter than the rise times of the fastest signals, demanding frequencies well above the upper limits we are presently considering.

On the proximity effect: Its main effects are to increase r and decrease l as f increases. The modifications to the constant parameter assumption can be significant for wide wires separated by short distances. Let us consider first the changes on l. Among the terms in (6.11) it is the partial self inductance contribution the most sensitive to proximity effects, the current on each wire tends to redistribute towards the surfaces closer to the neighbor wires. The classical quasi-static treatment of chapter 2 is replaced by FastHenry simulations. The partial self inductance for wires described on table 6.2, can decrease up to 4% from the quasi-static values when computed at frequencies near 10 GHz. On the other hand the variation in partial mutual inductance, over the same frequency range, is less than 1% for all the configurations displayed on Table 6.2. The combined effect is that the loop inductance decreases by less than 6% in going from the quasi-static values to 10 GHz. See table 6.3.

The relative variation of the resistance due to proximity effect is larger than the corresponding reactance variation. See table 6.4.

The net result on our solution space is that an increase of $r(\omega)$ and a decrease of $l(\omega)$ makes inequality (5.23) more restrictive.

We verify the impact on the solution intervals when proximity effects are included. We focus our attention on the solution intervals for s, the most suitable running vari-

Table 6.4: Relative Increase of Loop Resistance from Static to 10 GHz.

g (in μm)	% increase in r
10	25%
15	26%
30	26%
50	25%

Note: $t = 0.65\mu$m and $w = 10\mu$m.

Table 6.5: s_1 change in Table 6.2 when Proximity Effects are Considered.

ID	Previous s_1 (in μm)	New s_1 (in μm)
1	0.28	0.33
7	0.37	0.56
13	0.71	1.8

Note: $g = 6\mu$m.

able. We take a collection of configurations from table 6.2 and their respective solution intervals for s. We use FastHenry to compute the parameters r and l for a given value of s in the interval at the maximum frequency considered, 10 GHz. For these parameters we check if inequality (5.23) is satisfied.

The main modification for a given interval in s, (s_1, s_2), and given w and g is to increase s_1 so as to compensate in (5.23) the increase in r and the decrease in l. Furthermore, this compensation is more important for longer wires. See table 6.5.

The existence and nature of the solution intervals does not change. Moreover, the utilization of 3D field solvers does not undermine the efficiency of our approach that relies on the utilization of simpler algorithms during the iterative process. In fact, we need 3D field solvers basically to update the lower bound s_1 on the solution interval. The characteristic impedance Z_0 decreases with increasing frequency. This results in relaxation of (6.4) and consequently an increase in the upper bound s_2.

Feasible solutions at 130 nm for transmission line behavior do exist up to lengths L of the order of chip dimension (cm scale.) The upper limit depends on specific details of the technology and the particular wire under consideration (through r_s.)

Consider the technology scale down factor Λ with $\Lambda \approx 0.7$ from generation to generation. L_{max} is determined by the equality limit in (5.23). Both under ideal and

nonideal scaling (do not scale t)

$$L_{max} \approx \Lambda^2. \tag{6.23}$$

This implies that chip-length wires, at 90 nm and beyond will require repeaters to ensure transmission line behavior, just as they do in the RC domain to preserve linearity. With regards to L_{min}, whose value is determined by (5.40), its scaling behavior is given by $L_{min} \approx \Lambda$, making even shorter wires capable of undergoing transmission line propagation on scaled down technologies. At 130 nm, and $T_{rise} = 30$ ps we have this lower limit at about 2.2 mm, we expect this lower limit to be about 800μm at 45 nm.

We started our analysis from DM solutions with zero rise time, and constant RLC parameters. The frequency content of a Heaviside pulse extends from zero to infinity. In this open frequency interval, RLC parameters cannot be considered constant. Consistency in the formalism is restored once we properly account for the corrections due to nonzero rise time using (5.16) and (5.39). The presence of finite rise time chops the high frequency limit at current technology down to 10 GHz. This upper limit scales up as $1/\Lambda$. We have verified in previous sections the almost constancy of the electromagnetic parameters in the frequency regime under consideration for present technology. We have also verified that the perturbations to the constancy of the parameters only modifies the lower limits of the separation intervals. Since the transmission line representation, as given by solutions to (5.3), holds valid down to the regime where uniform current distribution is applicable, our treatment becomes a posteriori justifiable and self-consistent.

6.7 Presence of extra wires

We introduce among the spectrum of variables that can impact on our calculation, the addition of extra wires that could contribute to the current return path, e.g. external power/ground grids. The method described for a simple sandwich element generalizes to the presence of multiple (same length) ground wires, in the uniform current approximation, in the following way: The loop resistance of a signal wire connected to n ground wires in parallel becomes [45]:

$$r_{loop} = r_s + r_{GND}, \tag{6.24}$$

where $r_{GND} = (r_{g1}^{-1} + \ldots + r_{gn}^{-1})^{-1}$ and r_{gi} is the resistance of the ground wire i.

Similarly, the loop inductance becomes [45]:

$$l_{loop} = \sum_{i=0}^{n} \alpha_i \sum_{j=0}^{n} \alpha_j l_{i,j}, \tag{6.25}$$

with $\alpha_0 = 1$ and $\alpha_i = \frac{-r_{GND}}{r_{gi}}$ for $i > 0$.

Clearly, (6.24) and (6.25) become (6.8) and (6.11), respectively, for the sandwich element (1 signal, 2 grounds.)

The capacitance remains the same as in (6.12) since it is insensitive to the presence of non nearest neighbors ground wires on the same layer, due to shielding.

6.8 Solution space for an entire tree

We have in previous sections developed a method to find solution intervals for each branch (sandwich element) of an SBHT. We can use separability to compute the electrical parameters such that the whole tree operates in Region I. We have on the other hand omitted the effect of reflections on the solution space. Reflections occur at each physical discontinuity such as the T's on the tree. Reflections are rarely accounted for in the timing behavior of digital systems, an approximation that is no longer sustainable in the electromagnetic domain. Reflections are an unavoidable consequence of wave propagation phenomena.

Consider a T-junction. The magnitude of the reflection coefficient is proportional to the difference between signal line impedances at the T-junction. Thus, to eliminate the effects of reflection, the combined impedance of the downstream branches should be matched with the impedance of the upstream branch. The impedance of a branch is a function of its RLC parameters which can be altered by modifying the physical parameters of the branch. Such procedure does not alter the RLC parameters of other branches, since ground wire segments in one branch are sufficiently separated from signals in other branches not to perturb these signals' return path. Thus, by adjusting the appropriate physical parameters of downstream branches we could achieve the required impedance matching with the upstream branch. In this fashion we minimize the effects due to reflections. This process is performed iteratively over branches of the SBHT.

6.8.1 Reflections

Consider an SBHT of depth n. At each T-junction we have two identical branches in parallel, to equalize the impedance, and thus eliminate reflections, each one of the downstream branches must have twice the impedance of the upstream branch, i.e.:

$$Z_i = 2Z_{i-1} = \ldots = 2^i Z_1 \quad \text{for } i = 2, \ldots, n. \tag{6.26}$$

where the subindex i characterizes the depth of the tree.

Now,

$$Z_i = Z_{i,0}\sqrt{\frac{p + \frac{r_i}{l_i}}{p}}, \tag{6.27}$$

with $Z_{i,0} = \sqrt{\frac{l_i}{c_i}}$, and p the Laplace complex variable.

The following high frequency approximation is made: $Z_i \approx Z_{i,0}$. This is an accurate approximation for the high frequency part of the impedance. For $p = j2\pi f_{max}$ with $f_{max} \approx 10\,\text{GHz}$, the error in this approximation is small, getting even smaller as we move to higher frequencies. The propagation delay in Region I (see Fig. 5.8,) is governed by the time response during

$$0 \leq t \leq t_f + T_{rise}. \tag{6.28}$$

The upper limit of this interval is much lower than the settling time of the signal at the end of the line. Since we are only interested in the time period (6.28) to guarantee minimum delay, we are able to use the short time behavior of the signal. Due to well know theorems of Laplace transforms, the short time behavior of $V_{out}(t)$ is entirely dominated by the high frequency components of its transform. Henceforth we are well justified to make the replacement Z_0 for Z.

The above discussion also implies that at T-junctions we do not need to match DC resistance. Hence, we are free to keep, for routing purposes, common w and g on all branches. This feature constitutes an important advantage for clock tree routing purposes.

To minimize reflections, for fixed w and g, we vary s_i from one level of the tree to the next in such a way as to satisfy (6.26).[†] The modification demanded by impedance matching on our previous analysis translates into an iterative process. The first step

[†]We neglect effects due to vias present at the T-junctions, their dimension being negligible vis-a-vis the wavelength.

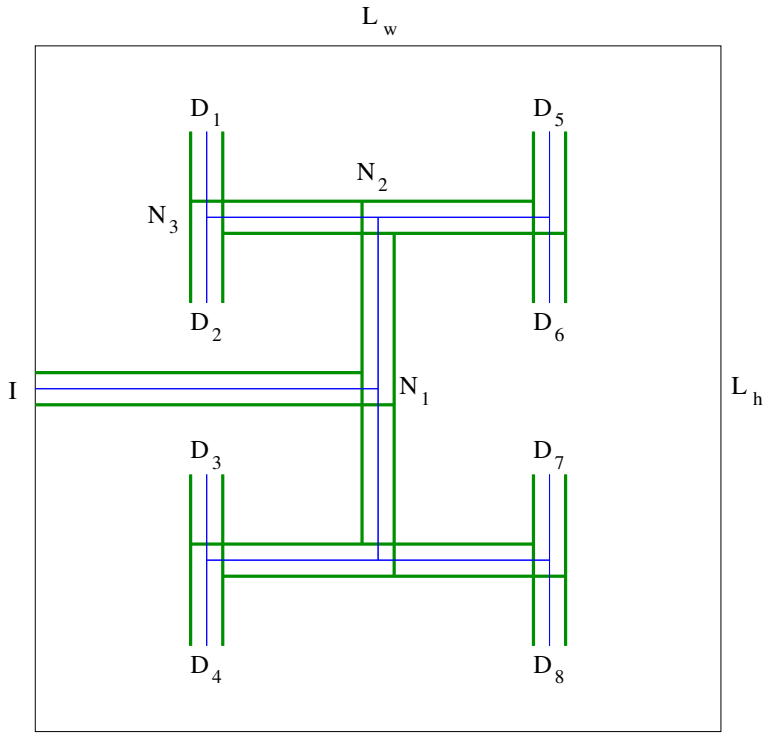


Figure 6.15: A SBHT example

consists of choosing a driver of strength R_{tr} feeding the main branch and find its solution interval $(s_{1,1}, s_{1,2})$. Choose a value s_1 belonging to this interval, subsequently find the values of s_i for the remaining levels using (6.26). Notice that the appropriate L that enters into (5.23) is the sum of the L's corresponding to the father plus those corresponding to the sons up to the leaf. We denote this length as L_n.

The computation proceeds as follows: We consider the SBHT as being just a branch of length L_n. We search for the minimum allowable s call it s_1. The appropriate values for the remaining branches s_i, are obtained by solving iteratively (6.26).

The process stops at iterate i if s_{i+1} is larger than a given maximum acceptable value (e.g. 0.1λ.) We update the values s_i restarting the process but with n redefined as $n = i$. This is to say we assume the tree has a depth i.

We proceed with a simple toy model, in which we generate a tree uniformly embedded in a rectangle, as shown in Fig. 6.15. For such tree, the length L_n is calculated using the following expression:

$$L_n = \sum_{i=1}^{n} L_{n,i}, \tag{6.29}$$

where

$$L_{n,i} = \begin{cases} \frac{L_w}{2^{\lfloor i/2 \rfloor + 1}} & \text{if } i \text{ is odd,} \\ \frac{L_h}{2^{i/2+1}} & \text{if } i \text{ is even.} \end{cases} \tag{6.30}$$

with L_w, L_h the dimensions of the rectangle where the SBHT is embedded (Fig. 6.15.)

We return to table 6.2. We assume that $L_h = L_w = 2L$. We found that for the regime of parameters considered, the maximum tree depth is $n = 3$ (two T-junctions.) For example, take the parameters of ID 1 with $g = 8\mu$m. Searching a configuration layout for $n = 4$, we obtain: $s_1 = 0.36\mu$m, $s_2 = 5.0\mu$m, $s_3 = 1422.07\mu$m and $s_4 = \infty$. For $n = 3$ the outputs becomes: $s_1 = 0.34\mu$m, $s_2 = 4.2\mu$m, $s_3 = 705.0\mu$m. This update step permits a significant area reduction ($\approx 50\%$) at the last level of the tree. Narrowing the signal line, permits the exploration of longer depths. These results are expected on general grounds: Except for small s, the rate of growth of $Z_{i,0}$ with s is slow, since the total capacitance c rapidly reaches an asymptotic constant value (the capacitance to the substrate and the other lower metal layers), while the loop inductance varies logarithmically as a function of s. It is expected then, that for deeper levels of the tree the resulting interwire separation becomes too large to be acceptable, since (6.26) demands an exponential growth of functions Z_i. The inability to continue to deeper levels can be overcame by using repeaters. The branches downstream from the repeater get effectively decoupled from the original problem. The method can be restarted from the repeater on as a new SBHT. The resulting configuration would be that of an SBHT with repeaters located at some T-junctions.

6.8.2 Repeater Insertion

The previous method looses efficiency beyond a few branches (typically two or three) due to the unacceptably large separations s demanded. To continue to deeper levels we use repeaters to be able to restart the algorithm, since the remaining levels of the tree will decouple in the presence of repeaters. The procedure continues until the overall length to be considered violates the lower bound (5.40) ($L = 1.5$ mm at 130 nm.) A full clock of course, needs to layout in such a way as to arrive to multiple no equidistant final destinations. This is achieved by the introduction of grid like interconnect in the

vicinity of receivers [60, 66]. The longer paths of the clock layout with SBHT, to be followed in the neighborhood of the receivers with grid like interconnect structures. The presence of the grid interconnect does not affect the results of this work, since the grids extend over a length scale bounded by $o(100)\mu$m length domain in which inductance effects are negligible. The delay contribution arising from these short branches can be adjusted by more traditional means such as resistance matching, and buffer insertion near the destinations, always necessary ingredients to minimize skew.

Inserting repeaters amounts to inserting a finite load capacitance C_{load}. To preserve the validity of transmission line behavior, load capacitance of the repeater must be small compared to line capacitance. The load capacitance can be adjusted by properly sizing the transistors on the repeater. The presence of repeaters adds some extra delay, that is typically small compared to the chip length line delay (expression (5.41)).

6.9 A Synthesis Example

For illustration purposes we include as example an SBHT that incorporates the synthesis methodology presented in this chapter.

The flow is as follows: We are given a square area of $L_w = L_h$, where an SBHT of depth n has to be embedded. We fix $n = 6$, $L_w = L_h = 2.4$ cm and assume a common metal layer thickness for the entire tree of $t = 0.65$ μm. The resistance of the device driving the tree is fixed to $R_{tr} = 80$ Ω.

As explained in Section VII, interwire separation s becomes unacceptable after a depth of two-to-three. To ensure acceptable separations at any level of the tree we construct the exemplary SBHT with repeaters every two levels. The branch lengths at each level of the tree are chosen based on (6.30).

We take for the first two levels common signal and ground width $w = 7\mu$m and $g = 14\mu$m, respectively. From (6.30), $L_{6,1} = 12$ mm and $L_{6,2} = 6$ mm. Solving both $F = 0$ and $P = 0$, the solution interval of separations for the first level of the tree results in $s = (0.7, 1.73)$ μm. We take as first separation $s_1 = 1.5\mu$m, thus providing a safety net against high frequency effects (see Section VI.)

Forcing impedance matching at the first T-junction results in a separation for the second level of the tree of $s_2 = 94.5\mu$m. We place repeaters of $R_{tr} = 80$ Ω at each of the two ends of this level and restart the procedure for the following two levels of the SBHT. Taking advantage of the decoupling, we are free to reduce the signal and ground

Table 6.6: Values of the physical parameters at each level of the tree

Depth i	$L_{6,i}$ (in mm)	w_i (in μm)	s_i (in μm)
1	12	7	1.5
2	6	7	94.5
3	6	5	2.
4	3	5	93.2
5	3	3	0.8
6	1.5	3	9.53

Note: $g_i = 2w_i$ and $t_i = 0.65\mu$m for all i.

widths in the following levels for further space saving. Alternatively, we could have kept the widths of the signal and ground wires for simplicity of the layout.

On the third and fourth level we take common signal and ground width $w = 5\mu$m and $g = 10\mu$m, respectively. Since two branches are connected in parallel to the repeater the effective resistance of the repeater is twice its nominal resistance, i.e. $R_{tr} = 160\ \Omega$. From (6.30), $L_{6,3} = 6$ mm and $L_{6,4} = 3$ mm. The corresponding solution interval for the third level is then $s = (1.6, 33.7)\ \mu$m. Using $s_3 = 2\ \mu$m and forcing impedance matching results in a separation $s_4 = 93.2\mu$m for the fourth level. We place eight new repeaters with $R_{tr} = 80\ \Omega$ and restart for the last step of the procedure. For the fifth and sixth level $w = 3\mu$m, $g = 6\mu$m, $L_{6,5} = 3$ mm and $L_{6,6} = 1.5$ mm. The corresponding solution interval is $s = (0.62, 6.2)\ \mu$m. We take $s_5 = 0.8\ \mu m$ and impedance matching leads us to $s_6 = 9.53\mu m$.

In table 6.6 we summarize the resulting separations and the other physical parameters for each level of the tree.

This SBHT has 32 source-destination paths of length $L_6 = 3.15$ cm, with repeaters every two levels, and 32 endpoint receivers. Local wiring can be attached to these 32 endpoint receivers to properly feed the logic.

For deeper levels of the tree, s decreases, which indeed ensures the absence, at these levels, of unexpected large mutual inductance coupling between the branches which might jeopardize the validity of the cascade rule (see section 6.10.)

To make the example more realistic, we embed it on a power-ground grid. We of course preserve our dedicated ground wiring for the clock signal, albeit we incorporate the grid layout for standard power delivery.

We use FastHenry to simulate the effects of the power-ground grid on the vicinity

Table 6.7: Change in loop resistance and loop inductance when a ground grid is included

Config.	(R,L) at 1 GHz	(R,L) at 10 GHz
Without grid	(195 Ω,15.6 nH)	(233 Ω,15.5 nH)
Including grid	(191 Ω,16.1 nH)	(229 Ω,15.4 nH)

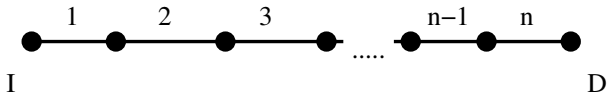


Figure 6.16: Labeling of a path, from source I to destination D.

of a a complete SBHT.

Consider two configurations, one with the SBHT and no grid, and the other, a worst case configuration, consisting of the SBHT in the presence of a same layer grid with an interwire separation of 300 μm. Results in table 6.7 show that both loop resistance and loop inductance of the tree are modified by the presence of the grid by a maximum of 3% for frequencies starting at 1 GHz.

The domains of validity of region I are essentially unaffected, since in addition, the capacitance coupling to the signal is essentially unaffected by the presence of these extra wires due to total screening.

The SBHT is a stable layout structure capable of transmitting signals efficiently, provided they are adequately driven.

6.10 inductance cascade rule

We prove the cascade rule for the loop inductance of any path in an SBHT. For convenience we label a path consisting on n branches as in Fig. 6.16. Each edge in the graph represents a sandwich element.

We denote as $i-j$ the path that starting at edge i includes all branches up an including edge j; $\mathcal{L}_{i-j}$ the loop inductance of the path $i-j$; $\mathcal{L}_{i-j,k}$ the mutual inductance between the path $i-j$ and branch k; $\mathcal{L}_i$ the loop inductance of branch i; $\mathcal{L}_{i,j}$ the mutual inductance between branches i and j.

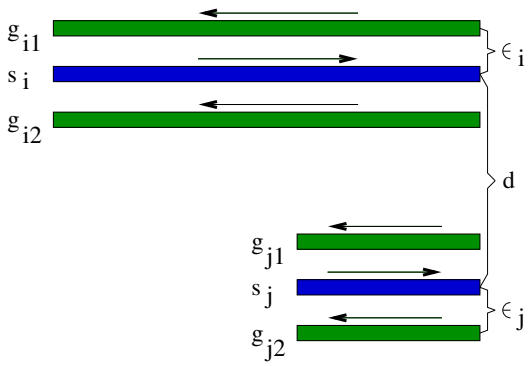


Figure 6.17: Two overlapping branches.

A straightforward application of (6.11) leads to the loop inductance of the path 1−2:

$$\mathcal{L}_{1-2} = \mathcal{L}_1 + \mathcal{L}_2 + 2\,\mathcal{L}_{1,2}. \tag{6.31}$$

Similarly for $n = 3$:

$$\mathcal{L}_{1-3} = \mathcal{L}_{1-2} + \mathcal{L}_3 + 2\,\mathcal{L}_{1-2,3}. \tag{6.32}$$

Using (6.31) and the fact that $\mathcal{L}_{1-2,3} = \mathcal{L}_{1,3} + \mathcal{L}_{2,3}$,

$$\mathcal{L}_{1-3} = \mathcal{L}_1 + \mathcal{L}_2 + \mathcal{L}_3 + 2(\mathcal{L}_{1,2} + \mathcal{L}_{1,3} + \mathcal{L}_{2,3}). \tag{6.33}$$

it is immediately apparent that for the general path $1-n$

$$\mathcal{L}_{1-n} = \sum_{i=1}^{n} \mathcal{L}_i + 2 \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} \mathcal{L}_{i,j}. \tag{6.34}$$

Now, $\mathcal{L}_{i,j}$ includes mutual inductance between orthogonal sandwich elements which are zero. We examine the leading term that gives the largest contribution to the previous sum, since it provides maximum overlap between the two loops.

Fig. 6.17, which in terms of partial inductance reduces to:

$$\begin{aligned}\mathcal{L}_{i,j} =& l_{s_i,s_j} \\ &+ \frac{1}{4}(l_{g_{i1},g_{j1}} + l_{g_{i1},g_{j2}} + l_{g_{i2},g_{j1}} + l_{g_{i2},g_{j2}}) \\ &- \frac{1}{2}(l_{g_{i1},s_j} + l_{g_{i2},s_j} + l_{g_{j1},s_i} + l_{g_{j2},s_i})\end{aligned} \tag{6.35}$$

with $l_{i,j}$ the partial mutual inductance between wires i and j.

We use narrow wire approximations on this simplified analysis. The results can be recasted in terms of GMD's.

The expression for $l_{i,j}$ derived from (2.40) with $L^2 >> d^2$ is

$$l_{i,j} = \frac{\mu}{2\pi}\left(\ln\left(\frac{2L}{d}\right) + \frac{d}{L} - 1\right) \tag{6.36}$$

Substituting this expression in (6.35) results in

$$\begin{aligned}&\mathcal{L}_{i,j} = \\ &\frac{\mu}{4\pi}\left[\frac{1}{2}\ln\left(\left(1 - \frac{\epsilon_i^2}{d^2}\right)\left(1 - \frac{\epsilon_j^2}{d^2}\right)\right)\right. \\ &\left.-\frac{1}{4}\ln\left(\left(1 - \frac{(\epsilon_i - \epsilon_j)^2}{d^2}\right)\left(1 - \frac{(\epsilon_i + \epsilon_j)^2}{d^2}\right)\right)\right]\end{aligned} \tag{6.37}$$

with d the distance center-center between the two signal wires s_i and s_j; ϵ_i and ϵ_j the signal-ground distance at sandwich element i and j, respectively.

Since $\epsilon/d < 1$, (6.37) is well approximated to

$$\mathcal{L}_{i,j} \approx \frac{\mu(\epsilon_i^4 + \epsilon_j^4)}{2\pi d^4}. \tag{6.38}$$

The distance d is generally $O(1)$ mm while the distances ϵ_i and ϵ_j are $O(10)\mu$m. Therefore the mutual inductance between two parallel branches in a path of an SBHT is negligible. The reader can verify using the same approach that the remaining terms in the sum (6.34) are also negligible. This is to be expected on physical grounds, since these terms correspond to mutual inductance between two magnetic dipoles. This completes the verification of the cascade rule.

6.11 Concluding remarks

We propose a natural way to exploit inductance, using sandwich configurations with controllable return paths and low impedance drivers and repeaters, to sustain speed of light propagation in the medium and the absence of undesirable overshoots. We develop a methodology to obtain appropriate values for the parameters of the lines and drivers. The technique, that is computationally efficient, can be used in synthesis of clock trees. The amount of real estate necessary in upper metal layers is reasonable, maximum separations at 130 nm can be made smaller than 100 μm.

The synthesis method is the result of rigorous analysis based on transmission line representation exact equations. The resulting wire configurations, for particular driver strengths and signal rise times behave as transmission lines.

The signal delay associated with the configurations is stable with respect to process variations, unlike an RC system whose diffusion delay is very sensitive to the exact values of the process parameters. It is the constancy of the speed of light the source of stability. To ensure a safety net with regards to process variations, it suffices to choose as initial configuration one whose s is sufficiently separated from s_1 so as to guarantee that under any combination of process fluctuations the lower limit will not be violated. The upper limit s_2 is easily controllable.

We carefully examine most known factors that could impact on our analysis such as perturbations due to power-ground grids on the RLC parameters, and frequency dependence of the same electromagnetic parameters.

We verify the almost constancy of the electromagnetic parameters in the frequency regime under consideration for $f \leq 10GHz$. We develop simple and yet accurate techniques permitting the calculation of l, c in CPU times usually attributable to extractors rather than field solvers, keeping the precision of the latter. We verify that the perturbations to the constancy of RLC only modifies lower limits of the separation intervals, barely affecting our synthesis strategy.

Moreover, it is well known that, with scaling accompanied by growth in overall chip dimensions, full chip synchronization is at a crossroad. Our approach to find configurations whose wire delay is dictated by speed of light propagation finds a natural set of applications in local and global clock design. It helps a bit, in making the clock period easily predictable, significantly less dependent on process parameter variations. A separate analysis including nonlinearities associated with drivers and receivers is forth-

coming, issues such as repeater locations, strength, input and output impedance and skew control will be discussed elsewhere, so will be the sensitivity to process variations.

We found that working in the time domain and exploiting monotonicity of the functionals were paramount in the current study. The classical alternative to our approach is to pose the problem in the frequency domain, with parameters that are frequency dependent and perform the inverse Laplace transform numerically. This alternative approach is loaded with numerical instabilities, that we could avoid. Given the monotonicity properties of the functionals that determine the allowed intervals, the frequency domain approach can be avoided.

Chapter 7

Conclusions

We considered reserving this chapter for apologies explaining what went wrong, how could we do it better if we had four more years, and things of that nature. In a rather remarkable fashion the technology we developed does significantly better than the alternatives coming from Sequence, Cadence/Columbia and Synopsys. Maybe we can omit the apologies. We have, on the other hand, some saying into what would amount to be desirable problems to solve to improve our understanding on the subject matters discussed in this dissertation. We start by refreshing the state of the art in dynamic impedance extraction when this work started in 2002, while in passing inserting newer developments from our competitors in academia and industry. As of 2002 and before, Sequence submitted their first patent applications to 3D loop inductance treatment. Work that included no frequency dependent behavior for resistance or inductance. Sequence's technology requires external calibration for each process. Any and all wires in the design are included, technique that results in the output of large amounts of superfluous data. Model Order reduction techniques were not and are not on their toolbox kit. Sequence main merit: being first at releasing a product. Not a technological contender in terms of accuracy or predictive power. Columbia researchers [18, 67], working with Cadence introduced a well thought approach to inductance extraction. A key ingredient in their approach is a partitioning strategy into a set of disconnected regions generated by "halos" as briefly discussed in chapter 3. The halo technology is touted as one that preserves passivity. No poles with negative real part in the complex s plane. This observation is made without proof. Plausibility comes about in the following way: Each three dimensional region that the halo construct generates has on its boundaries ground wires or the continuation of ground wires, no signal wires on the boundary. Signal wires

couplings to other signals in different regions are arbitrarily set to zero, even if the regions have a common boundary. These configurations, would otherwise generate the largest mutual couplings, making them the leading candidates to violate the diagonal dominance in the inductance matrix.

Computation of the R,L loop matrices is done within each interaction region, in a 3D formalism. Their partitioning mechanism and ours are notably different. In our formalism, we can in most cases quantitatively determine that we are dropping negligible terms. Both the tube construct around the victim wire, and the inclusion of a number of return wires well beyond nearest neighbors, leads to a ratio of mutual loop inductance to self loop inductance that falls off as a power of the separation [49, 68]. Neglecting mutual couplings beyond a tube interaction region is thereby justifiable. On the other hand, we face the curse of long range couplings. These terms are unavoidable and necessary in our treatment, so diagonal dominance will not be present, since for example, when signal wires share a return path, the fall off on the mutual inductance with distance is only logarithmic, and its ratio to the self inductance can be close to one. When our treatment and PEEC are compared for accuracy, as in chapter 3 and as in a recent independent validation, we feel comfortable with our results (Fig. 3.22-3.24). In practice we found that the possible presence of poles with real part negative, while close to zero, barks but does not bite. Neglecting pole contributions with the wrong sign does not impact the quality of the frequency response, except of course at very low frequencies, which is immaterial.

Comparing our treatment to PEEC [7] for all but toy examples is almost unfair. The PEEC approach does not scale. It requires keeping the entire system of wire segments for the whole design in a huge dense matrix, and then attempt to solve this system, an n^3 complexity problem. We replace this problem with a large collection of very small problems. The relative performance advantage of our method is simply overwhelming. The follow ons to PEEC, in terms of inverse methods, now employed by Synopsys, do not fare better. They need to invert the full matrix, and then neglect, or partition, invert and then neglect, with the second approach not quite developed in the literature.

7.1 Contributions and forthcoming additions

What have we added to the knowledge base of the community? The core engine is a reliable engineering tool, but not an original contribution. Our conception and im-

plementation of the loop approach in chapter 3 is new and physically meaningful. We personally cannot claim credit for most of the system level features, such as the geometrical engine to bound the search for nearby grounds and signals. That particular engine has been engineered by colleagues in our design to silicon engineering division. The system level performance of the flow is positively impacted by the work of another member of our division who developed a Model Order reduction engine, that reduces the size of the netlist to be simulated by nearly a factor of 100 [69–71].

Our tool [13] is capable of capturing frequency phenomena in wire impedance characterization for frequencies up to 50 GHz, that correspond to millimeter wavelengths in Si, significantly shorter than global wires. A full wave treatment of Maxwell Equations is mandatory for larger frequencies. Work in progress in this domain is taking place in our team [72]. Regarding other emerging concerns, substrate impact on impedance is one of the first that comes to mind. For frequencies below 15 GHz we have verified with FastHenry that our treatment can account for substrates, simply by treating it as a uniform plane of given thickness of low conductivity. This treatment parallels that of ground planes discussed in chapter 3. For higher frequencies, better methods are recommended, and are being studied by colleagues in our group [73]. Another natural extension is that of incorporating non-Manhattan routes in a loop formalism. The simplified bundle construct will loose most of its effectiveness. The decomposition into separate x and y routes is no longer tenable. The practical impact of these extensions can be localized typically to small analog features within a larger design. The core engine does not change. The problem as posed is not intellectually demanding but remains to be done.

Our incursion in the RF domain has two components of novelty. The first one is a simplified expression for the mutual impedance among two inductors or other passive devices (see equation (4.29)). The decoupling of the n-inductor problem into lower dimensionality single inductor problems with a simply computable correction factor to account for the dominant interaction, is a computationally efficient procedure. It is in fact a good approximation for not too closely coupled objects [9]. For short distances we compute the coupling using the full matrix. The second one is the RL+C approach we used for predicting the quality factor and impedance of intentional inductors is competitive in accuracy with full RLC field solvers (HFSS, Sonet, etc). It is more accurate than ASITIC, and the underlying description is simple and compelling. Our method demands the separate accurate computation of the capacitance matrix. This we do with

the help of the work of another team member [74, 75]. We can deal with problems of meaningful size to RF designers, which is a significant improvement over HFSS.

Our simple extension of the work of Davis and Meindl [54] in a direction that permits us to account for finite rise time and load capacitance effects, in predicting time delay for RLC lines (equation (5.41)) is novel and well quoted in the literature. Follow up approximations to our results were recently presented by researchers from UCLA [59]. While studying propagation delay in RLC interconnects we found some limited understanding of electromagnetic phenomena in IC's by members of the CAD community. In fact a number of contributors proposed time delay expressions for signals in the RLC domain, using a lump representation, as a π or T circuit. The conclusions deriving from such simplification are fully inadequate, for two basic reasons: the first one shown in chapter 5, that identifies the length of signals for which there is a manifestation of RLC effects, length that falls within the domain $L \geq \lambda/6$ that demands distributed representation. The transfer function for a distributed chain has a completely different high frequency behavior than the single lumped reduced circuit. RLC analysis at high frequency phenomena, is incompatible with reduced lumped RLC circuits, a low order representation valid for small frequencies.

Our contribution to the synthesis of clock trees: using inductance as a vehicle to propagate signals over chip level scale dimensions with signal delay proportional to the length of the wire. This is a novel idea, that addresses a problem mentioned at the introduction, we are referring to the dominance of the wire delay over logic delay as a key impediment to the continuous exponential growth of the performance curve. We mentioned in the introduction, that the exponential performance growth was well accounted for a system delay that is dominated by the transistor delay with wires being a perturbation. This is tantamount to a wire being represented as a contributor to the load capacitance. A valid description for short distances, and consistent with instantaneous propagation. Well for long wires, at current frequencies, finite effects of speed of light propagation are present. Our aim on this work is to propose one method to permit signal propagation on chip to travel as fast as is physically possible, the speed of light in the medium. It is one of the possible approaches to extend the visible life of increased performance to future technology nodes.

A more complete analysis of the clock problem including nonlinearities associated with drivers and repeaters in the presence of inductance is forthcoming, issues such as repeater locations, strength, input and output impedance and skew control will be

discussed elsewhere.

As an interesting note we point the reader to the fact that the new generation of microprocessors from IBM, the POWER6, includes an H-tree clock, working in transmission line mode [76]. This proves the applicability in real life of our contribution.

7.2 Engineering and commercial novelties

A patent protecting the clock tree application was granted in mars 2006 [12]. The patent protecting the impedance extraction in IC and the intentional inductors simulator was filed in February 2006 [8].

The self-impedance part of our impedance extractor for IC was released as a commercial tool in 2004 and followed a 1-year beta testing period. During this period, several customers validated the performance as well as the accuracy of our tool against their own results coming from measurements and from impedance simulators such as FastHenry. Following its commercial launch, the tool has been used in the design flow of RF devices by a well-known mobile phone company. It has been applied to problems in the digital domain, with designs containing several hundred of thousand transistors. The mutual impedance part of our tool was implemented in 2005 and launched in the same year. Customers doing noise analysis have been well impressed by its accuracy. A noise estimator that warns the designer if safe limits on magnetic noise coupling are violated is in Beta testing by customers. It is intended to be used for RF applications in exploring layout configurations consisting of multiple inductors. It has been validated, against measurements, by a customer in a Phase Locked-Loop (PLL) design. The n-inductor noise problem falls within the category of inherent parallel problems, a concurrent implementation in a shared memory environment is forthcoming.

7.3 Additional references

The following papers, patents and patents applications are related to this work:

- R. Escovar and R. Suaya, "Optimal design of clock trees for multi-gigahertz applications," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 23, no. 3, pp. 329– 345, Mar. 2004.

- ——, "Transmission line design of clock trees," in *Proc. IEEE/ACM International Conference on CAD*, Nov. 2002, pp. 334–340.
- R. Escovar, S. Ortiz, and R. Suaya, "Mutual inductance extraction and the dipole approximation," in *International Symposium on Physical Design (ISPD)*, April 2004.
- ——, "An improved long distance treatment for mutual inductance," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 24, no. 5, pp. 783–793, May 2005.
- ——, "Mutual inductance between intentional inductors: Closed form expressions," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006.
- R. Suaya, R. Escovar, S. Thelapurath, S. Ortiz, and D. Petranovic, "Extracting impedance effects from a circuit design using an electronic design automation synthesis tool," U.S. Patent application, Feb. 2006.
- R. Suaya and R. Escovar, "Synthesis strategies based on the appropriate use of inductance effects," U.S. Patent, number 7,013,442, March 2006.

Conclusion (français)

Nous avons voulu réserver ce chapitre pour nous excuser de ce qui a mal tourné et de ce que nous aurions pu améliorer si nous avions eu quatre années de travail supplémentaires. Cependant, la technologie que nous avons développée améliore de manière significative les solutions proposées par Sequence, Cadence/Columbia et Synopsys. Nous pouvons donc omettre les excuses. En échange, nous avons beaucoup de choses à dire sur les problèmes que l'on devrait résoudre pour améliorer notre compréhension des thèmes discutés dans cette dissertation.

Nous commençons par rappeler la situation dans l'extraction dynamique d'impédance quand ce travail a commencé en 2002, au même temps que nous ajoutons les nouveaux développements de nos concurrents dans le milieu universitaire et l'industriel parus durant la réalisation de ce travail. Déjà en 2002, Sequence avait soumis ses premières applications de brevet pour le traitement 3D de l'inductance en boucle. Ce travail n'incluait aucun comportement lié à la fréquence pour la résistance ou l'inductance. La technologie de Sequence exigeait le calibrage externe pour chaque processus. Tous les fils dans la conception devaient être considérés en même temps, ce qui aboutissait à la production de grandes quantités de données superflues car les techniques de réduction d'ordre n'étaient pas et ne sont toujours pas présentes dans leur outil. Le principal mérite de Sequence est d'être le premier à lancer sur le marché ce produit, bien qu'il ne soit pas un bon concurrent en termes d'exactitude ou de performance.

Les chercheurs de Columbia [18, 67], travaillant pour Cadence, ont présenté une approche bien conçue de l'extraction d'inductance. L'ingrédient principal, dans leur approche, est une stratégie de division dans un ensemble de régions débranchées, produites par des "halos", comme il en a été brièvement discuté dans le chapitre 3. La technologie de halo est sensée préserver la passivité des circuits, i.e., pas de pôles avec la partie réelle négative dans le plan s complexe.

Cette observation est faite sans preuve, mais sa plausibilité vient du fait que chaque

région tridimensionnelle, produite par les halos, a des fils de masse dans ses frontières et qu'aucun fil de signal n'est sur ces frontières. Des accouplements de fils de signal à d'autres signaux, dans différentes régions, sont arbitrairement égalisés à zéro, même si les régions ont une frontière commune. Ces configurations produiraient, autrement, les plus grands accouplements mutuels, qui sont les principaux candidats pour violer la dominance diagonale de la matrice d'inductance. Le calcul des matrices de boucle R et L est fait à l'intérieur de chaque région, en utilisant un formalisme 3D. Leur mécanisme de partition est différent du nôtre. Dans notre formalisme, nous pouvons, dans la plupart des cas, déterminer de façon quantitative, les couplages que nous négligeons. L'utilisation du tube d'interaction autour du fils victime, ajouté à la sélection d'un nombre de fils de retour, au-delà des deux plus proches, assure que le rapport d'inductance propre et d'inductance mutuelle décroît comme une puissance de la distance [49, 68].

Il est alors justifié de négliger les couplages inductifs au-delà du tube d'interaction. Malgré cela, nous sommes toujours soumis à la malédiction des couplages de longue distance. Ces termes sont inévitables et nécessaires dans notre traitement, donc la dominance diagonale ne sera pas présente, étant donné, par exemple, que quand deux signaux partagent le même fil de masse leur couplage décroît en fonction du logarithme de la distance, et le rapport avec l'inductance propre peut être approximativement égal à un. Quand nous comparons la précision de notre traitement avec celui du PEEC, telle qu'elle est montrée dans le chapitre 3, nous sommes satisfaits de nos résultats. Négliger la contribution de pôles avec le signe incorrect n'affecte pas la qualité de la réponse fréquentielle.

Il est injuste de comparer notre traitement avec celui du PEEC pour des exemples de grande taille. Pour le PEEC, il faut considérer tous les fils dans un énorme système linéaire dense et essayer de le résoudre. Nous faisons autrement en divisant le problème en petits sous-problèmes. L'avantage relatif des performances de notre méthode est accablant. Les améliorations existantes pour le PEEC, basées sur les méthodes inverses ne font pas mieux. Pour ces méthodes, il faut inverser la matrice, puis négliger des termes pour ensuite la réinverser.

Contributions et futures améliorations

Qu'avons-nous ajouté à la connaissance de la communauté? Notre noyau de calculs est un outil très fiable pour l'ingénierie, bien qu'il ne soit pas une contribution origi-

nale. Notre conception et notre réalisation de la méthode de boucle, présentées dans le chapitre 3 est une nouvelle contribution avec un vrai contenu physique. Nous ne pouvons pas prendre tout le crédit pour le développement de cet outil, la partie géométrique, qui reconnaît les fils, a été développée par nos collègues de la division “design to silicon”.

Notre outil [13] est capable de capturer les phénomènes fréquentiels dans l'impédance des fils, pour des fréquences allant jusqu'à 50 GHz, ce qui correspond à des longueurs d'onde d'un millimètre en silice (Si), beaucoup plus petites que les fils globaux. Un traitement complet des équations de Maxwell est nécessaire pour les plus hautes fréquences. Du travail dans ce domaine est déjà en progrès dans notre équipe [72]. D'autres facteurs intéressants à considérer sont les effets que le substrat peut avoir sur l'impédance des fils. Pour des fréquences de moins de 15 GHz, nous avons vérifié avec FastHenry que notre traitement pouvait prendre en compte le substrat comme un autre fil mais avec une résistivité beaucoup plus élevée. Cette façon de traiter le substrat est parallèle à celle de traiter les plans de masse, présentée dans le chapitre 3. Pour de plus hautes fréquences, d'autres méthodes plus précises sont nécessaires. Le travail sur ce sujet est aussi en progrès grâce aux collègues de notre équipe [73]. Une autre extension naturelle de notre méthode est celle qui consiste à incorporer dans notre traitement de boucle, le routage de fils non-Manhattan. Cependant, la séparation en x et y n'est plus possible, mais le noyau de calculs est capable de considérer des ” bundles ” avec des fils qui ne sont pas parallèles. Le problème n'est pas difficile à résoudre et sera fait ultérieurement.

Notre incursion dans le domaine des RF a deux directives : La première est l'expression simplifiée de l'impédance mutuelle entre deux inducteurs, ou celle d'autres dispositifs passifs (voir équation (4.29)). Le découplage du problème de n inducteurs en problèmes de plus petites dimensions est très efficace en termes de performance. La deuxième est le modèle RL+C, utilisé pour prédire la fréquence de résonance et le facteur de qualité d'un inducteur, comparable en précision à celle des outils RLC plus complexes (HFSS, Sonet, etc). Il est plus précis qu'ASITIC tout en gardant la même simplicité dans la description. Notre méthode demande le calcul précis de la matrice de capacités par un outil externe. Nous utilisons pour cette tâche un outil d'un autre membre de notre équipe [74, 75]. Nous pouvons traiter des problèmes de taille importante pour les concepteurs de RF, ce qui représente une nette amélioration vis-à-vis des outils comme HFSS.

Notre extension au travail de Davis et Meindl [54] , qui nous permet de considérer

un temps de montée du signal d'entrée différent de zéro, et une capacité de charge à la fin de la ligne, est nouvelle et a été très citée dans la littérature. Des approximations de notre résultat ont été récemment présentées par des chercheurs à l'UCLA [59]. Durant notre étude du temps de propagation en RLC, nous avons trouvé des membres de la communauté avec une connaissance limitée des phénomènes électromagnétiques. En effet, quelques-uns proposaient des expressions pour le délai d'un signal dans le domaine RLC en utilisant des modèles simplifiés, valables uniquement pour des longueurs d'onde très grandes, i.e. pour de très basses fréquences.

Notre contribution à la synthèse des arbres d'horloge : utiliser l'inductance pour assurer la propagation des signaux à la vitesse maximale, celle de la lumière dans le milieu. C'est une nouvelle idée qui vient répondre à la problématique présentée dans l'introduction, celle de la dominance du délai des interconnexions sur le délai des dispositifs. Notre contribution est une des nombreuses approches pour assurer un incrément de la performance dans les technologies futures.

Comme note intéressante, nous attirons l'attention du lecteur vers le nouveau processeur d'IBM, le POWER6, à paraître en 2007 [76]. Ce processeur contient un arbre d'horloge en H qui a été conçu de manière à assurer un comportement de ligne de transmission. Celui-ci démontre l'applicabilité dans la vie réelle de notre contribution.

Nouveautés commerciales

Un brevet sur l'application des arbres d'horloge a été adjugé en mars 2006 [12], ainsi qu'un autre brevet, sur notre méthode d'extraction d'impédance dans les circuits intégrés et des inducteurs intentionnels, a été déposé en Février 2006 [8].

La partie pour le calcul de l'impédance propre de notre méthode a été lancée sur le marché en 2004 après avoir suivi un an de période d'essai. Durant cette période, de nombreux clients ont pu valider nos résultats avec leurs propres résultats, provenant de mesures ou d'autres outils. Après le lancement commercial, l'outil a été utilisé dans la conception de dispositifs RF chez un constructeur très connu de téléphones portables. Il a aussi été utilisé dans le domaine numérique pour la conception de circuits intégrés avec plusieurs centaines de millions de transistors.

La partie d'impédance mutuelle a été lancée en 2005. Les clients intéressés par l'analyse du bruit dans les interconnexions ont été très impressionnés par la précision et l'efficacité de notre outil. Concernant les inducteurs, un outil de vérification a été

développé, permettant aux concepteurs de placer plusieurs inducteurs dans une même plaque, en s'assurant que le bruit entre les inducteurs ne dépasse pas une certaine limite. L'outil a été validé par un client en RF, en utilisant des mesures faites sur la conception d'une boucle à verrouillage de phase (PLL).

Références additionnelles

Les articles et brevets suivants ont été publiés durant la réalisation de cette thèse:

- R. Escovar and R. Suaya, "Optimal design of clock trees for multi-gigahertz applications," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 23, no. 3, pp. 329– 345, Mar. 2004.
- ——, "Transmission line design of clock trees," in *Proc. IEEE/ACM International Conference on CAD*, Nov. 2002, pp. 334–340.
- R. Escovar, S. Ortiz, and R. Suaya, "Mutual inductance extraction and the dipole approximation," in *International Symposium on Physical Design (ISPD)*, April 2004.
- ——, "An improved long distance treatment for mutual inductance," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 24, no. 5, pp. 783–793, May 2005.
- ——, "Mutual inductance between intentional inductors: Closed form expressions," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006.
- R. Suaya, R. Escovar, S. Thelapurath, S. Ortiz, and D. Petranovic, "Extracting impedance effects from a circuit design using an electronic design automation synthesis tool," U.S. Patent application, Feb. 2006.
- R. Suaya and R. Escovar, "Synthesis strategies based on the appropriate use of inductance effects," U.S. Patent, number 7,013,442, March 2006.

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